

OPERATION AND MAINTENANCE
MAINTENANCE SUPPORT
1XN FREQUENCY DIVERSITY
DR 6/11-135A
DESCRIPTION
CIRCUIT PACKS

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This practice contains a circuit description and symbolic block diagram for each circuit pack in the radio, line terminal bay, and regenerator bay. A diagram of each unit faceplate is under the "Controls, Jacks, Indications, and Options" tab.

This practice is reissued to update equipment descriptions. The practice is used in binder 421-101-001.

ISSUING ORGANIZATION

Published by the AT&T Documentation Management Organization.

210A MODULE—VOICE FREQUENCY CODER/DECODER

The 210A module (Fig. 1) provides encoding and decoding between voice frequency and digital 64-kb/s PCM (pulse-coded modulation). It has a 4-kHz bandwidth (VF), a standard input level of -16 dBm, and a standard output level of $+7$ dBm.

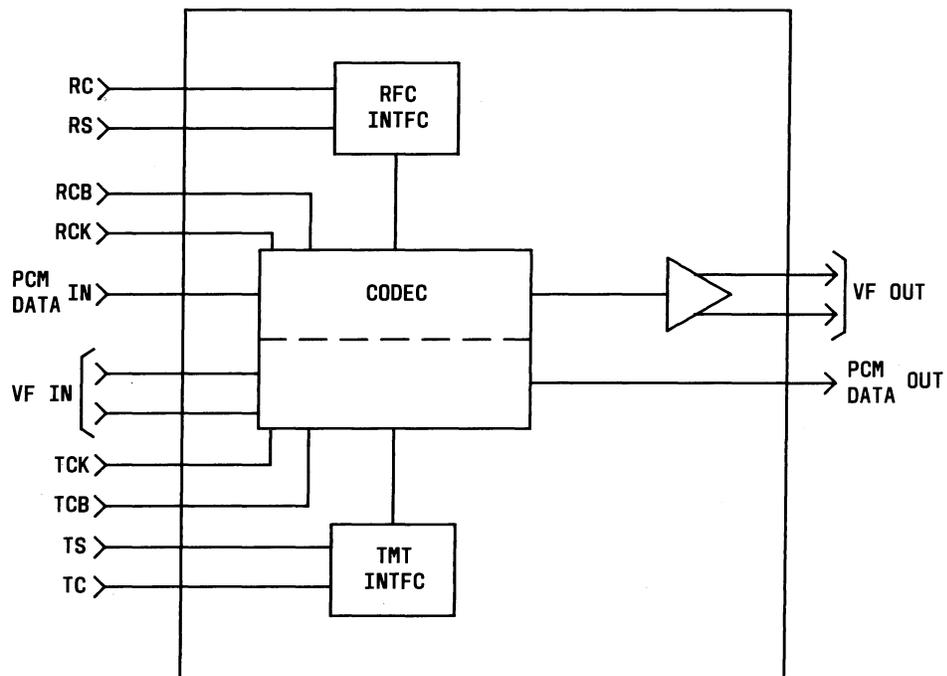


Fig. 1—210A Module—Voice Frequency Coder/Decoder

210B MODULE—4 x 16 KB/S

The 210B module (Fig. 2) serves as a demultiplexer/multiplexer from a 64-kb/s subchannel to four 16-kb/s RS-422 channels. Each RS-422 channel is capable of extending one E2A serial port to another station.

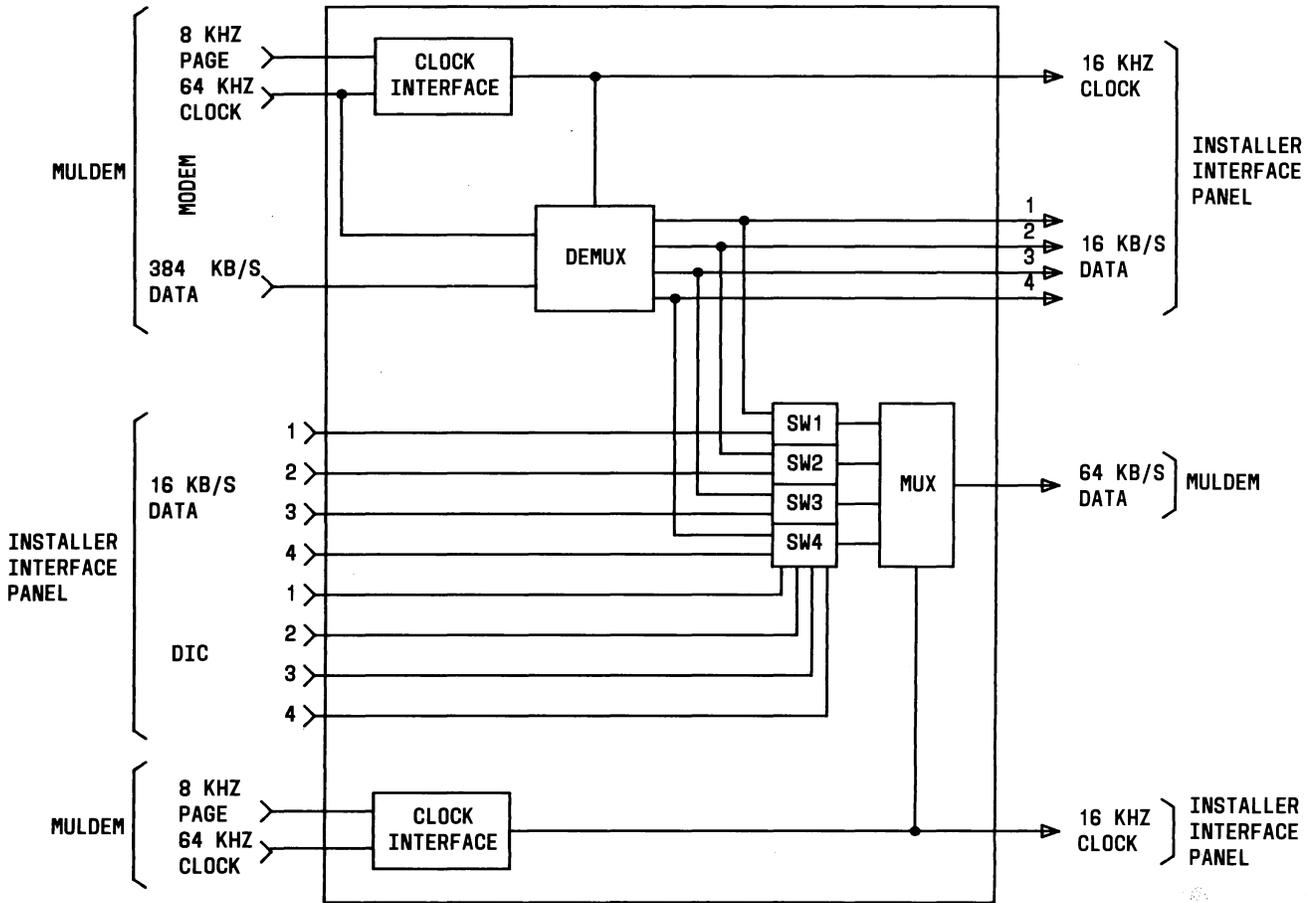


Fig. 2—210B Module—4 x 16 KB/S

210C MODULE—DAS EXTENDER

The 210C module (Fig. 3) provides an interface between E2A DAS telemetry equipment at one station and an RS-232C data set, or an equivalent device (by the service channel), at another station.

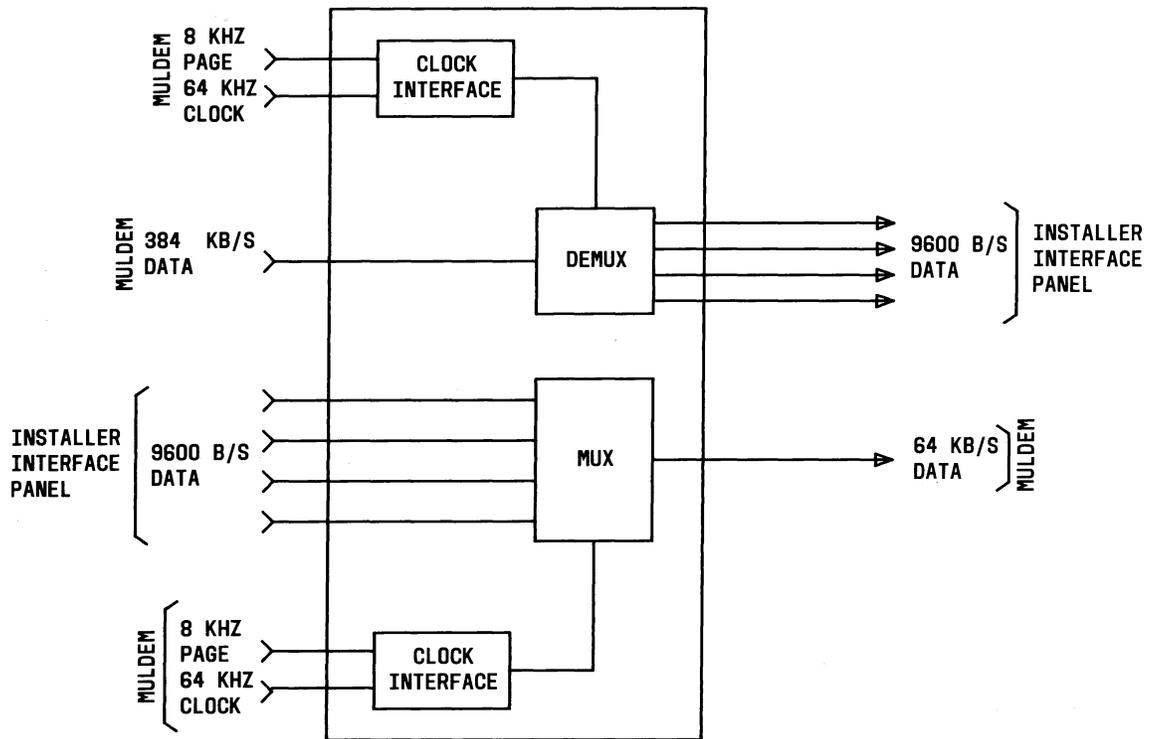
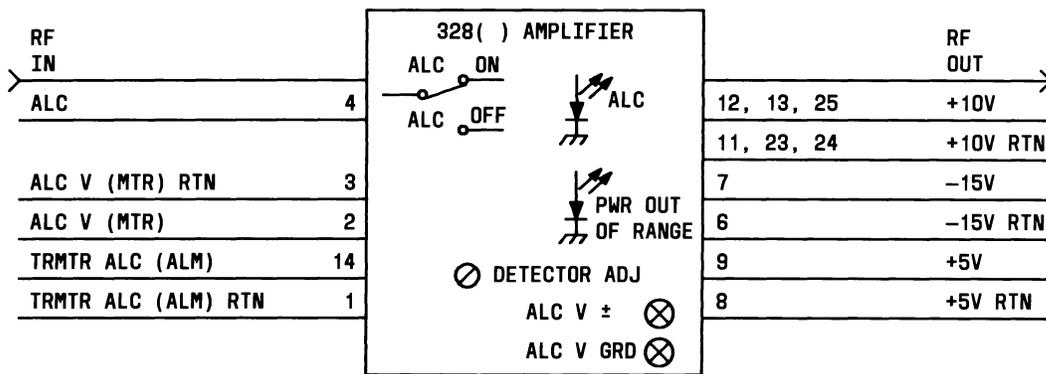


Fig. 3—210C Module—DAS Extender

328A AMPLIFIER (SOLID-STATE)

The 328A solid-state amplifier (Fig. 4) is used as the last stage RF signal amplifier in the radio transmitter. This unit is designed to operate over the entire 6-GHz common carrier band and has a typical gain of 43 dB. The following controls and/or indications perform the indicated functions:

- ALC ON-OFF switch Selects input to the ALC circuitry
- ALC LED Lighted when the ALC switch is off
- PWR OUT OF RANGE Lighted when the output power varies by more than 0.3 dB
- DETECTOR ADJ Used to null the voltage generated by the signal detector when the transmitter is adjusted for nominal output level
- ALC V ± & ALC V GRD ALC voltage test points.



NOTE:
 1. Numbers on leads are pin numbers of J6 which connects to the 328 Amplifier

Fig. 4—328A Amplifier (Solid-State)

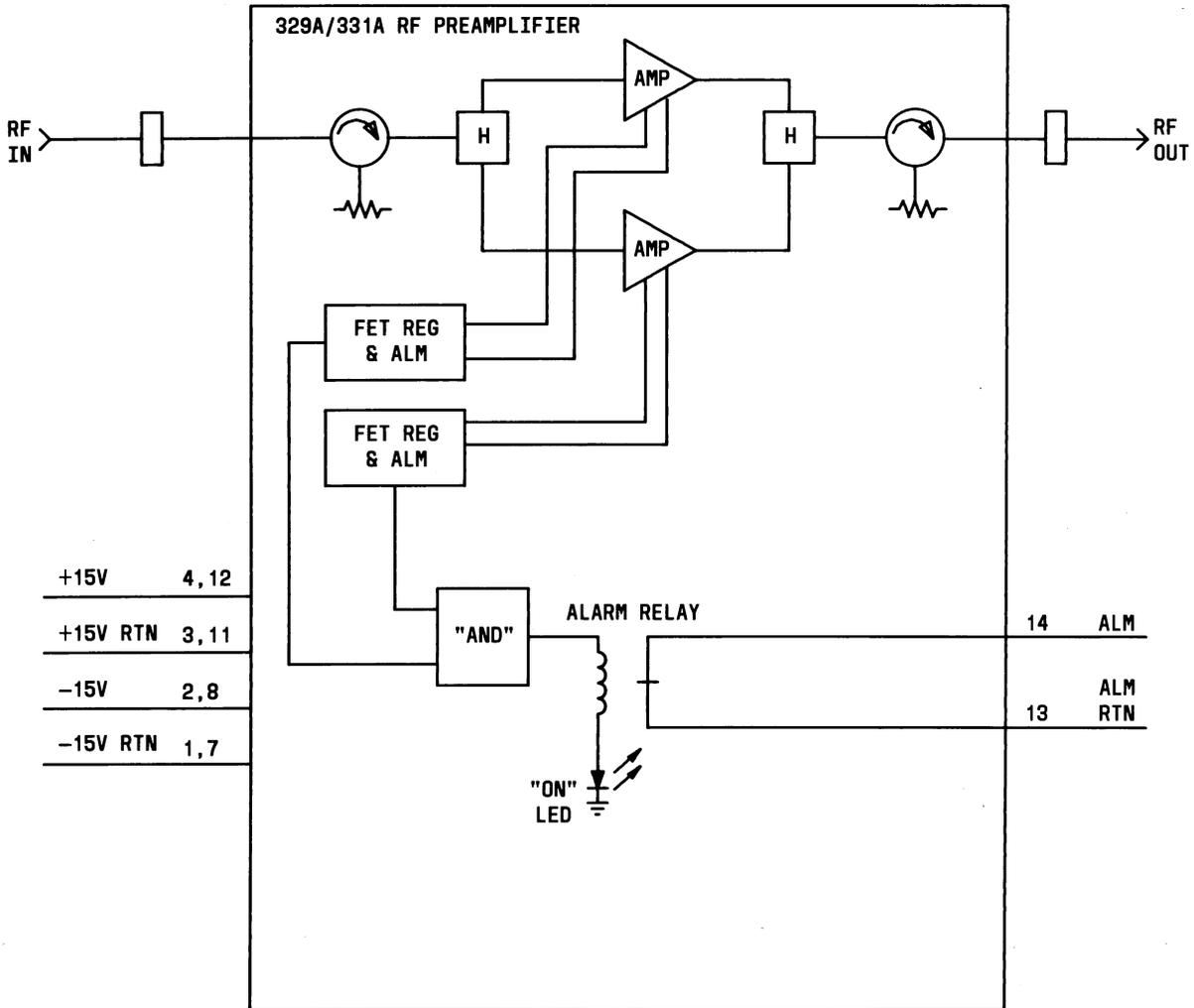
329A/331A RF PREAMPLIFIER (6 GHZ)

The 329A and 331A units (Fig. 5) are low-noise preamplifiers used to increase the system gain and to improve the noise figure of the radio receivers in long radio hops. Because these units operate over the full lower-six band, they are located in the common waveguide receiver run and amplify the signal to all of the receivers in a bay lineup. The gain of each amplifier is obtained by paralleling two gain stages powered from a common radio receiver or two separate radio receivers. These preamplifiers have a green LED that is *on* during normal operation.

The internal alarm circuits monitor the bias current of the individual gain stages. When there is deficient bias current or excessive bias current in a gain stage, a relay within the preamplifier provides a contact closure that activates the RF PRE AMP alarm on the ALARM AND METER unit and turns the green LED on the preamplifier off. The LED will also go off when the dc power plug is pulled. However, since in this case no contact closure is provided, the RF PRE AMP alarm is not activated and a silent failure results.

Some of the key preamplifier characteristics are as follows:

		NOMINAL (DB)	ONE GAIN STAGE FAILED (DB)
Gain (nominal)	329A	10	3
	331A	20	12
Noise Figure	329A	< 3.25	< 6.5
	331A	< 3.5	< 6.5



NOTE:
 NUMBERS ON LEADS ARE THE PIN NUMBERS ON THE
 PREAMPLIFIER PWR CONNECTOR

Fig. 5—329A/331A RF Preamplifier

471/474 BA POWER UNIT

The 471/474 BA POWER UNIT (Fig. 6) supplies either +5 V or -5 V power, depending on the strapping, to the terminal and regenerator circuit packs. The 471 unit is fed by a -24 V office supply. The 474 unit is fed by a -48 V office supply.

The power unit consists of an inrush current limiter, an input filter, a switching pulse-width-controlled power amplifier, output filters, and control circuits. The power unit latch contains an on/off switch that provides inrush protection and resets any latched protective shutdowns.

OFFICE SUPPLY	UNIT	OUTPUT
-24V	471BA	+5V OR -5V, DEPENDING ON STRAPPING*
-48V	474BA	

* UNIT ACTUALLY HAS BOTH OUTPUTS, BUT ONLY ONE IS USED.

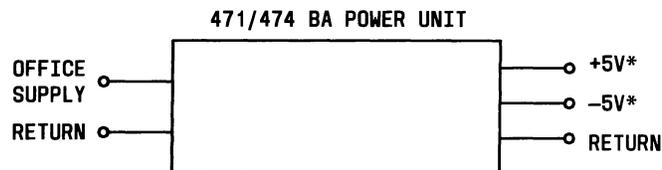


Fig. 6—471/474 BA Power Units

471/474 EA POWER UNIT

The 471/474 EA POWER UNIT (Fig. 7) supplies either +5 V or -5 V power, depending on the strapping, and +15 V and -15 V power to the terminal and regenerator circuit packs. The 471 unit is fed by a -24 V office supply. The 474 unit is fed by a -48 V office supply.

The power unit consists of an inrush current limiter, an input filter, a switching pulse-width-controlled power amplifier, output filters, and control circuits. The power unit latch contains an on/off switch that provides inrush protection and resets any latched protective shutdowns.

OFFICE SUPPLY	UNIT	OUTPUT
-24V	471EA	+5V OR -5V, DEPENDING ON STRAPPING* AND +15V AND -15V.
-48V	474EA	

* UNIT ACTUALLY HAS BOTH OUTPUTS, BUT ONLY ONE IS USED.

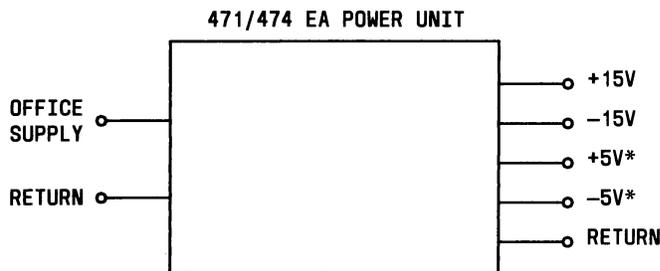


Fig. 7—471/474 EA Power Units

471/474 GA POWER UNIT

The 471/474 GA POWER UNIT (Fig. 8) supplies +10 V dc power to the solid-state amplifier. The 471 unit is fed by a -24 V office supply. The 474 unit is fed by a -48 V office supply.

The power unit consists of an inrush current limiter, an input filter, a switching pulse-width-controlled power amplifier, output filters, and control circuits. The power unit latch contains an on/off switch that provides inrush protection and resets any latched protective shutdowns.

OFFICE SUPPLY	UNIT	OUTPUT
-24V	471GA	10VDC
-48V	474GA	

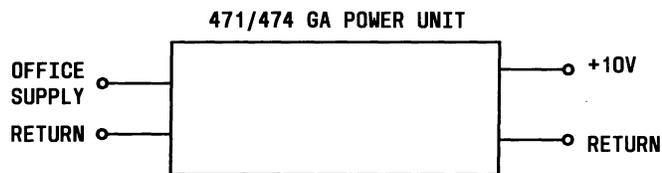


Fig. 8—471/474 GA Power Units

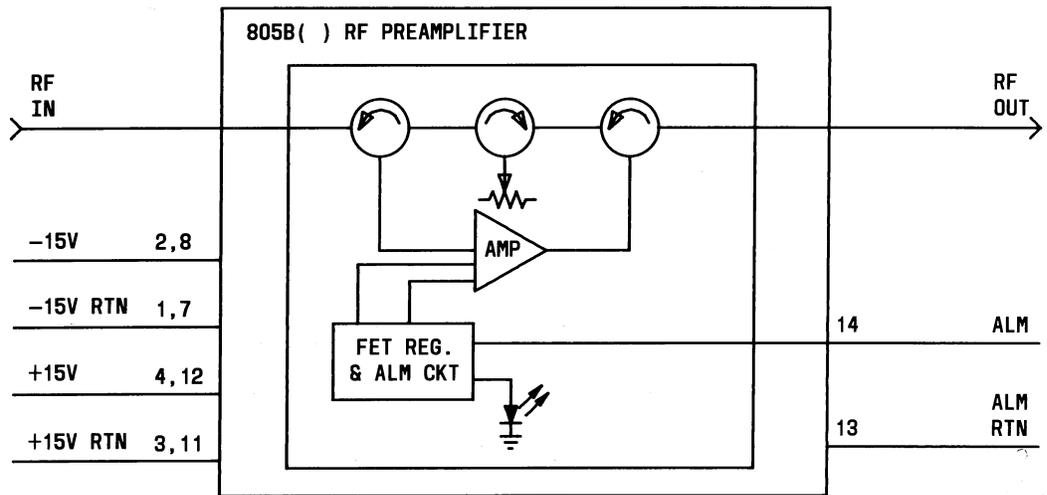
805B RF PREAMPLIFIER (11 GHZ)

The 805B unit (Fig. 9) is a low-noise preamplifier used to increase the system gain and to improve the noise figure of the radio receivers in long radio hops. This unit operates over the full 11-GHz frequency band and is located in the common waveguide receiver run. It amplifies the signal to all of the receivers in a bay lineup. The gain of this amplifier is obtained from one gain stage and is powered from two separate radio receivers.

The RF preamplifier has a green LED located on the unit that is ON during normal operation. The RF PRE AMP alarm monitors the FET (field effect transistor) bias current. When there is deficient bias current or excessive bias current, a relay within the preamplifier provides a contact closure that activates the RF PRE AMP alarm on the ALARM AND METER unit and turns the green LED on the preamplifier off. The LED will also go off when the dc power plug is pulled. However, since in this case no contact closure is provided, the RF PRE AMP alarm is not activated and a silent failure results.

Some of the key preamplifier characteristics are as follows:

	AMP OPERATING (DB)	AMP FAILED (DB)
Gain (nominal)	8.0	-20
Noise Figure	< 3.5	< 6.5



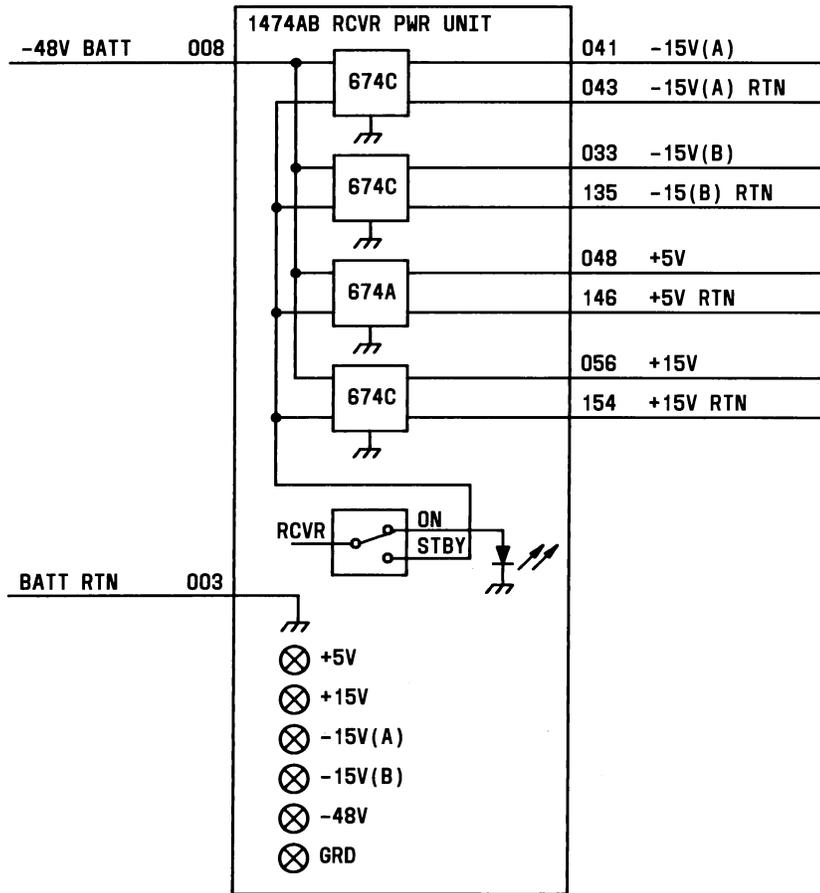
NOTE:
 NUMBERS ON LEADS ARE THE PIN NUMBERS ON THE
 PREAMPLIFIER PWR CONNECTOR

Fig. 9—805B RF Preamplifier

1474AB RCVR PWR

This unit provides +5 volts, +15 volts, and -15 volts to the receiver portion of the radio bay (Fig. 10). The required input voltage is -48 V (battery). Test points are provided to monitor the input and output voltages of this unit. The output voltages can be checked on the radio bay ALARM AND METER unit, if equipped.

In case of an interruption, this power unit automatically restores power to its output. An overload or the STBY/RCVR ON switch being set to the STBY position causes the unit to shut down. Depressing the STBY/RCVR ON switch to the RCVR ON position causes the unit to be powered up.



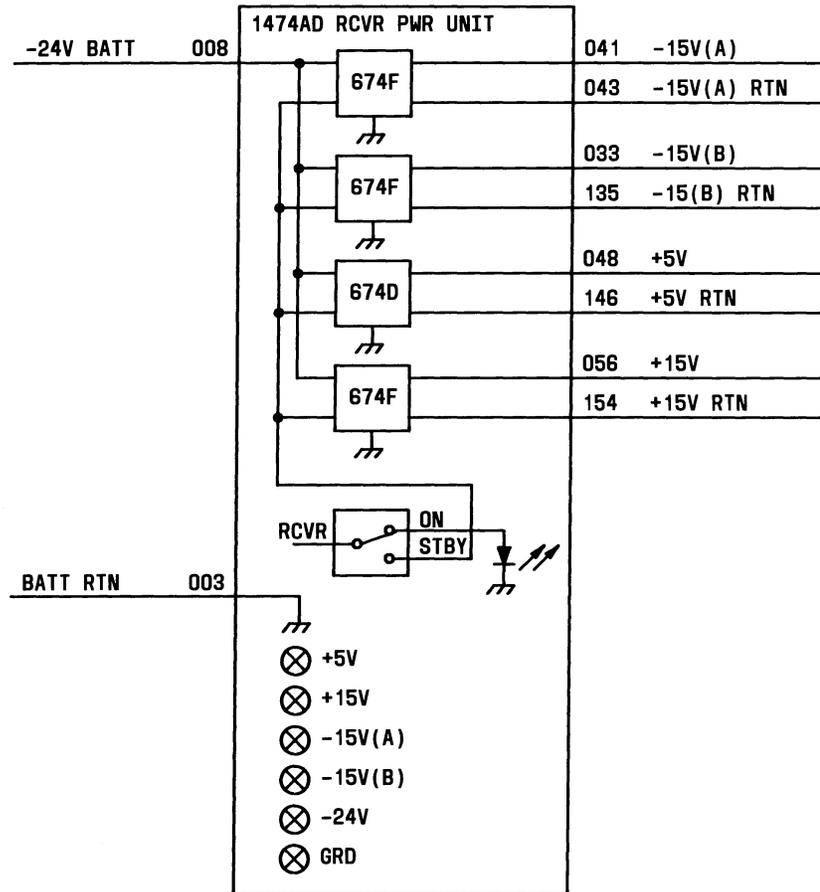
NOTE:
PIN CONNECTIONS ARE FOR P24 WHICH CONNECTS TO 1474AB RCVR PWR UNIT

Fig. 10—1474AB Receiver Power Unit

1474AD RCVR PWR

This unit (Fig. 11) provides +5 volts, +15 volts, and -15 volts to the receiver portion of the radio bay. The required input voltage is -24 V battery. Test points are provided to monitor the input and output voltages of this unit. The output voltages can be checked on the radio bay ALARM AND METER unit, if equipped.

In case of an interruption, this power unit automatically restores power to its output. An overload or the STBY/RCVR ON switch being set to the STBY position causes the unit to shut down. Depressing the STBY/RCVR ON switch to the RCVR ON position causes the unit to be powered up.



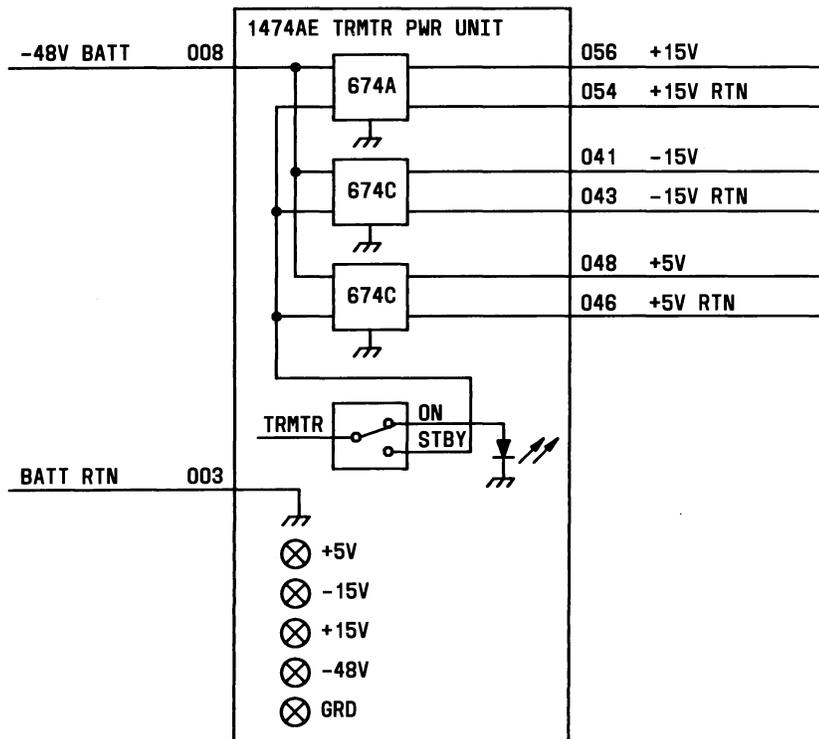
NOTE:
PIN CONNECTIONS ARE FOR P24 WHICH CONNECTS
TO 1474AD RCVR PWR UNIT

Fig. 11—1474AD Receiver Power Unit

1474AE TRMTR PWR

This unit (Fig. 12) provides +5 volts, +15 volts, and -15 volts to the transmitter portion of the radio bay. The required input voltage is -48 V battery. Test points are provided to monitor the input and output voltages of this unit. The output voltages can be checked on the radio bay meter, if equipped.

In case of an interruption, this power unit automatically restores power to its output. An overload or setting the STBY/TRMTR ON switch to the STBY position causes the unit to shut down. Depressing the STBY/TRMTR ON switch to the TRMTR ON position causes the unit to be powered up.



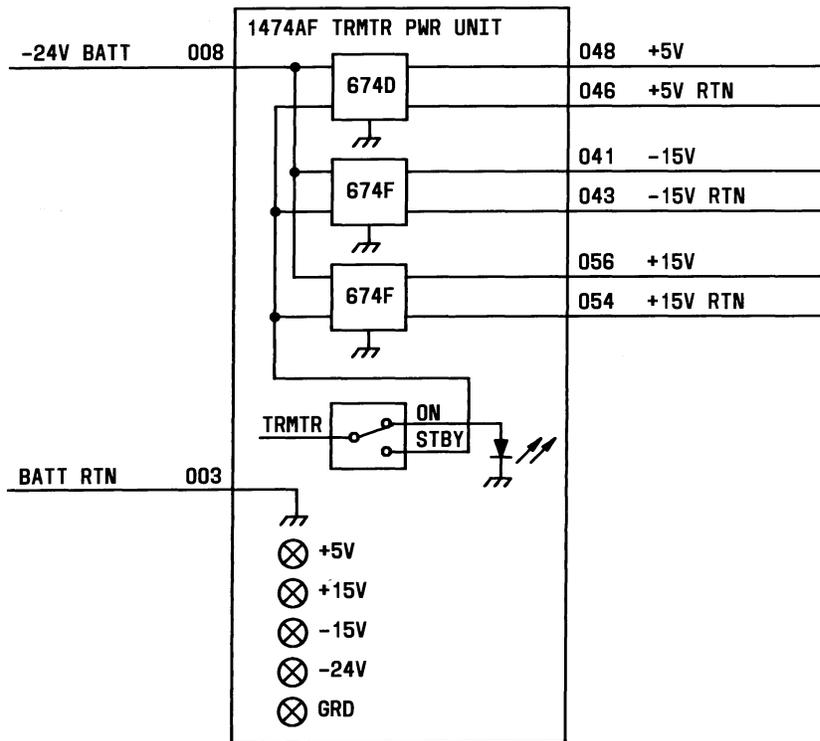
NOTE:
PIN CONNECTIONS ARE FOR P7 WHICH CONNECTS
TO 1474AE TRMTR PWR UNIT

Fig. 12— 1474AE Transmitter Power Unit

1474AF TRMTR PWR

This unit (Fig. 13) provides +5 volts, +15 volts, and -15 volts to the transmitter portion of the radio bay. The required input voltage is -24 V battery. Test points are provided to monitor the input and output voltages of this unit. The output voltages can be checked on the radio bay meter, if equipped.

In case of an interruption, this power unit automatically restores power to its output. An overload or setting the STBY/TRMTR ON switch to the STBY position causes the unit to shut down. Depressing the STBY/TRMTR ON switch to the TRMTR ON position causes the unit to be powered up.



NOTE:
PIN CONNECTIONS ARE FOR P7 WHICH CONNECTS
TO 1474AF TRMTR PWR UNIT

Fig. 13—1474AF Transmitter Power Unit

1477() ALARM/ALARM AND METER

The 1477C ALARM AND METER unit (Fig. 14) processes the alarm inputs from the associated radio T/R pair, displays local radio alarms, and generates up to three remote alarms. The 1477C also has the capability to monitor power supply output and control voltages via a rotary switch and digital meter located on the unit faceplate.

The 1477D ALARM unit functions identically to the 1477C, but without the monitoring capability.

When one or more receiver alarms are present, a remote RCVR ALM is generated. Similarly, a remote TRMTR ALM is generated whenever one or more transmitter alarms are present. Because the RF preamplifier is located outside the T/R bay, its alarm is processed separately. When present, the preamplifier alarm generates its own independent remote PRE AMP ALM. All remote alarms are initiated by providing a relay contact closure.

In some cases, incoming T/R alarms are delayed to avoid generating remote alarms due to atmospheric fading conditions. However, once a TRMTR or RCVR remote alarm is initiated, it is held or latched for at least 25 seconds to allow sufficient recognition time by the remote alarm reporting system. The faceplate of this network shows the presence of each radio alarm by means of a red LED. The relays used on this network are fail-safe, that is, if the dc power to the unit fails, the relays automatically initiate a remote alarm.

Except for the RF PRE AMP, BEAM FLT, and PWR ALM alarms, which provide a relay closure to indicate an alarm state, the circuits interpret the voltages that appear at their alarm input leads as follows:

Normal condition (no alarm):	-4 to -15 volts
Alarm condition:	-1 to +10 volts

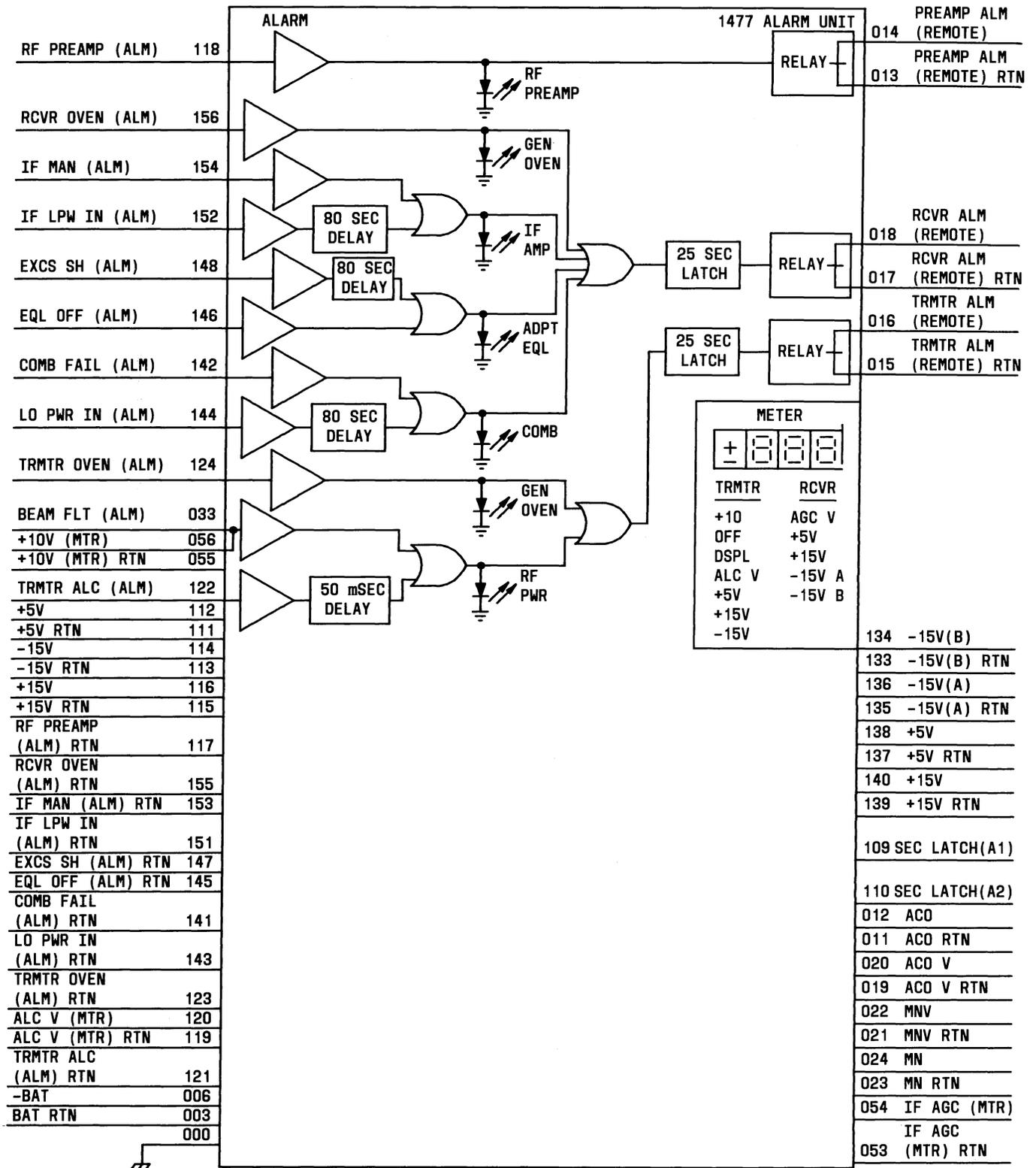


Fig. 14—1477C Alarm and Meter Unit

2003 () EQUALIZER ASSEMBLY

The 2003 equalizer assembly (Fig. 15) contains a 989() equalizer that is designed to operate in the 74-MHz frequency range. This assembly is used between the radio and regenerator or terminal equipment to control transmission frequency characteristics of the 74-MHz frequency panel by increasing loss with increasing frequency.

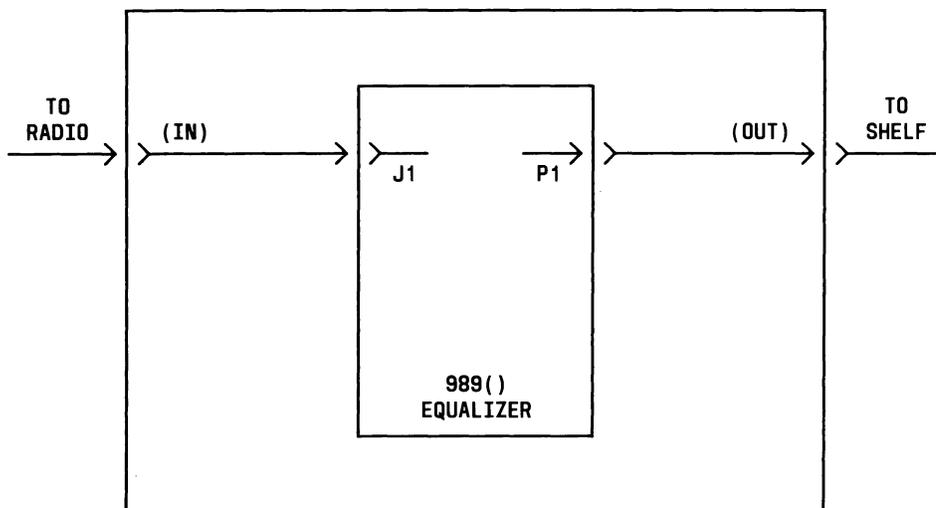
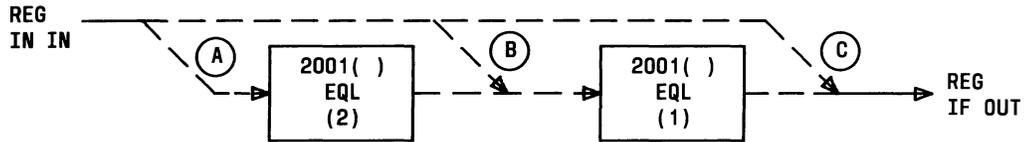


Fig. 15—2003 () Equalizer Assembly

4375A LINEAR DELAY EQUALIZER

The 4375A network (Fig. 16) can accommodate up to two 2001() linear delay equalizers. By selecting the appropriate equalizer code(s), the positive or negative linear delay slope of a radio hop can be corrected to within 1 nanosecond.

**NOTE:**

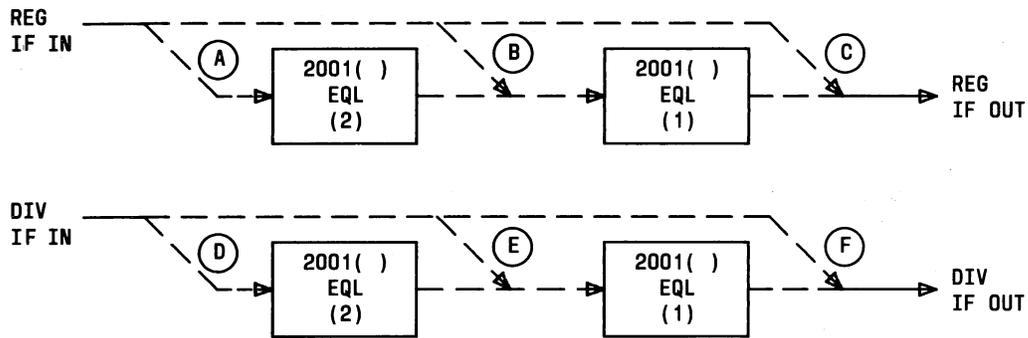
1. SIGNAL PATH MAY CONTAIN TWO EQUALIZERS (A), ONE EQUALIZER (B), OR NO EQUALIZER (C)
2. J27 MATES WITH IF IN AND J38 MATES WITH IF OUT

Fig. 16—4375A Linear Delay Equalizer

4375B LINEAR DELAY EQUALIZER (SPACE DIVERSITY)

The 4375B network (Fig. 17) can accommodate up to two 2001() linear delay equalizers in the regular signal path and up to two 2001() linear delay equalizers in the diversity signal path.

By selecting the appropriate equalizer code(s), the positive or negative linear delay slope of a radio hop can be corrected to within 1 nanosecond.



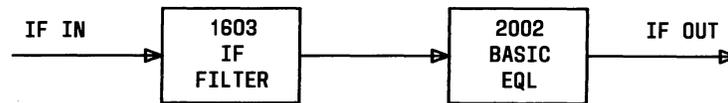
NOTES:

1. SIGNAL PATH MAY CONTAIN TWO EQUALIZERS (A) REGULAR AND (D) DIVERSITY, ONE EQUALIZER (B) REGULAR AND (E) DIVERSITY, OR NO EQUALIZER (C) REGULAR AND (F) DIVERSITY
2. REG IF IN MATES WITH J40, REG IF OUT MATES WITH J41, DIV IF IN MATES WITH J27 AND DIV IF OUT MATES WITH J43

Fig. 17—4375B Linear Delay Equalizer (Space Diversity)

4376F IF FILTER AND BASIC EQUALIZER

The 4376F network (Fig. 18) contains both a BPF (bandpass filter) and a BASIC (parabolic) equalizer. The function of the BPF is to improve the selectivity of the receiver by rejecting out-of-band signals at a point ahead of the IF AGC amplifier. The BASIC equalizer is primarily designed to compensate for the parabolic delay and amplitude shape contributed by the radio transmitter and receiver RF filters.

**NOTE:**

IF IN MATES WITH J29, AND IF OUT
MATES WITH J30

Fig. 18—4376F IF Filter and Basic Equalizer

4383 () TRANSMITTER UP CONV & MWV GEN

The 4383 () network (Fig. 19) is designed to operate in the 11-GHz frequency band. It consists primarily of three units: a 142 () microwave generator, a 2A multiplier, and a 17A up-converter mounted on a plug-in board. A microwave generator oven alarm interface circuit is also located on this plug-in board.

142 () MWV GENERATOR

The microwave generator is a free-running DRO (dielectric resonator oscillator). It is tuned to a frequency that is one-half of the required local oscillator frequency of the specific channel in the 11-GHz common carrier band. It is equipped with a fine frequency adjust control that has an adjustment range in excess of ± 500 kHz of the channel center frequency. The RF output level of this unit is about +10.0 dBm. This unit is housed in a small insulated oven that is maintained at a constant temperature of approximately 75 degrees C. The oven temperature is generated by a power transistor regulated by a thermister. The oven is powered directly from the -24 V battery plant or is reduced to -24 V by Zener diodes when powered from a -48 V battery plant. In the case of a power transistor short circuit, damage to the printed wiring is prevented by a thermal fuse located within the oven.

During the first 10 minutes following initial turn-on (cold start), the oven draws about 500 mA of current. As the oven temperature rises, the current gradually decreases and stabilizes at approximately 100 mA. This point is reached about 20 minutes following initial turn-on, at which time the GEN OVEN alarm (described further below) is switched off. At this time the generator frequency is still changing and requires additional time to stabilize. An oven control circuit generates an alarm voltage proportional to the current drawn by the power transistor. This voltage is monitored by the oven alarm interface circuit, which activates a GEN OVEN alarm when the alarm voltage is outside a predetermined range.

2A MULTIPLIER

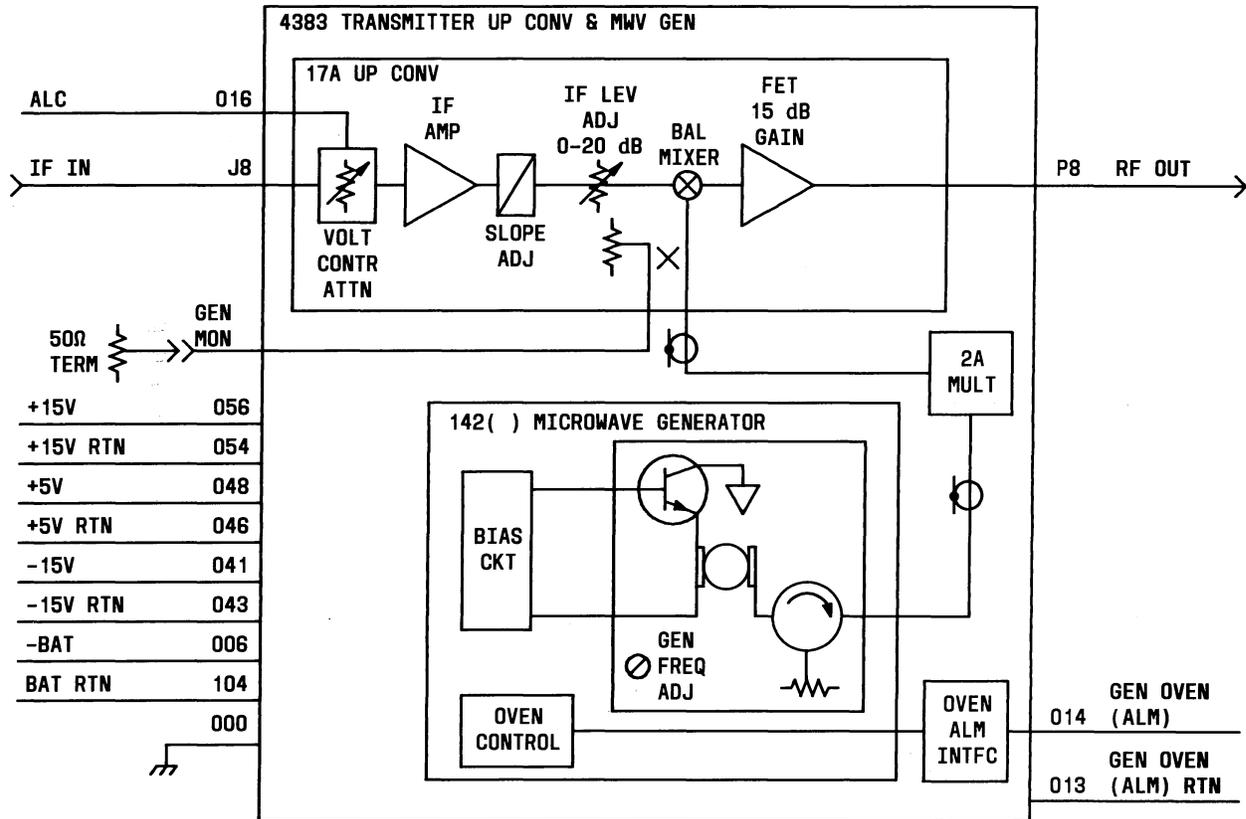
The 2A Multiplier doubles the frequency of the DRO output signal to be used as the local oscillator signal in the 11-GHz up-converter.

17A UP-CONVERTER

The 17A up-converter is designed to operate over the 11-GHz common carrier frequency band. It uses a balanced mixer to achieve the up-conversion of the 70-MHz IF signal.

The generator local oscillator signal from the 2A multiplier is applied to the mixer at a nominal level of +11.5 dBm through a 12-dB coupler located within the up-converter. The coupler output serves as the generator in-service power and frequency monitor port. The power level available at this port is approximately 0 dBm. The 70-MHz IF signal applied to this unit is fed through a voltage controlled attenuator, an amplifier, a manual slope adjust, a manually controlled attenuator, and finally to the mixer where it is up-converted to the 11-GHz frequency level. The resulting signal is then amplified by 15 dB and routed to the RF OUT port.

The degree of attenuation inserted by the voltage controlled attenuator is controlled by an ALC (automatic level control) voltage. This voltage is generated by an ALC circuit located at the output of the transmitter power amplifier. The function of this ALC loop is to maintain the overall gain of the transmitter relatively constant and independent of temperature variations. The slope adjust control permits the external adjustment of the transmitter amplitude slope by about ± 1 dB over a 40-MHz range. The manually controlled attenuator is also externally accessible and can provide up to 20 dB of loss to the IF signal. This control is normally adjusted during initial transmitter alignment for nominal transmitter output power level.



NOTE:
 NUMBERS ON LEADS OTHER THAN J OR P NUMBERS ARE PIN NUMBERS
 OF P5 WHICH MATES WITH 4383 TRANSMITTER UP CONV & MWV GEN

Fig. 19—4383() Transmitter Up-Converter and Microwave Generator

4384() RECEIVER DOWN CONV & MWV GEN

This network (Fig. 20) consists primarily of an 18B down-converter, a 142() microwave generator, and a 2A multiplier mounted on a plug-in board. A microwave generator oven alarm interface circuit is also located on the same board.

142() MWV GENERATOR AND 2A MULTIPLIER

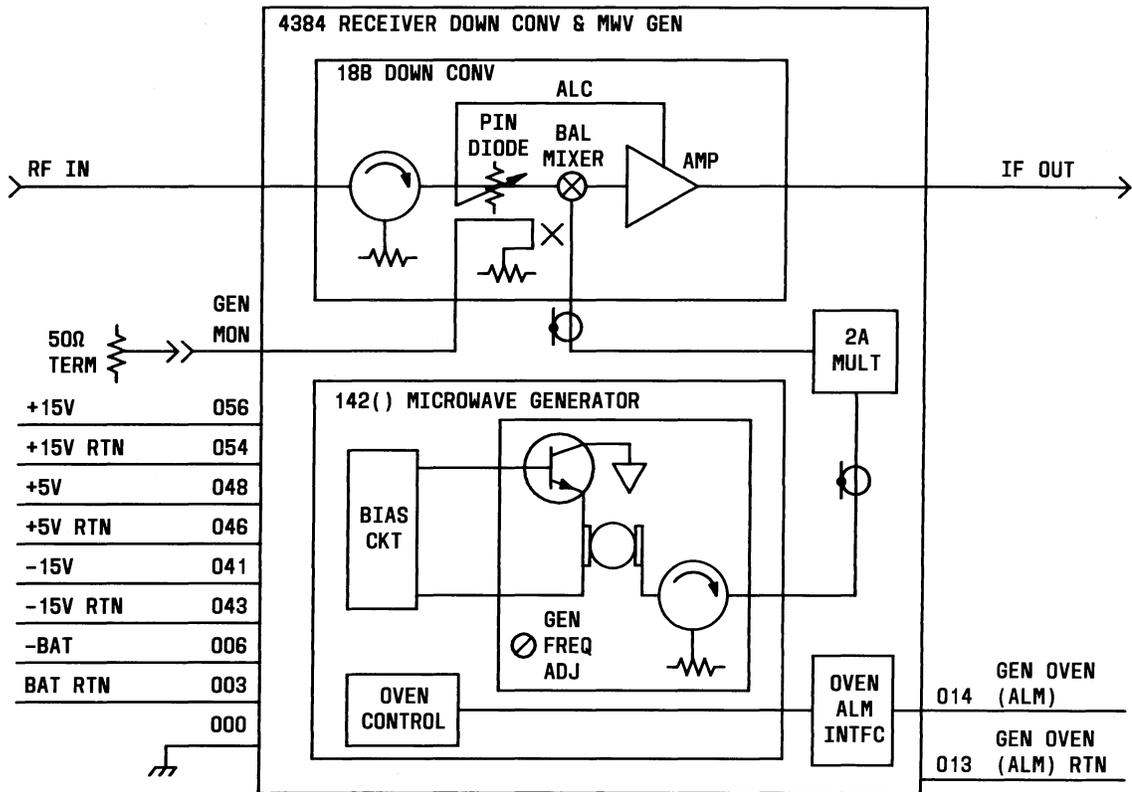
The microwave generator is a free-running DRO. It is tuned to one-half of a specific channel frequency on the 11-GHz common carrier band. This frequency is doubled to 11-GHz frequency range by the 2A multiplier. The generator is equipped with a fine frequency adjust control that has an adjustment range in excess of ± 500 kHz of the channel center frequency. The RF output level of this unit and the 2A multiplier is about +11.5 dBm. This unit is housed in a small insulated oven that is maintained at a constant temperature of approximately 75 degrees C. The oven temperature is generated by a power transistor regulated by a thermister. The oven is powered directly from the -24 V battery plant or is reduced to -24 V by Zener diodes when powered from a -48 V battery plant.

During the first 10 minutes following initial turn-on (cold start), the oven draws about 500 mA of current. As the oven temperature rises, the current gradually decreases and stabilizes at approximately 100 mA. This point is reached about 20 minutes following initial turn-on, at which time the GEN OVEN alarm (described further below) is switched off. At this time the generator frequency is still changing and requires additional time to stabilize. An oven control circuit generates an alarm voltage proportional to the current drawn by the power transistor. This voltage, in turn, is monitored by the oven alarm interface circuit, which activates a GEN OVEN alarm when the alarm voltage is outside a predetermined range.

18B DOWN-CONVERTER

The 18B down-converter uses a balanced mixer designed to operate in the 11-GHz common carrier frequency band. The generator signal is applied to the mixer through a 2A multiplier located within the down-converter. The output serves as the generator local oscillator signal into the balanced mixer of the down-converter.

The received signal level applied at the down-converter input is typically in the range of -14 dBm. This signal is fed through a circulator, to a pin diode, and finally to the mixer where it is down-converted to a 70-MHz IF signal. The IF signal is then amplified, fed through an attenuator, and routed to the down-converter IF OUT jack. The down-converter has a nominal gain of approximately 20 dB for received signal levels below about -30 dBm. For higher signal levels, the gain is progressively reduced by a pin diode that is controlled by an ALC voltage generated by the amplifier. The ALC function is primarily intended to prevent overdriving the receiver IF AGC amplifier during periods of strong signal up-fades.



NOTE:
 NUMBERS ON LEADS ARE PIN NUMBERS FOR THE CONNECTOR
 FOR THE 4384 RECEIVER DOWN CONV & MWV GEN

Fig. 20—4384() Receiver Down-Converter and Microwave Generator

4385 () RECEIVER DOWN CONV & MWV GEN (SPACE DIVERSITY)

This network (Fig. 21) consists primarily of an 18A down-converter, a 19A down-converter, and a 142() microwave generator, along with a 2A multiplier mounted on a plug-in board. A microwave generator oven alarm interface circuit is also located on the same board. The network is used in a space diversity receiver where two incoming signals are down-converted to two IF signals.

142 () MWV GENERATOR AND 2A MULTIPLIER

The microwave generator is a free-running DRO. It is tuned to one-half of a specific channel frequency of the 11-GHz common carrier band. This frequency is doubled to 11-GHz frequency range by the 2A multiplier. The generator is equipped with a fine frequency adjust control that has an adjustment range in excess of ± 500 kHz of the channel center frequency. The RF output level of this unit is about +11.5 dBm. The DRO is housed in a small insulated oven that is maintained at a constant temperature of approximately 75 degrees C. The oven temperature is generated by a power transistor regulated by a thermister. The oven is powered directly from the -24 V battery plant or is reduced to -24 V by Zener diodes when powered from a -48 V battery plant.

During the first 10 minutes following initial turn-on (cold start), the oven draws about 500 mA of current. As the oven temperature rises, the current gradually decreases and stabilizes at approximately 100 mA. This point is reached about 20 minutes following initial turn-on, at which time the GEN OVEN alarm (described further below) is switched off. At this time the generator frequency is still changing and requires additional time to stabilize. An oven control circuit generates an alarm voltage proportional to the current drawn by the power transistor. This voltage, in turn, is monitored by the oven alarm interface circuit, which activates a GEN OVEN alarm when the alarm voltage is outside a predetermined range.

The output of this microwave generator, along with the 2A multiplier, is used to supply an 11-GHz local oscillator signal to both the 18A down-converter and the 19A down-converter.

18A AND 19A DOWN-CONVERTERS

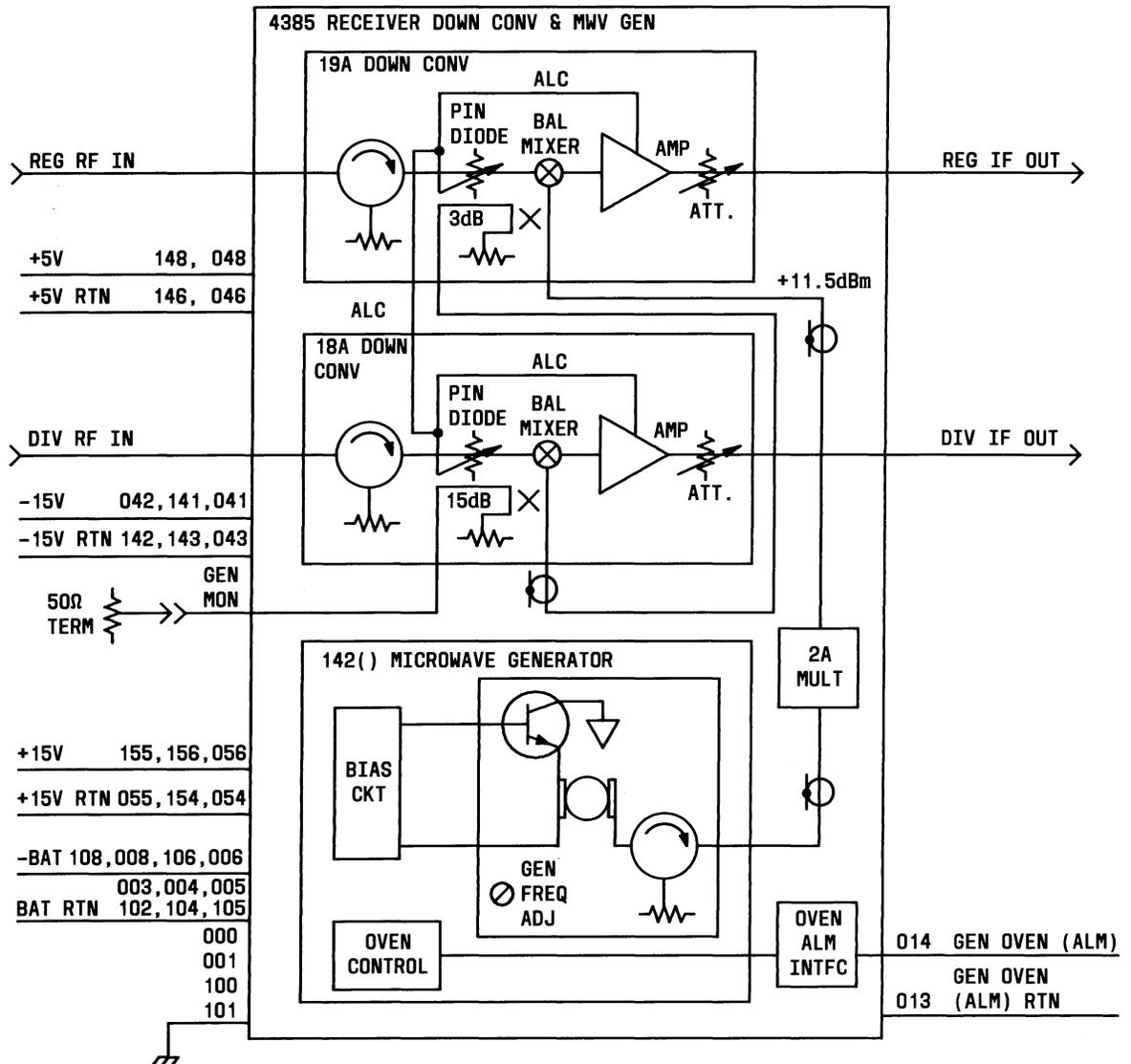
The 19A down-converter uses a balanced mixer designed to operate in the 11-GHz common carrier frequency band. The generator carrier signal is applied to the mixer through a 3 dB coupler located within the down-converter. A coupled output feeds into the balanced mixer of the 19A down-converter. The power available at this port is approximately -8 dBm.

The 18A down-converter is virtually the same as the 19A down-converter. The main difference is that it receives its generator carrier signal by the 19A down-converter rather than directly from the microwave generator and 2A multiplier.

The received signal level applied at the down-converter input is typically in the range of -14 dBm. Each signal is fed through a circulator, to a pin diode, and finally to the mixer where it is down-converted to a 70 MHz IF signal. The IF signal is then amplified, fed through an attenuator, and routed to the down-converter IF OUT jack. The down-converter has a nominal gain of approximately 17 dB for received signal levels below about -25 dBm. For higher signal levels, the gain is progressively reduced by the pin diode that is controlled by an ALC voltage. This voltage is generated within the down-converter. The ALC function is primarily intended to prevent overdriving the receiver IF AGC amplifier during periods of strong signal up-fades.

The ALC voltage of the two down-converters is tied together (bridged). This feature is designed to improve the signal-to-noise ratio of the combined downstream signal during conditions of shallow signal fades. It also allows the down-converter with the strongest RF input signal to generate the higher IF output level.

The output levels of the 18A and 19A down-converters are made approximately equal by adjusting the output attenuators.



NOTE:
NUMBERS ON LEADS ARE PIN NUMBERS FOR THE CONNECTOR FOR THE 4385 RECEIVER DOWN CONV & MWV GEN

Fig. 21—4385 () Receiver Down-Converter and Microwave Generator

4388A/4411C (11 GHZ) AND 4389A/4411B (6 GHZ) ALC NETWORKS

FUNCTIONAL DESCRIPTION

The basic function of the ALC (automatic level control) Network is to maintain the RF output power of the TWT amplifier at a constant level. If the RF output changes by more than 0.3 dB, the unit will activate a visual and remote alarm.

The 4388A and 4411C ALC Networks operate in the 10.7- to 11.7-GHz common carrier band and are functionally equivalent. The 4389A and 4411B ALC Networks operate in the 5.9- to 6.4-GHz common carrier band and are functionally equivalent.

BLOCK DIAGRAM DESCRIPTION

A block diagram of the ALC Network is shown in Fig. 22. Table A shows the signal input/output and dc power specifications.

The RF input signal from the *11-GHz* TWT amplifier is filtered by a *band reject* filter that rejects the *second* harmonics generated by the TWT amplifier. The RF input signal from the *6-GHz* TWT amplifier is filtered by a *low-pass* filter that rejects the *second and third* harmonics generated by the TWT amplifier. A sample of the signal output is detected and compared with that of an internal reference. The difference between the detected voltage and the reference voltage is the ALC voltage (ALC V [MTR]).

The ALC V (MTR) voltage, nominally 0.0 V dc, is level shifted and becomes the ALC control voltage (ALC V). The ALC V, nominally -5.0 V dc, is sent to the up-converter in the TRANSMITTER UP CONV & MWV GEN unit. The up-converter uses the ALC V to control an IF attenuator. The IF attenuator compensates for transmitter gain variations to maintain a constant TWT output power.

The DET ADJ (detector adjust) control is used to null the voltage generated by the signal detector when the transmitter is adjusted for nominal output level. When the ALC ON/OFF switch is in the OFF position, the ALC function is disabled and the LED indicator ALC OFF is lighted. With the ALC ON/OFF switch in the ON position, if the magnitude of the ALC V (MTR) becomes greater than 0.2 V dc, the LED indicator PWR OUT OF RANGE lights. This indicates that the TWT output power has changed by more than 0.3 dB from its nominal setting. In each of the above cases, the ALC Network generates a transmitter alarm (TRMTR ALC ALM) to indicate that these conditions must be corrected prior to returning the radio to normal service.

The ALC V (MTR) can be monitored by the ALARM AND METER unit in the radio transmitter and/or by an external meter connected to the ALC V test points on the unit. The RF MON port is an in-service transmitter monitor realized with a 30-dB coupler.

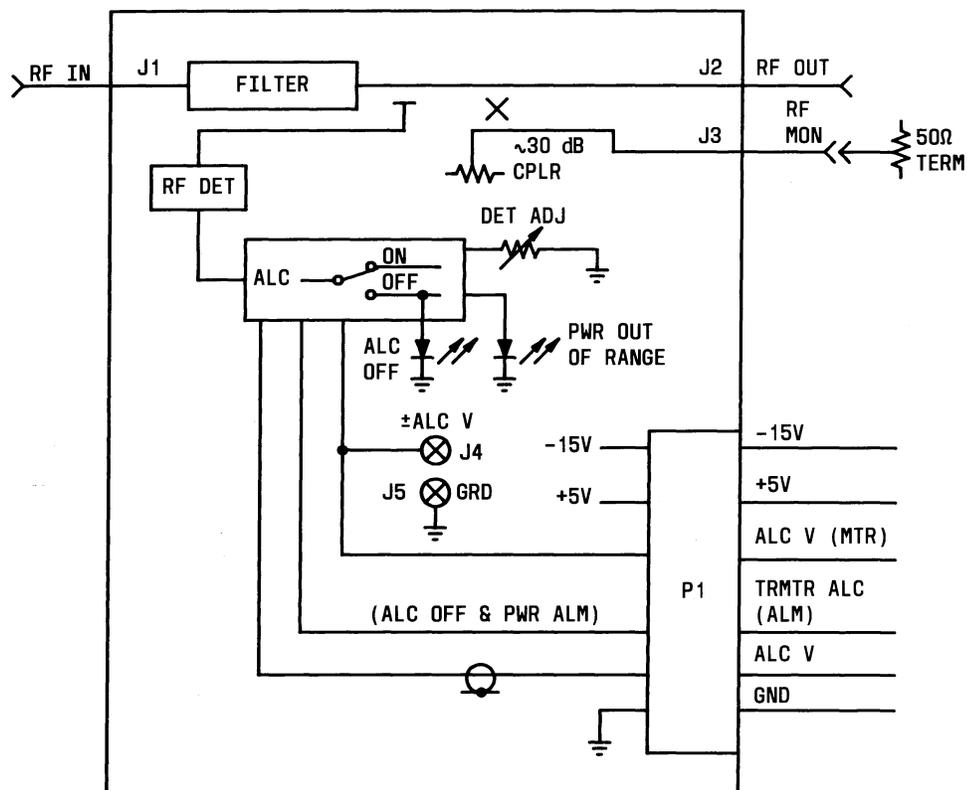


Fig. 22—4388A/4411C (11 GHz) and 4389A/4411B (6 GHz) ALC Networks

TABLE A			
SIGNAL INPUT/OUTPUT AND DC POWER SPECIFICATIONS FOR THE 4388A/4411C (11 GHZ) AND 4389A/4411B (6 GHZ) ALC NETWORKS			
DESIGNATION	PIN NO.	DESCRIPTION	SIGNAL
SIGNAL INPUT			
RF IN	J1	RF input port	+38.0 dBm (nominal)
SIGNAL OUTPUT			
RF MON	J3	RF monitor port	+8.0 dBm (nominal)
RF OUT	J2	RF output port	+36.9 dBm (nominal)
ALC V ±	J4	ALC voltage monitor	0.0 V dc (nominal)
ALC V (GRD)	J5	ALC voltage monitor return	—
ALC V	P1 (10)	Up-converter control signal	-5.0 V dc (nominal)
ALC V (MTR)	P1 (12)	ALC voltage monitor (meter)	0.0 V dc (nominal)
TRMTR ALC (ALM)	P1 (14)	Transmitter Alarm	TTL (active-high)
POWER			
+5 V	P1 (6)	+5 volt input power	+5 V dc (60 mA)
-15 V	P1 (2)	-15 volt input power	-15 V dc (60 mA)
GRD	P1 (1,3,5,9,11,13)	Common circuit return	—

4390() TRANSMITTER UP CONV & MWV GEN

The 4390() network (Fig. 23) consists primarily of a 141() microwave generator and a 20A up-converter mounted on a plug-in board. A microwave generator oven alarm interface circuit is also located on this plug-in board.

141() MWV GENERATOR

The microwave generator is a free-running DRO. It is tuned to a specific channel frequency in the lower-six common carrier band. It is equipped with a fine frequency adjust control that has an adjustment range in excess of ± 500 kHz of the channel center frequency. The RF output level of this unit is about +11.5 dBm. This unit is housed in a small insulated oven that is maintained at a constant temperature of approximately 75 degrees C. The oven temperature is generated by a power transistor regulated by a thermister. The oven is powered directly from the -24 V battery plant or is reduced to -24 V by Zener diodes when powered from a -48 V battery plant.

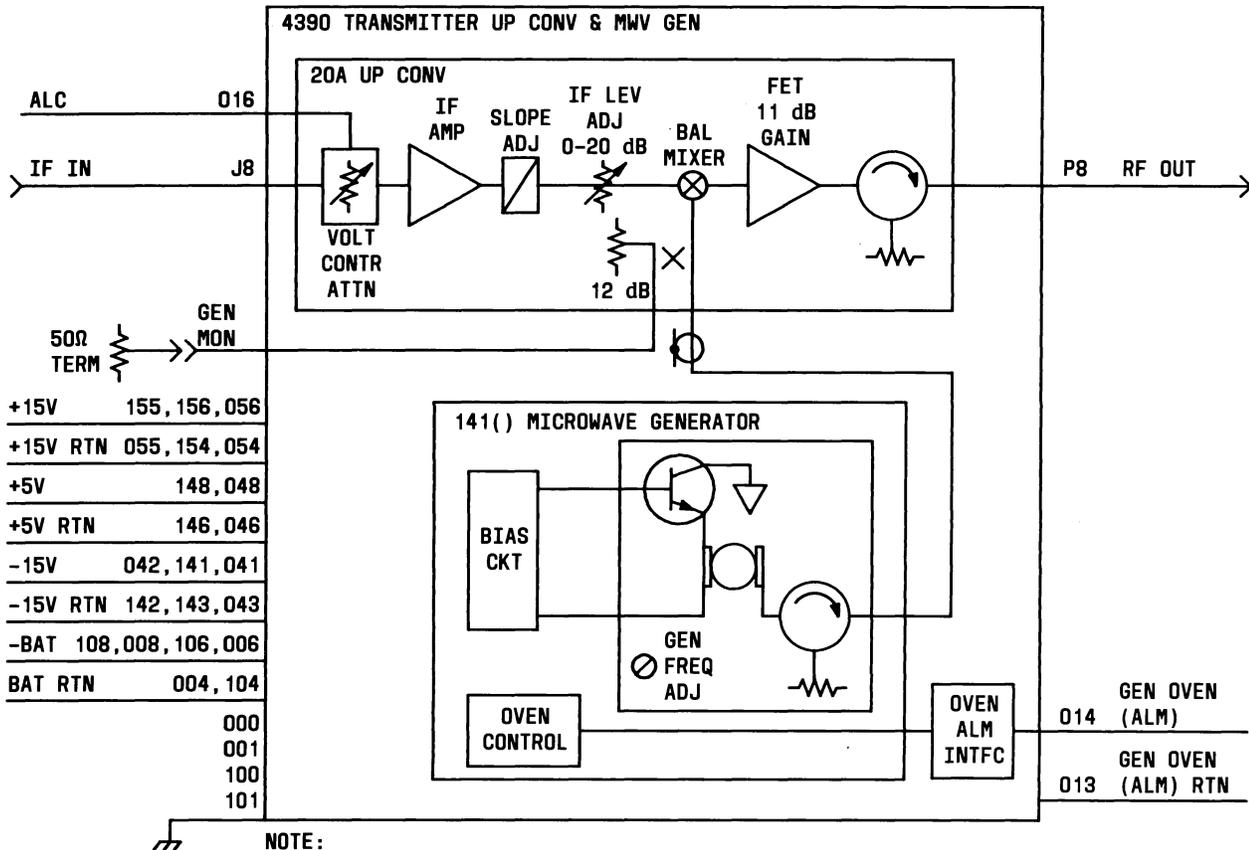
During the first 10 minutes following initial turn-on (cold start), the oven draws about 500 mA of current. As the oven temperature rises, the current gradually decreases and stabilizes at approximately 100 mA. This point is reached about 20 minutes following initial turn-on, at which time the GEN OVEN alarm (described further below) is switched off. At this time the generator frequency is still changing and requires additional time to stabilize. An oven control circuit generates a voltage proportional to the current drawn by the power transistor. This voltage, in turn, is monitored by the oven alarm interface circuit, which activates a GEN OVEN alarm when the alarm voltage is outside a predetermined range.

20A UP-CONVERTER

The 20A up-converter is designed to operate over the lower-six common carrier frequency band. This up-converter uses a balanced mixer to achieve the up-conversion of the 70-MHz IF signal.

The generator local-oscillator signal is applied to the mixer at a nominal level of +11.5 dBm through a 12-dB coupler located within the up-converter. The coupler output serves as the generator in-service power and frequency monitor port. The power level available at this port is approximately 0 dBm. The 70-MHz IF signal applied to this unit is fed through a voltage controlled attenuator, an amplifier, a manual slope adjust, a manually controlled attenuator, and finally to the mixer where it is up-converted to the 6-GHz frequency level. The resulting signal is then amplified by 15 dB and routed to the RF OUT port.

The degree of attenuation inserted by the voltage controlled attenuator is controlled by an ALC voltage. The voltage is generated by an ALC circuit located at the output of the transmitter power amplifier. The function of this ALC loop is to maintain the overall gain of the transmitter relatively constant and independent of temperature variations. The slope adjust control permits the external adjustment of the transmitter amplitude slope by approximately ± 1 dB over a 40-MHz range. The manually controlled attenuator is also externally accessible and can provide up to 20 dB of loss to the IF signal. This control is normally adjusted during initial transmitter alignment for nominal transmitter output power level.



NOTE:
 NUMBERS ON LEADS OTHER THAN J OR P NUMBERS ARE PIN NUMBERS
 OF P5 WHICH MATES WITH 4390 TRANSMITTER UP CONV & MWV GEN

Fig. 23—4390() Transmitter Up-Converter and Microwave Generator

4391() RECEIVER DOWN CONV & MWV GEN

This network (Fig. 24) consists primarily of a 21B down-converter and a 141() microwave generator mounted on a plug-in board. A microwave generator oven alarm interface circuit is also located on the same board.

141() MWV GENERATOR

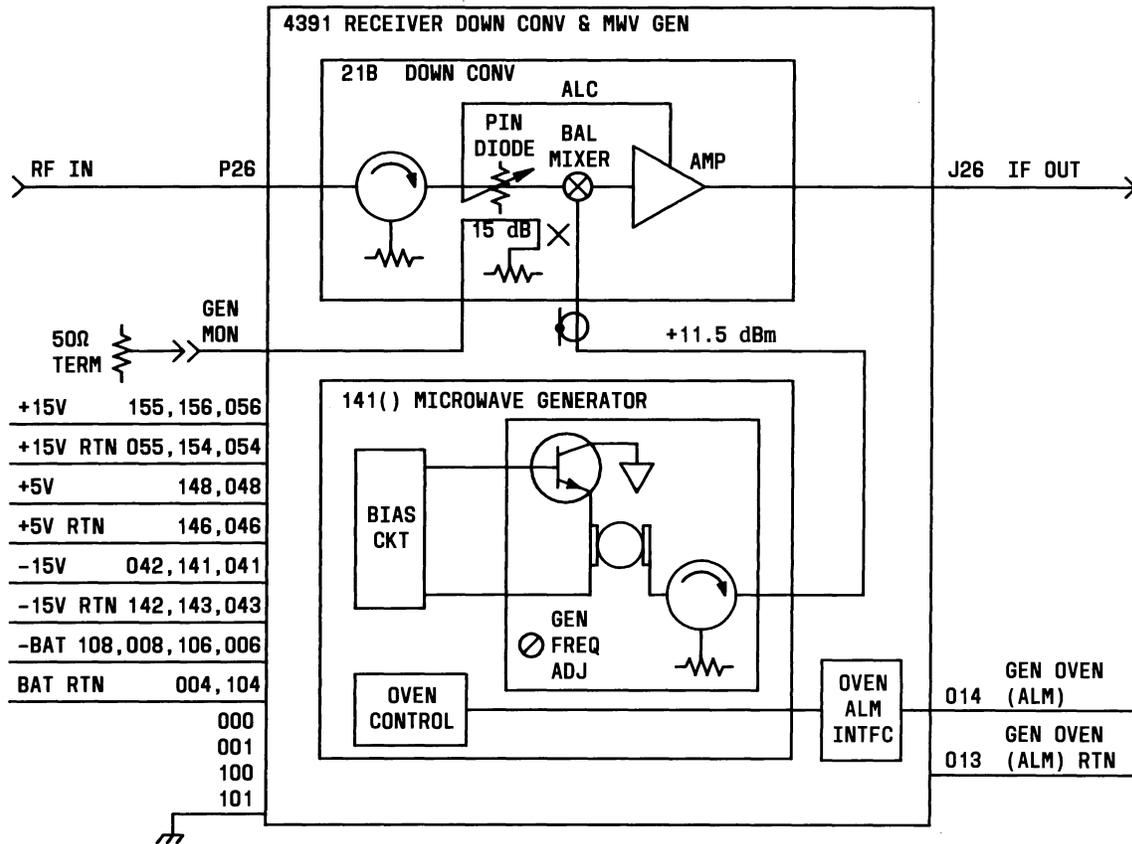
The microwave generator is a free-running DRO. It is tuned to a specific channel frequency in the lower-six common carrier band. It is equipped with a fine frequency adjust control that has an adjustment range in excess of ± 500 kHz of the channel center frequency. The RF output level of this unit is about +11.5 dBm. This unit is housed in a small insulated oven that is maintained at a constant temperature of approximately 75 degrees C. The oven temperature is generated by a power transistor regulated by a thermister. The oven is powered directly from the -24 V battery plant or is reduced to -24 V by Zener diodes when powered from a -48 V battery plant.

During the first 10 minutes following initial turn-on (cold start), the oven draws about 500 mA of current. As the oven temperature rises, the current gradually decreases and stabilizes at approximately 100 mA. This point is reached about 20 minutes following initial turn-on, at which time the GEN OVEN alarm is switched off. At this time the generator frequency is still changing and requires additional time to stabilize. An oven control circuit generates an alarm voltage proportional to the current drawn by the power transistor. This voltage, in turn, is monitored by the oven alarm interface circuit, which activates a GEN OVEN alarm when the alarm voltage is outside a predetermined range.

21B DOWN-CONVERTER

The 21B down-converter uses a balance mixer designed to operate over the entire lower-six common carrier frequency band. The generator local-oscillator signal is applied to the mixer by a 15-dB coupler located within the down-converter. The coupler output serves as the generator in-service power and frequency monitor port. The power available at this port is approximately -3 dBm.

The received signal level applied at the down-converter input is typically in the range of -14 dBm. This signal is fed through a circulator, to a pin diode, and finally to the mixer where it is down-converted to a 70-MHz IF signal. The IF signal is then amplified and routed to the down-converter IF OUT jack. The down-converter has a nominal gain of approximately 20 dB for received signal levels below about -25 dBm. For higher signal levels, the gain is progressively reduced by the pin diode that is controlled by an ALC voltage generated by the amplifier. The ALC function is primarily intended to prevent overdriving the receiver IF AGC amplifier during periods of strong signal up-fades.



NOTE:
 NUMBERS ON LEADS ARE PIN NUMBERS FOR THE CONNECTOR FOR THE 4391
 RECEIVER DOWN CONV & MWV GEN

Fig. 24—4391 () Receiver Down-Converter and Microwave Generator

4392 () RECEIVER DOWN CONV & MWV GEN (SPACE DIVERSITY)

This network (Fig. 25) consists primarily of a 22A down-converter, a 21A down-converter, and a 141 () microwave generator mounted on a plug-in board. A microwave generator oven alarm interface circuit is also located on the same board.

141 () MWV GENERATOR

The microwave generator is a free-running DRO. It is tuned to a specific channel frequency in the lower-six common carrier band. It is equipped with a fine frequency adjust control that has an adjustment range in excess of ± 500 kHz of the channel center frequency. The RF output level of this unit is about +11.5 dBm. The DRO is housed in a small insulated oven which is maintained at a constant temperature of approximately 75 degrees C. The oven temperature is generated by a power transistor regulated by a thermister. The oven is powered directly from the -24 V battery plant or is reduced to -24 V by Zener diodes when powered from a -48 V battery plant.

During the first 10 minutes following initial turn-on (cold start), the oven draws about 500 mA of current. As the oven temperature rises, the current gradually decreases and stabilizes at approximately 100 mA. This point is reached about 20 minutes following initial turn-on, at which time the GEN OVEN alarm (described further below) is switched off. At this time the generator frequency is still changing and requires additional time to stabilize. An oven control circuit generates an alarm voltage proportional to the current drawn by the power transistor. This voltage, in turn, is monitored by the oven alarm interface circuit, which activates a GEN OVEN alarm when the alarm voltage is outside a predetermined range.

The output of this microwave generator is used to supply a 6-GHz signal to the 22A down-converter and the 21A down-converter.

22A DOWN-CONVERTER

The 22A down-converter uses a balanced mixer designed to operate over the entire lower-six common carrier frequency band. The generator carrier signal is applied to the mixer through a 3-dB coupler located within the down-converter. A coupled output feeds the generator carrier signal into the balanced mixer of the 21A down-converter. The power available at this port is approximately -8 dBm.

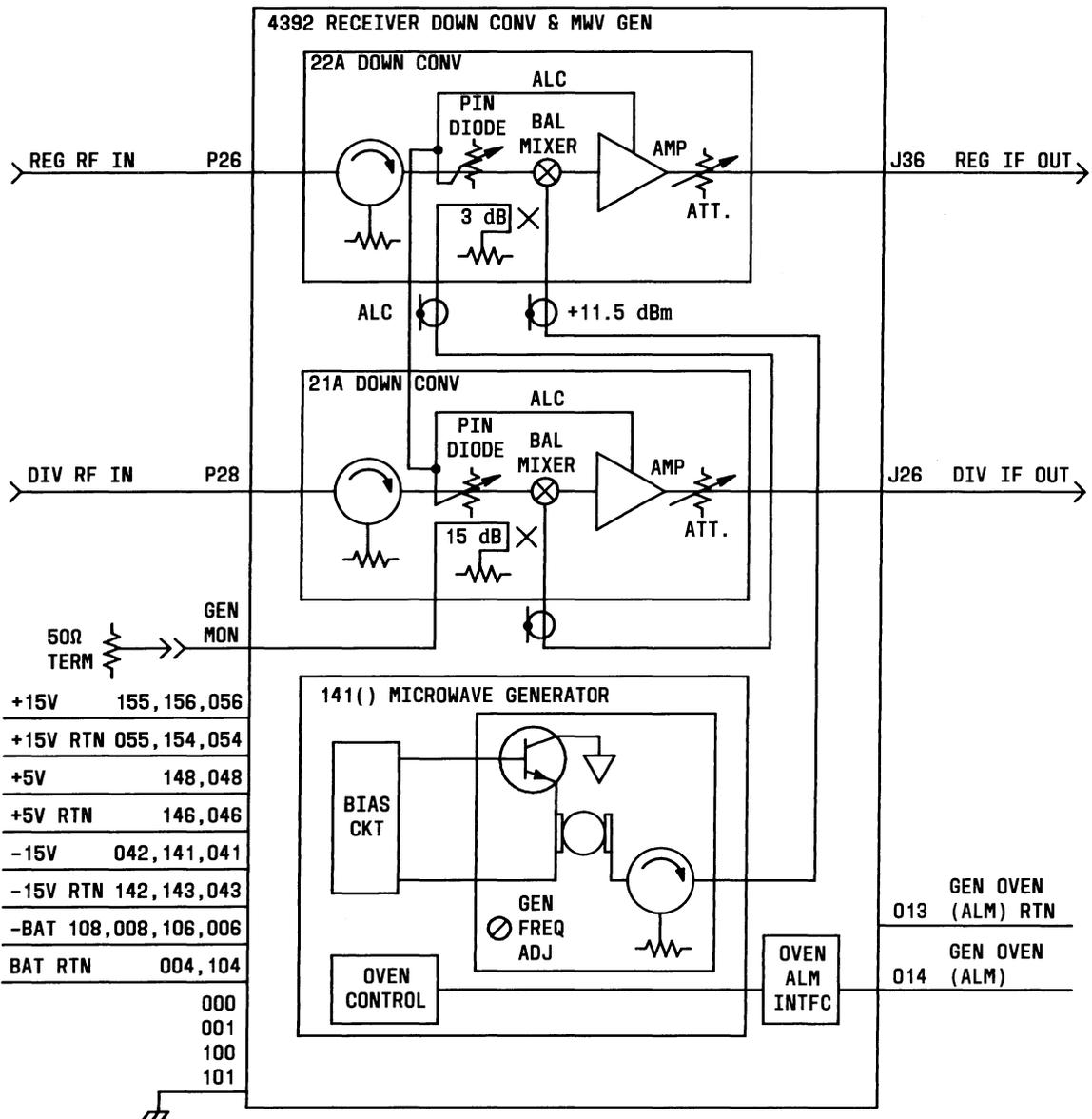
The received signal level applied at the down-converter input is in the range of -14 dBm. This signal is fed through a circulator, to a pin diode, and finally to the mixer where it is down-converted to a 70-MHz IF signal. The IF signal is then amplified, fed through an attenuator, and routed to the down-converter IF OUT jack. The down-converter has a nominal gain of approximately 17 dB for received signal levels below about -25 dBm. For higher signal levels, the gain is progressively reduced by the pin diode that is controlled by an ALC voltage generated by the amplifier. The ALC function is primarily intended to prevent overdriving the receiver IF AGC amplifier during periods of strong signal up-fades.

The ALC voltage of the two down-converters is tied together (bridged). This feature is designed to improve the signal-to-noise ratio of the combined downstream signal during conditions of shallow signal fades. It also allows the down-converter with the strongest RF input signal to generate the higher IF output level.

21A DOWN-CONVERTER

The 21A down-converter is virtually the same as the 22A down-converter. The main difference is that it receives its generator carrier signal from the 22A down-converter rather than directly from the microwave-generator.

The output levels of the 22A and 21A down-converters are made approximately equal by adjusting the output attenuators.



NOTE:
 NUMBERS ON LEADS OTHER THAN J OR P NUMBERS ARE PIN NUMBERS OF P23
 WHICH MATES WITH 4392 RECEIVER DOWN CONV & MWV GEN

Fig. 25—4392 () Receiver Down-Converter and Microwave Generator

AMR1/3 SPAN DIRECTOR

FUNCTIONAL DESCRIPTION

The SPAN DIR (span director) circuit pack switches DS3 signals at the line terminal, allowing a regular channel DS3 signal to be spanned to the protection channel as follows:

- Transmit-end: Provides a bridge to protection for one tributary (DS3 signal)
- Receive-end: Provides a tail-end switch to protection for one tributary (DS3 signal).

For the transmit-end application, one regular channel DS3 tributary can be switched to the protection channel. An access channel input and protection channel output are provided on the rear of the unit. They are accessible at the DS3 patch panel located on the left side of the growth shelf.

For the receive-end application, the received DS3 tributary from the protection channel is switched to the appropriate regular channel output. An access channel output and protection channel input are provided on the rear of the unit. They are accessible at the DS3 patch panel located on the right side of the growth shelf.

The AMR1 SPAN DIR unit is used for regular channels 1 through 7. The AMR3 SPAN DIR unit is used for regular channels 8 through 10.

BLOCK DIAGRAM DESCRIPTION

A block diagram of the SPAN DIR is shown in Fig. 26. Table B has the signal input/output and dc power specifications.

Front mounted jacks on the AMR1, labeled 1 through 7 (J2-J8), provide the DS3 signal interface for regular channels 1 through 7, respectively. For growth applications, channels 8 through 10 are connected to jacks 1, 2, and 3 (J2-J4) on the AMR3, respectively. Jacks 4, 5, 6, and 7 (J5-J8) are not used on the AMR3.

The protection channel port (PROT) is connected via the backplane and bay wiring to a VMR & CODER unit (receive-end) or a B3ZS DCODR (transmit-end) unit on the protection digital terminal shelf.

DS3 transmission flow is directed with dry reed type relays operated by the switch control circuit. The switch control circuit receives switch instructions from the protection (receive-end) or transmit (transmit-end) status (PROT or TRMT STAT) unit as BCD (binary coded data) signals (DIR0-DIR3). The switch control performs a three-to-eight decoding function and the appropriate relay bank is energized. Switch verification signals (DIRV0-DIRV3) are sent to the status unit.

Leads DIRA-DIRD and D are used to enable or disable the SPAN DIR circuit pack. In a growth situation where both AMR1 and AMR3 are required, these leads are connected in parallel (tied together) so that only one SPAN DIR is enabled.

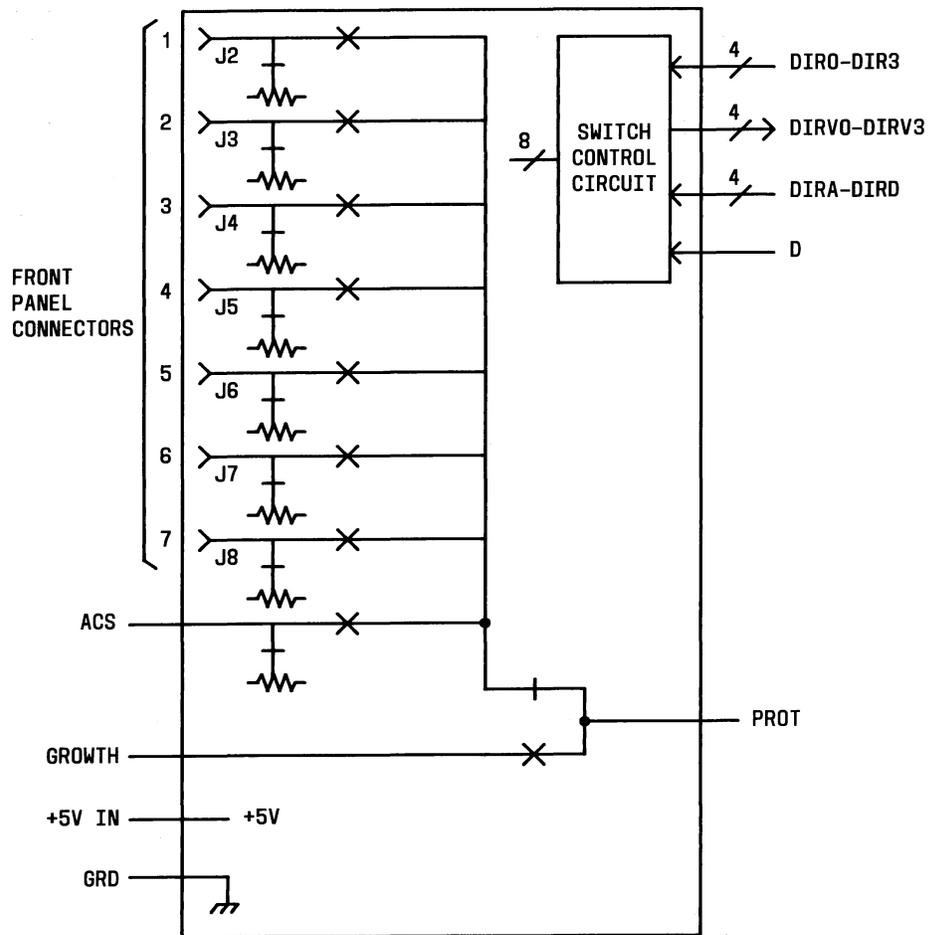


Fig. 26—AMR1/3 Span Director

TABLE B				
SIGNAL INPUT/OUTPUT AND DC POWER SPECIFICATIONS FOR THE AMR1/3 SPAN DIRECTOR				
DESIGNATION	PIN NO. (NOTE)	DESCRIPTION	I/O	SIGNAL
DS3 INTERFACE				
1-7	J2-J8	Regular DS3 interface (input for transmit-end, output for receive-end)	I/O	DS3 (45 Mb/s)
ACS	150	DS3 protection access (input for transmit-end, output for receive-end)		
GROWTH	135	Growth DS3 interface to from AMR3 PROT port (input for transmit-end, output for receive-end)		
PROT	030	Protection DS3 interface (input for transmit-end, output for receive-end)		
SWITCH CONTROL				
DIR0-DIR3	015,115,014,114	BCD switch control signals	I	TTL
DIRV0-DIRV3	111,011,112,012	Switch operate verification	O	
DIRA-DIRD	010,110,109,009	Switch control enable (backplane straps)	I	
D	008			
See note at end of table.				

TABLE B (Contd)				
SIGNAL INPUT/OUTPUT AND DC POWER SPECIFICATIONS FOR THE AMR1/3 SPAN DIRECTOR				
DESIGNATION	PIN NO. (NOTE)	DESCRIPTION	I/O	SIGNAL
POWER				
+5 V IN	045-047,145-147	DC voltage supply	I	+5 V dc (55 mA)
GRD	000,001,029,031, 034-036,049-051, 055,056,100,101, 129-131,134-136, 149,151,155,156	Ground	—	—
Note: Unless otherwise indicated, all pin numbers are associated with the circuit pack backplane connector J1.				

AMR2 B3ZS DECODER AND TRANSMIT ELASTIC STORE

The AMR2 B3ZS DCODR (Fig. 27) performs two main functions. The decoder section receives the bipolar 3-zero substitution DS3 signal and decodes it to binary clock and data. The data is then written to elastic store, where overhead and stuff bits are added to bring the output to a bit rate that is synchronous with the output of the other AMR2s in the system.

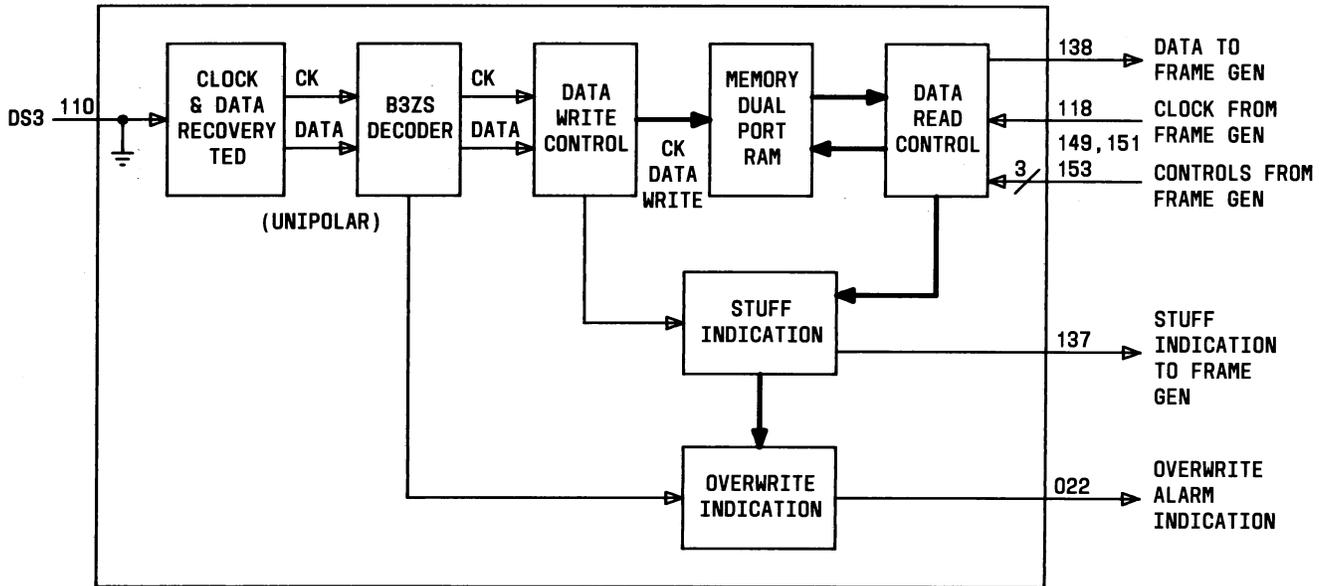


Fig. 27—AMR2 B3ZS Decoder

AMR5/155 FRAME GENERATOR

The AMR5/155 FRAME GEN (Fig. 28) performs the following functions:

- Generates the high-speed clock and the control signals for transmission to the elastic stores. These control signals determine where the elastic stores put dummy bits in the data stream for overhead bit insertion.
- Receives the data bits from the elastic stores and multiplexes them into the 6-rail format.
- Generates the system symbol clock.
- Scrambles the data received from the elastic stores.
- Generates and inserts the 64-QAM (quadrature amplitude modulation) frame format.
- Generates page pulses to align the rest of the DPU (digital processing unit) in the frame structure.
- Transmits the framed 6 rails, page signal, and symbol clock to the DPU and protection boards.

The AMR5 FRAME GEN unit is used in a regular channel.

The AMR155 FRAME GEN unit is used in the protection channel.

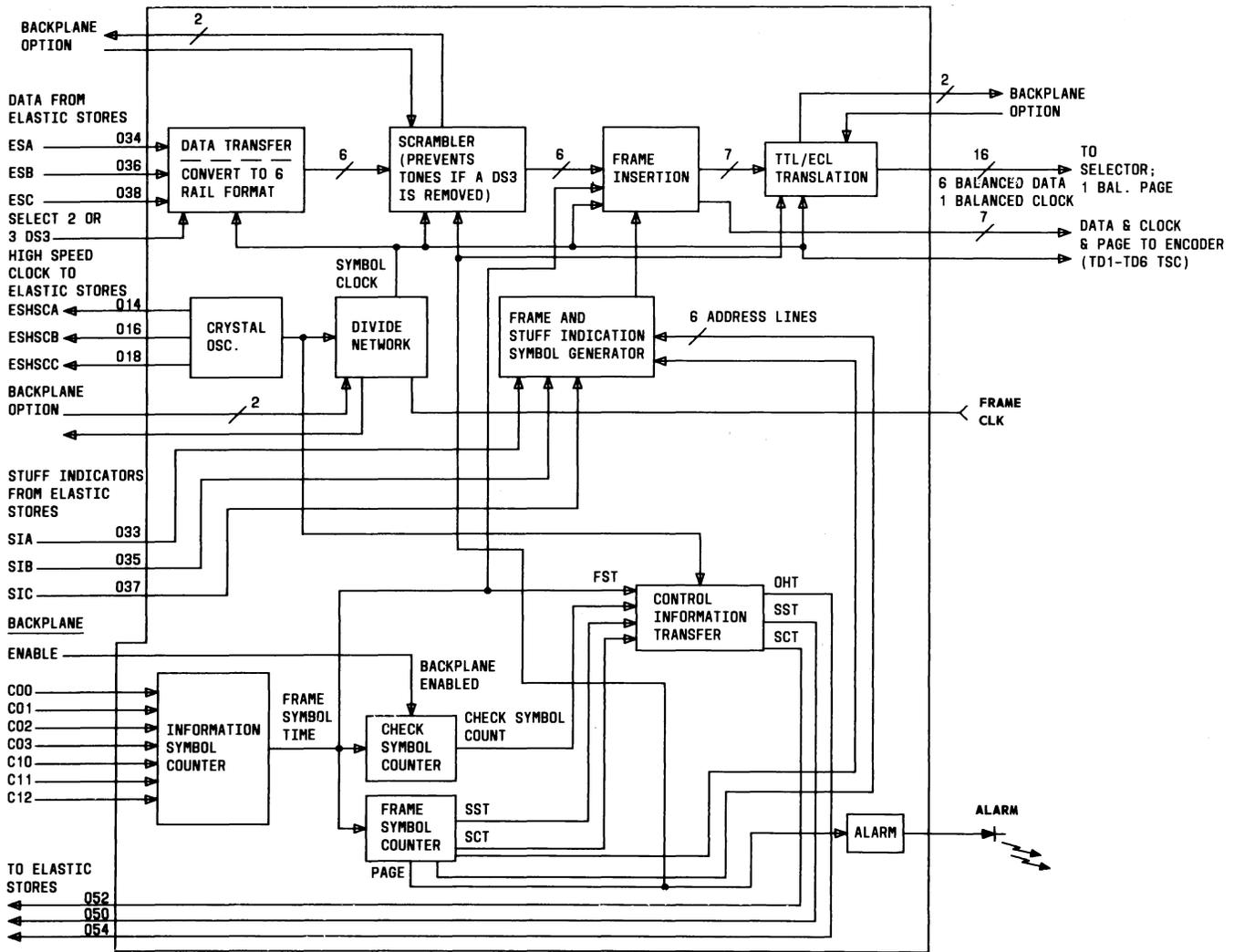


Fig. 28—AMR5/155 Frame Generator

AMR11 CRC CODER

The AMR11 CRC CODER (Fig. 29) performs a cyclic redundancy check on the incoming data, inserts service channel bits and cyclic redundancy bits into the data stream, and gray-codes the data before passing it on to the digital-to-analog converter (AMR20). The AMR11 also generates and transmits two signals (the TAC and TAP—transmit auxiliary clock and page) to the service channel muldem to ensure proper timing of the auxiliary data stream relative to the primary 135-Mb/s data stream.

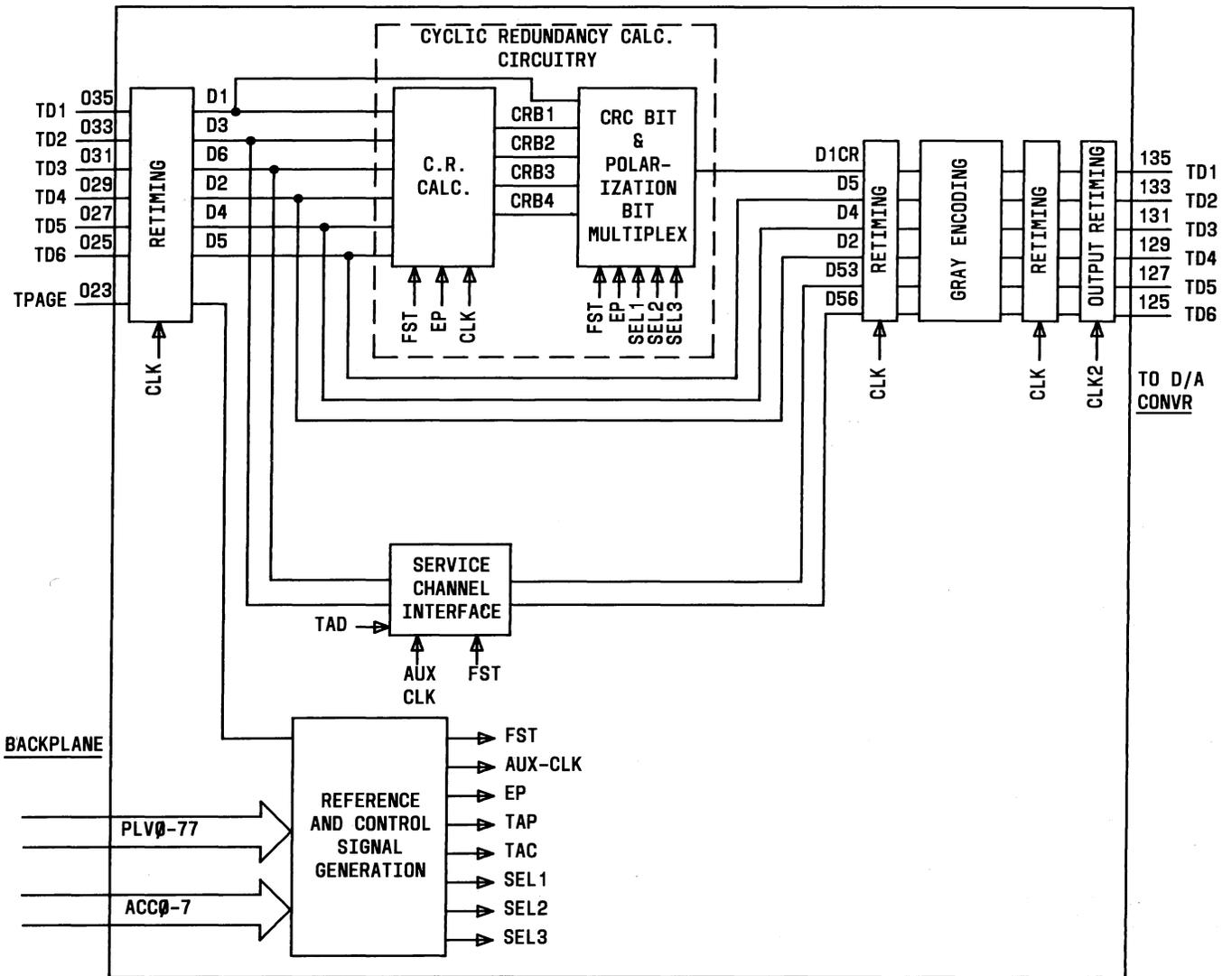


Fig. 29—AMR11 CRC Coder

AMR12 LINE SELECTOR

The AMR12 LINE SELR (Fig. 30) selects either the first regular channel, the protection channel, or the expansion port channel to bridge onto a protection channel. This unit provides a head-end bridge for the protection switch.

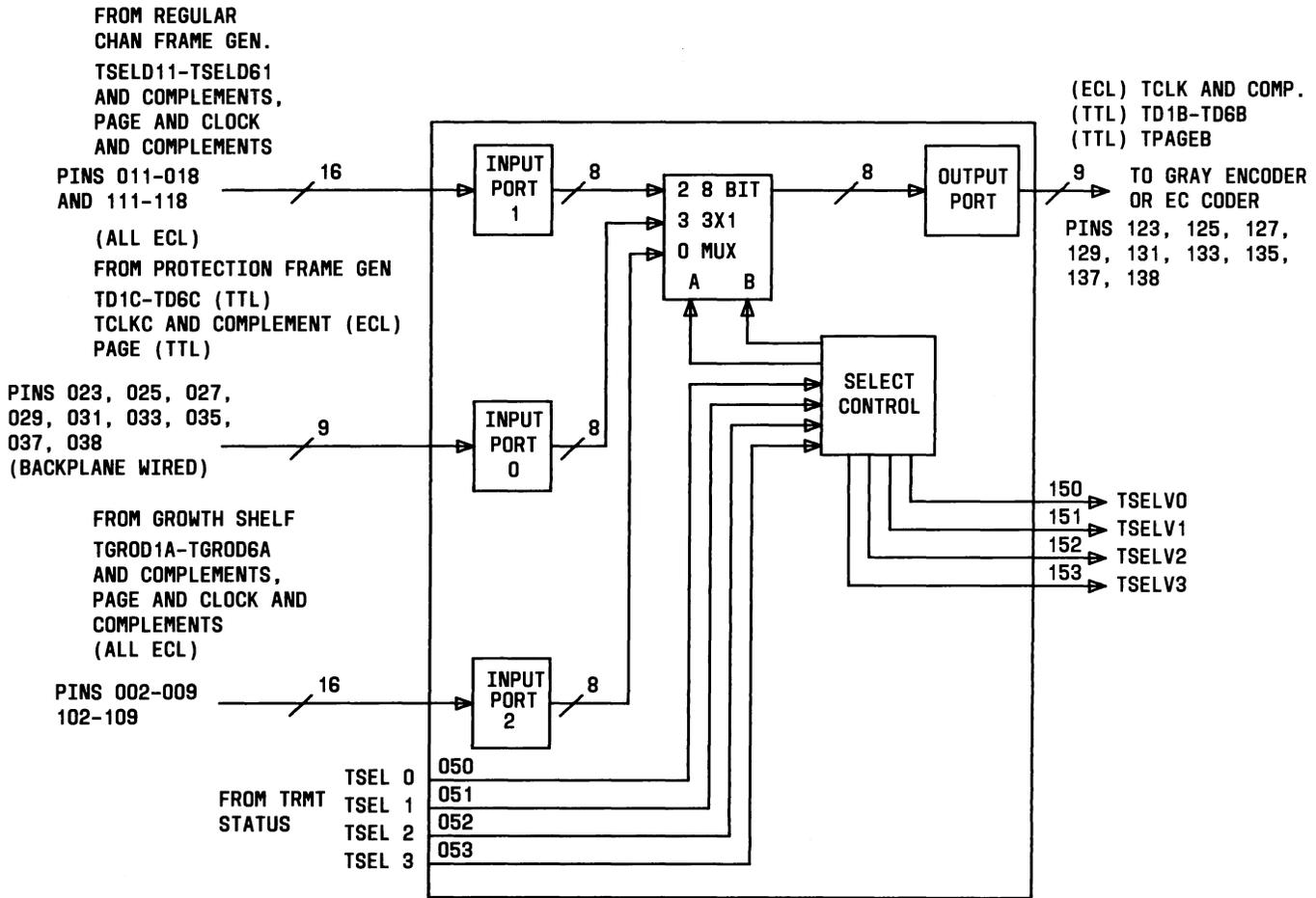


Fig. 30—AMR12 Line Selector

AMR13 GROWTH LINE SELECTOR

The AMR13 GR LN SELR (Fig. 31) receives data, page, and clock signals (and their complementary signals) from either an AMR6 FRAME GEN or a previous AMR13. The AMR13 also receives a 4-bit channel-select word from the AMR116 TRMT STAT, decodes the word, and selects the corresponding regular channel to be routed to the adjacent AMR13 or the AMR12 LINE SELR.

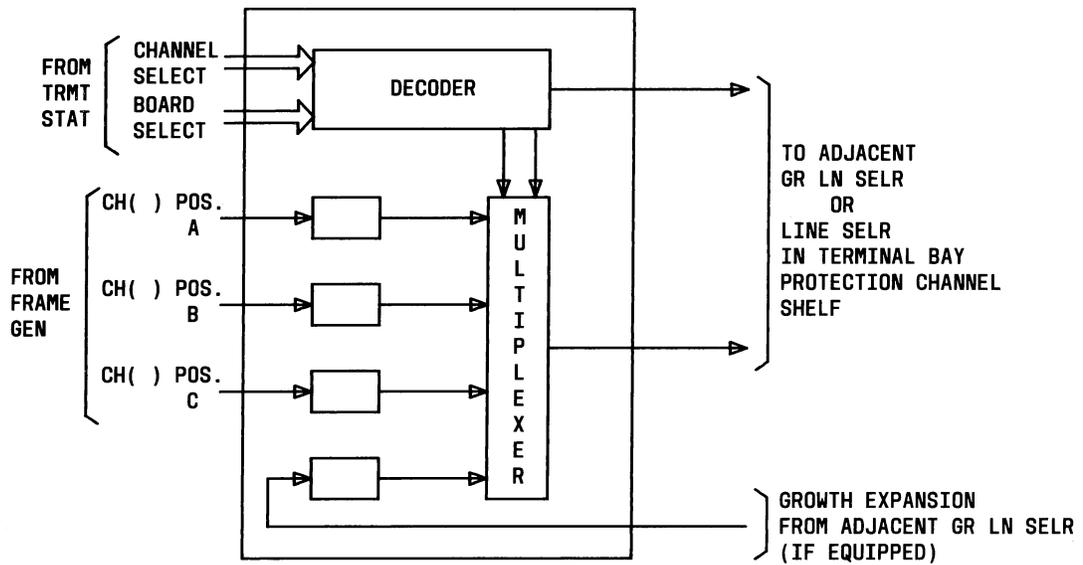


Fig. 31—AMR13 Growth Line Selector

AMR16/16B FRAME RESUPPLY

FUNCTIONAL DESCRIPTION

The FRAME RSPLY is an optional circuit pack that is installed in a regenerator shelf to provide:

- Service channel transmission within a valid frame format when the REGEN FRMR (regenerator framer) is unable to frame on the received data
- Valid frame for an out-of-service IF loopback test of a regenerator.

Note: The regenerator shelf must be equipped with a REGEN FRMR for the frame resupply option.

BLOCK DIAGRAM DESCRIPTION

The FRAME RSPLY (Fig. 32) receives clock and data from the REGEN FRMR. These clock and data are multiplexed with clock and data that are generated internally. The internally generated data contains a valid frame format that includes service channel data from the SC MULDM. When the clock and data from the REGEN FRMR are sent to the D/A CONVR, the FRAME RSPLY is considered off. Three conditions will turn the FRAME RSPLY on (allow it to pass the internally generated clock and data to the DA CONVR):

1. If the frame loss indication (AIFIFL) from the REGEN FRMR is low
2. If the control lead (CFRSR) from the CHAN CONTR is high
3. If the FRAME RSPLY is manually turned on with the MAN FRS pushbutton—provided the manual inhibit lead, CFRSI, is low.

The internal oscillator frequency of the FRAME RSPLY can be monitored at the faceplate jack FRS CLK.

The status of the FRAME RSPLY is indicated to the CHAN CONTR by the IFRS lead. This is normally high and goes low when the FRAME RSPLY turns on, lighting the FRS ON LED. The state of the MAN FRS pushbutton is indicated by the IMFRS lead. This is normally high and goes low when the pushbutton is pressed, lighting the MAN FRS ON LED.

PINOUT DESCRIPTION

Refer to Table C for signal input/output and power information.

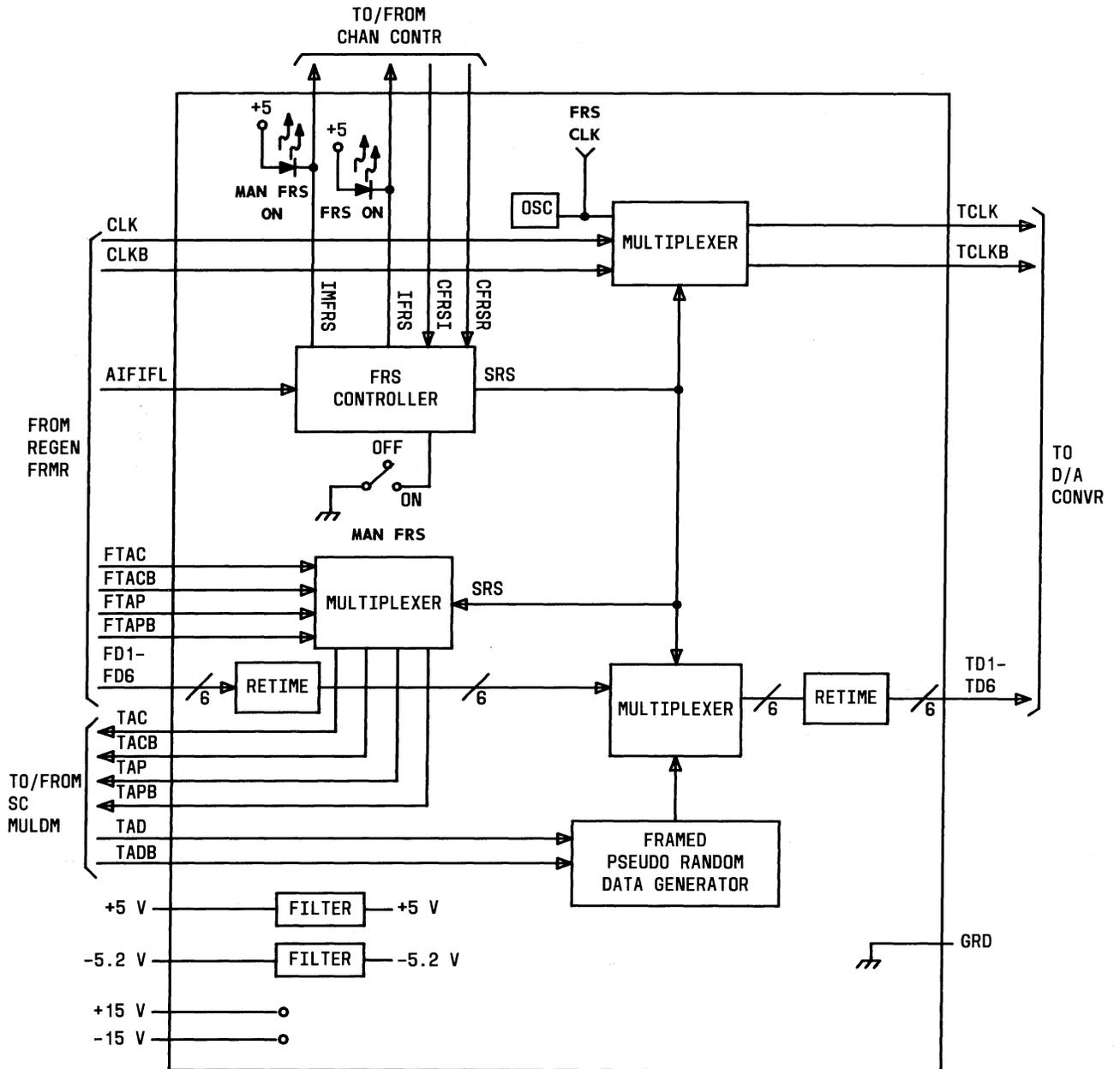


Fig. 32—AMR16/16B Frame Resupply Block Diagram

TABLE C			
SIGNAL INPUT/OUTPUT AND POWER REQUIREMENTS FOR AMR16/16B FRAME RESUPPLY			
DESIGNATION	PIN NO. (NOTE)	DESCRIPTION	SIGNAL
SIGNAL INPUT			
FD1-FD6	025,027,209,031, 033,035	Data rails	22.767 Mbaud, TTL
CLK	038	Clock	22.767 MHz, ECL
CLKB	037	Clock Inverse	22.767 MHz, ECL
FTAC	054	Framer Transmit Auxiliary Clock Inverse	384 kHz, TTL
FTACB	053	Framer Transmit Auxiliary Clock Inverse	384 kHz, TTL
FTAP	052	Framer Transmit Auxiliary Page	384 kHz, TTL
FTAPB	051	Framer Transmit Auxiliary Page Inverse	384 kHz, TTL
AIFIL	018	Frame Loss Indication	Normal = high
CFRSR	117	Control FRS Remote	Normal = low
CFRSI	017	Control FRS Inhibit	Normal = low
TAD	050	Transmit Auxiliary Data	384 kHz, TTL
TADB	049	Transmit Auxiliary Data Inverse	384 kHz, TTL
SIGNAL OUTPUT			
IFRS	016	FRS on Indication	Active low
IMFRS	116	MAN FRS on Indication	Active low
TAC	013	Transmit Auxiliary Clock	384 kHz, TTL
See note at end of table.			

TABLE C (Contd)			
SIGNAL INPUT/OUTPUT AND POWER REQUIREMENTS FOR AMR16/16B FRAME RESUPPLY			
DESIGNATION	PIN NO. (NOTE)	DESCRIPTION	SIGNAL
SIGNAL OUTPUT (Contd)			
TACB	113	Transmit Auxiliary Clock Inverse	384 kHz, TTL
TAP	012	Transmit Auxiliary Page	384 kHz, TTL
TAPB	112	Transmit Auxiliary Page Inverse	384 kHz, TTL
TCLK	138	Clock	22.767 MHz, ECL
TCLKB	137	Clock Inverse	22.767 MHz, ECL
TD1-TD6	135,133,131,129, 127,125	Data Rails	22.767 Mbaud, TTL
POWER			
+5 V	045-047,145-147	DC voltage input	+5 V dc, 800 mA
-5.2 V	040-043,140-143	DC voltage input	-5.2 V dc, 150 mA
+15 V	021,121	Not used	+15 V dc, 0 mA
-15 V	019,119	Not used	-15 V dc, 0 mA
GRD	000,001,005,024,026, 028,030,032,034,036, 039,049- 056,100,101, 104,124,126,128,130, 132,134,136,139,152, 155,156	Common return for all signals and voltages	Ground
Note: Unless otherwise indicated, all pin numbers are associated with the circuit pack backplane connector.			

AMR20 D/A (DIGITAL-TO-ANALOG) CONVERTER

The AMR20 D/A CONVR (Fig. 33) converts six input unipolar signals plus a clock into two quadrature 8-level baseband signals (BBI and BBQ). In a regenerator, the input signals are supplied by the frame resupply, the regenerator framer, or the 64-QAM decision units, depending on which is provided. In a terminal, the input signals are supplied by the CRC coder (if provided) or the frame generator.

The output BBI and BBQ signals are connected to the transmit filters.

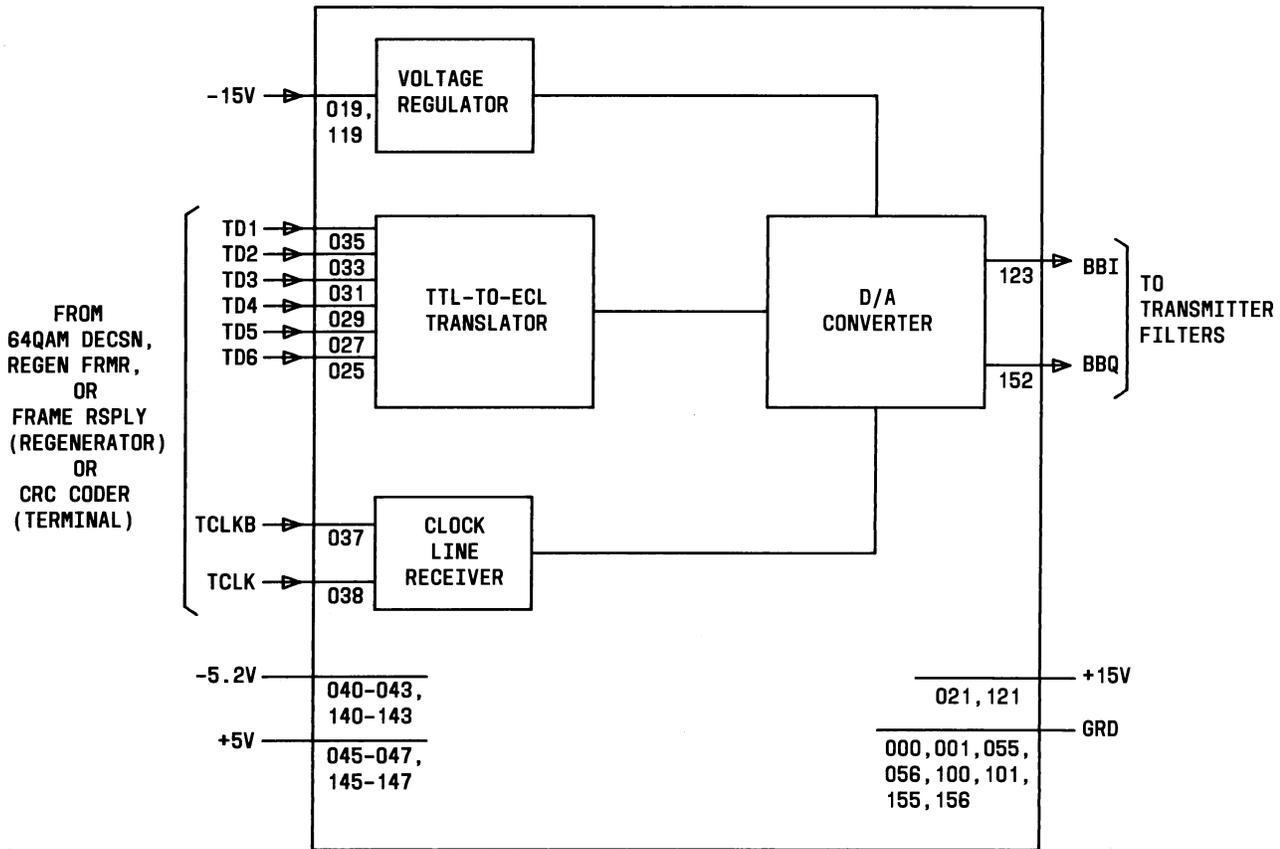


Fig. 33—AMR20 D/A Converter

AMR23 TRANSMIT FILTER

The AMR23 TRMT FLT (Fig. 34) limits the baseband frequency spectrum of the transmitter. It contains two identical low-pass filters, one for each rail of the system. Each filter presents half of the Nyquist shaping required for each rail. The other half is provided by the receive filter in the receive section of the system. Each filter section of the transmit filter circuit pack passes frequencies from dc to 11.3835 MHz and attenuates frequencies from 24 MHz to 100 MHz by 45 dB.

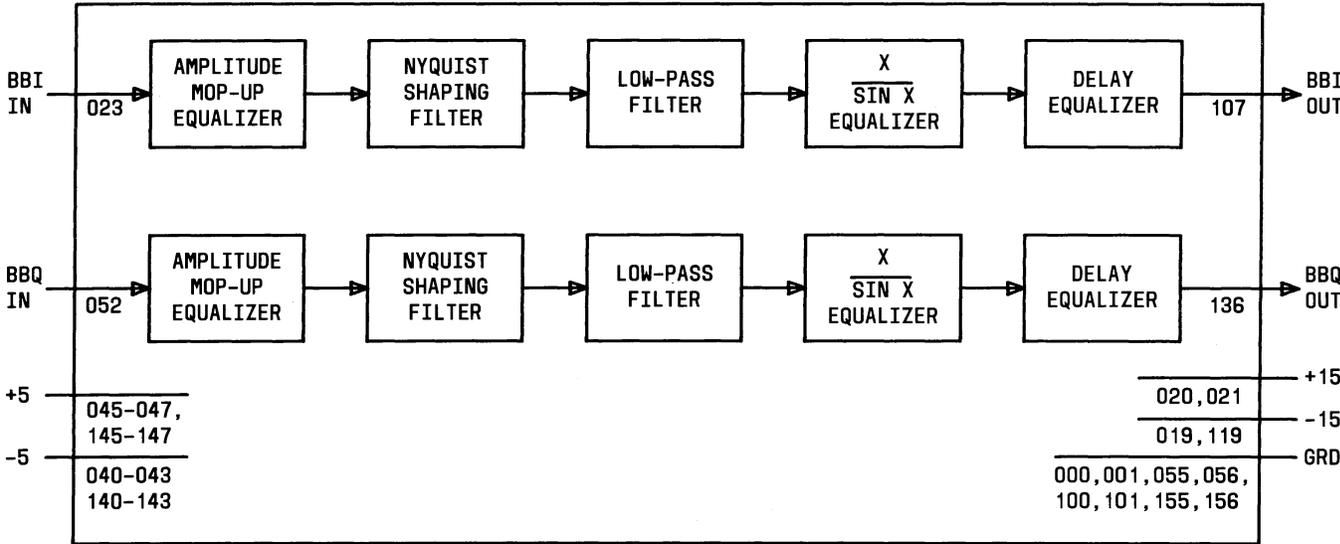


Fig. 34—AMR23 Transmit Filter

AMR27/28 64-QAM MODULATOR

The 64QAM MOD (Fig. 35) converts the two 8-level analog baseband input signals (I and Q) from the transmit filter into a single 64-state QAM IF signal at 70 MHz. The baseband amplifiers, A1 and A2, amplify the input I and Q signals and provide buffering and impedance matching between the Nyquist filters (located before the 64-QAM modulator) and the internal mixers. The low-pass filters provide a constant source impedance for the mixers and have a cutoff frequency of 51 MHz. Mixers then up-convert each signal to 70 MHz, each one having four amplitudes with two possible phase states apiece. The two 8-level IF signals are summed in amplifier A3 to form the 64-state QAM IF output signal. This IF signal is further amplified by amplifier A4, and then passed through a low-pass filter to the output. If the output power drops below -9 dBm, the OUTPUT LOSS LED lights. The output lead, AIMOL, permits external monitoring of the alarm.

Note: The AMR27 64QAM MOD unit is used when the IF cable is less than or equal to 50 feet long.

The AMR28 64QAM MOD unit is used when the IF cable is longer than 50 feet.

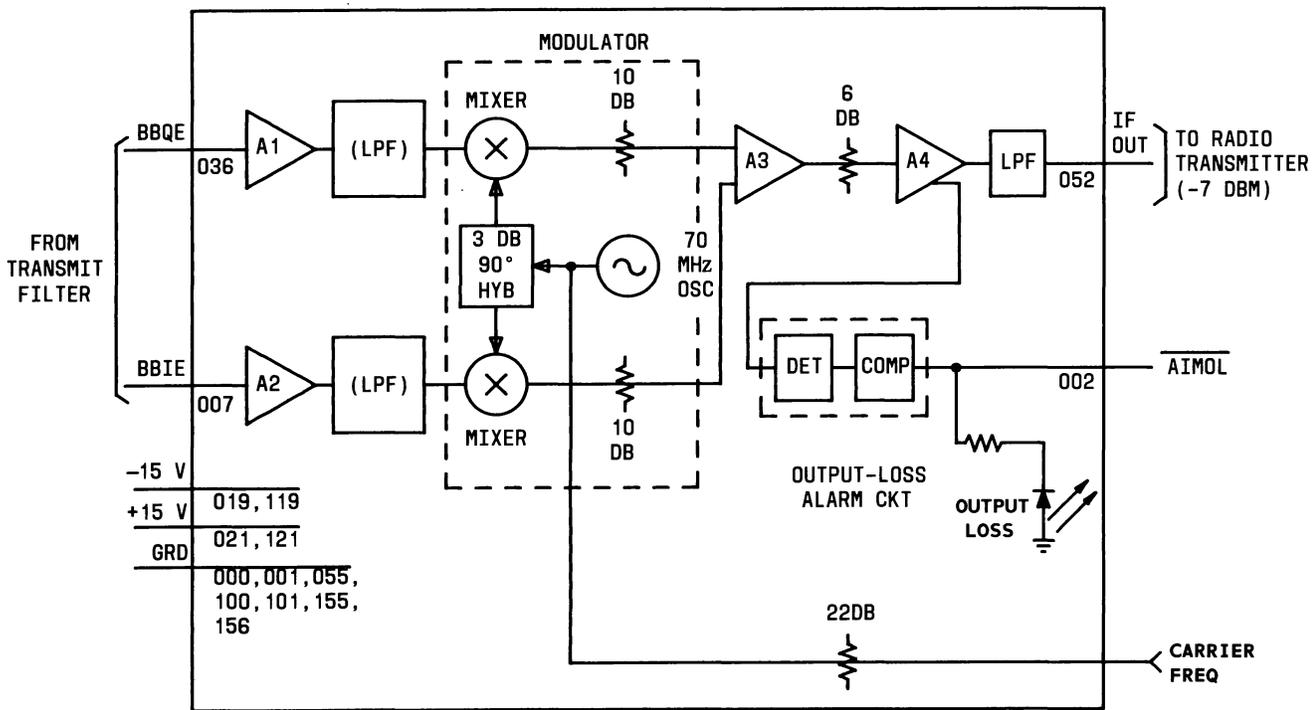


Fig. 35—AMR27/28 64-QAM Modulator

AMR29/30/229/230 64-QAM DEMODULATOR**FUNCTIONAL DESCRIPTION**

The 64QAM DEMOD circuit pack (Fig. 36) is used in the terminal and regenerator digital receiver shelves to convert the received 64-QAM double-sideband, suppressed carrier IF signal into two 8-level baseband signals. The 64QAM DEMOD also recovers the transmitted carrier for use in synchronously demodulating the IF signal.

There are four 64QAM DEMOD units, and they are identical in operation. They are distinguished, however, by their IF input loss. The AMR30 and AMR230 units are used when the IF interconnect cable from the associated radio receiver is less than or equal to 50 feet long. The AMR29 and AMR229 units are used when the IF interconnect cable is longer than 50 feet.

BLOCK DIAGRAM DESCRIPTION

The receiver 64-QAM double-sideband, suppressed carrier IF signal (IF IN) is first amplified to -5 dBm and then split into two -15 dBm signals. Each signal is then mixed with the recovered 70-MHz carrier. One signal is demodulated in-phase and the other at 90 degrees (quadrature). Each signal is then passed through a low-pass filter to remove unwanted out-of-band energy and then amplified to -9 dBm into 75-ohms.

The recovered carrier is provided by the VCO (voltage controlled oscillator) circuitry and is synchronized with the received carrier by phase detection signals (PH+ and PH-) from the CRLTR unit.

The 64QAM DEMOD units monitor the received carrier for loss of lock. If carrier lock-loss occurs, an amber faceplate LED (CARRIER LOCK LOSS) is lighted and an alarm signal (ICLL) is sent to the associated CHAN CONTR unit.

PINOUT DESCRIPTION

Refer to Table D for input/output and power information.

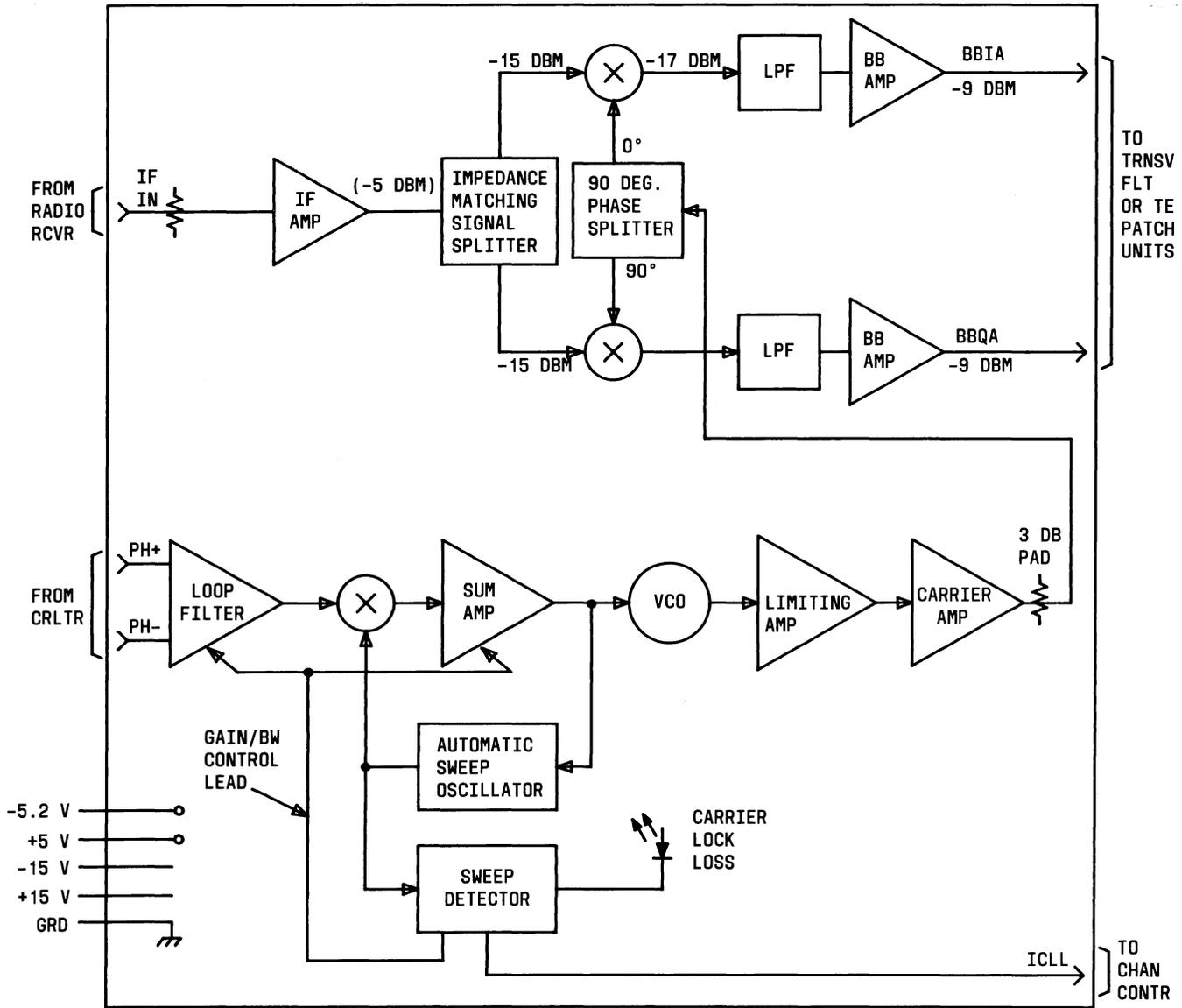


Fig. 36—AMR29/30/229/230 64-QAM Demodulator Block Diagram

TABLE D			
SIGNAL INPUT/OUTPUT AND POWER REQUIREMENTS FOR AMR29/30/229/230 64-QAM DEMODULATOR			
DESIGNATION	PIN NO. (NOTE)	DESCRIPTION	SIGNAL
SIGNAL INPUT			
IF IN	135	IF input	64-QAM 70-MHz -12 dBm, 75-ohms (AMR29/229) -8 dBm, 75-ohms (AMR30/230)
PH+	017	PLL filter input from CRLTR phase detector	DC voltage
PH-	117	PLL filter input from CRLTR phase detector	DC voltage
SIGNAL OUTPUT			
BBIA	154	8-level baseband (I)	8-level linear, -9 dBm, 75-ohms
BBQA	150	8-level baseband (Q)	8-level linear, -9 dBm, 75-ohms
ICLL	130	Carrier recovery lock-loss alarm	Normal = +9 V dc Alarm = less than 0 V dc
CARRIER LOCK LOSS	Faceplate LED (amber)	Out-of-lock indicator	OFF = in lock ON = out of lock
POWER			
-15 V	021,121	DC voltage input	-15 V dc, 268 mA
+15 V	019,119	DC voltage input	+15 V dc, 100 mA
+5 V	045-047,145-147	Not used	+5 V dc, 0 mA
-5.2 V	040-043,140-143	Not used	-5 V dc, 0 mA
GRD	000,001,034-036, 049-056,100,101, 134,136,149,151- 153,155,156	Common return for all signals and voltages	Ground
Note: Unless otherwise indicated, all pin numbers are associated with the circuit pack backplane connector.			

AMR32 TRANSVERSAL FILTER

FUNCTIONAL DESCRIPTION

The TRNSV FLT (transversal filter) circuit pack is used in the terminal and regenerator digital receiver shelves to reduce the intersymbol interference caused by multipath fading. Two TRNSV FLT units are required in each digital receiver, one for the I (in-phase) and one for the Q (quadrature) baseband signal. The TRNSV FLT and CRLTR units provide transversal equalization.

BLOCK DIAGRAM DESCRIPTION

The TRNSV FLT (Fig. 37) receives the BB IN (baseband signal) from the I or Q 64QAM DEMOD unit. This signal then passes through a series of seven synchronous complex-valued taps where both in-rail and cross-rail distortions are removed. The variable tap weight amplifiers are driven by control signals from the CRLTR unit to output the appropriate delayed or advanced XRO (cross-rail signal) to the adjacent TRNSV FLT unit. The XRI (cross-rail input signal) is summed with the main signal to cancel the cross-rail coupling and intersymbol interference.

PINOUT DESCRIPTION

Refer to Table E for signal input/output and power information.

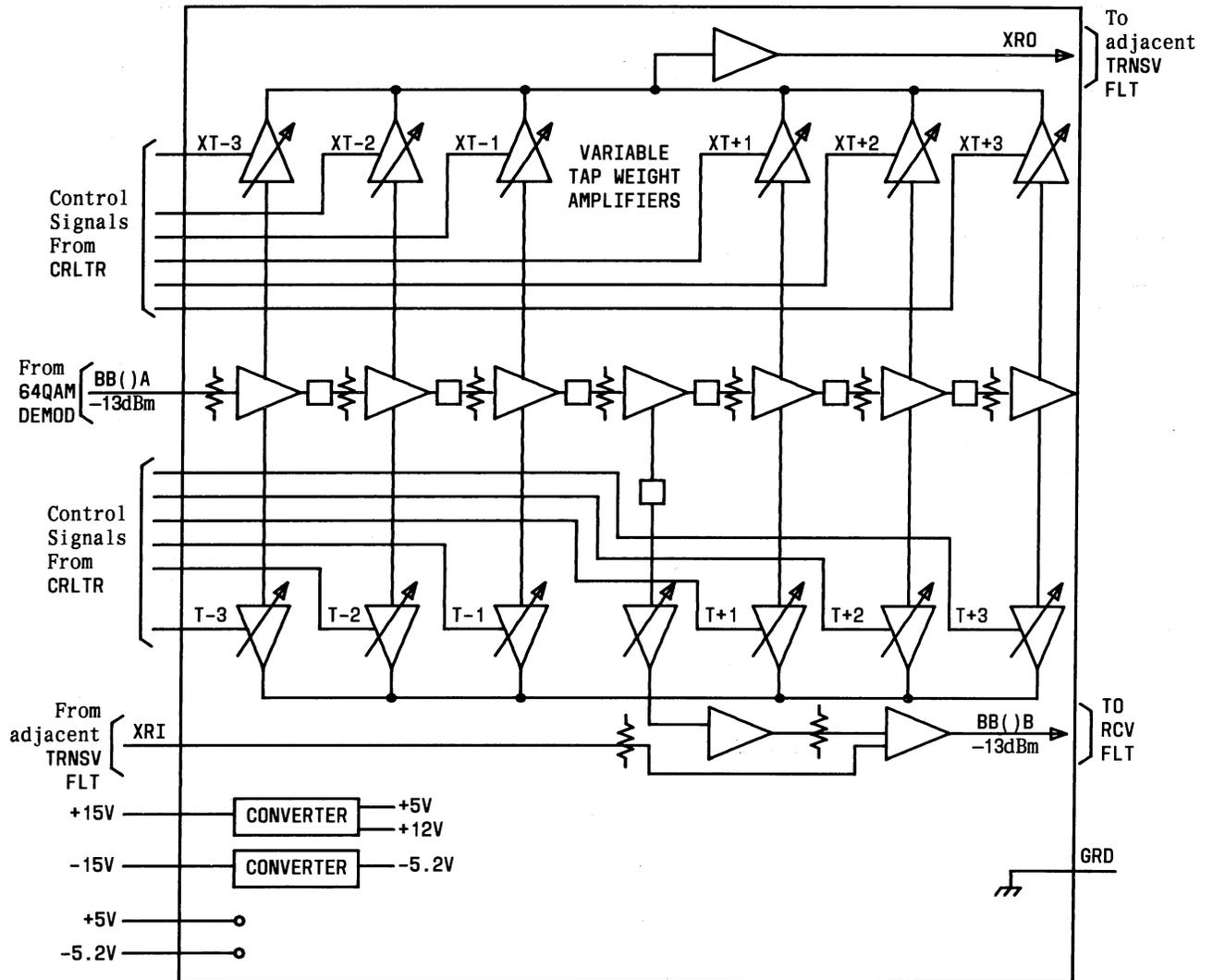


Fig. 37—AMR32 Transversal Filter Block Diagram

TABLE E SIGNAL INPUT/OUTPUT AND POWER REQUIREMENTS FOR AMR32 TRANSVERSAL FILTER			
DESIGNATION	PIN NO. (NOTE)	DESCRIPTION	SIGNAL
SIGNAL INPUT			
BB()A	054	Baseband in (I or Q)	8-level linear, -13 dBm, 75-ohm
Control Signals	048,108,110,112, 114,116,118,124, 127,128,130,148	Control signals for operating tap weight amplifiers	DC voltage
XRI	032,138	Cross-rail baseband in	8-level linear
SIGNAL OUTPUT			
BB()B	102	Equalized baseband out (I or Q)	8-level linear, -13 dBm, 75-ohm
XRO	035,135	Cross-rail baseband out	8-level linear
POWER			
+15 V	021,121	DC voltage input	+15 V dc, 300 mA
-15V	019,119	DC voltage input	-15 V dc, 200 mA
+5V	045-046,145-146	Not used	+5 V dc
-5.2V	040-043,140-143	Not used	-5.2 V dc
GRD	000-003,031,033, 034,036-039,053, 055,056,100,101, 103,131-134,139, 153-156	Common return for all signals and voltages	Ground
<p>Note: Unless otherwise indicated, all pin numbers are associated with the circuit pack backplane connector.</p>			

AMR34B/234 CORRELATOR**FUNCTIONAL DESCRIPTION**

The AMR34B/234 CRLTR circuit pack is used in both the terminal and regenerator digital receiver shelves. It contains the phase detector circuitry required for carrier recovery. It also provides the control signals required to operate the TRNSV FLT (transversal equalizer) units, if equipped.

A baseband adaptive transversal equalizer that provides equalization for transmission impairments caused by multipath fading is implemented using the CRLTR and two TRNSV FLT units. Equalization is provided using tapped delay lines that equalize the delay line TRNSV FLT units, one for each rail, by monitoring the intersymbol interference of each baseband signal.

BLOCK DIAGRAM DESCRIPTION

The CRLTR (Fig. 38) receives the clock and data signals from the I and Q 64QAM DECSN units and correlates the data for various combinations of symbol periods. The results are averaged to derive the control signals. Signals from different symbol periods are obtained by the shift registers with correlation taking place using EXCLUSIVE OR gates. The averaging is accomplished with balanced integrators to produce control voltages that control the gain of the tap weight amplifiers on the TRNSV FLT units.

PINOUT DESCRIPTION

Refer to Table F for signal input/output and power information.

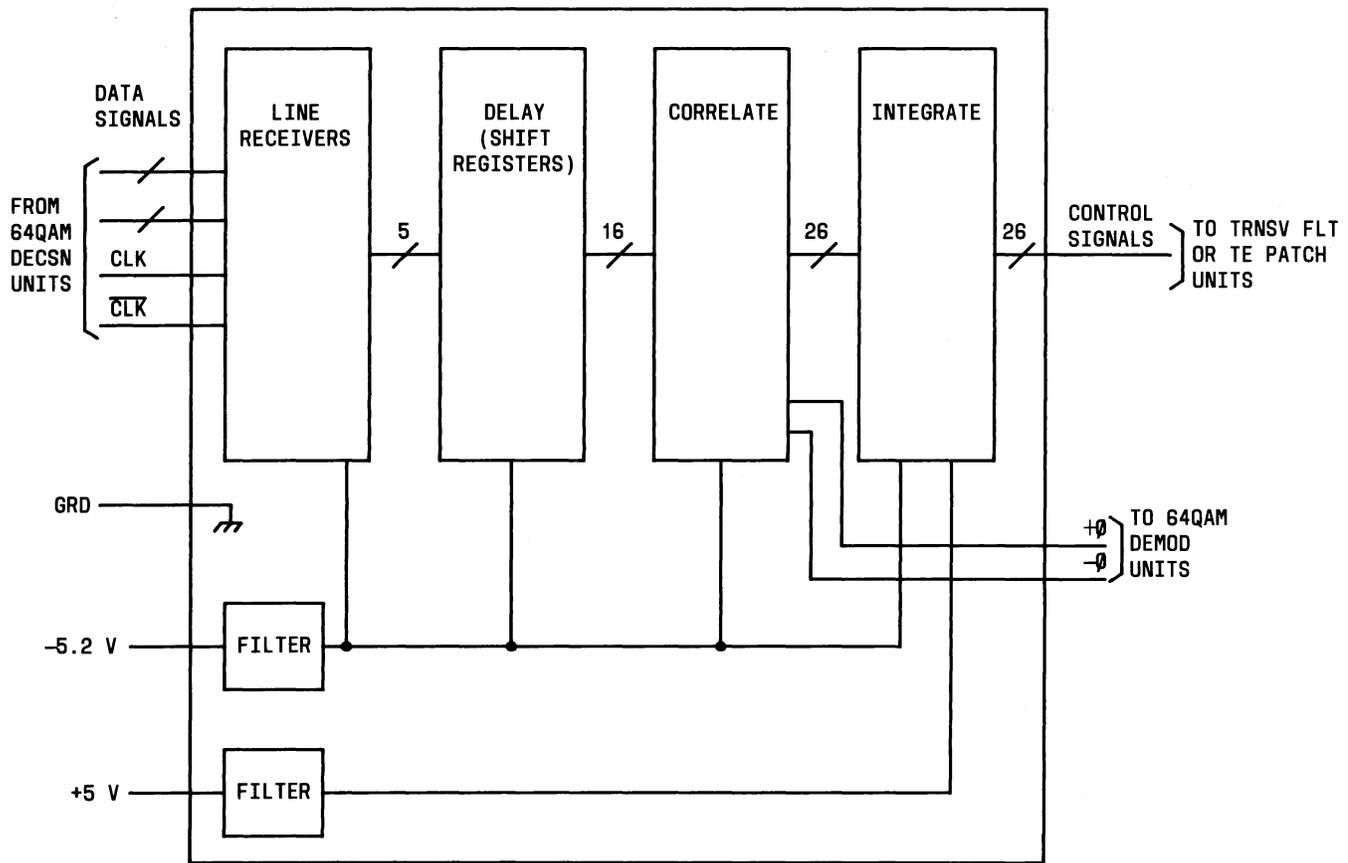


Fig. 38—AMR34B/234 Correlator Block Diagram

TABLE F
SIGNAL INPUT/OUTPUT AND POWER REQUIREMENTS
FOR AMR34B/234 CORRELATOR

DESIGNATION	PIN NO. (NOTE)	DESCRIPTION	SIGNAL
SIGNAL INPUT			
DATA SIGNALS	031,131,032,132, 033,133,034,134, 025,125,026,126, 022,122,023,123	Data Signals	22.767 Mbaud, ECL
CLK	135	Clock	22.767 MHz, ECL
CLK	136	Clock Inverse	22.767 MHz, ECL
SIGNAL OUTPUT			
CONTROL SIGNALS	008,010,012,013,014, 016,018,024,027- 30, 049,051,108,110,112, 114,116,118,124,127, 128,130,149,151	Control signals for TRNSV FLT tap weight amplifiers	Low frequency (less than 200 Hz)
0+	017	Carrier recovery phase detector signals	DC voltage
0-	117	Carrier recovery phase detector signals	DC voltage
POWER			
-5 V	040-043,140-143	DC voltage input	-5.2 V dc, 1332 mA
+5 V	045-047,145-147	DC voltage input	+5 V dc, 32 mA
GRD	000,001,055,056, 100,101,155,156	Common return for all output signals and voltages	Ground
Note: Unless otherwise indicated, all pin numbers are associated with the circuit pack backplane connector.			

AMR37 RECEIVE FILTER

The AMR37 RCV FLT (Fig. 39) limits the baseband frequency spectrum of the receiver. It contains two identical low-pass filters, one for each rail of the system. Each filter provides one-half of the Nyquist shaping required for each rail. The other half of the Nyquist shaping is provided by the transmit filter in the transmit section of the system. Each filter of the receive filter circuit pack passes frequencies from dc to 11.3835 MHz and attenuates frequencies from 24 to 100 MHz by 45 dB.

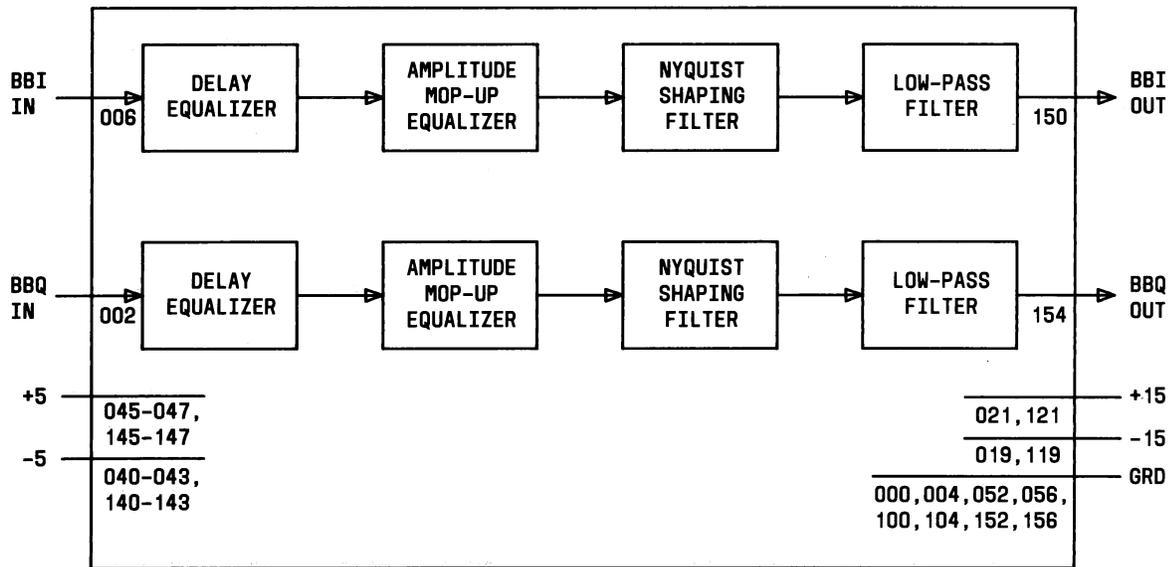


Fig. 39—AMR37 Receive Filter

AMR43/43B 64-QAM DECISION

The 64QAM DECSN (Fig. 40) regenerates the original three data signals with the use of a 6-bit A/D converter and passes them on to either the regenerator framer or the terminal framer unit.

Secondary functions necessary for proper A/D conversion are clock recovery to sample the signal at the proper time and threshold circuits to establish the proper references. Clock recovery is accomplished through the use of a phase-lock loop. This circuit derives a clock of the proper frequency and phase and maintains the sample time at the center of the received eye. The threshold circuits also use a decision directed algorithm to derive the top, center, and bottom references that are necessary to perform the A/D process.

The data signals and clock are output to the correlator unit for carrier recovery phase detection and transversal equalizer. Samples of the input baseband signal and the recovered clock are available at jacks on the printed wiring board of the AMR43 unit or at the faceplate of the AMR43B unit. Both units provide a faceplate jack for pseudo error sampling.

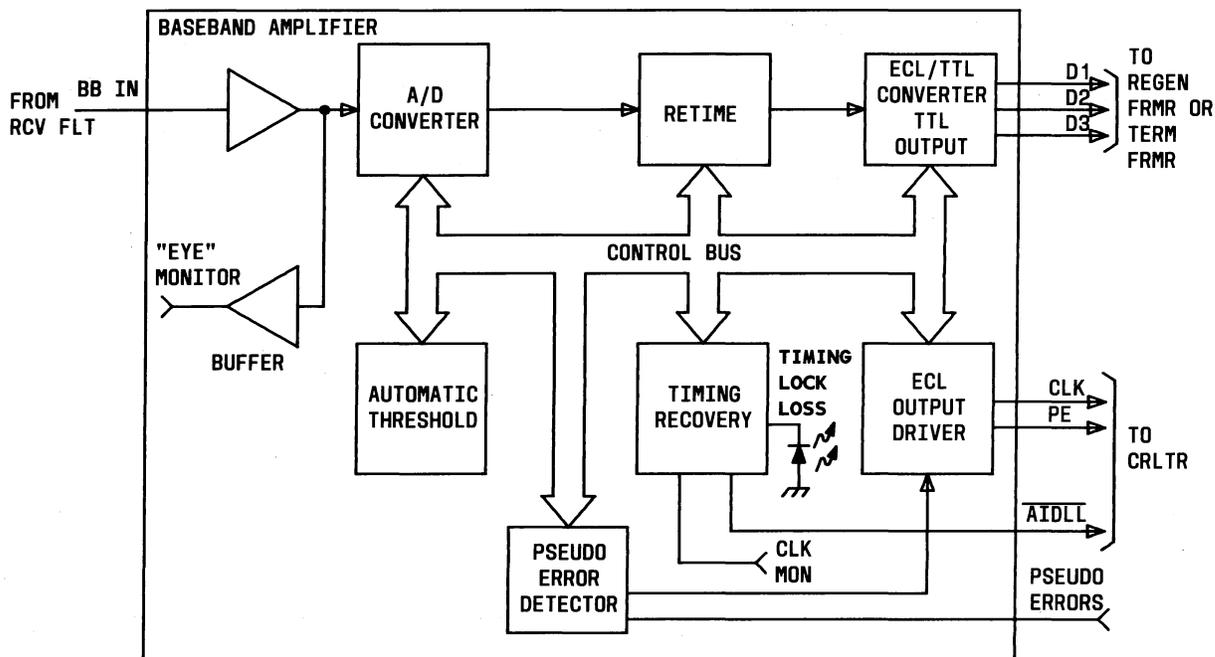


Fig. 40—AMR43/43B 64-QAM Decision

AMR47 TRANSVERSAL EQUALIZER PATCH

The AMR47 TE PATCH (Fig. 41) is used when the AMR32 Transversal Filter is not equipped. The AMR47 allows the BBI and BBQ outputs of the 64-QAM Demodulator to be passed on to the AMR37 Receive Filter.

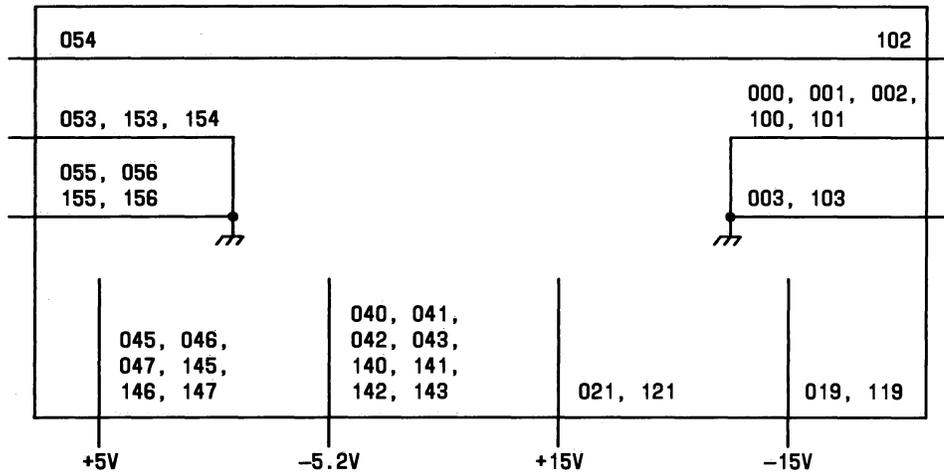


Fig. 41 — AMR47 Transversal Equalizer Patch

AMR55 LINE ALIGNMENT

The AMR55 LINE ALNMT (Fig. 42) adjusts delay on the protection channel feed to the first regular channel line switch so that the two channels may be properly aligned for errorless switching. The AMR55 also provides a feed to all other line switches through an expansion feed to the growth line distribution circuits (AMR61). The AMR55 passes the protection channel feed on to the rest of the protection channel unchanged.

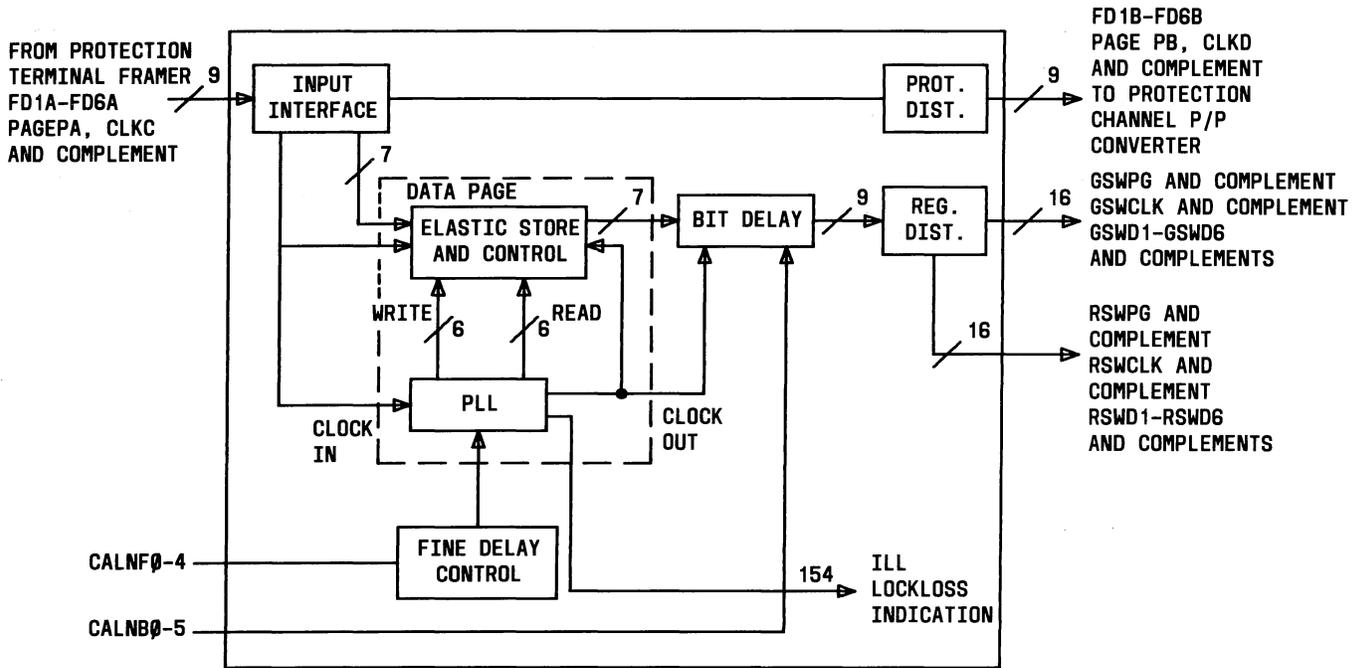


Fig. 42—AMR55 Line Alignment

AMR59 REGENERATOR FRAMER

The AMR59 REGEN FRMR (Fig. 43) is an optional circuit pack that receives clock and data from the decision circuit packs. The regenerator framer performs two functions:

- Monitors the transmitted data
- Provides service channel access.

The regenerator framer monitors the transmitted data for the frame pattern and compares the received CRC bits with CRC bits computed internally. If a valid frame pattern cannot be found, the AIFIFL lead goes low to signal the frame resupply and the channel controller that the received data is worthless. When framing is accomplished, the regenerator framer provides the channel controller with error indications from the CRC comparison.

The regenerator framer works with the service channel muldem to provide service channel access at a regenerator. Received service channel data, clock, and page signals (RAD, RAC, and RAP) are sent to the service channel muldem. After the service channel data is extracted from the data stream, it may be replaced by the transmit service channel data (TAD). Six control leads from the service channel muldem determine if the data is to be passed through or substituted on the six service channels. If substituted, the data will be internally generated pseudo data that maintains frame format. The transmit service channel data is synchronized with the regenerator framer by transmit clock and page symbols (FTAC and FTAP).

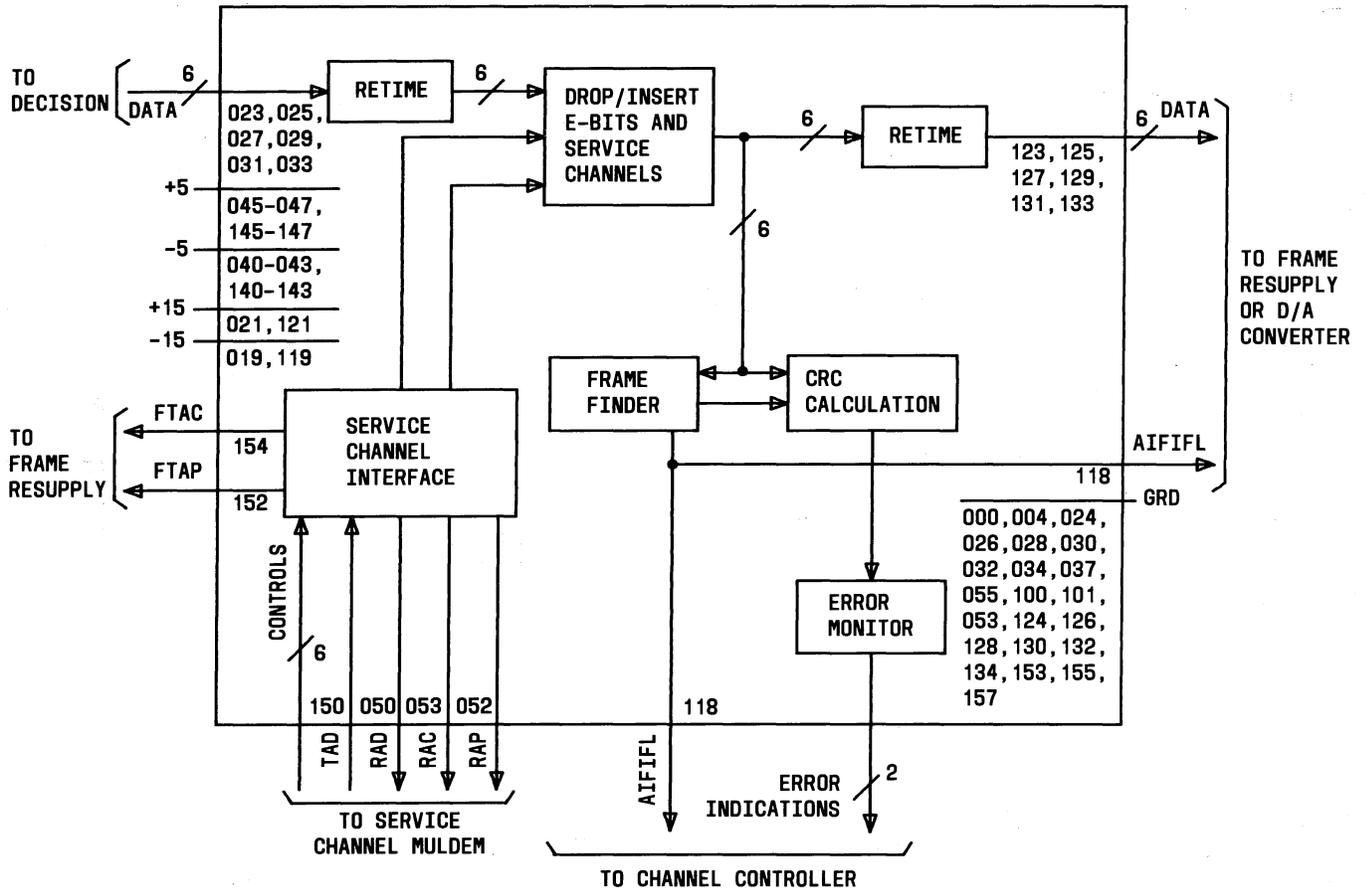


Fig. 43—AMR59 Regenerator Framer

AMR60 TERMINAL FRAMER

The AMR60 TERM FRMR (Fig. 44) has four functions:

- Finds the frame pattern to synchronize itself and the rest of the DPU with the received data
- Determines the quadrant rotation due to carrier phase ambiguity
- Monitors the error rate using the CRC bits and the error correction indication
- Extracts the service channel data and sends this data, a clock, and a page signal to the service channel muldem board (ANB1).

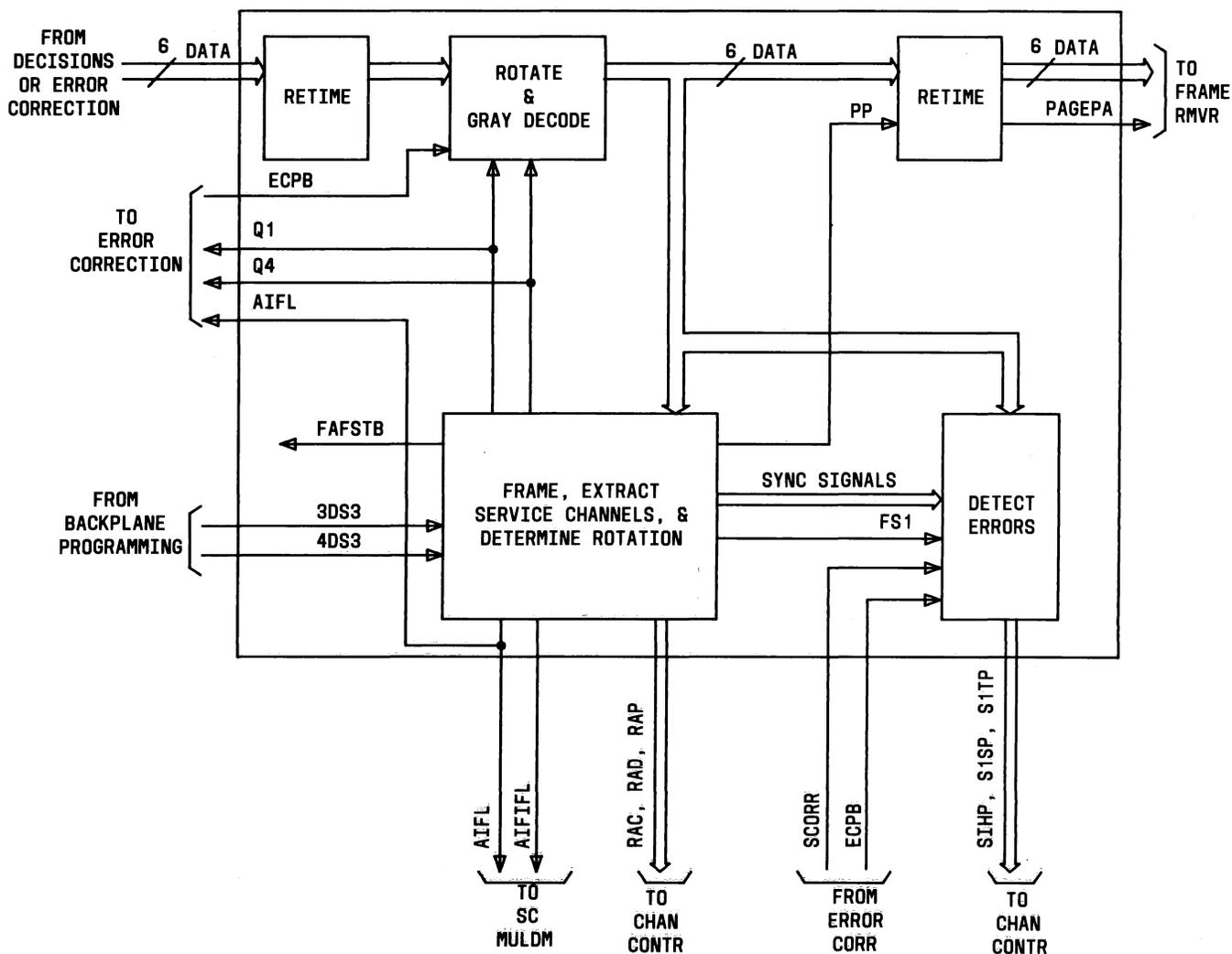


Fig. 44—AMR60 Terminal Framer

AMR61 GROWTH LINE DISTRIBUTION

The AMR61 GR LN DISTN (Fig. 45) receives data, page, and clock signals (and their complements) from the AMR55 Line Alignment. The AMR61 then distributes (fans out) the incoming signal to all of the faceplate ports. A selected channel determines which line selector will receive the channel signals from the AMR61.

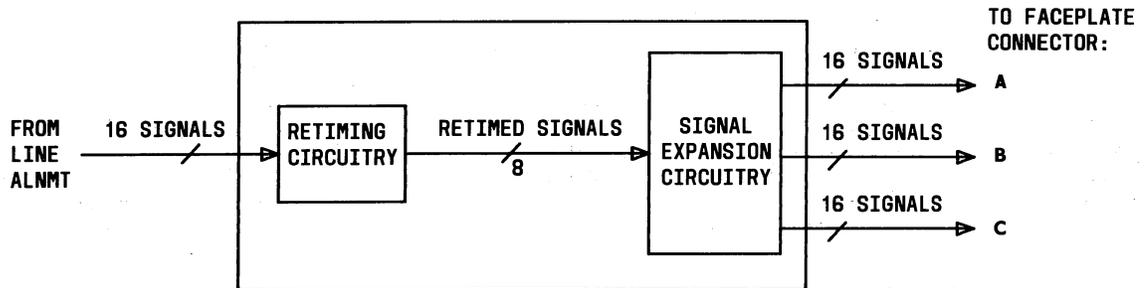


Fig. 45—AMR61 Growth Line Distribution

AMR65 LINE SWITCH

The AMR65 LINE SW (Fig. 46) provides protection switching at the 64-QAM point of a regular channel. When a head-end bridge is connected, the AMR65 switch receives the same data from two points: regular transmission from the terminal framer unit and protection channel transmission from the line alignment unit. The logic in the AMR65 switch can then be directed to transmit the protection channel transmission path. Later, when the regular channel transmission path is restored, the AMR65 will be switched to transmit the regular channel transmission.

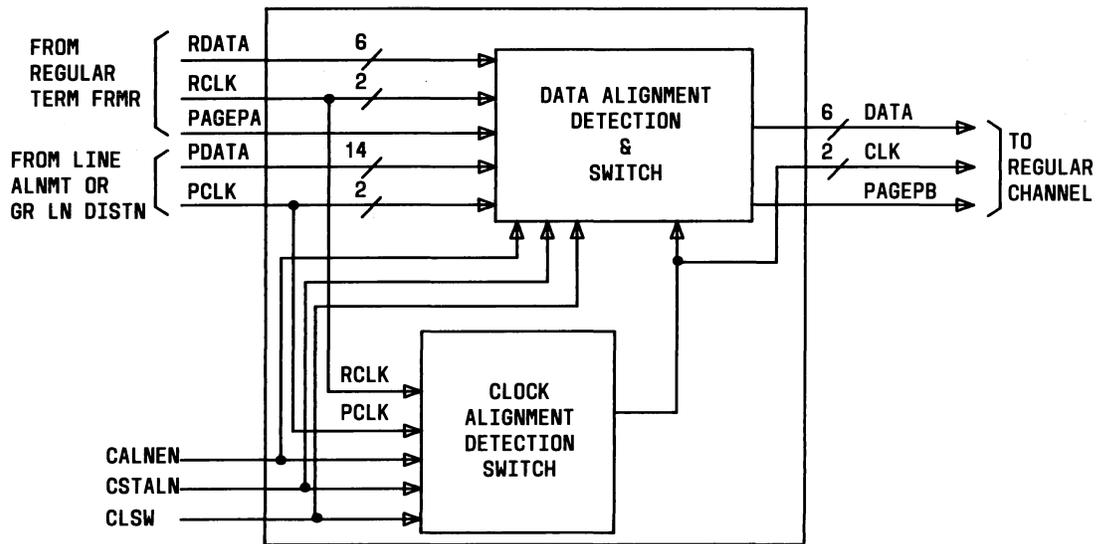


Fig. 46—AMR65 Line Switch

AMR72/72B VMR AND CODER

The AMR72 VMR & CODER (Fig. 47) receives data, clock, and enable signals from the frame remover. The elastic store portion of the AMR72 then removes the 64-QAM radio frame overhead bits, performs a parallel-to-serial conversion, and recovers the DS3 clock from the input high-speed clock. This clock and serial data are then sent to the violation monitor portion of the AMR72. This section of the AMR72 examines the data and clock for frame errors, parity errors, or logic errors. The outputs of the violation monitor go to the AMR72 coder section and to the AMR72 control logic. If a good signal is detected, the coder portion of the circuit outputs the appropriate signals to the DS3 output circuit that takes the pulses and forms the DS3 signals. When the violation monitor detects errors in the clock data signals, the control logic determines the type of errors and sends the appropriate response to the violation monitor and coder portions of the AMR72. The control section also has the capability to be controlled by the system firmware, which, in turn, allows the AMR72 to be monitored and updated as necessary.

The AMR72B VMR & CODER provides the same functions as the AMR72 plus the capability to allow external monitoring of DS3 signals.

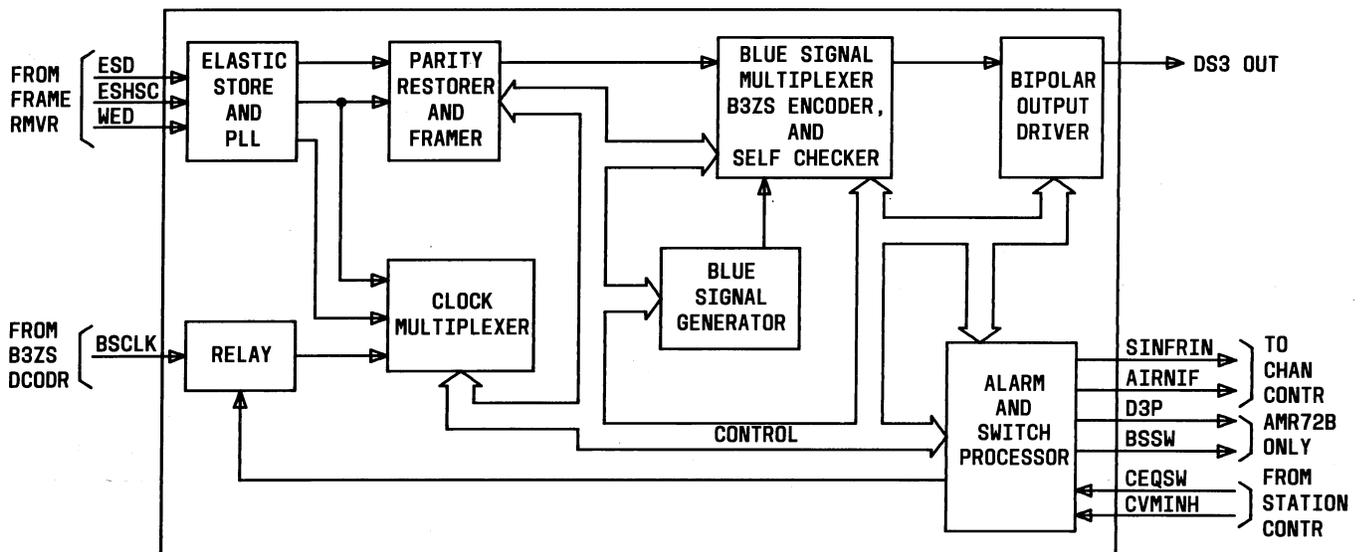


Fig. 47—AMR72/72B VMR and Coder

AMR75 FRAME REMOVER

The AMR75 FRAME RMVR (Fig. 48) has two main functions: descrambles incoming data and converts the six incoming data rails to two or three rails, depending on whether the system is 2-DS3 or 3-DS3. Each rail is sent to the receive elastic store portion of the VMR & CODER and is accompanied by an indication of whether it is a customer information bit or an inserted framing bit. The elastic store uses this indication to decide which bits must be removed from the data stream.

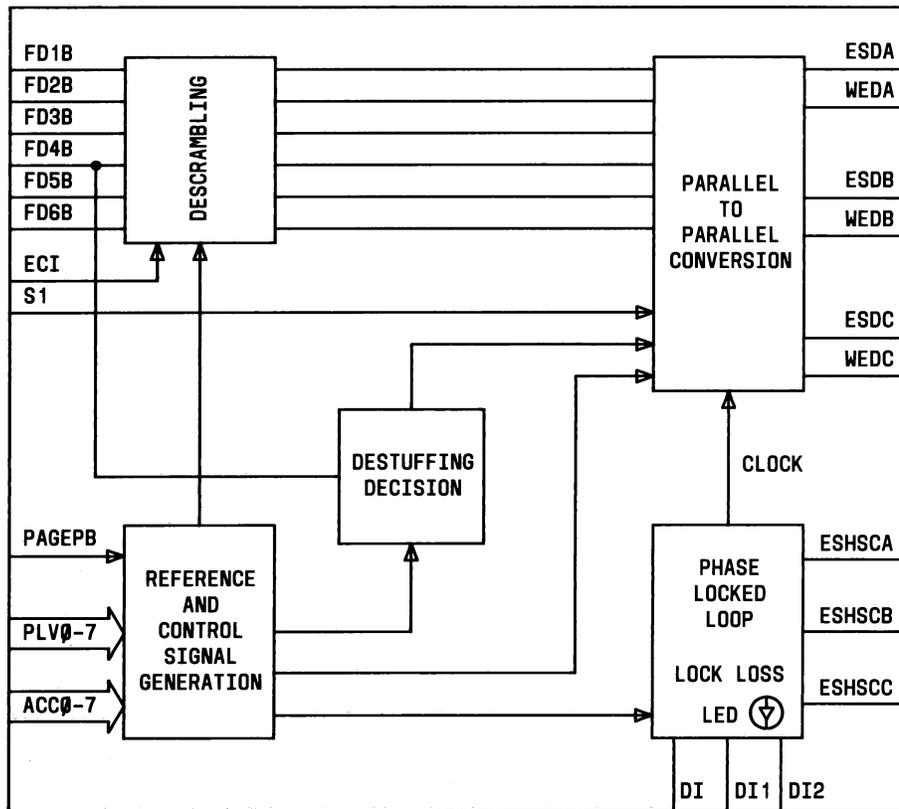


Fig. 48—AMR75 Frame Remover

AMR91 TERMINAL ORDER WIRE

The AMR91 TERM OW (Fig. 49) contains all of the voice frequency communications and signaling for the order-wire system. It consists of two major circuits:

- Voice frequency transmission
- Controlling logic.

The voice frequency section is further divided into two functions:

- Detects touch-tone signaling for the order-wire system that alerts personnel with an audible device
- Provides, on an optional basis, a DDD (direct distance dialing) interface.

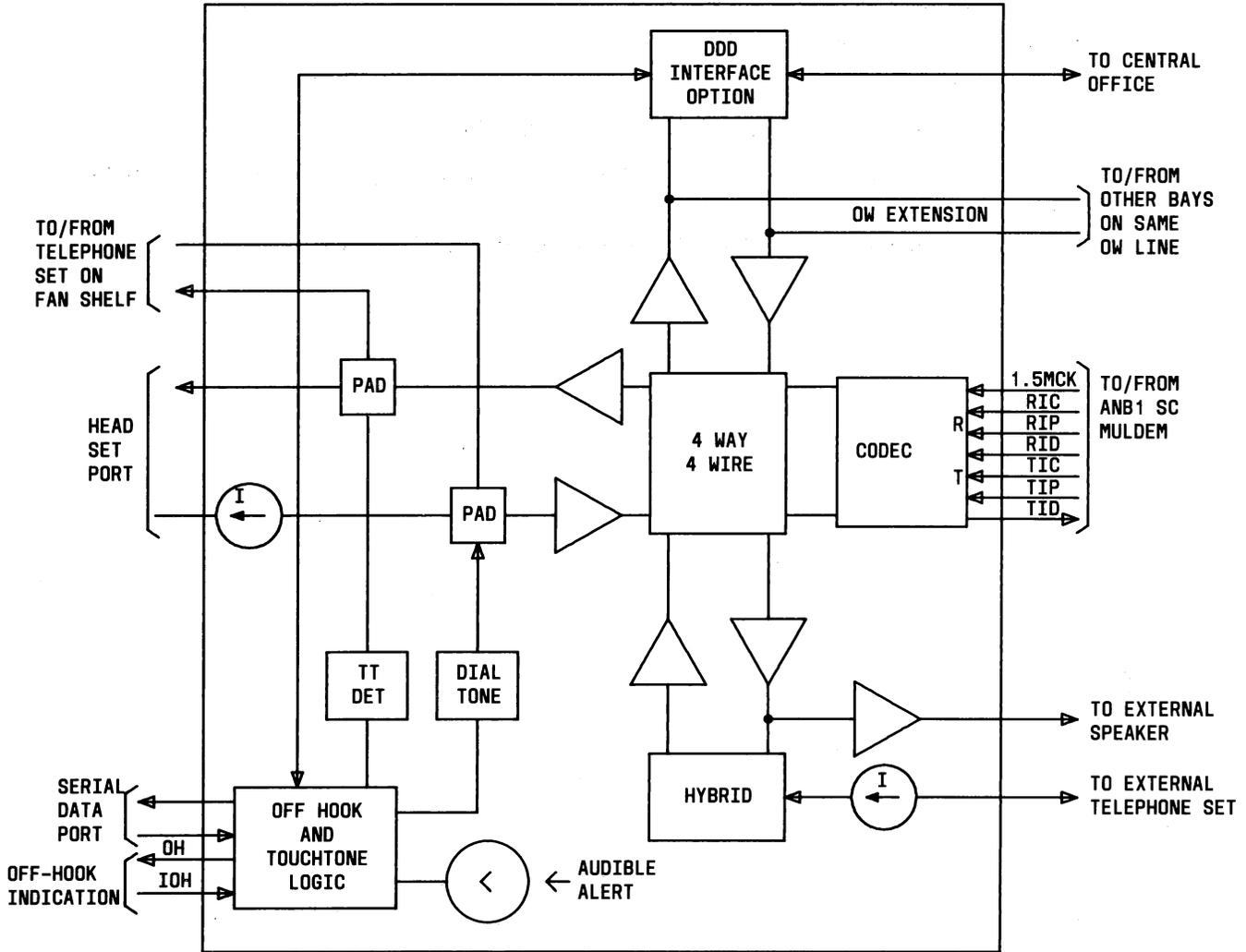


Fig. 49—AMR91 Terminal Order Wire

AMR94 SERVICE CHANNEL EXPANSION

The AMR94 SC EXPN (Fig. 50) supplies power and a physical interface for the 210-type modules that provide channels X, Y, and Z.

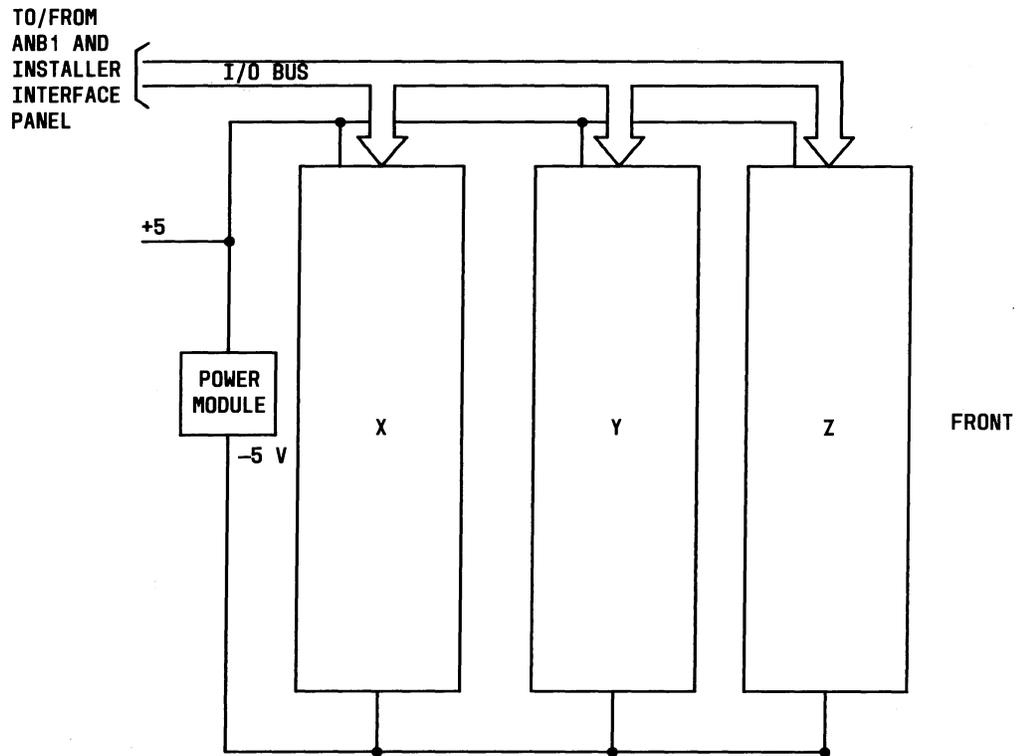


Fig. 50—AMR94 Service Channel Expansion

AMR95 REGENERATOR ORDER WIRE

The AMR95 REGEN OW (Fig. 51) contains all of the voice frequency communications and signaling for the order-wire system. It consists of two major circuits:

- Voice frequency transmission (detects touch-tone signaling for the order-wire system and alerts personnel with an audible device)
- Controlling logic.

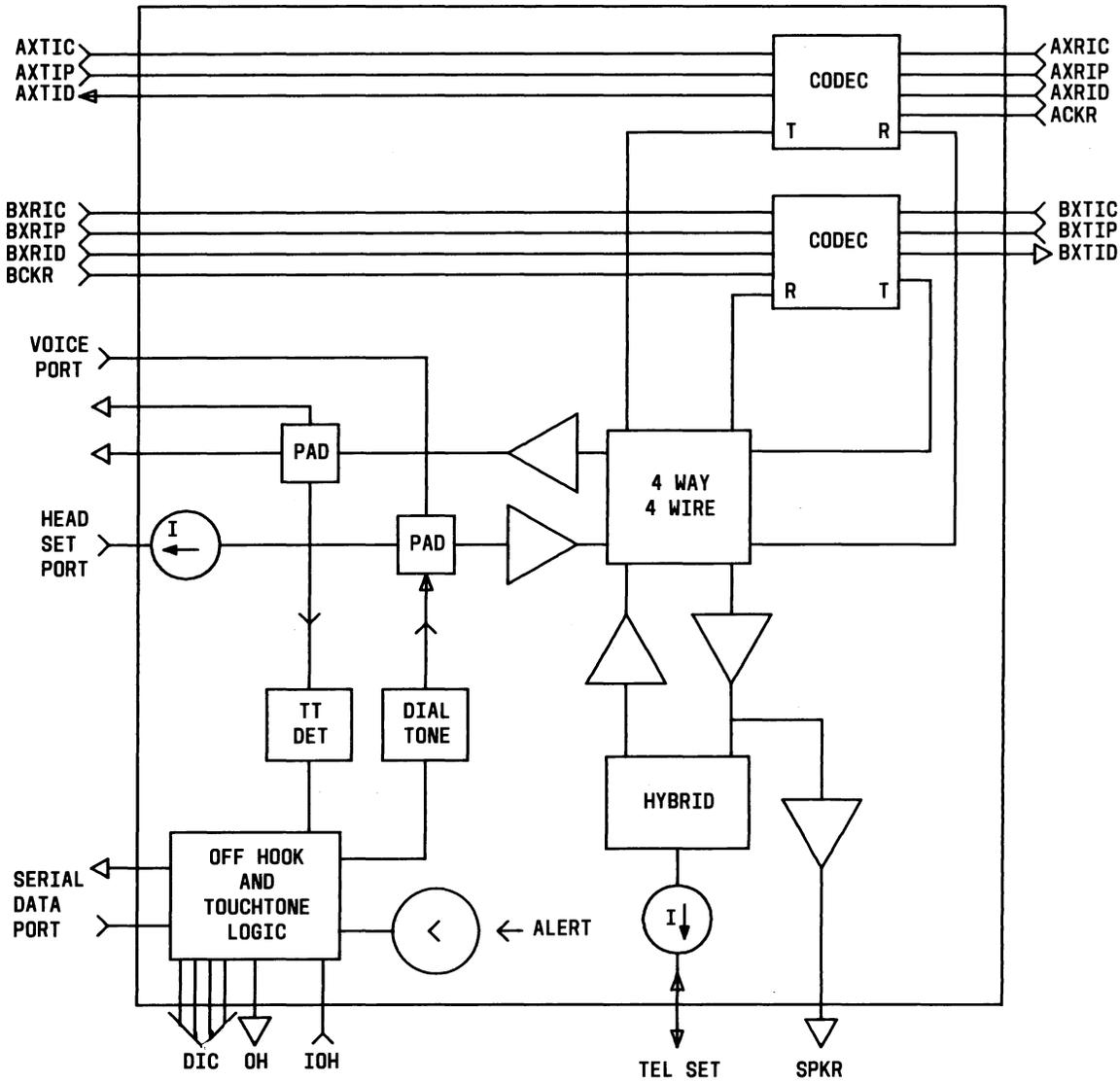


Fig. 51—AMR95 Regenerator Order Wire

AMR105 DISCRETE TELEMETRY**FUNCTIONAL DESCRIPTION**

The DSCRT TELEM (discrete telemetry) circuit pack is located in the control and service channel shelf to provide a discrete telemetry interface. This circuit pack has 24 scan point relays and 19 control point inputs. It is initialized and controlled by the station controller via an external 8-bit data bus. It is also shielded on both sides to minimize electromagnetic interferences.

BLOCK DIAGRAM DESCRIPTION

The block diagram in Fig. 52 complements the following description for the discrete telemetry circuit pack.

Primary Bus Interface

The primary bus interface for the DSCRT TELEM circuit pack consists of:

- An 8-bit bidirectional data bus (EAD0 through EAD7)
- The four least significant leads of the external address bus (ELA0 through ELA3)
- A chip select lead (ECS)
- A reset signal (ERES)
- The read and write control signals (ERD, EWR).

The 8-bit data bus provides the communication link between the DSCRT TELEM circuit pack and the station controller. The address and chip select signals are involved in device selection processing. The read and write signals control the direction of signal flow on the interface. The external reset signal, when logically high, forces the programmable ports on the DSCRT TELEM circuit pack into a reset mode. All signals in the primary bus interface are controlled by the station controller.

Address Decoding

The address decoding circuit in the DSCRT TELEM circuit pack has the ability to decode 16 contiguous address locations. Only eight locations are actively used in this design. Signals ECS, ELA2, and ELA3 drive the internal address decoder circuit. When the chip select signal is active low, address signals ELA2 and ELA3 internally activate one of the two local chip select signals (chip 1 or chip 2). Address signals ELA0 and ELA1 provide the two internal chip select signals with four possible address locations each, for a total of eight address locations. All addressable locations in the DSCRT TELEM circuit pack are used for selecting one of eight 8-bit parallel ports used in implementing the discrete telemetry interface.

Remote Scan Point Outputs

Twenty-four make contact relays (SP1 through SP24) are provided as the remote scan point interface to a discrete telemetry system. The relays feature mercury-wetted sealed contacts for chatter free operation and a maximum contact rating of 25 VA or 1 ampere.

Remote Control Point Inputs

Nineteen parallel inputs (CP1 through CP19) are available on the DSCRT TELEM circuit pack as the control point telemetry interface. All 19 inputs are equipped with a 1 k Ω pull up resistor to +5 volts dc and require a closure-to-circuit ground to properly activate them. As with the relays, the parallel inputs interface to the external 8-bit data bus (EAD0 through EAD7) through programmable parallel ports PPI 5 and PPI 9 as shown in the block diagram.

Internal <TEST> Loopback

The block diagram shows a signal defined as <TEST>. The intention of this signal is to provide the station controller the ability to detect whether the DSCRT TELEM circuit pack is inserted and properly initialized. The <TEST> signal is initialized low by the station controller and is constantly monitored via port PPI 9C. If this signal is ever read logically high by the station controller, the DSCRT TELEM circuit pack is either missing from the shelf or is not properly initialized.

PINOUT DESCRIPTION

Refer to Table G for signal input/output and power information.

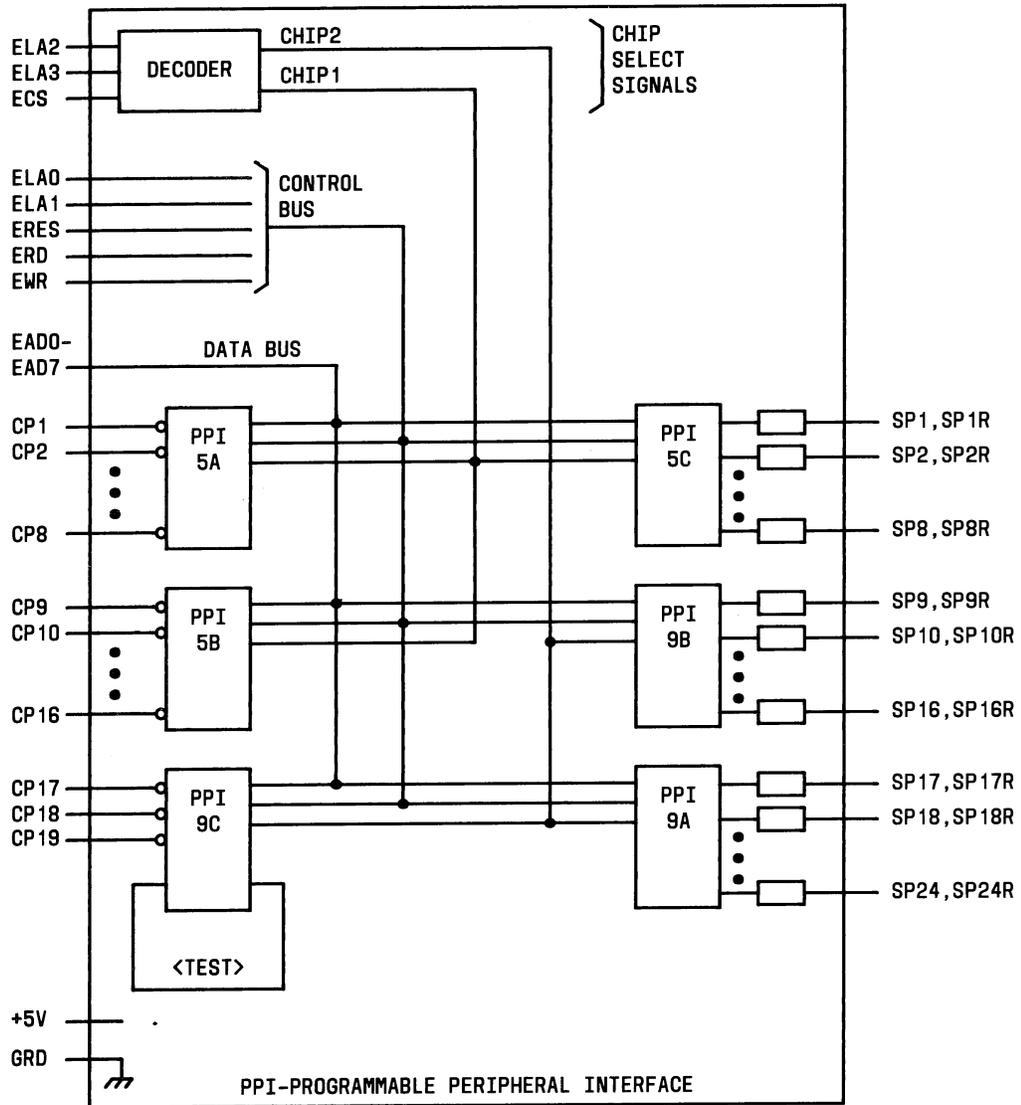


Fig. 52—AMR105 Discrete Telemetry Block Diagram

TABLE G			
SIGNAL INPUT/OUTPUT AND POWER REQUIREMENTS FOR AMR105 DISCRETE TELEMETRY			
DESIGNATION	PIN NO. (NOTE)	DESCRIPTION	SIGNAL
SIGNAL INPUT			
CP1,CP2,CP3,CP4 CP5,CP6,CP7,CP8 CP9,CP10,CP11,CP12 CP13,CP14,CP15,CP16 CP17,CP18,CP19	114,014,113,013 112,012,111,011 148,048,139,039 137,037,136,036 135,035,134	Control point inputs	TTL (active-low)
EAD0-EAD7	002,102,003,103 004,104,005,105	External latched data bus (bidirectional)	TTL
ECS	127	External address decoding signal	TTL
ELA0-ELA3	008,108,009,109	External latched address bus	TTL
ERD	006	External read control line	TTL (active-low)
ERES	007	External reset signal	TTL (active-high)
EWR	106	External write control line	TTL (active-low)
SIGNAL OUTPUT			
EAD0-EAD7	002,102,003,103 004,104,005,105	External latched data bus (bidirectional)	TTL
(SP1,SP1R),(SP2,SP2R) (SP3,SP3R),(SP4,SP4R) (SP5,SP5R),(SP6,SP6R) (SP7,SP7R),(SP8,SP8R) (SP9,SP9R),(SP10,SP10R) (SP11,SP11R),(SP12,SP12R) (SP13,SP13R),(SP14,SP14R) (SP15,SP15R),(SP16,SP16R) (SP17,SP17R),(SP18,SP18R) (SP19,SP19R),(SP20,SP20R) (SP21,SP21R),(SP22,SP22R) (SP23,SP23R),(SP24,SP24R)	(154,054),(152,052) (151,051),(150,050) (133,033),(122,022) (144,044),(153,053) (118,018),(117,017) (116,016),(115,015) (124,024),(123,023) (110,010),(138,038) (132,032),(131,031) (130,030),(129,029) (128,028),(127,027) (126,026),(125,025)	Scan point outputs and returns	Relay closure (make-contacts)
See note at end of table.			

TABLE G (Contd)			
SIGNAL INPUT/OUTPUT AND POWER REQUIREMENTS FOR AMR105 DISCRETE TELEMETRY			
DESIGNATION	PIN NO. (NOTE)	DESCRIPTION	SIGNAL
POWER			
+5 V	045-047,145-147	DC voltage input	+5 V dc (400 mA min, 1000 mA max)
GRD	000,001,055,056 100,101,155,156	Common return for all signals and voltages	Ground
<i>Note:</i> Unless otherwise indicated, all pin numbers are associated with the circuit pack edge connector.			

AMR110 TERMINAL CONTROLLER

FUNCTIONAL DESCRIPTION

The terminal controller circuit pack provides a controller function based on the 8088 microprocessor. Features include buffered data, address and control buses, interrupt controller circuitry, programmable timer, 8K RAM data memory, EPROM program memory, address decoding, and sanity timer hardware.

This unit forms the central part of the multiboard TERM CONTR (terminal controller) for frequency diversity systems and both the TERM and REGEN CONTR (terminal and regenerator controllers) for hot standby systems.

BLOCK DIAGRAM DESCRIPTION

The block diagram in Fig. 53 complements the following description for the terminal controller.

Microprocessor

The 8-bit 8088 microprocessor forms the central core of the circuit pack. Its nonmaskable ENMT (interrupt) is edge board, available along with the EHOLD (hold signal). For on-board program memory applications, such as hot standby, the EHOLD lead must be tied low on the backplane. For off-board applications, it is designed to be operated through an associated memory board in frequency diversity.

Clock/Reset/Wait State Control

The 8284A clock generator and driver generates the processor clock from a 14.7456 MHz crystal. The 8284A unit, in association with a 4-bit divider, provides the following buffered edge-board clock signals for use by the terminal controller peripheral circuit packs:

DESIGNATION	FREQUENCY
EOSC	14.7456 MHz
ECLK (EOSC/3)	4.9152 MHz
EPCLK (ECLK/2)	2.4576 MHz
EBCLK (EPCLK/2)	1.2288 MHz
EB3CLK (EPCLK/8)	307.2 kHz
EB2CLK (EPCLK/16)	153.6 kHz

The 8284A unit generates a synchronized system reset signal through its Schmitt trigger input from the following three sources:

1. An RC network for power on reset
2. A front panel recessed pushbutton for manual reset
3. A backplane input (ERESIN) for automatic reset from the manual hardware sanity timer circuit.

A wait state generator will introduce one machine cycle of delay for use when accessing slow peripheral devices. The output of the wait state generator feeds the 8284 unit, which provides a synchronized ready signal for the microprocessor. Use of the wait cycle is controlled by the wait signal, available as an output from the programmable address decoder circuit. The backplane ERDY input signal is available for any additional off-board generated wait state.

System Primary Bus

The primary bus is a reserved section of I/O backplane pins that goes to all terminal controller peripheral circuit packs. It consists of the following:

- 4-bits (ELA0-ELA3) from the 20-bit (ELA0-ELA19) latched and buffered address bus.
- An 8-bit bidirectional data bus. Tri-state control of the bidirectional transceiver is by the ONBRD signal. The ONBRD signal level disables the transceiver whenever a device local to the circuit pack is accessed, i.e., RAM, interrupt control, or timer. When in use for off-board functions, the data bus direction is controlled by the microprocessor's data transmit/receive (DT/R) signal.
- 3-bits (ERD, EWR, and ERES) from the 10-bit buffered control bus.
- A peripheral clock (EPCLK—2.4576 MHz) bus.

Secondary Address/Control/Clock Bus

The remaining 16 bits (ELA4-ELA19) from the latched and buffered address bus and the remaining control and clock signals are available at the backplane for use by the peripheral circuit packs.

Interrupt Controller

An 8-bit programmable interrupt controller (8259) facilitates interrupt requests to the 8088 microprocessor. Two interrupt inputs are active high, five are active low, and one is connected directly to a programmable system clock timer for an internally-programmed timer interrupt.

Timers

Three 16-bit programmable timers make up an 8253 timer device that provides user timing capability. One of the timers is dedicated as a software system clock, via interrupt 5. The other two are available for general use by the application software.

Data Memory

There are 8K bytes of RAM (random access memory) available for use by the application software.

Program Memory

A socket is provided for an optionally equipped on-board programmable memory device of three type-sizes: 27128-16K bytes, 27256-32K bytes, and 27512-64K bytes. Two optioning terminal fields associated with this selection must be used to indicate which device-type is selected:

PROM	E9 (PIN 1)	E5 (PIN 27)
27128	E10	E4
27256	E10	E3
27512	E8	E3

If on-board microcode application is desired, the EHOLD signal must be strapped to ground.

Address Decoder

Address decoding for all of the microprocessor interfaced devices, both internally on the unit and externally on the peripheral circuit packs, is accomplished in the following hierarchical fashion.

- a. **High-Level 20-bit Decoding:** The overall 20-bit address space is partitioned by a 512 X 8 bipolar PROM (programmable read-only memory). Partitioning allows a minimum block size of 4K bytes and allows for flexibility using the basic circuit for other applications. The specific configuration for the terminal controller is as follows:

SIGNAL	DESCRIPTION	ADDRESS RANGE	SIZE
EPROM	Program memory select	F0000-FFFFF	64K
EPS0	Page 0 select-64K data memory (RAM) and all memory mapped IO	00000-0FFFF	64K
CSRAM	Data memory select	00000-01FFF	8K
WAIT	Memory mapped IO wait state select	0C000-0FFFF	16K
PMEN	Performance monitor dual port RAM select	0C000-0CFFF	4K
FLEN	Fault locate dual port RAM select	0D000-0DFFF	4K
TELMEN	AS&C telemetry dual port RAM select	E000-0EFFF	4K
EBS0	Memory mapped I/O address space	0FF00-0FFFF	256
EN3		Not assigned	

- b. **Memory Mapped I/O Decoding:** An 8-bit comparator (25LS2521) decodes the upper 256-byte block from the page 0 select. This memory block, defined by the EBS0 signal, defines the EBS0 block that is used for peripheral circuit selection. The EBS0 block is divided into two 128-byte blocks via address ELA7 into the following areas.

1. The lower 128-byte block, EBS00, is used in frequency diversity to decode the channel status circuit packs (PROT STATUS—protection, CHAN STATUS—regular). Addresses ELA6 through ELA3 are used to decode the individual status slots via fixed backplane coded wiring, allowing for a maximum of 16 channels. Address A2 decodes the halves of the dual regular channel status units, leaving addresses ELA1 through ELA0 for the individual port decoding.
2. The upper 128-byte block is divided by a 3-line to 8-line decoder (LS138) into eight 16-byte memory segments used for peripheral circuit pack select leads. Addresses ELA3 through ELA8 are then available for port decoding on a given peripheral unit.

One of the eight 16-byte memory segments defined above, ECSC0, is divided further. This circuit select space is divided into two 8-byte memory segments by ELA3 and a dual 2-line to 4-line decoder (LS139). The lower eight bytes, represented by signal CSC07, decode the on-board peripheral chips. The upper eight bytes, represented by ECSC8F, is available for off-board selection.

The 256-byte EBS0 space can also be accessed via I/O mapping. For this mode of operation the I/O port addresses are from 0 to 255.

Sanity Timer

A hardware sanity timer, consisting of two stages, is provided. It may be strapped to automatically reset the microprocessor should the application program break out of program flow. The first stage is a 5-second delay timer that must be retriggered by the application program by writing (any data value) to the sanity timer address within this 5-second interval. If the program fails to retrigger this device, the sanity timer's two outputs will become active. One

output, CPUF, available on the backplane, drives the LED faceplate indicator CONTR FAIL to on. The second output drives the second stage, configured as a 1 ms one shot.

The output from the second stage, ERESTART, available on the backplane, is normally connected to the ERESIN input to the reset circuitry. It automatically resets the microprocessor when becoming active. The output can be disabled by pulling the RSTINH signal low.

The faceplate CONTR FAIL indicator is driven by the logic ORing of the CPUF and CONTRF signals. Should it be desired that the CONTRF signal have no control over the illumination of this indicator, drive CONTRF to ground with a strap on the backplane.

PINOUT DESCRIPTION

Refer to Table H for signal input/output and power information.

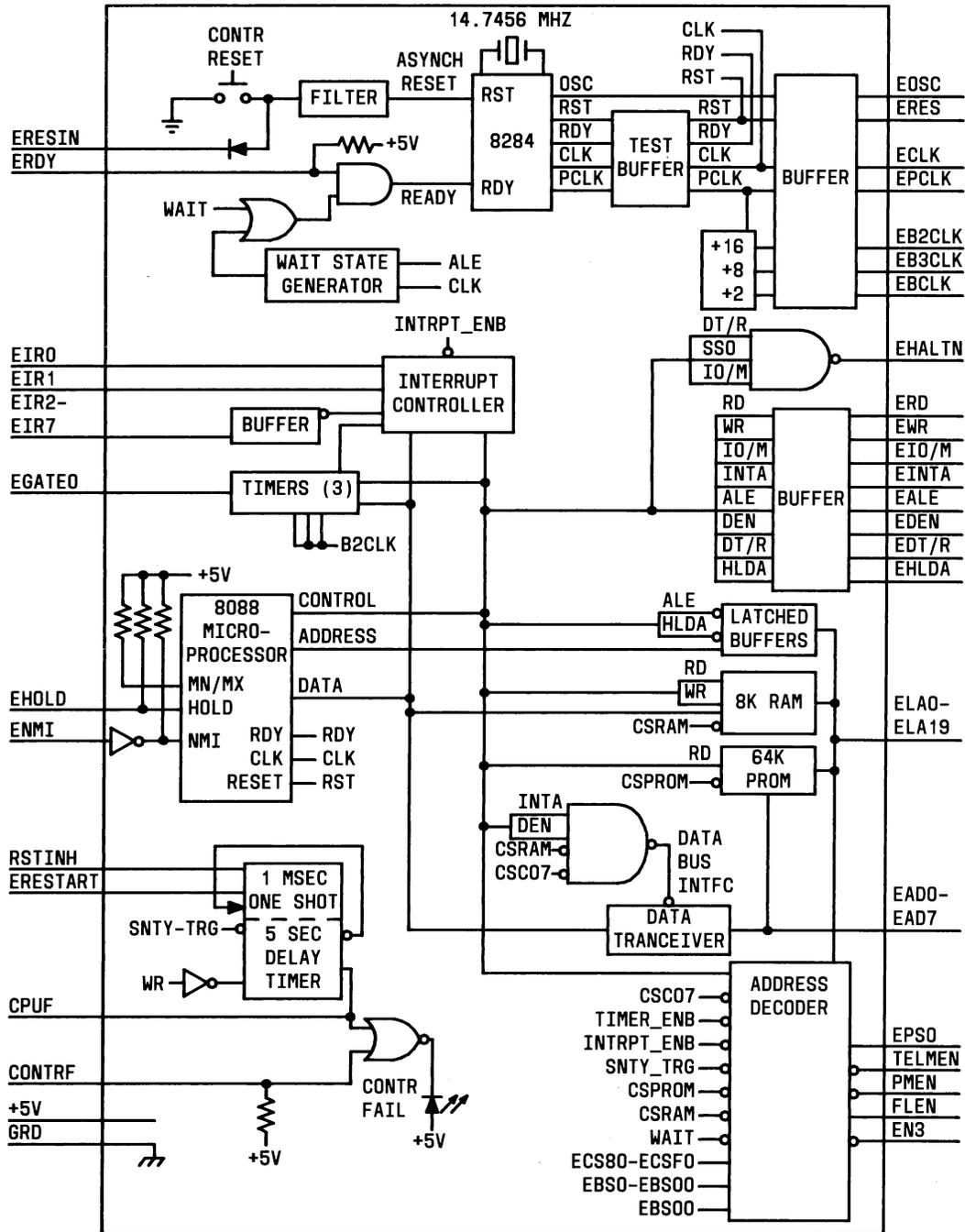


Fig. 53—AMR110 Terminal Controller Block Diagram

TABLE H			
SIGNAL INPUT/OUTPUT AND POWER REQUIREMENTS FOR THE AMR110 TERMINAL CONTROLLER			
DESIGNATION	PIN NO.(NOTE)	DESCRIPTION	SIGNAL
SIGNAL INPUT			
CONTRF	028	Controller fail	TTL (active-high)
EAD0-EAD7	002,102,003,103 004,104,005,105	External latched data bus (bidirectional)	TTL
EHOLD	024	CPU hold	TTL (active-high)
EIR0-EIR1	037,136	Interrupt signals	TTL (active-high)
EIR2-EIR7	134,036,135 133,033	Interrupt signals	TTL (active-low)
ENMT	054	Nonmaskable interrupt	TTL (active-low)
EPCLK	107	External peripheral clock	TTL (2.4576 MHz)
ERDY	124	CPU Ready	TTL (active-high)
ERESIN	151	Reset (CPU) In	TTL (active-low)
RSTINH	053	Reset inhibit	TTL (active-low)
SIGNAL OUTPUT			
CPUF	026	CPU fail	TTL (active-high)
ELA0-ELA19	008,108,009,109 010,110,011,111 012,112,013,113 014,114,015,115 016,116,017,117	External latched address bus	TTL
EALE	122	Address latch enable	TTL (active-high)
EB2CLK	125	Baud rate 2 clock	TTL (153.60 kHz)
EBCLK	020	Baud rate 1 clock	TTL (1.2288 MHz)
EBS0	128	Bank select 0 (IO address space)	TTL
EBS00	127	Bank select 0 (low half)	TTL
ECLK	120	Processor clock	TTL (4.9152 MHz)
ECS80	052	Circuit select 8	TTL
See note at end of table.			

TABLE H (Contd)			
SIGNAL INPUT/OUTPUT AND POWER REQUIREMENTS FOR THE AMR110 TERMINAL CONTROLLER			
DESIGNATION	PIN NO. (NOTE)	DESCRIPTION	SIGNAL
SIGNAL OUTPUT (Contd)			
ECS90	027	Circuit select 9	TTL
ECSA0	051	Circuit select A	TTL
ECSB0	150	Circuit select B	TTL
ECSC8F	152	Circuit select C (high half)	TTL
ECSD0	058	Circuit select D	TTL
ECSE0	149	Circuit select E	TTL
ECSF0	049	Circuit select F	TTL
EDEN	018	Data enable	TTL (active-low)
EDT/R	118	Data transmit/receive	TTL (Transmit = high, Receive = low)
EGATE0	129	Time 0 end-of-count indication	TTL (active-low)
EHALTN	137	Halt status	TTL (active-low)
EHLDA	023	Hold acknowledge	TTL (active-high)
EINTA	123	Interrupt acknowledge	TTL (active-low)
EIO/M	022	Input/output or memory select	TTL (I/O = high, Memory = low)
EN3	044	Enable 3 (spare)	Not used
EOSC	025	Oscillator	TTL (14.7456 MHz)
EPS0	138	Page select 0	TTL
ERD	006	External read control line	TTL (active-low)
ERES	007	External reset signal	TTL (active-low)
ERESTART	154	CPU restart	TTL (active low)
EWR	106	External write control line	TTL (active-low)
FLEN	139	Fault locate enable	TTL
See note at end of table.			

TABLE H (Contd)			
SIGNAL INPUT/OUTPUT AND POWER REQUIREMENTS FOR THE AMR110 TERMINAL STATION CONTROLLER			
DESIGNATION	PIN NO.(NOTE)	DESCRIPTION	SIGNAL
SIGNAL OUTPUT (Contd)			
PMEN	039	Performance monitor enable	TTL
TELMEN	038	AS C telemetry enable	TTL
POWER			
+5 V	045-047, 145-147	DC voltage input	+5 V dc (1000 mA max)
GRD	000,001 055,056, 100,101, 155,156	Common return for all signals and voltages	Ground
Note: Unless otherwise indicated, all pin numbers are associated with the circuit pack edge connector.			

AMR112 MASTER ALARM

The AMR112 MSTR ALARM (Fig. 54) interfaces the terminal station controller to the office alarm system. It also has manual controls that initiate system features. When one of the master control pushbuttons is operated with the associated OPR key of a status unit, the switch system features are initiated. Additional features include order-wire off-hook control interfacing, power and fan fail alarming, up to 16 user remote scan points, and up to 3 user remote controls.

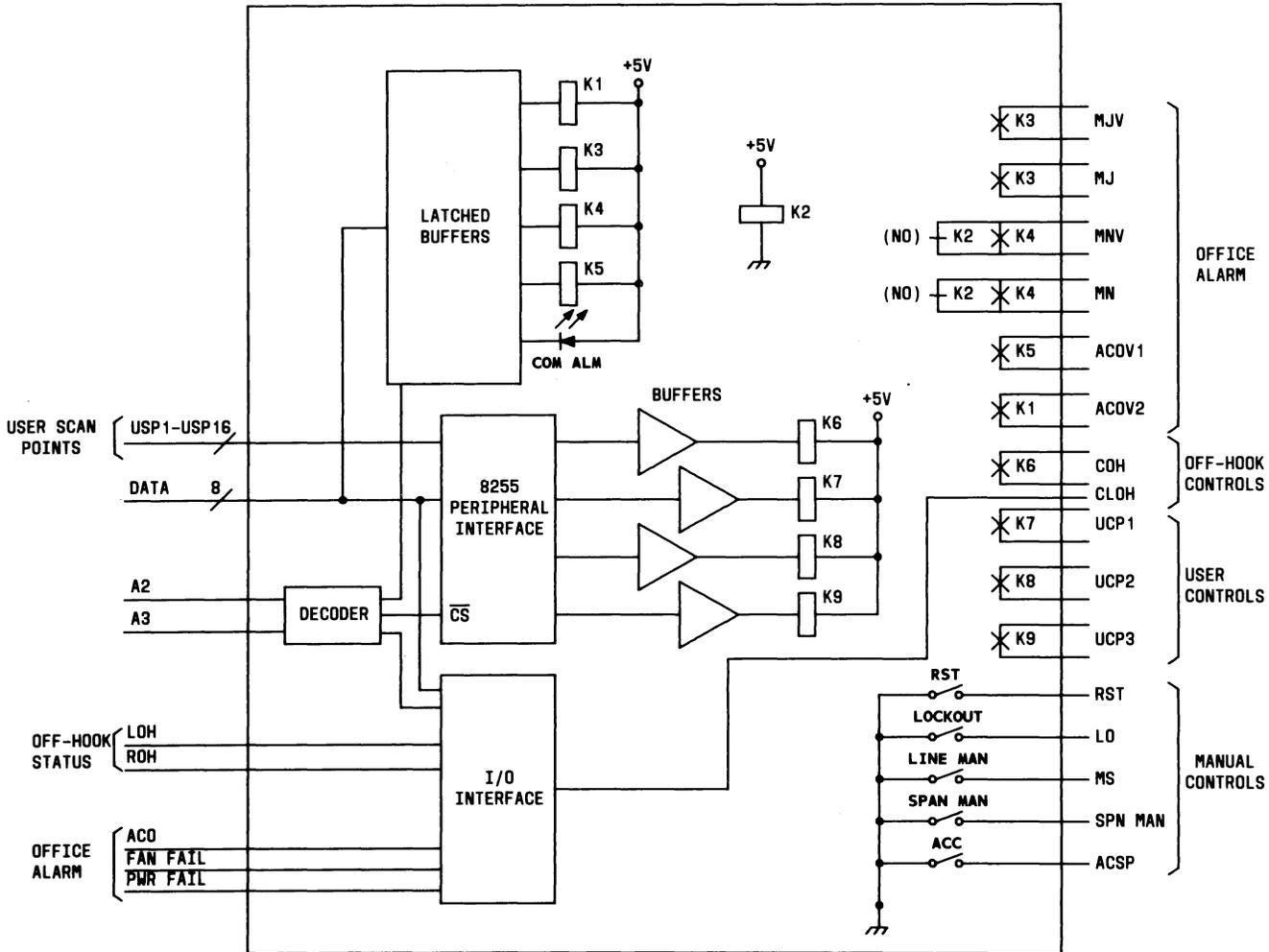


Fig. 54—AMR112 Master Alarm

AMR113 PROTECTION STATUS

The AMR113 PROT STAT (Fig. 55) provides parallel interfaces for microprocessor input/output to the protection channel for manual controls, status, and alarm indications. This unit also provides the control interface between the microprocessor and/or the line alignment circuitry.

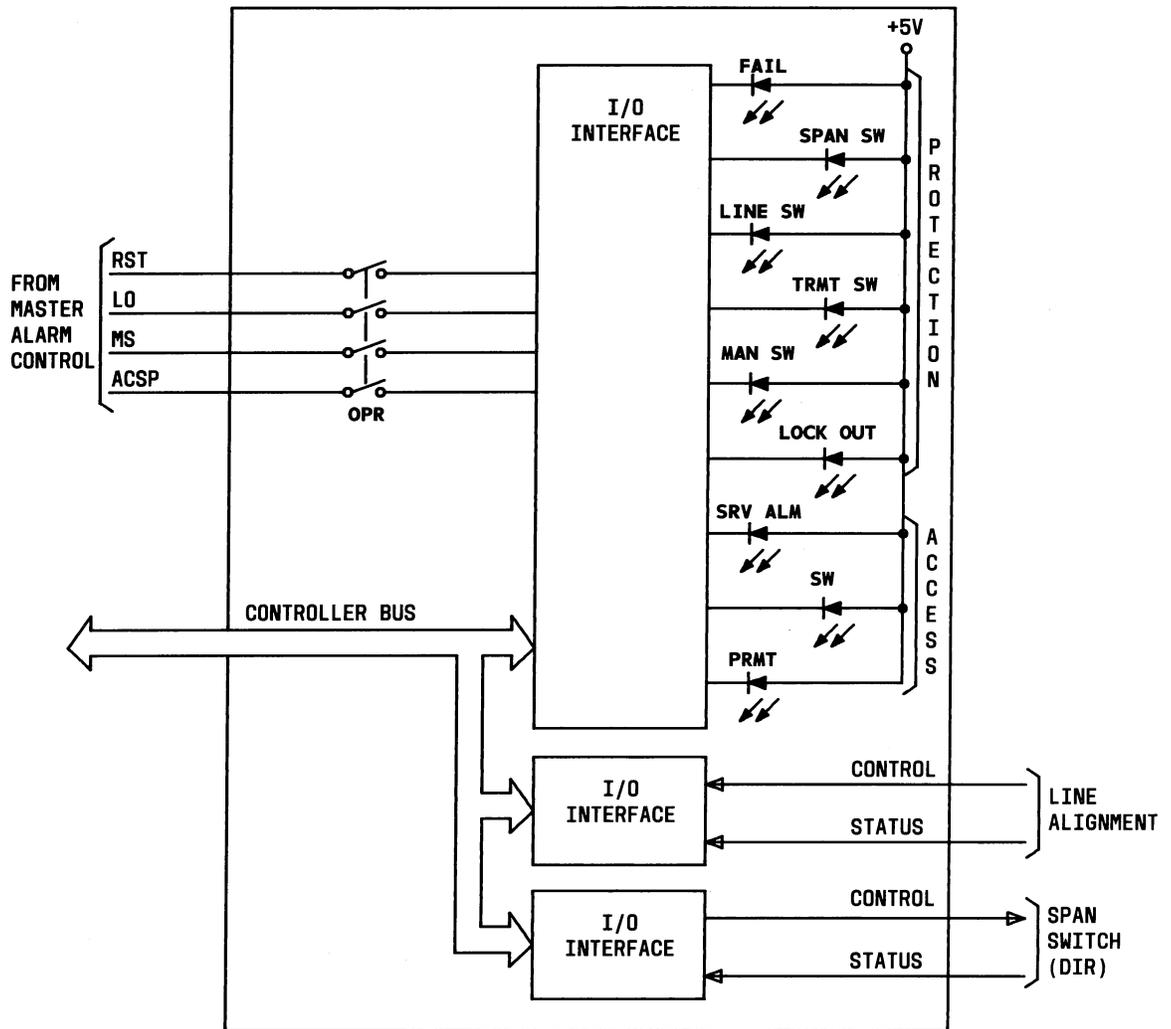


Fig. 55—AMR113 Protection Status

AMR114 CHANNEL STATUS

The AMR114 CHAN STAT (Fig. 56) provides a microprocessor input/output parallel interface to each of the regular channels. The circuitry for two channels is contained on one unit.

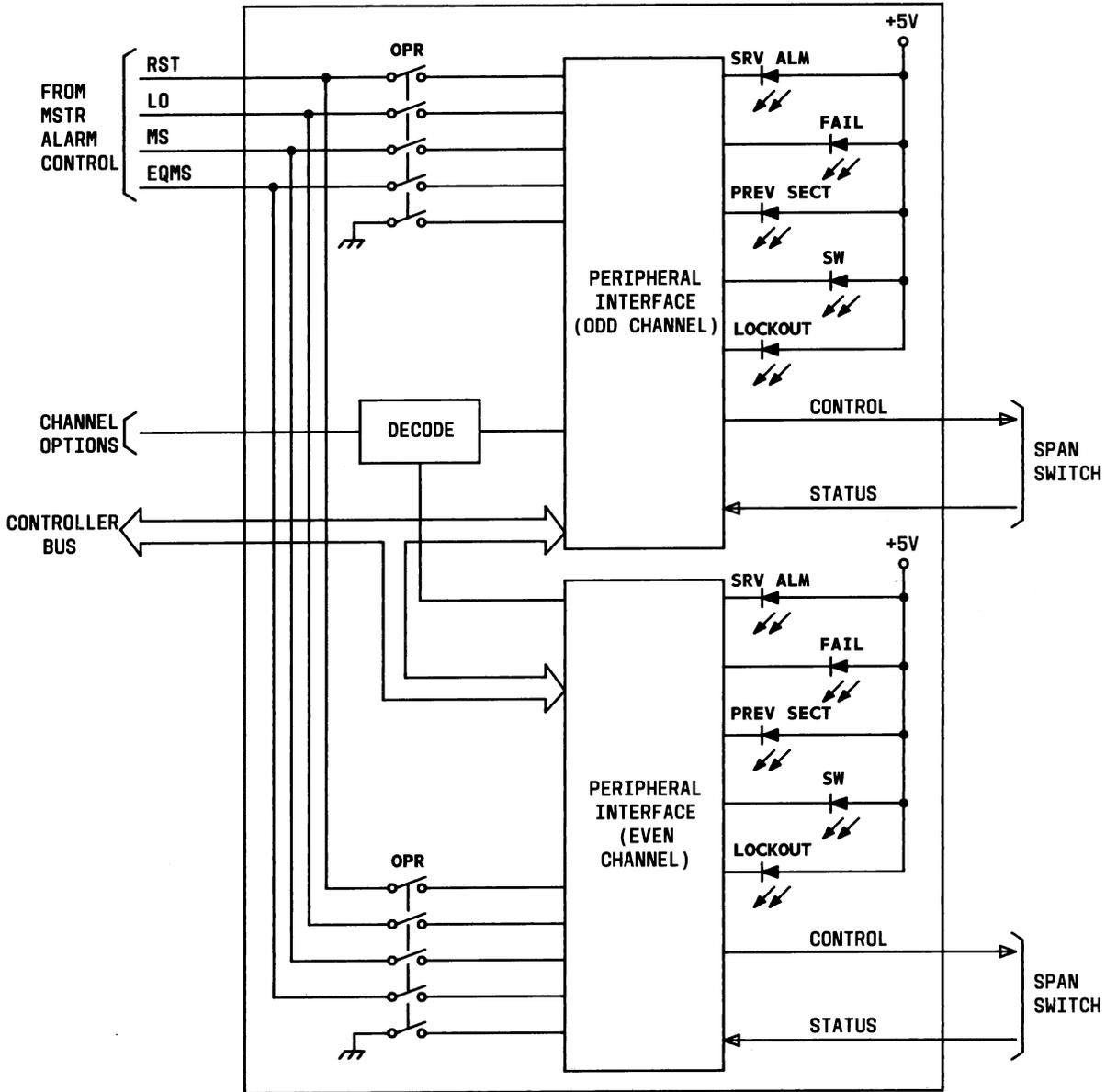


Fig. 56—AMR114 Channel Status

AMR115 RECEIVING STATUS

The AMR115 RCV STAT (Fig. 57) provides a microprocessor interface for manual test controls and a display for the diagnostic code. The AMR115 unit provides a UART (universal asynchronous receiver/transmitter) for the following serial connections: the terminal protection signaling data network, the hop protection signaling data network, and the TDN (terminal data network) that connects all channel controllers to the station controller. It also provides the service channel switch control interface.

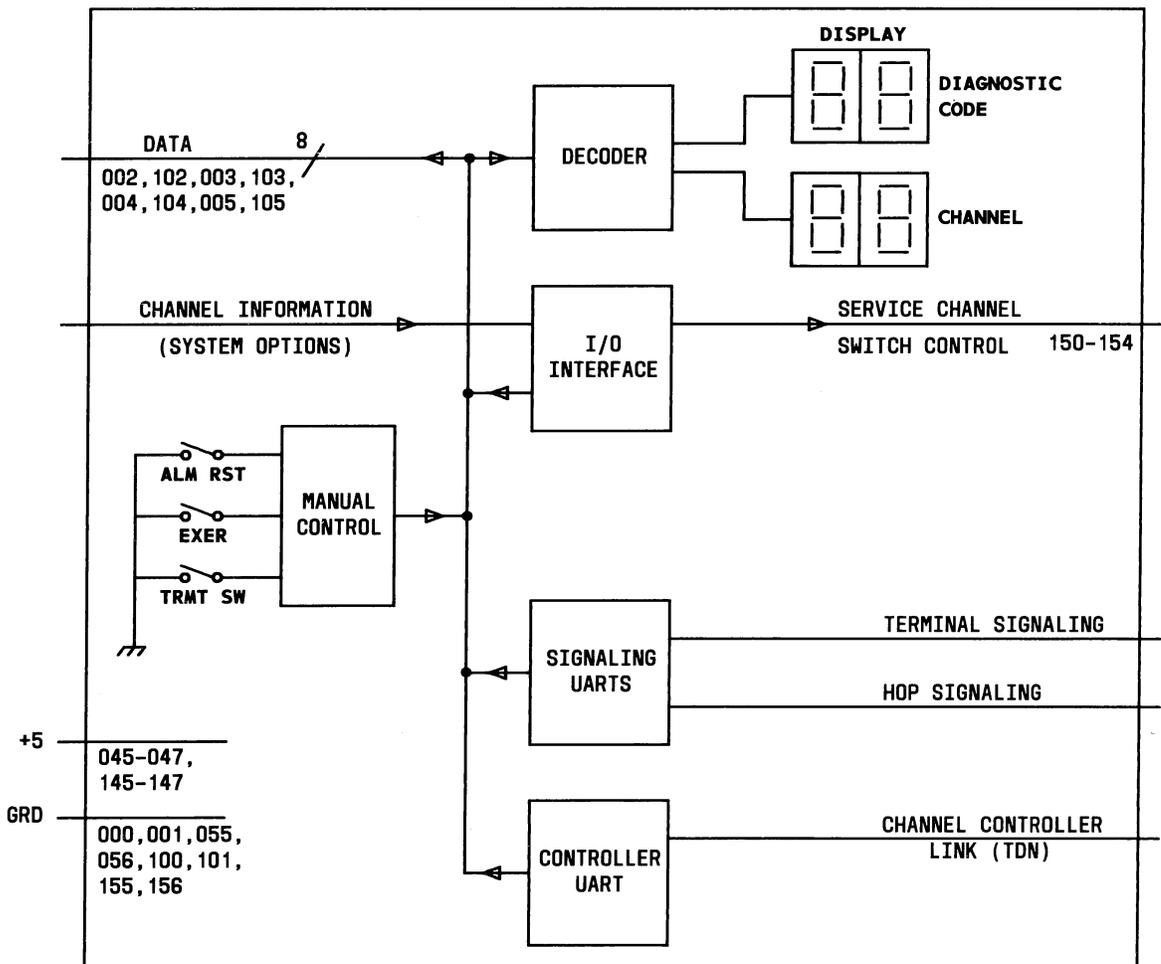


Fig. 57—AMR115 Receiving Status

AMR116 TRANSMITTING STATUS

The AMR116 TRMT STAT (Fig. 58) provides a microprocessor interface for common manual control inputs, transmitting status indicators, and transmitting switch control.

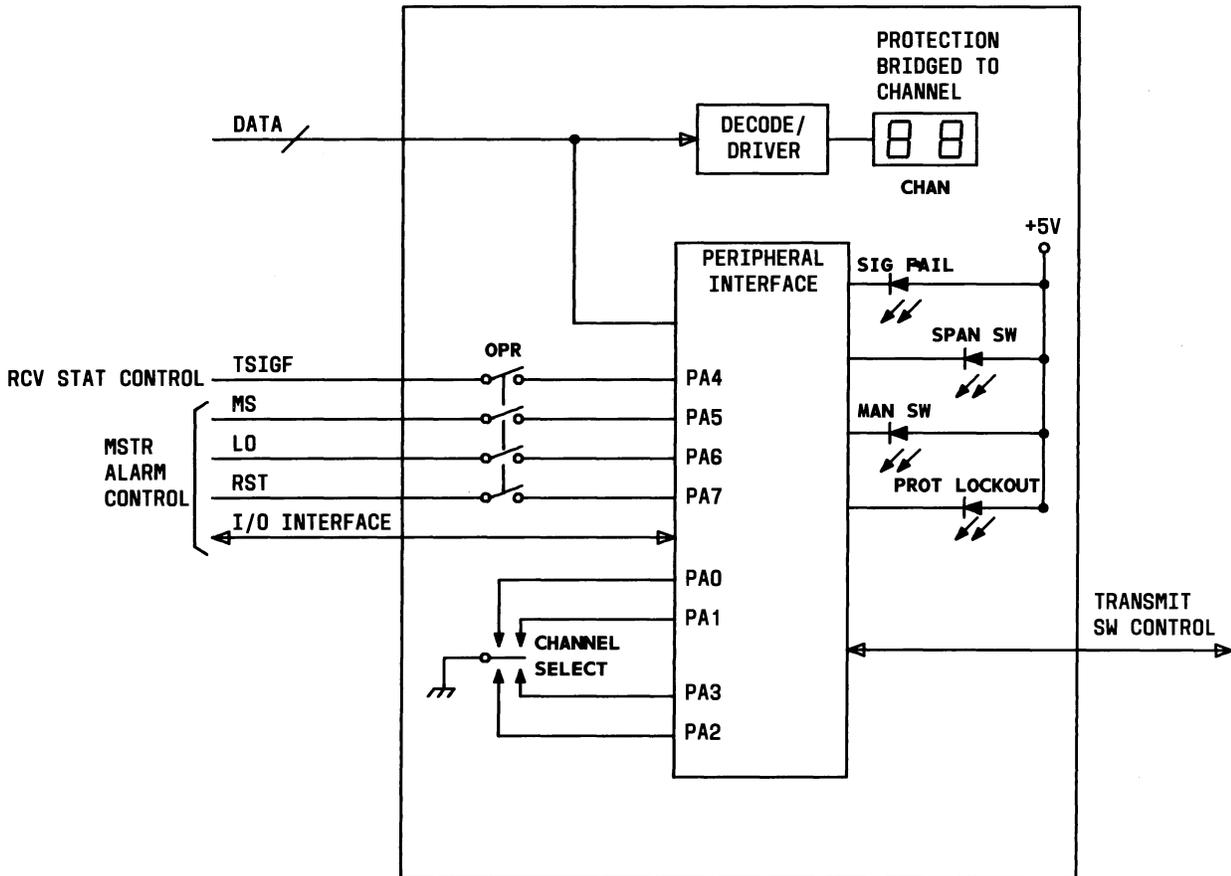


Fig. 58—AMR116 Transmitting Status

AMR127 REGENERATOR I/O**FUNCTIONAL DESCRIPTION**

The REGEN I/O (regenerator input/output) circuit pack is used in a regenerator control shelf to provide interfacing for the REGEN CONTR (regenerator controller) unit. The REGEN CONTR requires two REGEN I/O circuit packs. Input and output information is in the form of serial and parallel data buses.

BLOCK DIAGRAM DESCRIPTION

A block diagram of the REGEN I/O circuit pack is shown in Fig. 59. Table I shows signal input/output and dc power specifications.

The functions of the REGEN I/O are described in the following paragraphs.

External Bus Interface

The external bus interface uses an address, control, and data bus to control data transfers between the REGEN CONTR and REGEN I/O. The data bus (D0-D7) is eight bits wide and is bi-directional. The control bus consists of signals necessary to control data transfers on the data bus (WR and RD) and also a reset (RST) and a clock (CLK) signal. The reset signal is used to put all programmable chips on the REGEN I/O into a known starting state.

The address bus is composed of five chip select signals [EN()] and the two lowest address bits A0 and A1 of the address bus. Each chip select signal selects one of the five programmable devices on the data bus, and the address signals select ports and registers within the programmable devices.

Service Channel Interface

The REGEN I/O provides three serial ports (SR2, ST2, SR3, ST3, SR4 and ST4) for the SC (service channel) interface. Separate baud rate clocks (SRIC and STIC) supply the receive and transmit sections of the serial ports. The baud rate of the serial ports is typically 16 kB/s and the electrical interface is RS-422.

Interrupt capability is currently available on the receive side of serial port 2 and serial port 3. The <RXRDY> interrupt control signal from each device is wire OR'd and output on signal (INT). That is, if either or both serial ports receive a word, the (INT) interrupt lead will go to a logic high until the respective serial port(s) has been serviced.

Also included in the service channel interface is a dedicated DIC (Drop Insert Control) lead enable output for each serial port output. This control lead, when active-low, informs the service channel hardware to take its input from the control signal's respective transmitting port. This permits the 16-kb/s data stream to be multiplexed into the frame structure of the digital radio.

Service Channel Switch Control

Two additional control outputs (ASCRSW and ASCTSW) are defined as service channel switch control signals. Service channel switching requires two control signals because the switches are independent. Normally, a logic zero output is held on both control signals to keep the service channel switches in their normal positions. A logic one on the control signals instructs the service channel switches to be placed in their alternate states. Even though the receive and transmit service channel switches are independent, their switch positions normally track. It is only during very abnormal conditions that the requests on the receive and transmit service channel switch control signals do not agree.

Channel Status

Eight parallel inputs are reserved for channel status information from the protection channel and channel 1. Currently the only channel status signals used are the frame loss signals [()FLREQ], which are involved in the receive service channel switch control.

User or Discrete Telemetry Status and Control Interface

Sixteen parallel inputs and two relay closures are provided on each REGEN I/O. In a user application, the sixteen inputs are identified as user status points [USP()] and provide a customer interface into the serial scan point maps. Each input is pulled up to +5 volts with a 1k-ohm resistor and expects a relay closure to circuit ground to become active.

Two user control point [UCP()] relays are operated via the serial AS&C (TABS or TBOS) telemetry link. They provide general purpose local or remote control capability.

In a discrete telemetry application, the REGEN I/O provides a discrete telemetry interface via the user status and control leads described above. For this application the USPs provide a station control interface using external relay closures and the UCPs provide station alarm indications.

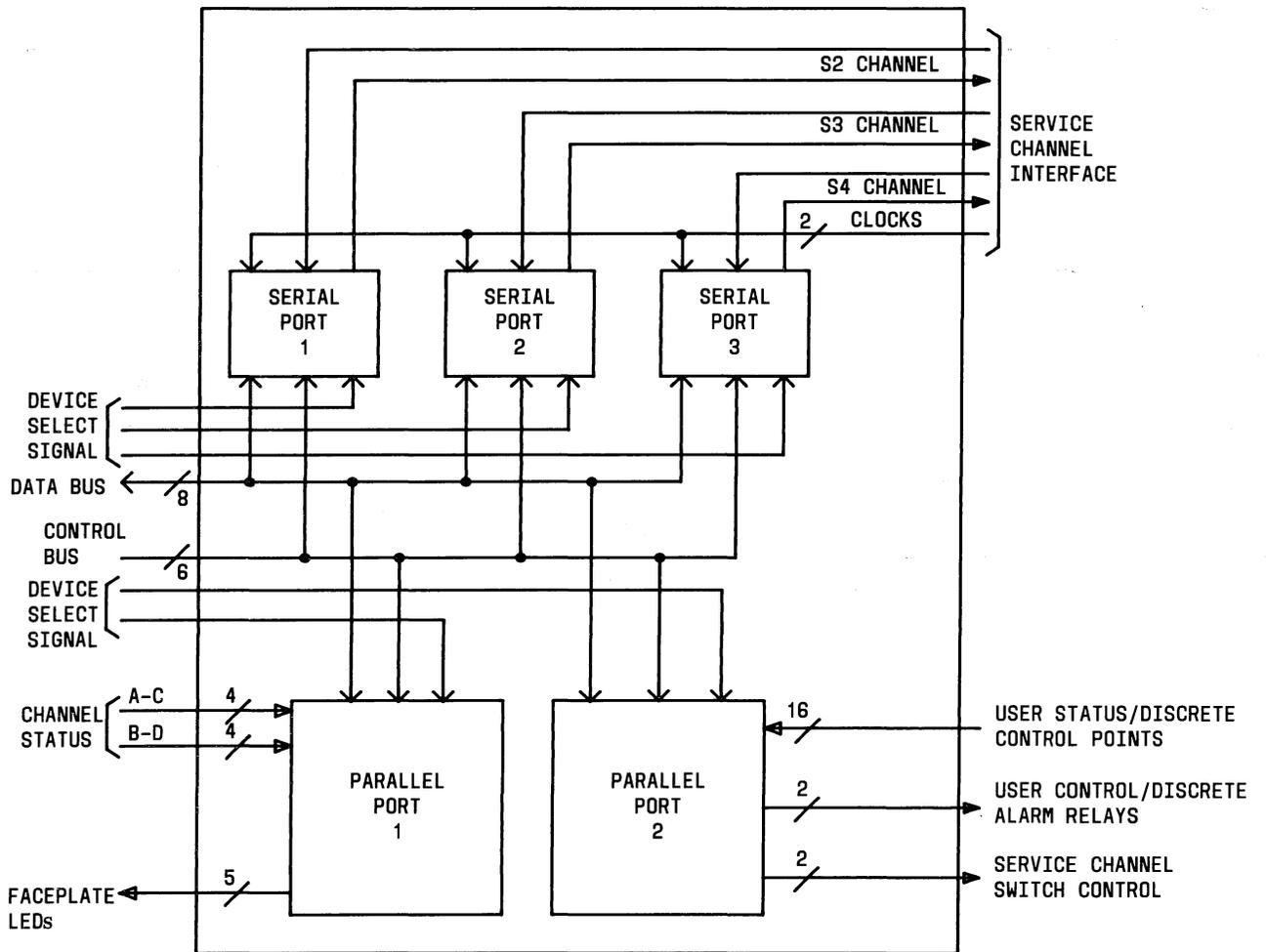


Fig. 59—AMR127 REGEN I/O Block Diagram

TABLE I					
SIGNAL INPUT/OUTPUT AND DC POWER SPECIFICATIONS FOR THE AMR127 REGEN I/O					
DESIGNATION	PIN NO. (NOTE)	DESCRIPTION	I/O	SIGNAL	
EXTERNAL BUS					
D0-D7	032-039	External data bus	I/O	TTL	
A0,A1	152,151	External latched address bus	I		
EN1-EN5	027-031	Device select signals	I	TTL (act-low)	
WR	153	External write control			
RD	150	External read control			
RST	154	External system reset		TTL (active-high)	
CLK	149	External clock		TTL (460.8 kHz)	
SERVICE CHANNEL INTERFACE					
SR2, $\overline{SR} 2$	011,111	S2 receive port	I	RS422	
SR3, $\overline{SR} 3$	115,114	S3 receive port			
SR4, $\overline{SR} 4$	109,009	S4 receive port			
SRIC, \overline{SRIC}	012,112	16 kHz receive clock			
STIC, \overline{STIC}	108,008	16 kHz transmit clock			
ST2, $\overline{ST} 2$	117,017	S2 transmit port	O		
ST3, $\overline{ST} 3$	120,020	S3 transmit port			
ST4, $\overline{ST} 4$	016,116	S4 transmit port			
S2DIC	014	Drop insert control			TTL (active-low)
S3DIC	113				
S4DIC	013				
ASCRSW	122	Receive switch control	I	TTL	
ASCTSW	018	Transmit switch control			
INT	007	S3/S4 receive port interrupt		TTL (active-high)	
CHANNEL STATUS					
AIFLREQ	051	Protection frame loss	I	TTL (active-low)	
AIMFRREQ	053	Protection manual frame resupply		TTL (not used)	
AIBERREQ	054	Prot. bit error			
AIMGREQ	050	Prot. modulator fail			
CIFLREQ	048	Regular frame loss		TTL (active-low)	
CIFRREQ	049	Regular manual frame resupply		TTL (not used)	
CIBERREQ	052	Reg. bit error rate			
CIMGREQ	148	Reg. modulator fail			
See note at end of table.					

TABLE I (Contd)				
SIGNAL INPUT/OUTPUT AND DC POWER SPECIFICATIONS FOR THE AMR127 REGEN I/O				
DESIGNATION	PIN NO. (NOTE)	DESCRIPTION	I/O	SIGNAL
USER OR DISCRETE TELEMETRY INTERFACE				
UCP1,UCP1R	107,103	User control or discrete alarm	O	Relay closure (25 VA or 1 amp)
UCP2,UCP2R	005,104			
USP1-16	125,026,126,124, 023,025,127,123, 133,024,022,132, 131,130,129,128	User scan or discrete control	I	TTL (active-low)
POWER				
+5V IN	045,145,046, 146,047,147	DC voltage supply	I	+5 VDC (850 mA)
GRD	000,100,001,101, 055,155,056,156, 118,134,135,138, 139	Ground	—	—
<i>Note</i> Unless otherwise indicated, all pin numbers are associated with the circuit pack backplane connector J1.				

AMR243 64-QAM DECISION

FUNCTIONAL DESCRIPTION

The AMR243 64QAM DECSN circuit pack is used in the terminal and regenerator digital receiver shelves to regenerate the original three data signals from the baseband input. Two 64QAM DECSN units are required in a digital receiver, one for the I (in-phase) and one for the Q (quadrature) baseband signals.

BLOCK DIAGRAM DESCRIPTION

The 64QAM DECSN (Fig. 60) first amplifies the received input BB (baseband) signal and then passes it on to a 6-bit A/D converter to derive digital signal information. Secondary functions necessary for proper A/D conversion are clock recovery, to sample the signal at the proper time, and threshold circuits, to establish the proper references.

Clock recovery is accomplished by using a PLL (phase-lock loop). This circuit derives a clock of the proper frequency and phase and maintains the sample time at the center of the receiver eye. The threshold circuits also use a decision directed algorithm to derive the top, center, and bottom references that are necessary to perform the A/D process.

Signal information and the associated clock are output to the CRLTR unit for carrier recovery, phase detection, and automatic transversal equalizer control. Samples of input baseband signal (EYE), recovered clock (CLK), and pseudo errors (PSEUDO ERRORS) can be monitored from faceplate mounted jacks.

The 64QAM DECSN unit monitors the clock recovery for loss of lock. If a timing lock-loss occurs, an amber faceplate LED (TIMING LOCK LOSS) is lighted and an alarm signal (IDLL) is sent to the associated CHAN CONTR unit.

PINOUT DESCRIPTION

Refer to Table J for signal input/output and power information.

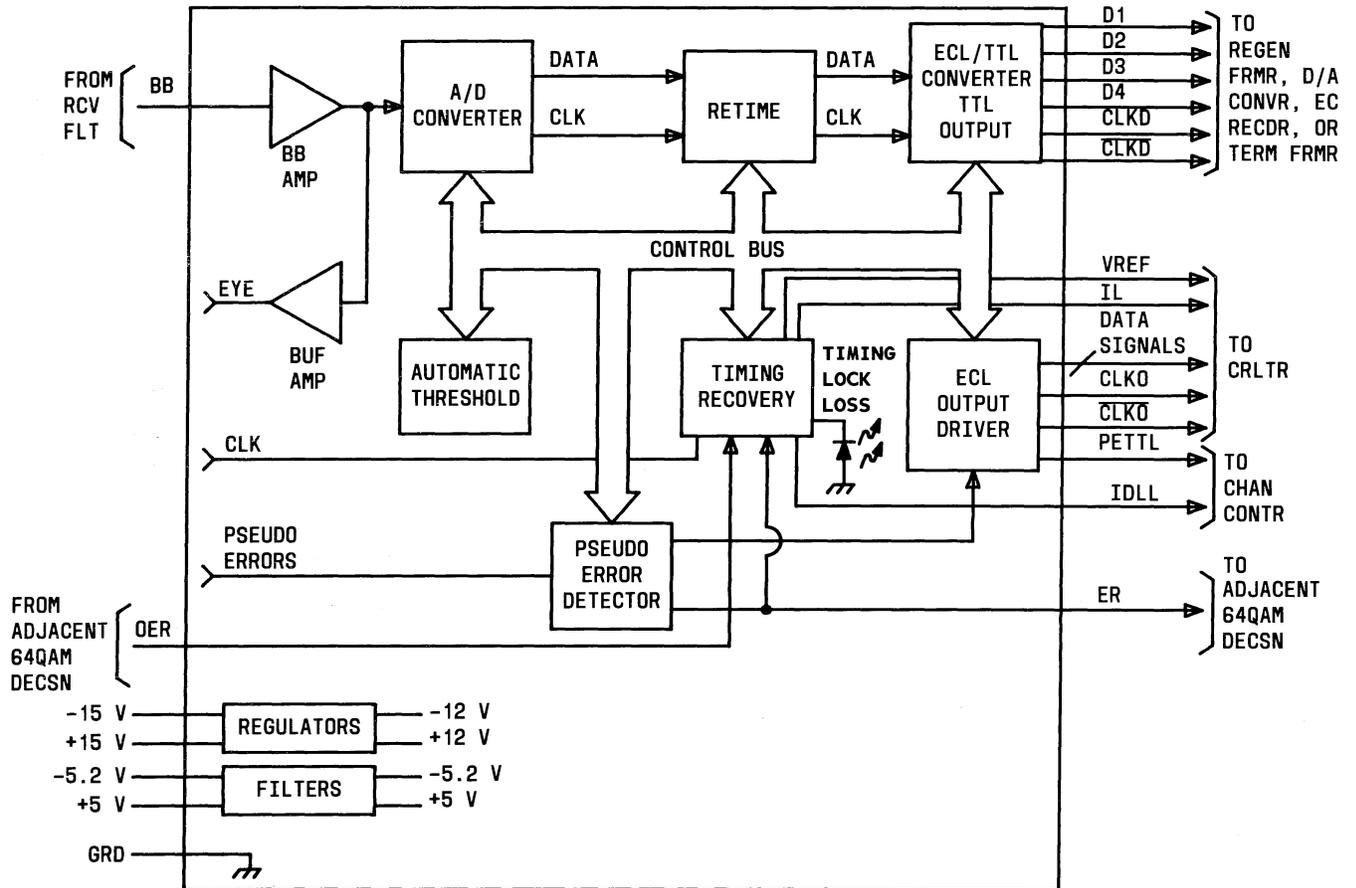


Fig. 60—AMR243 64-QAM Decision Block Diagram

TABLE J			
SIGNAL INPUT/OUTPUT AND POWER REQUIREMENTS FOR AMR243 64-QAM DECISION			
DESIGNATION	PIN NO. (NOTE)	DESCRIPTION	SIGNAL
SIGNAL OUTPUT			
D1	133	Data bit 1	22.767 Mbaud, TTL
D2	132	Data bit 2	22.767 Mbaud, TTL
D3	131	Data bit 3	22.767 Mbaud, TTL
D4	111	Error bit	22.767 Mbaud, TTL
CLKD	136	Recovered clock (high)	22.767 MHz, ECL
$\overline{\text{CLKD}}$	135	Recovered clock (low)	22.767 MHz, ECL
IL	106	Loss of lock indicator	TTL (logic 1 = in lock)
VREF	113	Internal status	TTL (active low)
Data signals	022,122,023,123, 025,125,026,126	Data signals for CRLTR	22.767 Mbaud, ECL
CLKO	036	Recovered clock (high)	22.767 MHz, ECL
$\overline{\text{CLKO}}$	035	Recovered clock (low)	22.767 MHz, ECL
PETTL	109	Pseudo error divided by 16	TTL (in lock = no transitions)
IDLL	107	Lock loss indication	TTL (high = in lock)
ER	013	Error rate indication	TTL (high = low error rate)
EYE	J3 (faceplate)	Baseband input monitor	22.767 Mbaud, -9 dBm, 75-ohms
CLK	J2 (faceplate)	Recovered clock monitor	22.767 MHz, ECL
PSEUDO ERRORS	J4 (faceplate)	Pseudo error monitor	TTL (logic 0 = pseudo error)
SIGNAL INPUT			
BB	050	8-level baseband input	8-level linear, -13 dBm, 75-ohms
OER	102	Error rate	TTL (low = low error rate)
See note at end of table.			

TABLE J (Contd)			
SIGNAL INPUT/OUTPUT AND POWER REQUIREMENTS FOR AMR243 64-QAM DECISION			
DESIGNATION	PIN NO. (NOTE)	DESCRIPTION	SIGNAL
POWER			
-15 V	021,121	DC voltage input	-15 V dc, 40 mA
+15 V	019,119	DC voltage input	+15 V dc, 6 mA
+5 V	045-047,145-147	DC voltage input	+5 V dc, 230 mA
-5.2 V	040-043,140-143	DC voltage input	-5.2 V dc, 710 mA
GRD	000,001,027-030, 034,037,039,049, 051,055,056,100, 101,108,127-130, 134,137,139,149, 150,151,155,156	Common return for all signals and voltages	Ground
Note: Unless otherwise indicated, all pin numbers are associated with the circuit pack backplane connector.			

ANB1 SERVICE CHANNEL MULDEM

The ANB1 SC MULDM (Fig. 61) receives the 384-kb/s signal from the DPU and demultiplexes it into six 64-kb/s subchannels. It also multiplexes the six subchannels to a 384-kb/s signal going to the DPU. The six subchannels are applied as follows:

- S - Used for internal communications between terminal stations and among all stations of a switch section. Because all protection switch information is contained within this subchannel, no external facilities are required for system operation.

The S subchannel is further subdivided as follows:

- S1 - Protection switch signaling
- S2 - Hop switch signaling (service channel)
- S3 - Scan point signaling
- S4 - Fault location data.

- OW - Used for an order wire to telemetry extensions or RS422 extensions between various terminal and regenerator stations when bays are prewired.
- W,X,Y - Used, if equipped, to provide voice frequency trunks, E2A DAS telemetry extensions, or RS422 extensions between various terminal and regenerator stations.
- Z - Used, if equipped, to provide a voice-frequency trunk or an E2A DAS telemetry extension between various terminal and regenerator stations.

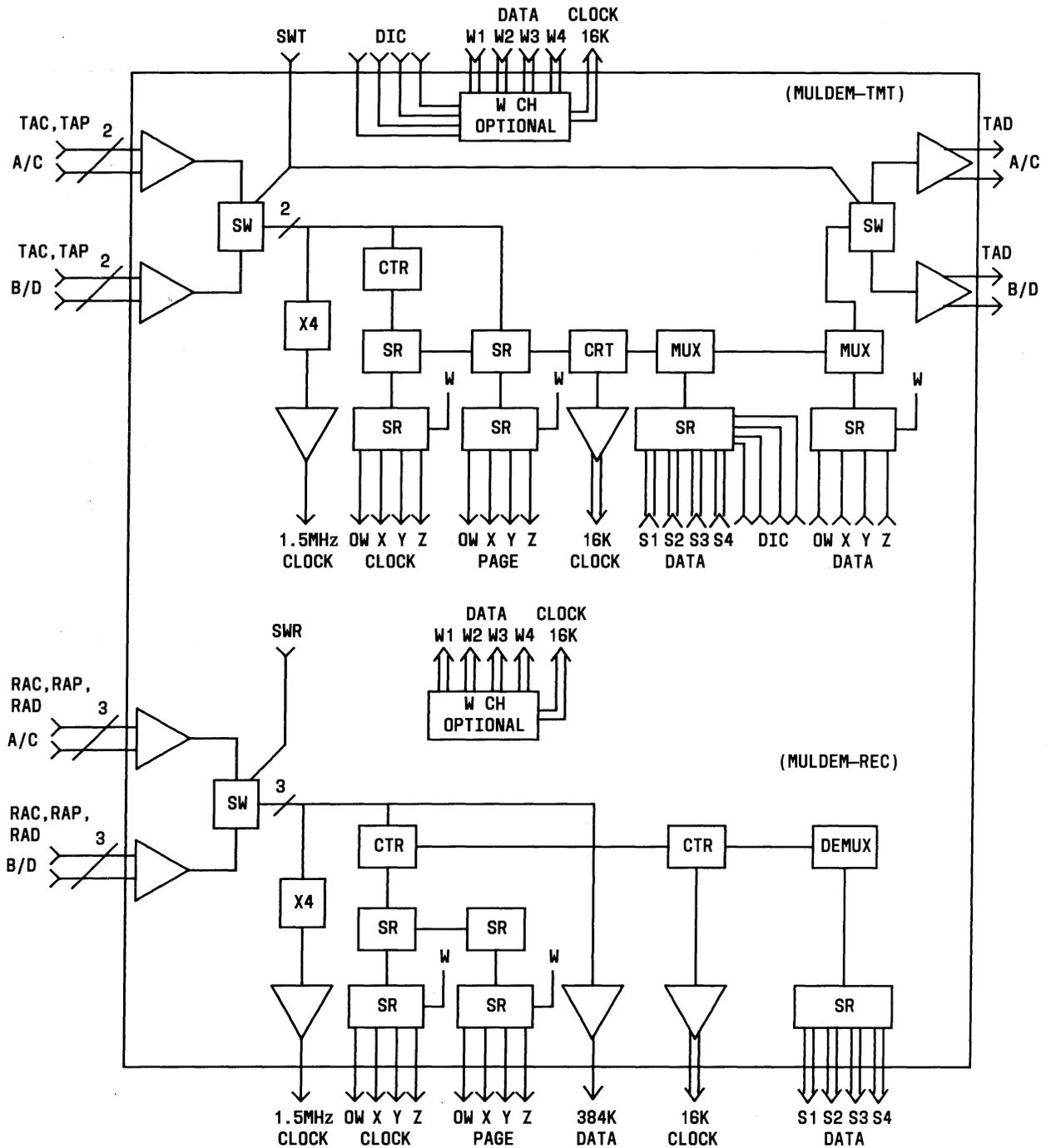


Fig. 61—ANB1 Service Channel Muldem

ED-8C657-30 ORDER-WIRE STAR EXTENSION

FUNCTIONAL DESCRIPTION

The ED-8C657-30 order-wire star extension provides an interface for connecting three or four radio system order-wire circuits together. This interface allows voice transmission and off-hook logic to be passed between the connected systems. The unit consists of two components, ED-8C657-30-G1 and ED-8C657-30-G2, that are mounted either in the terminal bay installer interface panel, if space permits, or miscellaneously.

BLOCK DIAGRAM DESCRIPTION

A block diagram of the order-wire star extension is shown in Fig. 62. Table K shows signal input/output and dc power specifications. For system wiring information, refer to the SD-7C525-01 drawing.

Order-wire circuits from each radio system are connected to terminal strip TS1 on the front of the ED-8C657-30-G1 component. These circuits are connected to the PWB (printed wiring board) on the ED-8C657-30-G2 component by a ribbon cable. Each order-wire circuit consists of a VF (voice frequency) input VFIN(), VF output VFOUT(), control off-hook COH(), and receive off-hook ROH() signal where () represents the associated radio system A, B, C, or D. The signal return leads are identified as VFIN()R, VFOUT()R, COH()R, and ROH()R.

The VF interface provides a bridge that allows one order wire to communicate with each of the other connected order wires. Each connected order wire must provide a +7 dBm output to the VF interface. This compensates for a -23 dB loss realized in the circuit and thereby provides the proper input power level of -16 dBm to the receiving order wires.

The off-hook logic interface receives the off-hook signal ROH() from an order wire and passes that signal as COH() to each of the other system order wires. This function is provided by a PAL (programmable array logic) circuit.

When only three order wires are connected, the VF connections for the unused port VFIND and VFOUTD must be terminated by connecting these pins to the VFINDT and VFOUTDT pins, respectively.

Operating power is connected to the unit at PWB terminals E1 (BAT) and E2 (RTN). A power module allows a -21 to -60 V dc battery supply to be used, typically -24 or -48 V dc. This voltage supply is filtered, converted to +5 V dc, and regulated for proper circuit operation. A 0.5 ampere fuse provides circuit protection.

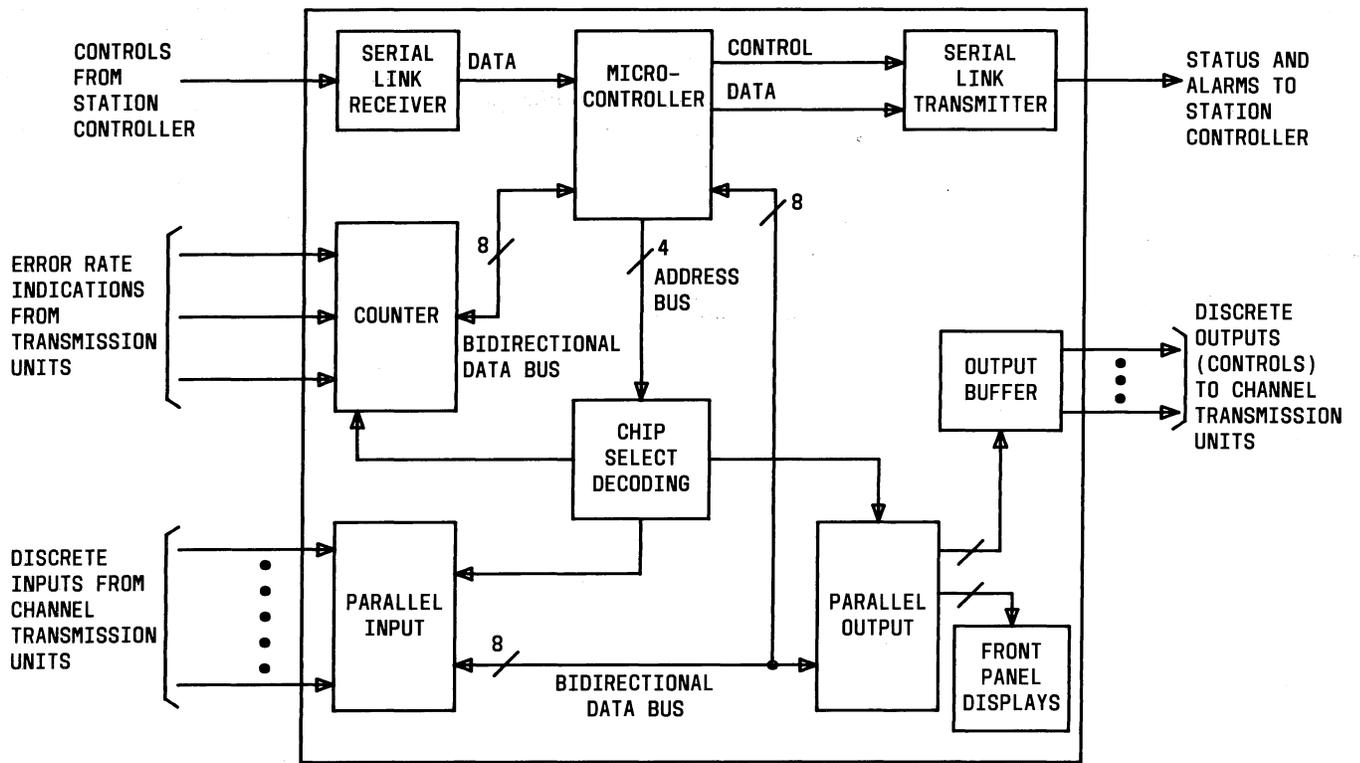


Fig. 62—ED-8C657-30 Order-Wire Star Extension Block Diagram

TABLE K				
SIGNAL INPUT/OUTPUT AND DC POWER SPECIFICATIONS FOR THE ED-8C657-30 ORDER WIRE STAR EXTENSION				
DESIGNATION	PIN NO. (NOTE)	DESCRIPTION	I/O	SIGNAL
OFF-HOOK LOGIC SIGNALS				
COHA, COHAR	32, 14	Control off-hook signaling and return	O	TTL (active-low)
COHB, COHBR	31, 13			
COHC, COHCR	30, 12			
COHD, COHDR	29, 11			
ROHA, ROHAR	36, 18	Receive off-hook signaling and return	I	TTL (active-low)
ROHB, ROHBR	35, 17			
ROHC, ROHCR	34, 16			
ROHD, ROHDR	33, 15			
VOICE FREQUENCY (VF) SIGNALS				
VFINA, VFINAR	28, 10	VF input signal and return	I	VF +7 dBm
VFINB, VFINBR	27, 9			
VFINC, VFINCR	26, 8			
VFIND, VFINDR	25, 7			
VFINDT	24	VF input 600-ohm termination		—
VFOUTA, VFOUTAR	20, 2	VF output signal and return	O	VF -16 dBm
VFOUTB, VFOUTBR	21, 3			
VFOUTC, VFOUTC	22, 4			
VFOUTD, VFOUTDR	23, 5			
VFOUTDT	5	VF output 600-ohm termination		—
POWER				
BAT	E1	DC battery voltage supply	I	-24 or -48 V dc
RTN	E2	Voltage supply return	—	—
Note				
Pin numbers other than E numbers are part of PWB connector J1 which connects to TS1 on ED-8C657-30-G2 via ribbon cable.				

MC450() CHANNEL CONTROLLER

FUNCTIONAL DESCRIPTION

The CHAN CONTR (channel controller) is the interface between the station controller and the regular or protection channel transmission units. Communications between the station controller and the CHAN CONTR is done by a high-speed RS422 serial link. The monitoring functions of the CHAN CONTR are performed on a *per hop* basis while the switch request information is processed on a *section* basis. Software is controlled by an on-board microprocessor based program. This program is divided into four parts:

1. **Switch Requests:** The CHAN CONTR calculates the bit error rate for the radio channel. If the count exceeds a number that corresponds to the switch threshold, a switch request is sent to the station controller. A switch request will also be sent if frame loss or equipment failure occurs.
2. **Performance Monitoring:** The CHAN CONTR monitors radio channel performance. This performance monitoring consists of out-of-frame, error rate, and equipment failure. This information is sent to the station controller for further processing.
3. **Alarms:** All radio channel scan point information is consolidated and, upon request, is sent to the station controller.
4. **Displays:** The CHAN CONTR displays performance monitoring information and local equipment status (alarms) on the faceplate. Performance information includes excessive bit-error rate, excessive misframe rate, and excessive activity indicated by individual LEDs. Frame loss and hop error rate are displayed on a bar graph. The bar graph is graduated into eight sections that light from bottom to top as the error rate increases. When a frame loss occurs, the bar graph lights fully and flashes. Local equipment status includes transmit and receive channel failure indications for both radio and digital equipment.

BLOCK DIAGRAM DESCRIPTION

The block diagram in Fig. 63 complements the following description for the channel controller.

With the exception of the serial link receiver and transmitter, all inputs and outputs are connected to the microcontroller through an 8-bit data bus. This is done by bus oriented I/O expanders and counters. Each I/O device is selected by a chip decoding circuit from a 4-bit address. The I/O information is put onto the data bus and read into the microcontroller. The microcontroller processes the information and passes the data to the station controller via the serial port.

Parallel Inputs

Alarms: The alarm inputs come from receiving and transmitting units of the bay. The first group of inputs (AIRNIFA-D) detects unit failures from the receive network. The second group of inputs (AITNIFA-D) detects unit failures from the transmit network. The third group (AIRNSFA-D) comes from the desync and frame monitor. And the last group comes from the digital processing, modulator, decision, demodulator, and frame generator units.

Status: The status inputs come from all parts of the system. The status inputs from the radio bay indicate the failure of the TWT amplifier, transmit and receive radios, and/or dc to dc power converters. The status inputs from the terminal/regenerator bay indicate if the network frame insert has been activated, if the switch verification is active (frequency diversity only), or in the case of the regenerator, the status of the frame resupply.

Parallel Outputs

Control: The control outputs from the CHAN CONTR operate the alignment enable output, the switch operate output, the frame resupply output, the false clock output (CICK), and the network frame insert outputs (CINNFR-A-D).

Display: The outputs for the display functions are generated on board the CHAN CONTR. The fail inputs are processed and the appropriate LED on the faceplate is lit. The parity bits from the input are counted and are then displayed on the faceplate bar graph.

Serial Ports

The serial ports on the CHAN CONTR communicate with the station controller using a RS422 formatted signal at a 19.2 kBaud.

Counters

The counters count the number of parity errors that are detected by the decision and framer boards or the number of CRC errors detected by the decision boards. This information is used to calculate switch requests and display information for the bar graph.

Option And Equipped Leads

When strapped, the option leads indicate to the channel controller that message telephone service, error correction, and/or pseudo parity is provided. The equipped leads indicate channel number (frequency diversity only), direction, and tributary equipped information.

PINOUT DESCRIPTION

Refer to Table L for signal input/output and power information.

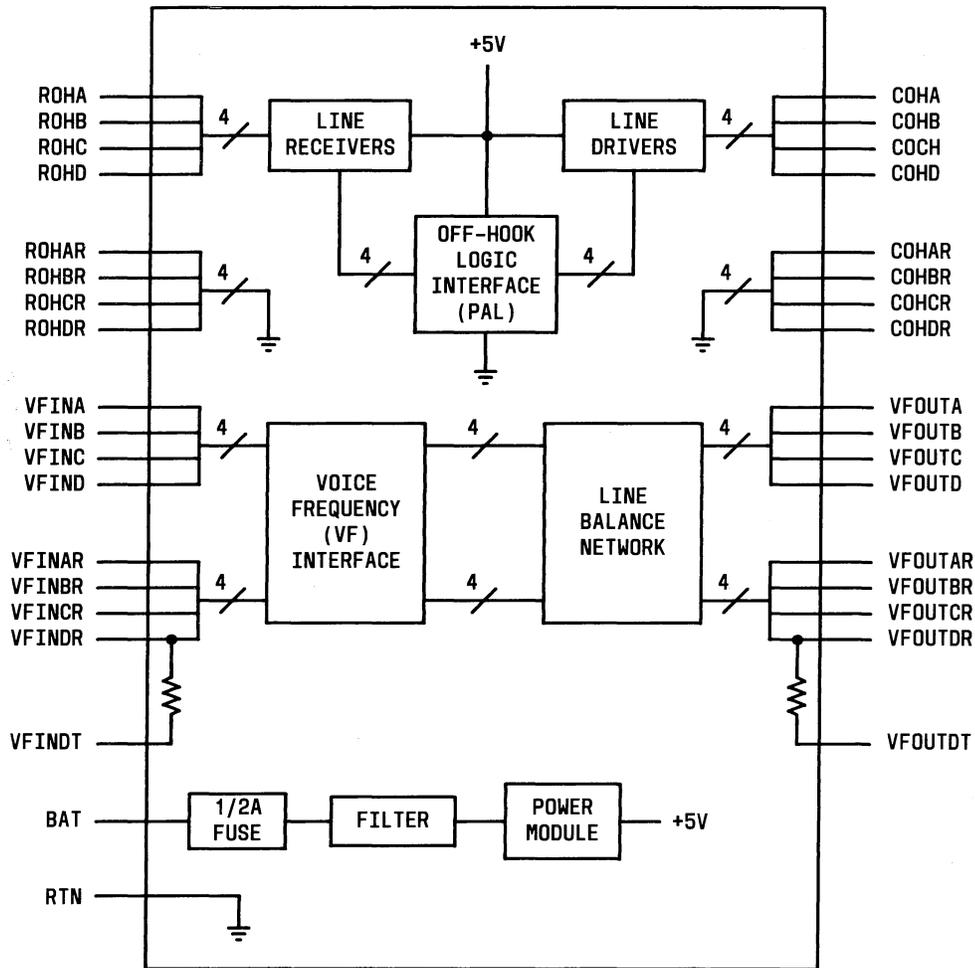


Fig. 63—MC450() Channel Controller Block Diagram

TABLE I				
SIGNAL INPUT/OUTPUT AND POWER REQUIREMENTS FOR MC450() CHANNEL CONTROLLER				
DESIGNATION		PIN NO. NOTE	DESCRIPTION	SIGNAL
TERMINAL	REGENERATOR			
SIGNAL INPUT				
AICLL	AICLL	022	Carrier lock loss	Normal = +12 V dc
AD1-AD4*	—	111-114	Channel address (option straps)	Equipped = 0
AIDLL	AIDLL	102	Decision lock loss	TTL (active-low)
AIFGCL	AIFGCL	122	Frame generator lock loss	TTL (active-high)
AIFIFL	AIFIFL	104	Frame-in-frame loss	TTL (active-low)
AIFL	AIFL	002	Frame loss	
AIMOL	AIMOL	003	Modulator output loss	+12 V dc
AIRNIFA-D	—	133,135, 137,139	Receive network interface fail leads	TTL (active-low)
AITNIFA-D	—	029,030, 129,130	Transmit network interface fail leads	
AIRNSFA-D	—	033,035, 037,039	Receive network interface desync and frame monitor status	
EC	EC	110	Error correction (option strap)	Equipped = 0
MTS	MTS	108	Message telephone (option strap)	DDS = 1
PAST	PAST	109	Signal parity (option strap)	CRC = 0, pseudoarity = 1
—	AC/BD	107	Channel direction (option strap)	AC = 0
PDN	PDN()	050	Serial link	RS422 (19.2 kBaud)
PDNB	PDN()B	150	Serial link inverse	
See note and footnote at end of table.				

TABLE I (Contd)				
SIGNAL INPUT/OUTPUT AND POWER REQUIREMENTS FOR MC450() CHANNEL CONTROLLER				
DESIGNATION		PIN NO. NOTE	DESCRIPTION	SIGNAL
TERMINAL	REGENERATOR			
SIGNAL INPUT (Contd)				
SIDEMI	SIDEMI	106	Decision eye monitor	TTL
SIDEMQ	SIDEMQ	103	Without framers pseudo-parity counter	
SIHP	SIHP	105	Hop parity counter	TTL (active-low)
SILSV*	—	028	Switch verification status	
SINFRIND	—	027	—	
SINFRINC	—	020	Network frame insert status (terminal), manual frame resupply/frame	
SINFRINB	SIMFRS	115	resupply (regenerator)	
SINFRINA	SIFRS	015		
SITP	—	004	Transmission parity counter	
SIXPA	SIXPA	128	Power alarm	Contact closures
SIXTWT	SIXTWT	120	TWT alarm	
SIXRTF	SIXRTF	024	Radio fail	
SIXPRF	SIXPRF	025	RCV Radio Fail	
SIXPREF	SIXPREF	026	Radio preamp fail	
SIXPAR	SIXPAR	127	Signal return leads	Return
SIXTWTR	SIXTWTR	124		
SIXRTFT	SIXRTFR			
SIXRRFR	SIXRRFR	125		
SIXPREFR	SIXPREFR	126		
TEQB-D	—	017,118,018	Equipped tributary info (option straps)	Equipped = 0
TTTA-D	—	132,134,136,138	Tributary equipment info (option straps)	
See note and footnote at end of table.				

TABLE I (Contd)				
SIGNAL INPUT/OUTPUT AND POWER REQUIREMENTS FOR MC450() CHANNEL CONTROLLER				
DESIGNATION		PIN NO. NOTE	DESCRIPTION	SIGNAL
TERMINAL	REGENERATOR			
SIGNAL OUTPUT				
AILBER	AILBER	031	Low bit error rate	TTL (active-low)
OUT1*	—			
AIHBER	AIHBER	148	High bit error rate	
USRB*	AI()FLEQ**			
AILCLR	—	044	RTX switch request	TTL (active-high)
CLSW*			Line switch request	
AILCLT	AILCLT	144	Transmit switch request	
CALNEN*	—		Alignment Enable	
—	CFRSI	116	Frame resupply indication	
CICK	CICK	049	False clock	
CINNFRA-D	—	032,034, 036,038	Blue signal control	
—	CRFSR	016	Frame resupply control	
RDN	RDN	053	Serial link	RS422 (19.2 kBaud)
RDNB	RDNB	153	Serial link inverse	
POWER				
+5 V	+5 V	045-047,145- 147	DC voltage input	+5 V dc (750 mA)
GRD	GRD	000,100,001,101, 055,155,056,156, 124-127	Common return for all signals and voltages	Ground
<p>Note: Unless otherwise indicated, all pin numbers are associated with the circuit pack edge connector.</p> <p>*Frequency Diversity systems only.</p>				

MC450() MEMORY

The MC450() MEM (Fig. 64) contains four EPROMs (erasable programmable read-only memory) that contain the application firmware and four RAMs (random access memory) used by the terminal controller. Address decoding is controlled by a 1k x 8 programmable bipolar PROM (programmable read-only memory). Auxiliary functions provided are full buffering at the data, address, and control buses.

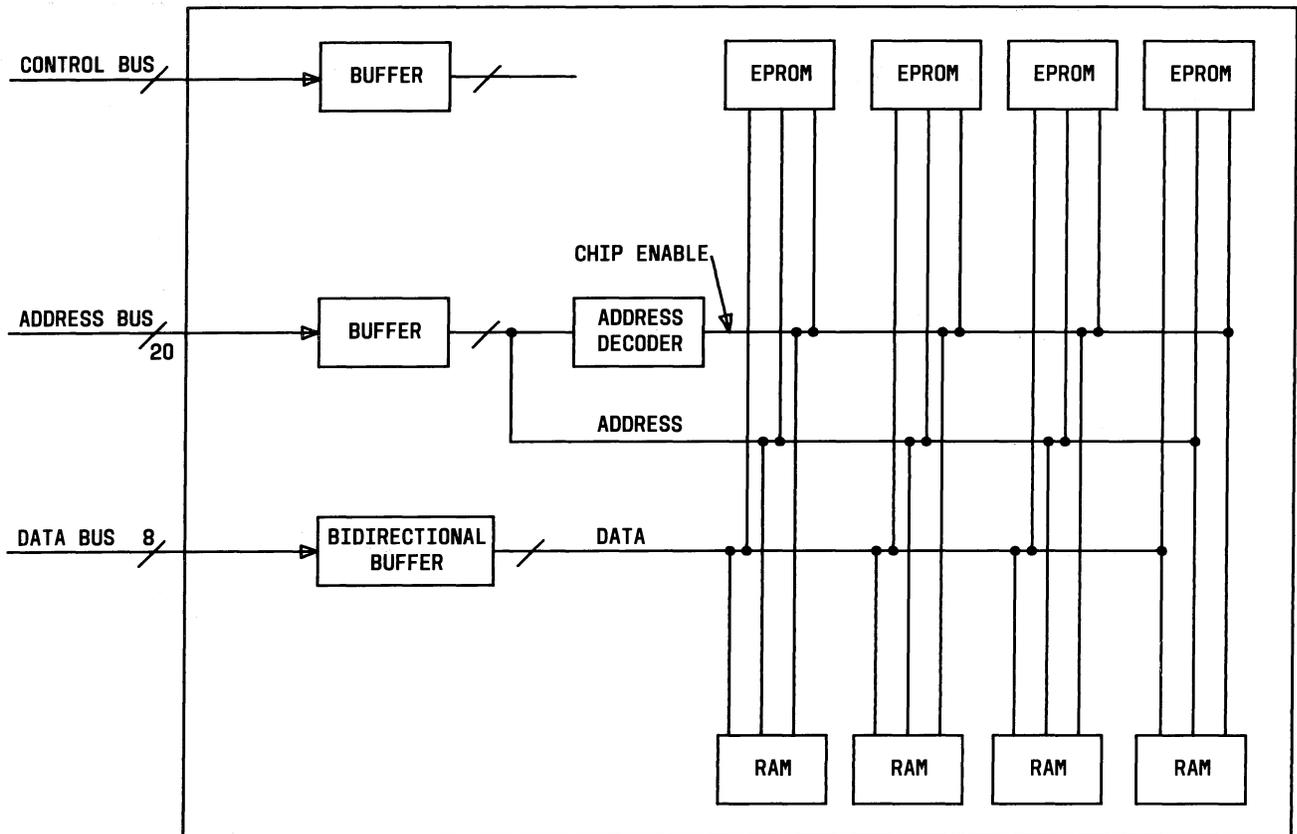


Fig. 64—MC450() Memory

MC450() REGENERATOR CONTROLLER

The regenerator controller (Fig. 65) consists of an 8-digit microcontroller, a program and data semiconductor memory, parallel input and output ports, and serial ports. A regenerator controller requires two AMR127 regenerator I/O circuit packs.

Functionally, the regenerator controller can be broken down into the following areas: CPU (central processing unit), semiconductor memory, buses, address decoding, parallel ports, and serial ports.

An 8-bit microcontroller is used as the CPU for the entire regenerator controller design. The microcontroller controls its internal components, all the peripheral devices located on the unit, and all the peripheral devices on both AMR127 circuit packs by executing an application program stored in the unit's program memory device. The microcontroller's responsibility is to control and process such activities as office alarms, serial telemetry, service channel switching, and manual control interfaces.

The regenerator controller is equipped with 8,192 bytes of ROM (program memory) and 384 bytes of RAM (data memory). The ROM memory is nonvolatile and is, therefore, used to permanently store the application program for the regenerator controller. The entire 8k of program memory is provided by a single memory chip and communicates with the CPU via the internal data bus. Data memory is used as a place to temporarily store data. Examples of this data could be temporary counters or timers required by the application program or a large buffer area holding the station alarms for the serial telemetry process. Data memory also communicates with the CPU via the internal data bus.

Two levels of buses exist in the design: internal to the board and external to the board. Internal buses consist of an 8-bit data bus, a 16-bit address bus, and a control bus. All peripheral devices communicate with the CPU via the bidirectional data bus. The address bus is used in selecting the appropriate port or memory location requested by the CPU. The control bus is used to direct the data flow on the data bus. The external buses provided by the unit operate identically to the internal buses but are electrically buffered from them. The external buses are provided to communicate with peripheral devices on both AMR127 controller I/O units.

The address decoding function is an internal process that is involved in determining which peripheral device the CPU is requested to communicate with on any bus operation. The address decoding for program memory is controlled directly by the microcontroller unit. However, data memory, parallel ports, and serial ports must be individually selected for each bus transaction. The address decoding circuit provides a separate device select line to each peripheral device connected to the data bus. Currently, three device select signals are used internally to the unit, ten are used for the AMR127s, and three are spares.

The parallel ports in the regenerator controller are dedicated to initialization leads, faceplate lights, and office alarm control. The initialization leads are used to configure the application program to meet the needs of a particular regenerator station. This includes such information as the number of equipped channels, the station address, radio alarm reporting, and service channel status. Three faceplate lights are provided on the unit: COM ALM, CONTR FAIL, and CONTR SIG ALARM. The office alarm lines are used to control three relays that are identified as major, minor, and aco.

The regenerator controller has two serial ports. One is a 19.2k baud, RS422 data link that interfaces with all channel controller units equipped at the station. The regenerator controller gathers all per-channel data over this link. The other serial link is a 2400 baud, RS422 data link that provides a serial telemetry interface using the TBOS protocol.

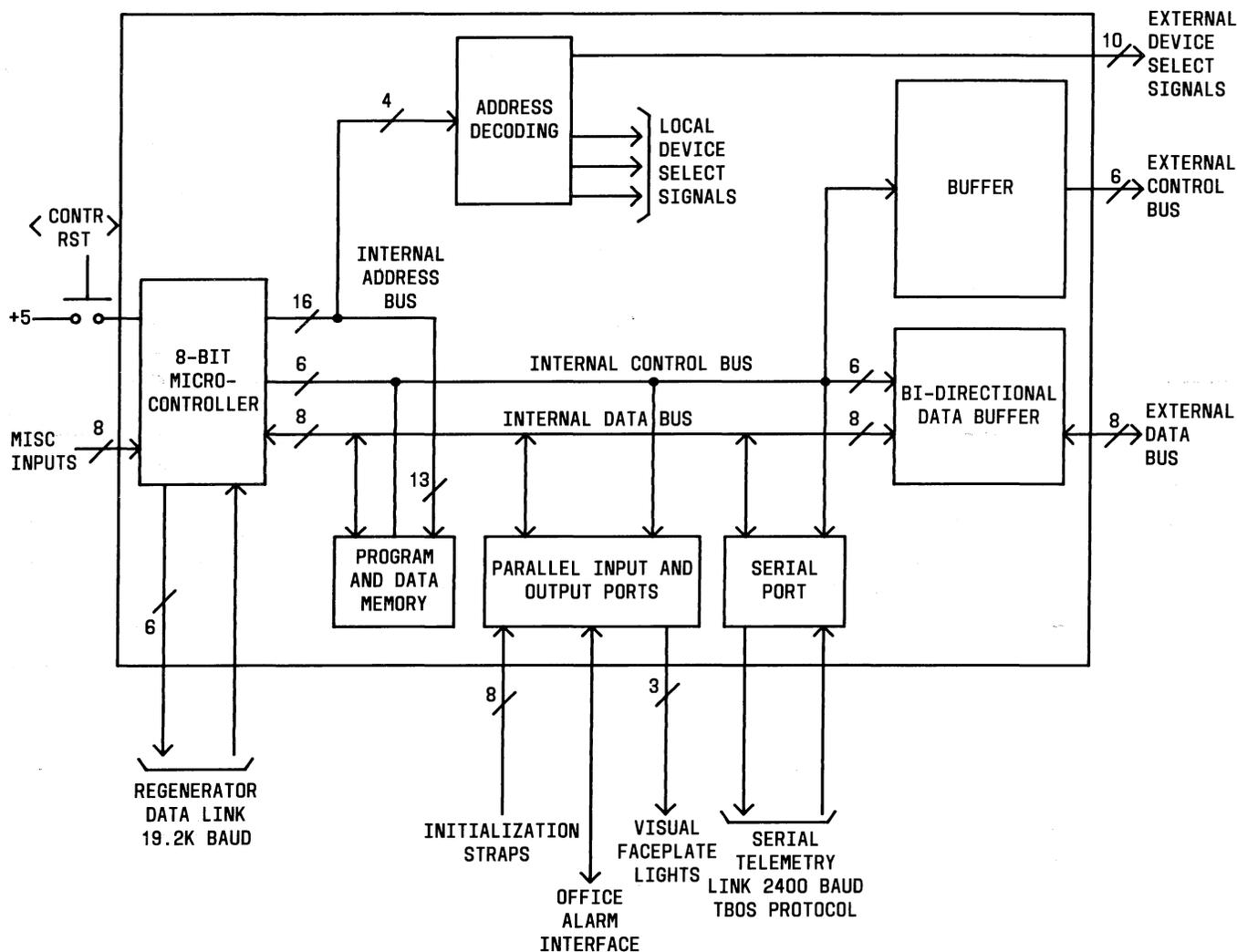


Fig. 65—MC450() Regenerator Controller

MC45021A1 SERIAL TELEMETRY (TBOS)

The MC45021A1 SER TELEM unit (Fig. 66) is a slave processor that provides an AS&C (alarm surveillance and control) serial telemetry interface between the terminal bay and the E2A (or equivalent) monitoring device using TBOS protocol. All communications with the external monitor are over an RS422 standard serial link at 2400 b/s. A dual port RAM (random access memory) provides bidirectional communication with the terminal station controller through a common bus. The unit also has a loopback on the serial link to perform a self-test.

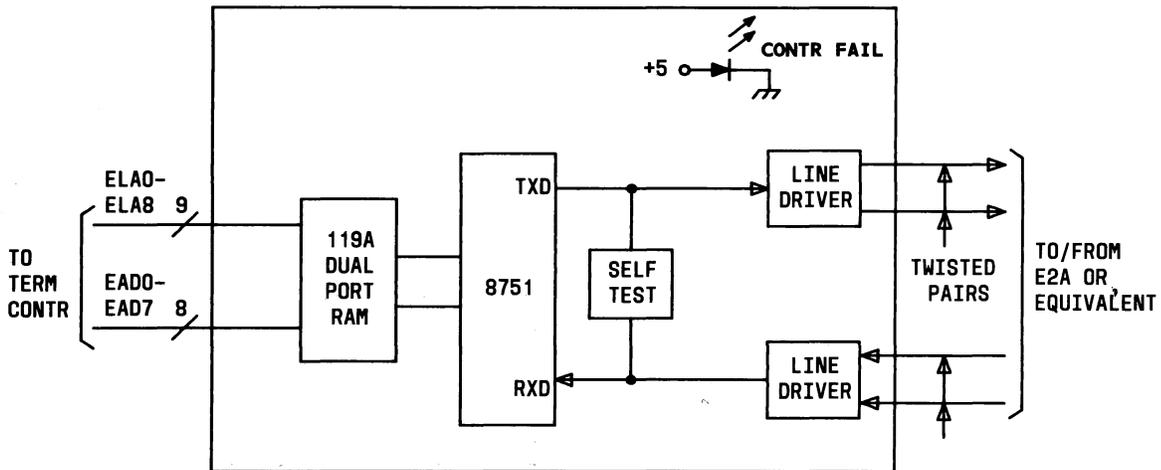


Fig. 66—MC45021A1 Serial Telemetry (TBOS)

MC45022A1 FMAS TELEMETRY

The MC45022A1 FMAS TELEM unit (Fig. 67) provides FMAS capability at the terminal bay and communications to regenerator bays for implementing remote FMAS capability. The unit can provide up to three interfaces to the GTP (general telemetry processor) using TABS protocol. These interfaces are AS&C, PM (performance monitoring), and FL (fault locating) data.

Each interface contains a UART to provide the TABS link to the GTP and a dual port RAM for bidirectional communications with the terminal station controller. The AS&C and FL circuitries also have a UART for providing communications to regenerator bays using the S3 and S4 service channel, respectively.

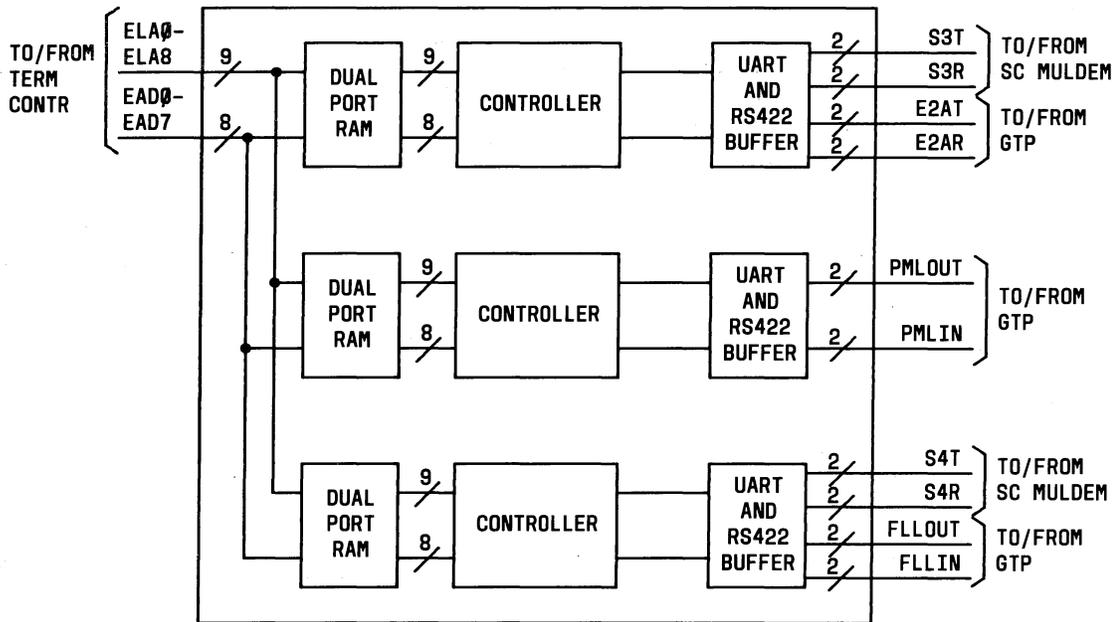


Fig. 67—MC45022A1 FMAS Telemetry

MC45090A1 TERM TELEMTRY

The MC45090A1 TERM TELEM unit (Fig. 68) provides AS&C serial telemetry using TABS protocol at the terminal bay and communications to regenerator bays for implementing remote TABS AS&C capability. The unit contains UARTs to provide the TABS link to the GTP and the link with the regenerator bays. It contains a dual port RAM for bidirectional communication with the terminal station controller. The unit can also be strapped to vary the number of regenerators from which it will collect serial telemetry.

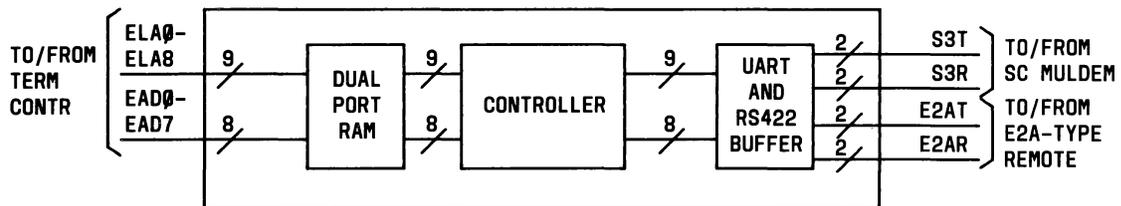
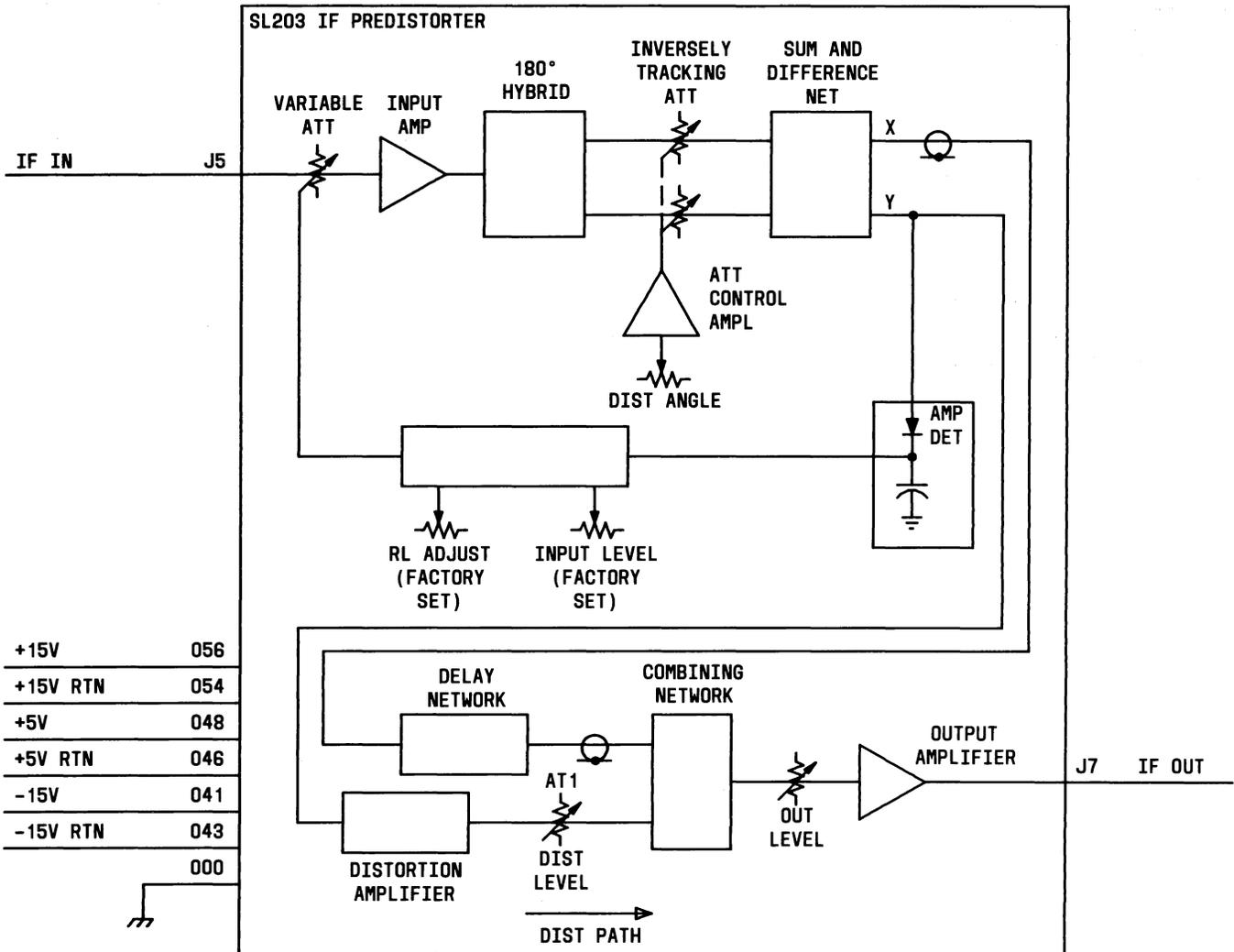


Fig. 68—MC45090A1 TERM Telemetry

SL203 IF PREDISTORTER

The function of the IF predistorter (Fig. 69) is to generate third-order distortion of the proper phase and magnitude to cancel third-order distortion generated in the traveling wave tube or solid-state amplifier at the output of the radio transmitter. This unit is capable of canceling the distortion product by more than 20 dB, thereby allowing greater transmitter output power while meeting the linearity required for 64-QAM transmission. The predistorter operates at 70 MHz with a 40-MHz bandwidth and at an overall gain of 0 dB. Three field adjustable controls are accessible through the faceplate. There are no LEDs or alarms activated by this unit.

The predistorter is capable of canceling distortion over 180 degrees. A field selectable switch is provided to allow cancellation of distortion over a full 360 degrees. The switch is positioned according to whether the LO is above or below the channel frequency of the transmitter. Tables in the IF predistorter procedures in the "Replacement Procedures" tab specify the proper switch position.



NOTE:
 NUMBERS ON LEADS OTHER THAN J NUMBERS ARE PIN NUMBERS OF
 P10 WHICH MATES WITH SL203 IF PREDISTORTER

Fig. 69—SL203 IF Predistorter

SL244 RADIO DATA CARD

The purpose of the radio data card (Fig. 70) is to keep a record of the various frequencies, voltages, currents, and power levels for various components that make up the transmitter and receiver (both regular and diversity). Levels of the output voltages for the dc power supplies used in the transmitter and receiver are permanently recorded for reference purposes only.

There is a place on the radio data card to record the serial numbers of the traveling wave tube (TWT-SN), the power unit (PS-SN), and the control unit (CU-SN) that are used in the transmitter portion of the radio.

Other information that is recorded on the radio data card is the system used and the position numbers and channel numbers for the receiver and transmitter.

SIDE VIEW

FRONT VIEW

RADIO DATA CARD		POSITION NO. _____	
	SYSTEM _____		
	CHANNEL NO. _____		
T R M T R	GEN MON PWR _____	dBm	
	GEN MON FREQ _____	MHz	
	IF IN LEVEL (J4) _____	dBm	
	ALC V NORMAL _____	V	
	AT PWR OUT OF RANGE LIMITS } _____	+ _____ V	
	ALC NET OR } SER NO. _____	- _____ V	
	PWR AMPL } RF MON OUT _____	dBm	
	PWR AMPL } RF OUT _____	dBm	
	FOR TWT APPLICATIONS IK _____	mA	
			TWT-SN _____
		PS-SN _____	
		CU-SN _____	
		IH _____ mA	
	DC-DC POWER SUPPLY } +5.0V±0.3V	+15.0V±0.4V	
	VOLTAGE TOLERANCES } +10.0V±0.3V	+15.0V±0.4V	
R C V R	CHANNEL NO. _____	REG _____	DIV _____
	RF PREAMPL GAIN _____	dB	dB
	RECEIVED SIGNAL LEVEL _____	dBm	dBm
	CONV RF IN _____	dBm	dBm
	CONV IF OUT _____	dBm	dBm
	LIN DEL EQL IF OUT _____	dBm	dBm
	GEN MON PWR _____	dBm	dBm
	GEN MON FREQ _____	MHz	MHz
	IF COMB IF OUT _____	dBm	(SPACE DIV ONLY)
	IF FLT BASIC EQL IF OUT _____	dBm	
	IF AGC AMPL IF OUT _____	dBm	
	AGC V NORMAL _____	V	
	AT LPW IN _____	V	
	ADPT SL EQL IF OUT _____	dBm	
	CONT V MAN _____	V	
CONT V AUTO _____	V		
POSITIVE SL TEST _____	V		
NEGATIVE SL TEST _____	V		

DATA
CARD

SL
244

Fig. 70—SL244 Radio Data Card

TWT AMPLIFIERS (6 AND 11 GHZ)

The TWT amplifier (Fig. 71) is used as the last stage RF signal amplifier in the radio transmitter. These units, which are designed to operate over the entire 6 or 11 GHz common carrier band, have a typical gain of 46 dB and are adjusted for a nominal RF output signal level of +38 dBm. The following controls and/or indications perform the indicated function:

ON-OFF switch: Controls dc power to the TWT power supply. A green ON LED is lighted when the switch is in the ON position.

TRANS-STBY switch: Controls the transmission of the RF signal through the TWT.

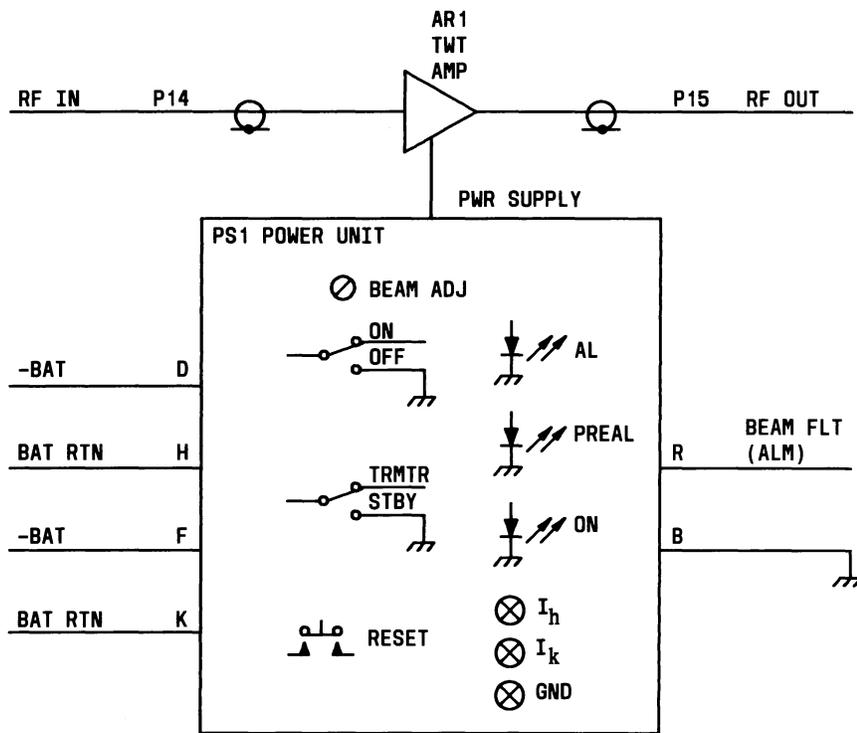
RESET pushbutton: Overrides the shutdown feature and tries to turn on the TWT again.

PREAL: An amber LED. This alarm is activated when the TWT I_h (helix current) increases to within the range of 2.2 to 2.8 mA. The helix current is a measure of how well the TWT is focused. Typically, as the TWT approaches end-of-life, the value of I_h increases and the TWT exhibits a decrease in gain. This alarm is connected to the transmitter alarm and meter network.

AL: A red LED. This alarm indicates a more severe alarm state than the PREAL above and is activated by a higher I_h . When the AL is activated, the TWT shuts down eight times (once per second for eight seconds). If the trouble is not cleared during this interval, the TWT remains shut down. This alarm is not connected to the transmitter alarm and meter network.

I_h and I_k : Test points that allow the measurement of the I_h and I_k (beam current).

BEAM ADJ: An adjustment control used to adjust the TWT beam current to a predetermined value.



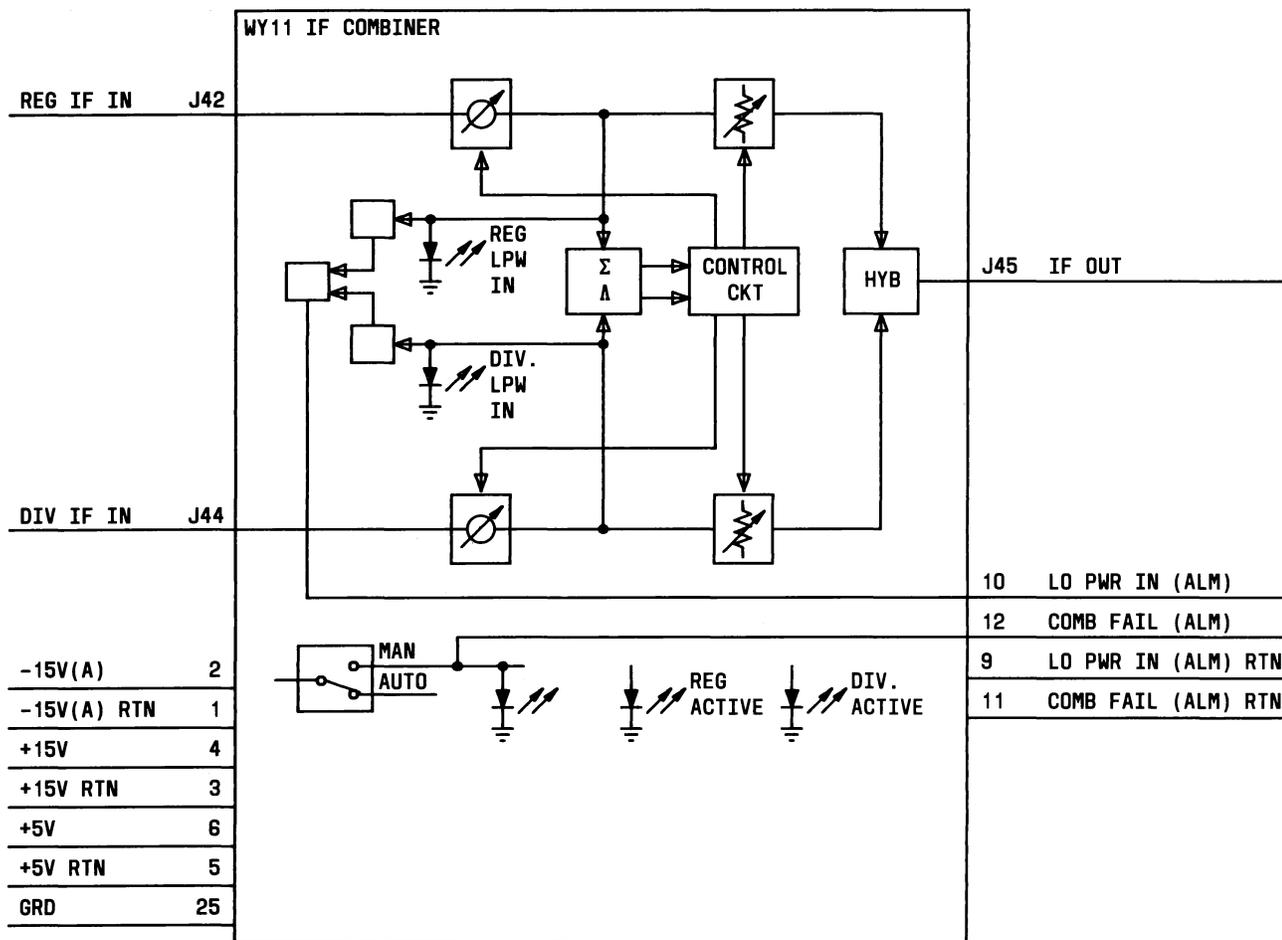
NOTE:
 NUMBERS ON LEADS OTHER THAN J NUMBERS ARE PIN NUMBERS
 OF J9 WHICH CONNECTS TO PS1 POWER UNIT

Fig. 71—TWT Amplifiers (6 and 11 GHz)

WY11 IF COMBINER

The space diversity combiner (Fig. 72) accepts two IF inputs from the down-converter units and combines them into a single IF output signal. This is achieved by measuring the relative phase and amplitude of the applied signals and applying the resulting information to a control algorithm. The algorithm, which is both phase and amplitude dependent, is then used to control the phase and amplitude of the weaker signal prior to combining at the IF output. This method, in essence, permits the radio receiver to select the signal from either or both antennas during fading conditions without causing transmission errors.

An automatic gain control is used to extend the combiner dynamic range during fading conditions. This control may be switched to either the automatic (normal) or to the manual mode of operation. When in the manual mode, an LED (MAN) located on its faceplate is lighted and a manual alarm is initiated. Another alarm is also initiated when the signal level to either IF input is excessively low. Two additional LEDs (REG ACTIVE and DIV ACTIVE), also located on the faceplate, are used to indicate which of the two IF input signals is contributing to the IF output signal.



NOTE:
 NUMBERS ON LEADS OTHER THAN J NUMBERS ARE PIN NUMBERS OF
 J25 WHICH CONNECTS TO WY11 IF COMBINER

Fig. 72—WY11 IF Combiner

YJ102 ADAPTIVE SLOPE EQL

The function of the adaptive slope equalizer (Fig. 73) is to automatically correct for linear amplitude slope of the IF digital spectrum. A control circuit samples the applied signal and controls Bode networks that affect a slope reduction of 10:1. This reduces a fade produced slope of 10 dB across the received signal to 1 dB. This unit simultaneously lights an LED on its faceplate and generates an EXCS SH alarm when the slope at the 70 ± 10 MHz points exceeds approximately ± 7 dB. A pushbutton switch is also provided to allow the equalizer correction to operate in either the manual or automatic (normal) mode. When in the manual mode, this unit simultaneously lights an LED located on its faceplate, initiates a MAN alarm, and places a predetermined correction on the Bode networks.

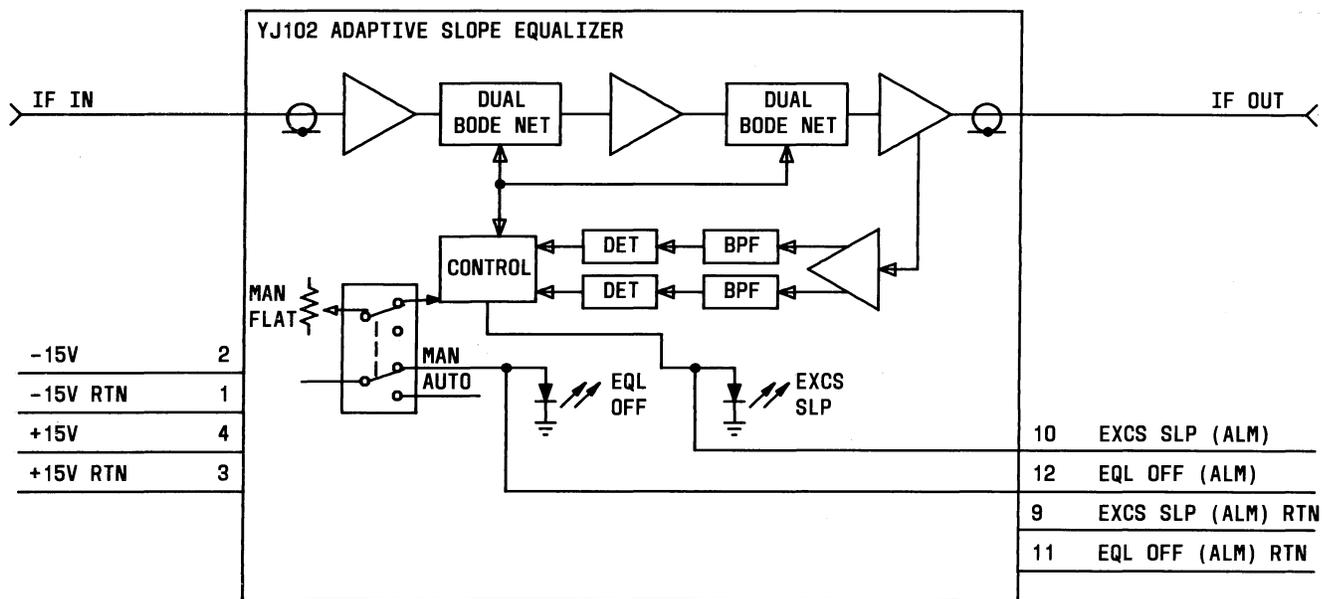


Fig. 73—YJ102 Adaptive Slope Equalizer

YJ104B IF AGC AMPL

The function of the YJ104B amplifier (Fig. 74) is to supply an IF signal with a constant output level of approximately -2 dBm for an input signal level variation of -10 to -55 dBm. This unit makes use of three AGC stages followed by a fixed gain stage that can provide a maximum gain of 75 dB. The amplifier can be switched to operate in either an AGC (AUTO) or a constant gain manual (MAN) mode. Independent AUTO and MAN gain adjust controls are used to set the output level for each mode of operation. The fixed gain MAN mode is not the normal operating mode and is generally used when troubleshooting or performing swept type tests. For this reason, when operated in this mode, the switch also lights a MAN LED located on the faceplate of the unit and initiates a MAN alarm.

A power detector is used to monitor the IF input signal. When this signal falls below a value preset by the LPW IN TRIP adjust control, a LPW IN LED located on the faceplate of the unit is lighted and an LPW IN alarm is initiated. The AGC voltage gives an indication of the received signal level. This voltage is available at the AGC V test points on the faceplate of the unit and is also sent to the ALARM AND METER unit (if equipped) where it can be observed by the meter at that point.

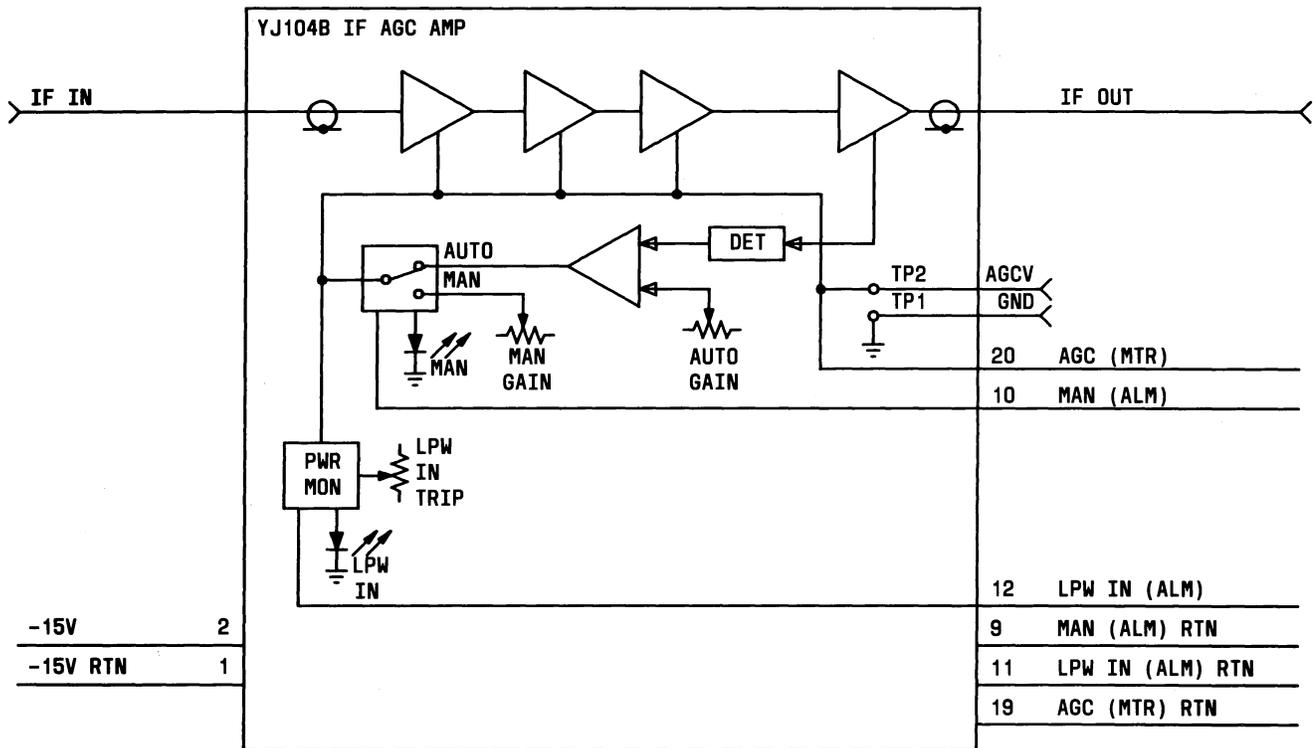


Fig. 74—YJ104B IF AGC Amplifier