

REGISTER SENDERS SD-65816-01  
AND SENDER LINKS SD-65820-01  
OPERATION TESTS  
USING SENDER TEST CIRCUIT SD-65827-01  
STEP-BY-STEP TYPE PBX

1. GENERAL

1.01 This section describes the method of testing the operating features of the register sender and link circuits arranged for dc key-pulsing, using sender test circuit SD-65827-01. Pulsing tests, using the sender test circuit and pulsing checking test set J94723A (SD-96362-01), are also included in this section. Miscellaneous tests which are made without the sender test circuit or pulse checking test set are also included.

1.02 This section is reissued to make minor revisions and to bring the section up to date.

1.03 The tests covered are:

A. *Preference*: This test checks the ability of the sender link to evenly distribute register sender usage and hold the senders busy after seizure until all available senders have been seized.

B. *Registration*: This test checks the ability of the sender to receive signals for conversion to pulses.

C. *Ready Lamp Flutter*: This test checks the ready lamp flutter when digits are keyed faster than the sender outpulses.

D. *Clear*: This test checks the release of the sender, sender link, and link switch before outpulsing is completed.

E. *Trouble*: This test checks the ready lamp flash when trouble is encountered in the signal leads or storage circuit.

F. *Class of Service (Selector Appearance of Central Office Trunk)*: This test checks the ready lamp flutter and sender in preparation for outpulsing at 20 pps.

G. *Class of Service (Switchboard Appearance of Central Office Trunk)*: This test checks the sender for outpulsing at 20 pps.

H. *Timing*: This test checks the time-out features of the sender and sender link.

I. *Group and Select*: This test checks that any attendant position may seize all the sender links and senders.

J. *Pulsing*: This test checks the pulses per second and percent break during sender outpulsing.

K. *Interdigital Timing*: The following features are checked. (1) Busy indication from sender. (2) Sender link made busy. (3) Timing between digits being outpulsed.

1.04 *Tests A to G*: When the test circuit is attached to a particular sender and trouble is encountered or a retest is to be made, operate the CT key on the test circuit to cancel timing. Also, to retest, manually release the sender CS relay and allow it to reoperate to clear the sender.

1.05 *Tests H and I*: The attendant position under test must be made busy.

1.06 *Tests J and K*: Test J shall be applied before Test K. Whenever verification for Test J cannot be met, change PG1 sender pulsing relay and retest. If PG1 relay is changed and verification is not met, see circuit notes in SD-65816-01 for location of resistors and straps for adjusting pulses per second and percent break. Whenever PG1 relay is replaced, Tests J and K shall be applied.

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**1.07 Installation Test:** When this section is used to apply initial tests on the equipment at time of installation, set the D potentiometer of all senders to midposition. Perform each test, A through K, in order.

**1.08 Lettered Steps:** A letter a, b, c, etc, added to a step number in Part 3 or 4 of this section, indicates an action which may or may not be required depending on local conditions. The condition under which a lettered step or a series of lettered steps should be made is given in the ACTION column, and all steps governed by the same condition are designated by the same letter within a test. Where a condition does not apply, all steps designated by that letter should be omitted.

**2. APPARATUS**

**Tests A Through J**

**2.01** Test circuit for register sender and sender link circuits (SD-65827-01).

**2.02** Patching cord, P3U cord, 7 feet long, equipped with one 353A plug (A and B) and one 351G plug (L) (J58837AD List 2 cord assembly) (for connecting the test circuit to a left vertical unit test jack on the link switch).

**2.03** Patching cord, P3U cord, 7 feet long, equipped with one 353A plug (C and D) and one 351G plug (R) (J58837AD List 3 cord

assembly) (for connecting the test circuit to a right vertical unit test jack on the link switch).

**Tests J and K**

**2.04** Blocking and insulating tools, as required. Use tools and apply, as covered in Section 069-020-801.

**Test J**

**2.05** Pulse checking test set, J94723A (SD-96362-01).

**2.06** Patching cord, P3K cord, 12 feet long, equipped with two 310 plugs (3P15B cord) (for connecting the test circuit to the test set).

**2.07** Testing cord, W2M cord, 9 feet long, equipped with two 59 cord tips and one 310 plug (2W12A cord) (for connecting battery and ground to test set).

**Test K**

**2.08** KS-3008 stopwatch, or equivalent.

**3. PREPARATION**

**3.01** The attendant positions appear on a left vertical unit and a corresponding right vertical unit on the link switch. If a spare vertical unit is not provided, an attendant position must be made idle, and the associated vertical units used for all tests.

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<b>STEP</b>	<b>ACTION</b>	<b>VERIFICATION</b>
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**Tests A through J**

1	Connect A,B and C,D plugs of P3U cords to corresponding jacks of test unit.	
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**Tests A through G and J**

2	Connect plugs L, R of P3U cords to idle LEFT, RIGHT vertical unit test jacks on link switch (see 3.01).	
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**Tests H and I**

3	Connect plugs L, R of P3U cords to LEFT, RIGHT vertical unit test jacks on link switch of position to be tested (see 1.05).	
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STEP	ACTION	VERIFICATION
<b>Test J</b>		
4	Connect battery, ground to test set using cord equipped with 310 plug and two 59 cord tips, red lead to ground, white lead to equipment end of a fuse.	
5	Adjust CAL rheostat with PPS/PCB key of test set normal.	Meter reads 0 percent break.

**4. METHOD**

STEP	ACTION	VERIFICATION
<b>A. Preference</b>		
<i>Note:</i> See Table A for sequence of sender seizure.		
3	Depress START key.	RL, SDRS- lamps lighted. Sender link AB- relay released. Sender link ABA- relay operated.
4	Release START key.	RL, SDRS- lamps remain lighted. AB- relay does not operate. ABA- relay remains operated.
5	Depress END key momentarily.	RL, SDRS- lamps extinguished. AB- relay does not operate. ABA- relay remains operated.
6	Repeat Steps 3 to 5, inclusive, until last sender seized.	Last SDRS- lamp lighted. All preceding AB- relays operated. All preceding ABA- relays released. Last sender link AB relay released. Last sender link ABA relay operated.
7	Depress END key momentarily.	RL, last SDRS- lamps extinguished. AB- relay does not operate. ABA- relay remains operated.
8a	If no further tests are to be made — Restore all keys, remove remaining cords.	

**B. Registration**

3	Depress START key momentarily.	RL, SDRS- lamps lighted.
4	Key digit 1.	DIGIT 1 lamp lighted.
5	Key digit 2.	DIGIT 1 lamp extinguished. DIGIT 2 lamp lighted.

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<b>STEP</b>	<b>ACTION</b>	<b>VERIFICATION</b>
6	Key digits 3, 4, 5, 6, 7, 8, 9, 0, 1.  <i>Note:</i> In order to observe the digit being outpulsed it will be necessary to wait until outpulsing of each digit is completed before next digit is keyed.	Preceding DIGIT- lamp extinguished. Succeeding DIGIT- lamp lighted.
7	Depress END key momentarily.	RL, DIGIT-, SDRS- lamps extinguished.
8a	If no further tests are to be made — Restore all keys, remove remaining cords.	
<b>C. Ready Lamp Flutter</b>		
3	Depress START key momentarily.	RL, SDRS- lamps lighted.
4	Key digit 0 six times as rapidly as possible.	RL lamp fluttered. DIGIT 0 lamp lighted. After fourth digit 0 outpulsed, RL lamp lighted steady.
5	Key any five digits, depress END key momentarily.  <i>Note:</i> The last digit outpulsed will not light the digit lamp.	DIGIT lamps light in sequence keyed. When last digit outpulsed, RL, DIGIT-, SDRS- lamps extinguished.
6a	If no further tests are to be made — Restore all keys, remove remaining cords.	
<b>D. Clear</b>		
3	Depress START key momentarily.	RL, SDRS- lamps lighted.
→ 4	Key digit 0 six times, depress CLEAR key (RLS FWD) momentarily before all digits are outpulsed.	DIGIT 0 lamp lighted as each digit outpulsed. When CLEAR key is depressed — Sender stops outpulsing. DIGIT 0 lamp extinguished. After approximately 2 seconds, RL, SDRS- lamps extinguished.
5a	If no further tests are to be made — Restore all keys, remove remaining cords.	
<b>E. Trouble</b>		
3	Depress START key momentarily.	RL, SDRS- lamps lighted.
→ 4	Key digit 0 six times, key digits 7, 8 simultaneously before all digits are outpulsed.	DIGIT 0 lamp lighted as each digit outpulsed. After fifth digit 0 outpulsed, RL lamp flashed at 120 ipm.

STEP	ACTION	VERIFICATION
5	Depress CLEAR key (RLS FWD) momentarily.	DIGIT 0 lamp extinguished. After approximately 2 seconds, RL, SDRS-lamps extinguished.
6a	If no further tests are to be made — Restore all keys, remove remaining cords.	
→	<b>F. Class of Service (Selector Appearance of Central Office Trunk)</b>	
3	Depress START key momentarily.	RL, SDRS- lamps lighted.
4	Key digit 9.	RL lamp fluttered. DIGIT 9 lamp lighted.
→ 5	Operate RV key (nonlocking).	RL lamp lighted steady.  <i>Note:</i> Sender is now conditioned to output at 20 pps (T option), 10 pps (S option).
6	Key digit 1.	DIGIT 9 lamp extinguished. DIGIT 1 lamp lighted.
7	Key digits 2, 3, 4, 5, 6, 7, 8, 9, 0, 1.  <i>Note:</i> In order to observe the digit being outpulsed it will be necessary to wait until outpulsing of each digit is completed before next digit is keyed.	Preceding DIGIT- lamp extinguished. Succeeding DIGIT- lamp lighted.
8	Depress END key momentarily.	RL, DIGIT-, SDRS- lamps extinguished.
→ 9	Restore RV key (nonlocking).	
10a	If no further tests are to be made — Restore all keys, remove remaining cords.	
→	<b>G. Class of Service (Switchboard Appearance of Central Office Trunk)</b>	
3	Depress START key momentarily.	RL, SDRS- lamps lighted.
4	Depress CLA key momentarily.  <i>Note:</i> Sender is now conditioned to output at 20 pps (T option), 10 pps (S option).	
5	Key digits 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, 1.  <i>Note:</i> In order to observe the digit being outpulsed it will be necessary to wait until outpulsing of each digit is completed before next digit is keyed.	DIGIT lamp lighted in sequence keyed. Preceding DIGIT- lamp extinguished. Succeeding DIGIT- lamp lighted.

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<b>STEP</b>	<b>ACTION</b>	<b>VERIFICATION</b>
6	Depress END key momentarily.	RL, DIGIT-, SDRS- lamps extinguished.
7a	If no further tests are to be made — Restore all keys, remove remaining cords.	
<b>H. Timing</b>		
4	Depress START key momentarily.	RL, SDRS- lamps lighted. In approximately 15 to 25 seconds, RL, SDRS- lamps extinguished.
5	Block nonoperated HOLD magnets to which L, R plugs are connected.	
6	Hold START key depressed.	Sender link ST- relay operated. SEL- magnet pulsed. In approximately 2 to 5 seconds, sender link ST- relay released, reoperated.
7	Release START key.	Sender link ST- relay released. SEL- magnet stops pulsing.
8	Remove blocking tools from hold magnets.	
9	Move L, R plugs to vertical unit test jack associated with next position to be tested (see 1.05).	
10	Repeat Steps 4 to 9, inclusive, until all posi- tions have been tested.	
11a	If no further tests are to be made — Restore all keys, remove remaining cords.	
<b>I. Group and Select</b>		
4	Depress START key momentarily.	RL, SDRS- lamps lighted.
5	Depress END key momentarily.	RL, SDRS- lamps extinguished.
6	Repeat Steps 4, 5 until all senders are seized.	
7	Move L, R plugs to vertical unit test jack associated with next position to be tested (see 1.05).	
8	Repeat Steps 4 to 7, inclusive, until all positions have been tested.	
9a	If no further tests are to be made — Restore all keys, remove remaining cords.	

STEP	ACTION	VERIFICATION
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**J. Pulsing**

6	Depress START key momentarily.	RL, SDRS- lamps lighted.
7	Operate CT key on test circuit.	
8	Depress CLA key on test circuit momentarily.	
9	Block nonoperated W relay of sender seized.	
10	Block operated IDC relay of sender seized.	Sender pulsed steady.
→ 11	Connect PPS jack of test circuit to P jack of test set using cord equipped with two 310 plugs.	
12	Operate PCB/PPS key on test set to PCB position.	Meter reads 61.5 to 65.5 percent break.  <i>Note:</i> If verification is not met, see 1.06 and Table B.
13	Operate PCB/PPS key on test set to PPS position.	Meter reads 20 pps (T option), 10 pps (S option).  <i>Note:</i> If verification is not met, see 1.06 and Table B.
→ 14	Release DTI relay manually.	Meter reads 10 pps.  <i>Note:</i> If verification is not met, see 1.06 and Table B. Strap out 600-ohm TR resistor, SD-65816-01 B6.
15	Remove blocking tools.	Sender stops pulsing. Meter reads 0 pulses per second.
16	Restore CT key.	
17	Depress END key momentarily.	RL, SDRS- lamps extinguished.
18	Restore PCB/PPS key.	
19	Repeat Steps 6 to 18, inclusive, on all senders to be tested.	
20	Remove all cords on completion of tests.	

**K. Interdigital Timing**

1	Operate sender MB key.	MB lamp lighted. Sender link AB- relay released. Sender link ABA- relay operated.
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<b>STEP</b>	<b>ACTION</b>	<b>VERIFICATION</b>
2	Block operated CS, RT sender relays.	
3	Block nonoperated RC relay.	
4	Depress sender TS key, start timing.	5.5 seconds elapse before sender stops pulsing.  <i>Note:</i> If this verification is not met, momentarily remove blocking tool from CS relay. Adjust D potentiometer clockwise to increase timing, counterclockwise to decrease timing. Repeat Step 4 until verification is received.
5	Remove blocking tools from CS, RT, RC relays.	
6	Restore MB key.	MB lamp extinguished.

TABLE A

NO. OF SENDERS	SEQUENCE OF SENDER SEIZURE																		
	LINK SWITCH 0								LINK SWITCH 1										
2	0 or 1								1 or 0										
3	0	1 or 2							1	2 or 3									
4	0	1	2 or 3						1	2	3 or 0								
5	0	4	1	2 or 3					1	2	3	0 or 4							
6	0	4	1	5	2 or 3				1	5	2	3	0 or 4						
7	0	4	6	1	5	2 or 3			1	5	2	3	0	4 or 6					
8	0	4	6	1	5	2	7 or 3		1	5	2	7	3	0	4 or 6				
9	0	4	6	1	5	2	7	3 or 8		1	5	2	7	3	9	0	4 or 6		
10	0	4	6	1	5	2	7	9	3 or 8		1	5	2	7	9	3	8	0	4 or 6
	LINK SWITCH 2								LINK SWITCH 3										
2	0 or 1								0 or 1										
3	2	0 or 1							0	1 or 2									
4	2	3	0 or 1						3	0	1 or 2								
5	2	3	0	4 or 1					3	0	4	1 or 2							
6	2	3	0	4	1 or 5				3	0	4	1	5 or 2						
7	2	3	0	4	6	1 or 5			3	0	4	6	1	5 or 2					
8	2	7	3	0	4	6	1 or 5		3	0	4	6	1	5	2 or 7				
9	2	7	3	8	0	4	6	1 or 5		3	8	0	4	6	1	5	2 or 7		
10	2	7	9	3	8	0	4	6	1 or 5		3	8	0	4	6	1	5	2	7 or 9

Note: The last two senders on any link switch will be seized alternately.

TABLE B

CORRECTION FOR PERCENT BREAK AND PULSES PER SECOND				
Percent break 61.5 to 65.5		Pulsing speed		
TO INCREASE	TO DECREASE	PPS	TO INCREASE	TO DECREASE
Decrease PG5 Resistor	Increase PG5 Resistor	10	Decrease PG2 and/or PG4 Resistors	Increase PG2 and/or PG4 Resistors
		20	Decrease PG4 Resistor	Increase PG4 Resistor

Note: If verifications for Steps 12, 13, and 14 are not met, see 1.06 and adjust per Table B.