SL-1

2-Mb/s Digital Trunk Interface

Installation

Publication number: 553-2911-200
Product release: Group H
Document status: Standard
Date: 93 07 31

-

Reason for revision

93 07 31

This NTP has been updated to include the changes requested by PRS AA04566 and a portion of PRS BV20562.

90 11 02

This publication has been changed to add Standard Group F (Phase 6) Generic X11 Supplementary Features.

Contents

General **1-1**
Related documentation 1-1

Installation **2-1**
Equipment 2-1
Circuit pack locations 2-2
Clock Controller card location 2-3
Interfacing the carrier 2-4
Equipment installation 2-5

Data administration **3-1**

Acceptance test **4-1**
QCAD281A cable information 4-4

General

This Northern Telecom Publication (NTP) identifies the equipment associated with the 2-Mb/s Digital Trunk Interface (DTI2) and Japan Digital Multiplex Interface (JDMI) features for Meridian/Meridian 1 SL-1 Generic X11 including Supplementary Features and provides the procedures required to install, add to or change the features. It also includes the required software provisioning procedures (data administration) as well as the appropriate acceptance test procedures.

The features provide an interface between a network loop and an external digital carrier termination for both voice and data transmission over 30 digital channels. The Clock Controller (CC) provides the necessary clocking to enable the system to be either a slave to an external clock or to function as a clocking master.

The features are optionally available for Meridian MS, ST, XT, network enhanced N and XN, and on Meridian 1 System option 21, 51 and 71.

Related documentation

Refer to the following NTPs for additional and related DTI2/JDMI information:

553-2911-100 Feature description

553-2911-500 Maintenance

553-2911-510 Fault Clearing Procedures

553-2001-450 Traffic Measurement

553-2201-150 Equipment Identification and Ordering Information

553-3001-153 Spares Planning Guide

553-2301-511 Maintenance Input/Output

Appendix 2 toFeatures and Services Description and
553-2311-105 Implementation

553-YYY1-210 Detailed SL-1 Installation (for each option).

Refer to the following CCITT Recommendations for general reference information:

- G.703 — Interface at 2048 Kb/s
- G.712 — Performance Characteristics of PCM channels at Audio Frequencies
- G.732 — Characteristics of Primary PCM Multiplex Equipment Operating at 2048 Kbit/s
- Q.171 — Specifications for Instrumentation to Measure Timing and Jitter on Digital Equipment
- Q.422 — Clauses for Exchange Line vs Signaling Equipment
- Q.507 — Transmission Characteristics for Telephony of Digital Exchanges
- Q.724 — Functional Characteristics of Interfaces Associated with Network Nodes

Installation

This section describes the procedures required to install, cable and test the equipment required for the 2-Mb/s Digital Trunk Interface (DTI2) and Japan Digital Multiplex Interface (JDMI) features. These instructions are for the Meridian MS, ST, NT, XT, network enhanced N and XN and Meridian 1 System Options 21, 51 and 71.

Equipment

The features use the following circuit packs:

— QPC536 2-Mb/s Digital Trunk Interface (DTI2)

or

— QPC536D series B 2-Mb/s Digital Trunk Interface (for Italy)

or

— QPC915 2-Mb/s Digital Trunk Interface (for France)

or

— QPC785 Japan Digital Multiplex Interface (JDMI)

— QPC471/QPC775 Clock Controller (CC)

— Cables and EMI Filter.

Note: The QPC471 and QPC775 are not directly interchangeable. In a system with two CCs, the packs must be the same type.

Note: The QPC536D series B circuit pack includes a 4-dB atentuation pad to meet ISPT specification.

Circuit pack locations

The Interface circuit pack occupies two adjacent slots of a Common Equipment (CE) shelf (Table 2-1). Specific locations depend on the machine type and mode of operation as well as the availability of space. Where multiple interfaces are required, as many as six circuit packs can be plugged into an empty Network Shelf along with a Power Converter circuit pack.

When no vacant positions are available to install Interface cards, additional Network shelf(s) can be configured for the existing system in place of a Peripheral Equipment (PE) shelf(s). If an additional cabinet is required to install the additional Network shelves, a cabinet of the following type must be used:

— MS – QCA109

— N, XN, NT, XT, System Options 51, 71 – QCA108

— ST, System Option 21 – QSD73 DTI shelf in the QCA141 cabinet.

MS. Interface packs should only be installed in the CE shelf if the machine is configured for minimum capacity (60 to 180 lines). If the machine is configured for more than 180 lines, the packs should be installed in a CE Expansion shelf (for installation of a CE Expansion shelf. refer to 553-2261-210).

N, NT and System Option 51. If no vacant card slots are available and more interface cards are to be installed, additional network shelves can replace either (or both) PE shelf location on the rear of the CE, tape or disk shelves. In this (additional type) configuration a QUD15 cooling unit and a special power cable (QCAD172A) is required for each shelf added. The number of interface cards must be limited to three per shelf when installed in this additional shelf configuration. Chart 2-7 describes this special installation.

N A network expansion cabinet (QCA108) modified to ***o*** include a QRF8 rectifier and space for 22 DTI/JDMI cards can be ***t*** used to provide for any additional space required. ***e***

Table 2-1
QPC536/QPC785 circuit pack locations

CAUTION:
Circuit pack QPC536/QPC915/QPC785 is a double-width assembly. When installed, it utilizes two adjacent slot positions in the appropriate shelf.

Note: The slots listed herein can only be used if they are not required for other cards. For example, the DTI2 Card can not be inserted into the slot labelled Peripheral Signalling (P.S.).

System	Shelf	Slot
N, NT, XN, XT, System Options 51, 71	Network (LH)	2 – 13
N,NT, XN, XT, System Options 51, 71	Network (RH)	2 – 12
XN, XT, System Option 71	CPU/Memory	9 – 13
N, NT, System Option 51	CPU/Memory	3, 4, 12, 13
MS	CE	2 – 8
MS	CE Expansion	1 – 13
ST, System Option 21	CE	6 – 12
SN	CE	6 – 13*

* If slot number 13 is used, the first PE position is lost.

Clock Controller card location

The Clock Controller circuit pack locations are summarized in Table 2-2.

Note: QPC471 and QPC775 cannot be intermixed in the same

system.

XN	The QPC471/QPC775 CC is located in the CPU shelf.
XT, System Option 71	The QPC471/QPC775 CC is located in the CPU/MEM shelf.
N, NT, System Option 51	The QPC471/QPC775 CC plugs into a network shelf in the slot normally occupied by Intergroup Switch (IGS) 01.
MS	The QPC471/QPC775 CC plugs into a CE shelf in slot 9.
ST, System Option 21	The QPC471/QPC775 CC plugs into a CE shelf in slots 8, 9, 10, 12 or 13.
SN	The QPC471/QPC775 CC plugs into a CE shelf in slots 6 to 10, 12 or 13.

Table 2-2
QPC471/QPC775 Clock Controller circuit pack locations

System	Shelf	Slot
N, NT, System Option 51	Network (LH)	13
N, NT, System Option 51	Network (RH)	2
MS	CE	9
XN	CPU	14
XT, System Option 71	CPU/MEM	15
ST, System Option 21	CE	8, 9, 10, 12, 13
SN	CE	6 to 10, 12, 13

Interfacing the carrier

The DTI2/JDMI provides an interface to the carrier either directly, via channel banks or via office repeater. Regulations require that Network Channel Terminating Equipment (NCTE), such as the Northern Telecom QRY551 Channel Service Unit, may be required at the demarcation point for connections to registered common carrier trunks.

Equipment installation

The following Charts, with associated Tables and Figures, are used when installing, removing or replacing Digital Trunk/Multiplex Interfaces and Clock Controllers:

— Chart 2-1: Installation of Digital Interface

— Chart 2-2: Removal of Digital Interface

— Chart 2-3: Clock Controller Installation/Replacement – Multi-Group (XN, XT, System Option 71)

— Chart 2-4: Clock Controller Installation/Replacement – Single-Group (N, NT, System Option 51)

— Chart 2-5: Clock Controller Installation/Replacement –Half-Group (N, NT, System Option 51)

— Chart 2-6: Clock Controller Installation/Replacement – (MS, ST, System Option 21)

— Chart 2-7: Installation of an N, NT or System Option 51 additional network shelf.

Chart 2-1
Installation of Digital Interface

The Reference column lists sources of additional information.

Step	Task	Reference
1	Determine from the order, the cabinet and shelf location of the circuit pack to be installed. Open the cabinet doors.	553-YYY1-210
2	Unpack and inspect circuit packs	553-YYY1-210
3	Install circuit pack into the assigned shelf and slot.	Table 2-A

4	Install Network circuit pack.	553-YYY1-210 (IP 0128)

—continued—

Chart 2-1 (continued)
Installation of Digital Interface

The Reference column lists sources of additional information.

Step	Task	Reference
5	Install I/O adapters in I/O panel, if required.	553-YYY1-210 (DP 1003)
6	Run and connect cables.	Figure 2-1, 2-2 or 2-3 and Table 2-4

CAUTION:
The QCAD130 cable connecting the QPC471/775 Clock Controller and QPC536/QPC915/QPC785 Interface Card must not be routed through the center of the cabinet past the power harness. Instead, it should be routed around the outside of the equipment shelves.

7	If required, install connecting blocks at MDF or wall mounted cross-connect terminals.	553-YYY1-210
8	If required, designate connecting blocks at MDF or wall mounted cross-connect terminal.	553-YYY1-210
9	If required, install NCTE.	
10	Cross-connect Interface circuits at the Carrier Interface (e.g., Office Repeater, NCTE).	

Note: The distance from the Interface to the Carrier Interface should be a maximum of 400 ft. (121 m).

11	Run Interface Acceptance Test.	Chart 3-1
12	Add related office data into system memory. Refer to work order.	Chart 3-1

Chart 2-2
Removal of Digital Interface

The Reference column lists sources of additional information.

Step	Task	Reference
1	Disable Network Loop using Maintenance Overlay program 60. The command is DISL *'loop number'.*	553-2301-511
2	Remove data from memory.	Chart 3-1
3	Determine from work order, the cabinet and shelf location of the circuit packs to be removed and open cabinet doors.	553-YYY1-210
4	Remove cross connections at MDF or wall-mounted cross-connect terminal.	553-YYY1-210
5	Disconnect cables at carrier interface (e.g., Office Repeater, NCTE).	Figure 2-1, 2-2 or 2-3
6	Tag and disconnect cables from pack. Rearrange CC pack cables if required.	Figure 2-1, 2-2 or 2-3
7	Remove DTI2/JDMI and Network circuit packs.	553-YYY1-210
	Note: If other circuit of dual Network pack is in use, do not do Step 7 for the Network pack	
8	Pack and store circuit pack.	553-YYY1-210

9	Close cabinet doors.	553-YYY1-210

Chart 2-3
Clock Controller installation/replacement
Multi-Group (XN, XT, System Option 71)

CAUTION 1:

Do not deviate from this procedure. Deviation will not cause the system to SYSLOAD or initialize, but could stop call processing.

CAUTION 2:

Call processing will cease if both CC cards are DISABLED, whether in software or via the faceplate switch, regardless of whether the CC to Junctor Board cable is connected or not.

CAUTION 3:

If the CC card in the active CPU shelf is removed, the other card cannot become active and call processing will cease.

CAUTION 4:

If the CC0 is to be replaced, then CC1 and CPU1 must be active, similarly, if CC1 is to be replaced then CC0 and CPU0 must be active.

Note 1: If the cable connecting a CC to the Junctor board is disconnected, the CC card in the active CPU shelf will become active and the clock status display will indicate NO UART. This is normal. Check the cable going from the CC to the Junctor Board if the message appears repeatedly.

Note 2: If the faceplate switch of any CC card is set to DISABLE, the other CC card will become active.

Note 3 The system will operate with only one CC if it is in the ACTIVE CPU shelf.

—continued—

Chart 2-3 (continued)
Clock Controller installation/replacement
Multi-Group (XN, XT, System Option 71)

Note 4: Tracking on a Reference Clock (For QPC471 only); The Clock Controller, when enabled, will be in Free Run mode. It should stay in this mode for several minutes before being switched to tracking mode.

Note 5: Pull-in Time for Tracking Mode; For the QPC471, 20 minutes must pass before the clock is actually locked and tracking. There should be no slips after this time. The QPC775 will lock and track within 10 seconds.

Note 6: The Reference column lists sources of additional information.

Note 7: QPC471 and QPC775 are not interchangeable and cannot be mixed in the same system.

Step	Task	Reference
1	Determine from work order, the cabinet and shelf location of the circuit pack to be installed and open cabinet doors.	553-YYY1-210
2	Add related office data into system memory.	Work order and Chart 3-1
3	Unpack and inspect circuit packs.	553-YYY1-210
4	Set option switches and insert jumper plugs for each QPC471/QPC775 being added.	Table 2-C
5	Set faceplate toggle switch to DISABLE on each QPC471/QPC775 being added.	

6	When replacing an existing QPC471/QPC775 CC card, make sure it is inactive, using overlay program 60. When replacing an existing QPC411 System Clock Generator (SCG) card, make sure it is inactive using overlay program 39.	553-2301-511

—continued—

Chart 2-3 (continued)
Clock Controller installation/replacement
Multi-Group (XN, XT, System Option 71)

Note: Switching Clock Controllers using overlay program 60 may generate ERR20 messages. These can usually be ignored, but excessive switching, especially when counters are near the maintenance or out-of-service thresholds, should be avoided. The switching of clocks could generate maintenance threshold messages or cause the Interface to be automatically disabled. It could also mislead the craftsperson into believing that an actual trouble had caused the maintenance or out-of-service threshold to be exceeded. The contents of counters should be checked, in overlay program 60 and, if necessary, reset using the RCNT command.

Step	Task	Reference
7	On the clock card being replaced, set the faceplate toggle to DISABLE (see Caution 2 and Note 2).	
8	Disconnect cable(s) from QPC411 SCG card or QPC471/QPC775 CC card (see Note 1).	Figure 2-3
9	Remove QPC411 or QPC471/QPC775 card from shelf (see Caution 3 and Note 3).	
10	Install QPC471/QPC775 CC in same slot.	
11	Reconnect QCAD110 cable to faceplate connector J3 of QPC471/QPC775.	Figure 2-3
12	Connect primary reference to J2.	Figure 2-3

13	Connect secondary reference to J1 (if available).	Figure 2-3
14	Set faceplate toggle switch to ENABLE.	
15	Turn off DISABLE LED using overlay program 60 and the commands ENL CC 0 and ENL CC1.	553-2301-511
16	To install second card, first switch the CPU, using overlay program 35 (see Notes 3 and 6).	553-2301-511

—continued—

Chart 2-3 (continued)
Clock Controller installation/replacement
Multi-Group (XN, XT, System Option 71)

Step	Task	Reference
17	Make the second Clock inactive by switching clocks in overlay program 60 (see Note 2).	553-2301-511
18	Repeat Steps 7 to 15.	
19	To track on a primary or secondary reference clock, use overlay program 60. The command is ECKT *"loop"* (see Notes 4 and 5).	553-2301-511

Chart 2-4
Clock Controller installation/replacement
Single-Group (N, NT, System Option 51)

CAUTION 1:

Do not deviate from this procedure. Deviation will not cause the system to SYSLOAD or initialize, but could stop call processing.

CAUTION 2:

Call processing will cease if the CC to CC cable (J3 connector) is connected and BOTH CC cards are disabled by their faceplate switches.

CAUTION 3:

If the CC0 is to be replaced, then CC1 and CPU1 must be active, similarly, if CC1 is to be replaced then CC0 and CPU0 must be active.

Note 1: The CC card can also be plugged into the active shelf without switching the CPU.

Note 2: If the CC to CC cable (connector J3) is disconnected, the card in the active shelf will be active and the clock status display will indicate 'NO UART'. This is normal. The clock cannot be switched unless this cable is connected at both ends.

Note 3: If the CC card is removed from the active shelf, the PS card will distribute clock.

Note 4: If the CC to CC cabinet (connector J3) is disconnected and the faceplate switch of the CC in the active shelf is or becomes disabled, clock control will become disabled and the PS card will

distribute clock. When clock status is read by the CPU, the CC card will respond as being the active clock, but disabled.

Note 5: Always set the faceplate switch to DISABLE before removing or installing the CC to CC cable (J3 connector).

Note 6: If the CC to CC cable (J3 connector) is disconnected, the active CC will report a "NO UART" error when its status is read.

Note 7: Tracking on a Reference Clock (for QPC471 only).
The Clock Controller, when enabled, will be in Free Run mode. It should stay in this mode for several minutes before being switched to tracking mode.

Note 8: Pull-In Time for Tracking mode;
For the QPC471, 20 minutes must pass before the clock is actually locked and tracking. There should be no slips after this time. The QPC775 will lock and track within 10 seconds.

Note 9: QPC471 and QPC775 are not interchangeable and cannot be mixed in the same system.

Note 10: The Reference column lists sources of additional information.

– continued –

Chart 2-4 (continued)
Clock Controller installation/replacement
Single-Group (N, NT, System Option 51)

Step	Task	Reference
1	Determine from the work order, the cabinet and shelf location of the circuit packs to be installed. Open the cabinet doors.	553-YYY1-210
2	Unpack and inspect circuit packs.	553-YYY1-210
3	Set option switches and insert option plugs on the QPC471/QPC775 being added.	Table 2-C

4	On the QPC441 3PE cards in Network Shelves housing CC cards, set option switch position 2 to ON.	553-YYY1-210
5	Set faceplate toggle switch to DISABLE on the QPC471/QPC775 being added.	
6	When replacing an existing QPC471/QPC775 CC card, make sure all DTI2/JDMI channels are disabled while idle using overlay program 60.	553-2301-511

Note: Switching Clock Controllers using overlay program 60 may generate ERR20 messages. These can usually be ignored, but excessive switching, especially when counters are near the maintenance or out-of-service thresholds, should be avoided. The switching of clocks could generate maintenance threshold messages or cause the Interface to be automatically disabled. It could also mislead the craftsperson into believing that an actual trouble had caused the maintenance or out-of-service threshold to be exceeded. The contents of counters should be checked, and if necessary, reset using the RCNT command in overlay program 60.

7	On the clock card being replaced, set the faceplate toggle to DISABLE (see Cautions 2 and 3).	
8	Disconnect cable(s) from Clock card (see Caution 2 and Notes 2 to 6).	Figure 2-2
9	Remove card from shelf (see Notes 3 and 4).	

—continued—

Chart 2-4 (continued)
Clock Controller installation/replacement
Single-Group (N, NT, System Option 51)

Step	Task	Reference
10	Install QPC471/QPC775 CC in the same slot (see Note 1).	

11	Connect cable to faceplate connector J3 (see Note 5).	Figure 2-2
12	Connect primary reference to J2.	Figure 2-2
13	Connect secondary reference to J1 (if available).	Figure 2-2
14	Set faceplate toggle switch to ENABLE.	
15	Turn off DISABLE LEDs using overlay program 60 and the commands ENL CC 0 and ENL CC 1.	
16	Add related office data into system memory.	Work order, Chart 3-1
17	Repeat Steps 3 to 16.	
18	To track on a primary or secondary reference clock, use overlay program 60. The command is ECKT *'loop'* (see Notes 7 and 8).	553-2301-511

Chart 2-5
Clock Controller installation replacement
Half-Group (N, NT, System Option 51)

CAUTION:
Do not deviate from this procedure. Deviation will not cause the system to SYSLOAD or initialize, but could stop call processing.

Note 1: Tracking on a Reference Clock (for QPC471 only); The CC, when enabled, will be in Free Run mode. It should stay in this mode for several minutes before being switched to tracking mode.

Note 2: Pull-In Time for Tracking mode;
For the QPC471, 20 minutes must pass before the clock is actually locked and tracking. There should be no slips after this time.
The QPC775 will lock and track within 10 seconds.

Note 3: QPC471 and QPC775 are not interchangeable and cannot be mixed in the same system.

Note 4: The Reference column lists sources of additional information.

Note 5: The CC status display in this mode will indicate "NO UART".

Step	Task	Reference
1	Determine from the work order, the cabinet and shelf location of the circuit pack to be installed. Open the cabinet doors.	553-YYY1-210
2	Unpack and inspect circuit pack.	553-YYY1-210
3	Set option switches and insert option plugs on the QPC471/QPC775 being added.	Table 2-C

—continued—

Chart 2-5
Clock Controller installation replacement
Half-Group (N, NT, System Option 51)

Step	Task	Reference
4	Set faceplate toggle switch to DISABLE on the QPC471/QPP775 CC card using overlay program 60, make sure all DTI2/JDMI channels are disabled while idle (use command DISA *'loop'*). Use the command TRCK FRUN to make CC free run.	553-2301-511
	Note: Switching Clock Controllers using overlay program 60 may generate ERR20 messages. These can be ignored in this case.	
5	On the CC card being replaced, set faceplate toggle to DISABLE.	
6	Disconnect cable(s) from Clock card and remove card from the shelf.	Figure 2-1
7	Install QPC471/QPC775 CC in the Network shelf.	
8	Connect primary reference to J2.	Figure 2-1
9	Connect secondary reference to J1 (if available).	Figure 2-1
10	Set faceplate toggle switch to ENABLE.	
11	Turn off DISABLE LED using overlay program 60 and the command ENL CC 0.	553-2301-511
12	Add related office data into system memory.	Work order, Chart 3-1

13	a) Enable all channels on DTI2/JDMI and clear all errors using overlay program 60. b) To track on a primary or secondary clock, use overlay program 60. The command is ECKT *'loop'* (see Notes 1 and 2).	553-2301-511

Chart 2-6
Clock Controller installation/replacement (MS, ST, System Option 21)

CAUTION:
Do not deviate from this procedure. Deviation will not cause the system to SYSLOAD or initialize, but could stop call processing.

Note 1: Pull-In Time for Tracking mode. For the QPC471, 20 minutes must pass before the clock is actually locked and tracking. There should be no slips after this time. The QPC775 will lock and track within 10 seconds.

Note 2: QPC471 and QPC775 are not interchangeable and cannot be mixed in the same system.

Note 3: The Reference column lists sources of additional information.

Step	Task	Reference
1	Unpack and inspect circuit pack.	553-YYY1-210
2	Set option switches and insert option plugs on the QPC471/QPC775 being added.	Table 2-C
3	Set faceplate toggle switch to DISABLE on the QPC471/QPC775 being added.	

4	When replacing an existing QPC471/QPC775 CC card using overlay program 60, make sure all DTI2/JDMI channels are disabled while idle (use command DISA *'loop'*). Use the command TRCK FRUN to make CC free run.	553-2301-511

Note: Switching Clock Controllers using overlay program 60 may generate ERR20 messages. These can be ignored in this case.

—continued—

Chart 2-6 (continued)
Clock Controller installation/replacement
(MS, ST, System Option 21)

Step	Task	Procedure
5	On the clock card being replaced, set the faceplate toggle to DISABLE.	
6	Disconnect cable(s) from Clock card.	Figure 2-1
7	Remove card from shelf.	
8	For MS, install QPC471/QPC775 CC in slot 9 of the CE shelf. For ST, install QPC471/QPC775 CC in slot 8, 9, 10, 12 or 13.	
9	Connect primary reference to J2.	Figure 2-1
10	Connect secondary reference to J1 (if available).	Figure 2-1
11	Set faceplate toggle switch to ENABLE.	
12	Turn off DISABLE LED using overlay program 60 and the command ENL CC 0.	553-2301-511
13	Add related office data into system memory.	Work order, Chart 3-1

14	a) Enable all channels on DTI2/JDMI and clear all errors using overlay program 60. b) To track on a primary or secondary reference clock, use overlay program 60. The command is ECKT *'loop'* (see Notes 1 and 2).	553-2301-511

Chart 2-7
Installation of an additional network shelf to an N, NT or System Option 51

CAUTION:
The maximum number of QPC536/QPC915/QPC785 cards must not exceed three per shelf, because the Network shelf cable harness(es) share the power breaker associated with each CPU for Interface cards in N, NT, System Option 51.

Note 1: This procedure is used when additional shelf space is required for DTI2/JDMI cards in N, NT or System Option 51. A QUD15 cooling unit is required for each additional shelf installed. When additional Interface shelf space is required for MS, XT, XN, or System Option 51, consult the applicable 553-YYY1-210 NTP.

Note 2: The Reference column lists sources of additional information.

Note 3: The CC status display in this mode will indicate NO UART. This is normal since the SL-1 is operating in the Half-Group mode.

Step	Task	Reference
1	Determine from the work order, the cabinet and shelf location of the Network shelf to be installed. Open the cabinet doors.	553-YYY1-210
2	Unpack and inspect the shelf.	553-YYY1-210
3	Remove the existing left or right rear PE shelf (if required).	553-YYY1-210
4	Install the additional Network shelf in the PE (Step 3) location.	553-YYY1-210

5 Install a QUD15 cooling unit directly below the Network shelf and secure with 4 mounting screws.

—continued—

Chart 2-7 (continued)
Installation of an additional network shelf to an N, NT or System Option 51

Step	Task	Procedure
6	Install and connect the QCAD172A power cable to the added QUD15 cooling unit as follows: If the added QUD15 is located below the left Network shelf, unplug the C11 connector from the QCAD111 power harness that connects to the existing left side QUD15 and plug it into the single ended connector of the QCAD172A power cable. Plug one of the two connectors at the other end of the QCAD172A power cable into the existing QUD15 (replaces the C11 that was removed previously). Plug the remaining connector of the QCAD172A power cable into the added QUD15. If the added QUD15 is located below the right Network shelf, the procedure is identical except the C21 connector from the QCAD111 power harness is used instead of the C11.	
7	At the QCAD111 power wiring harness, untie and then connect the C17 connectorized power connection cable to the right rear Network Shelf (use the C19 connectorized cable if connecting to the left rear Network shelf).	553-YYY1-210

CAUTION:
Do not place the circuit packs into the shelf until this step is completed.

8	Install DTI2/JDMI trunks and enter related shelf and Interface office data into system memory.	Chart 2-1 Chart 3-1

Table 2-3
QPC471/QPC775 Clock Controller option settings

		SL-1 Type		
Controller	**Switch**	**XN**	**N**	**MS**
QPC471A	SW2	OFF	ON	N.A.
QPC471B, C	SW1	OFF	ON	ON
	SW2	OFF	OFF	ON
	Jumper Plug J1	TP8-TP9	TP8-TP9	TP8-TP9
	Jumper Plug J2	TP11-TP12	TP11-TP12	TP11-TP12
QPC775	SW2	OFF	ON	ON
	SW2	OFF	OFF	ON
	SW4 (1, 2)	ON	ON	OFF

Table 2-4
Digital Interface cabling — Single-and Half-Group (N, NT, ST, MS, System Options 21, 51)

Note 1: Run only when DTI2/JDMI unit is the primary reference clock source.

Note 2: Run only when DTI2/JDMI unit is the secondary reference clock source.

Note 3: Run for Single-Group mode only.

Note 4: Run to connector on associated network panel.

Note 5: Run via cabinet I/O panel to cross-connect terminal (NCTE)

Note 6: Run to cross-connect terminal (NCTE).

Note 7: QPC536 may be QPC785 or QPC915.

—continued—

Table 2-4 (continued)
Digital Interface cabling — Single-and Half-Group (N, NT, ST, MS, System Options 21, 51)

Cable type	From	Des	Con	To	Des	Con	Note
QCAD130	QPC536	DTI2	J1	QPC471/775	CC-0	J2	1
QCAD130	QPC536	DTI2	J1	QPC471/775	CC-0	J1	2
QCAD130	QPC536	DTI2	J2	QPC471/775	CC-1	J2	1, 3
QCAD130	QPC536	DTI2	J2	QPC471/775	CC-1	J1	2, 3
QCAD125	QPC471	CC-0	J3	QPC471/775	CC-1	J3	3
NEA18QA	QPC536	DTI2	J4	Network			4
(Optional) QCAS282A	QPC536	DTI2	J3	I/O Panel			
(Optional) QCAD282A	I/O Panel			NCTE			5
QCAS281A	QPC536	DTI2	J3	NCTE			6

Table 2-5
Digital Interface cabling
Multi-Group (XN, ST, System Option 21)

Note 1: Run only when DTI2 unit is the primary reference clock source.

Note 2: Run only when DTI2 is the secondary reference clock source.

Note 3: Run to connector on associated network panel.

Note 4: Run via cabinet I/O panel to cross-connect terminal (NCTE).

Note 5: Run to cross-connect terminal (NCTE).

Note 6: QPC536 may be QPC785 or QPC915.

Cable type	From	Des	Con	To	Des	Con	Note
QCAD130	QPC536	DTI2	J1	QPC471/775	CC-0	J2	1
QCAD130	QPC536	DTI2	J1	QPC471/775	CC-0	J1	2
QCAD130	QPC536	DTI2	J2	QPC471/775	CC-1	J2	1
QCAD130	QPC536	DTI2	J2	QPC471/775	CC-1	J1	2
QCAD110	QPC471/ QPC775	CC-0	J3	QPC417	JCTR	J11	
QCAD110	QPC471/ QPC775	CC-1	J3	QPC417	JCTR	J12	
QCAD12F	QPC536	DTI2	J4	Network			3
(Optional) QCAD28A	QPC536	DTI2	J3	I/O Panel			4
(Optional) QCAD28A	I/O Panel			NCTE			4

QCAD28A	QPC536	DTI2	J3	NCTE	5

Figure 2-1
DTI2/CC cabling arrangement
(N, NT Half-Group, MS, ST, System Option 21)

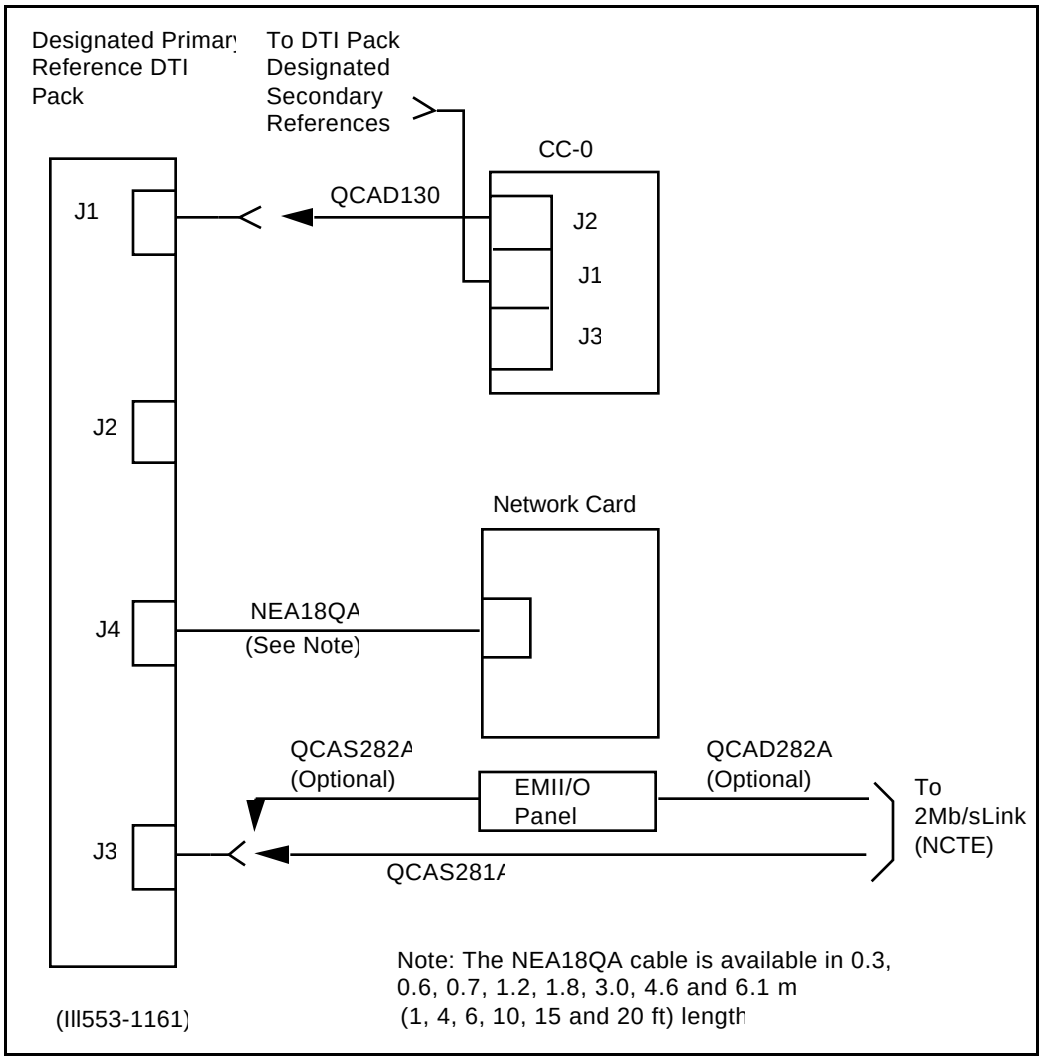
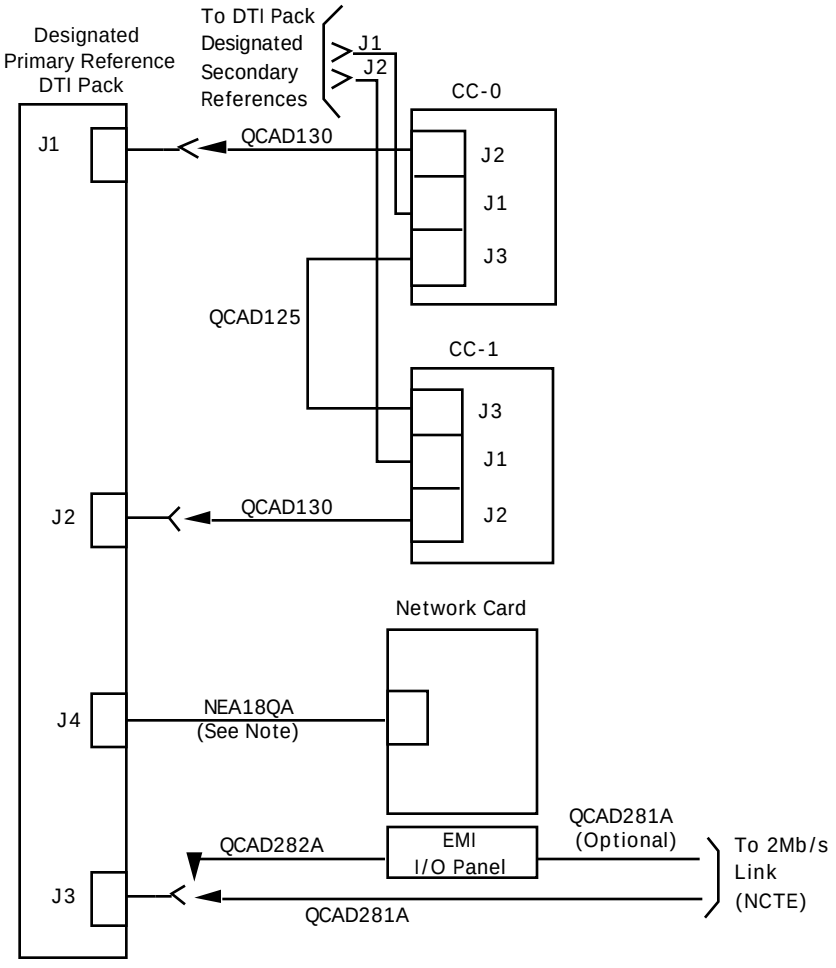
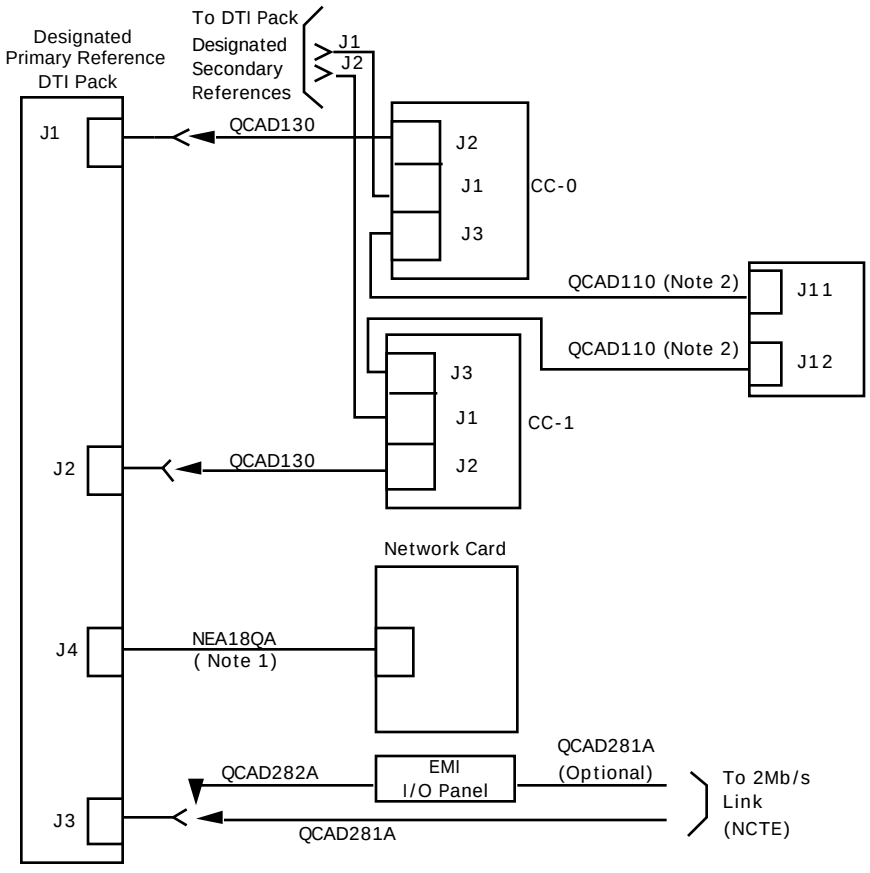


Figure 2-2
DTI2/CC cabling arrangement (N, NT Single-Group)



Note: The NEA18QA cable is available in 0.3, 0.6, 0.7, 1.2, 1.8, 3.0, 4.6 and 6.1 m (1, 4, 6, 10, 15 and 20 ft) lengths.

Figure 2-3
DTI2/CC cabling arrangement
(XN, XT, System Option 51)



Note 1: The NEA18QA cable is available in 0.3, 0.6, 0.7, 1.2, 1.8, 3.0, 4.6 and 6.1 m (1, 4, 6, 10, 15 and 20 ft) lengths.

Note 2: The QCAD110B cable is available in 3 m (10 ft) lengths. The QCAD110A cable is available in 7.6 m (25 ft) lengths.

(lll553-1163)

Figure 2-4
JDMI/CC cabling arrangement
(ST, System Option 21)

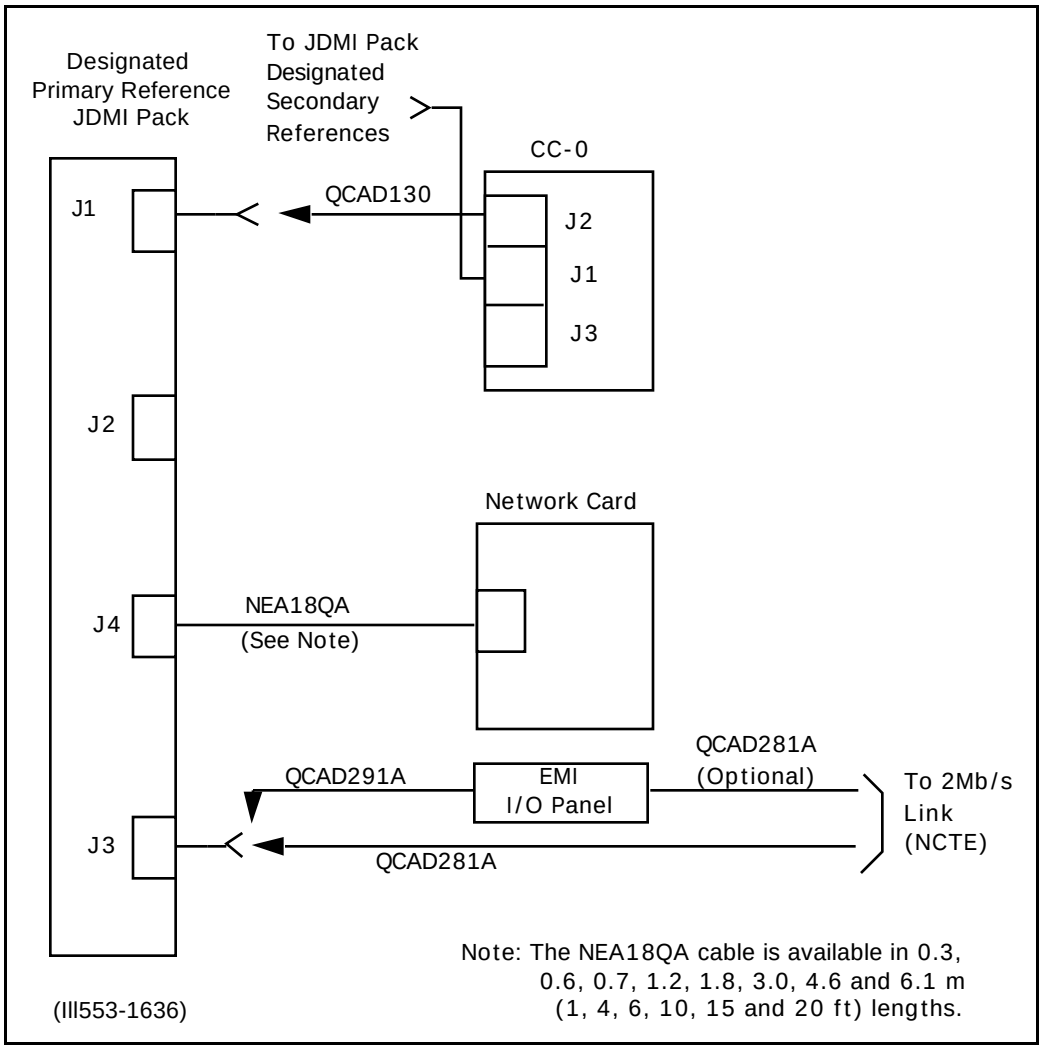


Figure 2-5
JDMI/CC cabling arrangement
(N, XN, MS Half-Group)

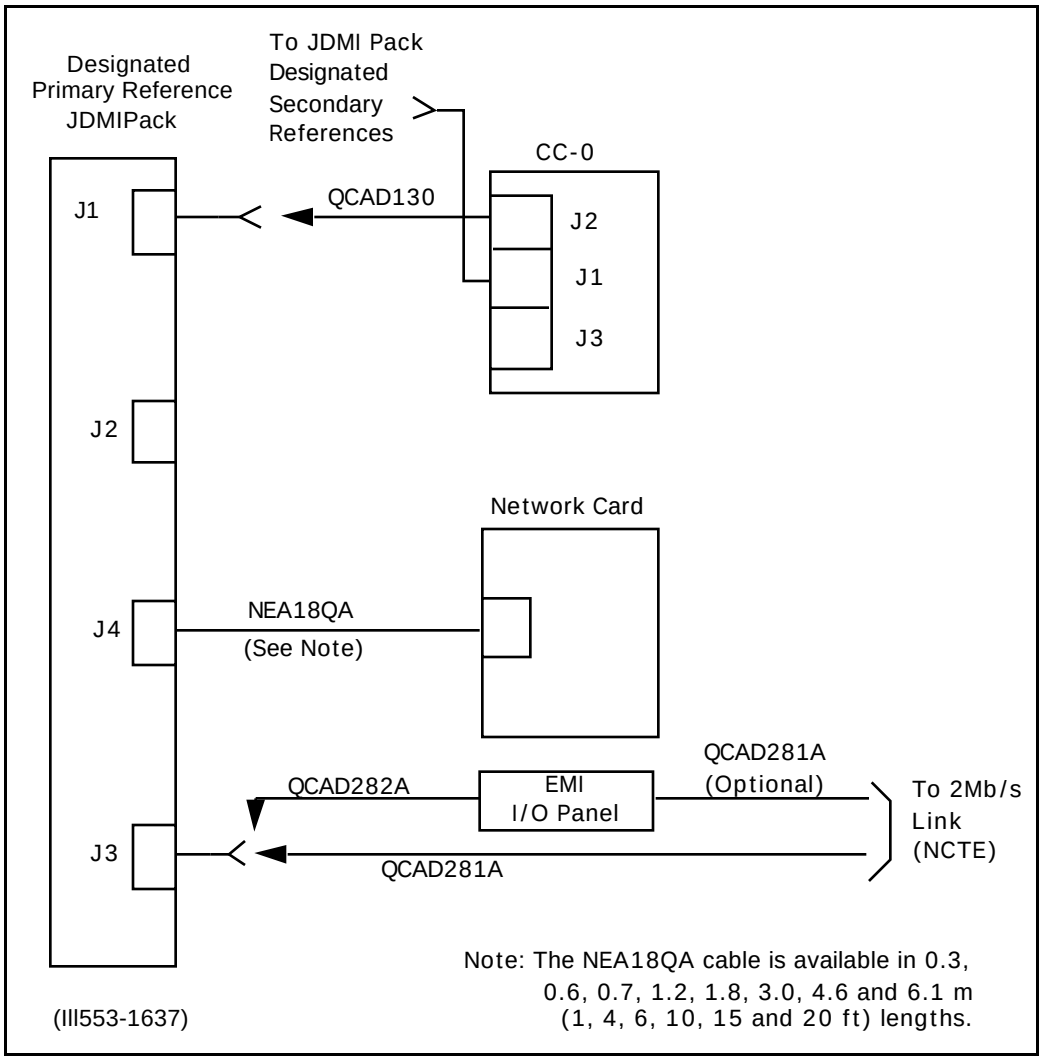


Figure 2-6
JDMI/CC cabling arrangement (N, NT Single-Group)

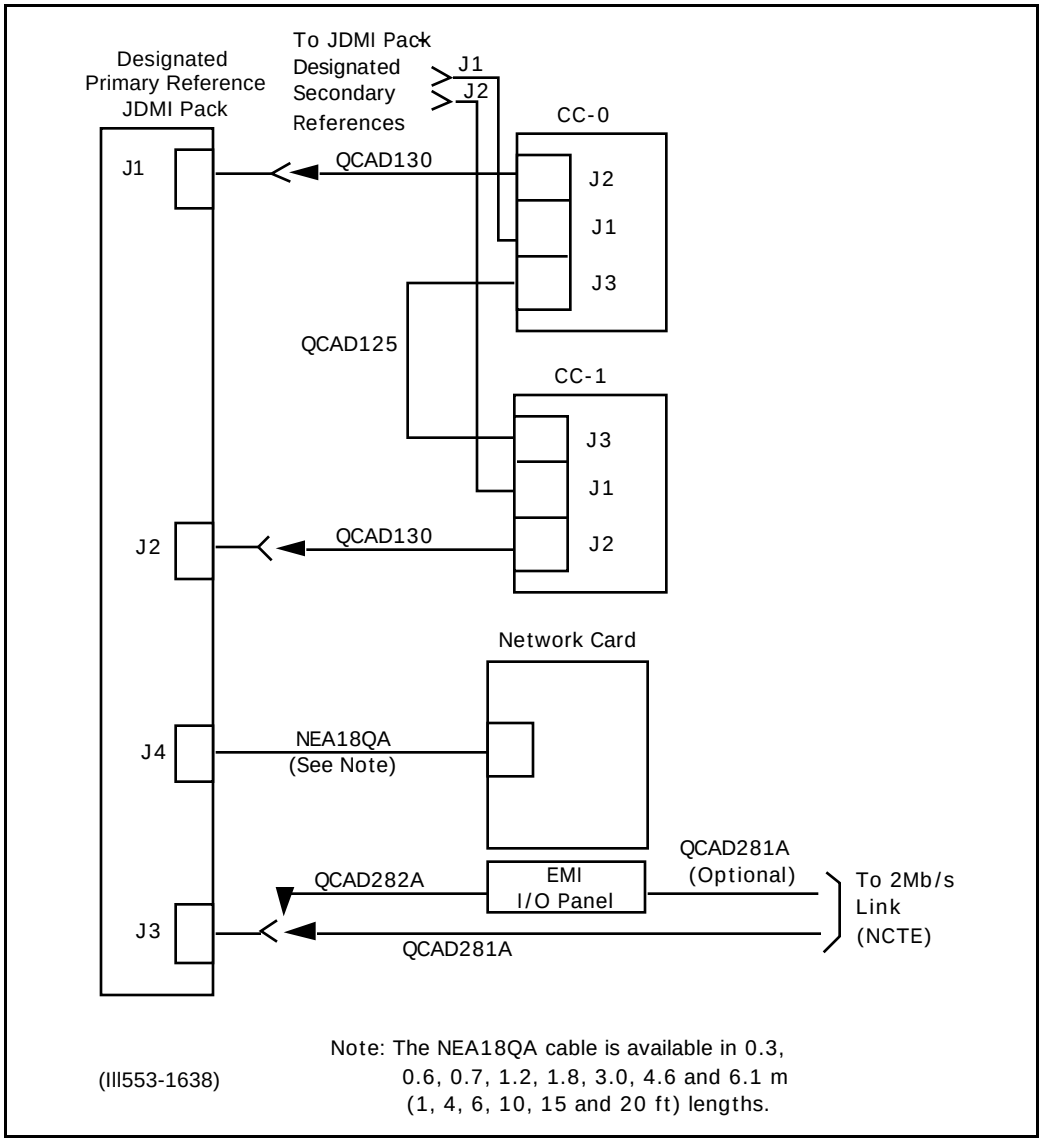
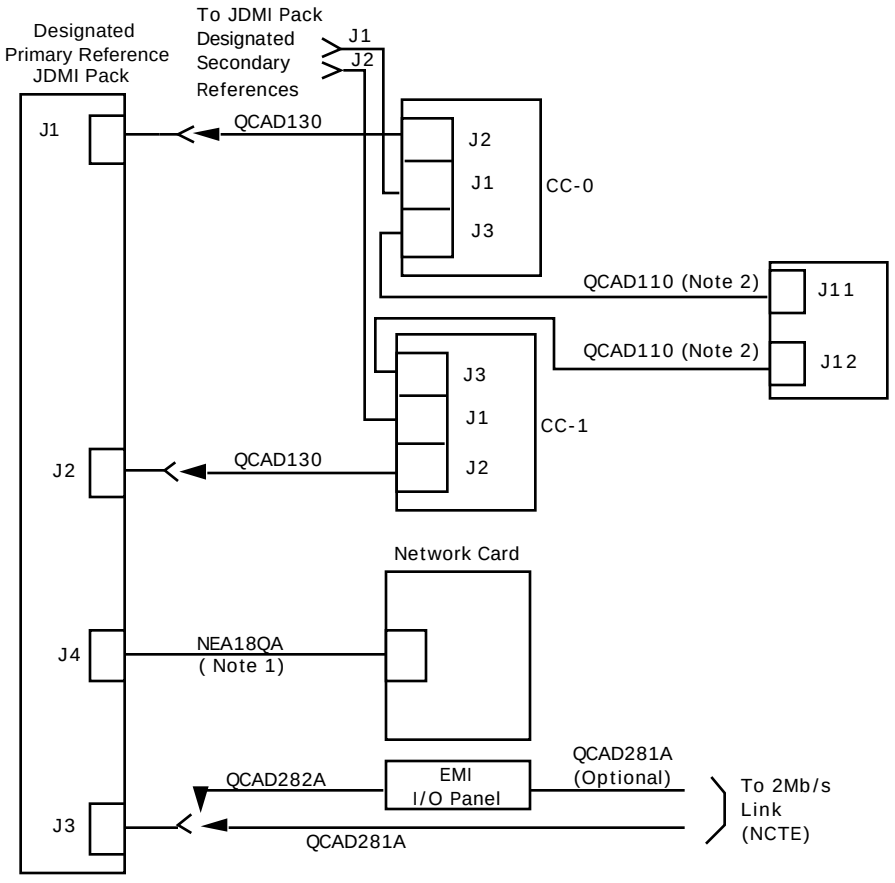


Figure 2-7
JDMI/CC cabling arrangement
(XN, XT, System Option 51)



Note 1: The NEA18QA cable is available in 0.3, 0.6, 0.7, 1.2, 1.8, 3.0, 4.6 and 6.1 m (1, 4, 6, 10, 15 and 20 ft) lengths.

Note 2: The QCAD110B cable is available in 3 m (10 ft) lengths. The QCAD110A cable is available in 7.6 m (25 ft) lengths.

(lll553-1639)

Data administration

The 2-Mb/s Digital Trunk Interface (DTI2) and Japan Digital Multiplex Interface (JDMI) impact the following Service Change and Print programs, the complete description of which is found in Appendix 1 to 553-2311-311:

10,11,12,13	Terminals
14	Trunks
16	Route
17	System Configuration
20	Print Routine 1
21	Print Routine 2
22	Print Routine 3
25	Move Data Blocks
73	Digital Trunk Interface

Chart 3-1 describes the data administration procedures for the DTI2/JDMI feature. These include adding, changing, moving, removing and querying these interface features.

Chart 3-2 shows the ABCD table defaults.

Chart 3-3 describes the data administration procedures for the following 2-Mb/s DTI enhancements:

— Direct Inward Dialing Call Offering

— Fault Signal

— Release Control

The information presented here assumes the reader is familiar with the general principles of data administration on the SL-1 as described in 553-3001-300 and appendix 1 to 553-2311-311.

Table 3-1
Data administration: Digital Interface and Clock Controller

1. Response is required to the following prompts in Overlay Program 17:

Prompts	Responses	Comments
REQ	NEW,CHG,MOV	create a new data block
:		
:		
DTI2	L L L	Loop available for DTI2
		Only prompted if DTI2 package equipped.
		If channels are still allocated to loop *'l'* an error message is issued and response is not allowed.
JDMI	L L L	Loop available for JDMI
		Only prompted if DTI2 and JDMI packages are equipped.
		If channels are still allocated to loop '*l*' an error message is issued and response is not allowed.
	XL	Remove loop

PCML	MU/(A)	System PCM law

—continued—

Table 3-1 (continued)
Data administration: Digital Interface and Clock Controller

2. Response is required to the following prompts in Overlay Program 14:

Prompts	Responses	Comments
REQ	NEW,CHG,MOV	create a new data block
TYPE	T	RLR and RLM are added to COT, WAT, FEX, DID and TIE as legal types for DTI2 and JDMI.
TN	L Ch	If the DTI2 package is equipped, and if type is a legal DTI2 type, then this prompt will accept a DTI2 loop 'L' and channel number 'Ch' will be valid in the extended range "1-30". Loop must already be defined in the Configuration record (LD 17). For OUT command, no further prompts are given. For MOV command, the next and last prompt is TOTN. For NEW and CHG commands, the next prompt will be SICA.
TOTN	L Ch	For MOV command only, 'L' and 'Ch' as for TN prompt. DTI2/JDMI TNs can only move to DTI2/JDMI loops. No further prompts given for MOV command.
:		
:		

RTMB	0-127, 1-126	Route member number. Route's DTRK type must match loop type.

—continued—

Table 3-1 (continued)
Data administration: Digital Interface and Clock Controller

Prompts	Responses	Comments
SICA	(1)-16	Signaling category table number. For 2 to 16, the category used must already have been defined in LD 73. Default is 16 if loop type is JDMI.
PDCA	(1)-16	Pad Category table number. For 2 to 16, the category used must already have been defined in LD 73. Pads are not used during a Data call. Default is 16 if loop type is JDMI.
PCML	MU/A	'MU' or 'A' law PCM active in channel. Conversion is required only when the call originates or terminates on the switch and the channel is running with a different law PCM. Conversion is done on both outgoing and incoming calls. Conversion is not done during a Data call, but this information is still required for call set-up. Not prompted for JDMI loops (when Channel PCML is set same as System PCML to ensure that no conversion is done).

3. Response is required to the following prompts in Overlay Program 16:

REQ	NEW, CHG	create a new data block
:		
DTRK	(NO), YES	Digital Trunk Route

—continued—

Table 3-1 (continued)
Data administration: Digital Interface and Clock Controller

Prompts	Responses	Comments
DGTP		Digital Trunk type for this route Prompted only if DTRK = YES and DTI2 or PRI2 package is equipped.
:		
	(DTI)	1.5-Mb/s DTI
	PRI	ISDN (23B + D)
	DTI2	2-Mb/s DTI
	PRI2	ISDN (30B + D)
	JDMI	Japan Digital Multiplex Interface
DSEL	DTA, VCE, (VOD)	On a DTI2 route, this existing prompt will appear for any legal DTI2 route type. A 1.5-Mb/s DTI will only prompt this for TIE routes since 1.5-Mb/s DTI only allows data to be used for TIE trunks.
:		
:		
OPDL	(0)-8064	Outpulsing delay (milleseconds) Prompted only if DGTP = DTI2 or JDMI.

4. Response is required to the following prompts in Overlay Program 73:

Note: The ABCD response represents the following trunk supervisory signals:

— Steady signals - bits 0, 1 or U (where U = do-not-care). If c or d are not input they default to 0 and 1 respectively.

— Pulsed signals - P (pulsing), X (not pulsed) or U (do-not-care)

—continued—

Table 3-1 (continued)
Data administration: Digital Interface and Clock Controller

— For JDMI applications, only the *'a'* signaling bit of the *'abcd'* string is required: however all four bits are allowed to be set. The software will use all four bits for call processing as usual, but ignore the *'bcd'* bits for sending and receiving; these will be defaulted by hardware to 101 for reporting signaling changes. Therefore, if any changes are made to received signals, the *'bcd'* bits must be set to 101 or else these signals will not be recognized.

Prompts	Responses	Comments
REQ	NEW	create a new data block
	CHG	modify existing data
	PRT	print the specified data
	OUT	remove data block
	END	terminate overlay activity
TYPE	DTI2	2-Mb/s DTI
	DDB	1.5-Mb/s DTI
FEAT	ABCD	digital signaling category
	PAD	digital pad category
	LPTI	digital loop timers and signals
	SYTI	digital system timers and counter
If FEAT - ABCD, the following prompts are given		
(See Table 3-2 for default ABCD table with suggested values):		
SICA	2-16	signaling category
	1	if REQ = PRT then 1 must be input to print default table

<CR>	if REQ = PRT all signaling tables are printed

—continued—

Table 3-1 (continued)
Data administration: Digital Interface and Clock Controller

Prompts	Responses	Comments
TNLS	YES, (NO)	list of trunk TNs using requested SICA tables will (will not) be printed following the table
DFLT	(1)-16	default signaling category to be used for default values
Incoming/outgoing calls		
IDLE(S)	abcd	(send) idle signal bits 0 or 1
IDLE(R)	abcd	(receive) idle signal bits 0 or 1
FALT(S)	abcd	(send bits 0 or 1 DTI out-of-service
	N	if FALT (send) signal not required
FALT(R)	abcd	(receive) bits 0 or 1 DTI out-of-service
	N	if FALT (receive) signal not required
Incoming calls		
SEZ(R)	abcd	seize signal (send or receive) for voice or data calls from or to a non SL-1. Bits 0 or 1
SEZD(R)	abcd	seize signal (send or receive) for data calls between SL-1s. Bits 0 or 1
	N	if SEZD(R) signal not required
SEZV(R)	abcd	seize signal (send or receive) for voice calls. Bits 0 or 1
	N	if SEZV(R) signals not required

P CALL(R)	abcd	(receive) signal sent during seize by an incoming PSTN trunk

—continued—

Table 3-1 (continued)
Data administration: Digital Interface and Clock Controller

Prompts	Responses	Comments
TIME	ON, OFF	length of pulse time off, and time on. (default 2 seconds on, 8 seconds off)
SEZA(S)	abcd	seize signal acknowledgement (send). Bits 0 or 1
	N	if SEZA(S) signal not required
P WNKS(S)	abcd	wink start (corresponds to a pulsed seize acknowledgement). prompt if SEZA(S) not required
	N	if WNKS(S) signal not required
TIME	10-630 (220)	time for WNKS(S) signal in milleseconds
P DIGT(R)	abcd	(receive) decadic pulse
	N	if DIGT(R) not required
NRCV(S)	abcd	number received signal (send). Bits 0 or 1
	N	if NRCV(S) signal not required
P EOSF(S)	abcd	end of selection free (send)
	N	if EOSF(S) not required
TIME	100-150 (100)	time for EOSF(S) in milleseconds
P EOSB(S)	abcd	end of selection busy (send)
	N	if EOSB(S) not required
TIME	100-150 (100)	time for EOSB(S) in milleseconds
P OPCA(R)	abcd	operator calling time (receive) signal
	N	if OPCA(R) not required

TIME	64-192 (128)	time of OPCA(R) pulse in milleseconds
REPT	(1)-5	number of OPCA(R) pulses
CONN(S)	abcd	connect send

—continued—

Table 3-1 (continued)
Data administration: Digital Interface and Clock Controller

Prompts	Responses	Comments
CONN(R)	abcd	connect received
P RRC(S)	abcd	register recall (send) signal, activated by Malicious Call Trace
	N	if RRC(S) not required
TIME	10-150 (100)	time of RRC(S) signal in milleseconds
P BURS(S)	abcd	bring up receiver (send), uses switch-hook flash timer for timer
	N	if BURS(S) not required
P BURS(R)	abcd	bring up receiver (receive), uses switch-hook flash timer for timer
	N	if BURS(R) not required
P CAS(S)	abcd	CAS Flash Time of flash is the same as for analog trunks. The signal can be configured but it will only be operational if the CASM package is equipped.
	N	if CAS(S) not required
CLRB(S)	abcd	clearback (send) signal
	N	if CLRB(S) not required (IDLE signal is used)
P RCTL(S)	abcd	release control (send) signal
	N	if RCTL(S) not required
P OPRS(R)	abcd	operator (receive) manual recall signal
	N	if OPRS(R) not required

TIME	min; 8-2040 (48) max; min-2040 (128)	minimum and maximum time range for OPRS(R) in milleseconds

—continued—

Table 3-1 (continued)
Data administration: Digital Interface and Clock Controller

Prompts	Responses	Comments
P NXFR(S)	abcd	network transfer signal (send) pulse. Pulse time not variable
	N	if NXFR(S) not required
P ESNW(S)	abcd	ESN wink signal (send) pulse. Pulse time not variable
	N	if ESNW(S) not required
P CAS(S)	abcd	Centralized Attendant signal (send) pulse. Pulse time not variable
	N	if CAS(S) not required
CLRF(R)	abcd	clear forward (receive)
	N	if CLRF(R) not required
SOSI	abcd, N	special operator signal defined (undefined). Prompted if OPRC = N.
Outgoing Calls		
SEZ(S)	abcd	seize voice or data from or to a non SL-1 switch
SEZD(S)	abcd	seize data (send) signal. Only recommended for SL-1 to SL-1 applications
	N	if SEZD(S) not required
SEZV(S)	abcd	seize voice (send) signal. Only recommended for SL-1 to SL-1 applications
	N	if SEZV(S) not required

—continued—

Table 3-1 (continued)
Data administration: Digital Interface and Clock Controller

Prompts	Responses	Comments
SEZA(R)	abcd	seize acknowledgement (receive) signal
	N	if SEZA(R) not required
P WNKS(R)	abcd	wink start pulsed seize acknowledgement (receive) signal
	N	if P WNKS(R) not required
TIME	20-500 (140), 20-500 (290)	length of WNKS(R) pulse in milleseconds (min, max). Prompted only if WNKS(R) is defined. Minimum and maximum pulse width (milleseconds)
P EOS(R)	abcd	end of selection (receive) signal
	N	if EOS(R) not required
TIME	64-192 (128)	length of EOS(R) pulse in milleseconds
CONN(S)	abcd	connect send
CONN(R)	abcd	connect receive
P OPRC(R)	abcd	operator recall signal for special services. Minimum three pulses, 160 milleseconds each
	N	in OPRC(R) not required
P BURS(S)	abcd	bring up receiver (send) for L1 networking
	N	if BURS(S) not required
P BURS(R)	abcd	bring up receiver (receive) for L1 networking

N	if BURS(R) not required

—continued—

Table 3-1 (continued)
Data administration: Digital Interface and Clock Controller

Prompts	Responses	Comments
P CAS(R)	abcd	CAS FLASH Timing of flash is same as for analog trunks. This signal can be configured, but it can only be operational if CASR package is equipped.
	N	if CAS(R) not required
TIME	64-192 (128)	length of BURS(R) pulse in milleseconds
CLRB(R)	abcd	clear back
	N	if CLRB(R) not required, when IDLE would be used
P RCTL(R)	abcd	release control
	N	if RCTL(R) not required
P NXFR(R)	abcd	network transfer
	N	if not required
P ESNW(R)	abcd	ESN wink signal
	N	if ESNW(R) not required
P CAS(R)	abcd	centralized attendant service signal
CLRF(S)	abcd	clear forward (send)
	N	if CLRF(S) not required
TIME	x, (0)	time; x = 0 is the only allowed value; default is 0; 0 = 800 milliseconds.

Note: Prompted only if the *abcd* bits entered in response to the CLFR(S) prompt are different from the *abcd* bits of the IDLE signal.

SOSO	abcd, (N)	special operator signal defined (undefined)

Note: Prompted if OPRC = N

—continued—

Table 3-1 (continued)
Data administration: Digital Interface and Clock Controller

Prompts	Responses	Comments
If FEAT = PAD, the following prompts are given.		
PDCA	1-16	pad category
	<CR>	print all the pad category tables
TNLS	YES, (NO)	for the PRT command will (not) print list of trunk TNs using requested pad category tables following table
DFLT	2-16	default pad category
	<CR>, 1	category 1 (CCITT) defaults

The following ten prompts and associated responses identify the pad codes (*x* for receive and *y* for transmit). The relationship between pad codes and pad values are as follows:

code	0	1	2	3	4	5	6	7
value (dB)	-1	-2	-3	+12	-6	+10	+0.6	+8
code	8	9	10	11	12	13	14	15
value (dB)	idle	+6	+5	+4	+3	+2	+1	0

Note 1: Positive dB represents loss and negative dB represents gain.

Note 2: Code 15, pad value 0, is equivalent to ‘no pad’. It is used for DTA (data only) and VOD (voice or data) call types.

Note 3: Code 8 – PCM signals are converted to silence.

Prompts	Responses	Comments
ONP	x y	on premises extension
	<CR>	initial values; x = 2, y = 5

—continued—

Table 3-1 (continued)
Data administration: Digital Interface and Clock Controller

Prompts	Responses	Comments
OPX	x y	of premises extension
	<CR>	initial values; x = 2, y = 15
DTT	x y	digital TIE trunks
	<CR>	initial values; x = 15, y = 15
DCO	x y	digital COT, FEX, WAT and DID trunks
	<CR>	initial values; x = 15, y = 15
NTC	x y	nontransmission compensated. Analog TIE
	<CR>	initial values; x = 11, y = 14
TRC	x y	transmission compensated. Analog TIE
	<CR>	initial values; x = 11, y = 14
DTR	x	pad values while DTR is connected (receive only).
	<CR>	initial value, x=2
VNL	x y	via net loss. Analog TIE
	<CR>	initial values; x = 11, y = 14

ACO	x y	analog COT and WATS trunks
	<CR>	initial values, x = 11, y = 14
AFX	x y	analog FEX trunks
	<CR>	initial values; x = 11, y = 14
ADD	x y	analog DID trunks
	<CR>	initial values; x = 11, y = 14

—continued—

Table 3-1 (continued)
Data administration: Digital Interface and Clock Controller

If FEAT = LPTI, the following prompts are given.

Prompts	Responses	Comments
LOOP	L	DTI loop number (must be defined in overlay program 17)
P DIGT(S)	abcd	(send) digit pulse timing from TDS. Bits P (pulsing) and X (fixed). Default id 'PXXX' for JDMI.
	N	if DIGT(S) signal not required
P METR(R)	abcd	metering (recv). Bits P (pulsing) or X (fixed). Only two P bits allowed. COT and DID trunks only. PPM package must be enabled. PPM metering is not allowed on the QPC785 JDMI.
	N	if METR(R) signal not required
EDGE	0, 1	0 = PPM bit counted when changed from 1 to 0. 1 = PPM bit counted when changed from 1 to 1
TIME	40-480 (240)	maximum time METR signal can be on in msec

SASU	0-8064 (1920)	seize acknowledge supervision period in msec Default is '4992' milleseconds for JDMI loops.
MFAO	YES, NO, <CR>	DTI card will or will not set bit 3 of timeslot 0 if loss of MFAS (multiframe alignment signal) occurs. The default (<CR>) means no change is required. Default is YES for JDMI loops.
SZNI	YES,(NO), (<CR>)	To allow (disallow) PSTN incoming seize during lockout and far-end fault states.
TGLR	YES, (NO), <CR>	Only prompted for JDMI loops. Toggle reserve bits in Frame 0, Timeslot 0.

—continued—

Table 3-1 (continued)
Data administration: Digital Interface and Clock Controller

The following prompts and associated responses define the grade of service timers for the DTI2 card.

Group I problems are treated individually. They are bipolar violations, bit error rate (frame alignment) problems and slips.

Group II problems are treated as a group. They are bit 3 of TS0 (far-end out of service), bit 6 of TS16 (far-end lost multiframe alignment), Alarm Indication Signal (AIS), loss of frame alignment and loss of multiframe alignment

Responses are interpreted as follows:

mt = maintenance threshold time.

ct = new call suppression (hardware service removal) threshold time.

ot = out of service threshold time.

dt = no new data calls suppression threshold time.

Each of the above response times are expressed as follows:

nnnnT – time in milleseconds where nnnn = 20-5000
(input to nearest 20 milleseconds)

nnnS – time in seconds where nnn = 1-240

nnnM – time in minutes where nnn = 1-240

nnH – time in hours where nn = 1-24

—continued—

Table 3-1 (continued)
Data administration: Digital Interface and Clock Controller

Prompts	Responses	Comments
BPV	nb mt dt ct ot	bipolar violations nb (max. count) = 1-255 default values are 205 10S 3S 3S 1S
FAP	nf mt dt ct ot	bit error rate (frame alignment) nf (max. count) = 1-255 default values are 32 4S 1S 1S 100T
SLP	ns mt dt ct ot	slips count ns (max. count) = 1-255 default values are 20 30S 10s 10S 6S If the loop is used for data applications more stringent values are recommended for SLP. eg 20 5H 2H 2H 6S
GP2	t2 mt dt ct ot	group II problems t2 (max. time) = 1-255 default values are 20 100S 12S 12S 4S

Note: each unit of 't2' = 128 milleseconds

If FEAT = SYTI, the following prompts are given.

Prompts	Responses	Comments
MAND	0-(15)-1440	maintenance guard time (minutes)
NCSD	0-(15)-1440	new call suppression guard time (minutes)
OSGD	0-(15)-1440	out of service guard time (minutes)
OOSC	0-(5)-127	out of service occurrences since midnight (DTI2 disabled)

PERS	0-(100)-254	persistence timer (in milleseconds) for far-end problems

—continued—

Table 3-1 (continued)
Data administration: Digital Interface and Clock Controller

Prompts	Responses	Comments
PREF CK0	LLL	primary reference for clock controller zero. LLL is the loop from which the clock controller will be deriving its primary clock pulses
	<CR>	primary reference remains at current setting
	X	primary reference reverts to the free-run mode
SREF CK0		secondary reference from clock controller zero. LLL is the loop from which the clock controller will be deriving its secondary clock pulses
	<CR>	secondary reference remains at current setting
	X	secondary reference reverts to the free-run mode
PREF CK1		primary reference for clock controller one. LLL is the loop from which the clock controller will be deriving its primary clock pulses
	<CR>	primary reference remains at current setting
	X	primary reference reverts to the free-run mode
SREF CK1		secondary reference for clock controller one. LLL is the loop from which the clock controller will be deriving its secondary clock pulses

<CR>	secondary reference remains at current setting

—continued—

Table 3-1 (continued)
Data administration: Digital Interface and Clock Controller

Prompts	Responses	Comments
	X	secondary reference reverts to the free-run mode.
		Note: The CC prompts will only appear for clocks which are valid for the machine type being configured. The prompts will only appear if the system is in a valid state for the definition of DTI CC data (i.e., the 1.5-Mb/s DTI clock references must be unused or in a free-run mode).
CCGD	0-(15)-1440	clock controller out of service guard time (minutes)
CCAR	0-(15)	clock controller audit rate. The time (in minutes) between normacc CC audits. Only programmable with DTI2 equipped.

Table 3-2
Default ABCD table with suggested values

Note: 'Undefined' is the equivalent of an N being entered for those signals which are optional.

Call type	Signal	Default Value	Suggested Value
IN/OUT CALLS	IDLE(S)	1001	
	IDLE(R)	1001	
	FALT(S)	1101	
	FALT(R)	1101	
INCOMING CALLS	SEZ(R)	0001	
	SEZD(R)	undefined	0011
	SEZV(R)	undefined	0010
	CALL(R)	undefined	XPXX
	SEZA(S)	1101	
	WNKS(S)	undefined	PXXX
	DIGT(R)	undefined	PXXX
	NRCV(S)	undefined	1001
	EOSF(S)	undefined	XPXX
	EOSB(S)	undefined	PXXX
	OPCA(R)	undefined	PXXX
	CONN(S)	0101	
	CONN(R)	0101	
	RRC(S)	undefined	PXXX
	BURS(S)	undefined	XXPX

	BURS(R)	undefined	XXPX

—continued—

Table 3-2 (continued)
Default table with suggested values

Call type	Signal	Default value	Suggested value
	CLRB(S)	1101	
	RCTL(S)	undefined	PXXX
	OPRS(R)	undefined	XPXX
	NXFR(S)	undefined	XPXX
	ESNW(S)	undefined	XPXX
	CAS(S)	undefined	XPPX
OUTGOING CALLS	SEZ(S)	0001	
	SEZD(S)	undefined	0011
	SEZV(S)	undefined	0010
	SEZA(R)		
	WNKS(R)	undefined	PXXX
	EOSB(R)	undefined	PXXX
	CONN(S)		
	CONN(R)		
	OPRC(R)	undefined	XXPX
	BURS(S)	undefined	XXPX
	BURS(R)	undefined	XXPX
	CLRB(R)		
	RCTL(R)	undefined	PXXX

NXFR(R)	undefined	XPXX
ESNW(R)	undefined	XPXX
CAS(R)	undefined	XPPX

Table 3-3
Data administration: DID Call Offering, Fault Signal, and Release

1. Response is required to the following prompts in Overlay Program 73:

Prompts	Responses	Comments
REQ	NEW, CHG	Create a new data block
TYPE	DTI2	2-Mb/s DTI
:		
:		
Incoming calls:		
P RCTL(S)	abcd	Release control (send) signal
	N	Not required
TIME	100 - (150) - 300	Time value for release control stored in multiples of 10 milleseconds.
P RCOD(S)	abcd	Release Control Originating Disconnect
	N	Not required
TIME	150	Time value in milleseconds
:		
Outgoing calls:		
P EOS(R)	abcd	End of selection (receive) signal
	N	Not required
TIME	64 - 320 - 64 (256) - 320	Time value range of EOS pulse in multiples of 8 milleseconds.

:

P RCTL(R)	abcd	Release control (receive) signal
	N	Not required

—continued—

Table 3-3 (continued)
Data administration: DID Call Offering, Fault Signal and Release

Prompts	Responses	Comments
TIME	96 - (128) - 320 96 - (256) - 320	Time value range for release control stored in multiples of 8 milleseconds.

Note: Only the TIME values have been changed

Note: RCTLs are prompted when the CLRB signal is defined the same as the IDLE signal, or is unused.

Note: RCOD is only prompted when RCTL is defined.

Acceptance test

This section describes the acceptance test procedure as well as the idle channel and remote link tests for the 2-Mb/s Digital Trunk Interface (DTI2) and Japan Digital Multiplex Interface (JDMI) feature. The test verifies the operation of the system hardware.

Chart 4-1
Acceptance test, Digital Interface

Step	Subtask	Procedure Number
1	Log into the overlay area.	553-2201-230, DP 3000
2	Load overlay program 60 (Digital Trunk Interface Diagnostic). Enter LD 60.	553-2301-511
3	Enter ENLL L to enable Interface (DTI2/JDMI) pack to loop L.	
4	Enter DISL L to disable Interface pack to loop L.	
5	Enter SLFT L to test Interface pack to loop L.	
6	If system response is other than OK, refer to 553-2911-510 to analyze message.	
7	Enter ENLL L to enable the Interface pack.	

8	Enter **** to abort overlay program 60.

Chart 4-2 gives the procedure for performing an idle channel confidence test on the DTI2/JDMI hardware when the Interface loop is enabled.

Chart 4-2
Idle Channel Test, Digital Interface

Step	Subtask	Procedure Number
1	Log into the overlay area.	553-2201-230, DP 3000
2	Load overlay program 60 (Digital Trunk Interface Diagnostic). Enter LD 60.	553-2301-511
3	Find an idle channel on the DTI2/JDMI loop by using the STAT command.	
4	If all 30 channels are indicated BUSY by the response of the STAT command, this test cannot be run. Otherwise, select an idle channel and disable it. Enter DSCH L C.	
5	Enter SLFT L C to execute the idle channel test on channel C of loop L.	
6	If the system response is other than OK, refer to 553-2911-510.	
7	Enter ENCH L C to enable DTI2/JDMI channel C.	
8	Enter **** to abort overlay 60.	

Chart 4-3 gives the procedure for performing a remote link diagnostic test on the Interface hardware when the loop is disabled. This procedure assumes that the testing is being run from a local to a colocated Interface.

Chart 4-3
Remote link test, Digital Interface

The test should be run on both the local and colocated Digital Interfaces.

Step	Subtask	Procedure Number
1	Log into the overlay area for both the local and colocated SL-1.	553-2201-230, DP 3000
2	Load overlay program 60 (Digital Trunk Interface Diagnostic). Enter LD 60.	553-2301-511
3	Enter DISL L1 to disable the DTI2/JDMI pack on the local SL-1 on loop L1. Enter DISL L2 to disable the Interface pack on the colocated SL-1 on loop L2.	
4	On the colocated SL-1, enter RLBK L2 to place this Interface in the remote loopback mode.	
5	On the local SL-1 enter RMST L1 to test the physical link between the local and the colocated Interfaces.	
6	the system response is other than OK, refer to 553-2911-510.	
7	On the colocated SL-1, enter DLBK L2 to disable the remote loopback mode.	

8 Enter NLL L1 to enable the pack on the local SL-1 on loop L1.

Enter ENLL L2 to enable the pack on the colocated SL-1 on lop L2.

9 Enter **** on both the local and colocated SL-1 to abort overlay.

QCAD281A cable information

Information to build QCAD281A cables of nonstandard lengths for Digital Interface applications is provided herein.

This cable (QCAD281A) is used to transport the 2-Mb/s digital signals from the circuit pack (QPC536 or QPC785) or the I/O assembly (located at the cabinet bulkhead) to the Network Channel Terminating Equipment (NCTE) interface. Its standard length is 50 ft (15.3 m).

Construction and connector information for the QCAD281A cable is as follows:

- Construction – individually foil shielded, twisted pairs, 24 AWG, stranded
- P1 Connector – 9-pin, female subminiature D, with jack-screws
- P2 Connector – 9-pin, male subminiature D, with jack-screws.

Refer to Table 4-1 for the QCAD281A cable wire list.

Table 4-1
QCAD281A cable wire list

X = Transmit

R = Receive

NC = No Connection

From	To	Signal (Note 2)	Colour
DTI2			
P1-1	NC	GRD Shield (Note 4)	
P1-2	P2-2	RTIP 75/120 Ω	RED
P1-3	P2-3	RRING 120 Ω	BLACK
P1-4	P2-4	RRING 75 Ω	BLUE
P1-5	P2-5 (Note 3)	GRD-SIGNAL	BLACK
P1-6	P2-6	XTIP 75/120 Ω	WHITE
P1-7	P2-7	XRING 120 Ω	BLACK
P1-8	P2-8	XRING 75 Ω	GREEN
P1-9	P2-9 (Note 3)	GRD-SIGNAL	BLACK
JDMI			
P1-1	NC	GRD Shield (Note 4)	
P1-2	P2-2	RRING 75/120 Ω	RED
P1-3	P2-3	RTIP 120 Ω	BLACK
P1-4	P2-4	NC	BLUE
P1-5	P2-5 (Note 3)	GRD-SIGNAL	BLACK
P1-6	P2-6	XTIP 110 Ω	WHITE
P1-7	P2-7	XRING 110 Ω	BLACK
P1-8	P2-8	NC	GREEN
P1-9	P2-9 (Note 3)	GRD-SIGNAL	BLACK

Note 1: Connections for QCAD282 and QCAD291 are the same as for

the QCAD281.

Note 2: For 75 ohms unbalanced signal, strap pin 4 to pin 5 and pin 8 to pin 9 and MDF.

Note 3: The signal ground on pins P2-5 and P2-9 must not be connected to frame ground at any point.

Note 4: In installations where the P2 connector is removed and the QCAD281 cable is wirewrapped, soldered, etc. directly to the MDF, the cable shields are to be connected to the frame (MDF ground). The shields are connected to the hood of the P2 connector on the QCAD282 and QCAD291 DTI2/JDMI-I/O panel cable used on EMI cabinets. This connects the shields to the frame ground through the P2 connector.

2-Mb/s Digital Trunk Interface

Installation

Standard
Group H
93 07 31
Printed in Canada