Meridian 1

Digital Clock Controllers

Installation and adminstration

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Introduction

During digital data transmission, all members of the communication network must transmit and receive at the same frequency to minimize data loss and error. To attain a satisfactory level of accuracy, Meridian 1 systems use Clock Controllers to synchronize operations.

This document discusses Clock Controllers, focusing on installation and replacement procedures. This introduction provides background information about the purpose and function of Clock Controllers for readers who may be unfamiliar with the devices.

Clock Controllers commonly work in conjunction with the Digital Trunk Interface (DTI) and Primary Rate Interface (PRI) cards. The dual-CPU systems (NT, XT, XN, options 61, 71, 81, and 81C) are shipped with two Clock Controllers (one Clock Controller for each CPU). Single CPUs also require a Clock Controller when DTI or PRI is configured.

Analog applications do not require a Clock Controller.

Defining the Clock Controller

Clock Controllers synchronize the system clock rate with the clock rates of digital switching and transmission equipment over a T1 circuit. Dual-CPU systems have two Clock Controllers: CC0 (associated with CPU 0) and CC1 (associated with CPU 1). One Clock Controller is the primary and the other is a backup.

The standard Meridian 1 Clock Controller is the **QPC471**, currently available in vintages C, D, E, F, G, and H. The option 81 and option 81C systems must use vintage H.

Customers outside the United States can use the **QPC775**. Vintage A of the QPC775 can be used with nonnetworked systems (systems linked directly to a central office); vintage B is appropriate for networked systems (Meridian 1 to Meridian 1 configurations). Customers with option 81 or option 81C systems must use QPC775 vintage C.

> *Note:* A system cannot use both the QPC471 and the QPC775. A system can mix Clock Controller vintages A through G. A vintage H Clock Controller can be used only with another vintage H Clock Controller.

Why networks use Clock Controllers

Both ends of a digital communication link must operate at the same data rate. If link synchronization is not established, data bit slips can occur resulting in a loss of data. Synchronized timing is essential for reliable digital data transfer.

Synchronization methods

When two Meridian 1 switches are connected to one another, one system can derive its timing from the other in a master/slave mode. In a larger network, the digital systems must use one of two synchronization methods:

— Nodal clocks can run independently at the same nominal frequency. Frequency differences among clocks result in frame slips, although the number and magnitude of slips can be minimized by using stable clocks and dynamic buffers that can absorb a limited number of data bits.

— Nodal clocks can be automatically locked to an external reference clock: the central office (CO) or another Meridian 1. This method is recommended; it eliminates frame slips if dynamic buffers are large enough to compensate for transmission variances.

Hierarchical synchronization

The primary timing reference in North America is based on a cesium beam atomic clock. The digital network in the United States, for example, is divided into two regions (one in St. Louis, the other in Boulder, Colorado), each with its own cesium atomic clock. Any DS-1 signal leaving these switches is synchronized to the cesium oscillators. Every digital node should be linked to one of the cesium atomic clocks.

In the North America digital network, a priority master/slave method is the basis for node synchronization. The telecommunications industry in the United States adheres to a four-level categorization: stratum 1, stratum 2, stratum 3, and stratum 4. The Canadian node category A is equivalent to the U.S. stratum 1 (the Canadian cesium clocks are located in Calgary and Ottawa); categories B and C are equivalent to stratum 2; category D is equivalent to stratum 3; and category E is equivalent to stratum 4.

— Stratum 1, the atomic standard, provides the highest level of accuracy.

— Stratum 2 clocks are typically used in large digital switching systems, such as a toll office.

— Stratum 3 clocks help synchronize CO and PBX operations. The Meridian 1 Clock Controllers adhere to this standard.

— Stratum 4 clocks are the least accurate.

Table 1 shows the parameters required for nodes that conform to each stratum.

Table 1
Node accuracy and parameters

	Stratum 2	Stratum 3	Stratum 4
Accuracy	+/– 1.6 * 10^{-8} Hz	+/– 4.6 * 10^{-6} Hz	+/– 3.2 * 10^{-5} Hz
Holdover	1 * 10^{-10} per day	<=255 frame slips in first 24 hours	Not required
Hardware duplication	Required	Required; nonduplicated clock hardware that meets other stratum 3 requirements is referred to as stratum 3ND.	Not required
MTIE during rearrangement	MTIE≤1 μsec Phase Change Slope: ≤81 ns in any 1.326 msec	MTIE≤1 μsec Phase Change Slope: ≤81 ns in any 1.326 msec	Not required; stratum 4 hardware that meets MTIE requirements during rearrangements is referred to as 4E
Pull-in range	3.2 * 10^{-8} Hz	9.2 * 10^{-6} Hz	6.4 * 10^{-5} Hz
Dedicated timing required	Required	Required	Not required

When the Meridian is used in a hierarchical digital network, each clock accepts synchronization from the external master clock designated as a higher-level source. The individual clocks help synchronize lower-level clocks. If the network connection fails, clocks receive synchronization signals from the highest available source.

Frame slip

A *frame slip* is the repetition or deletion of the 193 data bits of a DS-1 frame and results from a discrepancy between buffer read and write rates. When data bits write to the buffer faster than they are being read, the buffer overflows: this is a slip-frame deletion. When data bits are read faster than they are written, the buffer runs dry: this is a slip-frame repetition.

Slippage can affect data as follows:

— encrypted text: encryption key must be present

— video: freeze frame for several seconds; loud pop on audio

— digital data: deletion or repetition of data; possible misframe

— facsimile: deletion of 4–8 scan lines; drop call

— voice band data: transmission errors for 0.01 to 2 seconds; drop call

— voice: possible click

Determining network configuration

In a master/slave network, the master clock should be the highest stratum clock. If there is more than one clock at this level, the clock with the most connections to other clocks should be the master. If two or more clocks have the same number of connections, the most reliable clock should be the master.

The configuration should avoid timing loops, which occur when a clock uses a signal that can be traced to the output of that clock. Closed timing loops on the primary clock are not permitted as they lead to frequency instability. Timing loops are sometimes unavoidable on the secondary clock reference source.

All central office/system links used as clock references should be traceable to the same stratum 1 clock source.

The most common network configuration uses a master Clock Controller that synchronizes the other (slave) Clock Controllers. The master can link directly to all the slaves, or it can be associated with them in a hierarchical relationship. Figure 1 shows an example of a simple master/slave operation.

Figure 1
Master/slave relationship

PREF <CR>
SREF <CR>

loop x   loop x

PREF loop X
SREF <CR>

Master clock
(Source: free-run)

Slave
Clocks off Master
Tracks on loop X

553-5945
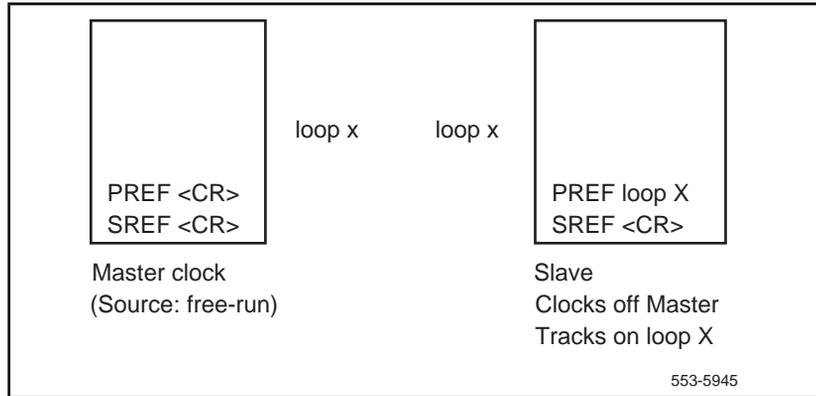
For tie lines between systems connected to a central office, the system, not the CO, establishes the clocking.

As Figure 2 shows, when a secondary digital loop is available, it can be used as a secondary clock source if the primary source fails.

Figure 2
Master/slave with a secondary clock source

M-1   M-1

LD73
PREF <CR>
SREF <CR>

loop x   loop x

loop y   loop y

LD73
PREF loop X
SREF loop Y

Master clock
(Source: free-run)

Slave
Clocks off Master
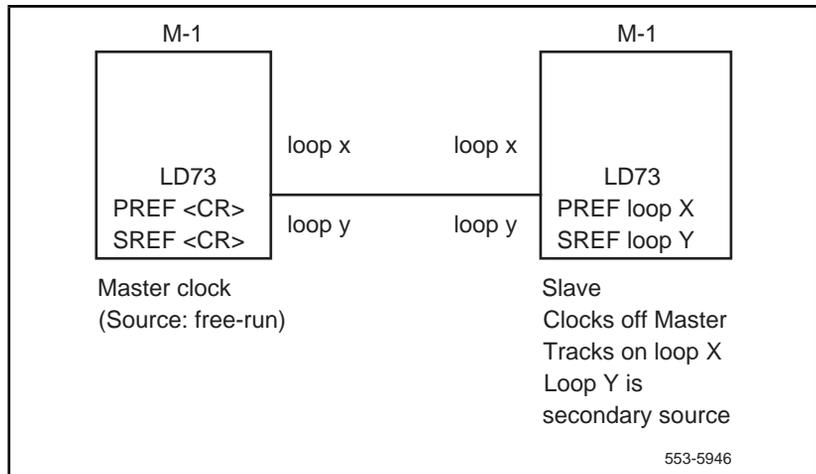Tracks on loop X
Loop Y is
secondary source

553-5946

Figure 3 shows a star arrangement: one hub system is linked to the central office. All other systems are connected as slaves. If a second system digital loop from the hub system is available, it can be used as a secondary clock source if the primary source fails.

Figure 3
Star clocking arrangement

553-5947
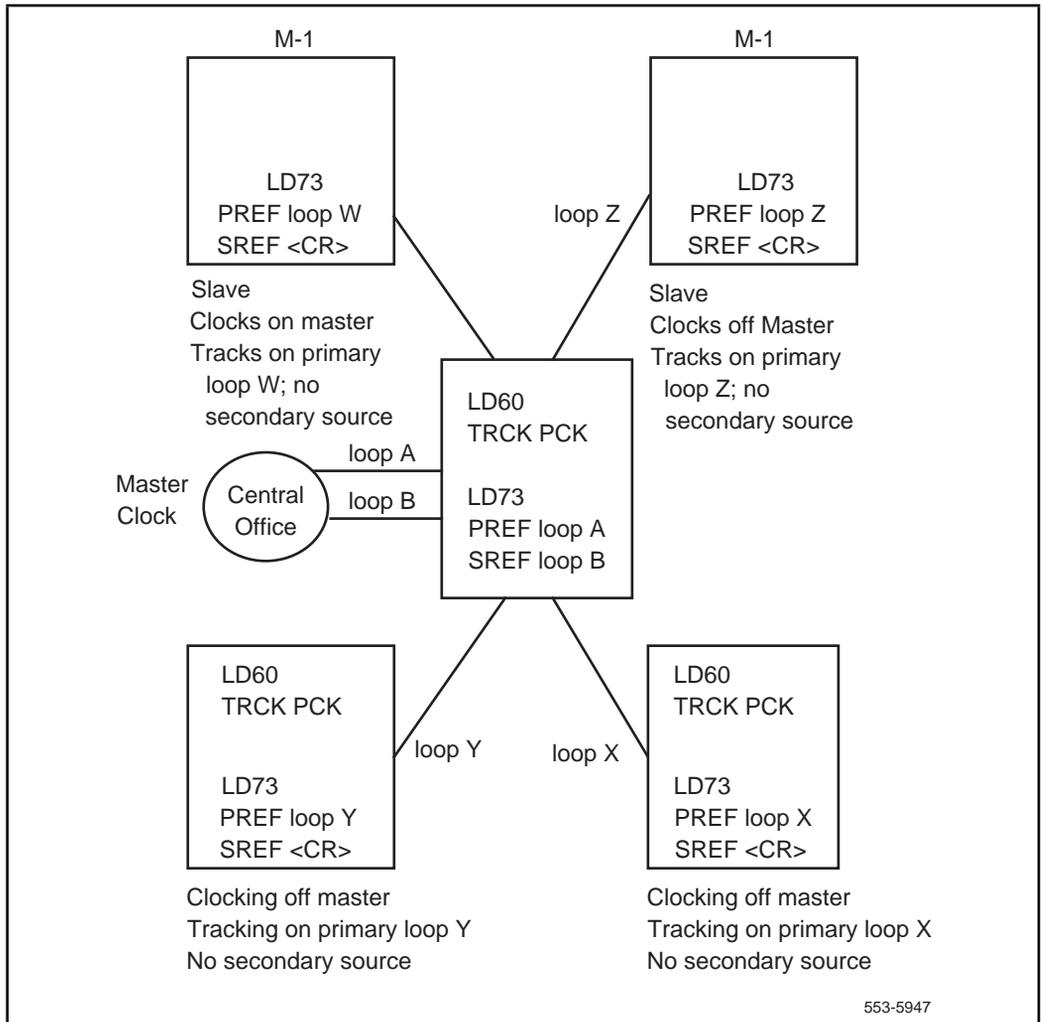
A small network can use a mutual synchronization structure, in which all members can receive synchronization signals from the others.

In another configuration, systems operate independently, each clocking off its own central office master clock. The systems use loops that interconnect them as secondary clocking sources. In this configuration, all central offices must have a path to the same stratum 1 source.

The previous figures indicate the LD 60 and LD 73 software commands required to set up the system. For more information, see "Clock Controller commands" on page 19.

Other documents

Refer to the following documents to learn more about the systems environment for Clock Controllers:

— *Digital Trunk Interface/Computer-to-PBX Interface installation and data administration* (553-2811-200)

— *ISDN Primary Rate Interface installation* (553-2901-200)

— *X11 input/output guide* (553-3001-400)

Clock Controller operation

This chapter describes basic principles of clock operation, with a discussion of operating modes, error handling, and recovery principles.

Clock operation

Vintages A through F have two types of clock operation: tracking mode and free run mode. Vintages G and H have three possible modes: tracking, free run, and holdover.

Tracking mode

LD 73 defines the digital loop (or loops) supplying an external clock reference to a Clock Controller. If two loops are defined, one is the primary reference source for clock synchronization, the other a secondary reference source that backs up the primary reference.

A dual-CPU system can have two Clock Controllers (CC0 and CC1), a primary and a backup. Each is completely locked to the reference clock as shown in Figure 4.

Free run (nontracking) mode

The clock synchronization for a digital loop can operate in free run mode if

— no loop is defined as a primary clock reference

— the primary and secondary references are disabled

— the primary and secondary references are in red (local) alarm

Holdover mode

Vintages G and H provide a holdover mode that retains references in case of system failure. Holdover mode remembers the last Clock Controller position and restores references upon system restart to maximize synchronization accuracy.

Reference clock errors

The Meridian 1 auditing software checks every 15 minutes to see if a Clock Controller or reference clock error has occurred. Reference clock errors typically result from problems with the clock driver or with the reference system clock at the far end.

In tracking mode, one active Clock Controller tracks a single reference clock. If a Clock Controller error is detected on dual-CPU systems, the system switches to the backup Clock Controller. Figure 4 illustrates the primary and secondary tracking functions.

Figure 4
Clock Controller primary and secondary tracking
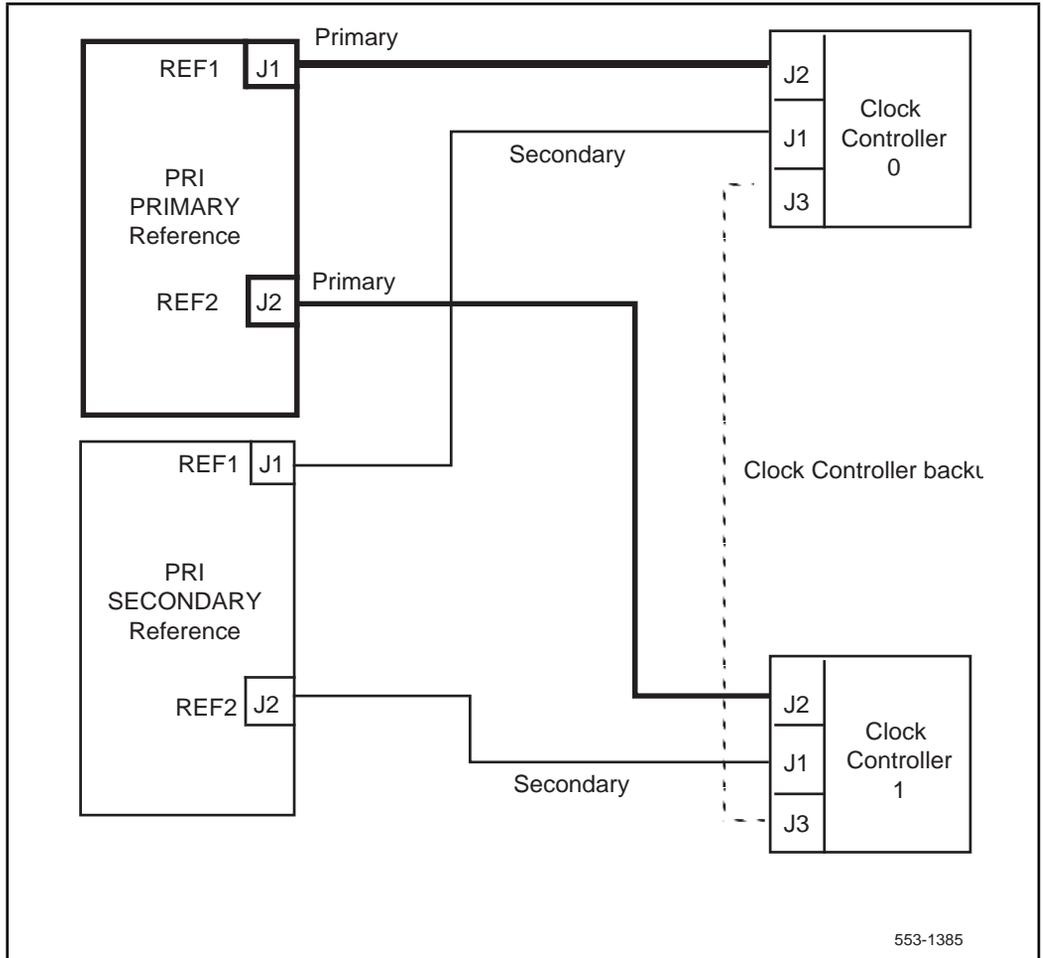
Automatic clock recovery

A red (local) alarm disables a loop. After loop recovery, the loop restarts and automatic clock recovery restarts the clocking devices.

— If the loop is assigned as the primary reference clock but the Clock Controller is tracking on the secondary reference or in free run mode, it is restored to tracking on primary.

— If the loop is assigned as the secondary reference clock but the Clock Controller is in free run mode, it is restored to tracking on secondary.

— If the 15-minute clock check indicates the system is in free run mode, the primary reference clock, if defined, resumes tracking.

— If the primary reference is disabled or in red (local) alarm, the secondary reference clock, if defined, assumes the tracking responsibilities.

A system deliberately set to free run resumes tracking on a reference clock at this time unless the clock-switching option has been disabled (LD 60, command MREF) or the reference clock is undefined in the database.

In X11 release 14, the EREF command in LD 60 enables the automatic recovery after LD 70 has been used to set AUTO=YES. With X11 release 15 and later, set AUTO=YES in LD 73; the EREF command is not required.

Automatic clock switching

Automatic changes in tracking may occur when clock recovery is enabled. Normally, the primary reference clock resumes tracking. If the assigned primary reference clock is not available, the secondary reference clock assumes tracking responsibilities. If the secondary reference clock cannot provide tracking, the system switches to free run.

Clock Controller installation

There are three steps to installing a Clock Controller:

1   Determine the location of the Clock Controller card (shelf and slot).

2   Set the switches on the card.

3   Insert the card and connect the cables. This step may also entail removing an old card.

This chapter describes this process.

CAUTION
Do not deviate from the procedures described in this section, as deviation stops call processing.

Determining slots and shelves

The Clock Controller card installation site varies from system to system. Table 2 shows the systems, the shelves used, and the available slot or slots.

Table 2
Clock Controller shelves and slots

System	Shelf	Slot(s)
ST, STE	CE	5–12
MS	CE	9
RT	network	13
N, NT	QSD39 network (LH) QSD40 network (RH)	13 2
XN	QSD17 CPU	14
XT	QSD62	15
21, 21E	NT8D11 CE/PE Module	4–5
51, 61	NT6D39 CPU/Net Module	9
51C, 61C	NT5D21 CPU/Net Module	9
71	NT8D34 CPU Module	14
81	NT6D60 Core Module	6
81C	NT8D35 Network Module QSD39 network QSD40 network	13 2 13

Before installing a Clock Controller, set the switches as shown in Tables 3 through 7. Tables 3, 4, and 5 display the settings for different vintages of the QPC471 Clock Controller card. Tables 6 and 7 show the settings for the QPC775 Clock Controller card.

Table 3
QPC471 vintage A switch settings

System	Switch	Setting
N, NT, RT	SW2	on
XN, XT	SW2	off
Vintage A applies only to these systems		

Table 4
QPC471 vintage B through G switch settings

Switch or Jumper	MS	ST, STE, 21A, 21	N, NT, RT, 51, 61	XN, XT, 71
SW1	on	on	on	off
SW2	on	off	off	off
Jumper F38	TP9-TP10	TP8-TP9	TP8-TP9	TP8-TP9
Jumper G38	TP12-TP13	TP11-TP12	TP11-TP12	TP11-TP12

Table 5
QPC471 vintage H switch settings

System	SW1				SW2				SW4			
	1	2	3	4	1	2	3	4	1	2	3	4
ST, STE, 21A, 21, 21E	on	on	on	on	off	off	off	off	off	off	off	off
MS, SN	on	on	on	on	on	on	on	on	off	off	off	off
RT, N, NT, 51, 51C, 61, 61C	on	on	on	on	off	off	off	off	off	on	*	*
XN, XT, 71, 81	off	off	off	off	off	off	off	off	off	on	*	*
81C	on	off	off	off	off	off	off	off	**	on	*	*
					Cable length between the J3 faceplate connectors:							
					0–4.3 m (0–14 ft)						off	off
					4.6–6.1 m (15–20 ft)						off	on
					6.4–10.1 m (21–33 ft)						on	off
					10.4–15.2 m (34–50 ft)						on	on

* If there is only one Clock Controller card in the system, set to OFF. If there are two Clock Controller cards, set to match the cable length between the J3 faceplate connectors. Determine the total cable length (no single cable can exceed 25 ft) between the J3 connectors. Both cards must have the same setting.

** Set to ON for clock controller 0. Set to OFF for clock controller 1.

Table 6
QPC775 switch settings

System	SW2				SW3				SW4			
	1	2	3	4	1	2	3	4	1	2	3	4
XN, XT, 71,81, 81C	off	off	off	off	off	off	off	off	on	on	on	on
N, NT, RT, ST, STE, 21A, 21, 21E, 51, 51C, 61, 61C	on	on	on	on	off	off	off	off	on	on	on	on
MS, SN	on	on	on	on	on	on	on	on	off	off	off	off

Table 7
QPC775 vintage E switch settings

System	SW2				SW3				SW4			
	1	**2**	**3**	**4**	**1**	**2**	**3**	**4**	**1**	**2**	**3**	**4**
ST, STE, 21A, 21, 21E	on	on	on	on	off	off	off	off	off	off	off	off
MS	on	on	on	on	on	on	on	on	off	off	off	off
RT, N, NT, 51, 51C, 61, 61C	on	on	on	on	off	off	off	off	off	on	*	*
XN, XT, 71, 81	off	off	off	off	off	off	off	off	off	on	*	*
81C	on	off	off	off	off	off	off	off	**	on	*	*
					Cable length between the J3 faceplate connectors:							
					0–4.3 m (0–14 ft)						off	off
					4.6–6.1 m (15–20 ft)						off	on
					6.4–10.1 m (21–33 ft)						on	off
					10.4–15.2 m (34–50 ft)						on	on

* If there is only one Clock Controller card in the system, set to OFF. If there are two Clock Controller cards, set to match the cable length between the J3 faceplate connectors. Determine the total cable length (no single cable can exceed 25 ft) between the J3 connectors. Both cards must have the same setting.

** Set to ON for clock controller 0. Set to OFF for clock controller 1.

Replacing a Clock Controller

See step 2 in the Procedure 1, 2, and 3 for instructions on how to replace a Clock Controller card.

Do not disable an active clock or a clock associated with an active CPU.

Installing a Clock Controller

Be sure to inspect the Clock Controller card before installing it. Refer to the tables at the beginning of this chapter for shelf, slot, and switch setting information. Remember, do not use both the QPC471 and the QPC775 on a single system. QPC471 vintage H cards cannot be mixed with cards of an earlier vintage.

Starting the Clock Controller

The Clock Controller, when first enabled, is in free run mode. It stays in this mode for several minutes before being switched to tracking mode. Manual intervention is possible if the capability has been set in LD 60.

For the earlier QPC471 vintages, up to 20 minutes may pass before the clock locks and tracks. The QPC471 vintage G and H cards begin tracking within 5 minutes.

Clock Controller commands

During the installation procedure, you will use some of the Clock Controller commands available in LD 60. In the following list of commands, "x" refers to the Clock Controller number: 0 for the card associated with CPU0, 1 for the card associated with CPU1.

— DIS CC x: disable system Clock Controller x

— DSCK loop: disable clock for specified loop

— DSYL loop: disable yellow alarm processing for specified loop

— ENCK loop: enable clock for specified loop

— ENL CC x: enable system Clock Controller x

— ENYL loop: enable yellow alarm processing for specified loop

— EREF: enable automatic switchover of system clocks

— SSCK x: obtain status of system clock x

— SWCK: switch system clock between active and standby

— TRCK aaa: set Clock Controller track where aaa can be PCK (the primary DTI/PRI reference), SCLK (the secondary DTI/PRI reference) or FRUN (free running)

Procedure 1
Installing the Clock Controller in the ST, STE, 21, 21E, MS, N, RT, 51, and NT half group

> *Note:* Refer to the tables in this chapter to be sure you are using the correct vintage.

1   Set the ENL/DIS toggle switch to DIS (disable) on the new circuit card.

2   If replacing an existing card, follow these steps:

— Perform a status check on the clock with the SSCK command in LD 60. The new controller should have the same status.

— Disable the old card using LD 60.

> *Note:* ERR20 messages may be generated. These can usually be ignored. However, excessive clock switching should be avoided, especially when counters are near the maintenance or out-of-service thresholds. Excessive switching could generate threshold-exceeded messages or cause the PRI to be automatically disabled. Check the counters in LD 60. If necessary, reset the counters using the RCNT command.

— Set the old card's faceplate ENL/DIS switch to DIS.

— Disconnect cables from the old Clock Controller card and remove the card from the shelf.

> *Note:* The Clock Controller status display in this mode indicates NO UART (no universal asynchronous receiver transmitter). Do not perform a clock status check when receiving this code.

3   Install the new Clock Controller in the selected slot.

4   Connect the cables to the new card.

— Connect the primary reference to J2.

— If applicable, connect the secondary reference to J1.

5   Set the faceplate ENL/DIS switch to ENL (enable).

6 Set the error detection thresholds and clock synchronization control in LD 73. (This step is optional if replacing a pack but required with a new installation.)

7 Enable the Clock Controller by entering ENL CCx in LD 60.

8 To track on a primary or secondary reference clock, use LD 60. The command is

TRCK PCK (for primary)
SCLK (for secondary)
FRUN (for free run)

9 Issue the SSCK command to check controller status.

Installing the Clock Controller in a single group

Procedure 2
Installing the Clock Controller in the NT and 61

1   Set the faceplate ENL/DIS switch to DIS (disable) on the new circuit card.

2   If replacing an existing card, follow these steps:

—   Perform a status check on the clock with the SSCK command. The new card should have the same status.

—   Disable the old card using LD 60. Use software to disable a card only if the card is associated with a standby CPU and is in standby state.

Note: ERR20 messages may be generated. These can usually be ignored. However, excessive clock switching should be avoided, especially when counters are near the maintenance or out-of-service thresholds. Excessive switching could generate threshold-exceeded messages or cause the PRI to be automatically disabled. Check the counters in LD 60. If necessary, reset the counters using the RCNT command.

—   Set the old card's faceplate ENL/DIS switch to DIS.

—   Disconnect the cables from the old Clock Controller card and remove the card from the shelf.

Note: The Clock Controller status display in this mode indicates NO UART (no universal asynchronous receiver transmitter). Do not perform a clock status check when receiving this code.

3   If the 3PE switches have not been modified to recognize the Clock Controller card, adjust them as follows:

QSD39 (left-hand side)
    SW1 OFF (OPT 61 shelf 0)
    SW2 ON
    SW4 OFF

QSD40 (right-hand side)
    SW1 OFF (OPT 61 shelf 1)
    SW2 ON
    SW4 OFF
    SW8 OFF

4   Set the faceplate ENL/DIS switch to DISABLE.

5   Install the Clock Controller in the selected slot.

6   Run and connect the cables.

     — Connect the primary reference to J2.

     — If available, connect the secondary reference to J1.

     — Connect the cable between the two clocks to J3 on each controller card.

7   Set the faceplate ENL/DIS switch to ENL.

8   Enable the Clock Controller by entering ENL CC x in LD 60.

9   Set the error detection thresholds and clock synchronization controls in LD 73. (This step is optional in a replacement but required in a new installation.)

10   To track on a primary or secondary reference clock, use LD 60. The command is

     TRCK   PCK   (for primary)

                 SCLK   (for secondary)

                  FRUN   (for free run)

11   Issue the status check command, SSCK.

12   Activate the new Clock Controller with the LD 60 SWCK command.

13   Repeat, if necessary, for the second Clock Controller.

Procedure 3
Installing the Clock Controller in the XN, XT, 71, 81, and 81C

Note: The option 81 and option 81C systems require a QPC471 vintage H Clock Controller card or a QPC775 vintage E Clock Controller card.

1 Set the faceplate ENL/DIS switch to DIS on the new circuit card.

2 If replacing an existing card, follow these steps:

— Perform a status check on the clock with the SSCK command. The new card should have the same status.

— Disable it using LD 60. Use software to disable a card only if the card is associated with a standby CPU and is in standby state.

Note: ERR20 messages may be generated. These can usually be ignored. However, excessive clock switching should be avoided, especially when counters are near the maintenance or out-of-service thresholds. Excessive switching could generate threshold-exceeded messages or cause the PRI to be automatically disabled. Check the counters in LD 60. If necessary, reset the counters using the RCNT command.

— Set the old card's faceplate ENL/DIS switch to DIS.

— Disconnect the cables from the old Clock Controller card and remove the card from the shelf.

Note: The Clock Controller status display in this mode indicates NO UART (no universal asynchronous receiver transmitter). Do not perform a clock status check when receiving this code.

3 Set the faceplate ENL/DIS switch to DIS.

4 Verify the switch settings on the Clock Controller card. See Table 5, "QPC471 vintage H switch settings," on page 16 or Table 7, "QPC775 vintage E switch settings," on page 17 for a list of Clock Controller switch settings.

5 Install the Clock Controller in the selected slot. The slot locations varies from system to system. For a list of clock controller slot locations, refer to "Determining slots and shelves" on page 14.

6   Run and connect the cables.

— Connect the primary reference to J2.

— If available, connect the secondary reference to J1.

— Connect the cable between the two clocks to J3 on each controller card.

7   Set the faceplate ENL/DIS switch to ENL.

8   Enable the Clock Controller by entering ENL CC x in LD 60.

9   Set the error detection thresholds and clock synchronization controls in LD 73. (This step is optional in a replacement but required with a new installation.)

10   To track on a primary or secondary reference clock, use LD 60. The command is

    TRCK   PCK   (for primary)
           SCLK   (for secondary)
           FRUN   (for free run)

11   Issue the status check command, SSCK.

12   Activate the newly installed Clock Controller with the LD 60 SWCK command.

13   Repeat, if necessary, for the second Clock Controller.

Cabling requirements

Clock Controllers can require three different kinds of cable connections:

— In a single-controller system, cable QCAD130 or NT8D79xx connects QPC720/QPC472 (PRI or DTI card) to QPC471/QPC775 at J2 when DTI/PRI is the primary reference clock source.

— In a single-controller system, cable QCAD130 or NT8D79xx connects QPC720/QPC472 to QPC471/QPC775 at J1 when DTI/PRI is the secondary reference clock source.

— With dual controllers, cable QCAD125 or NT8D75xx connects the Clock Controller cards to each other at J3 in single- group mode.

NT8D74 Clock Controller to InterGroup cable

This cable connects the QPC471 or QPC775 Clock Controller card to the NT8D36 InterGroup Module.

This cable is available in the following lengths:

— NT8D74AC   1.2 m (4 ft)
— NT8D74AD   1.8 m (6 ft)
— NT8D74AE   2.4 m (8 ft)
— NT8D74AF   3 m (10 ft) (QCAD110B)
— NT8D74AJ   4.8 m (16 ft)

NT8D75 Clock Controller to Clock Controller cable

This cable connects QPC471 Clock Controller cards to each other.

This cable is available in the following lengths:

— NT8D75AC   1.2 m (4 ft)
— NT8D75AD   1.8 m (6 ft)
— QCAD125   3 m (10 ft)

NT8D79 PRI/DTI to Clock Controller cable

This cable connects the PRI/DTI card to the QPC471 Clock Controller card.

This cable is available in the following lengths:

— NT8D79AB   0.6 m (2 ft)
— NT8D79AC   1.2 m (4 ft)
— NT8D79AD   1.8 m (6 ft)
— NT8D79AE   2.4 m (8 ft)
— NT8D79AF   3 m (10 ft) (QCAD130)

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