INPUT/OUTPUT AND AUXILIARY INTERFACE CIRCUITS
MAINTENANCE SUPPORT INFORMATION
"DIMENSION®" "PRELUDE*" PBX

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1. GENERAL

1.01 This section covers the processor interface with input and output (I/O) and auxiliary circuits. The circuits provide functions that relate to and support call processing via the DIMENSION PRELUDE PBX network.

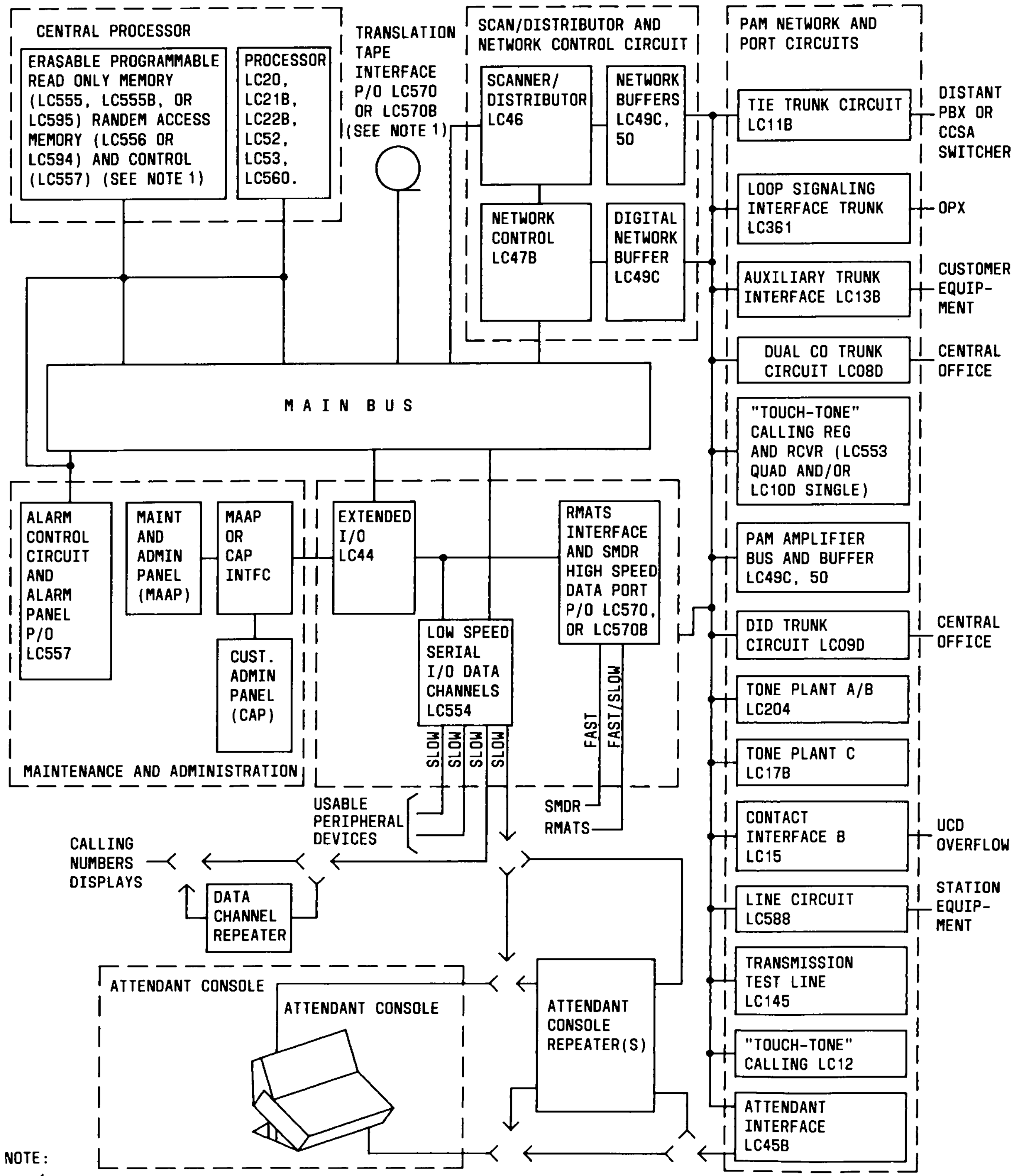
1.02 Whenever this section is reissued, the reason(s) for reissue will be listed in this paragraph.

1.03 The auxiliary circuits involved are shown in relation to the overall PBX systems in Fig. 1. The circuits provide interface, control, and buffering for the following functions and/or peripheral units:

- I/O buffer
- Maintenance and Administration Panel (MAAP) and Customer Administration Panel (CAP)
- Remote Maintenance, Administration, and Traffic System (RMATS)
- Data channels for attendant consoles, display units, Station Message Detail Recording (SMDR), and traffic monitoring circuits
- Data channel repeaters
- Attendant console repeaters
- Peripheral Interface Circuit (PIC).

1.04 The following functional maintenance support information is covered in this section:

- General interface operation of peripheral devices
- General message structure
- General message decoding
- Read/write data channel commands
- The MAAP functions
- Data channel and attendant console repeaters



NOTE:

1. THE LC555, LC556, AND LC570 IN MODEL A AND B SYSTEMS CAN BE REPLACED BY THE LC595 OR LC555B, LC594, AND LC570B, RESPECTIVELY, IN MODEL C THROUGH J SYSTEMS.

Fig. 1—DIMENSION PRELUDE PBX—Block Diagram

- Alarm message decoding
- Response of peripheral devices to processor commands via the data channels
- Maintenance considerations.

1.05 Subsystem peripherals such as SMDR and RMATS are covered in separate Bell System Practices (BSPs). This section describes the data channel to all devices, including the operations of particular devices which are not subsystems (MAAP, CAP, and display units). The devices covered are shown by heavy lines in Fig. 2.

1.06 This section is based on the drawings listed in Part 10. If this section is to be used with equipment or apparatus reflecting later issue(s) of the drawing(s), reference should be made to the SDs and CDs to determine the extent of the changes and the manner in which the section may be affected.

2. GENERAL INTERFACE OPERATION OF PERIPHERAL DEVICES

2.01 Peripheral devices consist of data links, displays, MAAPs, CAP, PIC, and a data control interface for SMDR and RMATS subsystems.

DATA LINKS

2.02 The data link provides a 4-wire interface or a 5-wire interface between the I/O buffer and peripheral devices (Fig. 2). The 4-wire data link is used as a standard data channel, and the 5-wire data link is used as a special data channel. Both data link circuits (LC554 or LC570B) receive parallel data from the data bus and convert the information to serial form. The 4-wire interface transmits pulses (Fig. 3) over a pair of wires to the peripheral circuit and receives serial data over another pair. The 5-wire interface uses the Electronic Industries Association (EIA) RS-232C format to transmit serial data over one lead and to receive serial data over another lead. Received data is stored in a register and upon command from the processor is parallel gated to the data bus. A software option, available with the LC570B, permits operation at preselected speeds.

A. Standard Data Link (LC554)

2.03 The standard data link (LC554) provides four channels operating in the slow mode (185 kilobits per second). These channels provide interface between the PBX and the following peripheral equipment operating at this speed.

(a) The ***attendant console*** responds to the serial pulses received over the slow-mode data link (185 kilobits per second) by turning lamps and ringers on or off for displaying operational information to the operator. The received pulses are converted to standard logic levels and shifted into an input register. When the complete message has been received, the data is parallel-gated into decoders which determine the action required of a valid message. As each bit is shifted into the console input register, a bit is transmitted to the processor. The bit can be either a repeat of the received bit or part of the address of an operated button.

(b) The ***PIC*** (Fig. 4) converts data from the PBX to the EIA standard RS-232C format and converts data from the peripheral unit to data acceptable by the PBX. The PIC functions as the interface for long-distance billing, as the communications interface for property management systems, and provides for connection of journal printers and energy communications control terminal to the DIMENSION PRELUDE PBX.

(c) The calling number ***display units*** respond to serial data via the 4-wire data link by displaying the extension number of the calling PBX party.

B. Special Data Link (LC570B)

2.04 The special data link provides an EIA RS-232C interface at a software selectable operating rate. The data link also provides a standard high-speed interface between the PBX and the following subsystems.

(a) The ***SMDR*** is a feature that provides a record of various types of incoming and outgoing calls processed by the associated PBX. The SMDR equipment responds to serial data from the processor via the 4-wire data link operating in the fast-speed mode (833 kilobits per second). Each received bit is converted to standard logic levels, serial-shifted into a storage register, converted into a parallel format, and entered into memory. The call-data information can be read from memory and converted to serial format to drive a paper printer or a tape punch for the direct output ver-

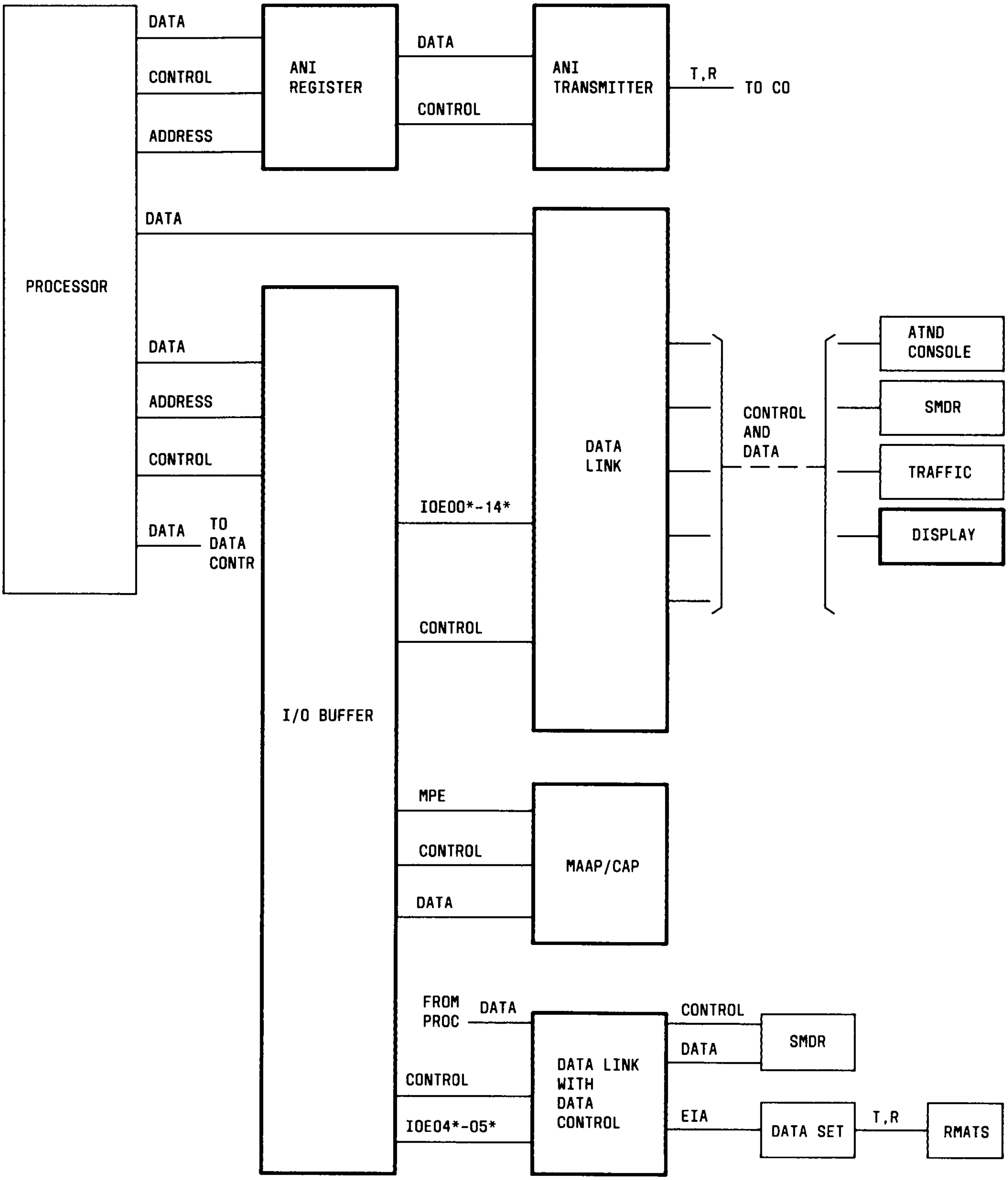
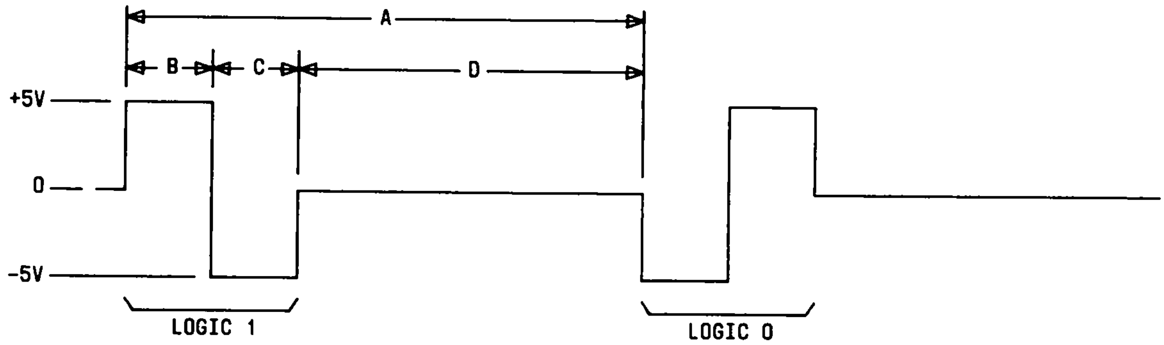


Fig. 2—I/O and Auxiliary Circuits



DATA SPEED OPTION	RATE	RATE INTERVAL (A)	FIRST BIPOLAR PULSE (B)	SECOND BIPOLAR PULSE (C)	SETTLING INTERVAL (D)
SLOW	185.1852 KHZ	5.4μS	.9μS	.9μS	3.6μS
FAST	833.3333 KHZ	1.2μS	.2μS	.2μS	.8μS

Fig. 3—Serial Data Format—Timing Diagram

sion, or the call-data information can be read from memory and recorded on a 9-track magnetic tape in binary-coded decimal format. For each bit of data received via the data link, an echo bit is transmitted to the processor for error checking. This data channel also provides an interface to the Centralized Message Detail Recording (CMDR) system that collects data from remote customer-premises locations and provides the data at a central location. The Network Control Office Support System—Local Storage Unit (NCOSS—LSU) also provides an interface by a data channel. The NCOSS provides detailed call records for use by operating company personnel at a network control office that may be used for traffic studies.

(b) The ***RMATS*** provides remote access to the logic and memory of DIMENSION PRELUDE PBX systems from a central facility. This allows maintenance, administrative, and traffic routines to be performed from a remote location. The RMATS access to the DIMENSION PRELUDE PBX is via a dial-up data link, using EIA interface and operating at a rate of 300 baud. Access provides the capability to administer and change nearly all customer services, features, and restrictions from a remote operation center.

(c) The Braemar tape unit provides high density storage for system translations. In case of power failure that exceeds the system power reserve, system translations can be restored from the tape. The tape unit responds to a data link equipped with an EIA interface, operating at 9600 baud, and can be activated via RMATS.

(d) The ***traffic measurements*** may be made using various devices which are interfaced by the 4-wire data link operating in the fast-speed mode (833 kilobits per second). The traffic measurement data is accumulated on-line and, when requested from some external device, the stored data will be transmitted for remote processing.

C. Input/Output (I/O) Data Buffer

2.05 The I/O data buffer provides the interface between the data links, the following subsystems, and the main data bus:

(a) The ***MAAP circuit*** displays digital information for maintenance and administrative operations. The circuit detects and stores control button operations, and on command, transmits the information to the processor. The control button

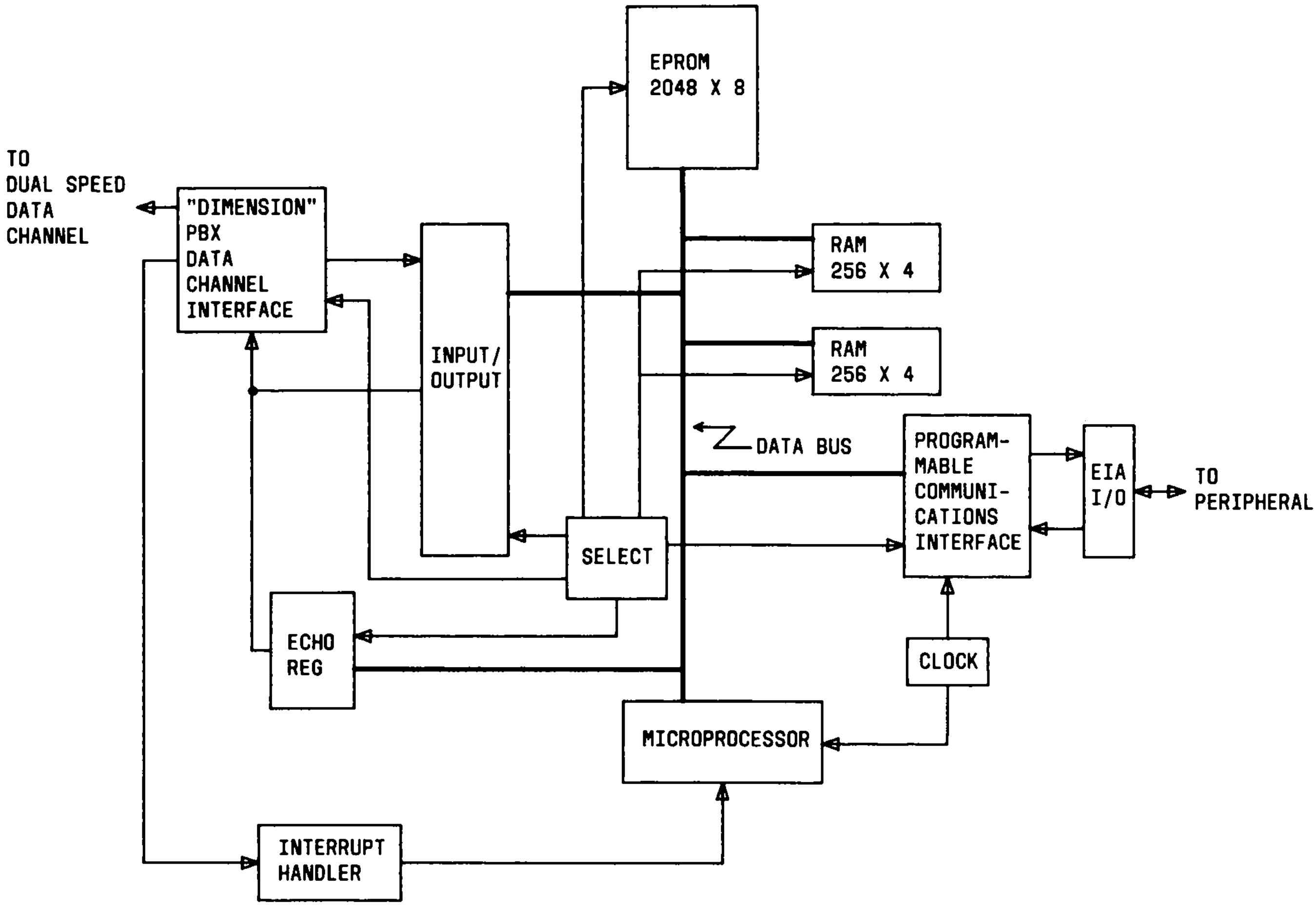


Fig. 4—Peripheral Interface Circuit—Functional Block Diagram

operations provide the means for craft personnel to interrogate the system status and to make changes in and test the system. Certain status information is also displayed on software and/or hardware-controlled light-emitting diodes (LEDs). The connecting interface directs parallel data via an 11-bit I/O data bus to the MAAP. A MAAP response to a received message is gated to the processor via the same parallel bus.

(b) The ***CAP*** is an adaptation of the MAAP. The CAP provides customer access to DIMENSION PRELUDE PBX systems for the purpose of performing administration of station features, ie, station rearrangement and change, facilities administration and control, and traffic data. The CAP circuit displays information for the administrative operations. The circuit detects and stores control button depressions, and on command, transmits the information to the processor. The received data is decoded and displayed by LEDs. The CAP transmits a response word simultaneously to any input word on a bit-for-bit basis. When the input word is a read command, the output word contains the address of a depressed button. If a button has not been depressed, or when any write command is received, the output word is an echo of the input word.

3. GENERAL MESSAGE STRUCTURE

3.01 The processor changes information with the various auxiliary or peripheral devices over the main buses either directly or via the I/O buffer and the data link (Fig. 2). The buses include a 16-bit unidirectional address bus, a 17-bit bidirectional data bus, and a 3-bit control bus.

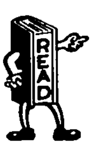
3.02 The information on the address bus selects the circuit to be affected. The information on the data bus defines the required action, and the information on the control bus determines the function to be performed.

3.03 The processor sends messages to scan or interrogate for status changes, distributes orders, provides data, and/or tests associated PBX components. Each message word contains 17 bits of data which may include an operation code (opcode) field, an address field, a data field, and a parity bit (Fig. 5). The specific message format is determined by the connected device. Some may require only a single message field, while others require a combination of fields. When included, the opcode field identifies the functions to be performed, the address field identifies the desired circuit within the peripheral, and the data field defines the required action. The parity bit is used to check the validity of the message.

4. MESSAGE DECODING

4.01 Communications between the processor and the peripheral circuits are initiated primarily to determine the status of the circuits and/or to change the existing states.

4.02 Information distributed from the processor on the main data bus is paralleled to nearly all of the I/O auxiliary or peripheral devices. The devices ignore this information unless enabled by the processor via the address and control buses. The address of the device must be present on the address bus, and a read or write command must be on the control bus.



Signal designations shown with an asterisk (eg, STMD*) indicate that the normal logic level is high (1) and the primary functions of the lead are performed in the low (0) logic state. Lead designations without an asterisk (MA00) indicate that the logic level is normally low (0) and the primary functions of the lead are performed in the high (1) logic state.

EXTENDED I/O BUFFER

4.03 The extended I/O buffer provides signal buffering between the processor and the data link channels and the MAAP/CAP interface unit. The I/O buffer (Fig. 6) decodes the information on the main address and control buses to enable the data channels and the MAAP/CAP interface unit. The circuit buffers the main data bus inputs to prevent overloading of leads when extended to the MAAP/CAP interface unit.

> *Note:* The MAAP or CAP access to the PBX is on a first-come-first-served basis. Whenever the CAP is in use, the on-off switch on the CAP disables the gating path to the MAAP.

4.04 The I/O buffer receives all address information from the processor on eight of the main address leads (MA04* through MA10* and MA15*). The information is parallel-loaded into the I/O address decoder, decoded, and an enabling signal (MPE* or IOE_ _*) is generated and directed to the selected circuit.

4.05 In addition to the enabling lead, each peripheral device must also receive an active read or write command signal before responding to information on the data bus. The read (RDIO*) and write (WRIO*) commands are received by the I/O buffer via the main control bus. The command is decoded by the I/O read/write control circuit which is enabled by one of the following signals from the address decoder:

(a) MP*—for an address directed to the MAAP/CAP circuit

(b) RWE—for an address directed to a data link.

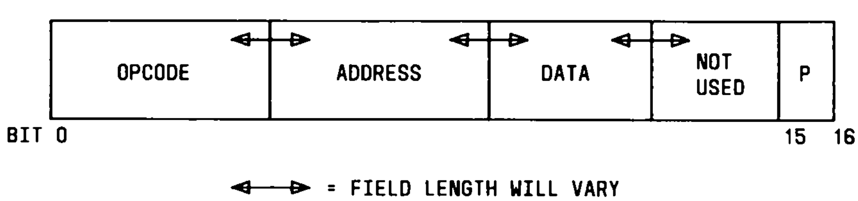


Fig. 5—Processor Message Format

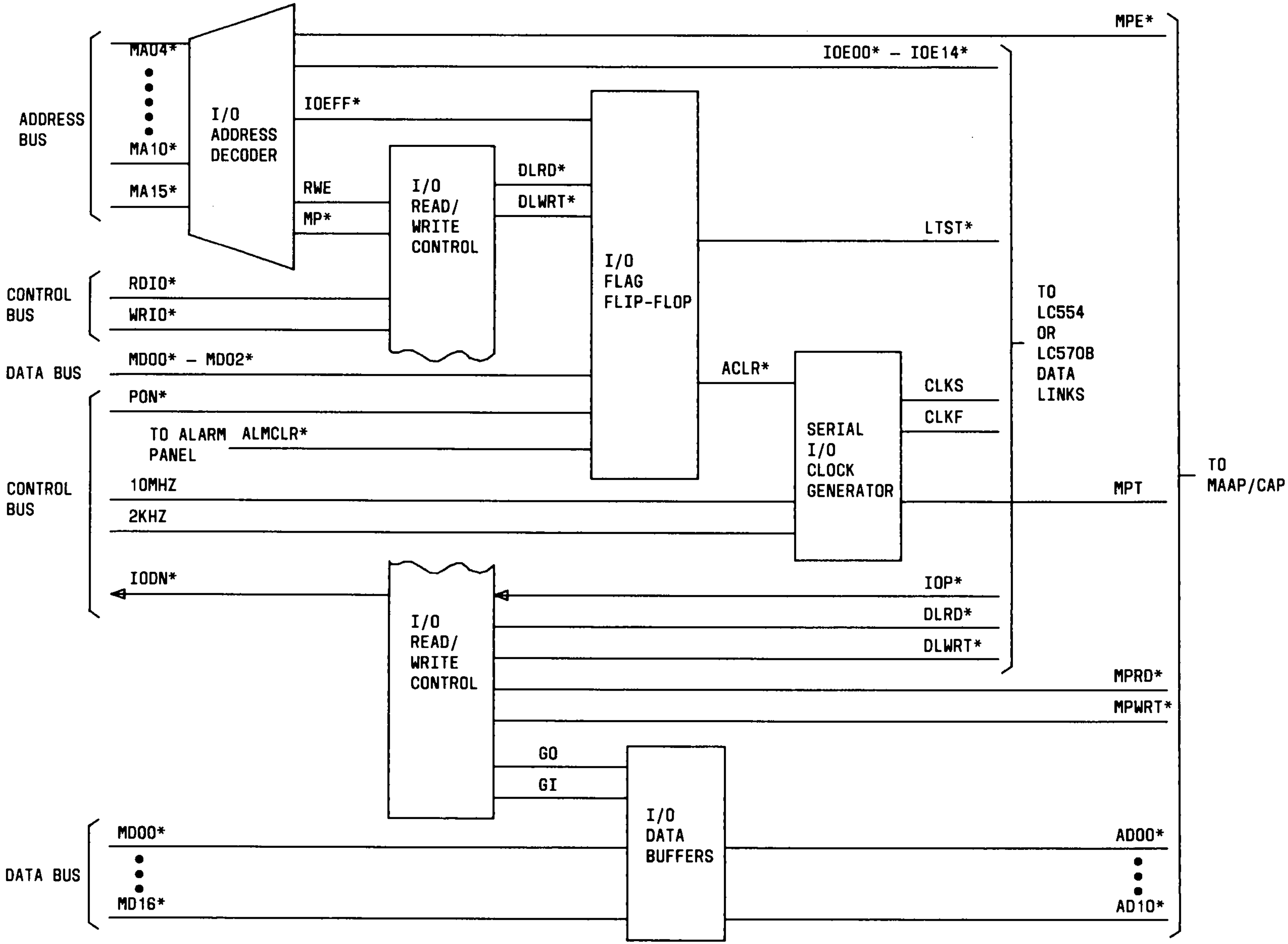


Fig. 6—Extended I/O Buffer (LC44)—Read and Write Commands

4.06 Table A lists the address bus inputs, the enabling lead, the associated I/O circuit and channel for all devices which may be decoded by the I/O buffer.

A. Decoding Messages to the Maintenance and Administration Panel/Customer Administration Panel (MAAP/CAP)

4.07 When a valid MAAP/CAP address and a read or write command have been decoded, the MAAP/CAP enable (MPE*), read (MPRD*), and write (MPWRT*) signals are generated to enable the MAAP/CAP (Fig. 7).

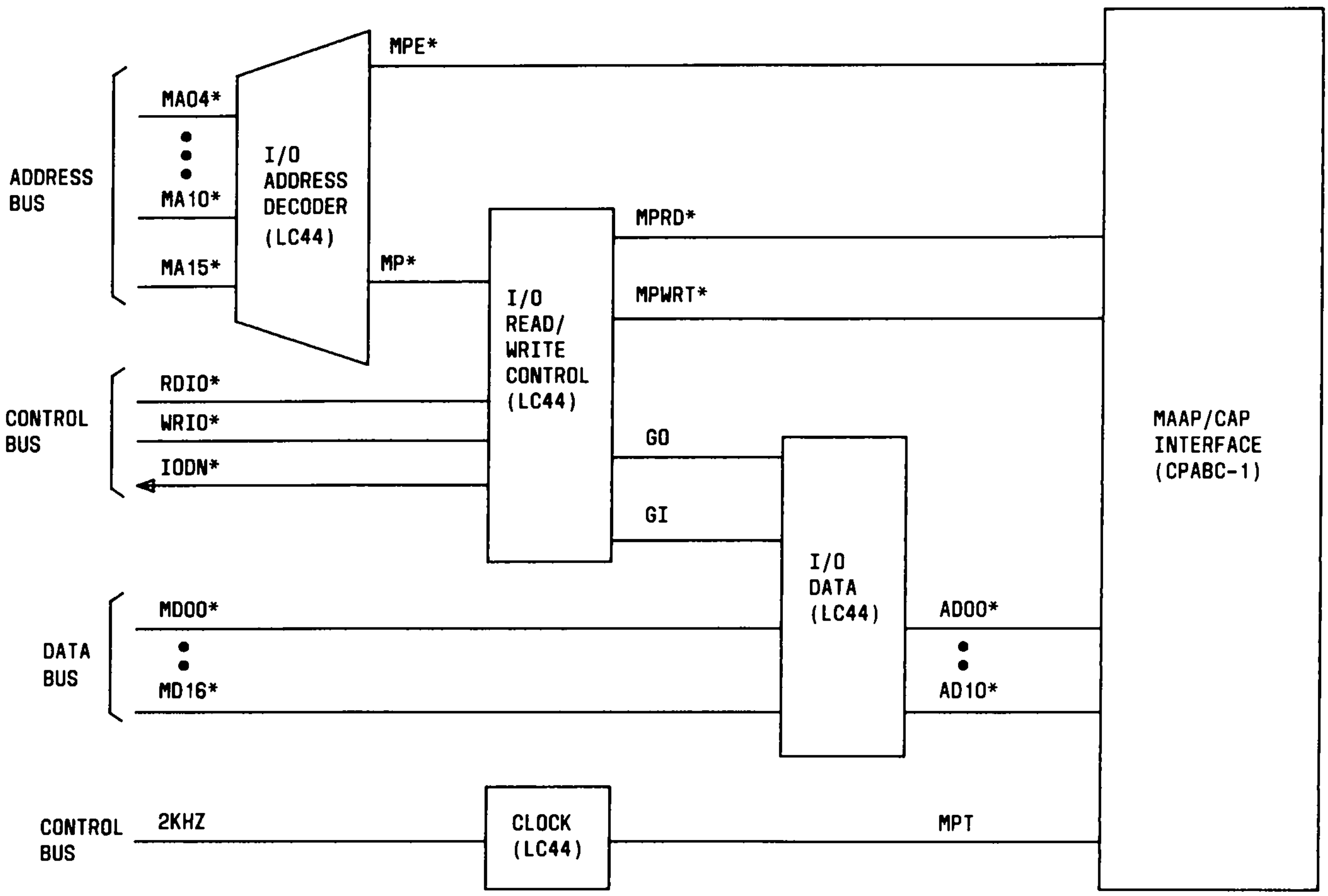
4.08 Data flow between the processor and the MAAP/CAP is via the I/O data buffers and the main data bus. When an active read command is decoded, the gate out (GO) signal is generated to gate data to the processor from the MAAP/CAP via the

TABLE A

I/O ADDRESS DECODER ASSOCIATED WITH J58891AA CARRIER

MAIN ADDRESS LEAD (MA—*)								ENABLE LEAD	PERIPHERAL CIRCUIT ASSOCIATED WITH ENABLE LEAD	SLOT	CARRIER
15	10	9	8	7	6	5	4				
1	1	0	0	1	1	1	1	IOEFF*	I/O Loop Test	27	0
1	1	0	0	1	0	1	1	MPE*	MAAP/CAP	29	
1	0	0	1	1	1	1	1	IOE00*	Data channel 0 (console 0)	30/33	
1	0	0	1	1	1	1	0	IOE01*	Data channel 1 (console 1)		
1	0	0	1	1	0	0	1	IOE06*	Data channel 2 (console 2)		
1	0	0	1	1	0	0	0	IOE07*	Data channel 3 (console 3)		
1	0	0	1	1	0	0	1	IOE02*	Data channel 6	31/34	
1	0	0	1	1	1	0	0	IOE03*	Data channel 7		
1	0	0	1	0	1	1	1	IOE08*	Data channel 8		
1	0	0	1	0	1	1	0	IOE09*	Data channel 9		
1	0	0	1	1	0	1	1	IOE04*	Data channel 4 (SMDR)	32/37	
1	0	0	1	1	0	1	0	IOE05*	Data channel 5 (RMATS/TAPE)		
1	0	0	1	0	0	0	1	IOE14*	Data channel 14		
1	0	0	1	0	1	0	1	IOE10*	Data channel 10	35/36	
1	0	0	1	0	1	0	0	IOE11*	Data channel 11		
1	0	0	1	0	0	1	1	IOE12*	Data channel 12		
1	0	0	1	0	0	1	0	IOE13*	Data channel 13		

* Indicates lead is active in the low state.



CONTROL		ADDRESS								FUNCTION
RDIO*	WRIO*	15	10	9	8	7	6	5	4	
0	1	1	1	0	0	1	0	1	1	READ COMMAND
1	0									WRITE COMMAND

Fig. 7—Decoding Messages Through I/O Buffer to MAAP/CAP Interface (CP ABC-1) Circuit

AD00* through AD10* leads. An active write command generates the gate in (GI) signal to gate the data in the other direction—to the MAAP/CAP.

4.09 A 2-kHz signal (MPT) from the processor is buffered and directed to the MAAP/CAP for use as a button-scan clock signal.

4.10 A low is generated on the I/O done (IODN*) lead to inform the processor that the MAAP/CAP address and the MPRD* or MPWRT* command have been decoded.

B. Decoding Messages to the Data Links

4.11 When a valid data link channel address and a read or write command have been decoded, the data link read (DLRD*) and write (DLWRT*) and one of the I/O enable (IOE00* through IOE14*) leads are generated to enable the selected channel (Fig. 8). The data link read and write signals are directed to all data channels; however, only the channel enabled by the IOE_ _* signal will respond to the processor command.

4.12 The I/O clock divides the 10-MHz input signal to provide the slow (CLKS) and fast (CLKF) clock signals for the data channels.

4.13 When the selected data link has been enabled, the IOP* signal is received by the I/O buffer. In turn, the I/O done (IODN*) signal is generated to inform the processor that the data channel address and the DLRD* or DLWRT* commands have been decoded.

5. READ/WRITE DATA CHANNEL COMMANDS

5.01 The data channel is a circuit which transfers data between the processor and the peripheral devices. The data channel may be provided on one of the four circuits in the LC554 or one of the two circuits in the LC570B as listed in Table B.

5.02 Data is transmitted over the 4-wire data link as a series of bipolar pulses with the leading edge of the bipolar pulse being positive or negative to indicate a 1 or 0 (Fig. 3). The 5-wire data link transmits data via the EIA RS-232C format.

5.03 The transmission rates for the data links are shown in Table B. A software option is provided with the LC570B to select the desired transmission speed. The LC554 provides four low speed channels.

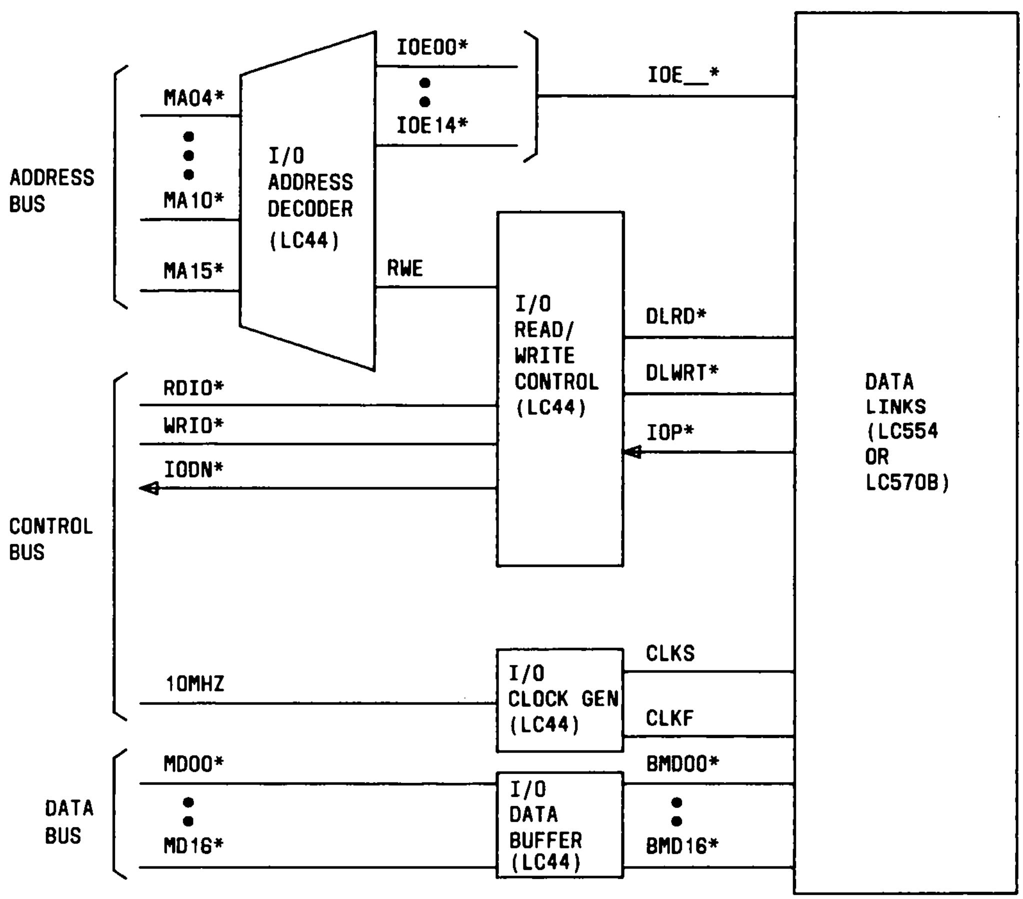


Fig. 8—Decoding Messages Through I/O Buffer to Data Links (LC554 or LC570B)

TABLE B

DATA CHANNEL CIRCUITS

CIRCUIT NUMBER	DESCRIPTION		TRANSMISSION RATE: KILOBITS PER SECOND 185	833	BAUD 300	1200	4800	9600	NUMBER OF CHANNELS
LC554	Low Speed Serial Data		•						4
LC570B	SMDR		•*	•					1
	RS232 Port	Tape				•*	•*	•	1
		RMATS			•	•*			

* At present, applications are not available for these transmission rates.

STANDARD DATA CHANNEL

5.04 The message to a peripheral device is transmitted via a data channel as a series of bipolar pulses (Fig. 3). The device must be capable of converting the data to standard logic levels and reconstructing the message into a word-oriented format (Fig. 5). Each word contains 16 bits plus a parity bit (parity is ignored by some devices). The message may contain more than one word with each word being separated by a predetermined interval.

5.05 Peripheral devices connected to a slow speed data channel should be located within 305 meters (1000 feet) of the processor. For installations where this distance is exceeded, a J58879KC-1 data channel repeater or a J58879KD-1 attendant console repeater is available to extend the data link to the device.

A. Write Command

5.06 The data channel responds to a write command by transmitting the information on the data bus to a peripheral device. The response is initiated as the processor places the command information on the address, control, and data buses (Fig. 9).

5.07 The command information is decoded by the I/O buffer circuits to generate the control signals to select and enable the desired data channel. The decoding performed by the I/O buffer has been previously described.

5.08 The I/O enable signal (IOE_*) is directed to the channel select, generating the channel (CHN) signal that enables the gate array. The two select (0,1) leads enable the proper transmit and receive channel. The select signal is used by the input multiplexer and output demultiplexer to activate one of the four transmit and receive channels.

5.09 The channel (CHN) signal and a low write I/O (DLWRT*) are detected by the gate array to generate a high on the transmit mode (XM) lead.

5.10 The timing and control circuit synchronizes the write gate signals with a slow (CLKS) input to provide the timing and control signals for the data channel.

5.11 At the proper time phase, a high on the transmit mode (XM) signal, together with the transmit clock (XT), parallel loads 17 bits of data from the main data bus (BMD00* through BMD16*) into the data register.

5.12 When the data has been loaded into the data register, the processor removes the write command (WRI0* goes high) from the control bus. The transmit mode (XM) goes low to condition the data register for serial operation. The transmit clock (XT) signal then serial shifts the data from the register into the gate array via the transmit serial data lead (XDATA).

5.13 The gate array uses the clock (CLK) and an internal counter to generate the buffer trans-

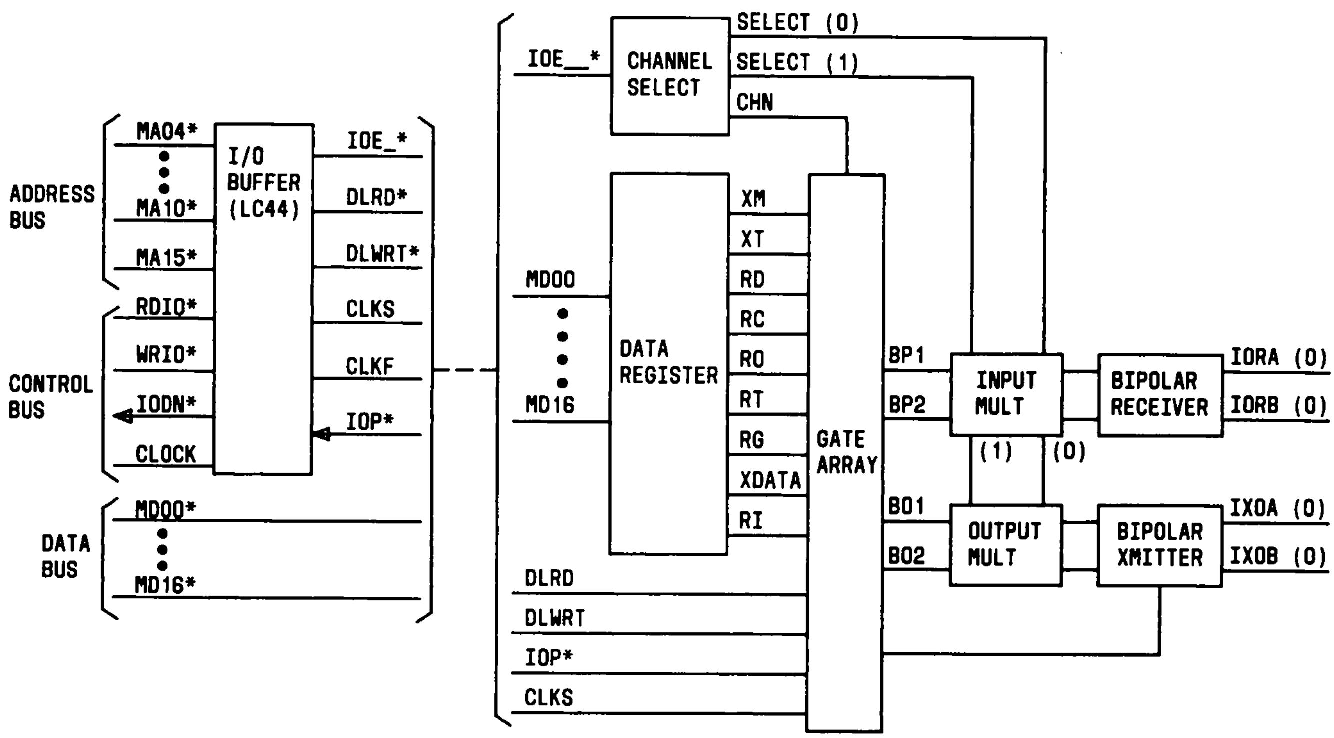


Fig. 9—Standard Data Link (LC554)

mit clock (BC) signal. This signal gates 17 bits of data over buffered outputs B01 and B02 to the preselected transmit circuit.

5.14 The transmit circuit forms the serial data into a series of bipolar pulses (Fig. 3). The signals are transmitted to the peripheral device via a pair of I/O transmit (IOXA and IOXB) leads. The transmission order of the message bits is the most significant bit through the least significant bit followed by the parity bit inverted. The clock (CLK) pulses are counted, and after 17 bits are transmitted, the buffer transmit clock (BC) signal turns off the data register.

5.15 While in the transmit mode, a high on the receive data (RD) lead enables the data register. A single bit is received for each bit transmitted. The data is received as bipolar pulses from the peripheral device via the pair of I/O leads (IORA and IORB).

5.16 The bipolar receiver converts the received data into digital logic levels. The gate array receives the data from the receiver over the incoming data pulses (BP1 and BP2) leads.

5.17 As part of the initialization process to receive data, the gate array clears the data register receiver by a low on the receiver clear (RC) lead. The data is now input into the data register via the receive serial input (RI) lead. The data is clocked in by the receiver clock input (RT).

5.18 After the 17 bits are received, the received serial output (RO) lead shuts down the receiver and stores the data where it can be parallel read by the data bus.

B. Read Command

5.19 The data message remains in the data register receiver to be read by the processor as often as required. The processor issues a read command similar to a write command. The command information is placed on the address and control buses as required (Fig. 9). The I/O buffer decodes the read command to generate the control signals to select and enable the desired data channel. The decoding performed by the I/O buffer is described in Part 4.

5.20 A low on the read I/O (DLRD*) is inverted to produce the high read signal (RIO). The read signal and the channel (CHN) are detected by the gate array.

5.21 If a received message has been completely shifted into the receive register of the data register, a high will be gated to the receive gate parallel (RG) lead. This parallel gates the data to the processor. If the data shift is not complete, the read command is ignored.

5.22 The I/O performing (IOP*) signal is generated by the data channel when a read or write command is received. The signal is decoded by the I/O buffer and directed to the processor via the I/O done (IODN*) lead. The signal informs the processor that the read or write command has been received and decoded.

SPECIAL DATA CHANNEL

5.23 The special data channel prov. 's for standard data set and high-speed data link access to the DIMENSION PRELUDE PBX. The data channel unit provides this interface for RMATS, the tape unit, and SMDR. The circuit responds to inquiries from a central facility and provides a path for data transmission to and from the facility. Traffic, translations, and maintenance data stored in the PBX are transmitted to the facility. Translation changes made from a central location are stored in memory. A run tape command transfers the changes to the translations tape.

A. 5-Wire Link

5.24 The data channel provides an interface that responds to the signals specified in the EIA standard RS-232C format and which are required by the data set associated with RMATS.

5.25 The control unit responds to messages to provide off/on status of data set and data carrier, to provide alarm status, to provide indications of transmitting errors, to transmit traffic and maintenance data, and to receive maintenance instruction data from the central facility.

5.26 The special interface functions similarly to other peripheral devices associated with the PBX. The processor continuously scans the data control unit for an input indication from the central facility.

5.27 The RMATS in the central facility must initiate the data link connection to provide this indication. To establish the connection, a call is made over the dialing network to the data channel. The data channel provides an automatic answer which is controlled by a permanent high on the carrier detector lead RMATS (CCR) (Fig. 10). The data channel responds also with a high on the data channel ready RMATS (CDR) and carrier on RMATS (CFR) leads. The first signal informs the processor that the data channel is ready, while the second indicates that the data link carrier signal is present. The carrier on signal is decoded to light the CARR LED.

Read Command

5.28 Data is received from the data set via the receive data (BBR) lead, then converted to the PBX form by the EIA interface. The EIA input multiplex checks for commands requiring a change of channel (discussed later) and serial shifts the data into the take I/O (T I/O) data register. The T I/O data register parallel loads the information into the receiver for temporary storage and waits for a read command from the processor.

5.29 To initiate the read command, the processor places the I/O address associated with the data channel (Table A) on the main data bus and a low on the read I/O (RDIO*) control lead.

5.30 The read command is decoded by the I/O buffer, and the following signals are directed to the control unit:

IOE05* = 0

DLRD* = 0.

5.31 The address decoder on the control unit responds to the incoming low address signal (IOE05*) and the low read I/O control (DLRD*) signal to generate the high read gate (RDG) signal.

5.32 The high read signal is used by the control unit to generate a low on the I/O performing (IOP*) lead. This signal is directed to the processor via the I/O buffer to indicate that the I/O command has been received.

5.33 The high read gate signal is also used to gate circuit status indications to the processor via the buffered main data bus (BMD08* through BMD15*) leads. The read gate signal is also inverted to produce the read initiate (RDI*) signal. The RDI*

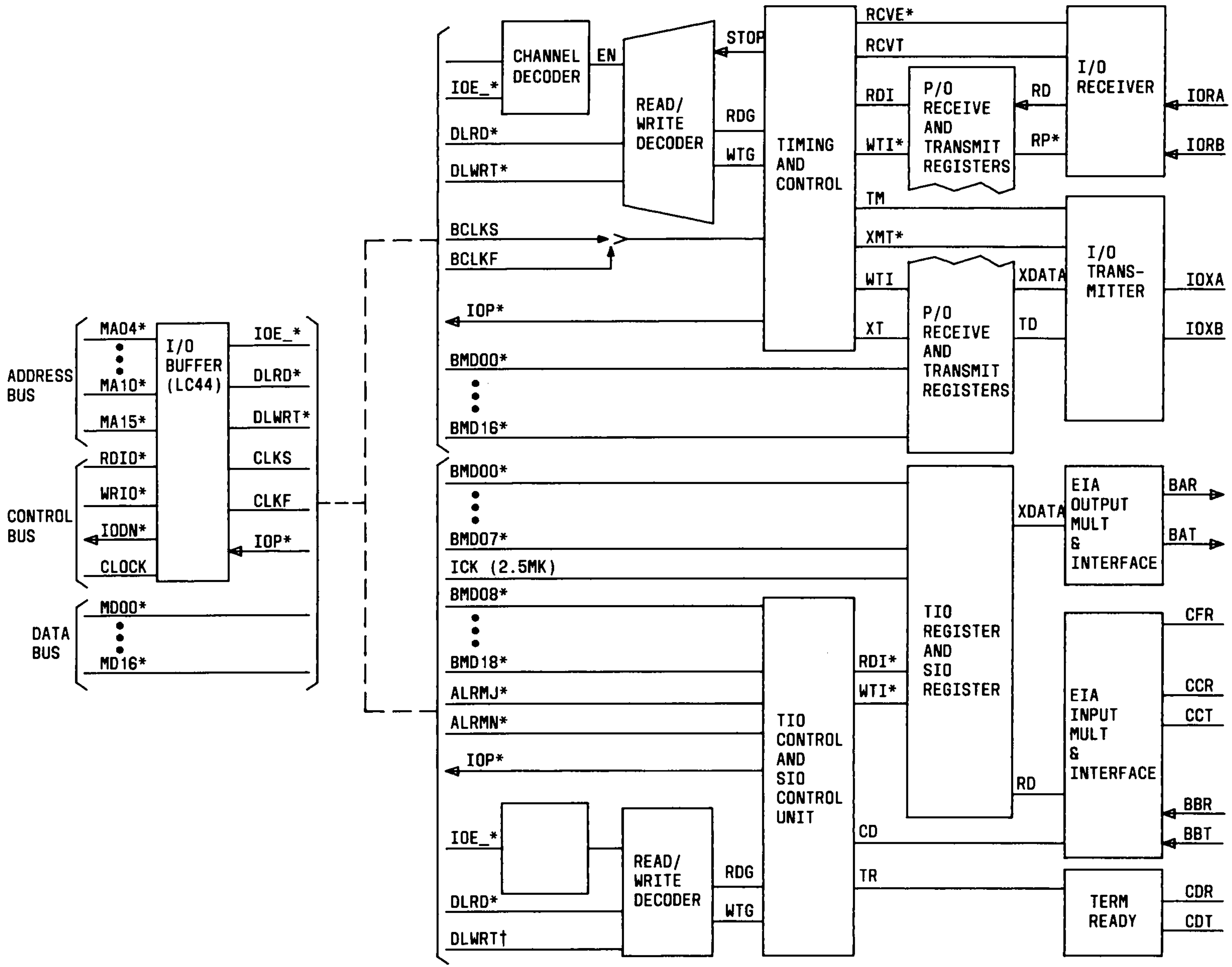


Fig. 10—Special Data Link (LC570B)

signal enables the T I/O data register. This permits the information stored in the T I/O data register to be gated to the processor via the buffered main data bus (BMD00 through BMD07) leads and the I/O buffer. The complete word format for the RMATS response to the read command is shown in Fig. 11.

Write Command

5.34 The processor responds to the information from the central facility with a write command. The command is placed on the main buses and decoded by the I/O buffer. The following signals are generated and directed to the data control unit:

IOE05* = 0

DLWRT* = 0

MD00* - MD15*

MD16* = (Write Command Data).

5.35 The control unit responds by decoding the incoming command signals to generate a high on the write gate (WRG) lead. The control unit responds by informing the processor that the I/O command has been received via a low on the I/O performing (IOP*) lead.

5.36 The buffered main data bus information (BMD08* through BMD16*) is parallel-loaded onto the control unit. The data on bit 15 conditions the control circuit to transmit or inhibit data flow to the central facility (Fig. 12). Bit 13 conditions the control circuit to generate the appropriate word length for transmitting either traffic (seven bits) or maintenance (eight bits) information. Bit 11 selects either RMATS or the tape unit as a destination.

5.37 The traffic or maintenance data, whichever is requested by the central facility, is received (BMD00* through BMD07*) and directed to the send (S I/O) data. The eight bits of parallel data are placed in a transmit register, shifted, and transmitted when the high write initiate (WTI*) signal is received. The data is converted to serial form and transmitted to the data set via the transmit data (BAR) lead. The format for the command is shown in Fig. 12.

5.38 The transmitted information consists of a start bit, the data bits (with the LSB first and MSB last), a parity bit, and one or two stop bits. The control circuit generates the additional start and

	RECEIVED DATA								RESPONSE							
BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	1	0	1	0	1	0	1	0	(SEE BELOW)							
	DATA RECEIVED FROM CENTRAL FACILITY WHEN BIT 10 = 0 (SAMPLE DATA SHOWN IS NOT REPRESENTATIVE)								RESPONSE TO READ COMMAND							

BIT 8 - MAJOR ALARM OCCURRED - 0 = NO; 1 = YES
BIT 9 - MINOR ALARM OCCURRED - 0 = NO; 1 = YES
BIT 10 - 0 = DATA IN BITS 0-7 IS A MAINTENANCE INSTRUCTION FROM CENTRAL FACILITY
1 = REQUEST FROM CENTRAL FACILITY TO SEND TRAFFIC DATA
BIT 11 - TRANSMIT BUFFER - 0 = EMPTY, READY TO SEND; 1 = FULL, NOT READY TO SEND
BIT 12 - VALID DATA IN BITS 0-7 - 0 = VALID; 1 = NOT VALID
BIT 13 - DATA SET READY - 0 = YES; 1 = NO
BIT 14 - CARRIER SIGNAL PRESENT - 0 = YES; 1 = NO
BIT 15 - ERROR OCCURRED - 0 = YES; 1 = NO

Fig. 11—Remote Maintenance, Administration, and Traffic System (RMATS) Response to Read Command

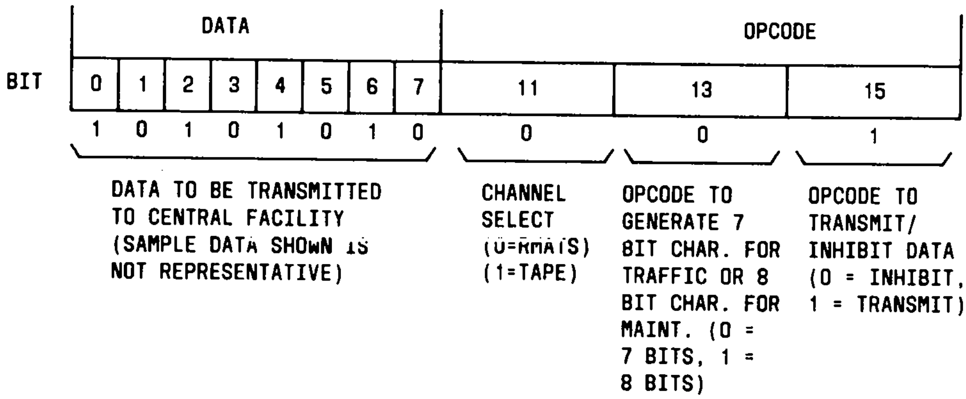


Fig. 12—RMATS Format for Write Command

stop bits to provide means for the central facility to distinguish between the end of one word and the start of another. The format of the maintenance and traffic messages is shown in Fig. 13.

5.39 When the EIA input multiplex detects a run tape command, the EIA interface connections are switched from the RMATS data set to the RS-232 tape unit (Fig. 10).

5.40 The data channel now provides an interface with the tape unit through the carrier detec-

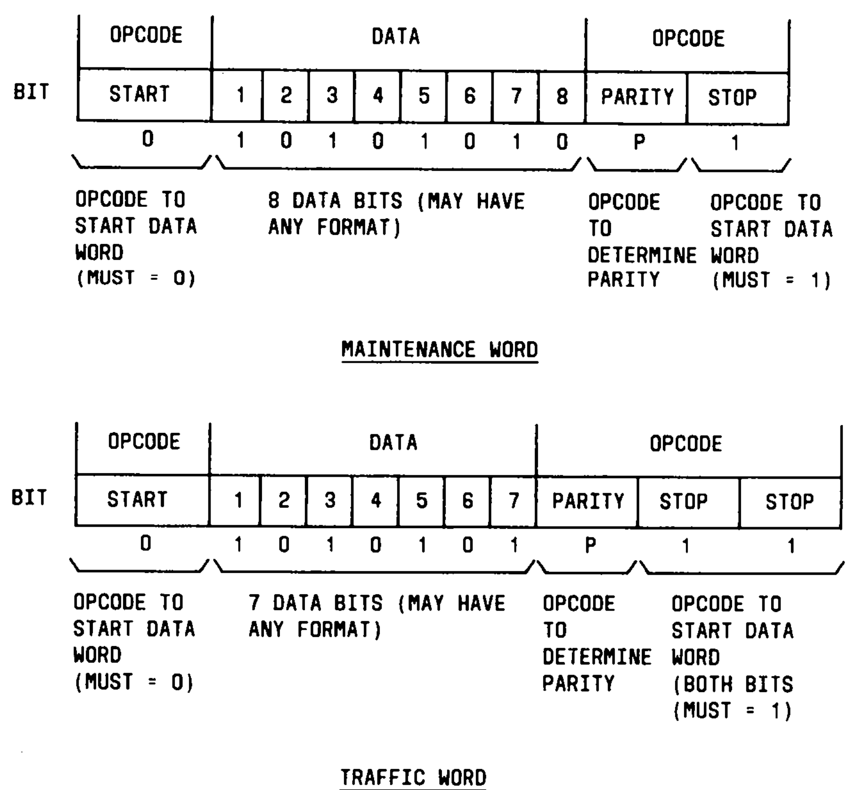


Fig. 13—Format for Maintenance and Traffic Words

tor lead tap (CDT), data channel ready (CCT), receive data tape (BBT), and transmit data tape (BAT) leads in the same manner as with the RMATS unit.

5.41 Changes made to the system's translations in the random access memory can now be transferred to the tape. When a run tape completes or an error is detected by the EIA multiplex, the EIA connections are shifted back to RMATS and the appropriate message returned to the RMATS location.

5.42 When the run tape operation is being performed, the Braemar tape unit (Fig. 14) provides a visual indication of operating status and error conditions via six LEDs. The three red LEDs, labeled motion, read, and write, light to indicate when these states are active. The three yellow LEDs use an off/on code to indicate a successful operation or the type of error detected. This error code is presented in Table C.

B. 4-Wire Link

5.43 The special data channel also provides for SMDR and traffic measurements interface. The interface is via a high-speed 4-wire circuit which transfers data between the processor and the peripheral device. The speed at which the data is transferred can be software selected (Table B).

5.44 The data is transmitted over the data link as a series of bipolar pulses with the leading edge of the bipolar pulse being positive or negative to indicate a 1 or 0 (Fig. 3).

5.45 Peripheral devices connected to a high-speed data channel (833 kilobits per second) must be located within 61 meters (200 feet) of the processor.

Write Command

5.46 The high-speed data channel responds to a write command by transmitting the information on the data bus to a peripheral device. The response is initiated as the processor places the command information on the address, control, and data buses (Fig. 9).

5.47 The command information is decoded by the I/O buffer circuits to generate the control signals to select and enable the desired data channel. The decoding performed by the I/O buffer has been previously described.

5.48 The I/O enable signal (IOE_ _*) is directed to the channel decoder to enable (EN) the read/write decoder circuit (Fig. 9).

5.49 The enable (EN) signal and a low write I/O signal (DLWRT*) are detected by the read/write decoder to generate the write gate (WTG) signal.

5.50 The timing and control circuit synchronizes the write gate signal with a slow (CLKS) or fast (CLKF) clock input to provide the timing and control signals for the data channel.

5.51 At the proper time phase, an active write command generates a high write initiate (WTI) signal which, together with the transmit clock (XT) signal, parallel loads 17 bits of data from the buffered main data bus (BMD00* through BMD16*) into the transmit register. A low write initiate (WTI*) signal clears the receive register to receive new information, while the low STOP signal inhibits a read command input to the read/write decoder.

5.52 When the data has been loaded into the transmit register, the processor removes the write command (WRIO* goes high) from the control bus. The write initiate (WTI) signal goes low to condition the transmit register for serial operation. The transmit clock (XT) signal then serial shifts the data from the register into the transmitter circuit via the transmit data (XDATA) lead.

5.53 The transmitter uses the clock (XMT*) and control (TM) signals to convert the shifted data (XDATA) into a series of pulses (Fig. 3). The signals are transmitted to the peripheral device via the pair of I/O transmit (IOXA and IOXB) leads. The transmission order of the message bits is the most significant bit through the least significant bit followed by the parity bit inverted. The clock (XT) pulses are counted and, after 17 bits, are transmitted; a control (TD) signal is generated to turn the transmitter off.

5.54 While in the transmit mode, a high on the receiver enable (RCVE*) lead enables the I/O receiver. A single bit is received for each bit transmitted. The data is received as serial pulses from the peripheral device via the pair of I/O receive leads (IORA and IORB).

5.55 The receive clock (RCVT) signal and the received parity (RP*) signal are used by the receiver to convert the serial pulses into digital logic levels. The receive clock (RCVT) signal also clocks the receive data (RD) into the register for storage.

5.56 After the 17 bits are received, the receiver enable (RCVE*) signal goes low to inhibit data

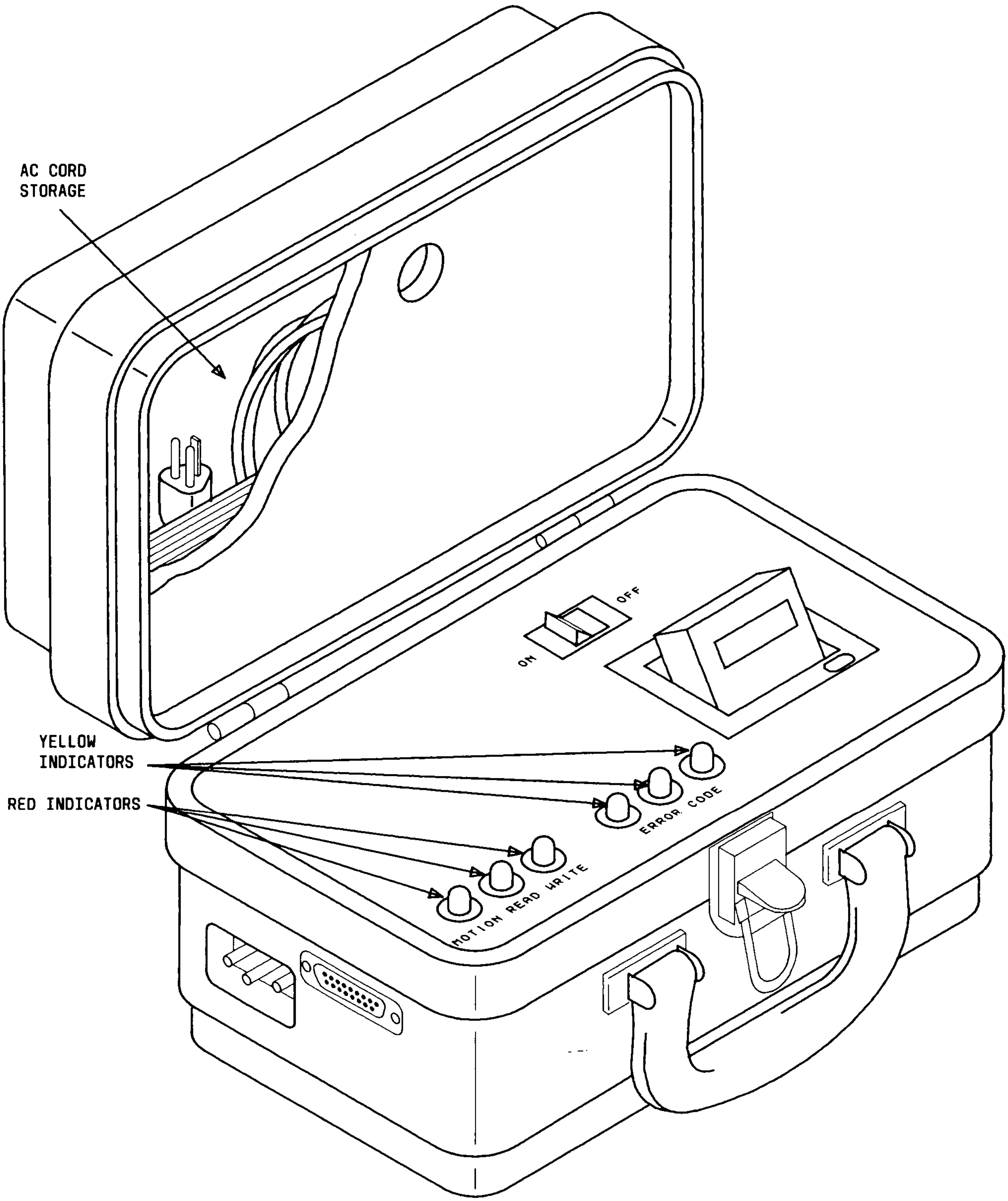


Fig. 14—Tape Drive

TABLE C

ERROR CODES

ERROR CODE LEDs			EXPLANATION
LEFT	CENTER	RIGHT	
OFF	OFF	OFF	Successful operation
OFF	OFF	ON	File not found
OFF	ON	OFF	WRITE protect error
OFF	ON	ON	End of tape
ON	OFF	OFF	Check/sum error
ON	OFF	ON	Filemark or READ
ON	ON	OFF	Block size greater than 2K bytes

reception at the receiver. The control (STOP) signal goes high to enable the read/write decoder to detect an incoming read command.

Read Command

5.57 The data message remains in the receiver register to be read by the processor as often as required. The processor issues a read command similar to a write command. The command information is placed on the address and control buses as required (Fig. 9). The I/O buffer decodes the read command to generate the control signals to select and enable the desired data channel. The decoding performed by the I/O buffer is described in Part 4.

5.58 The I/O enable (IOE_ _*) signal is directed to the channel decoder to enable (EN) the read/write decoder circuit (Fig. 15).

5.59 The enable (EN) signal, a low read I/O (DLRD* or BRDIO*) signal, and a high control (STOP) signal are decoded by the read/write decoder to provide the read gate (RDG) signal.

> ***Note:*** The high control (STOP) signal indicates 17 bits of data are available in the receive register. The data channel ignores the read command when this signal is not present.

5.60 The timing and control circuit decodes the read gate (RDG) signal to generate the read initiate (RDI) signal. The read initiate (RDI) signal gates the data in the receive register onto the data bus leads. The data is directed to the processor via the data bus (MD00* through MD16*) leads.

5.61 The I/O performing (IOP*) signal is generated by the data channel when a read or write command is received. The signal is decoded by the I/O buffer and directed to the processor via the I/O done (IODN*) lead. This signal informs the processor that the read or write command has been received and decoded.

6. MAINTENANCE AND ADMINISTRATION PANEL

6.01 The MAAP provides the means to alter translations, initiate traffic measurements, and initiate maintenance programs to isolate faults. The MAAP used in the DIMENSION PRELUDE PBX systems is shown in Fig. 16. Each MAAP provides buttons for entering data and commands into the system, and display devices to indicate data and status information from the processor.

6.02 The MAAP operations use a series of procedures to accomplish the desired functions. Each procedure is accessed by dialing an associated 2-digit code. Once the request to access a particular procedure is completed by the processor, the WAIT lamp on the MAAP is extinguished and the procedure

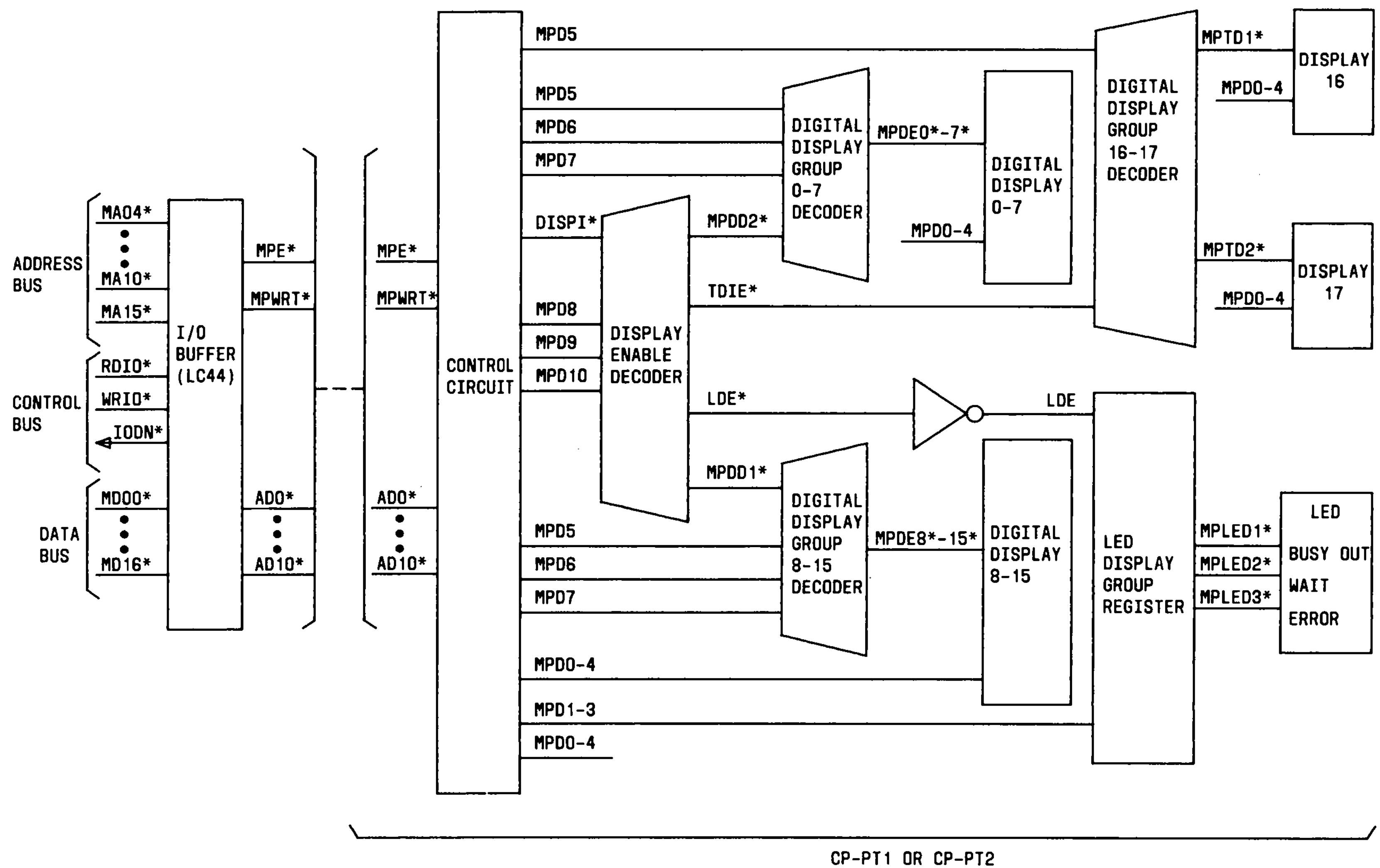


Fig. 15—MAAP (CP-PT1) and CAP (CP-PT2)—Write Command

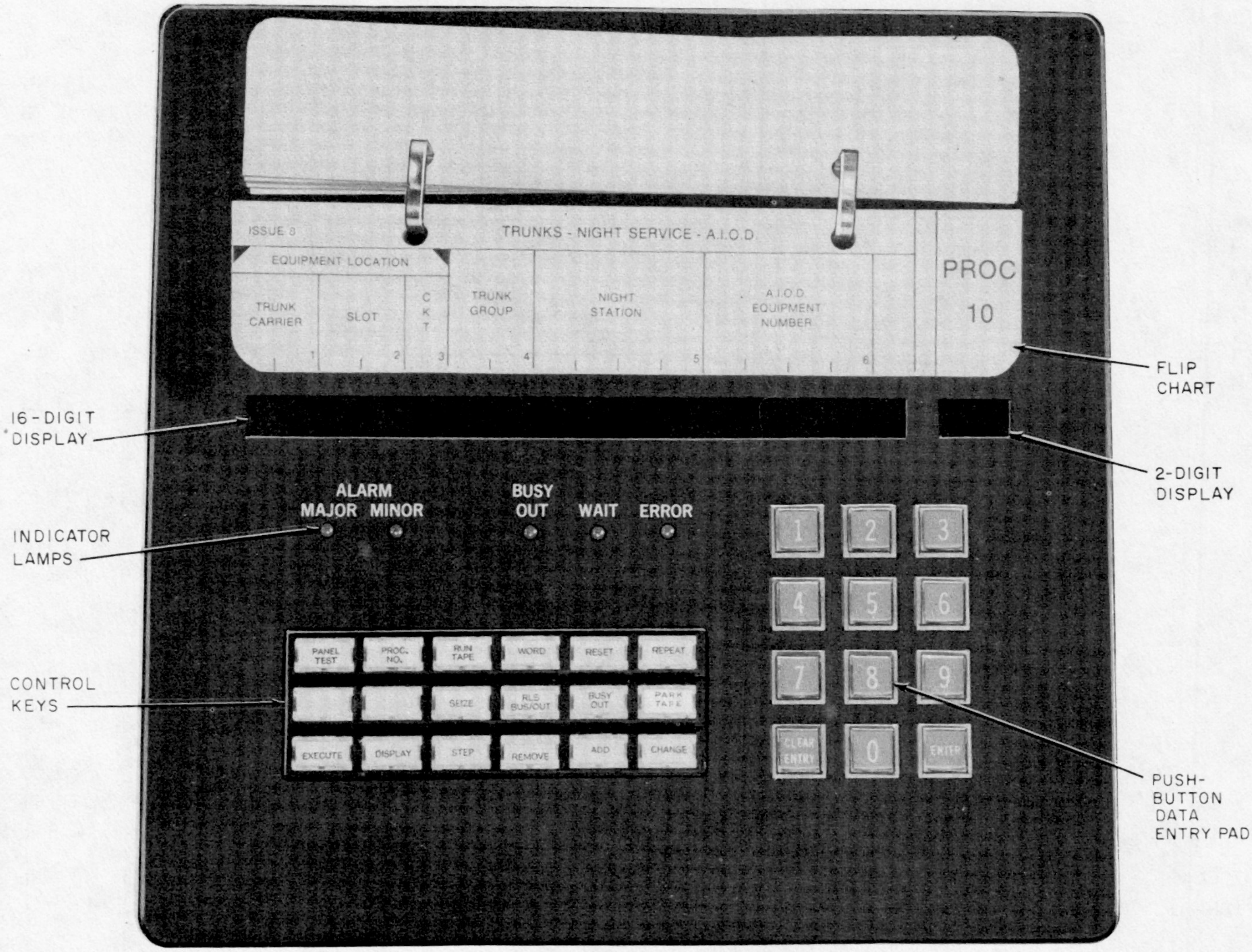


Fig. 16—Maintenance and Administration Panel

is ready for use. Proper operation of the MAAP will not usually interrupt customer service except for certain maintenance procedures.

6.03 The MAAP is stored in the equipment cabinet. Connectors are provided in the cabinets to accept the plug on the 2.4-meter (8-foot) cable associated with the MAAP. The MAAP must be removed from storage and connected before using.

J58879DA MAAP— "DIMENSION" "PRELUDE" PBX

6.04 The J58879DA MAAP is powered at the input connection. When the MAAP is connected and the CAP is not in use, the MAAP will respond to four control signals: (1) MAAP read (MPRD*), (2) MAAP write (MPWRT*), (3) MAAP enable (MPE*), and (4) MAAP timing (MPT). Data flow between the MAAP and processor is via the 11 data (AD00* through AD10*) leads. All data leads are used when a write command is addressed to the MAAP. Eight data (AD0* through AD7*) leads are required for a response to a read command.

A. Read Command

6.05 To initiate a read command, the processor places the MAAP address information on the address bus (see Table A) and a low on the control bus read I/O (RDIO*) lead. The information is decoded by the I/O buffer, as previously described, and the three control signals (MPE*, MPRD*, and MPT) are directed to the MAAP (Fig. 17). The read (RDIO*) control signal also enables the I/O buffer to gate data from the MAAP to the processor via the data (AD0* through AD7*) leads, the I/O buffer, and the main data bus (MD00* through MD16*) leads.

6.06 When the MAAP is plugged in, a 2000-Hz signal from the processor via the MAAP timing (MPT) lead drives a counter in the button scan control circuit. The outputs of the counter continuously scan the control buttons on the MAAP. The counter outputs are interpreted by the decoder (MPB0, MPB1, and MPB2) and by the multiplexer (MPB3, MPB4, and MPB5). The decoder output (MPBFC0 through MPBFC5) leads provide a signal via an operated button to one of the multiplexer input (D0 through D5) leads to perform the scanning function. The counter outputs are also directed to the MAAP data (AD0* through AD7*) leads.

6.07 The information on the counter leads reflects the identity of the button being scanned at that particular moment. When a button is operated, the counter stops at the button number and remains stopped until the button is released. The button enable (BE) lead from the multiplexer stops the counter when a button is pushed.

6.08 While the button is down and the scanning has stopped, a read command gates the button number to the processor over the I/O data (AD0* through AD5*) leads.

6.09 Two additional bits are gated onto the data bus during each read command. A low is placed on one data (AD6*) lead when a valid button number is available. A low on the other data (AD7*) lead informs the processor that the MAAP is plugged in and is operational. The CAP places a low on data (AD8*) lead as well as AD7* to inform the processor that a CAP is operational.

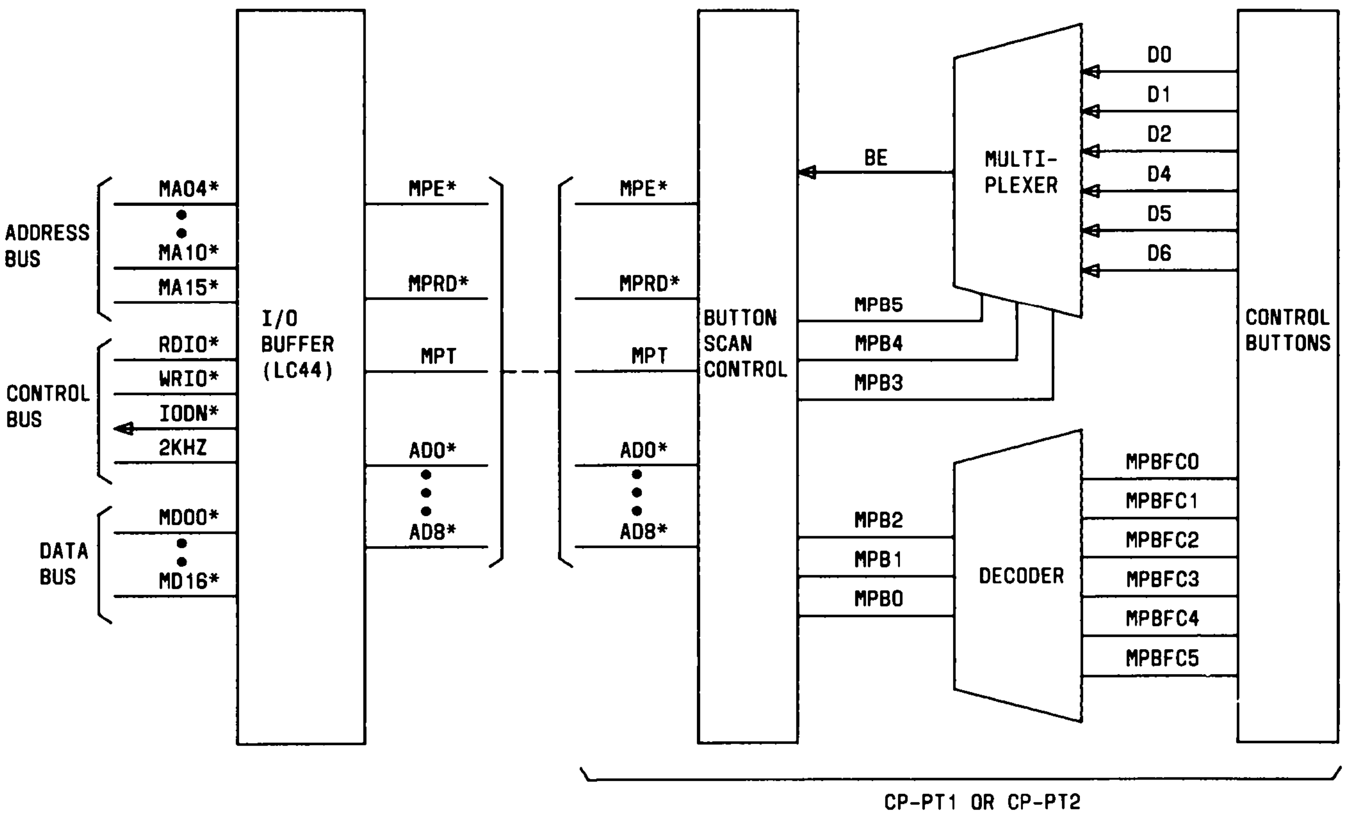


Fig. 17—MAAP (CP-PT1) and CAP (CP-PT2)—Read Command

6.10 Typical responses to read commands are shown in Table D. The location of each button and the associated 6-bit address expressed in octal form for the MAAP/CAP are shown in Fig. 18. The function of each button and the octal address are shown in Table E.

B. Write Command

6.11 To initiate a write command, the processor places the MAAP address information on the address bus (see Table A) and a low on the control bus write I/O (WRIO*) lead. The information is decoded by the I/O buffer as previously described, and the two control signals (MPE* and MPWRT*) are directed to the MAAP (Fig. 15). The write I/O (WRIO*) control signal also enables the I/O buffer to gate data from the processor to the MAAP via the main data bus (MD00* through MD16*) leads, the I/O buffer, and the data (AD0* through AD10*) leads.

6.12 A low on the two control (MPE* and WPWRT*) leads enables the control circuit and conditions the MAAP for a write command. The display initiate (DISPI*) lead goes low to enable the display enable decoder. The information on the data (AD0* through AD10*) leads is parallel-loaded into the control circuit, buffered, and directed to the various decoders and registers via the MAAP data (MPD0 through MPD10) leads.

6.13 Write commands to the MAAP are issued with data in two formats. One format is used to write one of the 18 digital displays. The other format is used to write the three software-controlled LEDs.

C. Display Format

6.14 The word format for writing a digital display is shown in Fig. 19. Operation code (opcode) bit 10 informs the MAAP to write a display. The data (AD10*) signal must be high for a MAAP response.

6.15 Two address bits (AD8* and AD9*) are decoded by the display enable decoder to select one of the four display groups on the MAAP. There are three digital display groups and one LED display group. The combination of signals required to select a particular group is shown in Table F.

TABLE D

TYPICAL RESPONSES OF MAAP/CAP TO READ COMMANDS

RESPONSE ON AD0*—AD8* LEADS									MEANING OF RESPONSE
8	7	6	5	4	3	2	1	0	
1	1	1	1	1	1	1	1	1	MAAP/CAP not plugged in
1	0	1	1	1	1	1	1	1	MAAP plugged in, no buttons operated
0	0	1	1	1	1	1	1	1	CAP plugged in, no buttons operated
1	0	0	1	1	1	1	0	1	MAAP run tape button operated- address = 111101 = 75 octal
1	0	0	1	0	1	1	1	1	MAAP execute button operated–address = 101111 = 57 octal
1	0	0	0	1	1	1	0	0	MAAP clear entry button operated–address = 011100 = 34 octal
0	0	0	0	1	1	1	0	0	CAP clear entry button operated–address = 011100 = 34 octal

* Indicates lead is active in the low state.

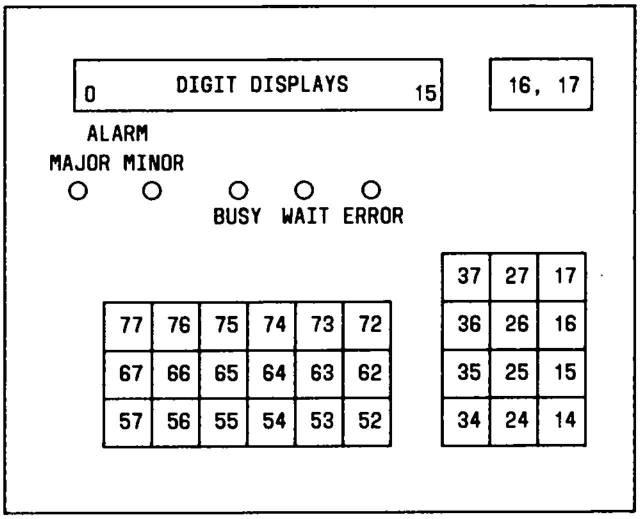


Fig. 18—MAAP—Layout of Displays, LEDs, and Control Buttons

6.16 Three address bits (AD5*, AD6*, and AD7*) are decoded by the enabled display group decoder to select one of the displays within the group. Only address (AD5*) bit 5 is required to select one of the two displays in display group 16 and 17. Only one digital display can be addressed at a time. When necessary to change ten displays, a series of ten write commands are required. The signals required to enable a digital display within a group are shown in Table G.

6.17 Five data (AD0* through AD4*) bits are provided to select the information to be written into the display. The information is directed to all digital displays via the MAAP data (MPD0 through MPD4) leads, but only the enabled display will respond. Data (AD4*) bit 4 turns the decimal point associated with the enabled display off and on. The remaining four data (AD0* through AD3*) bits are latched into the display and decoded to drive the display outputs. The data will remain in the display until new information is received. Table H shows the information displayed as a function of the data (AD0* through AD3*) leads.

D. Light Emitting Diode (LED) Format

6.18 The word format for a LED display is shown in Fig. 20. Again, opcode bit 10 informs the MAAP to write a display. The data (AD10*) signal must be high for a MAAP response.

6.19 The two address (AD8* and AD9*) bits are decoded by the display enable decoder to select the LED display group. The LEDs are addressed as a group; therefore, additional address leads are not required. A low on each address lead is required to select the LED enable (LDE*) lead (see Table F). The LED enable signal is inverted to enable the LED display register.

6.20 The three data (AD1*, AD2*, and AD3*) leads provide the information to write each LED. The LED associated with each lead is as follows:

AD1*—BO (Busy Out)

AD2*—WAIT

AD3*—ERROR.

6.21 When the register is enabled, the information on the three MAAP data (MPD1, MPD2, and MPD3) leads is parallel-loaded into the register to directly drive the LEDs via the three MAAP LED (MPLED1, MPLED2, and MPLED3) leads. A high is required on the associated data (AD_*) lead to light the LED.

7. PERIPHERAL DEVICE RESPONSE TO MESSAGES VIA DATA CHANNELS

7.01 Serial data channels provide the interface between the peripheral device and the PBX. The interface for most peripheral devices is provided by a standard data channel (LC554). A special interface, however, is required for a data set associated with RMATS or other similar traffic pollers. This interface is provided by the data control (LC570) circuit.

7.02 Typical peripheral devices for the DIMENSION PRELUDE PBX are the display units, attendant console(s), and peripheral interface circuits.

7.03 The calling number display unit (102D1-A) is used to display the extension number of a calling PBX party. The display unit will respond to messages to light or clear (blank) the 4-digit display.

7.04 To show a number on the display unit, the processor places a write I/O command on the control leads, the digit codes on the main data bus, and the I/O address of the associated data channel on the main address bus (Fig. 6).

7.05 The write command is decoded by the I/O buffer and enables the data channel associ-

TABLE E

BUTTON ADDRESS AND FUNCTION ON MAAP/CAP

BUTTON ADDRESS (OCTAL)	BUTTON FUNCTION	BUTTON ADDRESS (OCTAL)	BUTTON FUNCTION
77	Panel Test	53	Add
76	Procedure Number	52	Change
75	Run Tape	51-40	Unused, Invalid
74	Word	37	1
73	Reset	36	4
72	Repeat	35	7
71, 70	Unused, Invalid	34	Clear Entry
67	Spare	33-30	Unused, Invalid
66	Spare	27	2
65	Seize	26	5
64	Release, Busy Out	25	8
63	Busy Out	24	0
62	Park Tape (MAAP)	23-20	Unused, Invalid
61, 60	Unused, Invalid	17	3
57	Execute	16	6
56	Display	15	9
55	Step	14	Enter Data
54	Remove	13-00	Unused, Invalid

ated with the display unit (Fig. 9). The data channel responds by converting the data to a series of pulses and transmitting the information to the display unit.

7.06 The display receives a single-word message and ignores the parity bit. The format of the calling number message is shown in Fig. 21. Actual information to be displayed is a function of the 4-bit binary codes which are shown in Table I (bits 0 through 3, 4 through 7, 8 through 11, or 12 through 15, equal A through D, respectively).

7.07 The display unit responds to the write command by converting the received pulses to standard logic levels and shifting the data into the shift register (Fig. 22). A high is generated on the received bit (RB) lead for each incoming bit. The clock uses the received bit signal to generate clock pulses to control the overall operation of the unit.

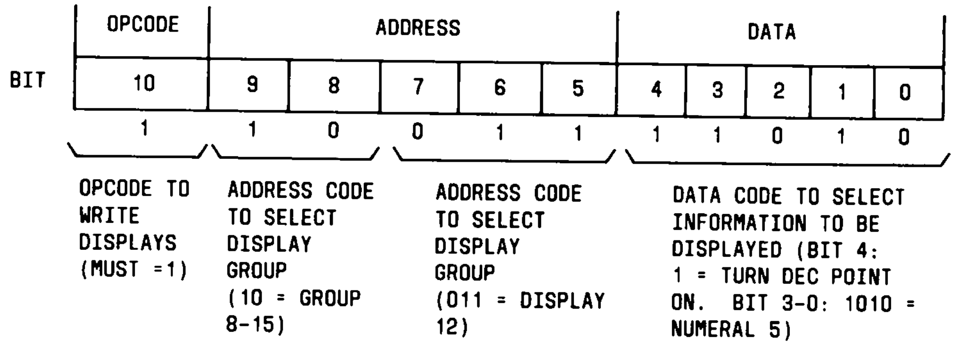


Fig. 19—Word Format for Command to Write Digital Display

TABLE F

SIGNALS TO ENABLE DISPLAY GROUPS ON MAAP

ADDRESS LEADS		DISPLAY GROUP	ENABLED LEAD
AD9*	AD8*		
1	1	Digital Display 0-7	MPDD2*
1	0	Digital Display 8-15	MPDD1*
0	1	Digital Display 16-17	TDIE*
0	0	LED Display (BUSY, WAIT, ERROR)	LDE*

* Indicates that the lead is active in the low state.

7.08 The shift register clock (PH1*) signal clocks the received data into the shift register. The register outputs are directed to each of the four digital displays (labeled 4 through 7) via the register data (DBA through DBD) leads.

7.09 The transmit clock (PH2* and PH3*) signals enable the transmitter gates to echo or retransmit each bit received. The reset (RES*) signal causes a low on the receive bit (RB) lead and conditions the receiver to accept the next incoming bit. The control clock (PH3*) signal is used by the control circuit to count the number of highs appearing on the received bit (RB) lead.

7.10 The current count of received bits is reflected by the circuit on the control data (DS* and BC through BE) leads. These leads are interpreted by the decoder and, when the count of four is reached, a low is placed on the enable display (END4) lead to permit digital display 4 to receive the output of the shift register (DBA through DBD). In turn, as the next four bits or digits of information are received, the decoder places a low on the next enable display lead and, in this manner, enables the other displays in order.

8. DATA CHANNEL AND ATTENDANT CONSOLE REPEATERS

DATA CHANNEL REPEATER

8.01 The data channel repeater provides range extension and/or lightning protection for DIMENSION PBX low-speed data channels. It is connected in series with the data channel to repeat data pulses and to provide isolation between input and output pairs.

TABLE G

SIGNALS TO ENABLE DIGITAL DISPLAY ON MAAP

ADDRESS LEADS			DISPLAY GROUP					
			0-7		8-15		16-17	
AD7*	AD6*	AD5*	ENABLE LEAD	DISPLAY	ENABLE LEAD	DISPLAY	ENABLE LEAD	DISPLAY
1	1	1	MPDE0*	0	MPDE8*	8	MPTD1*	16
1	1	0	MPDE1*	1	MPDE9*	9	MPTD2*	17
1	0	1	MPDE2*	2	MPDEA*	10	MPTD1*	16
1	0	0	MPDE3*	3	MPDEB*	11	MPTD2*	17
0	1	1	MPDE4*	4	MPDEC*	12	MPTD1*	16
0	1	0	MPDE5*	5	MPDED*	13	MPTD2*	17
0	0	1	MPDE6*	6	MPDEE*	14	MPTD1*	16
0	0	0	MPDE7*	7	MPDEF*	15	MPTD2*	17

* Indicates that the lead is active in the low state.

8.02 The repeater detects and reconstructs incoming modified bi-phase (bipolar) data pulses to eliminate any pulse attenuation or distortion as well as to increase data channel range.

8.03 The repeater circuit is designed to operate in unexposed environments without additional protection or in exposed environments with standard protection.

8.04 Each data channel consists of two data pairs, one for data transmission from the PBX to a peripheral device and the other pair for data response from the peripheral device to the PBX. Separate J58879KC, List 3 (AE-48) repeater circuits are required for each direction. A single channel repeater is shown in Fig. 23 and Fig. 24. illustrates a dual channel repeater. Both illustrations show the repeaters with range extension and without range extension (lightning protection). When only lightning protection is required, J58879KC, List 4 (WJ3) buffer circuit packs are used.

A. Circuit Operation

Receiver Circuit

8.05 Incoming data pulses are transformer-coupled into the receiver circuit. The receiver circuit compares the signal amplitude with a threshold level and produces low outputs whenever the signal level is greater than the threshold level.

8.06 The threshold level is automatically set in the receiver to one-half the peak-to-peak signal amplitude. This feature allows the receiver circuit to operate with a large variation of cable distances, types, and parameters without manual compensation.

Control Circuit

8.07 The control circuit checks the receiver outputs and generates the timing for the transmit circuit. A 300-nanosecond timing reference is supplied by the AE-49 rectifier and timing reference card via the 3.33-MHz clock signal.

TABLE H

OUTPUTS OF DIGITAL DISPLAYS ON MAAP/CAP

DATA LEADS				DISPLAYED INFORMATION
AD3*	AD2*	AD1*	AD0*	
1	1	1	1	0
1	1	1	0	1
1	1	0	1	2
1	1	0	0	3
1	0	1	1	4
1	0	1	0	5
1	0	0	1	6
1	0	0	0	7
0	1	1	1	8
0	1	1	0	9
0	1	0	1	Test Character (8)
0	1	0	0	(Blank)
0	0	1	1	(Blank)
0	0	1	0	Minus Sign
0	0	0	1	(Blank)
0	0	0	0	(Blank)

* Indicates that the lead is active in the low state.

8.08 The control circuit requires both polarities of the bi-phase pulse to be detected within 2.1 microseconds. If only a single pulse is detected, the control circuit inhibits the transmit circuit for the duration of the pulse. This feature allows the repeater to block noise hits.

Transmit Circuit

8.09 The transmitter generates modified bi-phase output pulses. The output pulse amplitude is

	OPCODE	ADDRESS		DATA		
BIT	10	9	8	3	2	1
	1	0	0	1	0	1
	OPCODE TO WRITE DISPLAYS (MUST =1)	ADDRESS CODE TO SELECT LED DISPLAY GROUP (00 = LED GROUP)		DATA CODE TO TURN ON/OFF EACH LED (1 = ON, 0 = OFF)		

DATA BIT	3	2	1
LED	ERROR	WAIT	BUSY OUT

Fig. 20—Word Format for Command to Write LEDs

5 volts; the pulse width is 1.2 microseconds for each polarity. A minimum dead time of 2.4 microseconds is forced by the control circuit.

B. Range Extension

8.10 Range extension is required when the DIMENSION PRELUDE PBX is located in a different building than the peripheral device. One repeater should be located in the peripheral device building (Fig. 25), with others between the two if distance requires more repeaters. A maximum of four repeaters can be cascaded which allow a maximum range of 3350 meters (11,000 feet). The requirement for one of the repeaters to be in the PBX building and another in the peripheral device building is due to lack of protective circuitry in the PBX and peripheral device interface circuits. The repeater-to-repeater link may be exposed if standard protection is provided.

C. Data Range

8.11 Data link range is a function of cable attenuation and receiver sensitivity. The repeater-to-repeater range is 915 meters (3000 feet) for 0.51 millimeter diameter (No. 24 AWG) cable. The PBX-to-repeater and repeater-to-peripheral device data links are limited to 305 meters (1000 foot) range by receiver sensitivity.

8.12 The data range is limited by the cable attenuation and round-trip propagation delay. The

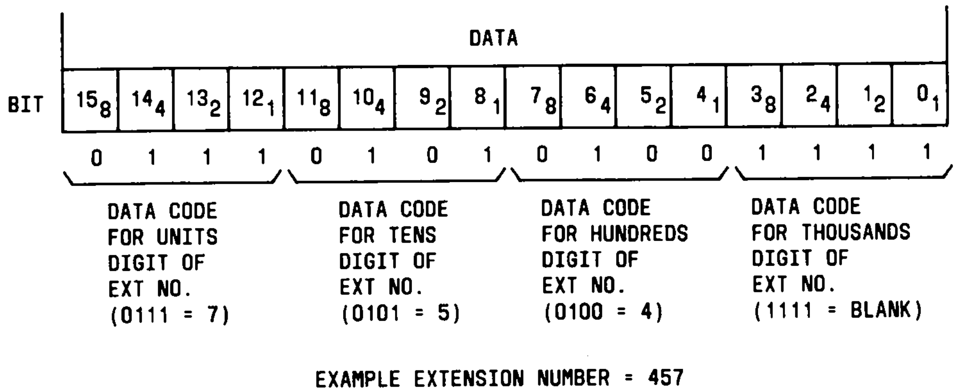


Fig. 21—Format of Calling Number Message

TABLE I

DATA CODE INPUT FOR ACTUAL DISPLAY

DATA CODE BITS					DATA CODE BITS				
D (8)	C (4)	B (2)	A (1)	ACTUAL DISPLAY	D (8)	C (4)	B (2)	A (1)	ACTUAL DISLAY
0	0	0	0	0	1	0	0	0	8
0	0	0	1	1	1	0	0	1	9
0	0	1	0	2	1	0	1	0	Test Pattern
0	0	1	1	3	1	0	1	1	Blank
0	1	0	0	4	1	1	0	0	Blank
0	1	0	1	5	1	1	0	1	Minus
0	1	1	0	6	1	1	1	0	Blank
0	1	1	1	7	1	1	1	1	Blank

cable attenuation is a function of the cable type and temperature.

D. Propagation Delay

8.13 The maximum data range is limited in software by the time allowed for a data channel response. Range extension increases the data response time due to repeater delay and cable propagation. The maximum distance between repeaters may be changed by using different gauge twisted pair wire as shown in Table J.

8.14 Each unidirectional repeater (AE-48) has a 2.4 microseconds delay. In an application employing two repeaters, a total of four repeater circuits is inserted in the loop for a total delay of 9.6 microseconds.

8.15 The cable propagation delay is approximately 1.7 microseconds per 305 meters (1000 feet). In

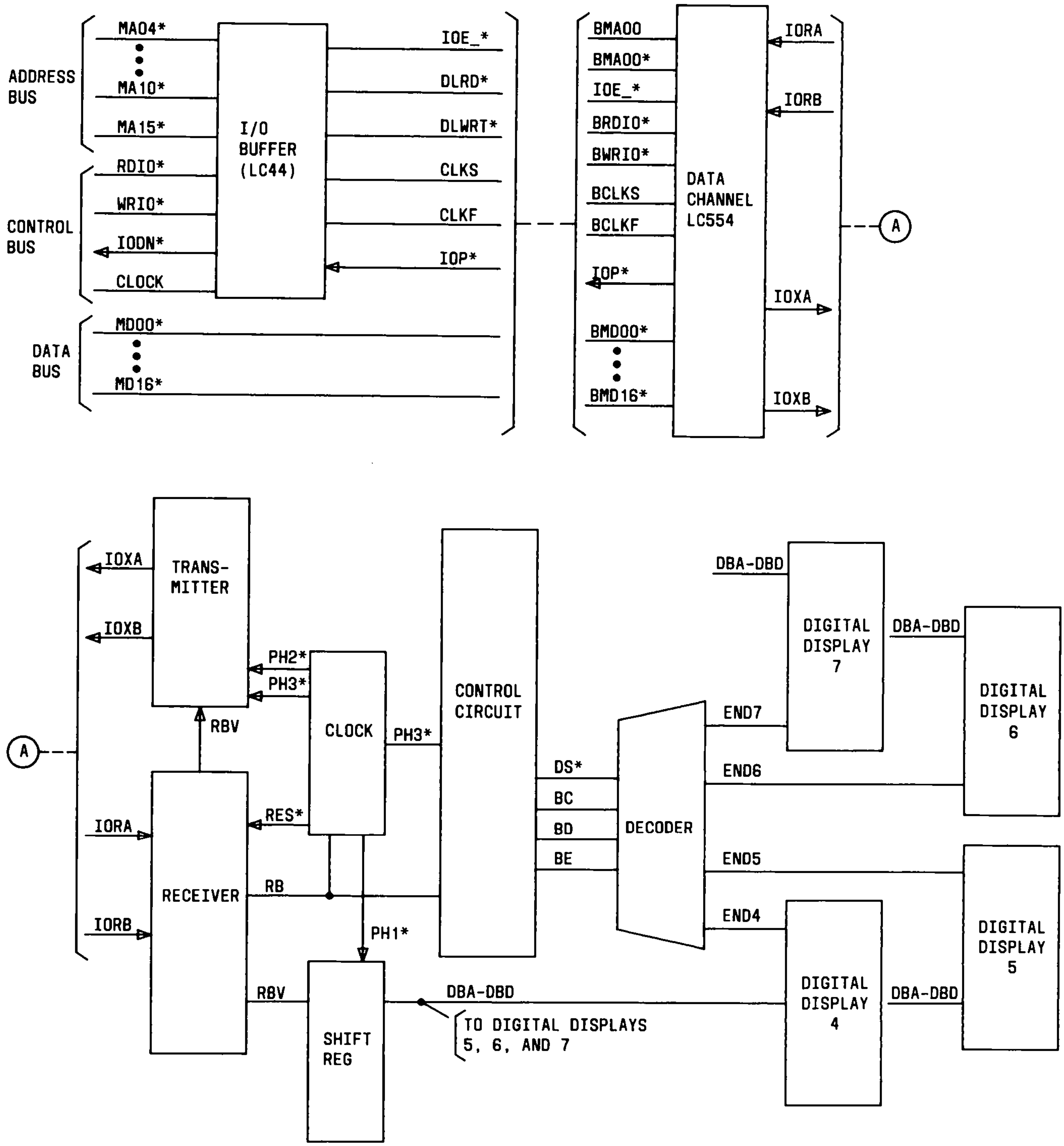
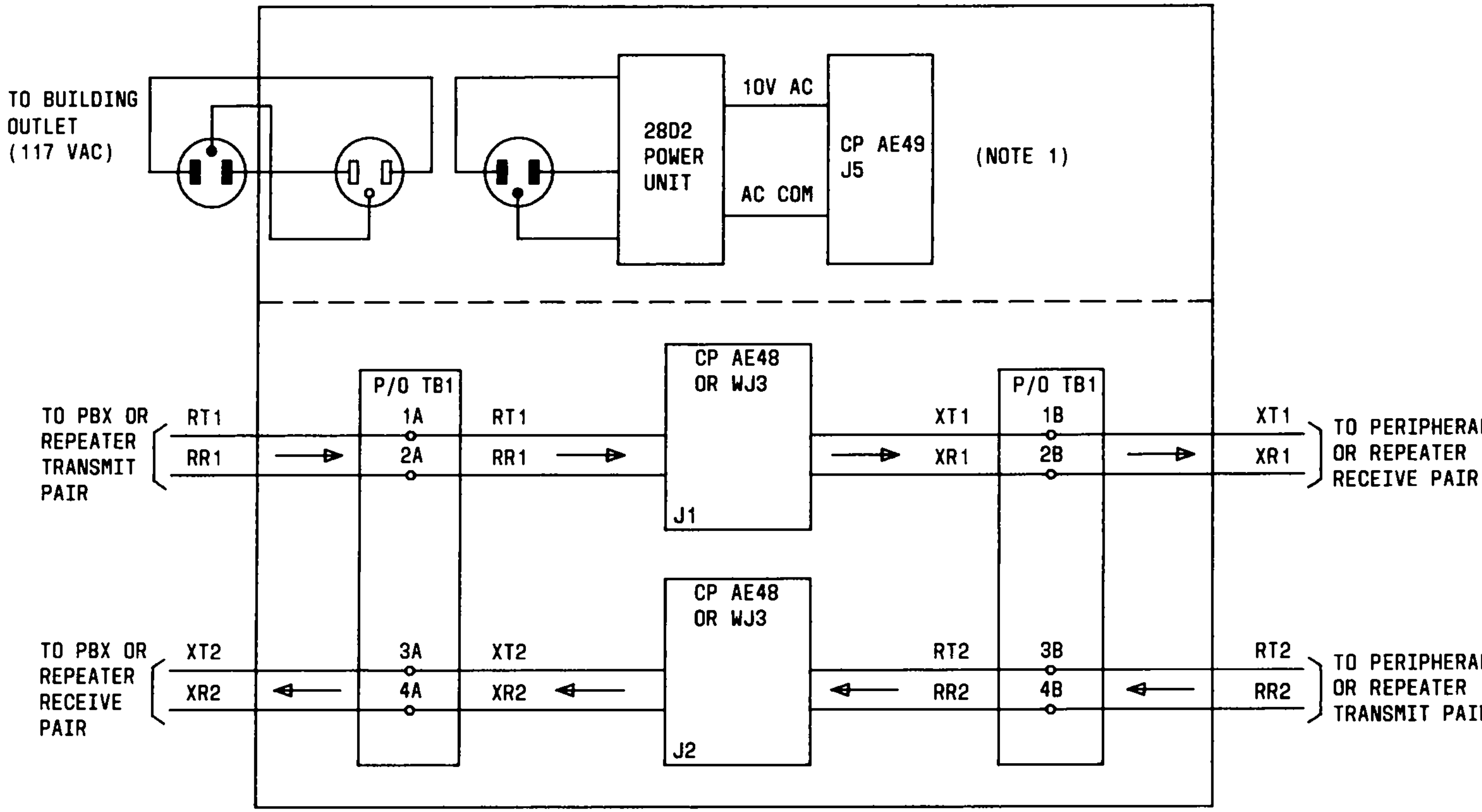
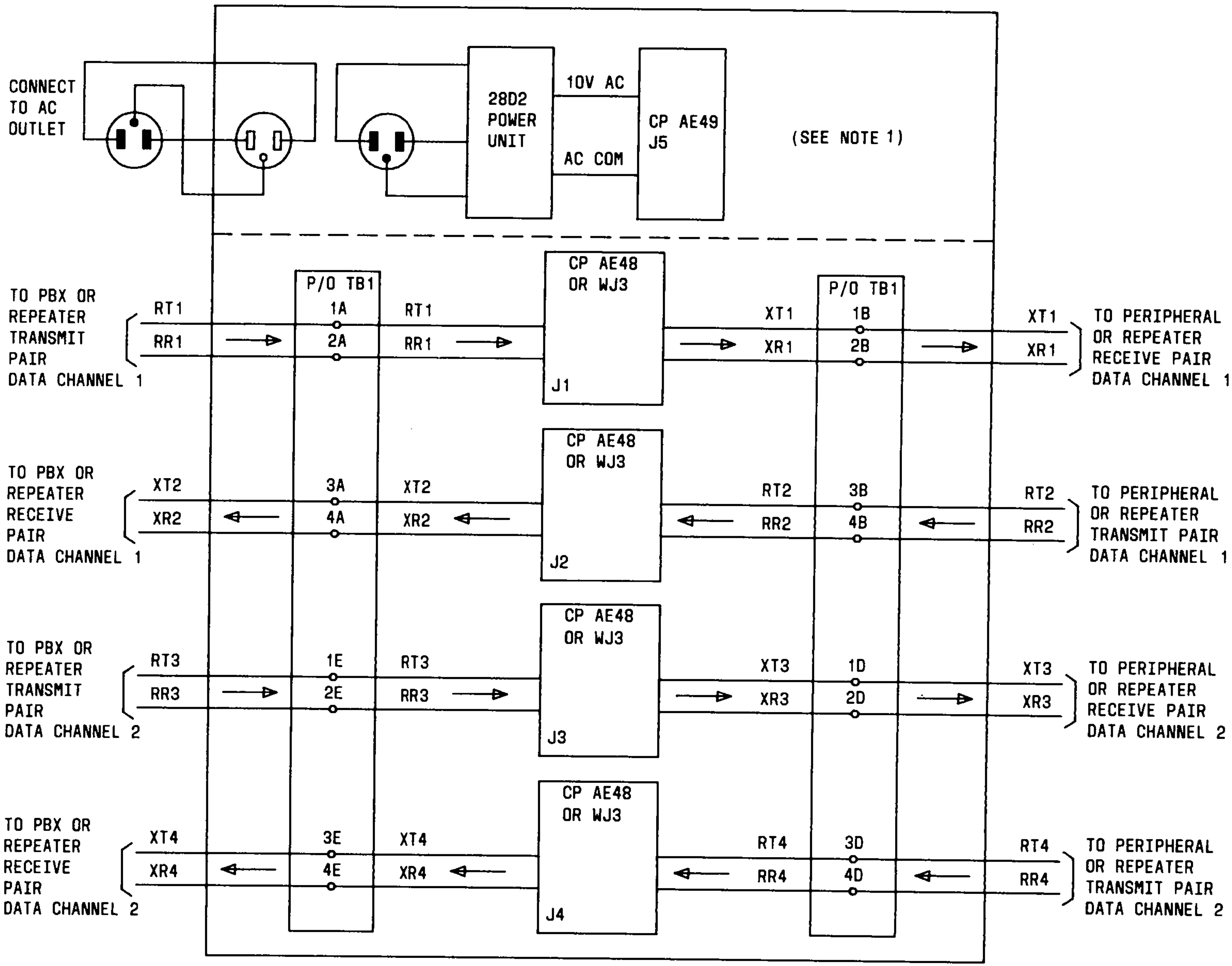


Fig. 22—Calling Number Display (102D1-A)—Write Command



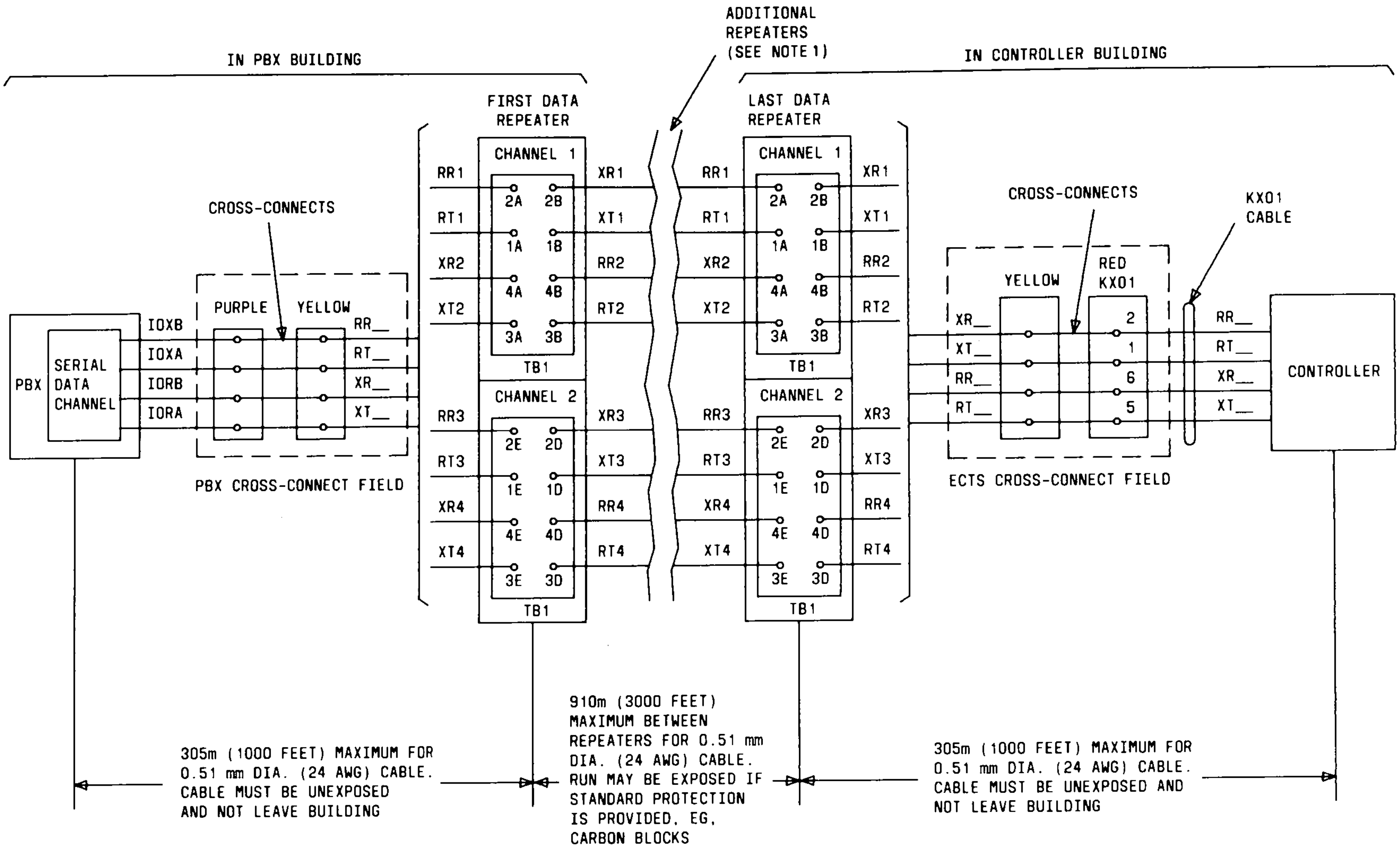
NOTE:
1. THE POWER SUPPLY UNIT AND CP AE49 ARE NOT REQUIRED WHEN THE WJ3 CIRCUIT IS USED.

Fig. 23—Single Channel Repeater With Range Extension (AE48) or Range Extension (WJ3)



NOTE:
1. THE POWER SUPPLY UNIT AND AE49 CIRCUIT PACK ARE NOT REQUIRED WHEN THE WJ3 CIRCUIT CARD IS USED

Fig. 24—Dual Channel Repeater With Range Extension (AE48) or Without Range Extension (WJ3)



NOTE:

1. ADDITIONAL CASCADED REPEATERS MAY BE ADDED TO EXTEND THE TOTAL DISTANCE BETWEEN PBX AND CONTROLLER TO 3350m (11,000 FEET).

Fig. 25—Data Channel Repeater Connection

TABLE J

DISTANCE CHANGE PER WIRE SIZE

WIRE SIZE		DISTANCE		PERCENT CHANGE
DIAMETER	AWG	METERS	FEET	
0.40 mm	26	731	2400	−20
0.51 mm	24	914	3000	0
0.64 mm	22	1097	3600	+20
0.91 mm	19	1463	4800	+60

an application at the maximum range of 1525 meters (5000 feet), 3050 meters (10,000 feet) of cable is used, resulting in a cable propagation delay of 17 microseconds.

8.16 Additional elements in the data response time are:

- Time to shift out the data (92 microseconds)
- Time required by the peripheral to respond to each bit (approximately 2 microseconds)
- Time for the PBX receiver to respond (1 microsecond).

ATTENDANT CONSOLE REPEATER

8.17 The attendant console repeater unit provides range extension and lightning protection for the DIMENSION PBX low-speed attendant console data channels. Power of 48 volts, ground, and alarm leads are provided for the console repeater. The repeater is connected in series with the attendant console data link to repeat data pulses and to provide isolation between input and output pairs. The repeater may be used to provide range extension for a remote location. Where lightning protection is required but range extension is not provided, console repeaters may be used to couple the PBX and console over a distance not to exceed 305 meters (1000 feet).

8.18 The repeater detects and reconstructs incoming modified bi-phase (bipolar) data pulses to eliminate any pulse attenuation or distortion as well as to increase data channel range.

8.19 The repeater circuit is designed to operate in unexposed environments without additional protection or in exposed environments with standard protection.

8.20 Each attendant console data channel consists of two data pairs, one for data transmission from the PBX to the console and the other pair for data response from the console to the PBX. Circuit pack WJ5, List 6, is used only in the repeater at the PBX end. Circuit pack WJ4, List 4, and a power supply unit 284B1, List 7, are used only in the repeater at the console end. These circuit packs are not required in the intermediate cascaded repeaters, but the terminals on the connecting block for the alarm, -48 volt and ground leads, must be strapped to allow a continuous path from the PBX to console. The strapping is required from terminals 11B to 11D, 12B to 12D, and 15B through 50B to 15D through 50D. Whenever an attendant console is located in a different building than the PBX, attendant console repeaters must be used.

A. Repeaters With Range Extension

8.21 When the distance between the PBX and an attendant console is more than 305 meters (1000 feet) but not more than 3350 meters (11,000 feet), each repeater must be equipped with two AE48 circuit packs and one AE49 circuit pack. Figures 26, 27, and 28 provide functional block diagrams and show connections when range extension is required.

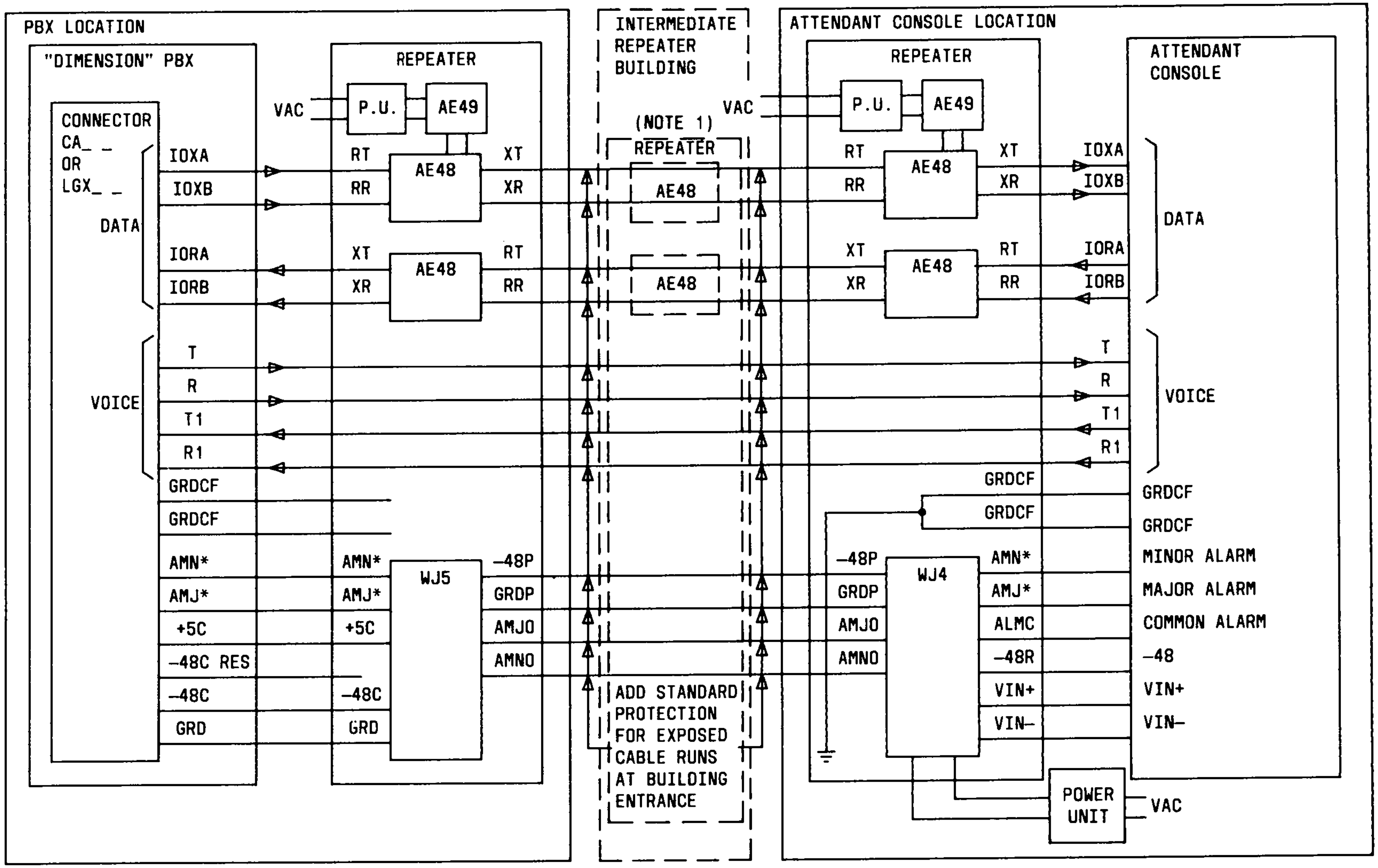
8.22 Use of the attendant console repeater to extend the range of a console beyond 305 meters (1000 feet) requires the button scan response time be 160 microseconds.

> ***Note:*** If propagation delay exceeds the maximum button scan response time provided by the generic, problems with range extension may be encountered.

Receiver Circuit Operation

8.23 Incoming data pulses are transformer-coupled into the receiver circuit. The receiver circuit compares the signal amplitude with a threshold level and produces active low outputs whenever the signal level is greater than the threshold level.

8.24 The threshold level is automatically set to one-half the peak-to-peak signal amplitude. This feature allows the receiver circuit to operate with a large variation of cable distances, types, and parameters without manual compensation.



305m (1000 FT) MAX FOR 0.51 mm DIA. (24AWG) CABLE. CABLE RUN MUST BE UNEXPOSED AND MAY NOT LEAVE THE BUILDING

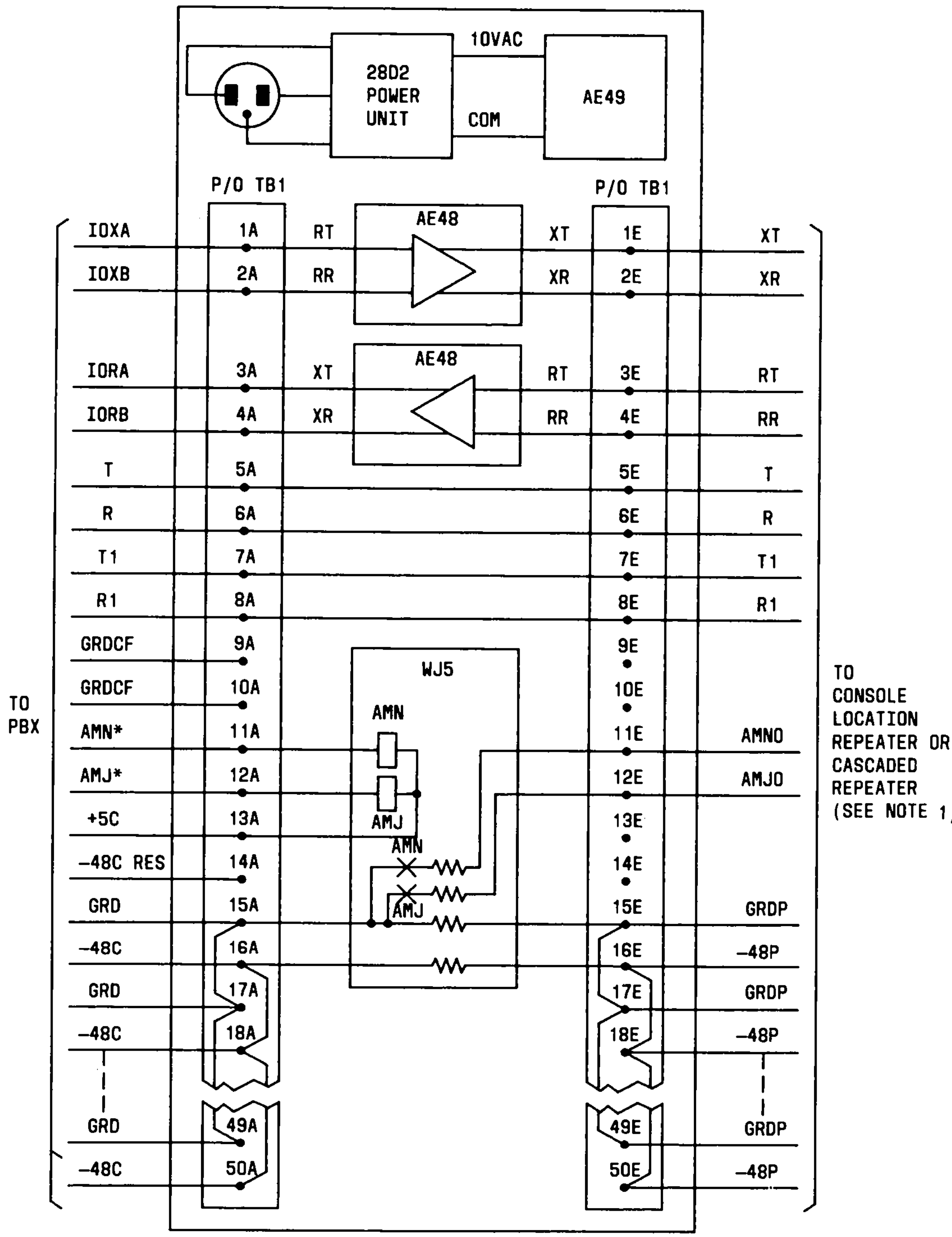
910m (3000 FT) MAX FOR 0.51 mm DIA. (24AWG) CABLE BETWEEN REPEATERS CABLE RUN MAY BE EXPOSED IF STANDARD PROTECTION IS PROVIDED

305m (1000 FT) MAX FOR 0.51 mm DIA. (24AWG) CABLE. CABLE RUN MUST BE UNEXPOSED AND MAY NOT LEAVE THE BUILDING

NOTE:

1. TWO INTERMEDIATE REPEATERS CAN BE CASCADED BETWEEN THE PBX REPEATER AND THE CONSOLE REPEATER ALLOWING A TOTAL DISTANCE OF 3350m (11,000 FEET) BETWEEN CONSOLE AND PBX.

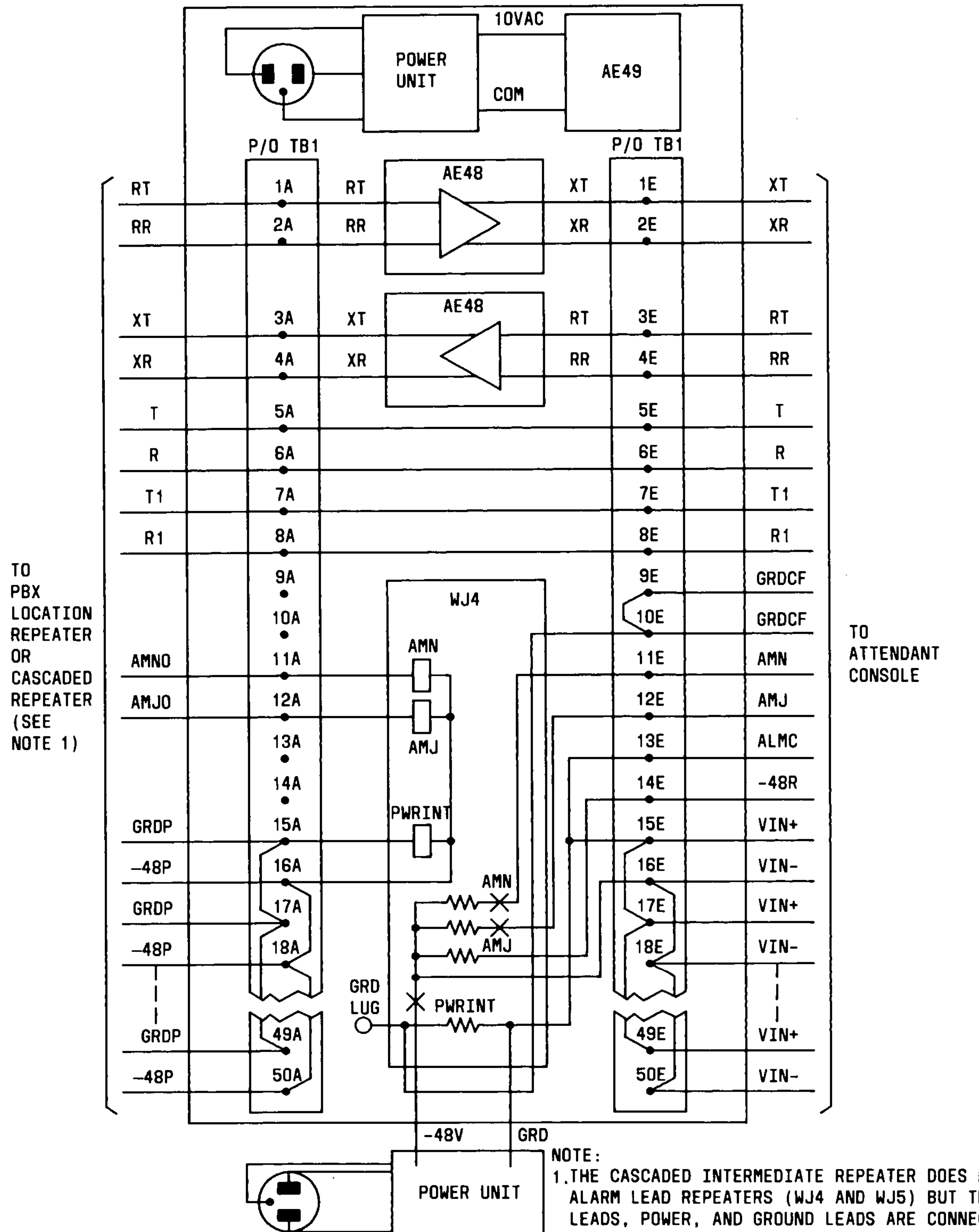
Fig. 26—Attendant Console Repeater With Range Extension



NOTE:

1. THE CASCADED INTERMEDIATE REPEATER DOES NOT REQUIRE ALARM LEAD REPEATERS (CPWJ4 AND CPWJ5) BUT THE ALARM LEADS, POWER AND GROUND LEADS ARE CONNECTED TO APPROPRIATE TERMINALS WITH STRAPPING FROM TERMINALS 11B TO 11D, 12B TO 12D, AND 15B THROUGH 50B TO 15D THROUGH 50D, RESPECTIVELY, ON THE INTERMEDIATE REPEATERS.

Fig. 27—Attendant Console Repeaters With Range Extension—PBX End



NOTE:
1. THE CASCADED INTERMEDIATE REPEATER DOES NOT REQUIRE ALARM LEAD REPEATERS (WJ4 AND WJ5) BUT THE ALARM LEADS, POWER, AND GROUND LEADS ARE CONNECTED TO APPROPRIATE TERMINALS WITH STRAPPING FROM TERMINALS 11B TO 11D, 12B TO 12D, AND 15B THROUGH 50B TO 15D THROUGH 50D RESPECTIVELY ON THE INTERMEDIATE REPEATERS

Fig. 28—Attendant Console Repeaters With Range Extension—Console End

Control Circuit Operation

8.25 The control circuit checks the receiver outputs and generates the timing for the transmit circuit. A 300-nanoseconds timing reference is supplied by the AE-49 rectifier and timing reference card via the 3.33-MHz clock signal.

8.26 The control circuit requires both polarities of the bi-phase pulse to be detected within 2.1 microseconds. If only a single pulse is detected, the control circuit inhibits the transmit circuit for the duration of the pulse. This feature allows the repeater to block noise hits.

Transmit Circuit Operation

8.27 The transmit circuit generates modified bi-phase output pulses. The output pulse amplitude is 5 volts; the pulse width is 1.2 microseconds for each polarity. A minimum dead time of 2.4 microseconds is forced by the control circuit.

B. Repeaters Without Range Extension

8.28 When a console is located in a different building than the PBX and range extension is not required because the console is within 305 meters (1000 feet) of the PBX, each repeater unit must be equipped with two WJ3 buffer circuit packs. Each circuit pack provides a single-direction data link buffer which protects the PBX and attendant console from surges due to lightning hits. Figures 29, 30, and 31 provide functional block diagrams and show connections when range extension is not required.

C. Extension of Alarms

8.29 The PBX-end repeater unit must be equipped with a WJ5 circuit pack, and the console-end repeater unit must be equipped with a WJ4 circuit pack. These circuit packs provide extension of alarm leads to the console and isolate the console from the PBX circuitry.

8.30 Power and ground leads from the PBX are routed through the WJ5 circuit pack (Fig. 27 and 30) and any intermediate repeaters to the WJ4 circuit pack in the console-end repeater unit (Fig. 28 and 31). A relay on the WJ4 is energized by the PBX power leads and connects the remote console to the 284B1 power unit in the console-end repeater. If power from the PBX should fail, the relay is de-energized and the console is disconnected from the 284B1 power unit.

8.31 The major alarm (AMJ*) and minor alarm (AMN*) leads from the PBX are connected to independent relays in the WJ5 circuit pack (Fig. 27 and 29). If an alarm lead goes low (ie, an alarm is present), the relay associated with that alarm lead is energized and causes a contact closure. This closure applies power to a second relay on the WJ4 circuit pack (Fig. 28 and 31). The contacts associated with this second relay close and pass the alarm to the appropriate indicator lamp on the attendant console.

D. Data Range

8.32 Data link range is a function of cable attenuation and receiver sensitivity. The repeater-to-repeater range is 910 meters (3000 feet) for 0.51 millimeter diameter (No. 24 AWG) cable. The PBX-to-repeater and repeater-to-attendant consoles are limited to 305 meters (1000-foot) range by receiver sensitivity.

8.33 The data range is limited by the cable attenuation and round trip propagation delay. The cable attenuation is a function of the cable type and temperature.

E. Propagation Delay

8.34 The maximum data range is limited in software by the time allowed for a data channel response. Range extension increases the data response time due to repeater delay and cable propagation.

8.35 Each unidirectional repeater has a 2.4 microseconds delay. In an application employing two repeaters, a total of four repeater circuits delay is inserted in the loop for a total delay of 9.6 microseconds.

8.36 The cable propagation delay is approximately 1.7 microseconds per 305 meters (1000 feet). At the maximum range from PBX to attendant console of 1520 meters (5000 feet), 3050 meters (10,000 feet) of cable is used, resulting in a cable propagation delay of 17 microseconds.

9. INPUT/OUTPUT (I/O) MAINTENANCE FUNCTION

9.01 An I/O maintenance function permits the processor to isolate trouble between the data

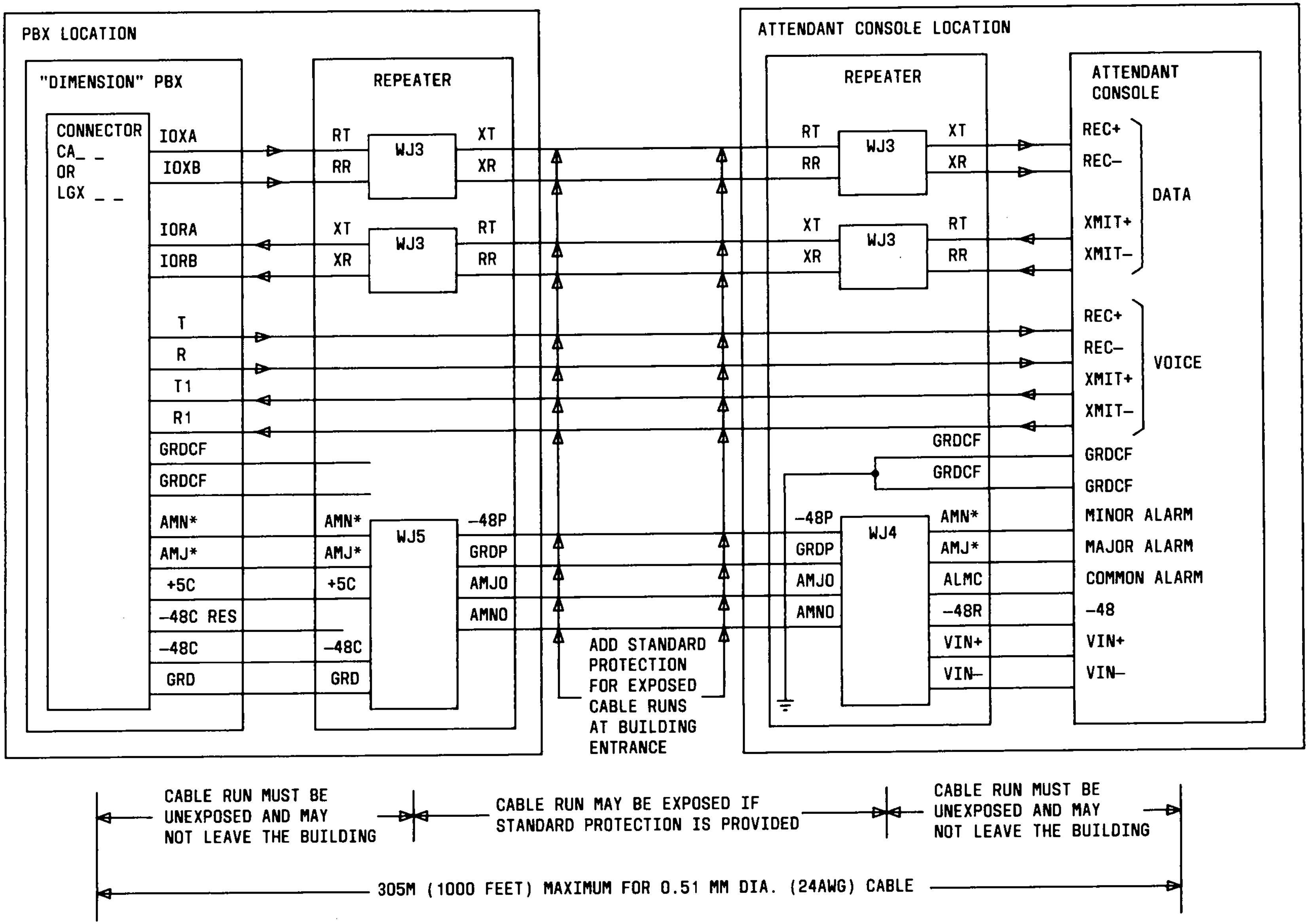


Fig. 29—Attendant Console Repeater Without Range Extension

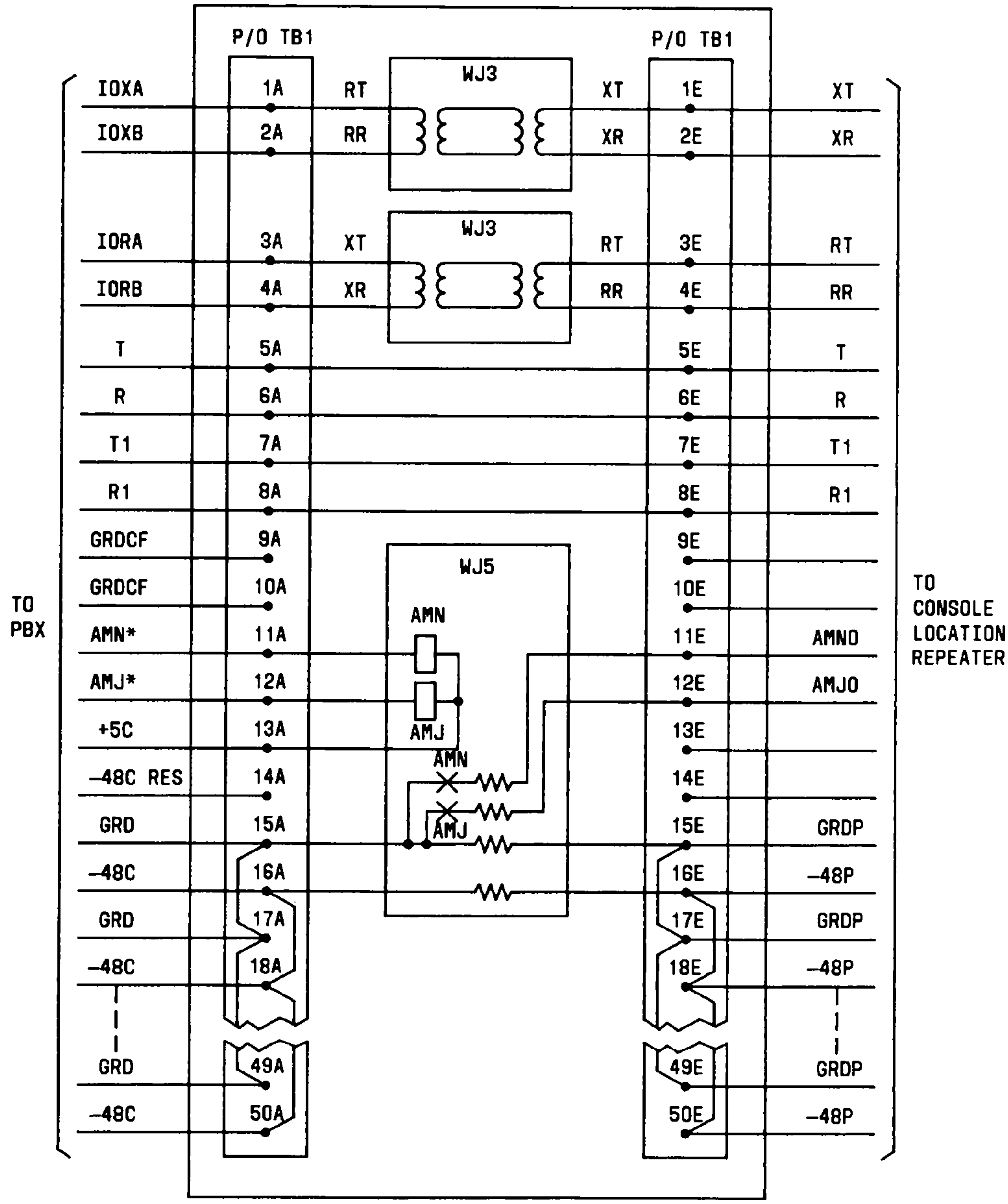


Fig. 30—Attendant Console Repeater Without Range Extension—PBX End

channel and the peripheral device. The function is performed by checking the receive and transmit capability of the data channel.

LOOP TEST

9.02 An I/O loop test conditions the channel for checking. The test permits information from the data bus to be parallel-loaded into the transmit register and shifted through the I/O receiver into the receive register. An active read command gates the information from the receive register to the processor for error checking.

A. Active Loop Test

9.03 To initiate the data channel loop test, the processor places the address of the loop test cir-

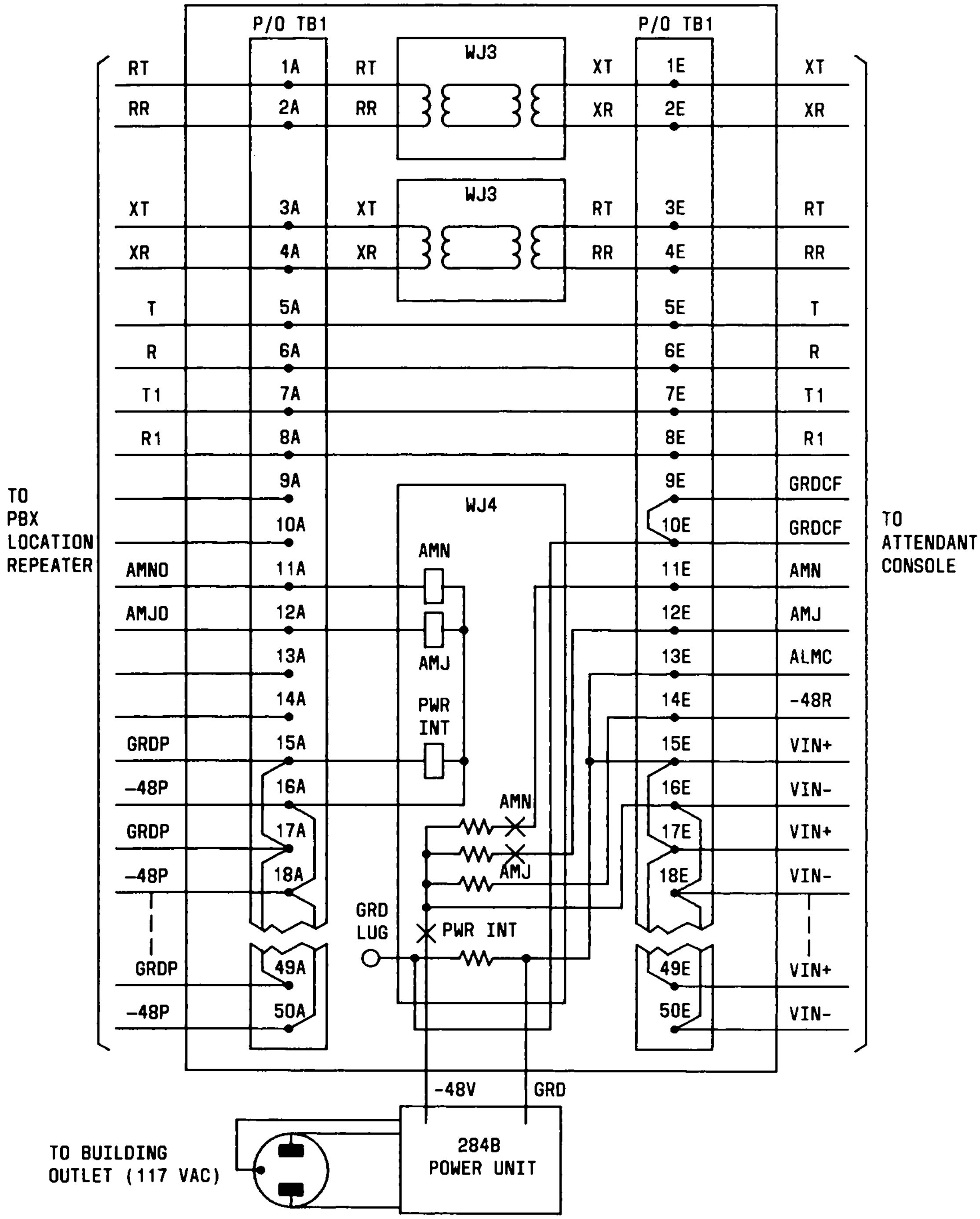


Fig. 31—Attendant Console Repeater Without Range Extension—Console End

cuit (see Table A) on the main address bus, a low on the control bus write I/O (WROP*) lead, and a low on the main data bus (MD00*) lead.

9.04 The information on the address bus is interpreted by the I/O address decoder (Fig. 32) to generate a low on (IOELT*) lead and a high on the read/write enable (RWE) lead.

9.05 The low I/O enable loop test signal partially enables the I/O loop test circuit and causes the read/write control circuit to generate a low on the I/O done (IODN*) lead. The low I/O done signal informs the processor that the address information has been received and decoded.

9.06 The high read/write enable (RWE) signal, together with the active write I/O (WRIO*) signal, generates a low on the data link write (DLWRI*) lead. This lead enables the I/O loop test circuit. The enabled loop test circuit decodes the low on the main data bus (MD00*) lead to generate a low loop test (LTST*) signal. This signal is directed to all I/O data channels; however, only the enabled channel responds to the signal.

9.07 The processor may deactivate the loop test by directing a write command to the circuit with a high on the main data bus (MD00*) lead. The high data signal removes the active loop test (LTST*) signal from the data channels.

9.08 The processor may also determine the status of the loop test signal by directing a read command to the loop test circuit. The command is interpreted by the address decoder and the read/write control to generate a low on the data link read (DLRD*) lead (Fig. 32). The I/O loop test circuit responds to the low read signal as follows:

MD00*	INDICATION
0	LTST* Signal is active
1	LTST* Signal is inactive

B. Data Channel Response to Loop Test

9.09 Each data channel responds the same to the active loop test signal when enabled. To enable the channel, the processor initiates a write command. The command is decoded and directed to the desired channel as previously described with a test word present on the data bus leads.

9.10 The data channel responds to the input signals to generate a high on the write gate (WTG) lead (Fig. 32). The timing and control circuit responds to the high write gate signal and the input clock (CLKS or CLKF) signal to generate a high on the write initiate (WTI) lead. The high write initiate signal conditions the transmit register to parallel-load the data from the data bus (MD00* through MD16*) leads. The transmit clock (XT) signal loads the test word into the register.

9.11 When the register is loaded, the processor removes the write command (places a high on the WRIO* lead). The timing and control circuit responds with a low on the write initiate (WTI) lead which conditions the transmit register to serial shift data. The transmit clock (XT) signal shifts the data to the I/O receiver via the transmit data (XDATA) leads.

9.12 The I/O receiver responds to the active loop test (LPTST*) signal and the transmit loop clock (XLC) signal to shift the data through the I/O receiver.

9.13 The I/O receiver converts the transmit loop clock signal to receive clock (RCVC) signal to shift the data into the receive register via the receive data (RD) lead. The information is retained in the register, until overwritten by new data, to be read by the processor.

9.14 The processor issues a read command to the selected data channel to complete the loop test. The command signals are decoded by the I/O buffer and directed to the channel. The timing and control circuit decodes the signal to generate a high on the read initiate (RDI) lead. The high read initiate signal gates the information from the receive register to the processor via the data (MD00* through MD16*) leads. The processor compares the data with the transmitted test word to isolate the trouble to the data channel or beyond to the peripheral device.

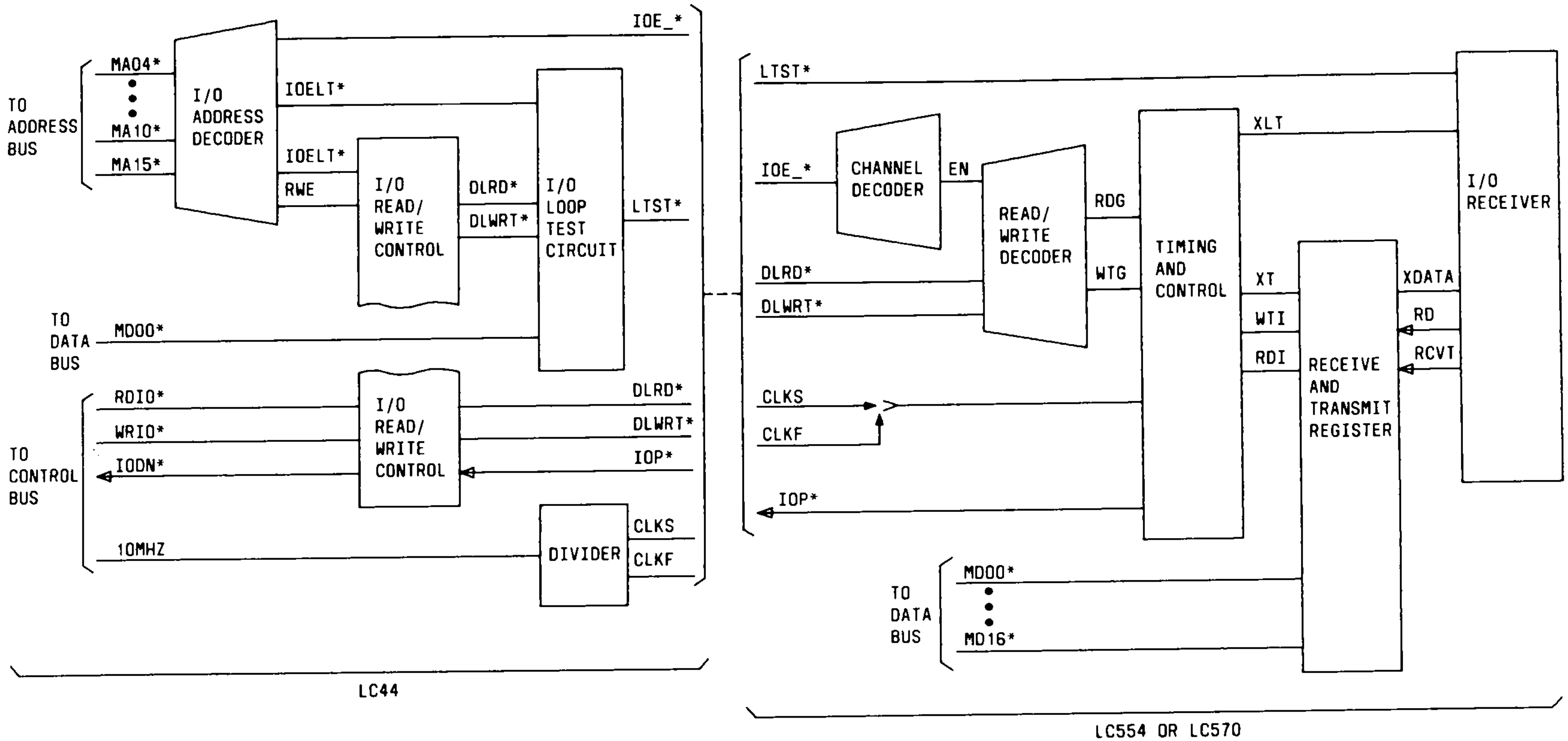


Fig. 32—Read and Write Command for I/O Loop Test