

COMMUNICATIONS DISPLAY TERMINAL (CDT)
CDIF814 STATION CONTROLLER INTERFACE MODULE
DESCRIPTION AND PRINCIPLES OF OPERATION

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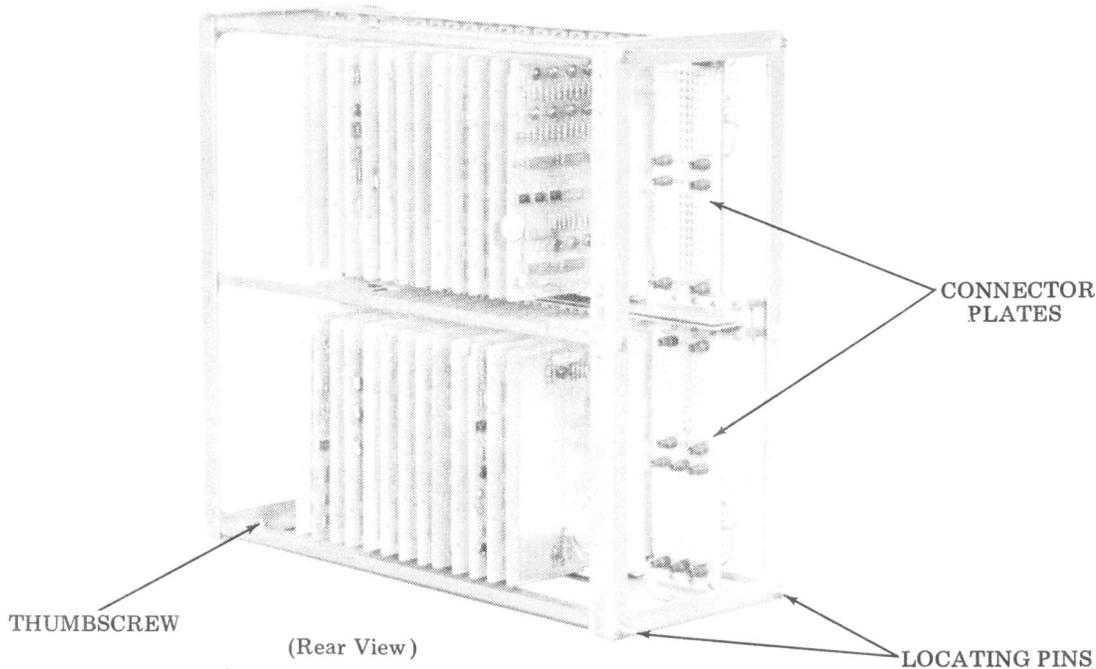


Figure 1 - CDIF814 Station Controller Module

1. GENERAL

1.01 This section provides a general description and principles of operation for the Communications Display Station Controller Interface module, CDIF814, shown in Figure 1.

1.02 Issue 1 of this section was a limited printing edition and was not made available nor generally distributed on a system wide basis. The reissuance of this section deletes information for the CDIF811 module which was factory discontinued. This issue incorporates later engineering information for the CDIF814 station controller module; hereafter, referred to as station controller.

1.03 Marginal arrows have been omitted from this section because this issue is a general revision and represents the first standard printing edition available for general Bell System distribution. Teletype change notice (TCN) information has been incorporated into this section, where applicable, up to the time of this printing.

1.04 The electronic circuitry of the station controller is contained on plug-in type logic circuits and their receptacles mounted within an open type metal frame that is designed for mounting into a communications display terminal (CDT) cabinet, or into the series 2540

independent buffer storage set cabinetry. No special tools or skills are needed to complete its installation. In the installed position, the module is fastened to a pull-out type shelf in the lower area of the CDT set cabinet. In the buffer storage set, it is mounted vertically on a spring loaded pull-up type rack that may be locked into either up or down positions. The module is installed to the shelf or vertical rack by means of two locating pins and a thumbscrew.

1.05 Since the station controller is a self-contained device, it only requires a dc power source for operation. All installations of the module into CDT devices, requires that the CDT set have an additional CDPS802 low voltage power supply to power the station controller. Series 2540 buffer sets are equipped with a low voltage power supply that supplies power to operate internally mounted interface and buffer modules; therefore, no other power source is necessary.

1.06 Use of the station controller is not restricted to only the series 2500 communications display terminals. It can be used with any medium speed send/receive (S/R) data terminal, or equivalent display terminal, provided that the data terminal S/R interface is equivalent and compatible to Teletype® parallel terminal interface (PTI) requirements.

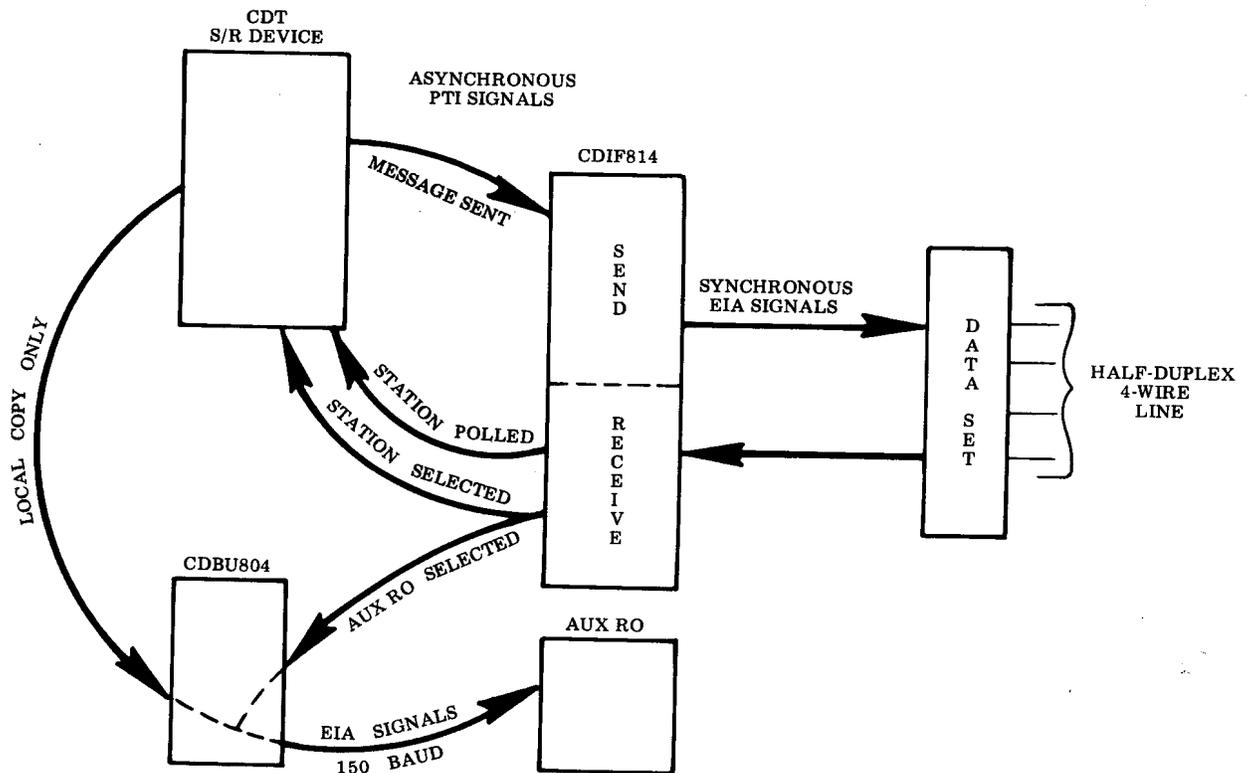


Figure 2 - Typical Station Arrangement With Optional RO Device

1.07 The solid state medium scale integrated circuitry in the station controller provides a local visual display S/R device with station control, error control and detection capabilities, and a S/R EIA (Electronics Industries Association) Standard RS-232-C interface for connecting a data set. It also provides an additional PTI interface for connection of an auxiliary receive-only (RO) hard copy print-out device. The auxiliary RO device can be conditioned to receive data locally from the visual display S/R device, or it can be activated to receive from a distant sender over the primary data channel.

Station Arrangement

1.08 Figure 2 illustrates a S/R device with optional connection of an auxiliary RO device with the station controller. The data set interface with the station controller provides the station controller a communications link into the 4-wire, alternate (half-duplex) 2-way data channel. Interface signals exchanged between the data set and station controller, and between the auxiliary RO hard copy device and its character buffer unit, are in serialized bipolar voltage form (EIA). Signals exchanged between the S/R device,

and between the character buffer unit and station controller are in PTI form.

1.09 When installed between the primary data channel and the S/R device, and auxiliary RO device that comprise the station, the station controller recognizes receipt of a poll sender, select receiver, or select auxiliary receiver address character sequences unique to its station and devices. It responds to receipt of these sequences according to the sending or receiving status of the devices.

1.10 The external clock signal derived in the 201B3 Data Set determines the on-line receive or transmit operating speed of the station controller. During on-line operation, the station controller is dependent upon the data set clock signal to load synchronous data received from the data line, or data to be transmitted synchronously from the station controller to the line. The 201 series data set clock signal occurs at a rate of 2400 bits per second. Since the synchronous character frame consists of eight data bit levels, this results in a line speed of 3000 words per minute (300 cycles per second).

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1.11 The maximum operating speed of the controller, determined by receipt of an external clock signal, is 3000 words per minute (2400 bits per second).

1.12 On the device interface of the controller is a multiwire hookup consisting of PTI signal drivers and a PTI signal terminator. Signaling between the devices and the controller is asynchronous, character by character. Data transfer from either a send or a receive device is under control of the station controller at all times.

System Applications

1.13 A brief overall system description is provided at various locations in this section, in order to explain signal interchange with the station controller, the S/R devices, and distant computer terminal.

1.14 Figure 3 illustrates a typical multistation arrangement to a computer control station. The main control station could consist of a Bell System, or equivalent customer-provided computer control station (CCS). Hereafter, references to the computer control station will be abbreviated to CCS. A station arrangement could consist of a CDIF814 station controller, data set, and peripheral devices, or equivalent devices that share the communications channel.

1.15 In multipoint station arrangements, the computer control station actively supervises and controls which station device has use of the primary data channel at all times. A station controller, only when properly addressed, links its send or receive device to the communications channel, and establishes character framing (synchronization) with the computer control station prior to allowing data exchange.

1.16 During data exchange all message traffic passes between the CCS and the addressed station controller S/R device. Only one device is permitted to send or receive data over the shared data channel. Other stations, not addressed by the CCS, ignore the data. Therefore, outlying station devices do not directly exchange data information.

1.17 Each station controller S/R device is addressed and given access to the primary data channel either sequentially or in random sequence depending upon the data traffic load and programming at the CCS. If the addressed device is not ready for operation, or is temporarily out-of-service, the station controller generates the appropriate negative response to the CCS. The CCS will then remain idle or if it has additional traffic, it will continue to poll or select other stations.

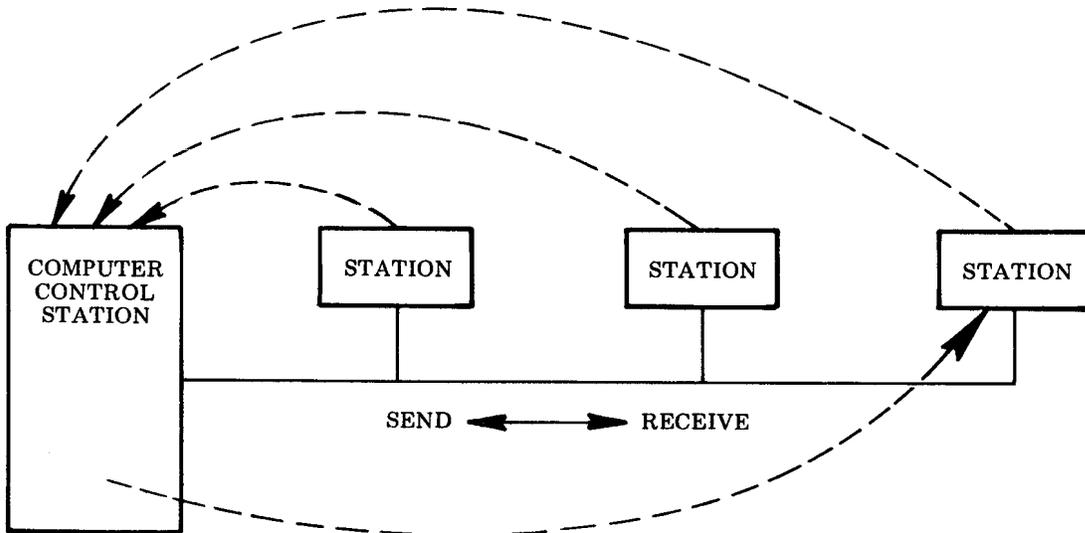


Figure 3 - Typical Multipoint Station Arrangement

2. DESCRIPTION

2.01 The station controller is essentially an input/output device controlled by the CCS. Its device control capabilities are as follows:

- Station Identification Detection and Generation
- Device Input/Output Interface
- Data Set Input/Output Interface
- Data Deserializing and Synchronizing
- Data Serializing and Format Generation
- Local Data Transfer between Send Device and one of the two Receive Devices
- Error Checking and Control

TECHNICAL DATA

A. Physical Characteristics

2.02 Dimensions and Weight (approximate):

Height14 inches
Width	6 inches
Depth14-1/2 inches
Weight	15 pounds

B. Electrical Characteristics

2.03 The input voltage necessary to operate the module under full current load are as follows (at 70 degrees F ambient):

+5 volts dc	+0.5 volts at 3.00 amperes
+12 volts dc	+1.2 volts at 1.00 ampere
-12 volts dc	+1.2 volts at 0.10 ampere

Total dc power consumption is 29 watts.

2.04 The station controller electronic logic may be operated in an environment of 10 to 90 percent relative humidity at a temperature of 40 degrees to 110 degrees F.

SIGNAL INTERFACE

A. Data Set

2.05 Serial input/output signaling from the station controller to a data set or equivalent telephone line modem, consist of synchronous serialized ASCII (American National Standard Code for Information Interchange) signals in accordance to EIA Standard RS-232-C.

2.06 When a 201B3 Data Set is used as the data line facility, the station controller will receive or transmit under control of the data set external clock signal at a maximum speed of 3000 words per minute (2400 bits per second).

Additional information for the Bell System data set can be referenced in Section 592-012-102. Data set installation information can be referenced in Section 592-011-201.

2.07 Data transmission and reception from the station controller's S/R interface toward the communications facility (data set) conforms to the 7-level ASCII (X3.4-1968). Signaling (data exchange) is synchronous by bit and character using odd parity and in conformance to EIA Standard RS-232-C. Operation of the station controller is on a nonsimultaneous (half-duplex) arrangement, but requires that the data line facility be a 4-wire arrangement.

2.08 Data signals and control interface signals between the data set and station controller are shown in Figure 4.

2.09 Data bit level signaling between the data set and station controller on the Transmitted Data and Received Data interface is considered a space data bit ("0" state) when the voltage level is between +3 to +25 volts dc. A mark data bit (1 state) is when the voltage level is between -3 to -25 volts dc.

2.10 Message control signals between the data set and station controller are considered on (1 state) when the signal voltage potential is between +3 volts to +25 volts dc. It is considered off when the potential is between -3 volts to -25 volts.

Message Control

2.11 The following, 2.12 through 2.20, provide a description of message control signals between the data set and station controller. These signals are exchanged for the purpose of establishing and maintaining received or transmitted data synchronism to the line and also for definitions of various degrees of readiness.

2.12 Data Carrier Detect (CF) — DIRECTION: Data Set to Station Controller. When on, CF signal indicates that the data set is receiving a carrier signal from the distant or remote computer control station transmitter data set. The data carrier detect signal is passed to the station controller and conditions its logic for receive operation (looking for SYN characters), if ready to receive. Since this is a 4-wire private line operation the data carrier detect signal remains on at all times. The station controller generates answer-back sequences to poll sender or select receiver inquiries. CF is held off for a brief period of time following all on/off transitions.

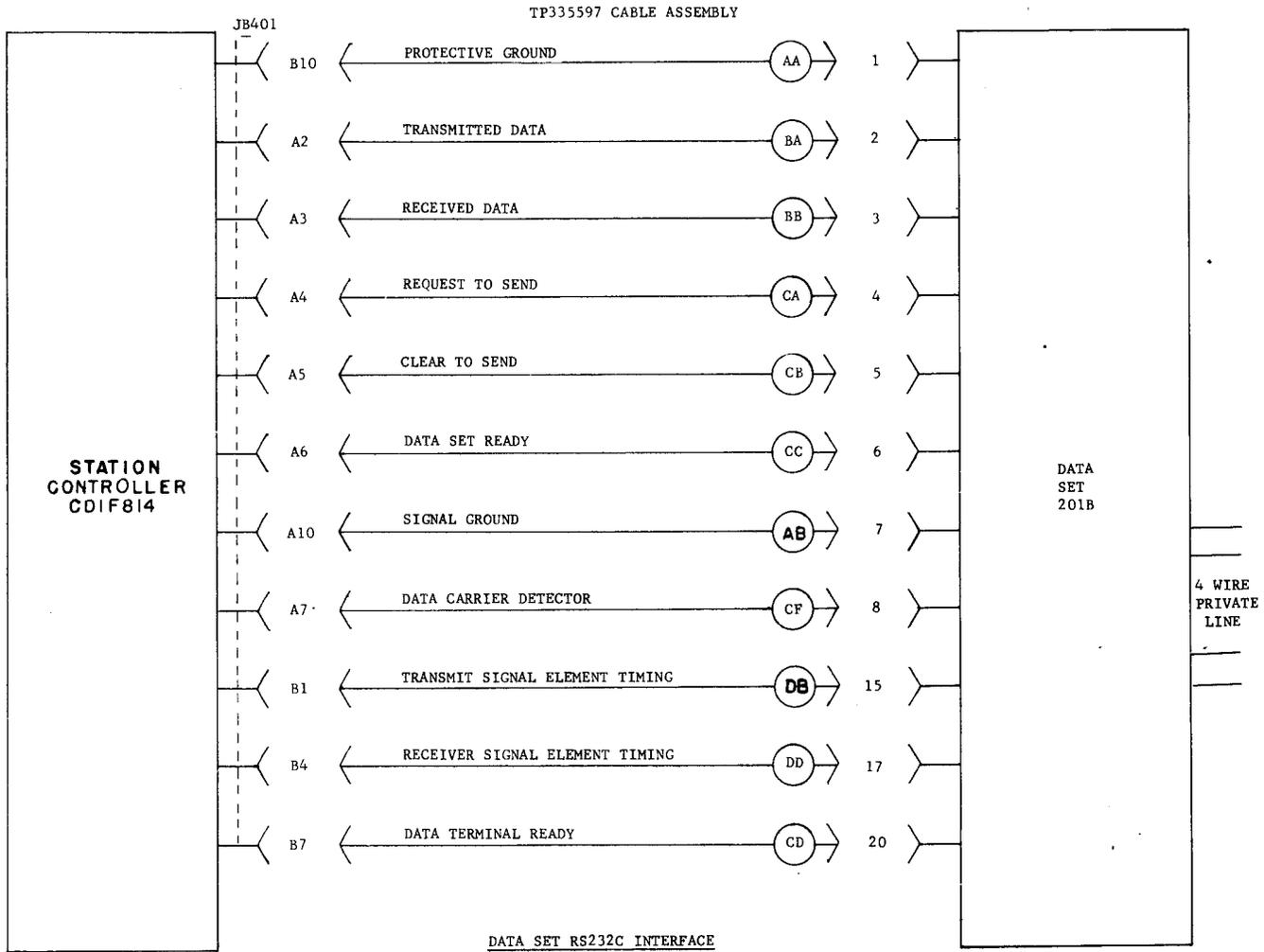


Figure 4 - Data Set Interface

2.13 Data Set Ready (CC) — DIRECTION: Data Set to Station Controller. A positive potential (ON) on this lead to the station controller informs it that the data set is in data mode and is capable of either sending or receiving. If the data set is not in the data mode, the data set ready (DSR) will be off (low state). In this application with the station controller, DSR signal is always on (high state) to the station controller unless power failure or interface disconnect occurs.

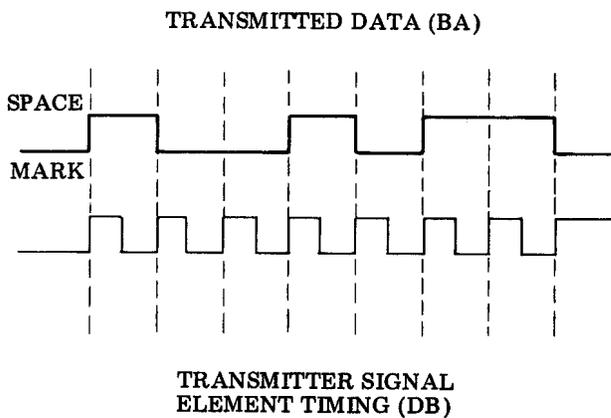
2.14 Data Terminal Ready (CD) — DIRECTION: Station Controller to Data Set. A positive potential is placed on this lead to the data set if the station controller sees that data set ready (DSR) is on. DTR on signal places the data set into data mode. Under normal operation in a multipoint access system, the station controller

generates a DTR on signal to the data set at all times, except for loss of interface connection.

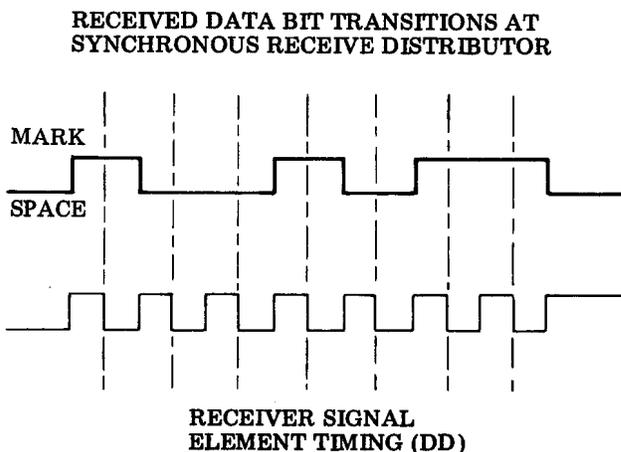
2.15 Receiver Signal Element Timing (DD) — DIRECTION: Data Set to Station Controller. Receiver signal element timing (DD) clock signal originates in the 201B3 Data Set and consists of a square waveform clock signal at a frequency of 2400 hertz. The external clock signal synchronizes received data (BB) and causes it to load into the station controller synchronous receive distributor. The off to on transition, positive going transition, of the clock signal (DD) occurs at the same time of mark or space bit transitions on the incoming received data (BB) line. The receiver signal element timing clock signal (DD) signal transition from on to off indicates the approximate center of each received signal bit and is used to clock (sample) the bit

information into the station controller synchronous receive distributor.

2.16 Transmitted Data (BA) — DIRECTION: Station Controller to Data Set. Serial data bit information from the station controller transmit distributor is carried by this lead to the data set transmit modulator. Synchronous serial bit transitions (BA) only occur on the positive transition of the transmitter signal element timing (DB) signal furnished by the data set. Serialized data bit transitions are in phase with positive timing signal transitions. In idle condition, the transmitted data lead is held marking (negative).



2.17 Received Data (BB) — DIRECTION: Data Set to Station Controller. Synchronous serial data bit information from the 201B3 Data Set is carried by this lead to the station controller synchronous receive distributor. Serial data bit transitions occur at 2400 bits per second and are in phase with the positive transition of the receiver signal element timing (DD) pulse. In the idle condition this input is held marking (negative potential).



2.18 Transmitter Signal Element Timing (DB) — DIRECTION: Data Set to Station Controller. Transmit signal element timing (DB) originates in the 201B3 Data Set and consists of a square waveform clock signal at a frequency of 2400 hertz. The signal element timing signal synchronizes the transmit data bit information (BA) causing it to unload from the station controller transmit distributor to the data set for transmission. All data bit information signal transitions occur at the positive transition of the clock signal. Transmit signal element timing (DB) signal is always present.

2.19 Request to Send (CA) — DIRECTION: Station Controller to Data Set. If the station controller S/R device does not have a message for transmission (idle state), the request to send (RTS) signal to the data set is held at a negative voltage for off condition. When the S/R device has a message for transmission, and is conditioned for transmit, the station controller upon detection of a polling sequence places a positive voltage on CA signal (on condition). CA signal, in on condition, causes the data set to send carrier signal over the primary data channel to the remote CCS data set. At the conclusion of the message transmission, the station controller turns CA signal off. Sufficient delay in turn-OFF is allowed in the station controller to assure the last character was completely transmitted by the data set.

2.20 Clear to Send (CB) — DIRECTION: Data Set to S/R Device Station Controller. When the sending device has a message for transmission, it signals the station controller to turn on the request to send signal (CA) to the data set. Receipt of this signal starts the data set oscillator and immediately places carrier signal on the line to the distant receiving data set. Before the data set signals the station controller, it is conditioned to transmit by returning the clear to send (CB) signal, a programmed time delay of eight and one-half milliseconds occurs. Delay of CA signal is an option provided in the type 201 Data Set. The clear to send (CB) lead is turned off (negative state-idle) when the station controller request to send (CA) signal is off.

2.21 Protective Ground (AA) and Signal Ground (AB) are conductors on the interface that are interconnected within the data set power supply. The same conductors in the station controller power supply are also interconnected within its power supply.

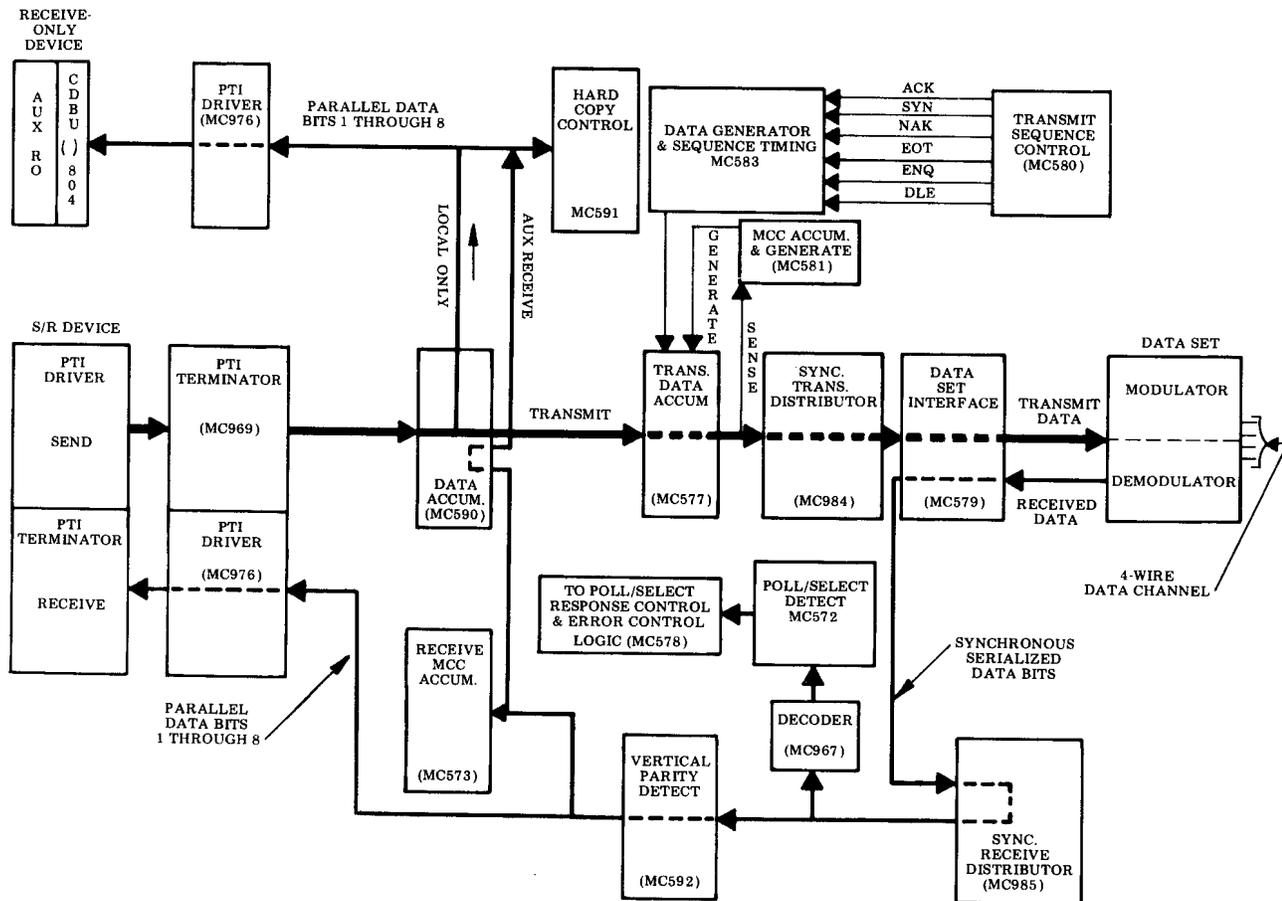


Figure 5 - Station Controller Send/Receive Data Flow

B. PTI/EIA Send and Receive Data Flow

2.22 The electronic circuitry in the CDIF814 station controller module can be functionally separated into three basic portions. These are transmit, receive, and receive error and station response controls. Figure 5 illustrates a basic receive and transmit data flow through the station controller from a CDT S/R device, with an auxiliary RO hard copy printer, to the data line modem. Error and format control logic is not shown in the illustration. For a complete functional diagram of the station controller, indicating signal flow and error and format logic circuitry, refer to 2597SD schematic diagram, sheets B1 through B5, that are furnished in the wiring diagram package, number WDP 0325.

C. Parallel Terminal

2.23 The receive and transmit ports of the module, that connect the CDT or equivalent S/R device and auxiliary RO device,

operates using Teletype's parallel terminal interface (PTI) signaling. This interface is used for send and receive data bit signaling and error control signaling between the local S/R device, auxiliary RO, and the station controller.

2.24 Parallel terminal interface signals, representing data bit information between the S/R device and the station controller module, are high state for space and a low state for mark. Control signals, to regulate data bit exchange and error control, are a high state for the on condition and a low state for the off condition. Since PTI signals are current sensitive and not voltage sensitive, in high state a maximum current of 20 milliamperes (milli is thousandths of one ampere) should flow on the interconnecting leads. In low state, no apparent current, less than three microamperes (micro is millionths of one ampere), should be detected. Length of the interconnecting cabling between the station controller module and terminal including the optional RO terminal buffer should not exceed 1000 feet each interconnection.

D. PTI Transmit

2.25 The following description is provided for understanding the control and data bit signaling sequence between the station controller and S/R device for establishing message transmission (Figure 6). It should be understood at this point that the station controller and remote computer have established synchronism through the data set interface; and that the station controller has received its discrete poll sender address as explained in 3.29 through 3.34. Data set interface signal exchange is explained in 2.09.

- (a) At JB101 transmit connector (input port) on the station controller, a selectable (S) signal is turned on (high state or current flow into the terminator card) indicating that the device is conditioned for message transmission. Selectable signal must be held on by the S/R device for the entire message transmission.
- (b) The PTI terminator circuitry at JB101 input port, passes the selectable (S) signal to the MC591 hard copy device control circuit. If a poll sequence is received, the hard copy control signals the terminator to turn on its message (M) signal, which is returned to the S/R device.
- (c) If the S/R device is ready to send a message, it responds by turning on its ready (R) signal which goes back to the station controller.
- (d) The message control signaling is now completed and the station controller requests parallel data bit information from the sender by responding with next character (NC) signal. This signal conditions the sender to present the first message character, parallel data bits one through eight on its transmit buss (PTI driver). The sender places the first character on the transmit buss, and after a delay of 100 microseconds, it responds to the station controller with a character available (CA) signal.
- (e) When the NC and CA signals are both on, the station controller, if prepared to accept the character, will sample the send device parallel data buss. When the station controller samples the data buss, NC signal goes off which turns off CA signal at the send device. When the next character is to be transmitted by the station controller, the NC and CA signal exchange is repeated for every

message character until the entire message has been read from the send device. Next character (NC) control is contained on the MC582 message heading detect and NC control circuit card. For explanation of message heading characters sent to the station controller, refer to 2582CD circuit description.

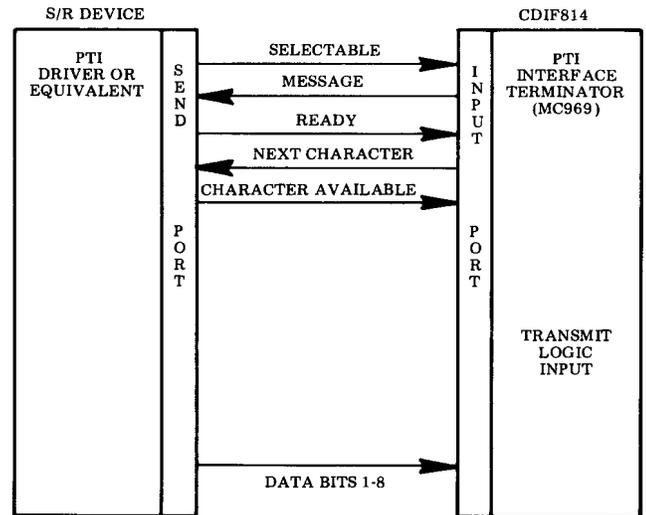


Figure 6 - Message Control Signaling Sequence for CDIF Transmit Logic

E. PTI Receive

2.26 Receive interface control signaling for the station controller and receive interface of the S/R device is similar to the information contained in 2.24 of this section, except that the receiver, when conditioned for receive, turns on selectable signal. The S/R device terminal interface control circuit logic either places selectable on the receive interface or the send interface to indicate the operation the terminal is conditioned for. It should be understood at this point that the station controller will not select the receive device for an incoming message, unless the discrete station address is received, and the central processor and station controller have established synchronism through the data set interface. Further explanation of discrete select receiver addresses are explained in 3.14 through 3.21. Data set interface signal exchange is explained in 2.08 through 2.20.

- (a) At JB103 connector (output port) on the station controller, a selectable (S) signal is turned on (high state or current flow into the station controller PTI driver

card) indicating that the S/R device is conditioned to receive message traffic. The PTI terminator in the S/R device should be programmed to provide a selectable signal to the interface module in the direction shown in Figure 7. Selectable signal must be held on by the S/R device for the entire time that the message is being received. It may turn off upon receipt of the message end-on character.

(b) If an address is received to select the S/R device to receive a message from the remote CCS station, and the selectable signal is on from the S/R device indicating it is ready to receive, the MC579 circuit card (data set interface and control logic) sets an electronic latch into receive operation and primes logic gates on MC579 to generate a receive message signal to the MC976 PTI driver. The PTI driver returns a message (M) signal, on, to the receive port of the S/R device.

(c) If the S/R device is conditioned for receive it returns a ready (R) signal, on, to the station controller MC976 interface circuit card. The interface circuit card forwards the ready signal to the MC575 circuit card to inform the logic that the receive device is ready to accept the message. If ready signal is not received, an error signal will be generated by MC575.

(d) The message control signaling is now completed and the device requests parallel data information from the station controller by responding with next character (NC) signal. The station controller turns on its parallel interface driver (transmit data buss) and after a delay of approximately 100 microseconds it returns a character available (CA) signal to the receive device.

(e) When NC and CA signals are both ON, the receive device, if ready to accept the character, will receive the character from the station controller transmit buss. After the data is sampled, the receive device turns off NC signal which turns off CA signal from the station controller. When the next character can be received by the S/R device, the NC and CA signal exchange is repeated until the message end-on character is received.

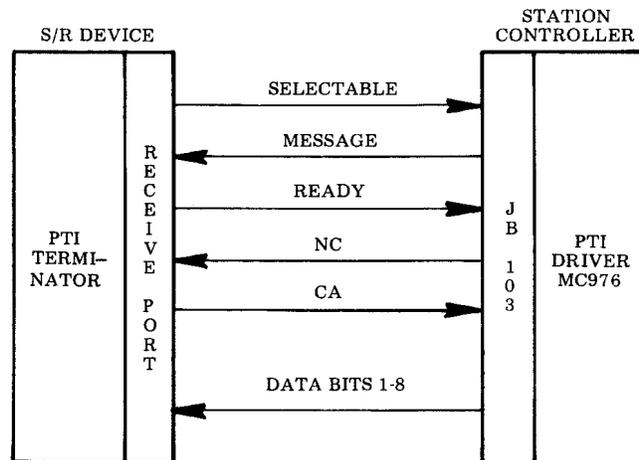


Figure 7 - Message Control Signaling Sequence for CDIF Receive Logic

F. Hard Copy

2.27 If the station controller is addressed by the remote CCS to select the auxiliary RO device, signals are exchanged between the RO and station controller in a similar manner as described in 2.26 of this section.

Local

2.28 The auxiliary RO device can also be controlled to receive data from the local S/R device when the EXT RELS and TRANSMIT buttons on the CDT display device are depressed. A description and illustration of the local hard copy interface is provided in 2.29 through 2.34 and Figure 8, respectively.

2.29 When hard copy is selected, it enables, through the MC589 circuit card, the logic gates on the MC591 circuit card to generate message and character control signals between the local send device and hard copy buffer module.

2.30 Once message interface is established, the next character (NC) and character available (CA) control signals are exchanged.

2.31 Next character (NC) signal is sent from the buffer through the station controller to the send device. The remaining exchange of NC and CA signals may be found in 2.26 (d) and (e).

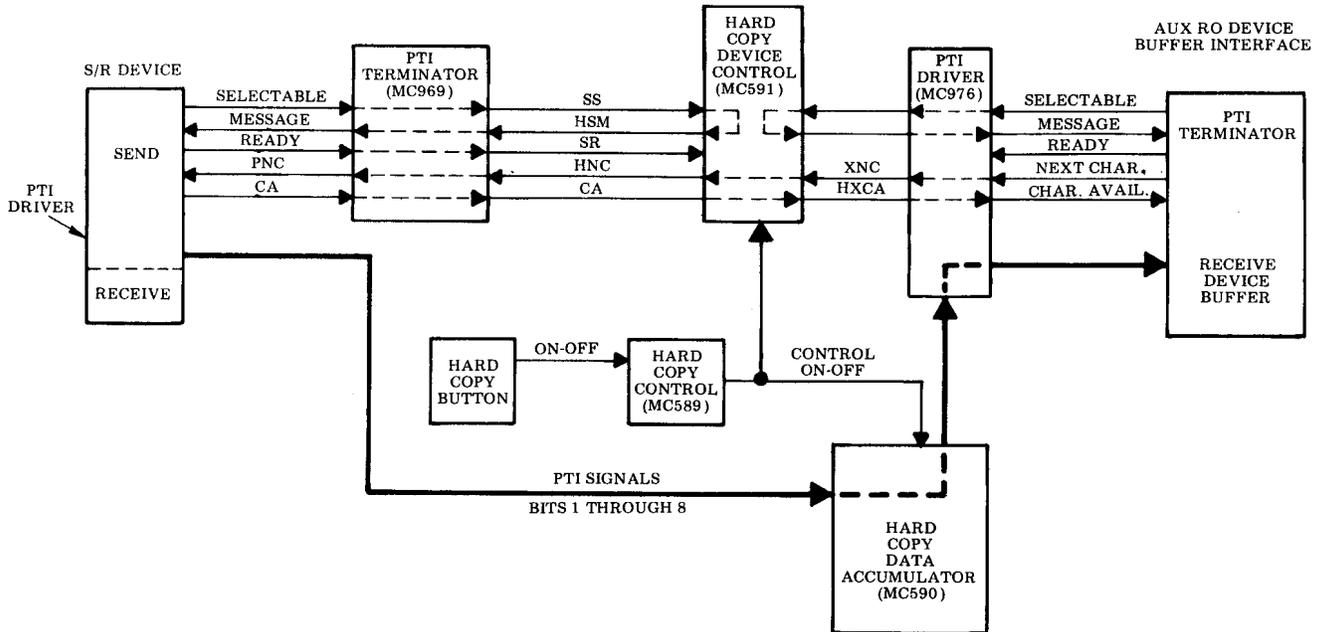
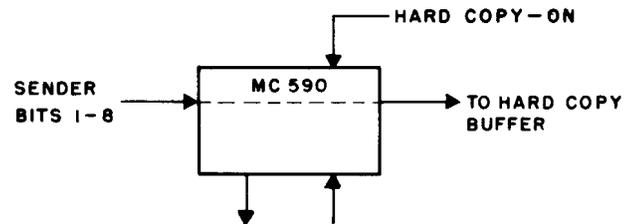


Figure 8 - Station Controller Hard Copy Signal Flow (Local)

Line

2.32 When local hard copy is off, the MC590 logic circuit is primed to transfer data received from the primary data channel to the hard copy device buffer. If the station controller receives an auxiliary select station address, it places an XRM signal on at input pin 19 of MC591, which results in an on condition at the output pin 26, and generates receive message (RM) to the hard copy buffer.



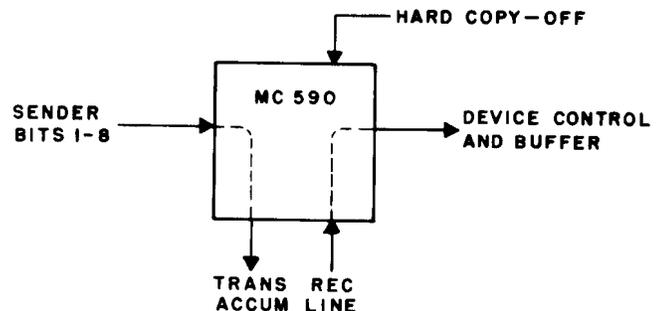
2.33 Once the message control is established (2.32) the next character (NC) and character available (CA) signal exchange occurs as previously described in 2.26 (d) and (e).

2.36 When the hard copy input is off, the MC590 circuit card switches the parallel data bits from the sender to the transmit data accumulator. Likewise, received data from the line is switched to the hard copy device control and hard copy buffer.

2.34 The MC591 circuit is also primed to transfer data from the send device to the synchronous transmit distributor when hard copy (2.32) is off. For additional information refer to 2591CD circuit description.

Hard Copy Data Accumulator

2.35 The MC590 circuit card is a logic gate circuitry that switches parallel data bit levels from the local send device to the hard copy device buffer whenever local hard copy is selected.



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G. Error Control

2.37 The station controller transmit and receive error control signal interface to the local S/R device is connected at JB201 connector.

2.38 The receive error control signal interface to the auxiliary hard copy device buffer is connected at JB402 connector.

Transmit

2.39 After establishing transmit operation on the primary data channel, the message is sent from the station controller send device over the data channel to the distant computer. Immediately following transmission, the station controller sends a message check character (MCC) and begins to timeout (4.11 and 4.12) while waiting for a response from the computer.

2.40 The computer station will respond to the station controller with either a positive acknowledgement (ACK) indicating no errors were received, or a negative acknowledgement (NAK) indicating the message was received with errors.

2.41 Transmit Data Acknowledge (TDA) — DIRECTION: Station Controller to Send Device. Upon decoding receipt of ACK character, the station controller will momentarily turn on transmit data acknowledge to the send device. Upon receipt of TDA signal the send device terminates transmit operation, and depending upon device programming may revert to either local or receive operation.

2.42 Transmit Data Error (TDE) — DIRECTION: Station Controller to Send Device. If the station controller receives a negative acknowledgement (NAK) from the computer station, it will momentarily turn on a transmit data error signal to the local send device. Upon receipt of TDE signal, the send device should prepare to retransmit the message. The MC576 error control logic allows up to two retransmissions of message containing errors upon receipt of a NAK character. If after two unsuccessful attempts to retransmit the message, if a NAK character is received from the distant computer, the station controller will abort (2.43) transmission.

2.43 Transmit Abort (TA) — DIRECTION: Station Controller to Send Device. If after two unsuccessful retransmits have occurred from the station controller send device, the MC576 error control logic upon detection of a third NAK character will momentarily turn on TA signal to MC571 error control drive. This signal is passed to the device through JB201 connector. Upon receipt of this signal the device may revert to a local alarm condition (example, flashing LOCAL button). The off condition of TA signal is not defined.

2.44 A transmit abort (TA) signal could also occur from the station controller to its send device if no response occurred, or if the answer-back response from the computer were undetected. If three timeout pulses (4.12) are received by the MC576 logic, the TA signal will turn on momentarily at the device interface causing it to abort transmission. This feature prevents unnecessary tie-up of the data set facility if the no response situation were allowed to persist.

Receive

2.45 After receive operation is established from the distant computer to the station controller receive device, or to the auxiliary hard copy device, the computer sends the message, message ending character, and then the message check character (MCC).

2.46 During receipt of the incoming message, the station controller MC573 logic circuit accumulates its own MCC character from the received data. After receipt of the message ending character, the received MCC character is compared to that of the station controller.

2.47 Receive Data Acknowledge (RDA) — DIRECTION: Station Controller to Receive Device. If the received MCC and the station controller MCC concur, request ACK signal will be initiated on the MC574 circuit. When the station controller sends ACK character, the receive data acknowledge (RDA) will momentarily turn on to the receive device. Upon receipt of RDA signal the device may change from receive to either local or idle operating condition. The off state of RDA signal is not defined.

2.48 Receive Data Error (RDE) — DIRECTION: Station Controller to Receive Device. If an error is detected in comparison of the station controller MCC and the received MCC

present on the incoming data buss, MCC error turns on and initiates request NAK on the MC574 circuit. When the negative acknowledgement character, NAK, is sent to the computer, the RDE signal turns on momentarily to the receive device. This signal indicates to the receive device that it should disregard the received data message and prepare to receive another transmission. The off state of RDE signal is not defined.

3. OPERATION

POWER ON — RESET

3.01 When the station controller power supply is first turned on, the MC958 (TP322958) circuit senses when the power supply voltage reaches the correct voltage level for operation and it generates a power on — reset (POR) signal pulse. The duration of the reset pulse is approximately 100 milliseconds (milli is thousandths of a second). The reset signal is distributed throughout the controller detection, decoding, transmission, reception, and error control logic circuitry for reset to begin operation.

3.02 The POR pulse is actually gated through an AND NOT gate with another logic reset pulse coming in on pin 5. The POR is generated when power is first turned on (3.01), but the POR/D-EOT pulse occurs only during operation whenever the mandatory disconnect sequence DLE-EOT is detected. Upon DLE-EOT detection, a logic reset on MC576 circuit is initiated as a 360 microsecond (micro is millionths of a second) pulse into the AND NOT gate on MC958 circuit. The output pulse from the gate is distributed to the same points as the POR pulse to reset to normal all message framing and formatting, and sequence detection circuitry on MC572, MC573, MC574, MC575, MC576, MC582, and MC588 circuits.

IDLE

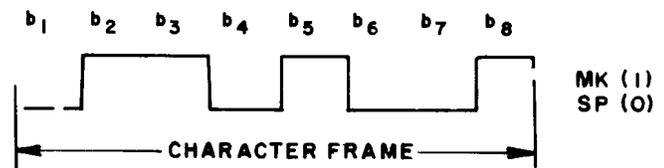
3.03 Idle condition is a term used to describe the condition of the station controller when it is ready to be addressed for station operation. In idle, all incoming data signals are monitored by the controller which is constantly looking for SYN characters to establish synchronization with the incoming data. Character data following the SYN characters, if synchronism has been achieved, is also examined to determine if the station controller has or has not received its discrete station address for either receive or transmit operation. At this time the message control interface between the controller and its device is in off condition, that is no

character transfer occurs. When the discrete address is received, the controller examines either receive selectable (RS) or send selectable (SS) from the device interface, depending whether a poll or select address is received, to determine if the device is ready for operation. In idle condition send message (2.25 (b)) and receive message (2.26 (b)) from the controller to the device is in off condition.

3.04 The idle data line follows pertinent control sequences such as ENQ, ACK, NAK, ETX MCC, or ETX and DLE EOT. In these instances the receiver (either station controller or computer) looks for SYN characters to re-establish character synchronization.

SYNCHRONIZATION

3.05 Upon receipt of two contiguous SYN characters, the controller logic circuits establish character synchronization with the incoming data signals. From the start of synchronization, the controller logic is locked on and begins counting on the first data bit received. Every eight data bits received thereafter is considered a data character. ASCII character SYN is illustrated below.



3.06 However, if the SYN characters are not contiguous, an off condition of the controller's first level SYN detect logic causes a reset of the SYN counter logic and character framing must be re-established before data exchange can begin. Receipt of the four SYN characters actually allows three chances for the controller to achieve character framing.

3.07 Synchronization, or character framing, will be aborted if at any time 16 contiguous bits of marking line are detected in the controller's receive data interface. Character framing must then be re-established.

SUPERVISORY SEQUENCE DETECTION

3.08 The MC985 receive distributor circuit utilizes the serial clock receive (SCR) from the data set for timing. Serialized incoming data bits load into the distributor circuit (first level) and come out in a parallel character format

where it is presented to MC575 receive character timing and control for detection of two contiguous SYN characters. Data in the MC985 distributor (first level) is valid for only one bit time.

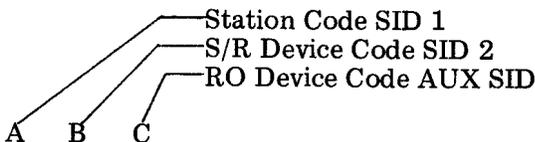
3.09 The second level parallel-in parallel-out storage level receives parallel data bits from the first storage level and retains them for one character time. Data bits from the second level are presented to the MC967 circuit for character decoding. From the decoder, the station SID program straps carry the column and row output of the programmed station device character to the MC572 receive character detect and poll/select detect circuit (3.10).

Received Character and Sequence Recognition

3.10 MC572 gate logic receives decoded SID character recognition from back plane wire straps installed between the circuit card receptacles in module positions ZB112 and ZB113. Logic gates on MC572 convert the row and column information determined from the back plane wire straps to the specific characters for the station and device address.

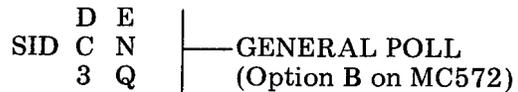
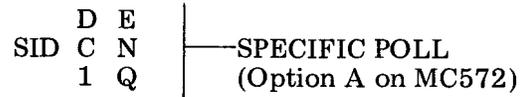
3.11 In addition to station and device address detection, poll sender or select receiver supervisory sequences are also detected in MC572 circuit logic. Output signals from MC572 are pulsed on whenever a select without replies (fast), select with replies, and poll sequences are decoded. All detected supervisory sequences must be contiguous; that is once the SID has been detected, the following characters must result in a sequence detection. A received character having bad vertical parity, or a character not in sequence resets the detection logic. Once this occurs the SID must be detected again to restart the decoding and sequence detection process.

3.12 Any two-character sequence (examples, AB, AC, or CA) can represent SID 1 and SID 2. If the station is equipped with a RO hard copy device with a character buffer (optional), then the AUX SID must be programmed. Station coding remains a two-character sequence (examples, AB or AC).



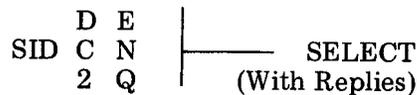
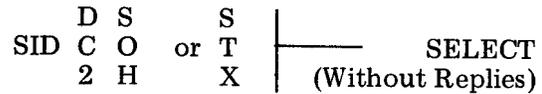
3.13 The station identification and device (SID) address followed by a poll sender sequence, or a select receiver (either without replies or select with replies) sequence is decoded on MC572 circuit. Detectable SID sequences are as follows.

Poll Sender Sequences



Note: MC572 circuit is programmable to detect either a specific poll or a general poll sequence, but not both. If the general poll sequence is used, the device code in the SID must be coded for the question mark (?) character.

Select Receiver Sequences



SELECT RECEIVER SEQUENCES WITH ANSWER-BACK

3.14 When a select sequence is detected on MC572 or MC588 auxiliary device control circuit, the involved receive device must be investigated as to whether it can be conditioned to receive data. This operation is performed on MC578 or MC588 by strobing the particular receive selectable (RS) from the device interface with the select pulse.

3.15 If the addressed device receive selectable is off at device interface, MC578 or MC588 will turn GEN NAK A/B ON which causes MC574 to generate a SID and NAK response on-line to the computer. The receive device selected determines on MC589 which second SID character, device or aux device output (pin 15 or 16), is to be sent to the MC982 character generator circuit. The response transmission operates through MC580, MC583, MC577, and MC984.

3.16 If the addressed device receive selectable (RS) is ON, GEN ACK A/B is generated and the station controller SID and ACK response is sent on-line to the distant computer station. Receive message (RM) from the station controller to the selected receive device interface is generated by either MC579 or MC588.

3.17 When the distant computer completes its turnaround, it will send SYN characters. When the SYN characters are detected by the station controller and synchronism with the distant computer is established, the first non-SYN character received by the station controller determines its course of action. If the computer did not receive the answer-back, it will send ENQ character. Receipt of ENQ character causes the last answer-back SID ACK or NAK to be sent again by the station controller MC574 circuit. Request answer-back may be repeated any number of times at discretion of the distant computer. If however, the first character detected is SOH or STX, the station controller passes all subsequent received data to the designated receive device, beginning with the characters SOH or STX (if SOH is not used) and ending with the message ending character ETX. Error control operation is described in 3.22 through 3.25.

3.18 Receipt of the mandatory disconnect sequence data link escape (DLE) and end of transmission (EOT) returns the station controller to the idle state.

SELECT RECEIVER SEQUENCES WITHOUT ANSWER-BACK

3.19 When select without replies sequence is detected on MC572 or MC588, the addressed receive device must be investigated as to whether it can be conditioned to receive. This operation is performed by strobing the particular receive selectable (RS) from the device interface with the fast select pulse on MC578 or MC588 circuit.

3.20 If the addressed device receive selectable (RS) is on, the station controller receive message (RM) is turned on to the selected receive device interface by either MC578 or MC588 circuit. Then the message transfer is initiated. After the message is received, operation occurs as described in 3.16 and 3.17.

3.21 If the receive selectable (RS) from the addressed device is off, either MC578 or MC588 circuit will turn on a GEN NAK RESP signal. Dependent upon which receive device was addressed, this signal determines what device code

is sent in the answer-back sequence, and it conditions the receive error control logic and transmit sequence control logic for negative answer-back. At the end of the incoming message, the station controller completes turnaround and generates SID NAK (negative acknowledgement) answer-back to the distant computer control station. The received message was not copied by the receive device addressed. Therefore, the computer station will either try to retransmit the message or it will direct the message through the system recovery procedure.

RECEIVE MESSAGE ERROR CONTROL

3.22 The station controller upon detection of a select sequence, if the device has receive selectable (RS) on, turns receive message (RM) on to the receive device. The first character of the message (SOH or STX) is presented to the device. At this time the signal SOH-ETX is turned on and is used as an enable for the receive message check character accumulator on MC573 circuit. All subsequent message characters received, excluding SYN, and up to and including ETX, are accumulated.

3.23 SOH-ETX is also used to gate copy enable. This signal is used to determine whether the character received should be presented to the device. Received SYN characters will turn copy enable signal off as will Null characters, however, Null will be accumulated in the MCC. Upon detection of ETX, SOH-ETX as well as copy enable are turned off after ETX character is presented to the device. The character immediately following ETX is the message check character (MCC) and is subsequently checked for accuracy.

3.24 If the message check character (MCC) is valid, that is no parity errors were received, and no receive device interface signals malfunctioned, the transmission of the SID and ACK (positive acknowledgement) is initiated by MC574 circuit and sent on-line to the distant computer station. Receive device acknowledge (RDA) is then presented to the selected receive device by MC574 or MC589.

3.25 If the received message check character (MCC) is invalid, if parity errors were detected, or if a receive device interface signal malfunctioned, SID NAK (negative acknowledge) is sent on-line from the station controller to the distant computer. Receive data error (RDE) is then initiated to the selected receive device.

3.26 Operation then occurs as described in 3.17 and 3.18.

ABORTED RECEIVE SITUATIONS

3.27 If ENQ character is received after receipt of SOH or STX or during message receipt before ETX is detected, SID NAK (negative acknowledge) answer-back is sent to the line. The station controller then initiates receive data error (RDE) to the device, after which operation continues as in 3.17 and 3.18.

3.28 If the disconnect sequence DLE EOT is received at any time during the course of the message, the station controller returns to idle (3.03).

POLL SENDER SEQUENCES

3.29 When a poll send device address is detected on MC572, a pulse is initiated that investigates if the send device is ready by sampling its send selectable (SS) signal from the device interface. If send selectable (SS) is on indicating that the device has a message ready for transmission, the station controller generates send message (2.25 (b)) to the transmit device. Message heading and detection logic and message transmission begins. The first character received by the station controller from the send device determines the course of action initiated by MC582 control circuit.

- (a) If the first character is Null or Delete, it and the following Nulls and Deletes are disregarded until the first non-Null, non-Delete character is detected, at which time operation occurs as described in (b), (c), or (d).
- (b) If the first non-Null, non-Delete character is SOH, the station controller synchronizes the line and sends SOH SID followed by the next character from the send device.
- (c) If the first non-Null, non-Delete character is STX, the station controller synchronizes the line and sends SOH SID STX followed by the next character from the send device.
- (d) If the first non-Null, non-Delete character is neither SOH nor STX, the station controller holds said character on the parallel buss, synchronizes the line and sends SOH SID STX followed by the character held on the parallel transmit buss.

3.30 As SOH is sent, the signal SOH-ETX is turned on and only turns off after ETX has been sent. This signal acts as an enable to the

transmit message check character accumulator on MC581. Characters from the device are accumulated in addition to the characters generated by the station controller during its heading generation as described above. The accumulated MCC is sent immediately following the transmission of ETX after which the station controller enables a timer (4.11) and waits for a response from the computer control station.

3.31 If SYN characters are detected during the station controller timeout, the first non-SYN character received determines the following course of action.

- (a) If the first non-SYN character is ACK, the station controller generates transmit data acknowledge (TDA) to the send device. It also initiates transmission of the disconnect sequence DLE EOT, after which the station controller returns to the idle state (3.03).
- (b) If the first non-SYN character is NAK, the station controller generates transmit data error (TDE) to the send device. At this time the send device conditions for a retransmit of the message. The station controller then counts the number of NAKs received after each transmission. If a third successive NAK is received after each transmit, the station controller generates transmit abort (TA) to the send device and waits for system timeout and recovery by the CCS.
- (c) Detection of ACK or NAK as described in 3.31 (a) and (b) causes the timeout timer to be reset. If the first non-SYN character is neither ACK nor NAK, the timer is not disabled and is allowed to complete its timeout. If the timer does complete its timeout, transmission of ENQ is initiated by the station controller after which the timer is re-enabled and operation continues as above. If the third successive timeout is detected, ENQ is not sent but transmit abort (TA) is generated to the send device, and the station controller returns to the idle state.

3.32 If send selectable (SS) is off when a poll sender address is received (3.29), the transmission of the no-traffic response, DLE EOT, is initiated and sent to the distant computer. The station controller then returns to the idle state.

ABORTED TRANSMIT SITUATIONS

3.33 During the course of message transmission from the send device, if a disconnect sequence of DLE EOT is detected from the computer control station, the station controller will generate transmit abort (TA) to the send device and return to the idle state.

3.34 Also during transmission from the send device, if a character cannot be obtained from the sender, the state of sender ready signal from the send device interface determines the course of action. If sender ready (SR) is off, transmission of the disconnect DLE EOT is initiated and transmit abort (TA) is generated to the device. The station controller then returns to the idle state.

LOCAL HARD COPY OPERATION

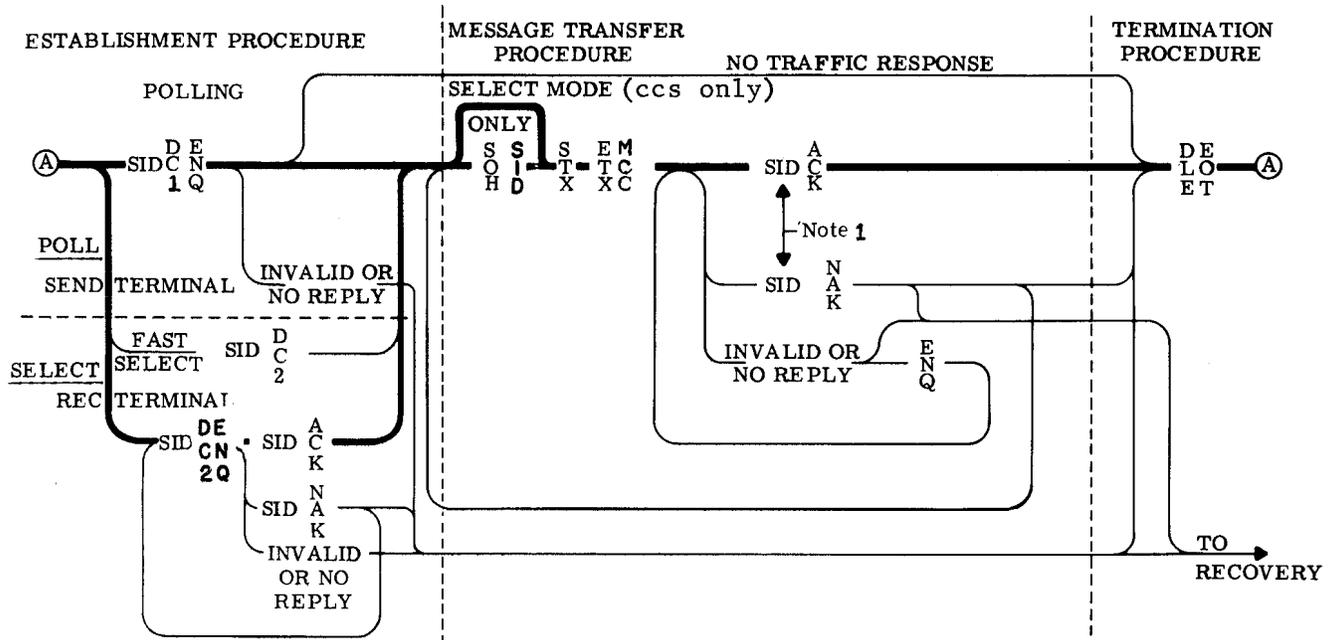
3.35 When the local hard copy operation is selected on the send device, and if the auxiliary receive device is ready to receive data

(selectable is on), the send device can begin sending and hard copy message transfer is initiated. In most CDT device applications, EX^T RELS button then TRANSMIT is depressed to initiate message transfer. The message transfer is in parallel terminal interface from MC976 with the slower device controlling the speed. Upon detection of ETX from the send device, the message transfer is ended, the send device reverts to local, and receive data acknowledge signal (RDA) is presented to the receive device.

3.36 While the local hard copy message transfer is in process, all signals to the module control logic are off. Any supervisory sequences (poll or select) received from the line will result in a negative reply (SID NAK) to the line.

4. TRANSMISSION LINE PROCEDURES

4.01 Figure 9 illustrates the line procedure method for establishment, message transfer, and termination procedure for poll and select sequences.



Note 1: Computer Control Station has no SID.

Figure 9 - Line Procedure Method

STATION SELECTION ADDRESS SEQUENCE

4.02 The station controller logic is capable of discerning between two types of station selection address sequences, select without replies, or select with replies received from the distant computer terminal. These differ only with the character sequence following the station and device address.

4.03 All station selection sequences received from the line must be contiguous characters preceded by idle line (3.03) and a minimum of four SYN characters. The selection sequences are as follows:

SELECT WITH REPLIES SEQUENCE



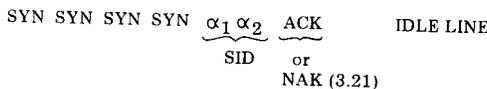
SELECT WITHOUT REPLIES SEQUENCE



4.04 The SID in the select with replies sequence is followed by the DC2 and ENQ characters. The ENQ character is omitted in the select without replies sequence (fast) in which case a station response is not requested until the end of the message receipt. In the select without replies sequence, SOH or STX TEXT follows the DC2.

STATION SELECTION RESPONSE (With Replies)

4.05 The station controller response to detection of a select with replies sequence, DC2 followed by ENQ character, is as follows:

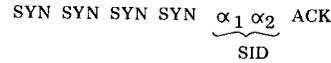


STATION SELECTION — NO RESPONSE (Fast)

4.06 The station controller will not respond (no answer-back sent) when the station selection sequence does not contain the ENQ character, but is followed immediately by an SOH or STX character. The station controller answers only at the end of the received message. At

completion of the message, the station controller will respond with either a positive (ACK) or negative (NAK) response to the line. The type of response sent depends on the condition of the receive device and whether or not any errors were detected (3.24).

(a) If the device was ready and the message was received error free, the station controller sends the following answer-back.



(b) If the message was not completed because of errors, or if the device was not able to receive, the station controller answer-back response is the same as 4.06 (a) except that NAK is transmitted in place of ACK.

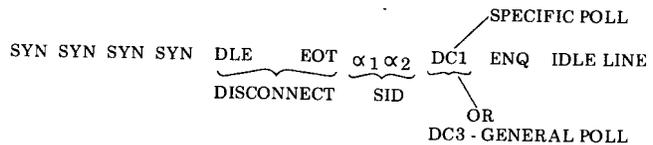
ERRORED STATION SELECT SEQUENCE

4.07 The station controller will not respond to a station select sequence containing character parity errors in the received transmission.

STATION POLLING

4.08 Station polling is the line procedure used by the remote CCS for accumulating message traffic from send devices sharing the primary data channel. The CSS station in this arrangement is always the recipient of a polled transmit device. Only one send station is activated at a time for point-to-point data transfer.

4.09 The CCS station poll send device sequence is as follows.



4.10 A polled station controller will respond to its discrete station address in one of two ways.

(a) Station ready to send — it will start sending the message.

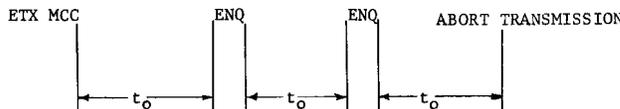
(b) Station not ready to send — it will transmit the terminate sequence consisting of data link escape (DLE) followed by end of transmission (EOT).

Note: The station controller will precede each answer-back response with transmission of four SYN characters. Also, the controller will not answer-back to errored polling sequences.

NO RESPONSE TIMER

4.11 The station controller includes a no response timer circuit that has a timing range of $1.5 \pm .50$ seconds. The timer is activated at the completion of each message transmission following the transmission of the message ending character and the message check character (ETX-MCC), or ENQ. It is reset upon receiving an appropriate response (answer-back) from the CCS terminal regarding the validity of the transmitted message.

4.12 The no response timing sequence begins after a polled station transmits the data and sends ETX and MCC characters. After each no response timeout period (t_o), the station controller sends ENQ character (acknowledge requested) and awaits a response. If after two retries, if a response is not received, the station controller will send the disconnect sequence DLE EOT and activate the send device station local alarm to signal the attendant of the abort (2.43).



MESSAGE FORMAT

4.13 The station controller transmit message format includes a message check character (MCC) for verification at the distant receiver (computer), and automatic retransmission of errored messages upon receipt of NAK (negative acknowledgement).

4.14 All messages sent from the station controller or received from the distant computer must be structured with message delimiters starting with characters start of heading (SOH), and ending with end of text (ETX). The message check character (MCC) is always transmitted immediately following the ETX character. Message structure is as follows:

SOH $\alpha_1 \alpha_2$ HEAD-STX TEXT-----ETX MCC IDLE LINE
SID

4.15 The message text must always be void of the following control characters: SOH, STX, ETB, ETX, EOT, ENQ, ACK, NAK and DLE to prevent any possible erroneous link control action during message transfer.

A. Time Fill Characters

4.16 The station controller with data set operate into systems where all data, sent or received, consists of a serialized stream of contiguous characters. In these applications the station controller will generate or will receive and recognize the SYN character as time or medial fill.

4.17 SYN characters are used during message transmission as time fill when no other characters are transmitted. The SYN character cannot be inserted as time fill between the DLE EOT or ETX MCC sequences.

4.18 If Null characters (all Space) are received from the CCS, the station control will not forward this character to the receive device. However, it includes this character in the formulation of the message check character (MCC).

4.19 As a send device, if Null characters appear in the message text, the station controller will transmit them to the CCS and also include them in the generation of the MCC character.

B. Error Control Features

4.20 Error control consists of error detection with automatic retransmission of errored messages.

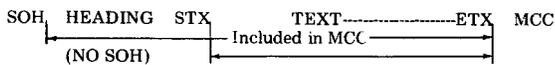
4.21 With automatic retransmission of errored messages, a message check character (MCC) is generated at the send and receive terminals. The MCC is always transmitted by the sender immediately after the end of text (ETX) character. A comparison of the check character transmitted with that locally generated at the receive station is made to determine the validity of the message data.

4.22 The MCC character is formulated by accumulating a binary total by bit of the text characters starting with SOH or STX, but not including this character, and ending inclu-

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sively with ETX. If the message starts with SOH, the STX character is included in the MCC accumulation.

4.23 The MCC summation is such that the number of marking bits in any level, excluding the eighth level, is even. The eighth bit of the MCC character shall conform to the vertical parity character summation depending on the message transmission parity option. In a synchronous transmission system, the SYN character is not included in MCC accumulation. Below is illustrated the message format with markers indicating the start and end of the MCC accumulation.



C. Error Control Response with Automatic Retransmission

Sender Response

4.24 As a sender, the station controller will wait for a response from the computer control station (CCS) as to the validity of data received. The CCS must respond by sending ACK if the message was free of errors, or NAK if an error was detected or the CCS became inoperative during data transmission. The response must be returned within one second. See no response time out (4.11). If the response from the CCS is garbled, the station controller will respond with an ENQ character and wait for another response. After two ENQs the station controller will stop sending and wait for system timeout and recovery.

4.25 If a NAK is received, the sender device will be conditioned to retransmit the message. After two attempts to retransmit message, the station controller will stop sending and wait for system timeout and recovery by the computer control station.

Receiver Response

4.26 As a receiver, the station controller will respond in one of two ways after receipt of a message:

- (a) If the message has been received free of detectable transmission errors, the station controller will send its SID followed by ACK. Detectable transmission errors are defined as:

- (1) Vertical parity errors
- (2) Message check character error
- (3) Receiver became inoperable during the transmission

(b) If the message has been received with detectable errors (as defined in (a)), the station controller will send its SID followed by NAK.

4.27 If the station controller has sent a response and the computer control station sends the ENQ character, the station controller will repeat its previous reply. If the station controller receives an ENQ character, but had not previously replied, it will send its SID followed by the NAK character.

D. Auxiliary Receive-Only Device

4.28 The station controller accommodates message transfer from either the CCS or the local send device to an auxiliary RO device.

4.29 A message transfer from the CCS to the auxiliary RO device is initiated by the station controller upon detection of the discrete station and device select sequence. Refer to 3.13 for station selection procedures.

4.30 A hard copy feature allows a message to be transferred from the local send device through the station controller to the auxiliary RO device. This transfer is initiated and completed if the following conditions exist:

- (a) The RO device can be conditioned to receive a message.
- (b) An ETX message ending character is present in the message so that the send device can be conditioned to send.

4.31 During the hard copy transfer the station controller will send a negative acknowledgement (SID NAK) to a select sequence.

STATION CONTROL FLOW CHARTS

4.32 The following station controller flow charts, Figures 10 through 14, are provided in a simple logic flow diagram showing on line operation of the station controller.

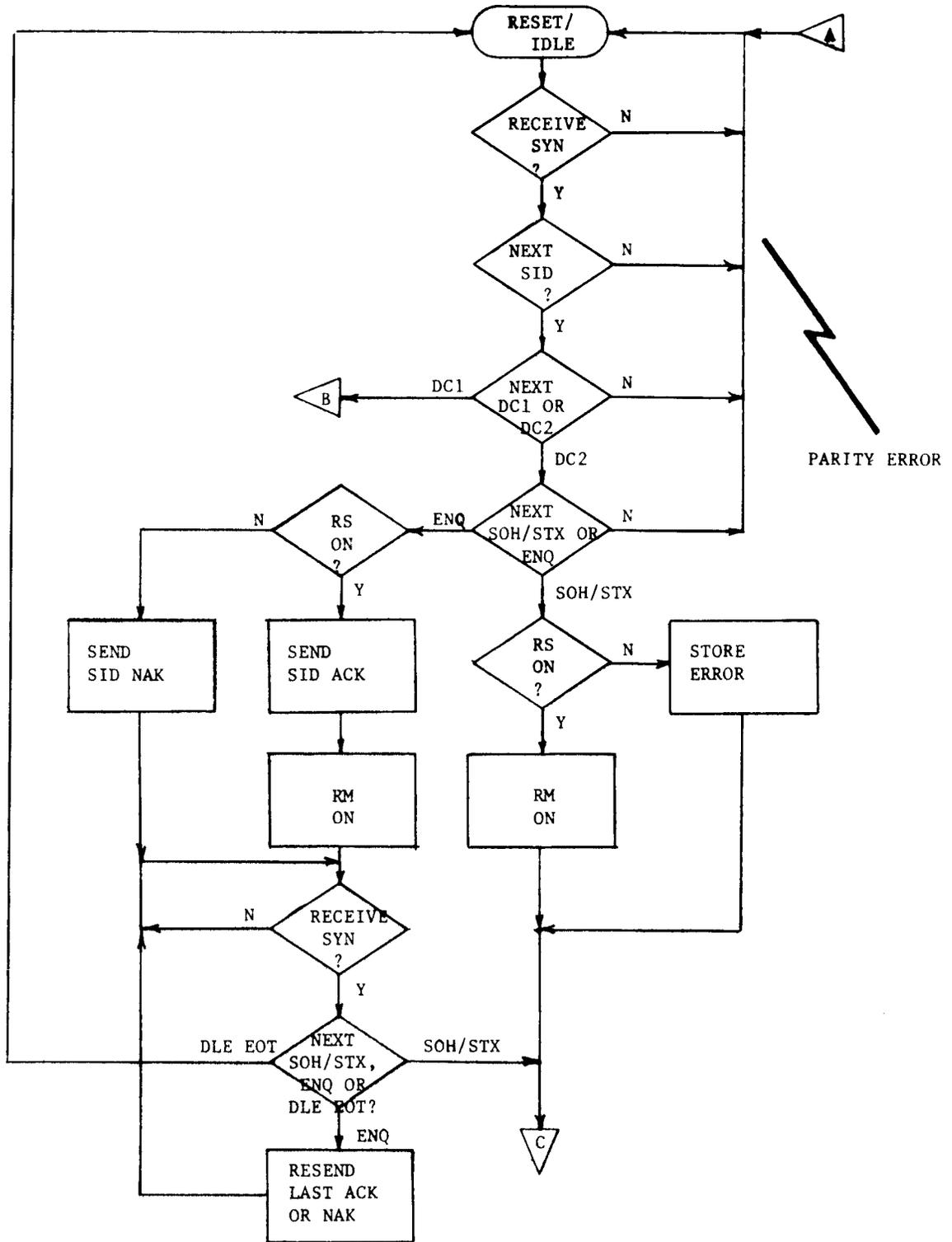


Figure 10

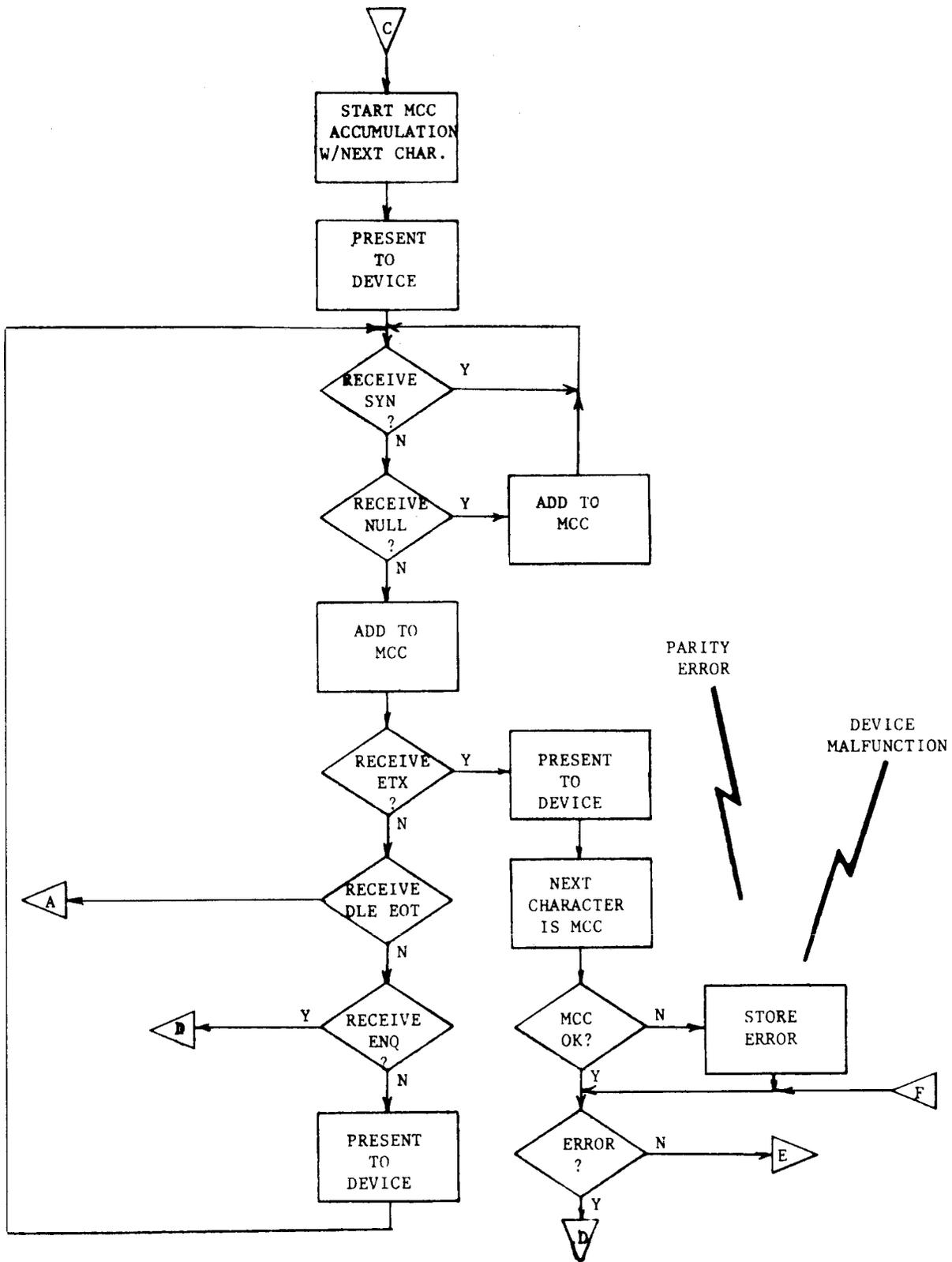


Figure 11

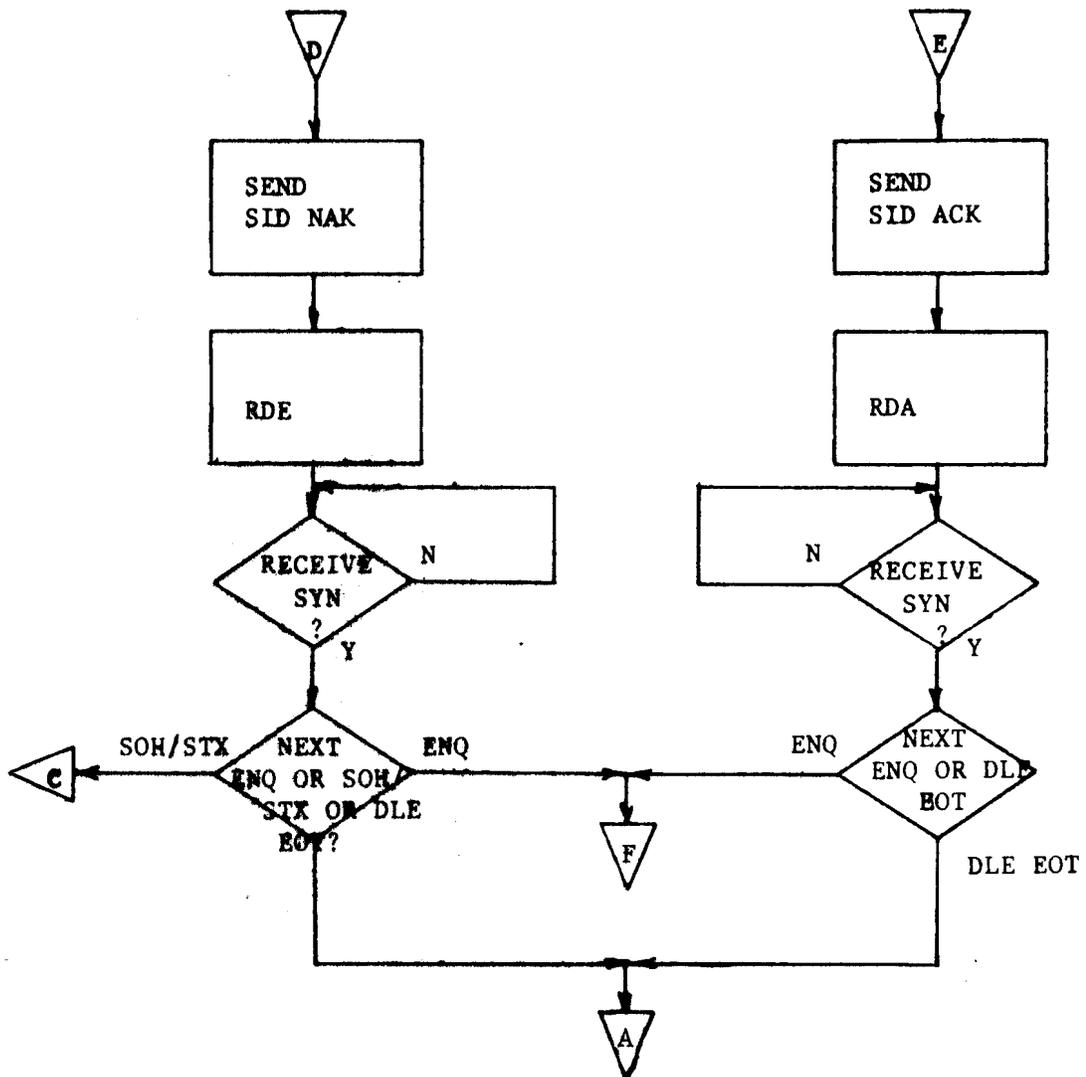


Figure 12

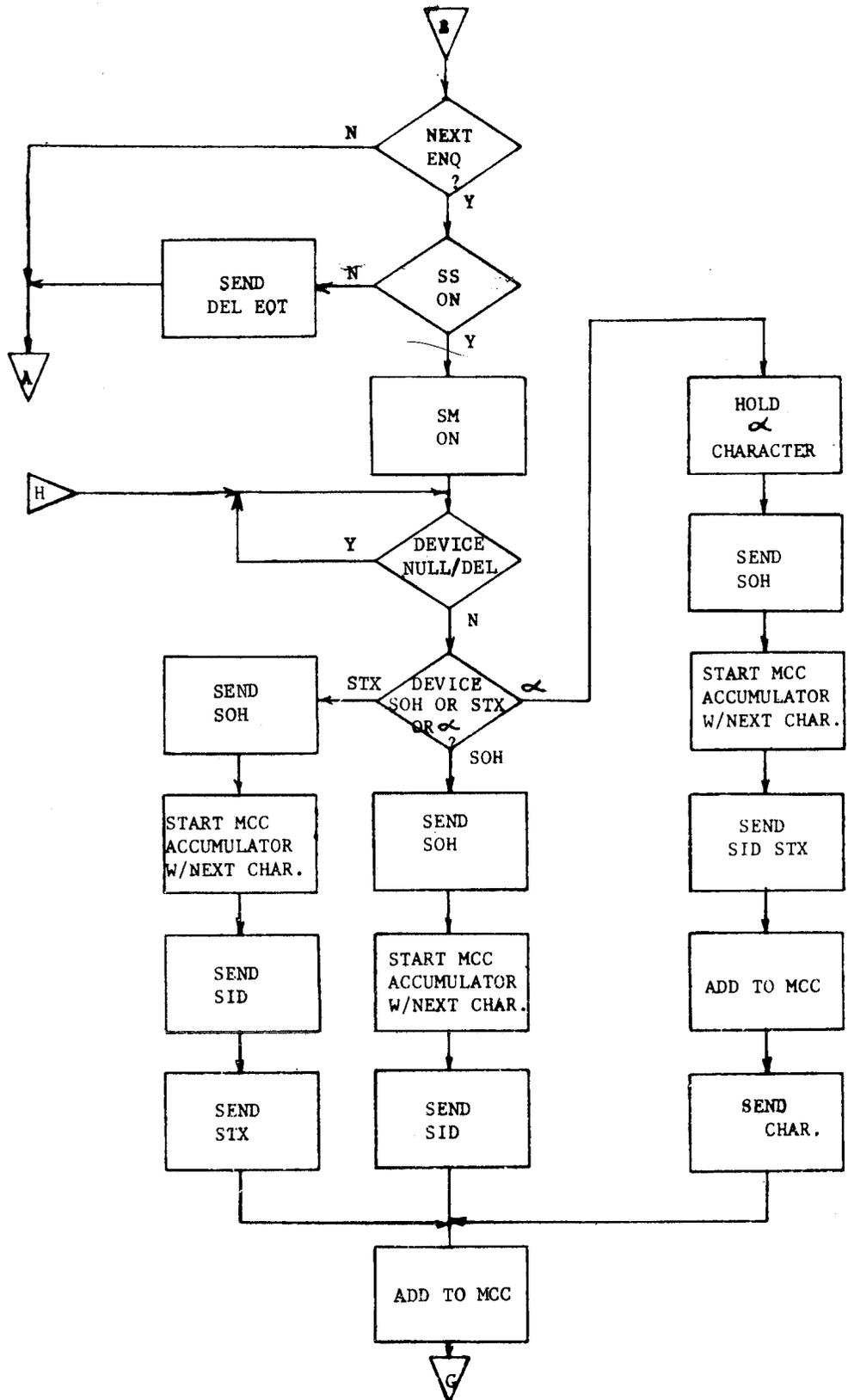


Figure 13

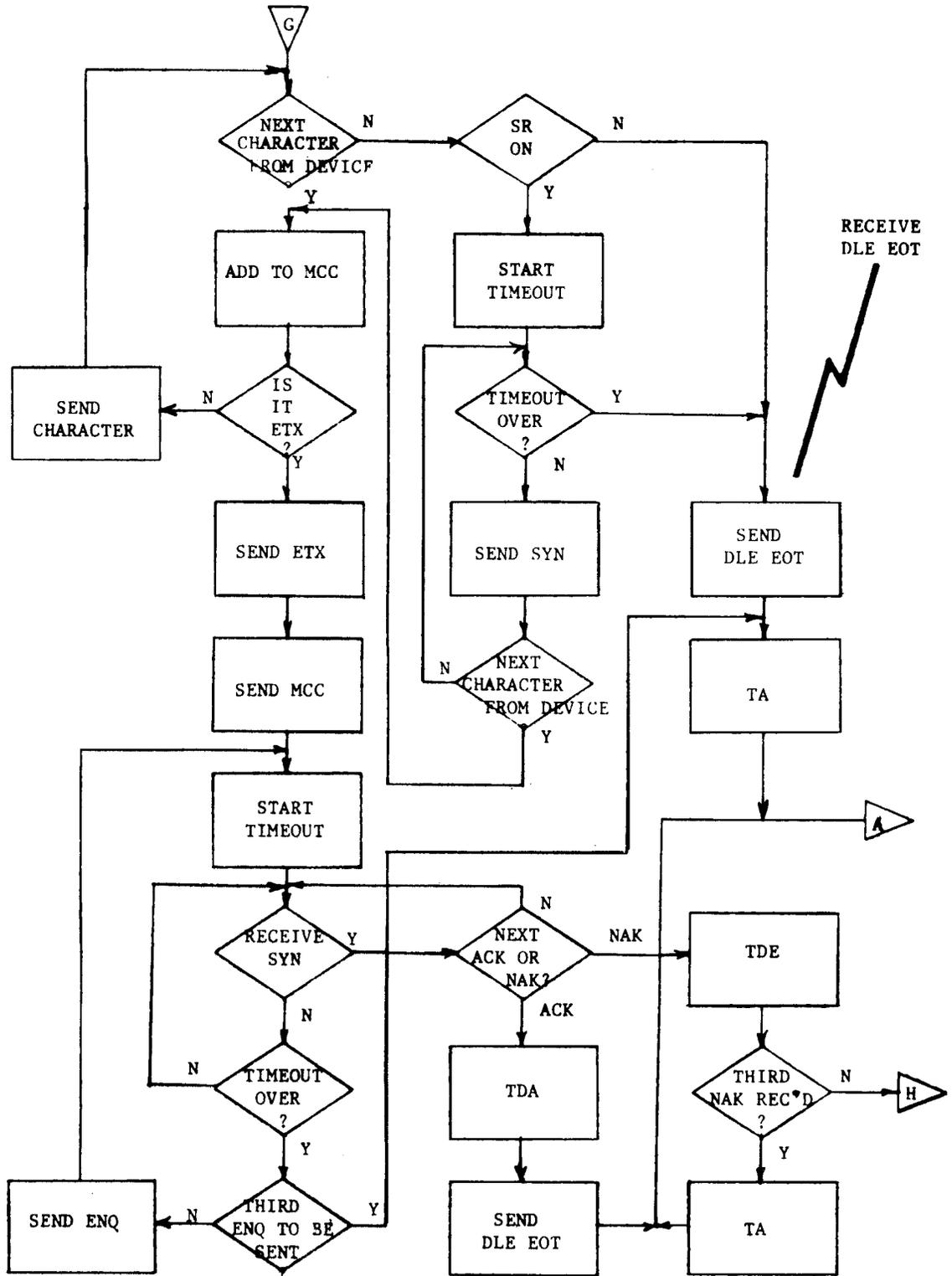


Figure 14