COMMUNICATIONS DISPLAY TERMINAL (CDT)

BUFFER MODULES CDBU801 AND CDBU802

DESCRIPTION AND PRINCIPLES OF OPERATION

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1. GENERAL

1.01 This section provides the description and principles of operation for the CDBU801 (Figure 1), and CDBU802 (Figure 2) buffer modules, either of which can be used in a Communications Display Terminal (CDT). It is reissued to include the latest engineering changes. Issue 1 of this section was a limited printing edition and did not receive general system-wide availability nor distribution. This is the first standard printing available for general Bell System distribution.

1.02 A buffer unit is a solid state device used for the temporary storage of messages at the input and/or output of a CDT.

2. DESCRIPTION

BASIC UNIT

2.01 Each buffer unit utilizes 8-level parallel signals which are compatible with ASCII (American National Standard Code for Information Interchange), and operates on a First-In-First-Out (FIFO) basis. Messages are accepted and stored in the buffer until transmission to a receiving device.

2.02 Since the buffer is a dynamic storage device, a loss of power applied to the buffer will result in the loss of any information in the buffer.

TECHNICAL DATA

A. Physical Characteristics

Weight:

CDBU801 — 14-1/2 pounds (fully carded)
CDBU802 — 15 pounds (fully carded)

Note: The following dimensions refer to both the CDBU801 and CDBU802 modules.

Height . . . . . 14-3/8 inches
Width . . . . . 6 inches
Depth . . . . . .19 inches

Prepared for American Telephone and Telegraph Company by Teletype Corporation

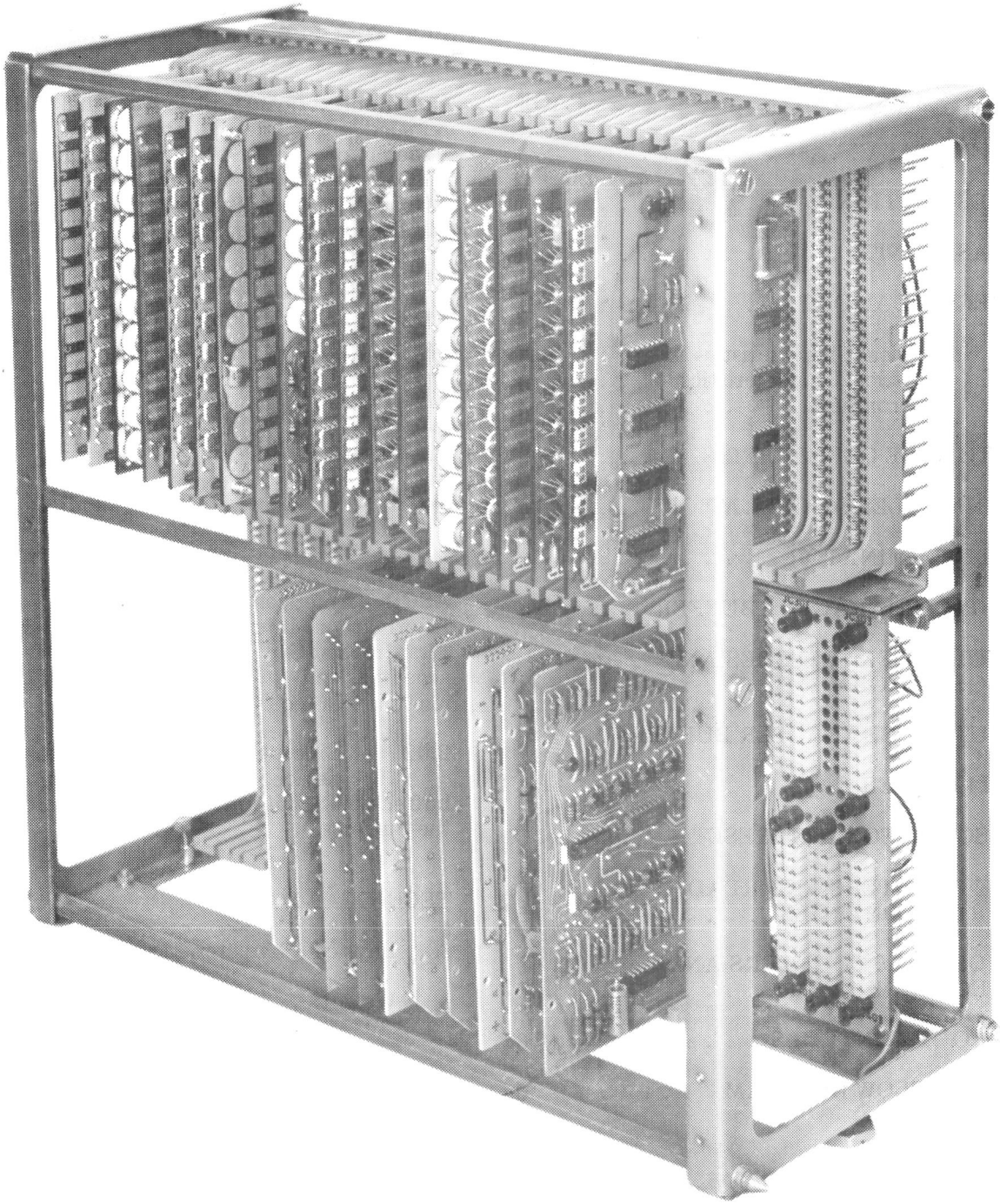

Figure 1 - CDBU801 Buffer Unit

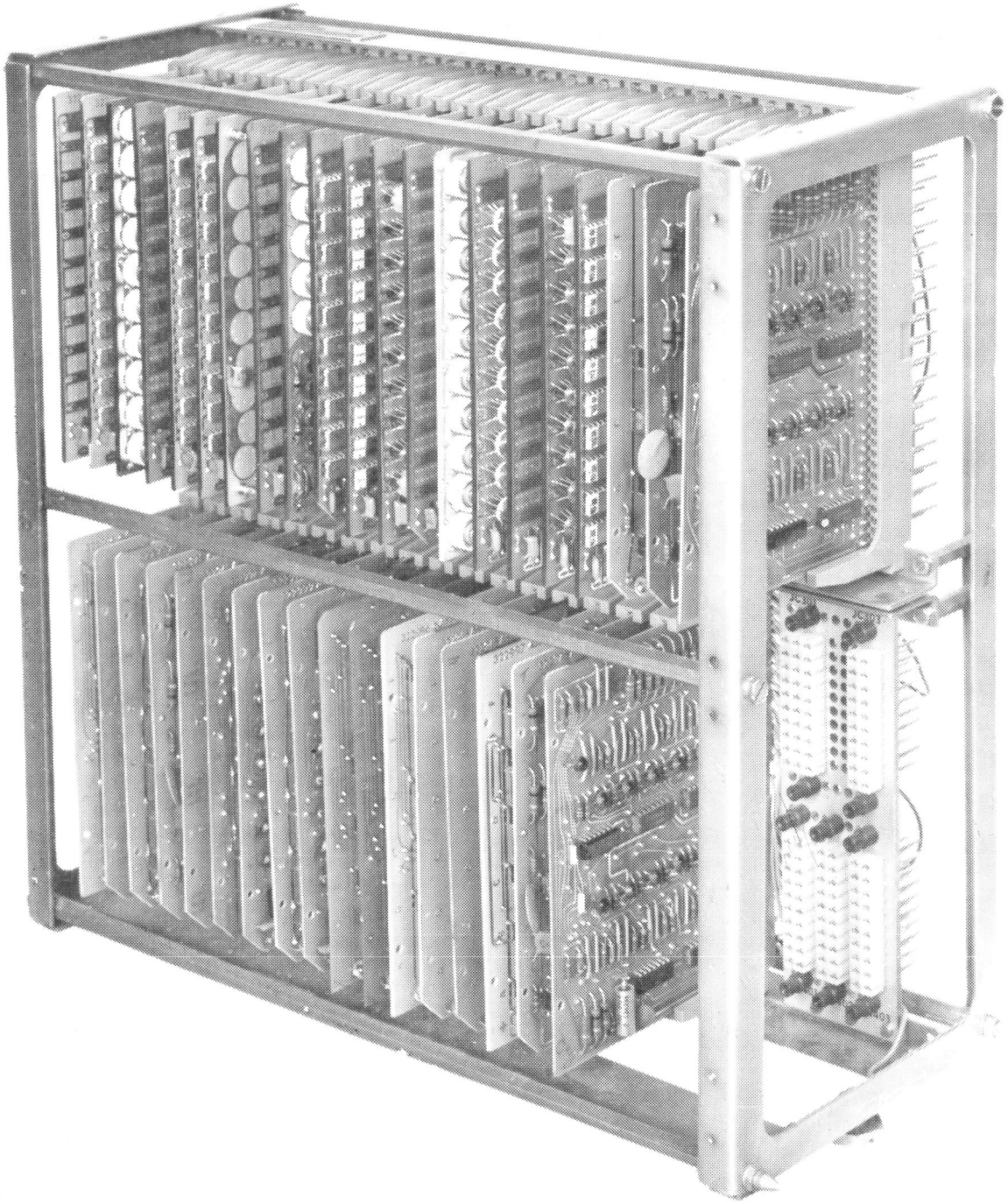

Figure 2 - CDBU802 Buffer Unit

B. Electrical Characteristics

2.03 Input voltages to the modules are as follows:

+5 v dc ±5% at 70°F (ambient)
+6 v dc ±5% at 70°F (ambient)
-11 v dc ±5% at 70°F (ambient)

C. Environment

Temperature ranges —
This equipment is intended to be operated in a room environment within the temperature range of 40°F to 110°F. Serious damage to it could result if this range is exceeded. In this connection, particular caution should be exercised in using acoustical or other enclosures.

Relative Humidity Range

Minimum	2%
Maximum	95%

STORAGE CAPABILITIES

2.04 The CDBU801 single buffer unit has a minimum storage capacity of 2000 characters. This amount can be increased in increments of 2000 characters up to a maximum of 12,000 characters.

2.05 The CDBU802 double buffer unit has two independent sections. Each section has a minimum storage capacity of 2000 characters, which can be increased in increments of 2000 characters up to a maximum of 12,000 characters. Section I has a maximum storage capacity of 10,000 characters, and Section II has a maximum storage capacity of 6000 characters, but the total combined storage of both sections cannot exceed 12,000 characters.

3. PRINCIPLES OF OPERATION

3.01 The principles of operation breaks the buffer down into various electronic operations and functions.

PTI TERMINATOR

3.02 The PTI (Parallel Terminal Interface) terminator is used to interface signals from a PTI driver by providing an interchange of control and data signals.

3.03 In the CDBU801 buffer, the input signals are applied to the terminator via the receive connector JC401. Input signals to the CDBU802 are applied to the terminator in Section I via the receive connector JC401 and in Section II via the receive connector JC303.

3.04 The parallel input data signals, b1 through b8, are in a LOW state for MARK and a HIGH state for SPACE. The control signals are in a HIGH state for the ON condition and a LOW state for the OFF condition. For all operations within the buffer unit, the data signals are HIGH or +5 volts for MARK and LOW or 0 volts for SPACE and the control signals are in a LOW state for the ON condition and a HIGH state for the OFF condition.

INPUT CHARACTER BUFFER

3.05 The input character buffer accepts the parallel data signals character-by-character at speeds up to 3000 words per minute (wpm) with a two-character buffer circuit card, MC945, or up to 12,000 wpm with a six-character buffer circuit card, MC946.

3.06 The data bits are shifted through the character buffer and applied to the multiplex switches for subsequent storage in the MOS (Metal Oxide Semiconductors) memory. The character buffer also provides control signals which indicate that it is capable of receiving additional characters, or that it is full and cannot accept more characters.

MULTIPLEX SWITCHES AND MOS MEMORY

3.07 The multiplex switches control the writing of characters from the input character buffer into the MOS memory. Selection of the proper multiplex switch for writing a character is done by the write modulo 6 counter.

3.08 Each multiplex switches circuit card, MC996, provides for the control of 2000 or 4000 characters of information. Two circuit cards are required for a storage capacity of 6000 or 8000 characters and three circuit cards are needed for a storage capacity of 10,000 or 12,000 characters.

3.09 Once the data is in the MOS memory it circulates through the multiplex switches and the MOS memory until the information is read from the memory. When data is read from the MOS memory, the multiplex switches pass the data from the memory into the output character buffer. As a character is transmitted to the character buffer, it is replaced in the MOS memory with a DELETE character (all MARK).

OUTPUT CHARACTER BUFFER

3.10 The output character buffer accepts the parallel data signals from the MOS memory and applies them to the PTI driver. The character buffer also provides control signals to the MOS memory and the in/out controls circuit card.

3.11 Character information is shifted into the output character buffer synchronously and shifted out of the character buffer character-by-character.

PTI DRIVER

3.12 The PTI driver is used to interface the signals with a PTI terminator to provide signaling compatibility between the buffer and a receiving device. Output signals from the CDBU801 are relayed to the receiving device via the transmit connector JC402. In the CDBU802, the output signals relayed to the receiving device from Section I via the transmit connector JC402, and from Section II via the transmit connector JC403.

3.13 The PTI driver accepts 8-level parallel signals from the sender and transfers them to the PTI terminator. It is used in applications where the cable distance between the PTI driver and associated PTI terminator is relatively long (up to 1000 feet).

OSCILLATOR AND RESET

3.14 The oscillator and reset circuit card, MC995, provides the clock and reset signals for the CDBU801 buffer. In the CDBU802 buffer, the card provides a common clock signal and separate reset signals to Section I and Section II.

3.15 The power-on reset signal operates for approximately one second when power is first applied to the buffer unit. This LOW signal holds the 2K counters and the modulo 6 counters in their RESET condition while the multiplex switch clears the MOS memory by inserting all MARK (DELETE) characters.

3.16 At the completion of the power-on reset, a delayed reset signal, which is HIGH for 2 ms, is applied to the input and output character buffer to clear them of false data that may have been inserted at turn-on.

Note: The "ϕ" symbol means "phase."

3.17 The oscillator circuit provides a $\phi 1$ and $\phi 2$ clock pulse that drives the MOS memory. The $\phi 1$ and $\phi 2$ are both continuous pulses which are HIGH (ON) for 250 ns and LOW (OFF) for 750 ns. These two pulses are separated by a 500 ns interval. The $\phi 1$ signal is also used to drive the 2K counters while an inverted $\phi 1$ signal is used to clock the input and output character buffer.

2K COUNTERS AND READ/WRITE CONTROLS

3.18 The write modulo 2K counter and read modulo 2K counter are synchronous binary counters that are reset to the zero count after 2000 counts of the $\phi 1$ clock pulse. Each counter provides a reset pulse that is equal to the period of the $\phi 1$ clock pulse. These counters determine when to perform the WRITE and READ operations.

3.19 The WRITE or READ operation is performed during the RESET of the respective counter and is accompanied by the inhibiting of one $\phi 1$ clock pulse for each character written into or read from the MOS memory. Thus, when normal counting is resumed, the counter will be delayed from its original counting rate.

3.20 As an example, assume that the write and the read modulo 2K counters are both in synchronism. If two characters are written into the MOS memory, the $\phi 1$ clock pulse is inhibited for two $\phi 1$ clock times. At the end of the WRITE operation normal clocking continues but the RESET of the write modulo 2K counter occurs two $\phi 1$ clock pulses after the RESET of the read modulo 2K counter.

3.21 The phase difference between the two counters remains until another WRITE or READ operation is performed. Since the counters are clocked at the same rate as the MOS memory, the location in the MOS memory addressed by the counter changes each time a bit is written into the memory. Thus, the bits are recorded into adjacent locations in the MOS memory.

3.22 At the reset of the write 2K or read 2K counter, a clock pulse is provided which clocks the respective modulo 6 counter.

MODULO 6 COUNTERS AND DECODERS

3.23 The modulo 6 counters select the proper multiplex switches to be used for the WRITE and READ operation. Since the multiplex switches are separated by 4000 characters of MOS memory and the modulo 6 counters are pulsed once for each count of 2000 characters, the modulo 6 counters recognize two successive counts to address one of the multiplex switches circuit cards.

3.24 With both the CDBU801 and CDBU802 buffers having variable storage capabilities from 2000 to 12,000 characters, it is necessary to have a programmable RESET of the modulo 6 counters. This programmed reset is achieved with the six screws located on the MC998 circuit card.

3.25 The MC998 circuit card also contains a circuit that detects and indicates a BUFFER FULL condition. This circuit gives an indication only when the buffer is full and there is no End-of-Transmission (EOT) character in the MOS memory. With one or more EOT characters in the memory, only the normal inhibiting of input data occurs via the interface.

3.26 The external release lamp and switch on the associated CDT terminal set provides an indication of a BUFFER FULL condition with no EOT in the MOS memory. Depression of the external release switch manually overrides this condition and allows transmission from the buffer unit if the receiving device is ready to accept the data from the buffer.

> Note: There is a strapping option available so that either Section I or Section II of the CDBU802 can utilize the external release switch. This information can be found in the appropriate circuit description.

IN/OUT CONTROLS

3.27 The in/out controls circuit card contains input control circuits that perform message control functions for the buffer unit. The output control circuits provide message control and character control of the shifting out of data from the output character buffer circuit card.

3.28 Transmission of data from the buffer cannot begin until at least one EOT character is in the MOS memory. The output control circuits are inhibited until an EOT character is recognized in the MOS memory. This EOT character is received at the end of each message transmitted to the buffer.

3.29 Once the output control circuits are enabled, transmission of data from the buffer continues until the EOT character is detected in the last stage of the output character buffer circuit card.

3.30 EOT character control of the transfer of data from the buffer unit can be bypassed with the insertion of two straps on the in/out control circuit card MC997. Selection of this option allows data transmission from the buffer to begin as soon as information is stored in the MOS memory providing that the receiving device is ready to accept this data.

4. DATA FLOW DIAGRAM

4.01 The flow of data through either the CDBU801 or CDBU802 buffers using 2000 character storage, is shown in Figure 3.

4.02 The vertical dashed line separates the basic parts of the buffer by individual circuit cards. The heavy black line shows the path that the data follows as it steps through the buffer.

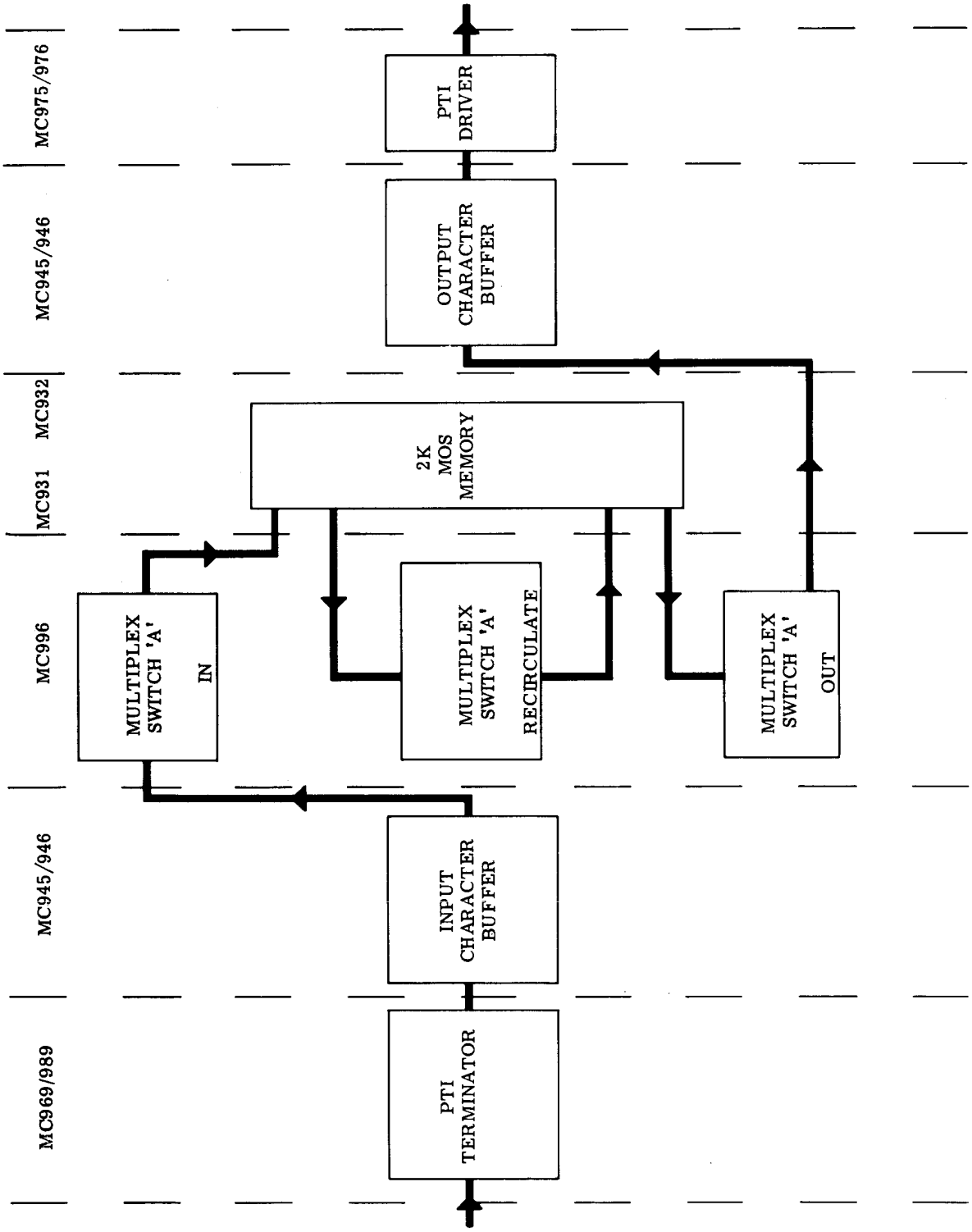

Figure 3 - Data Flow Diagram