COMMUNICATIONS DISPLAY TERMINAL BUFFER MODULE CDBU804

FOR USE WITH THE STATION CONTROLLER INTERFACE MODULE

DESCRIPTION AND PRINCIPLES OF OPERATION

CONTENTS

1. GENERAL

1.01 This section provides the description and principles of operation for the communications display buffer module CDBU804. Issue 1 of this section was a limited printing edition and did not receive general distribution. This reissue incorporates the latest engineering design information available at this time. For information concerning installation, checkout, and troubleshooting, refer to Section 578-120-201.

1.02 The CDBU804 buffer unit is designed to be used with the 2510 or 2511 Communications Display Terminal. This buffer provides a temporary storage facility for data that has been transferred through the station controller to an off-line Model 37 or INKTRONIC ® printer. This buffer unit is a solid state device that can also be used with a single station controller in an interface module and a cluster controller with a group of off-line receiving devices.

1.03 This buffer is designed for storage and transmission of 7-bit level ASCII (American National Standard Code for Information Interchange) with the eighth-bit level used for even parity. The buffer has a storage capacity of 2000 characters. The 2000 character arrangement may be expanded to 4000 by adding two extra MC955 and MC956 circuit cards and changing the strapping options on the module wiring field.

2. DESCRIPTION

2.01 The CDBU804 buffer unit interfaces with a hard copy printer by the EIA (Electronics Industries Association) Standard RS-232-C. The input data is received from the CDIF814 station controller (Figure 1) or cluster controller. The design of the buffer unit allows only one message to be entered into storage at a given time. Once a valid message has been entered, the buffer goes into a nonselectable condition and remains in this condition until the message has been completely transmitted to the

Prepared for American Telephone and Telegraph Company by Teletype Corporation

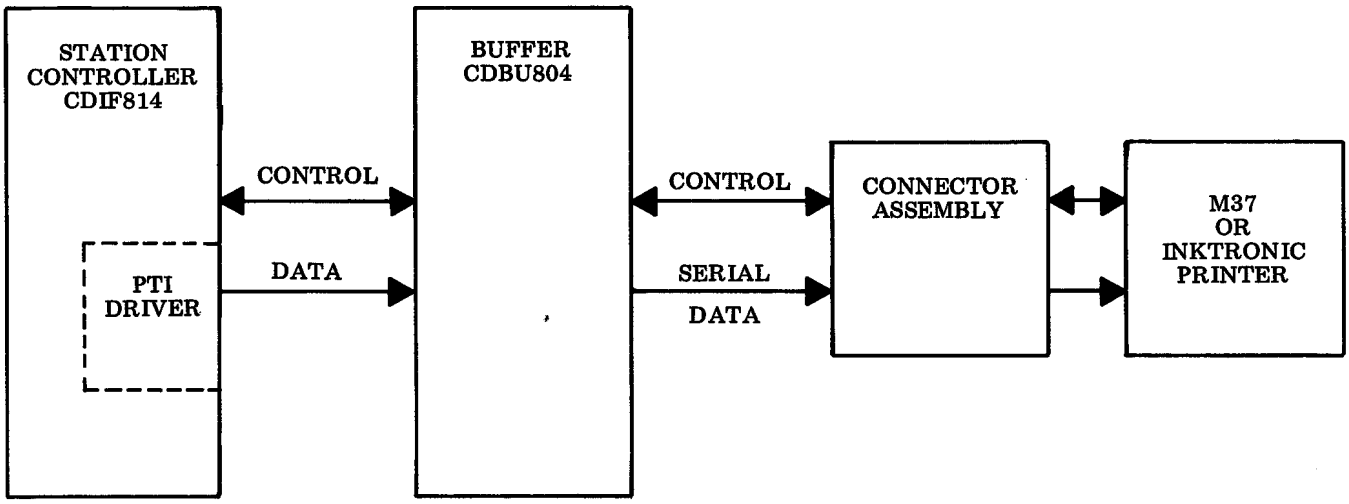


Figure 1 - Typical Set Diagram

hard copy printer. When transmission is complete, the buffer becomes selectable and will accept new data. Readout from the buffer is the destructive type. As each character is transmitted it is erased from memory and replaced with a delete character leaving all bits marking.

2.02 An error control feature is incorporated into the buffer unit so that only valid messages will be transmitted from the buffer after the receipt of a signal from the input device indicating that no errors have been detected. The buffer unit uses dynamic storage; loss of power to the buffer results in a loss of any information contained in the buffer.

Components

2.03 This buffer module contains mounting and interconnecting of electronic circuit cards and their connectors (Figure 2). Attached to connectors are input, output, and power cables. The circuit cards used in this buffer are:

MC091 Transmitting Distributor
MC512 2K Counters and Read/Write Control
MC514 Buffer Error Control
MC515 In/Out Controls
MC645 Input Character Buffer
MC645 Output Character Buffer
MC955 Three Level MOS Memory
MC956 Two Level MOS Memory

Note 1: The 2000 character arrangement requires two MC955 and one MC956 cards. The 4000 character arrangement requires four MC955 and two MC956 cards.

MC969 Parallel Terminal Interface Terminator
MC983 Serial (EIA) Interface
MC995 Oscillator and Reset
MC996 Multiplex Switch
MC998 Modulo 6 Counters and Decoders
MC977 Clock (1200 Baud for INKTRONIC)
MC961 Clock (150 Baud for Model 37)

Note 2: Only one clock circuit card is used with each arrangement.

2.04 The serial output interface is provided by the serial EIA interface circuit card. The serial data is derived from the transmitting distributor and converted to an EIA signal in the serial EIA circuit and sent out to the hard copy device.

2.05 The transmission speed is determined by the frequency of the clock circuit. Two clock circuits are available: 150 and 1200 baud. Additional EIA signals are used for control of the interface.

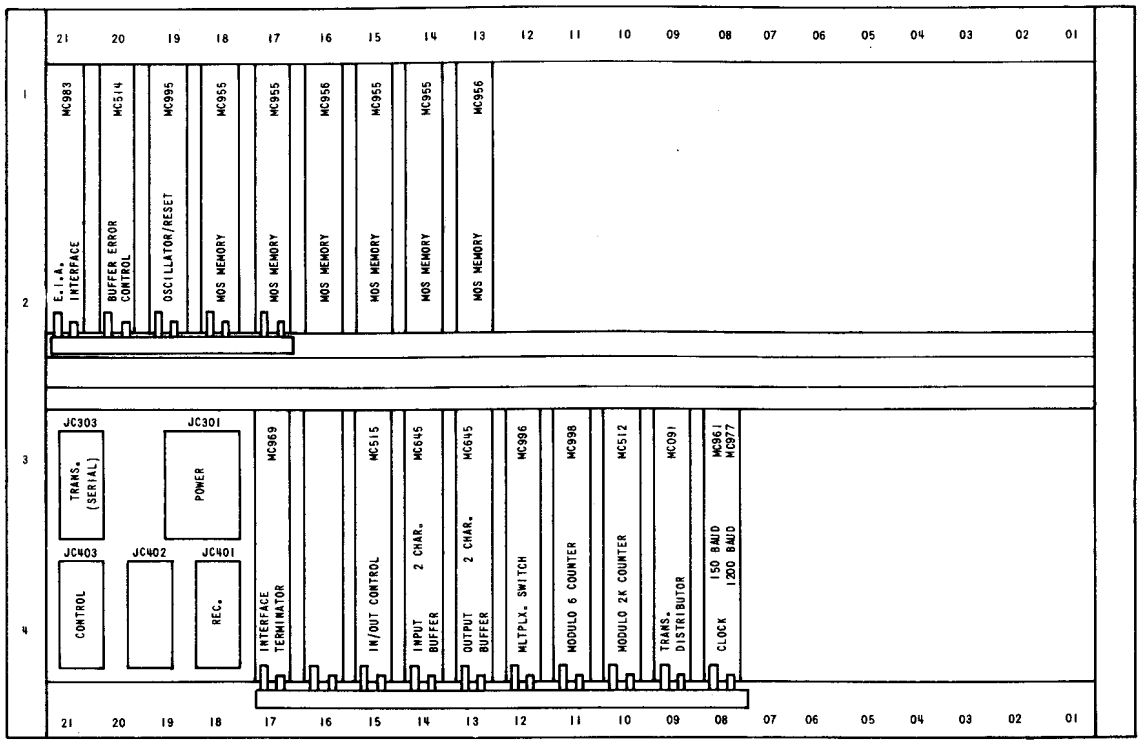


Figure 2 - CDBU804 Buffer Card Location

Wiring Options

2.06 Wiring options (a) through (g) provide the various signaling requirements of the receiving devices; these options are as follows:

(a) Provide 10-unit code for transmitting distributor

(b) Provide 150-baud clock for transmitting distributor

(c) Unit operation without a data set or motor control

(d) 2000 characters of storage

(e) 4000 characters of storage

(f) Provide 1200-baud clock for transmitting distributor

(g) Unit operation without a data set but with motor control.

2.07 All factory units are strapped for 10-unit code for the output of the transmitting distributor and are strapped for operation without a data set and with motor control.

2.08 Early designed units were factory wired for operation without a data set or motor control. For information on the circuit card strapping, refer to 9355WD and Section 578-120-201.

2.09 The following is a list of the common abbreviations and functional designations that will be helpful in understanding the operation of the buffer:

ϕ1	Clock Phase One
ϕ2	Clock Phase Two
ϕMV	Multivibrator Output
b1-b8	Code Bit No. 1 Through Code Bit No. 8
BFA	Buffer Full Alarm
CA	Character Available

CP	Clocking Pulse
DRS	Delayed Power-On Reset
EXR	External Release
IRO	Inhibit Read on Odd Modulo 6 Count
IWO	Inhibit Write on Odd Modulo 6 Count
LOI	Last Operation Indicator
MCS	Modulo 6 Counters Synchronized
PNC	Present Next Character
PRS	Power-On Reset
PTI	Parallel Terminal Interface
RCA	Receiver Character Available
RCL	Read Control
RD	Read From Memory
RDA	Receive Data Acknowledge
RDI	Read Initial Data
RDE	Receive Data Error
RM	Receive Message
RNC	Request Next Character
RR	Receiver Ready
RS	Receiver Selectable
SCA	Sender Character Available
SIN	Shift In
SM	Send Message
SOT	Shift Out
SR	Sender Ready
SS	Sender Selectable
WCL	Write Control
WR	Write in Memory
WRI	Write Initial Data

EIA Signal Abbreviations

RTS	Request to Send
DSR	Data Set Ready
CTS	Clear to Send

3. TECHNICAL DATA

Physical Characteristics

3.01 The module is an open metal frame with positions for 38 card connectors and five positions for input and output cable connectors. It has two locating pins at the lower rear of the frame and one mounting thumb screw in front. The module is designed to be mounted in the apparatus cabinet. The weight and dimensions of the metal frame with the circuit cards are as follows:

Weight	15 pounds
Height	14 inches
Width	6 inches
Depth	15 inches

Electrical Characteristics

3.02 The input voltages to the module from the power supply are:

+5 volts dc ±5% at 70°F ambient
+6 volts dc ±5% at 70°F ambient
-11 volts dc ±5% at 70°F ambient

Environment

3.03 Ambient temperature (outside module):

Minimum	40°F
Maximum	110°F

3.04 Relative humidity range:

Minimum	2%
Maximum	95%

Input Interface Signaling

3.05 Input interface signaling requires three inputs and these inputs use TELETYPE® Parallel Terminal Interface (PTI) signaling which may be used up to 1000 feet between a driver and the terminator circuit. These input data interface conditions are as follows:

Control Signals

Message Characters

Error Control Signals.

3.06 The data signals are parallel with the following conditions:

Low — 0 state — mark

High — 1 state — space (ON).

3.07 The input signals are low, 0 state, for mark; and a high, 1 state, for space. These signals are used in the transfer of parallel data. Control signals are in a low, 0 state, for an off condition; and a high, 1 state, for an on condition. The high state is defined by 20 ma current flow from the driver through the terminator input diode and returned to ground at the driver supply. Voltage indications in this current loop would be approximately +4 volts in 1 state when referenced to ground at the driver and when the source voltage to the driver is +5 volts. In the low, 0 state, no apparent current should flow in the loop, less than 3 microamperes, and the voltage indications would be 0 volts.

Output Interface Signaling

3.08 The output interface signaling of the buffer unit is 8-level serial signals that correspond to EIA RS-232-C. The output speed can be either 150 or 1200 baud. The control signals are outlined in Table A and the cable length can be up to 50 feet between the buffer and the receiving device.

TABLE A

CONTROL SIGNALS

DESCRIPTION	LOW	HIGH
Binary State	0	1
Signal Condition	Mark	Space
Input Voltages *	0	+4
Output Voltages	-3 to -25	+3 to +25
Control Functions	OFF	ON
Input Current	73 μa	20 ma

* When referenced to ground at the driver and the source voltage to the driver is +5 volts.

Power Supply

3.09 The buffer unit requires a low voltage power supply (CDPS802) that is mounted in the apparatus cabinet of the associated display module. The input voltages that are derived from the power supply are listed under Electrical Characteristics.

Input Interfacing

3.10 Input from controller to buffer consists of eight parallel data leads for the transfer of the ASCII 8-level code. Additional signals in this interface are included in Table B for the message and character control.

Error Control

3.11 The error control input consists of two symbols from the controller to the buffer; these are:

Controller — Receive Data Acknowledge → Buffer

Controller — Receive Data Error → Buffer

3.12 One of these two must be sent to the buffer after message transmission to direct the buffer to either forward the message or to erase it from storage.

Output Interfacing

3.13 The data terminal ready signal from the receiving device may be applied to the buffer where it is used as the data set ready and clear to send signals. The request to send signal from the buffer may be used as the data set ready signal to the receiving device. Send data at the buffer becomes receive data at the receiving

TABLE B

INPUT INTERFACING

MESSAGE CONTROL SIGNALS		
Buffer	RECEIVE SELECTABLE →	Controller
Buffer	← RECEIVE MESSAGE	Controller
Buffer	RECEIVE READY →	Controller
CHARACTER CONTROL SIGNALS		
Buffer	NEXT CHARACTER →	Controller
Buffer	← CHARACTER AVAILABLE	Controller

device. Both the buffer and the receiving device signal and protective ground leads are tied together.

3.14 The buffer data terminal ready signal is used to drive its data set ready signal. The request to send signal may be used to drive the carrier detect and/or data set ready input at the receiving device. The secondary transmit data from the receiving device may be used to drive the clear to send input of the buffer. Wiring options provide for additional output interfacing to satisfy the requirements of various receiving devices.

4. PRINCIPLES OF OPERATION

4.01 The principles of operation portion of this section is broken down by the interfaces used and the circuit cards (Figure 3). The electrical operations and functions will be displayed by block diagrams and flow charts. For detailed functional operation of the power supply and circuit cards, refer to the WDP 0331 package associated with this buffer unit.

PTI TERMINATOR

4.02 The Parallel Terminal Interface (PTI) terminator (MC969) is used to interface message control, character control, and data signals from the PTI driver circuit (MC976) located in the station controller module.

4.03 Input signals to the buffer unit are applied to the PTI terminator via the receive connector JC401. As the signals pass through the cable interconnecting the PTI driver circuit and terminator the signals are in the following states:

Data Signals
Bit 1 through bit 8 are low for mark and high for space.

Control Signals
High for on
Low for off.

INPUT CHARACTER BUFFER

4.04 The input character buffer accepts parallel data signals serially (character-by-character) at speeds up to 3000 wpm (words per minute) with a two character circuit card (MC645). The six character circuit card (MC646), not standard to this unit, provides up to 12,000 wpm and is available on special order.

4.05 The data bits are processed through the shift register and applied to the multiplex switches for storage in the memory. The character buffer also provides internal control signals which indicate that it is capable of receiving additional characters, or that it is full and cannot accept more characters.

MULTIPLEX SWITCHES

4.06 The multiplex switch receives input data from the input character buffer. This data is gated to the recirculated MOS memory in conjunction with the in/out control circuit (Figure 4). When a write signal is entered into the write amplifiers, the data is gated into the MOS memory and can be read out when the read amplifier receives the signal to give data to the output character buffer. All data to and from the multiplex switches are in parallel form.

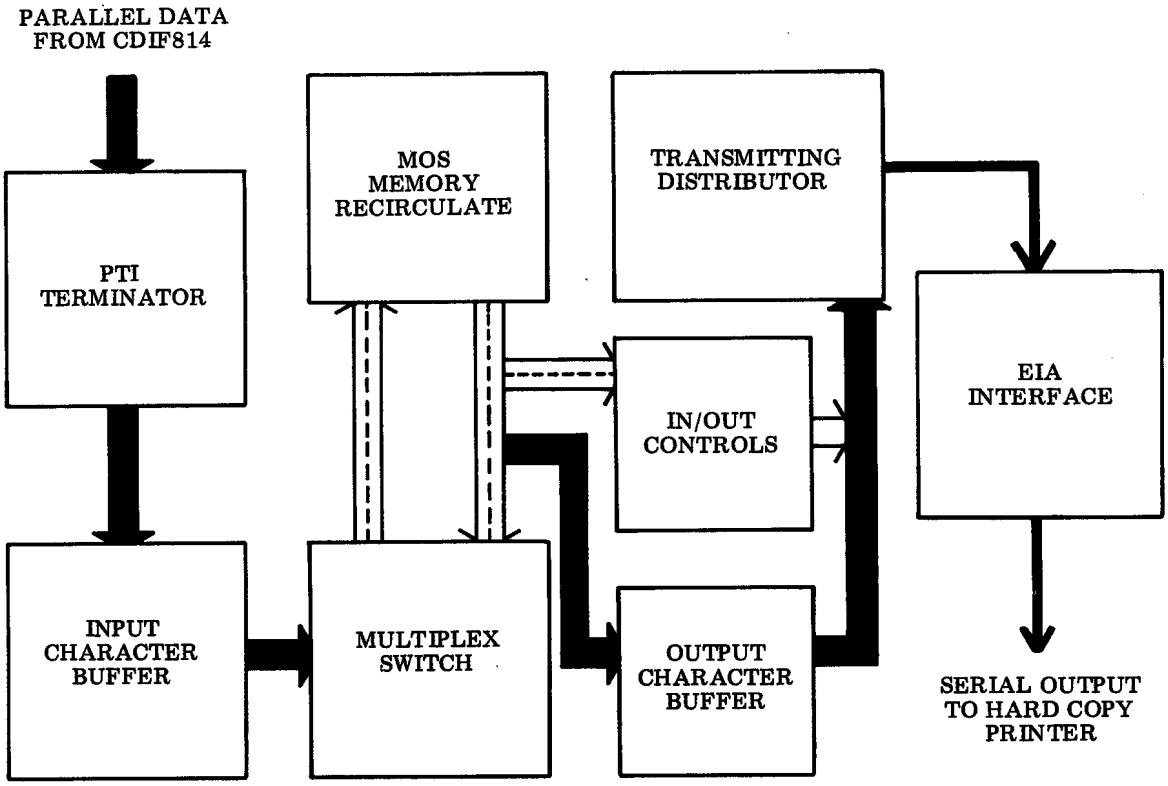
4.07 The multiplex switches control the writing of characters (Figure 5) from the input character buffer into the MOS memory. Selection of the proper multiplex switch for writing a character is done by the write modulo 6 counter.

4.08 The multiplex switches circuit card (MC996) controls the writing of characters from the input character buffer into the 2-thousand character (2K) or 4-thousand character (4K) MOS memory circuit cards. Similarly, it also controls the reading of characters from the MOS memory into an output character buffer circuit card.

4.09 Upon completion of message control signaling, the buffer module signals it is ready to receive data. Data begins transfer from the input character buffer, through the multiplex switches and into the MOS memory. Data transfer continues until the message terminating character is entered into the MOS memory.

4.10 When data is read from the memory, the multiplex switches pass the data from the memory into the output character buffer. As a character is transmitted to the character buffer, it is replaced by a DELETE character (all mark) in the memory of the multiplex circuit. The data placed in the recirculate MOS memory does not change until it is replaced by another character.

4.11 Eight identical sets of switches provide for control of eight individual code levels. Common amplifiers drive the switch gates



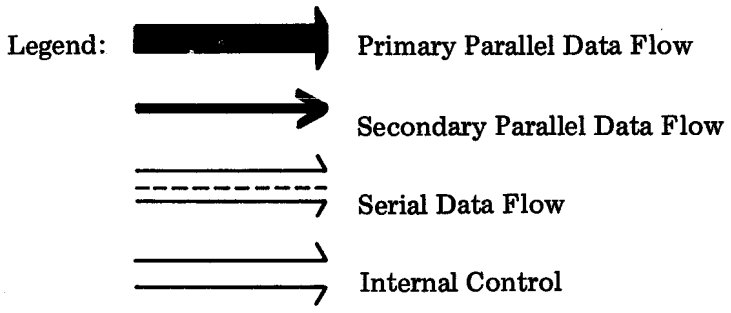


Figure 3 - Buffer Data Flow Diagram

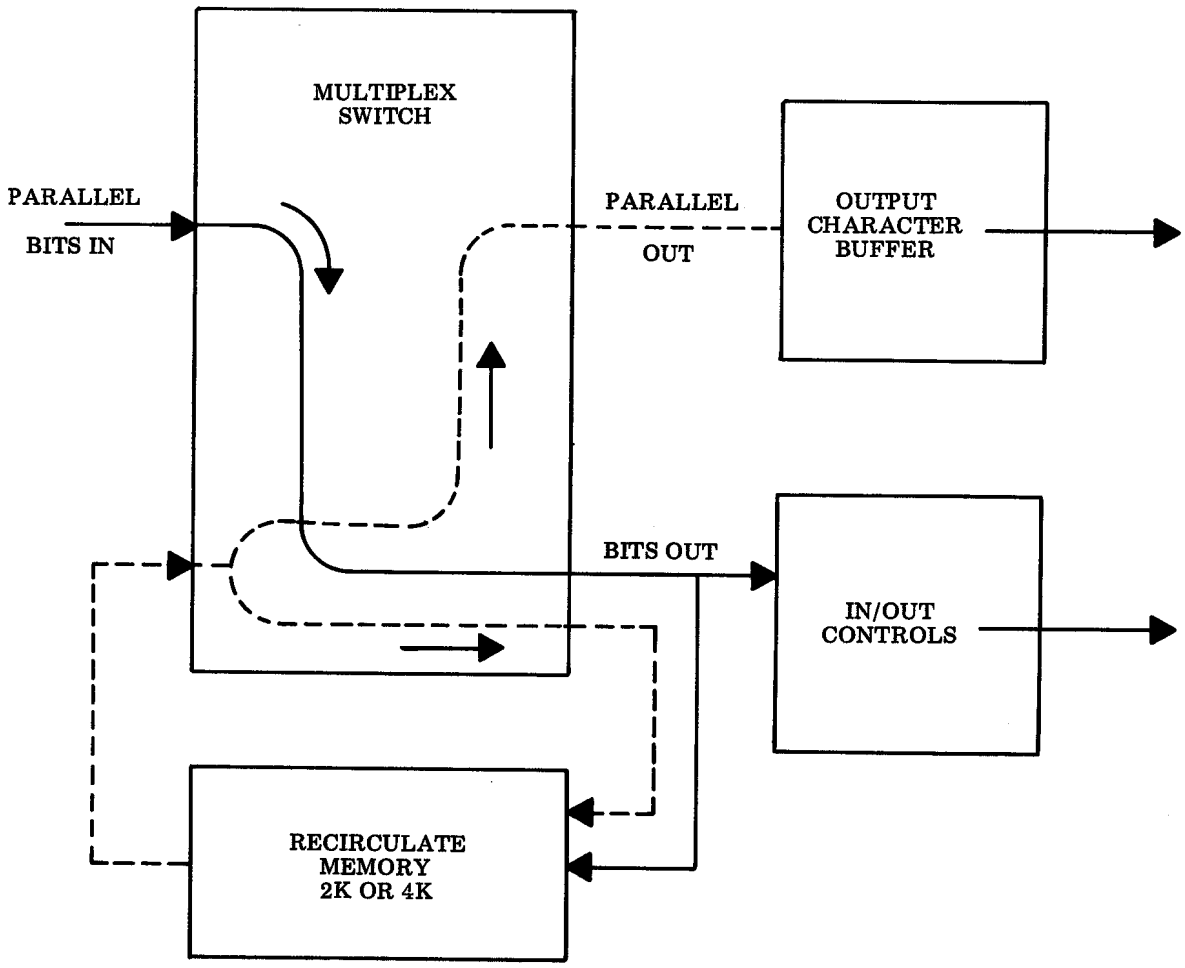


Figure 4 - Multiplex Switch and Recirculate Memory Flow Chart

for the read, write, and recirculate functions. The multiplex circuits in a buffer unit are designated A, B, C, etc, with the A circuit card controlling the first 2000 or 4000 characters, the B card controls the next group of characters.

4.12 The character bit information from the output of the MOS memory passes directly through the two groups of enabled gates and recirculates the data bits back into the MOS memory.

THREE AND TWO LEVEL MOS MEMORIES

4.13 The three and/or two level MOS memories receive data bits from the multiplex switch circuit. This data is received in parallel form and recirculated in the three and two level MOS memory circuits. These two circuit (MC955 and MC956) assemblies contain the following:

(1) Serial dynamic shift register storage that is capable of storing 2000 bits of information per code level.

(2) The shift register driving amplifiers which are controlled by "shift in" (phase 1) and "shift out" (phase 2) clock pulses.

4.14 The three level MOS memory, card number MC955, has three groups of shift registers; the two level memory, card number MC956, has two groups of shift registers. These two circuits make up the recirculating memory (one MC956 and two MC955) located in the metal frame at positions ZC116, ZC117, and ZC118. Each group of shift registers is contained in ten MOS packages; each package provides storage of 200 bits of information. Each level supplies storage for one level of data code.

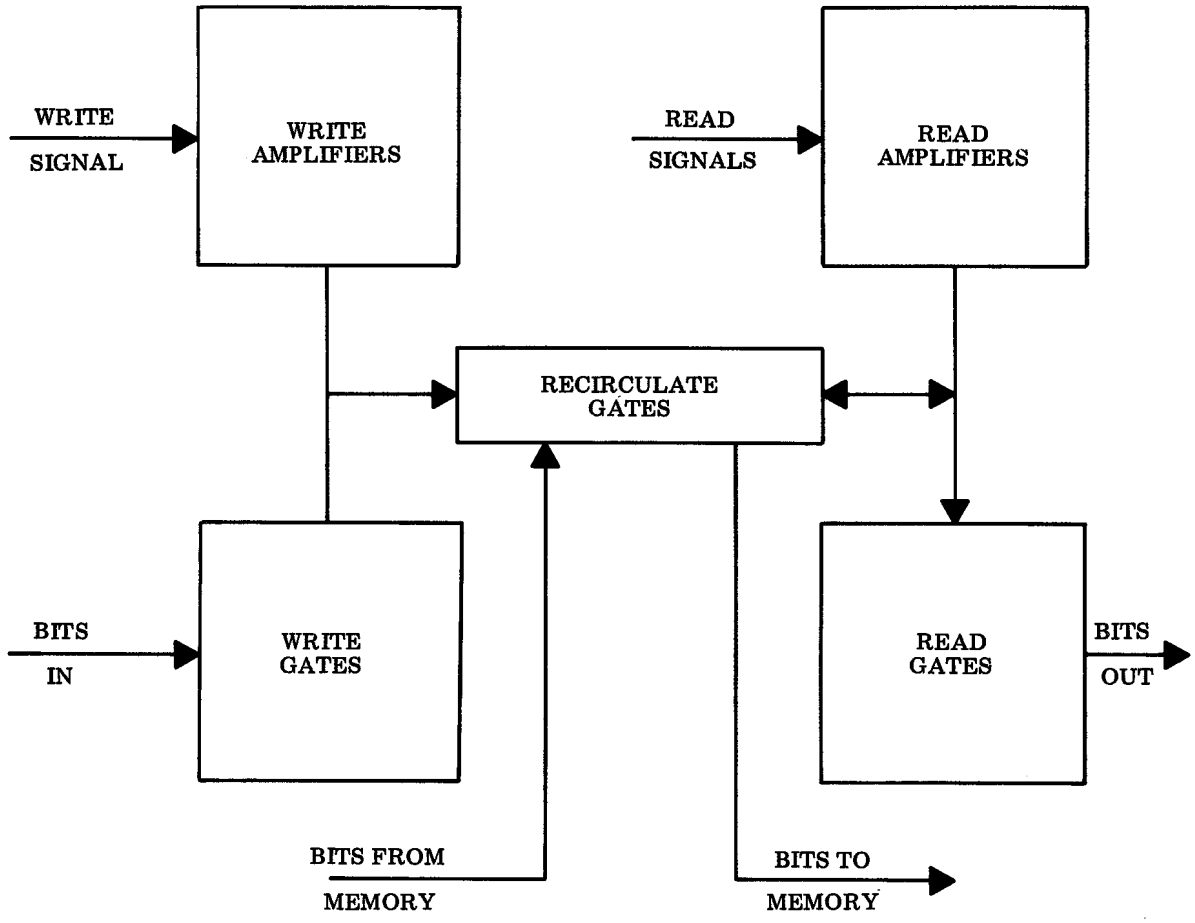


Figure 5 - Multiplex Switch Controls

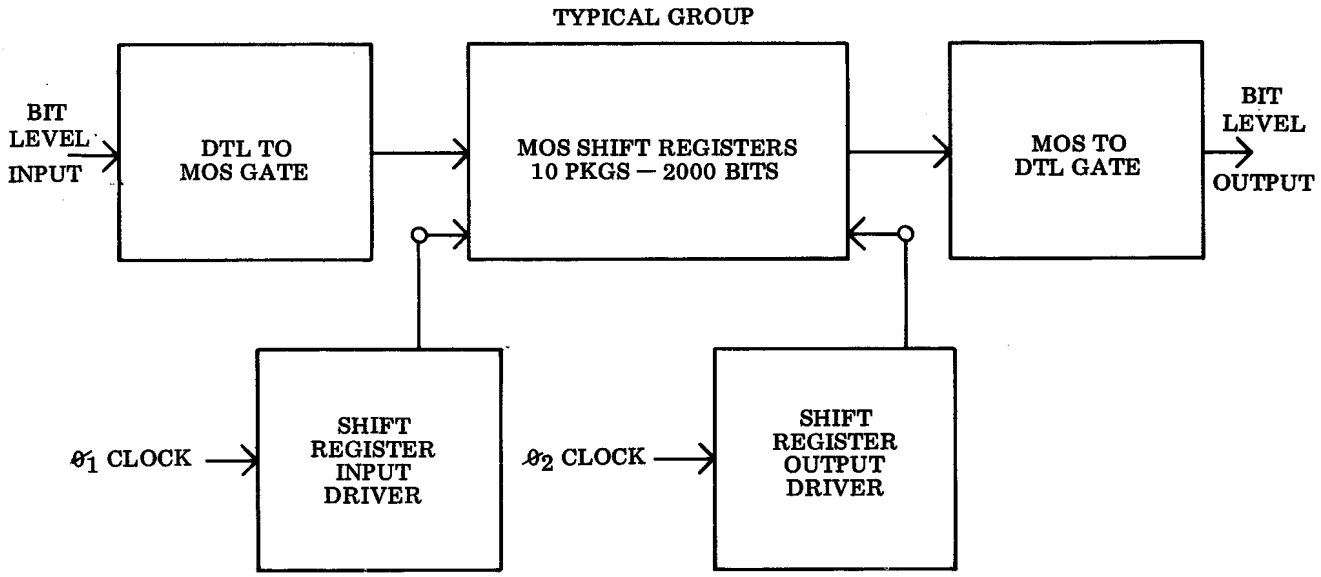
4.15 The "shift in" shift register driver employs the phase 1 (ϕ1) clock (Figure 6) pulse to shift data into the MOS registers. The "shift out" shift register driver employs the phase 2 (ϕ2) clock pulse to shift data out of the MOS registers.

ERROR CONTROL

4.16 The error control circuit (MC514) provides message control interfacing between the input and output of a buffer unit. Two inputs are available from the controller for control of a message that has been placed in the MOS memory of the associated buffer. One input allows the buffer to transmit the message out of the memory. The other input causes the message to be erased from the memory without being transmitted. Both inputs can be controlled from an external location by the PTI-type signal levels.

4.17 The simplified flow chart (Figure 7) concerns the basic inputs and outputs of the error control circuit. The two input signals are from the controller to the buffer: these are receive data acknowledge (RDA) and receive data error (RDE). One of these two signals must be sent to the buffer after the transmission of the message to direct the buffer to either forward the message or erase it from storage. While a message is being transmitted out of the buffer the MC514 card causes the buffer input to be blinded until the transmission has been completed.

4.18 Upon completion of a message, the buffer will retain the message in the memory until a RDA or RDE signal is received from the station controller. The RDA indicates that the message is valid and the buffer may proceed to transmit the message.



Note: CDT and CDIF814 use pin 25 for phase 1 (pins 26, 27, and 28 open) and for phase 2, only one pin is used and the rest are left open as in phase 1.

Figure 6 - Three and Two Level MOS Memories Flow Chart

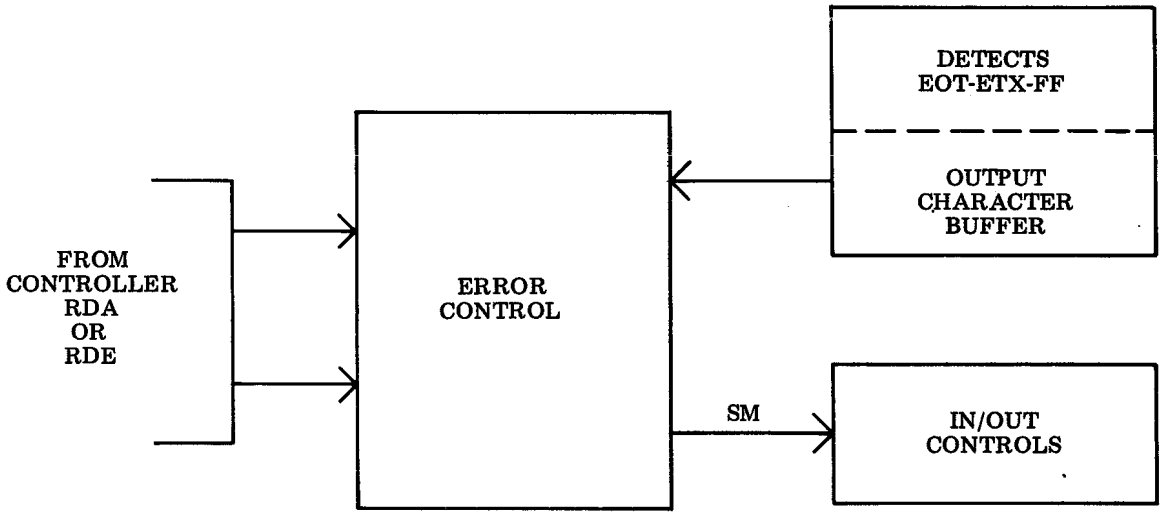


Figure 7 - Error Control Flow Chart

4.19 RDE signal would indicate that the station controller has found an error in the message and should not be transmitted. When the RDE signal is received by the buffer, a master reset to the MC995 card generates a power-on reset cycle to clear the message out of the buffer memory circuits.

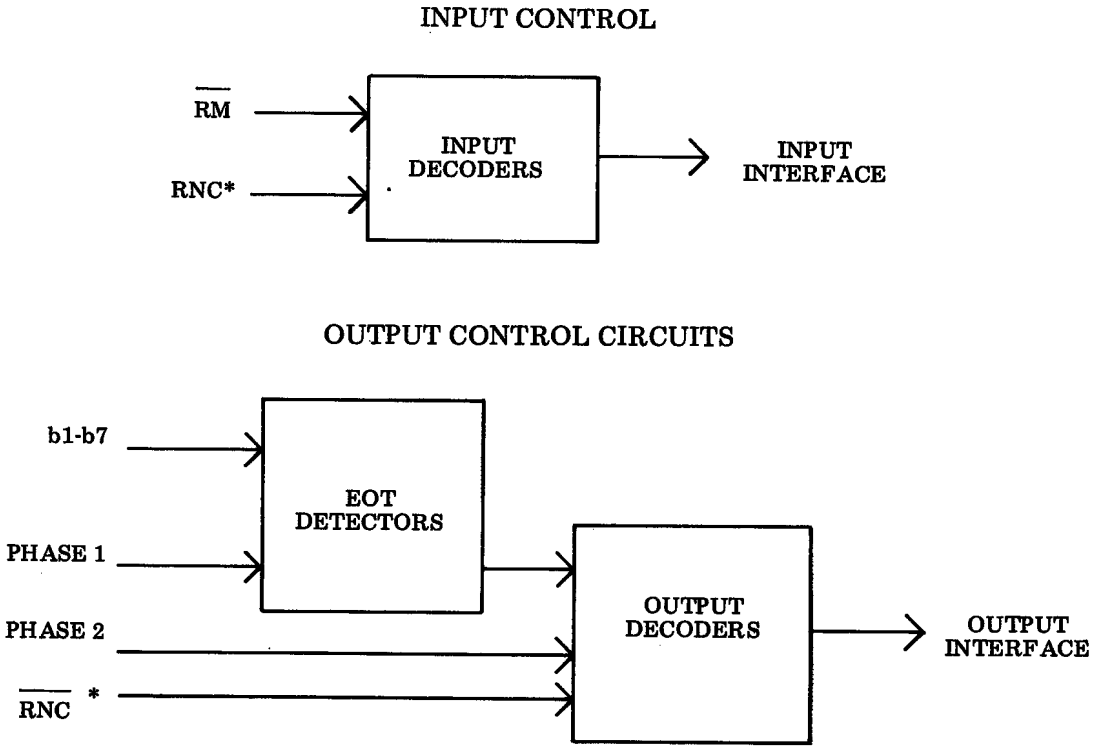
4.20 If the buffer receives the RDA signal, the message interfacing is completed by the buffer error control circuit card (MC514) generating the message (SM) signal to the in/out controls circuit card (MC515). Once the output control circuits are enabled, transmission of data from the buffer to the hard copy receive device continues until the end character (EOT, ETX, or FF) is detected in the last stage of the output character circuit card.

OUTPUT CHARACTER BUFFER

4.21 The buffer module is designed to provide an output interface to a hard copy receive device in either a serial or parallel data flow depending upon the module arrangement selected. The output character buffer accepts parallel data bit signals from the MOS memory and applies them to a PTI driver or serial transmitting distributor. The character buffer also provides control signals to the MOS memory and the in/out controls circuit card. Character information is shifted into the output character buffer synchronously and shifted out of the character buffer character-by-character.

IN/OUT CONTROLS (Figure 8)

4.22 The in/out control circuit (MC515) provides circuits to operate on the message and character control signals at the input and output interface. Input control signals perform control functions for the buffer unit. The output control signals provide for character control of the shifting out of data from the output character buffer circuit card. Message terminating character detection codes EOT, ETX, or FF are used at both the input to and output from the buffer memory units.



*From the input character buffer.

Figure 8 - In/Out Controls Flow Chart

4.23 Data transmission into the buffer continues through the input character buffer, multiplex switch, and into the MOS memory where it is circulated until the message terminating character has been received. An option screw is provided on this card to enable detection of any one of the three characters. The character programmed into the card, when detected, indicates that a complete message is stored into the memory.

4.24 Transmission of data from the buffer cannot begin until the ETX, EOT, or FF character is in the MOS memory. The output control circuits are inhibited until the character is recognized in the MOS memory. An ending character must be received at the end of each message transmitted to the buffer.

TRANSMITTING DISTRIBUTOR

4.25 The transmitting distributor is required for serial EIA interface. The distributor receives parallel data from the output character buffer and control signals from the in/out control circuit (MC515). The output is serial data to the EIA interface circuit. The basic function is to switch the length of the code from 6 to 11 units. The parallel input data signals are converted to a serial output signal with the length determined by electrical controls and the speed determined by an external clock.

4.26 This distributor is capable of transmitting a start-stop code or a start-bit synchronous code with one stop bit. Two clock sources can be used for transmission: an external bit or a free running clock that operates at 64 times the baud rate.

4.27 The transmission is a 10-unit code. This option is implemented by wire strapping on the module.

4.28 For a detailed description of the input and output characteristics, refer to 2091 circuit description.

OSCILLATOR AND RESET CIRCUITS

4.29 The oscillator and reset circuit is composed of a crystal oscillator with frequency out-dividing facilities which produce master clock pulses for the buffer unit. The reset circuitry is used for conditioning the circuits in the buffer unit to control clearing and starting when power is applied to the unit. The clearing function is first performed, followed by the generation of enabling pulses that start the associated circuits with the proper timing.

4.30 The power-on reset signal operates for approximately one second when the power is first applied to the buffer unit. This low signal holds the 2K counters and modulo 6 counters in their reset condition while the multiplex switches clear the MOS memory by inserting all mark (DELETE) characters.

4.31 The EIA serial output to the receiving device has a separate clock pulse signal to supply the bit timing to the serial transmitting distributor.

4.32 At the completion of the power-on reset signal, a delayed reset signal (which is high for 2 ms) is applied to the input and output character buffer to clear them of false data that may have been inserted at turn-on.

4.33 The oscillator circuit, with clock pulses 1 and 2, drives the MOS memory and timing of the read and write operations of the buffer. Both these pulses are continously high (on) for 250 nanoseconds and low (off) for 750 nanoseconds. These two pulses are separated by a 500 nanosecond interval.

2K COUNTERS AND READ/WRITE CONTROLS (MC512)

4.34 The write modulo 2K counter and read modulo 2K counter determine when to perform the write and read operations (Figure 9). These counters are synchronous binary counters consisting of shift registers that are reset to zero after 2000 counts of the phase 1 clock pulse. Each counter provides a reset pulse that is equal to the period of the phase 1 clock pulse. The write and read operations function through associated multiplex switches (MC966) at associated MOS memory circuits in the buffer unit.

4.35 The write operation is performed during the reset of the write modulo 2000 synchronous binary counter. This counter is reset when the coupled gates tied to the outputs of the binary counter detect the binary count of 1999.

4.36 When the counter detects 1999, the output gate goes low which activates the parallel enable (PE) inputs to the three counters. On the next phase 1 clock pulse received on terminal 3 (write into memory signal), the counter is reset to zero.

4.37 The read operation (similar to the write operation) is initiated when the counters are reset, circuit conditions are met, (refer to 1512CD), and the MOS memory is not empty.

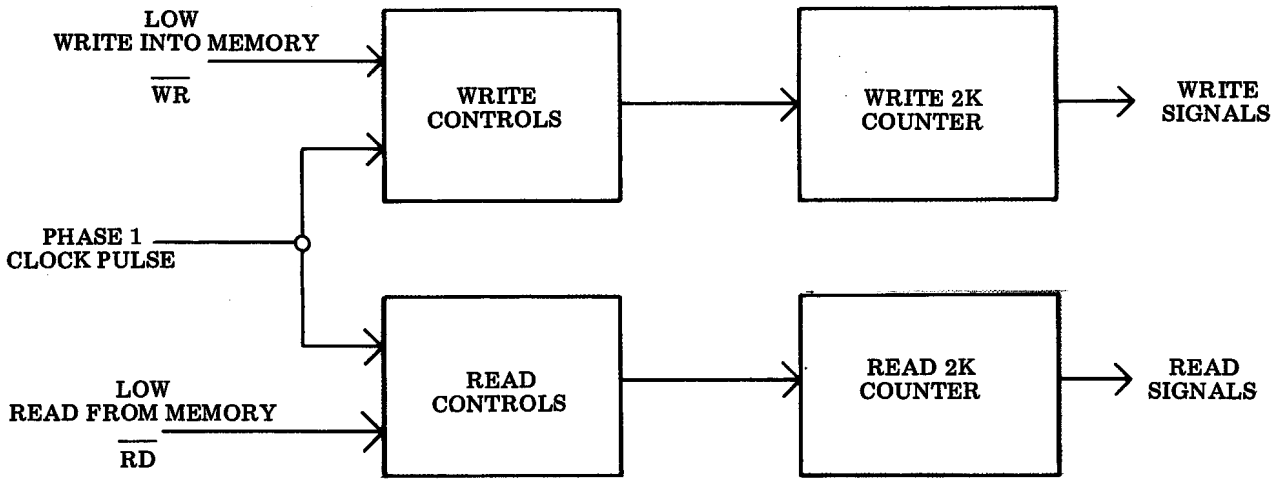


Figure 9 - 2K Counters and Read/Write Controls Flow Chart

4.38 The termination of the read operation occurs when either the output character buffer circuit card becomes full and pin 16 (shift in) goes low, or the MOS memory becomes empty and the read gate goes low.

4.39 When the MOS memory is empty, the write and read modulo 6 counters are once again in synchronism and the input signal MCS (modulo 6 counters synchronized) at card terminal 6 is high (conditioned gate) and allowing the phase 1 clock pulse to the read counter.

MODULO 6 COUNTERS AND DECODERS

4.40 The modulo 6 counters and decoders circuit card (MC998) controls the 2K counter if more than 2000 characters of storage are being used. In arrangements having 4000 characters, the MC998 will inhibit the read and write commands from the 2K counters on alternate counts; that is, a command will now only be given after 4000 counts to keep data recorded into adjacent locations.

4.41 This circuit card can be programmed from 2K to 6K storage capacity by means of optional screw placement on the circuit card. For information on how to program for the storage capacity, refer to Section 578-120-201 concerning installation, checkout, and troubleshooting.

4.42 The modulo 6 counters select the proper multiplex switches to be used for the write and read operation (Figure 10). Since the multiplex switches are separated by 4000 characters of MOS memory and the modulo 6 counters are pulsed once for each count of 2000 characters, the modulo 6 counters recognize two successive counts to address one of the multiplex switches circuit cards.

4.43 Selection of the proper multiplex switches during the write operation is determined by the WRA, WRB, and WRC signals. Each one of the three signals has two inputs connected to the Module 6 write counter. A high signal on WCL lead (write control), in addition to the above, detects and indicates when a full buffer condition exists.

MESSAGE CONTROL SIGNALS

4.44 After the PRS has occurred, the output interface is checked to determine the condition of the receiver associated with the buffer. With either interface (serial or parallel) the selectable signal is always applied via a strap to ground and the message signal is checked by the TP322514 buffer error control circuit card (MC514). Coincident with this, the MC514 presents a selectable RS signal to the input interface (MC969), which indicates to the interface that the buffer is capable of receiving data. At anytime when the module has traffic for the buffer it will indicate this by turning the message RM signal on. This signal will pass through the MC514 circuit card and on to the MC515 circuit card. The MC515 will turn the ready RR lead on and send this back to the interface module, via the MC969,

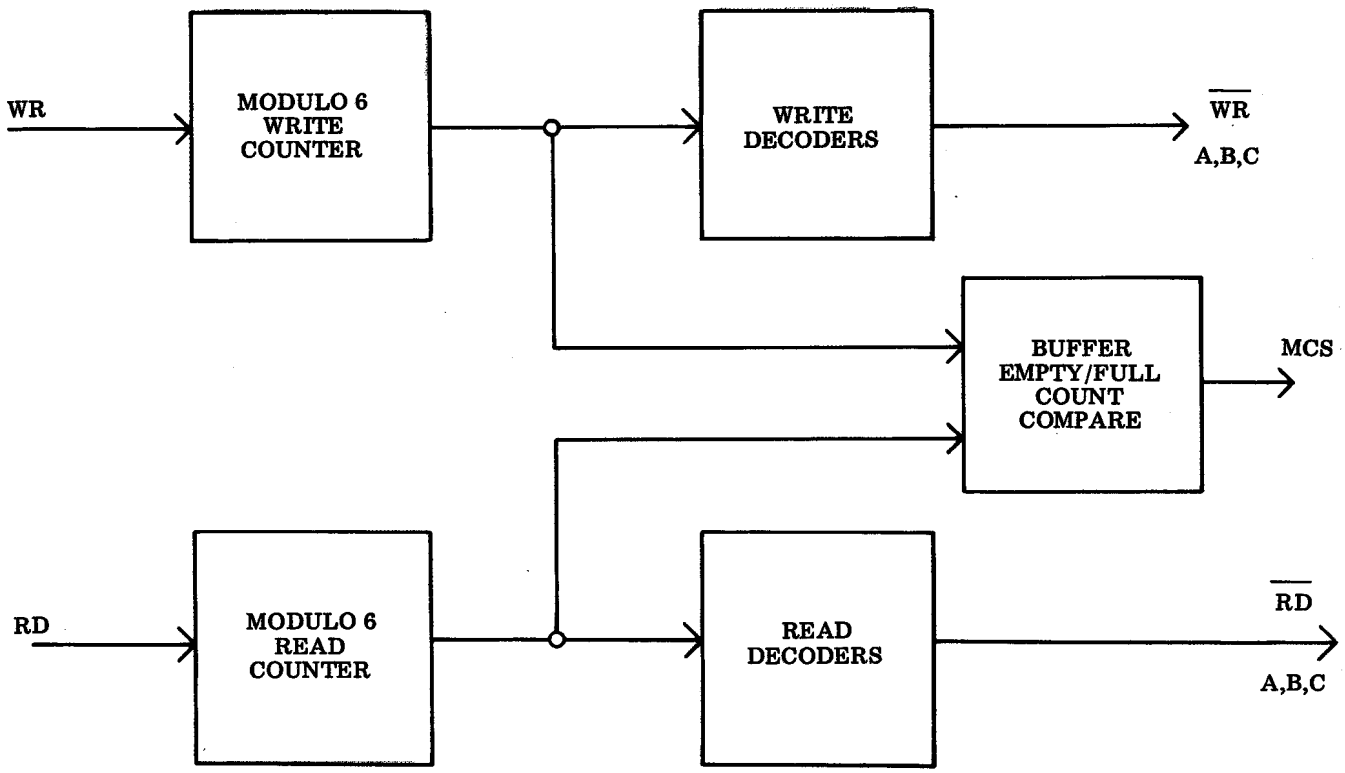


Figure 10 - Modulo 6 Counters and Decoders Flow Chart

as a confirmation of the receipt of message. At this time the initial message interfacing is complete and data transfer under character control may begin.

CHARACTER CONTROL AND DATA TRANSFER FROM MEMORY

4.45 Character control and data transfer into memory is accomplished upon the completion of the message control signaling. Upon completion of the control signals, the data transfer into the buffer is performed by the following steps. Refer to Figure 11, a partial block diagram of the control signaling.

(1) Control is started by a not character request signal ($\overline{RNC}$) from the input character buffer.

(2) Station controller recognizes the $\overline{RNC}$ signal.

(3) Character is presented on the data line.

(4) The presence of a valid character by turning the not receive character available ($\overline{RCA}$) signal on.

(5) The data and the $\overline{RCA}$ signal passes through the PTI circuit (MC969) and the in/out control circuit (MC515) to the input character buffer which turns off the $\overline{RNC}$ signal.

4.46 The above procedure notifies the station controller that a message has been accepted. The response is acknowledged by the $\overline{RCA}$ lead being turned off. Once this off condition is recognized by the two character buffer, the cycle is repeated by having the $\overline{RNC}$ lead turned back on, requesting the next character.

4.47 While the input portion of the two character buffer is conversing with the station controller, the output portion is under control of the 2K counters and read/write controls.

4.48 Data from MOS memory is removed via the multiplex switch (MC996) and loaded into the output character buffer (MC645) card. The transfer again is under the control of the in/out controls, and the modulo 6 counters and decoders circuit cards.

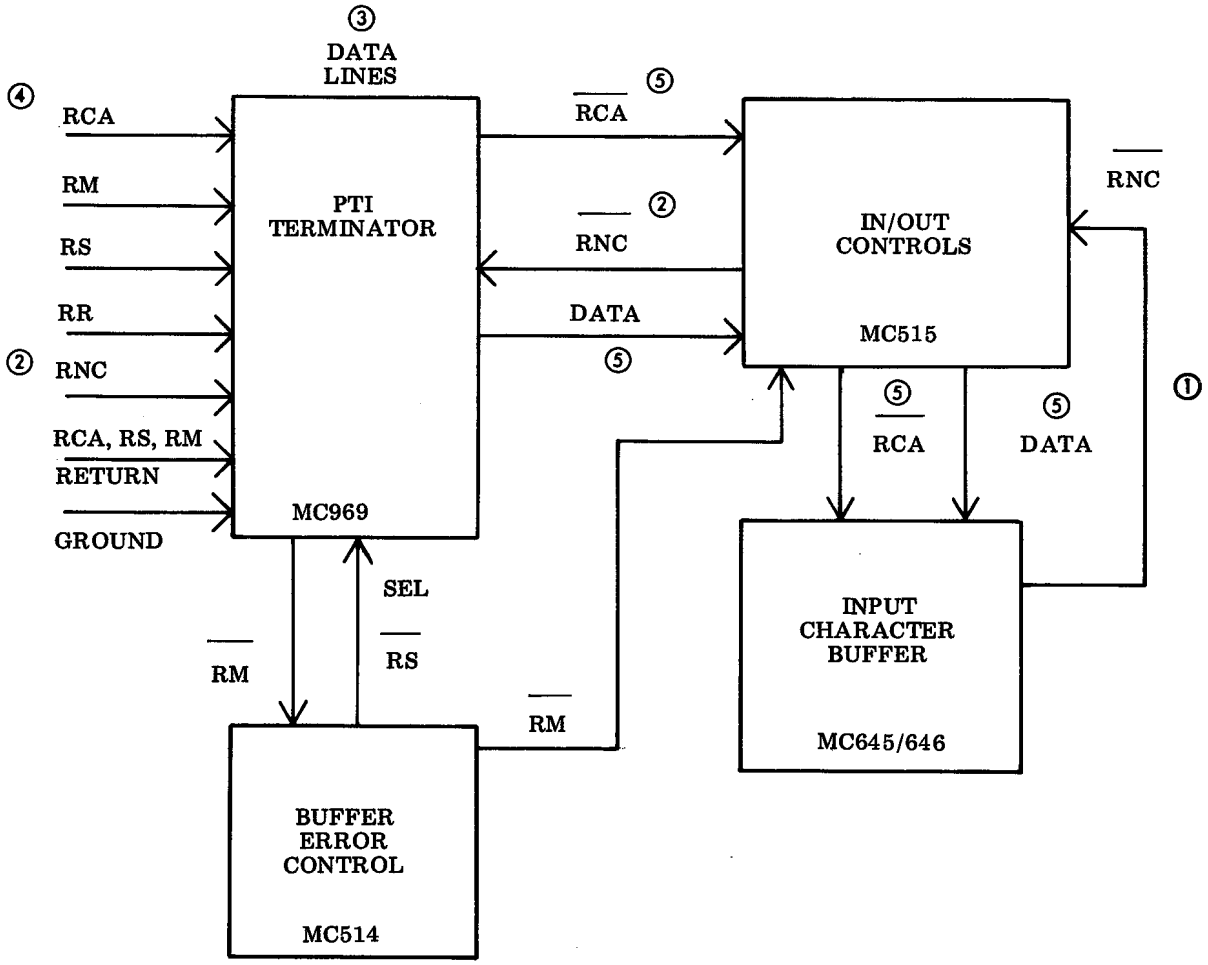


Figure 11 - Character Control and Data Transfer Flow Diagram

5. LOCAL RECEIVING DEVICE

5.01 The CDBU804 is used with serial output interfacing provided by the EIA driver circuit to a hard copy printer at low speed (refer to Transmitting Distributor 4.25 through 4.28.

5.02 The CDBU804 buffer can receive and transmit only one message at a time for storage and transmission to the local hard copy printer.

5.03 Data is sent from the output character buffer to the transmitting distributor. The data is serialized and transferred to the EIA driver circuit by the distributor circuit. The EIA driver circuit converts the data signals to EIA compatible signals and transmits these signals to the hard copy printer. The transmission speed is determined by the frequency of the clock signal in module location XZC308 which controls the speed of the transmitting distributor (MC091). Message control signals (EIA) are also used in the serial interface driver and receiving device.

5.04 Once the message has been completely transmitted to the local receiving device, the buffer again becomes selectable and signals the station controller that it can accept incoming messages. The character buffer is under control of the station device at all times.

5.05 The buffer module may be manually conditioned for local operation and accept message data from the terminal for transmission to the hard copy receive device. The display terminal attendant conditions the buffer by depressing the LOCAL or HARD COPY key on the console then by depressing the TRANSMIT key. All text displayed on the monitor will be transmitted to the hard copy device.