PARITY FAILURE DETECTOR (SA110)

DESCRIPTION AND PRINCIPLES OF OPERATION

CONTENTS PAGE

1. GENERAL

1.01 This section provides the description and principles of operation for the SA110 parity failure detector (Figure 1) and the bypass switch and indicator assemblies available for use with it (Figure 2). The variable features present for the coded versions of the SA110 are shown on Table A. Refer to Section 578-200-200 for installation information, Section 578-200-300 for checkout and troubleshooting procedures, and Section 578-200-800 for parts.

1.02 The parity detector (SA110) is an accessory to a receiving data terminal. It regenerates an incoming signal bit by bit and monitors it for transmission errors. Upon detecting an error, the parity detector supplies either (a) an output to stop the sending terminal or notify its operator or (b) an output to notify the operator of the receiving terminal.

1.03 The parity detector can be used with any eight-level, serial-by-bit signal that provides a parity bit, at any speed up to 2400 baud (2400 words per minute). It may be used with either even or odd parity systems and with signals employing either 10-unit or 11-unit character structure. The SA110 can be applied to 33 and 35 type automatic send-receive or receive-only terminals and Type 2 DATASPEED terminals. No prearrangement with a sender is necessary other than assurance of parity transmission.

1.04 Error detection is accomplished ahead of the receiving terminal by checking each incoming character for parity. Eight-level codes provide a parity bit in addition to the seven information bits so that the total number of marking bits in each character is always even, for even parity, or odd, for odd parity. Characters received with incorrect parity are detected as errors.

1.05 A supplemental error check based on detection of displaced signal transitions (significant distortion) is available as a strap option. The combination of this check and the parity check increases the error detection capability of the SA110 but also increases the number of false error indications received.

(a) The SA110 cannot detect every transmission error when strapped for parity checking alone because all characters with two, four, six, or eight bits in error will have correct parity; these characters will not be recognized as errors. The SA110 will detect approximately 75 to 80 percent of all transmission errors when strapped for parity checking alone. Because all characters with incorrect parity are detected as errors, a false error indication will occur whenever the

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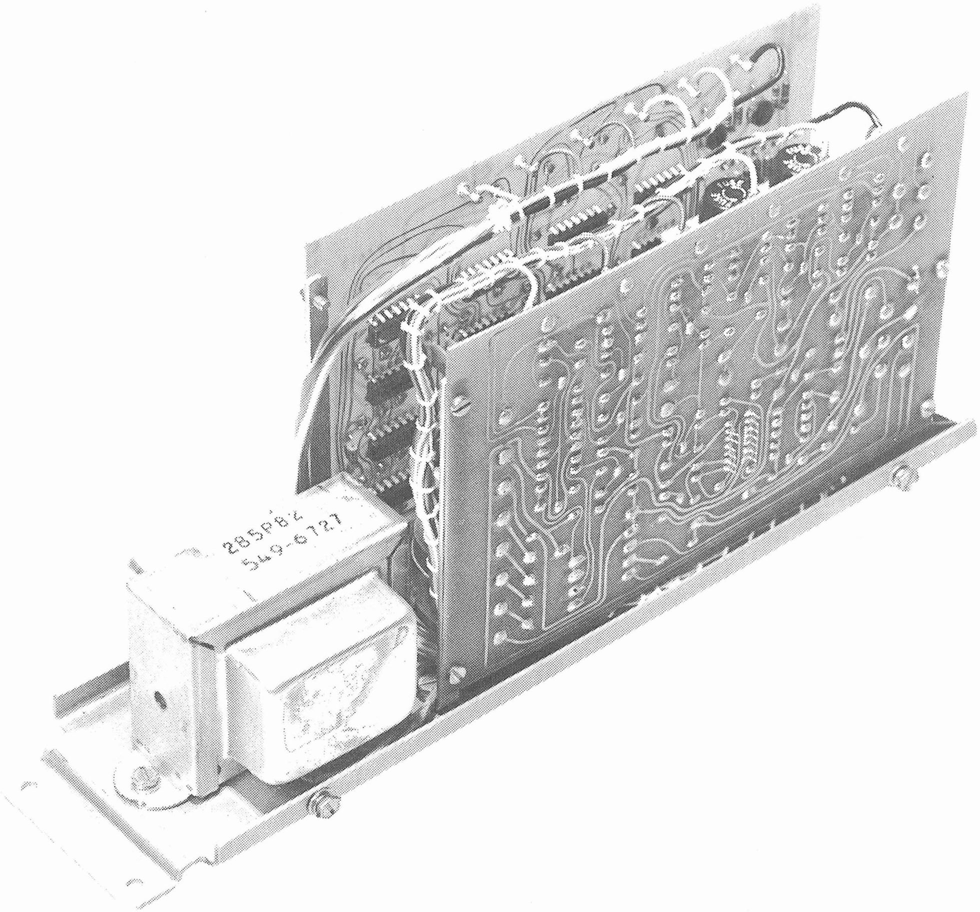


Figure 1 - SA110 Parity Failure Detector (Cover Removed)

parity bit is the only bit in error. With parity checking alone, 10 percent of all error indications can be expected to be false.

(b) The significant distortion check detects characters with one or more bits having 50 percent or greater distortion (a bit half as long as it should be or shorter). Some erroneous characters with correct parity will be detected by this check, but its effectiveness depends on the noise characteristics of the transmission channel used. In one case, 90 percent of all transmission errors were detected by the SA110 when this check was combined with parity checking. However, the number of false error indications increased considerably; in the same case, 30 to 35 percent of the error alarms were false. The increase in unnecessary retransmissions resulting from false error alarms is the price of more effective error detection using combined parity checking and significant distortion checking.

(c) Error rates, error detection percentages, and false error indication percentages are a function of the noise characteristics of a channel during the time of transmission. These characteristics can vary significantly from channel to channel, and from time to time on the same channel.

1.06 Errors may be indicated in the following ways:

(1) By generating a "break" signal (spacing line) on a half-duplex circuit (33 and 35 type receivers) or a break on the reverse channel lead (Type 2 DATASPEED receivers).

(2) By lighting an indicator lamp which flashes on each error or error burst.

(3) By lighting an indicator lamp which lights on the first error and blinks off briefly on following errors until reset.

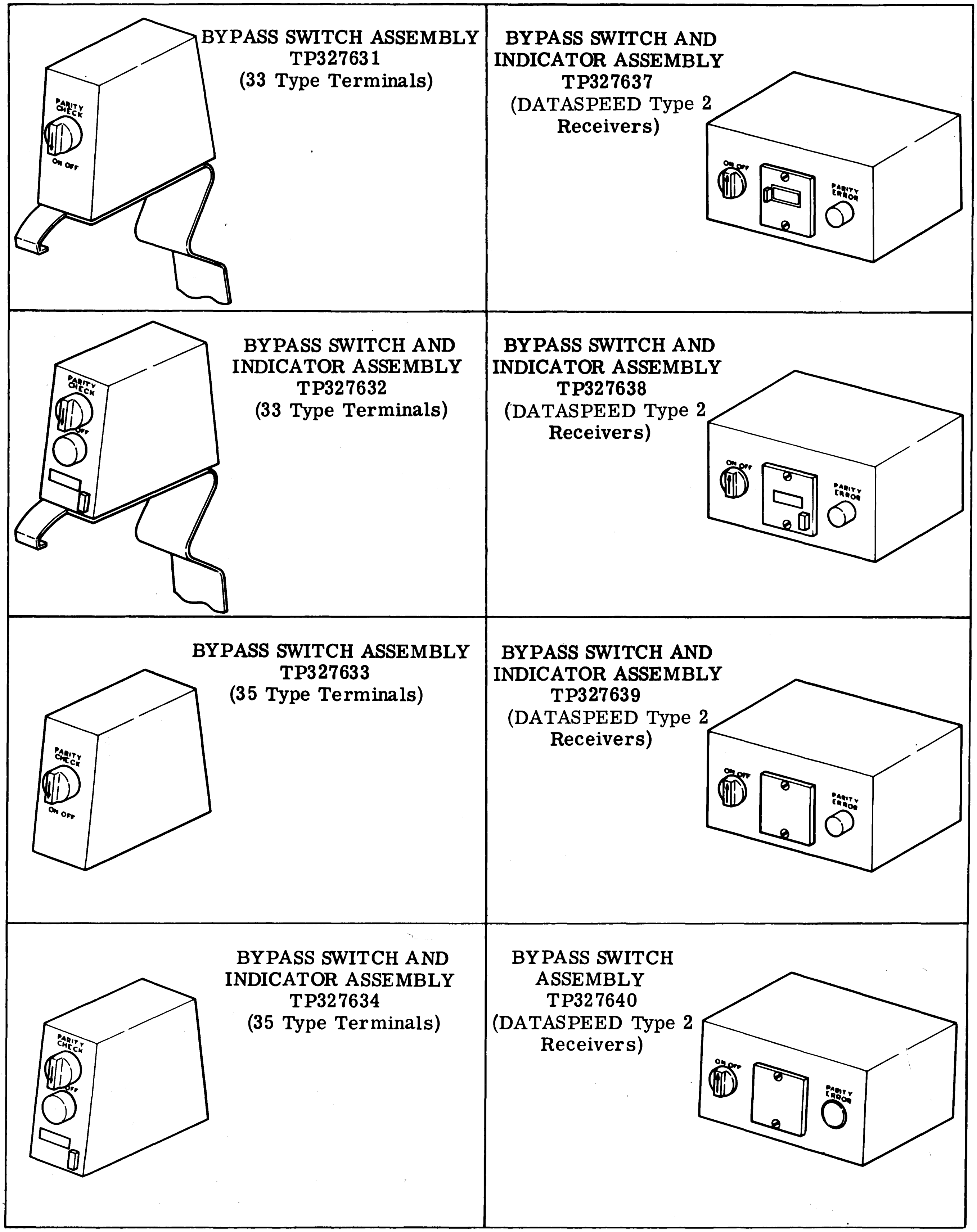


Figure 2 - Bypass Switch and Indicator Assemblies

TABLE A

SA110 PARITY DETECTOR VERSIONS

A. For Use on 33 Type Receiving Terminals

CODE	SPEED	BYPASS SWITCH AND INDICATOR ASSEMBLY AND FUNCTION
SA110 AB	110 Baud	No Assembly — Generates Line Break (HDX Line)
SA110 BA	110 Baud	TP327631 Bypass Switch — Generates Line Break (HDX Line)
SA110 BB	110 Baud	TP327632 Switch, Lamp, and Counter — Lights and Counts Errors

B. For Use on 35 Type Receiving Terminals

CODE	SPEED	BYPASS SWITCH AND INDICATOR ASSEMBLY AND FUNCTION
SA110 AB	110 Baud	No Assembly — Generates Line Break (HDX Line)
SA110 CA	110 Baud	TP327633 Bypass Switch — Generates Line Break (HDX Line)
SA110 CB	110 Baud	TP327634 Switch, Lamp, and Counter — Lights and Counts Errors

C. For Use on DATASPEED Type 2 Receiving Terminals

CODE	SPEED	BYPASS SWITCH AND INDICATOR ASSEMBLY AND FUNCTION
SA110 AD	1050 Baud	No Assembly — Generates Break on Reverse Channel
SA110 EA	1050 Baud	TP327640 Bypass Switch — Generates Break on Reverse Channel
SA110 EB	1050 Baud	TP327638 Switch, Lamp, and Counter — Lights and Counts Error Bursts
SA110 EC	1050 Baud	TP327639 Switch and Lamp — Lights on First Error Until Reset
SA110 ED	1050 Baud	TP327637 Switch, Lamp, and Counter — Lights and Counts Consecutive Errors

D. For Use on Other Equipment

CODE	SPEED	BYPASS SWITCH AND INDICATOR ASSEMBLY AND FUNCTION
SA110 AC	150 Baud	No Assembly — Generates Line Break (HDX Line)

<u>Note</u>: The TP327638 bypass switch and indicator assembly has a low speed counter identical to those in the TP327632 and TP327634 assemblies; the TP327637 assembly has a high speed counter capable of recording consecutive errors at 1050 baud.

(4) By lighting an indicator lamp which latches on with the first error until manually reset.

(5) By advancing an error counter.

Indication (2) or (3) may be combined with (5). The last four indications are available with the bypass switch and indicator assemblies described in Part 4, VARIABLE FEATURES.

1.07 Because the SA110 samples the incoming signal by shifting it through a single-bit register, it regenerates each character while checking its parity. Information bits containing up to 45 to 49 percent distortion are regenerated to a maximum of 5 percent distortion. Information bits containing 50 percent distortion or more will also be regenerated, but their mark or space state will probably be changed by the accessory.

1.08 The duration of the stop pulse of each regenerated character is such that the overall duration of each outgoing character is identical to its duration as received, provided the stop pulse of a 10-unit code input signal is 0.8 bit or longer or the stop pulse of an 11-unit code signal is 1.6 bits or longer. An overriding marking pulse provides a stop pulse of 0.8 bit for 10-unit code and 1.6 bits for 11-unit code whenever the incoming stop pulse is shorter than the minimum. (Characters having a stop pulse 0.5 bit long or less may be detected as errors if the significant distortion check is used, however.)

1.09 To prevent false starts during an idle line condition, all spacing signals of less than 0.5 bit duration are rejected as noise until a valid start pulse appears. A line break (continuously spacing line) may cause the accessory bit timer to run open and the output to lock in the marking state. For even parity, either a single garbled character will be passed to the terminal when a break occurs, or the accessory will present continuous NULL characters to the terminal; for odd parity, a single garbled character or NULL character will be presented before the accessory goes to the mark hold state. In either case, the presence of the accessory prevents any break detection circuitry in the terminal from detecting the line break.

PHYSICAL CHARACTERISTICS

1.10 The parity detector (SA110) is approximately 12 inches long, 2-1/2 inches wide, and 5 inches deep. It may be placed inside the pedestal of a 33 or 35 type cabinet or on an empty shelf in a Type 2 DATASPEED cabinet. It may also be mounted outside the cabinet, if preferred. Since it has no controls or indicators on the chassis it need not be accessible to the operator.

1.11 The parity detector may be operated over an ambient temperature range of 40 degrees F to 110 degrees F with relative humidity of up to 90 percent.

ELECTRICAL CHARACTERISTICS

A. Input

1.12 The SA110 parity detector accepts a serial signal consisting of a start bit, eight information bits, and a stop pulse of unity length or longer. It is available for receiving 110, 150, or 1050 baud signals and may be ordered for other baud rates up to 2400. The SA110 is factory wired for monitoring even parity, but it may be restrapped for odd parity.

1.13 The parity detector is connected in series with the receive data lead in the terminal. Its electrical interface is compatible with data sets meeting EIA Standard RS-232B, such as the 103E. The receive data levels of these sets are as follows:

Space = +3 to +25 volts
Mark = -3 to -25 volts

The input impedance is 3300 ohms. By strap option, a 20 ma or 60 ma current/no-current line or equivalent data set, such as the 101C or 105A, may be used as an input. Loop battery at the SA110 is provided by -14 volts dc.

1.14 For its power requirements, the parity detector plugs into any outlet supplying 115 v ac ±10% at 60 Hz ±2%. The maximum current required from this source is 3/8 ampere.

B. Output

1.15 The output is a serial signal consisting of a start bit, eight information bits, and one or two stop bits. The information bits are regenerated by the parity detector and contain less than 5 percent distortion.

1.16 Two forms of data output are available, EIA and dc current loop. The EIA output meets the requirements of Standard RS-232B (+5 volts minimum when terminated in 3000 ohms). These voltages are as follows:

Space = +6 volts ±1 volt
Mark = -8 volts ±2 volts

Source impedances are 4500 ohms and 1800 ohms respectively.

1.17 The dc current loop output is a switched transistor stage capable of providing a current/no-current signal. The maximum voltage which may be applied is -48 volts dc. Maximum current switched (limited externally) is 60 ma.

1.18 Two outputs are available to drive error display devices. One is a polar signal conforming to EIA Standard RS-232B. This output is normally negative (-14 volts) and goes positive (+14 volts) when a parity error is detected. The second output is a set of Form C (transfer) relay contacts. Provision has been made to connect the common terminal of the contacts to +14 or -14 volts, either directly or through a current-limiting resistor. Power applied to these contacts should be limited to 48 volts and 200 ma.

2. GENERAL DESCRIPTION

2.01 The parity detector contains two circuit cards and a power supply. It is completely self-contained except for an optional bypass switch or indicator assembly. These operational assemblies are described in Part 4, VARIABLE FEATURES.

2.02 Both SA110 circuit cards use integrated circuits as well as discrete components. They consist of a regenerator and parity detect logic card (TP322402-404) and an interface amplifier and break generator circuitry card (TP322405). Card TP322402 is used in parity detectors operating at 110 baud, card TP322403 in those operating at 150 baud, and card TP322404 in those operating at 1050 baud. The only difference between these cards is in the bit timer crystal and two associated capacitors.

2.03 The regenerator and parity detect logic card has strap options for 10- or 11-unit code operation, even or odd parity check, and enabling or disabling the significant distortion check. The interface amplifiers and break generator circuitry card has strap options for operation with 60 ma dc input, with 20 ma dc input or 101C or 105A data sets, or with EIA input; operation with 20 ma or 60 ma output (current must be limited externally) or with EIA or simulated 101C and 105A data set output; various operate time and inhibit combinations for the output pulse; energizing a relay during the output pulse or replacing it with a resistive load; relay operation on every error detected, relay latch on first error and drop-out and pick-up on following errors, or permanent relay latch on first error; and +14 volts or -14 volts output at relay contacts.

3. PRINCIPLES OF OPERATION

3.01 Schematic wiring diagram 8538WD (furnished with the SA110) is useful for understanding the following discussion. Actual wiring information is contained on 8539WD (actual wiring diagram for the SA110), 322402-404 (regenerators and parity detect logic card drawing), and 322405 (interface amplifiers and break generator circuitry card drawing).

3.02 A simplified block diagram of the SA110 parity detector logic is shown in Figure 3. The explanation of error detection operation which follows is based on this diagram. A complete circuit description is included in 8538WD. Refer to sheet CD10 for a logic flow chart for the SA110.

3.03 Input data from the signal line or channel is amplified by the input amplifier Q12-Q13, MC405, and converted to levels compatible with the parity detection logic (+6 volts for mark, 0 volt for space). This amplifier accepts a 60 ma current/no-current signal with straps K and L closed, a 20 ma current/no-current signal or the output of 101C and 105A data sets with strap K open and L closed (factory wiring), and an EIA signal with strap K open and L open. The dc inputs must be applied between terminals 1 and 2 or 1 and 4, and the EIA input must be applied between terminals 3 and 2 or 3 and 4. The output of this amplifier is applied to the input gating and the clock pulse input of the mark-space flip-flop (MSFF), both on MC402-404.

3.04 The input gating consists of inverter MLC3-10 and NAND gates MLD4-3 and MLD3-6. The output of MLC3-10 is used to prime the data flip-flop (DFF) and to provide the clock pulse for the space-mark flip-flop (SMFF). A second prime for the DFF is obtained from MLD4-3. The output of MLD3-6 is used to release and inhibit the bit timer counter flip-flops so that no clock pulse is developed if the spacing start pulse is less than 0.5 bit in duration.

3.05 The bit timer consists of a free-running crystal oscillator and seven binary flip-flops. The oscillator operates at 128 times the incoming bit rate and the seven flip-flops form a counter which divides its frequency down to the bit rate. Inhibiting these flip-flops controls the bit timer. The outputs of four of the flip-flops are used to regenerate the stop pulse, and the output of the final flip-flop is used to develop the clock pulse.

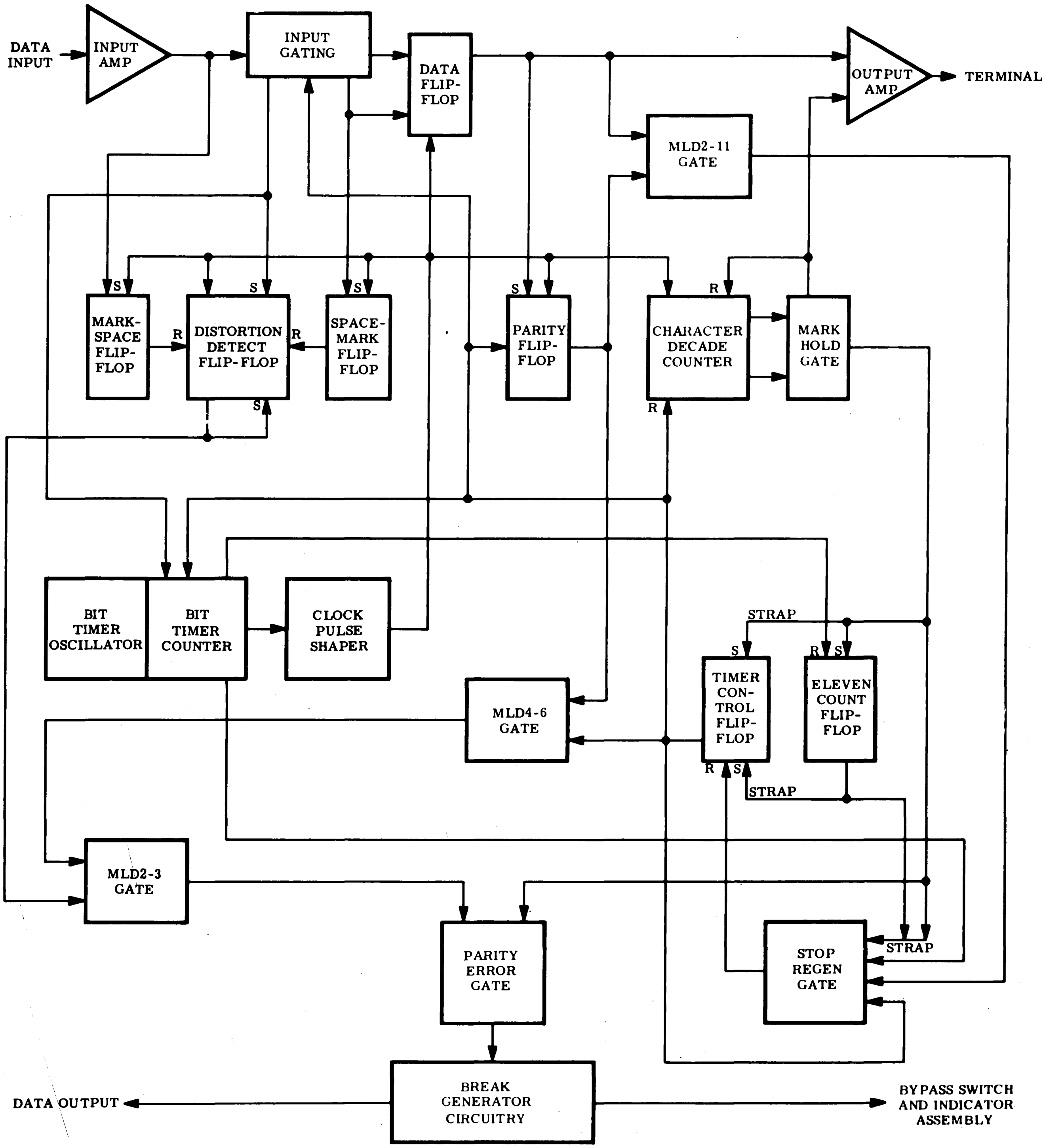


Figure 3 - Simplified Block Diagram of SA110 Parity Detector

3.06 Positive-going transitions at the output of the final binary flip-flop (MLC1-5) are transformed by the clock pulse shaper, NAND gates MLC4-3 and MLC4-11 and capacitor C7, to produce negative-going clock pulses of nanosecond duration at the output of MLC4-11.

3.07 Incoming data bits from the input gating are stored in the DFF for a duration of one bit. In conjunction with the clock pulses, this flip-flop reduces signal distortion to less than 5 percent. Its output, a unipolar signal (+6 volts space, 0 volt mark), is connected to the output amplifier, NAND gate MLD2-11, and the parity flip-flop (PFF).

3.08 The output amplifier, Q9-Q11, MC405, provides 20 ma or 60 ma current/no-current output signals with strap H closed and J open (this current must be limited externally), an output equivalent to that of a 101C or 105A data set with strap H open and J closed, and EIA signals with either or no strap open. The dc outputs are obtained across terminals 12 and 2 or 12 and 4, and the EIA output across terminals 10 and 2 or 10 and 4. The output of this amplifier is connected to the data input (SMD or equivalent) of the terminal.

3.09 The stop pulse of each character sent to the terminal by the output amplifier is regenerated by a circuit consisting of the character decade counter (CDC) and the mark hold (MH) gate. The CDC consists of J-K flip-flops MLA3 and MLB2, NAND gate MLB3-6, and inverter MLC3-6. It counts clock pulses. When ten clock pulses have been registered, the CDC signals the MH gate that a time equivalent to ten bits has elapsed.

3.10 The MH gate monitors the normal outputs of the second and fourth flip-flops in the CDC. These outputs both become high when the tenth clock pulse arrives, causing the output of the MH gate to go low. This output holds the output amplifier low, overriding the stop pulse, if necessary, to provide a minimum stop pulse of 0.8 bit for 10-unit code or 1.6 bits for 11-unit code. This maintains synchronism between sender and receiver. The output of the MH gate is also inverted by MLC3-2 and connected to the CDC (via a gate), the parity error (PE) gate, the eleven count flip-flop (ECFF), and — depending on the code strapping — to the timer control flip-flop (TCFF) and the stop regenerator (SR) gate. (The ECFF is used for eleven unit code only.)

3.11 The ECFF is set on the first count of the CDC (when the MH gate goes high) and is reset when the eleventh clock pulse occurs (the first bit timer output after the MH gate goes low). The output of this flip-flop is inverted by MLC3-4 and primes TCFF for reset. It is also strapped to an input of the SR gate.

3.12 The TCFF locks the bit timer on and unblocks the PFF for the duration of each character. It is set by the inverted output of the MH gate or the output of the ECFF, depending on the code strapping, when the first count of the CDC occurs. At the end of each character it is primed for reset by the MH gate or the ECFF, and is reset by the output of the SR gate. Its output is gated with the inverted output of the MH gate to reset the CDC at the end of each character.

3.13 The parity flip-flop, PFF, changes state for every spacing bit shifted into the DFF. The normal output of this flip-flop is used to detect even parity and the inverted output is used to detect odd parity. At the end of a character with correct parity, the strapped output is low; at the end of a character with incorrect parity, the strapped output is high. The output is connected to the MLD2-11 gate and NAND gate MLD4-6.

3.14 NAND gate MLD2-11 is used to detect loss of synchronization between the regenerator and the incoming signal. Its inputs are the inverted output of the DFF and the strapped output of the PFF, depending on whether even or odd parity is being checked. The output of this gate is connected to an input of the SR gate, so its state is important only after the last (tenth or eleventh) clock pulse occurs. If a mark is shifted into the DFF as the stop pulse at this time, input MLD2-12 is low. If the strapped parity is correct, input MLD2-13 is also low. With either or both of these conditions present, the output is high, allowing the logic to be reset. Only if both inputs are high (no stop pulse or short stop pulse and incorrect parity) does the output go low, indicating apparent loss of synchronization between the regenerator and the incoming signal.

3.15 The SR gate is used to reset the timer control flip-flop and, through it, the bit timer counter flip-flops at the end of a character, stopping the regenerator logic. It has four inputs. One input is from the MH gate or the ECFF, indicating that the last clock pulse (tenth or eleventh) has occurred. Another input is from the bit timer, indicating that the cycle is at 0.3 bit after the tenth clock pulse (10-unit code) or 0.1 bit after the eleventh clock pulse (11-unit code), depending on the code strapping. A third input is from NAND gate MLD2-11, indicating apparent synchronization between the regenerator and the incoming signal. The last input is from the TCFF to inhibit the output from changing states at the start of a character. Normally, when the first, second, and fourth inputs are high, the regenerator will be in synchronization and so the third input will be high also. This makes the output low, resetting the TCFF. If the third input is low at this time, the TCFF will not be reset and the bit timer counter will continue to run until a marking bit is shifted into the DFF. Any spacing bits appearing at this time will not be passed on to the terminal, since the output amplifier remains locked in the mark hold state. When the marking bit arrives, the TCFF and the bit timer counter are reset. The next spacing pulse to appear on the input data lead is recognized as the start of the next character. Any additional marking bits appearing between the marking bit which resets the TCFF and the next spacing bit will not be passed on to the terminal either. Therefore, the SA110 restores synchronization by rejecting first spacing and then marking bits until it detects a character that has either a valid stop pulse or correct parity. Synchronization will be restored by this process after from two to fifteen characters have elapsed. While this is taking place, the terminal will copy garbled characters at a speed less than the incoming character rate.

Note: A continuously spacing line (line break) causes slightly different operation, depending on whether the SA110 is strapped for even or odd parity and whether the break occurs in the middle of a character or after the end of a character. For even parity, a single garbled character will be passed to the terminal if the break causes the last character to have incorrect parity. (This character will also be missing a stop pulse because of the break, so the logic will lock in the mark hold state.) Continuous NULL characters will be passed to the terminal if the break occurs between characters or if the last character retains correct parity. (This is because the NULL character — all information bits spacing — has correct even parity. NULL characters are created by the MH gate adding the minimum stop pulse to the spacing line at the correct point for each character.) For odd parity, only one garbled character or NULL character will be presented to the terminal before the logic goes to the mark hold state. (NULL has incorrect odd parity.) In any case, the terminal is unable to detect the continuously spacing line when the SA110 is present, and so any break detection circuitry or indicator that it may have is disabled. The operator should be able to recognize that a break has occurred from the interrupted message or continuous NULL characters (for even parity), however.

3.16 As a strap option, the SA110 can check the incoming characters for significantly distorted information bits in addition to checking parity, in order to detect transmission errors which leave the characters with correct parity. This circuitry consists of the mark-space flip-flop (MSFF), the space-mark flip-flop (SMFF), and the distortion detect flip-flop (DDFF). When used, the DDFF output is strapped to the input of NAND gate MLD2-3 to control the output of the PE gate. Incoming data bits from the input amplifier are coupled to the clock pulse input of the MSFF via an RC network and, after inversion by MLC3-10, are coupled to the clock pulse input of the SMFF via a similar network. Both flip-flops are set on every clock pulse. When a bit having a mark-to-space transition is received, the MSFF is reset, and when a bit having a space-to-mark transition is received, the SMFF is reset. If another mark-to-space or space-to-mark transition is received before the next clock pulse, the affected flip-flop will toggle back to the set state again. The inverted outputs of these flip-flops are the inputs of NAND gate MLA4-11, whose output is inverted by MLA4-8 and connected to the reset prime of the DDFF.

3.17 The timing for significant distortion error detection is shown in Figure 4. A noise pulse occurring while the signal line input is idle causes the MSFF and SMFF to be reset. Both outputs are high at time T1, but since no clock pulse is developed the DDFF is not reset. Additional noise pulses cause the two flip-flops to toggle back and forth. If the last noise pulse (time T2) leaves them both reset, the mark-to-space transition occurring when the true start bit arrives sets the MSFF, so the DDFF is no longer primed when the first clock pulse is developed. Consequently, the SA110 will not indicate an error for idle line noise.

3.18 When undistorted or slightly distorted data bits appear at the input, the MSFF is reset on each mark-to-space transition (time T3) and set on the following clock pulse, and the

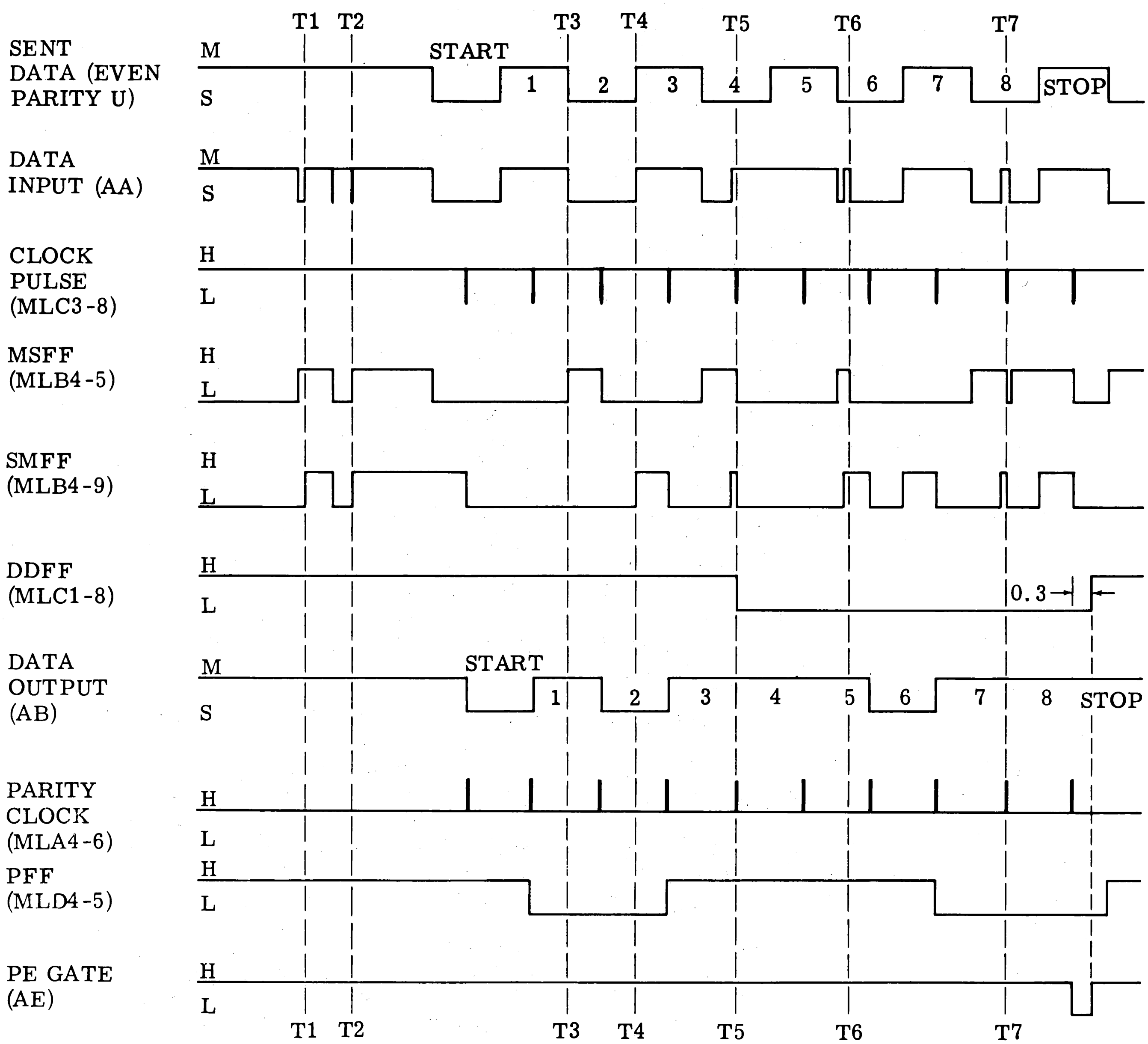


Figure 4 - SA110 Significant Distortion Error Detection (10-Unit Code)

SMFF likewise (time T4). If a bit is received so distorted that its length is 50 percent or less of its correct length (bit 4, for example), the MSFF is reset as usual but before it is set again the SMFF is also reset. When the clock pulse for this bit arrives (at time T5), it simultaneously sets the MSFF and SMFF and resets the DDFF, causing its output to switch from high to low. Once reset, the DDFF output remains low to indicate an error regardless of the condition of the remainder of the character; however, additional transmission errors are shown on Figure 4 to illustrate other aspects of operation.

Note: If the short spacing bit at time T5 which causes the significant distortion circuit to indicate an error was a brief spike, though long enough to pass through the networks at the inputs of the MSFF and SMFF, it would still be detected as an error. Consequently, signal sources which have brief spacing spikes between consecutive marking bits (such as the direct output of a 33 type sender) will have distortion errors indicated for valid characters. Normally, the modulation and demodulation of line transmission attenuates the 33 output spikes enough to prevent such false indications, but if not, it may be necessary to strap out the significant distortion check at terminals which receive from such senders.

3.19 If noise pulses occur and disappear before (or after) the clock pulse arrives, as shown for bit 6, the MSFF and SMFF will toggle from set to reset and back again. Prior to time T6 both flip-flops are reset, but since no clock pulse occurs at this time the MSFF is set again on the mark-to-space transition at the end of the noise pulse and the DDFF, though primed, is not reset. Consequently, no error indication is made, but since the data bit is in the correct state when the clock pulse arrives, no error occurs and the noise is eliminated from the regenerated bit at the data output. If a noise pulse occurs at the same time as the clock pulse however (time T7), both flip-flops will be high when the clock pulse arrives, causing the DDFF to indicate an error. In this case the regenerator will change the sense of the bit.

3.20 If two bits are changed in state (mark-to-space or space-to-mark) the parity of the regenerated character will be correct, so the PFF will not detect the error (Figure 4). The altered bits will nevertheless be detected by the MSFF and SMFF — unless both bits are completely reversed (that is, with no undistorted or noise-free portion of the original bit remaining) — causing the DDFF to be reset and indicate an error. The output of the DDFF remains low after it is reset until 0.3 bit after the tenth clock pulse (10-unit code) or 0.1 bit after the eleventh clock pulse (11-unit code). The DDFF is then set when the TCFF is reset by the SR gate. The outputs of the DDFF and NAND gate MLD4-6 are the inputs of NAND gate MLD2-3, whose output is connected to the parity error (PE) gate. When the MH gate changes state on the tenth clock pulse the PE gate is unblocked, permitting it to indicate an error if either input of gate MLD2-3 is low. As a result, the distortion detection circuit can cause an error to be indicated as late as the midpoint of the stop pulse. This means that a character received with a stop pulse shorter than 0.5 bit (10- or 11-unit code, but a stop pulse this short would be distorted 75 percent or more for 11-unit code) will be detected as an error even though the stop pulse will be regenerated to a minimum length of 0.8 bit and the character may be correct otherwise.

3.21 The error detection and timing signals are combined to a single output by NAND gates MLD4-6, MLD2-3, and the PE gate. The inputs of gate MLD4-6 are the outputs of the PFF and the TCFF. These signals will both be high when an incoming character with incorrect parity is received from the time the last spacing bit is monitored until the TCFF is reset 0.3 bit after the tenth clock pulse (10-unit code) or 0.1 bit after the eleventh clock pulse (11-unit code). When both inputs are high, the output, which is connected to an input of MLD2-3, is low.

3.22 NAND gate MLD2-3 acts as an OR gate by monitoring the low (error) outputs of gate MLD4-6 and the DDFF. For characters with correct parity and low distortion, both signals are high and the output is low. But with either or both error indications present, the output will be high. This signal is connected to an input of the PE gate. The other input of this gate is the inverted output of the MH gate, which becomes high when the tenth clock pulse arrives for each character. The output of the PE gate, then, will become low when an error is detected from the time the tenth clock pulse appears until 0.3 bit later (10-unit code) or 1.1 bit later (11-unit code). This output is connected to the break generator circuitry on MC405.

3.23 The break generator circuitry consists of an input amplifier, two one-shot multivibrators, a relay driver and relay, an output amplifier, and a latching circuit. An error indication triggers the one-shot multivibrators, causing a positive-going pulse (-14 volts to +14 volts) to appear at the output and energize the relay for the duration of the multivibrator timeout period. This is accomplished as follows.

3.24 Input amplifier Q1 is normally on (collector at 0 volt). When an error is detected, the negative-going pulse (+6 volts to 0 volt) at the output of the PE gate causes Q1 to become nonconductive.

3.25 Stages Q2 and Q3 form a one-shot multivibrator whose timeout period is controlled by R8, C1, and C2. Transistor Q2 is normally held off and Q3 is normally on. When Q1 is cut off by the PE gate output, Q2 is brought into conduction and a negative-going transition is produced at the collector. This transition is capacitively coupled to the base of Q3 by C1 and C2 or C2 alone. Stage Q3 is turned off and the multivibrator begins its timeout. The capacitors or capacitor charge until the base of Q3 becomes positive enough to allow it to conduct again. With both capacitors in the circuit (factory wiring), the timeout period of one-shot Q2-Q3 is approximately 500 milliseconds. Removing strap A so that only C2 is in the circuit reduces the timeout period to approximately 1 ms. An intermediate timeout period can be obtained by removing strap A and connecting a capacitor with a value between those of C1 and C2 across terminals 27 and 28.

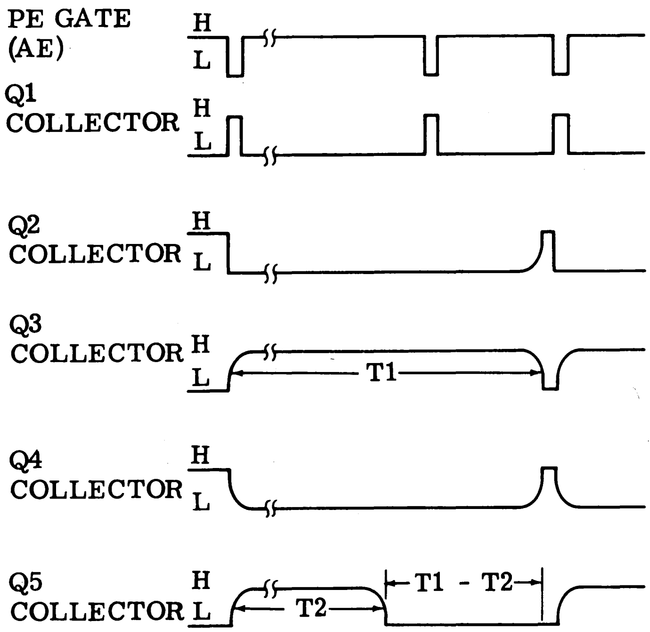
3.26 Stages Q4 and Q5 also form a one-shot multivibrator. Controlled by R14, C3, and C4, its operation is the same as for one-shot Q2-Q3. Stage Q4 reacts the same as Q2, and Q5 the same as Q3; all four stages switch at the same time initially. With both capacitors in the circuit (factory wiring), the timeout period of one-shot Q4-Q5 is approximately 250 ms. Removing strap B so that only C4 is in the circuit reduces the timeout period to approximately 3.5 ms. An intermediate timeout period can be obtained by removing strap B and connecting a capacitor with a value between those of C3 and C4 across terminals 29 and 30. For example, with a 5 microfarad (MFD) capacitor the timeout will be approximately 65 ms, and with the 2 MFD capacitor (furnished with versions of the SA110 having an indicator assembly) the timeout will be approximately 31 ms.

3.27 The timeout period of one-shot Q4-Q5, T2, controls the duration of the output pulse and the time that the relay is energized. If the timeout period of one-shot Q2-Q3, T1, is longer than T2, further triggering of one-shot Q4-Q5 will be inhibited for a time equal to the difference of the two periods. This timing is shown in Figure 5, Case A. Since T1 is longer than T2, the minimum interval in which repetitive errors will be indicated is T1 and errors will not be indicated during the inhibit period of T1 minus T2. If T1 is shorter than T2, as shown in Figure 5, Case B, there is no inhibit period and the minimum interval in which repetitive errors will be indicated is T2. These relationships, and the strapping required to obtain them, are summarized in Table B.

3.28 Despite the wide variety of timing options available for special applications, most SA110 installations use either the factory wiring or have straps A and B removed, with or without an added capacitor. The factory wiring provides a 250 ms output pulse for generating a line break (110 or 150 baud) or pulse on reverse channel (1050 baud and higher speeds) with a 250 ms inhibit before another error indication is made to accommodate the response of the reverse channel. (Normally the sender alarms on detecting the line break or reverse channel pulse, so additional error indications are not required.) This wiring is also used when a lamp is to be lighted on the first error which remains on until reset. Removing straps A and B to eliminate the error indication inhibit and reduce the output pulse to 3.5 ms allows a high speed counter to record errors at the character rate at 1050 baud. Adding a capacitor between terminals 29 and 30 with straps A and B removed allows a low speed counter to record errors at the character rate at 110 or 150 baud and error bursts at 1050 baud.

Note: The low speed counter supplied with the SA110 BB, SA110 CB, and SA110 EB requires a minimum make duration (output pulse) of 30 ms and a minimum break duration (delay between output pulses) of 30 ms. With a 2 microfarad capacitor added between terminals 29 and 30, the 31 ms output pulse leaves a remainder of the character duration at 150 baud of about 36 ms, permitting consecutive errors to be registered at both 110 and 150 baud.

3.29 Whatever its duration, the output pulse from the collector of Q5 is passed to relay driver Q6, either directly or through a latching circuit. This relay driver is normally held off (collector at +14 volts) by a low signal from Q5 or the latching circuit. When the output pulse is developed, Q6 turns on (collector at 0 volt) for the duration of the output pulse. Normally relay K1 is energized while Q6 is on,



Example: T1 = 500 ms (factory wiring)

(a) T2 = 250 ms (factory wiring)

T1 - T2 = 250 ms inhibit between error indications

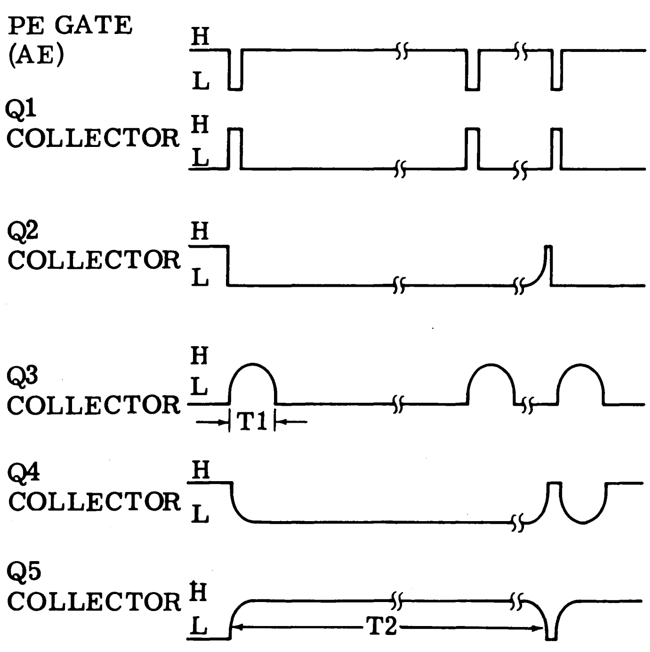
Minimum repetitive error indication interval = 500 ms (T1)

(b) T2 = 3.5 ms (strap option)

T1 - T2 = 496.5 ms inhibit between error indications

Minimum repetitive error indication interval = 500 ms (T1)

Case A - T1 (One-Shot Q2-Q3) > T2 (One-Shot Q4-Q5)



Example: T1 = 1 ms (strap option)

(a) T2 = 250 ms (factory wiring)

T1 < T2; inhibit between error indications = 0 ms

Minimum repetitive error indication interval = 250 ms (T2)

(b) T2 = 3.5 ms (strap option)

T1 < T2; inhibit between error indications = 0 ms

Minimum repetitive error indication interval = 3.5 ms (T2)

Case B - T1 (One-Shot Q2-Q3) < T2 (One-Shot Q4-Q5)

Figure 5 - Break Generator One-Shot Multivibrator Timing

TABLE B

ERROR INDICATION TIMING OPTIONS

STRAP A	STRAP B	ADDED CAPACITOR*	T1 (Q2-Q3)	T2 (Q4-Q5)	OUTPUT PULSE	INH BETWEEN ERROR IND	MIN ERROR IND INTERVAL
Closed	Closed	None	500 MS	250 MS	250 MS	250 MS	500 MS
Closed	Open	None	500 MS	3.5 MS	3.5 MS	496.5 MS	500 MS
Open	Closed	None	1 MS	250 MS	250 MS	0	250 MS
Open	Open	None	1 MS	3.5 MS	3.5 MS	0	3.5 MS
Open	Open	5 MFD Across 29-30	1 MS	65 MS	65 MS	0	65 MS
Open	Open	2 MFD Across 29-30	1 MS	31 MS	31 MS	0	31 MS

*These values are shown for example only. Other durations for T1 and T2 are obtainable with other capacitor values.

generating a line break or visually indicating the error by actuating a low speed error counter and lighting an indicator lamp, or lighting an indicator lamp only.

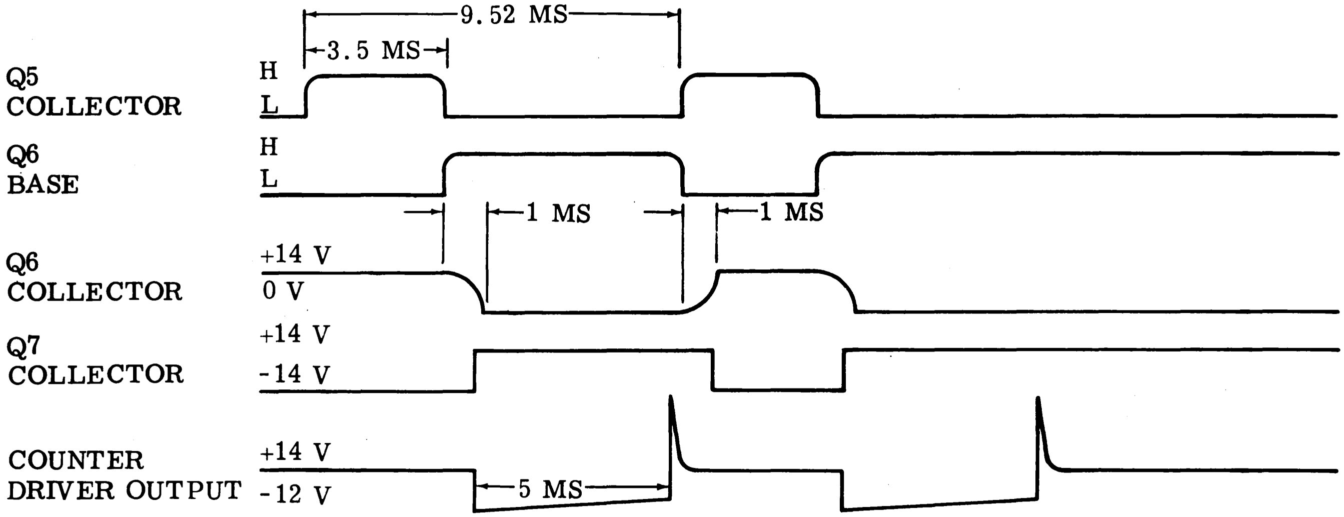
3.30 Because Q6 is normally off, the positive potential at its collector holds output amplifier Q7 off. The output of card MC405 at terminal 11 thus is normally -14 volts. When Q6 turns on, Q7 is turned on and its output rises to +14 volts. Terminal 11 remains at this level until Q6 turns off. This signal is used to advance a high speed error counter.

3.31 An option is available to replace the coil of relay K1 in the collector circuit of Q6 by a resistive load for counter operation at 2400 baud. This is done by leaving strap C in and removing strap D. It may not be desirable to use this option in every case, however, because it disables the indicator lamp. Refer to Figure 6 for the timing for high speed operation.

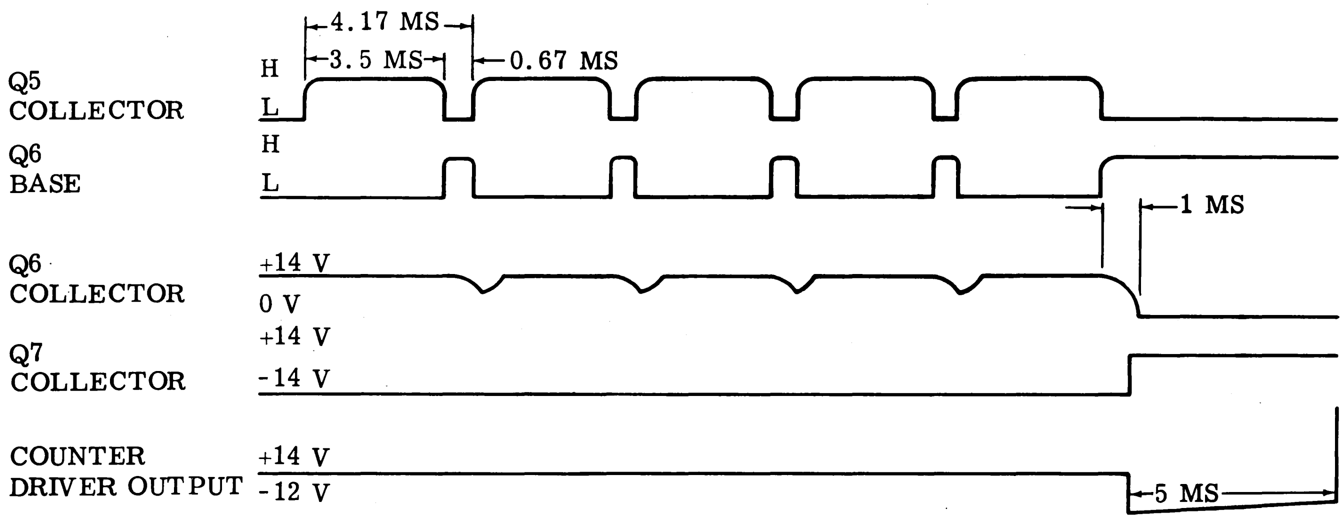
(a) For 1050 baud operation (Part A), the 3.5 ms output pulse is much shorter than the 9.52 ms character duration. (The "blink" option of the latching circuit inverts the output pulse, but counter operation is not affected except for the short delay before the counter actuating pulse is generated.) Consequently, the delay of roughly one millisecond at the collector of Q6 due to the coil of relay K1 (operate time 1 ms, release time 1 ms) has no effect on the output at the collector of Q7 other than to delay each transition slightly. This output is connected to a counter driver which generates a negative-going pulse of 5 to 6 ms duration for every output pulse at Q7 to actuate the high speed counter.

(b) For 2400 baud operation with the relay coil in the circuit and the latching circuit strapped for the blink option (Part B), the duration of each character is only 0.67 ms more than the 3.5 ms output pulse. If errors are received consecutively, the 1 ms delay caused by the inductance of the relay coil prevents the collector of Q6 from dropping to 0 volt on any output pulse before the last. As a result, only one pulse will be generated by the counter driver — regardless of how many consecutive errors are in the burst.

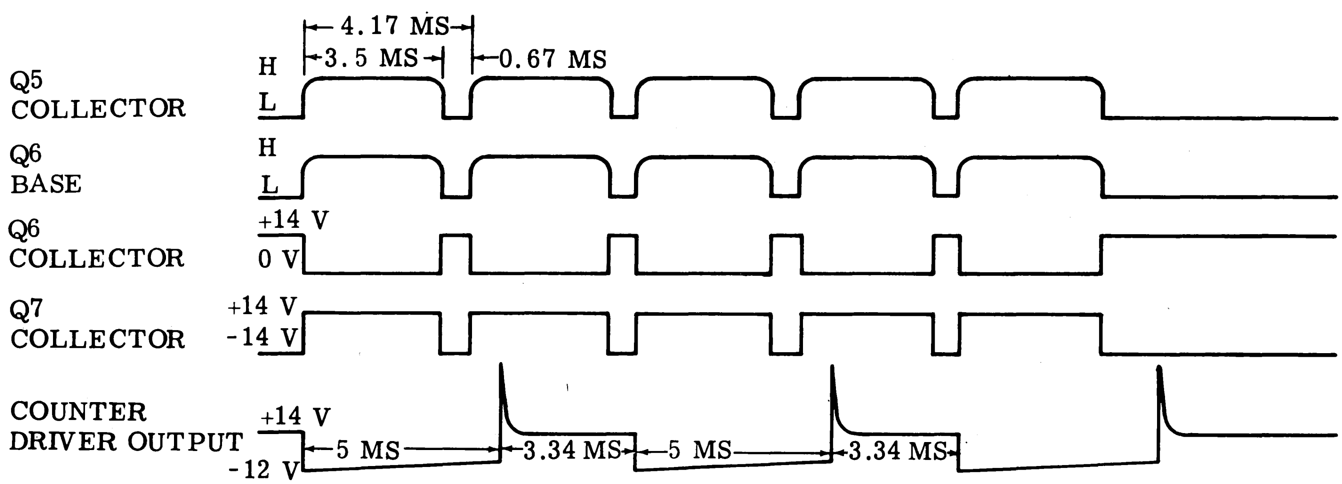
(c) If the latching circuit is bypassed and the relay coil is strapped out of the circuit (Part C), the output at Q7 is the same as the 3.5 ms output pulse at Q5 (except for squarer transitions), so an output to the counter driver is produced for every error. The counter driver cannot operate this fast, but produces 5 to 6 ms pulses at half the character rate. However, there is an interval of only 3.34 ms at most between consecutive pulses; the high speed counter nominally requires a minimum of 5 ms between actuating pulses, though most counters will operate correctly with a somewhat shorter interval. Nevertheless, this interval between pulses is probably too short to allow most counters to reset fully before being actuated again. Consequently erratic operation can be expected when this option is used, depending on the characteristics of the particular high speed counter furnished. The choice of option for 2400 baud operation, therefore, depends on whether the improvement in consecutive error counting obtained is worth disabling the indicator lamp to get.



A. 1050 Baud Operation, Strapped for Relay Latch for First Error and Blink



B. 2400 Baud Operation, Strapped for Relay Latch for First Error and Blink



C. 2400 Baud Operation Strapped for No Latch and Relay Coil Not in Circuit

Figure 6 - High Speed Counter Output Timing

3.32 Bypassing the latching circuit is accomplished by leaving strap E closed and opening straps F and G. This causes the output pulse at the collector of Q5 to pass unchanged to the base of Q6, energizing the relay or producing an output to a counter driver as described in 3.31 (c).

3.33 The permanent latch option is obtained by leaving strap G closed and opening straps E and F. This energizes relay K1 on the first error detected and latches it in this state until manually reset. This option is used for the SA110 EC, which has an indicator lamp only, to notify the operator that the received message contains one or more errors.

(a) In the quiescent state, Q5 is normally conducting and its collector is at approximately 0 volt. This signal is inverted by MLA-11 and connected to pin 10 of NAND gate MLA-8 as +6 volts. Pin 9 of MLA-8 is also connected to +6 volts through resistor R21, so the output of MLA-8 is 0 volt, holding Q8 off. The output of MLA-8 is also connected to pin 1 of NAND gate MLA-3, holding its output high and the output of MLA-6 low. This low potential is applied to the base of relay driver Q6 to hold it off.

(b) When an error is detected, one-shot Q4-Q5 is triggered and its output, at the collector of Q5, rises to +6 volts. The output of MLA-11 then drops to 0 volt, which produces a high output at MLA-8. This positive potential turns Q8 on. Its collector potential goes to approximately 0 volt (since 0 volt is connected to the emitter from the indicator assembly, via the manual reset switch and terminal 9), supplying a low input to MLA-8 to maintain its output high after the collector of Q5 returns to 0 volt. The high output from MLA-8 causes the output of MLA-3 to be low and the output of MLA-6 high, turning on relay driver Q6 and energizing the relay.

(c) Relay K1 remains energized — and the indicator lamp remains on — until the manual switch (in the lamp housing) is depressed. This action opens a normally-closed contact between the emitter of Q8 and ground, raising the collector potential of Q8 to +6 volts. The output of MLA-8 then drops to 0 volt, turning Q8 off and restoring MLA-3 and MLA-6 to their quiescent states. This turns off Q6 and releases the relay.

3.34 The permanent latch with "blink" option is programmed by opening strap E but leaving straps F and G closed. Relay K1 is energized for the first error detected and remains energized until manually reset as for the permanent latch option described above. Succeeding errors, however, cause the relay to de-energize at the beginning of the output pulse from Q5 and energize again at the end. The indicator lamp is powered through the relay contacts, so it turns on with the first error and blinks off and on with each following error. At 110, 150, or 1050 baud using the low speed counter the blink is clearly visible, but at 1050 baud and higher speeds using the high speed counter it usually is not. The low speed counter is also driven by the relay contacts and advances its count for each blink. The high speed counter (not driven by the relay contacts) can record consecutive errors at 1050 baud with this option, even though the indicator lamp appears to be on all the time.

(a) In the quiescent state, relay driver Q6 is held off as described in 3.33 (a). When an error is detected, one-shot Q4-Q5 is triggered, the potential at the collector of Q5 goes positive, and the output of MLA-11 drops to 0 volt. This low signal produces a high output at MLA-8, which turns on Q8. Up to this point operation is the same as for the permanent latch option. With the blink option, however, the low output of MLA-11 is connected to the other input of MLA-3, holding its output high. The resulting low output at MLA-6 holds relay driver Q6 off, keeping the relay de-energized.

(b) At the end of the Q4-Q5 timeout period, the collector of Q5 returns to 0 volt and the output of MLA-11 becomes high again. This signal causes the outputs of MLA-3 to go low and of MLA-6 to go high, turning relay driver Q6 on and energizing the relay. The relay is latched on by the output of Q8, via MLA-8, MLA-3, and MLA-6. When one-shot Q4-Q5 times out on succeeding errors, the output of MLA-11 will drop from high to low for the duration of the timeout period. This change is applied to an input of MLA-3, producing a corresponding change at MLA-6 and Q6. As a result, the relay is de-energized at the beginning of the timeout period and re-energized at the end.

3.35 The SA110 has a built-in lamp test feature for applications in which a lamp is driven by the relay contacts. By connecting a normally-open test contact between terminal 7 (the collector of Q6) and ground, the relay may be energized momentarily by closing this contact.

4. VARIABLE FEATURES

4.01 Versions of the SA110 are available for installation on 33 or 35 type receivers, DATASPEED Type 2 receivers, or other equipment. For each type of terminal two or four optional bypass switch or indicator assemblies are available (Table A and Figure 2) which are connected to the SA110 chassis by a cable. Those for 33 and 35 type terminals mount adjacent to the call control unit or copyholder, while those for DATASPEED Type 2 receivers have magnetic bases for mounting on top of the cabinet.

4.02 Three of the optional assemblies (TP327631, TP327633, and TP327640) provide a bypass switch only. They are used in applications in which a line break on a half-duplex line or on reverse channel is generated whenever an error is detected. Bypassing the accessory with the switch is necessary for the terminal to receive messages from nonparity senders. One assembly (TP327639) provides a bypass switch and indicator lamp to notify the operator of the receiving station that an error has been detected (a break cannot be generated when this assembly is used). The other assemblies all provide a bypass switch, indicator lamp, and error counter (either low or high speed) to enable the receiving operator to decide — on the basis of the number of errors counted and the length and content of the message — whether to accept the message or request a retransmission. These assemblies are also useful for maintenance purposes, since they allow transmission errors to be distinguished from machine errors.

Note: When the low speed counter is used in high speed operation (SA110 EB), only the number of widely-separated individual errors or error bursts will be recorded. The count registered may be as low as 15 percent of the number of errors detected by the SA110.

BYPASS SWITCH AND INDICATOR ASSEMBLIES FOR 33 TYPE SETS

4.03 Assemblies TP327631 and TP327632 are designed to be mounted on 33 type ASR, KSR, or RO sets. They are attached to a bracket which clips on the cover underneath the ivory lid and hooks around on the bottom edge at the rear (Figure 7). A single cable connects the assembly to the SA110 chassis which is placed inside the stand or mounted on an adjacent wall or table.

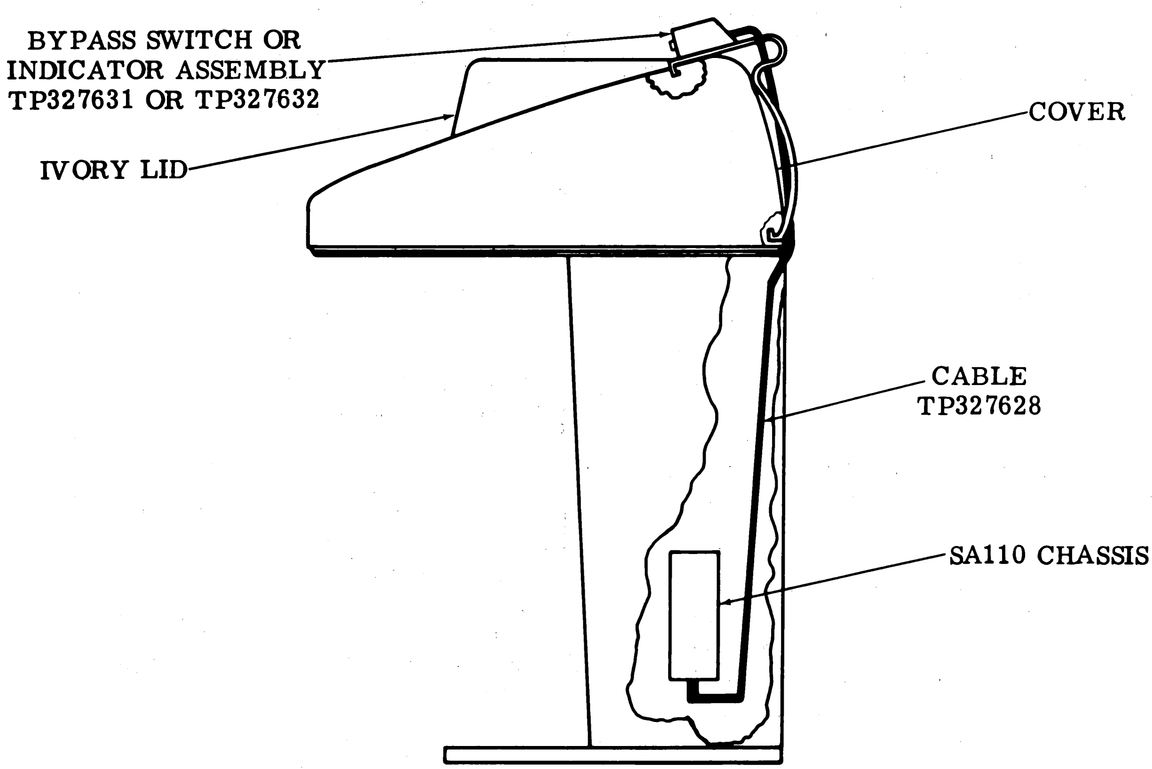


Figure 7 - Location of SA110 Chassis and Bypass Switch or Indicator Assembly on 33 Type Set

4.04 The wiring for bypass switch assembly TP327631, the SA110 chassis, and the terminal is shown in simplified form on Figure 8. Refer to 8716WD for a complete schematic and to 8566WD for actual wiring information.

(a) The bypass switch, SW1, has four transfer contacts but only three of them are used. In the bypass position (as shown on Figure 8), the data set output is fed in at pin 5 on the orange wire, transferred to pin 4, and fed out to the SMD input of the terminal on the yellow wire. Since pin 2 is closed to pin 6, the data output of the SA110 (white wire) is connected to the data input of the SA110 (red wire). The white-slate and white-purple wires are in series with the BREAK contact of the terminal (if present) and are tied together at pins 7 and 8. The slate and purple wires connect to the relay break contact in the SA110.

(b) When SW1 is activated, the data set output at pin 5 (orange wire) is transferred to pin 6 (red wire) where it is supplied to the data input of the SA110. The data output of the SA110 (white wire) at pin 2 is transferred to pin 4 (yellow wire) where it is supplied to the input of the SMD. This places the SA110 in series with the incoming data stream between the data set and the terminal. Also, the white-slate and white-purple wires at pins 7 and 8 are disconnected and the break contact of the SA110 relay is inserted between them in series. When energized, this relay opens the output data line, thereby causing a break to be generated.

4.05 The wiring for bypass switch and indicator assembly TP327632, the SA110 chassis, and the terminal is shown in simplified form on Figure 9. Refer to 8716WD for a complete schematic and to 8566WD for actual wiring information.

(a) The bypass switch, SW1, has four transfer contacts but only three of them are used. In the bypass position (as shown on Figure 9), the data set output is fed in at pin 5 on the orange wire, transferred to pin 4, and fed out to the SMD input of the terminal on the yellow wire. Since pin 2 is closed to pin 6, the data output of the SA110 (white wire) is connected to the data input of the SA110 (red wire). Since the bypass switch and indicator assembly does not have break generation capability, the white-slate and white-purple wires are tied back at the terminal.

(b) When SW1 is activated, the data set output at pin 5 (orange wire) is transferred to pin 6 (red wire) where it is supplied to the data input of the SA110. The data output of the SA110 (white wire) at pin 2 is transferred to pin 4 (yellow wire) where it is supplied to the input of the SMD. This places the SA110 in series with the incoming data stream, as for the TP327631 assembly. The counter coil, DS2, and the lamp, DS1, are connected to the relay transfer contact in the SA110. When the relay is energized, this contact permits the counter to register the error and the lamp to light. Depending on the SA110 strapping (3.29 and 3.34), the lamp will flash on for each error or latch on for the first error and flash off for each additional error. For each flash (on or off) of the lamp, the counter will register another count. The reset switch, SW2, extinguishes the lamp when the lamp housing is depressed; the counter is mechanically reset to zero by its own pushbutton.

BYPASS SWITCH AND INDICATOR ASSEMBLIES FOR 35 TYPE SETS

4.06 Assemblies TP327633 and TP327634 can be mounted on 35 type ASR, KSR, or RO sets. Two holes are drilled in the upper cover of the terminal and the bypass or indicator assembly attached with screws and lockwashers (Figure 10). A single cable connects the assembly to the electrical service unit "C" wiring field and the SA110 chassis, which is placed inside the pedestal or mounted on an adjacent wall or table.

4.07 The wiring for assemblies TP327633 and TP327634 is identical to that for assemblies TP327631 and TP327632, respectively (4.04 and 4.05).

BYPASS SWITCH AND INDICATOR ASSEMBLIES FOR "DATASPEED" RECEIVERS

4.08 Assemblies TP327637 through TP327640 are for use on DATASPEED receivers. They are held on the top of the cabinet by means of two magnets attached to the bottom of the assembly (Figure 11). Two cables are supplied to connect the assembly to the data set and the SA110 chassis, which is placed on a shelf inside the cabinet.

4.09 The wiring for bypass switch assembly TP327640, the SA110 chassis, the terminal, and the data set is shown in simplified

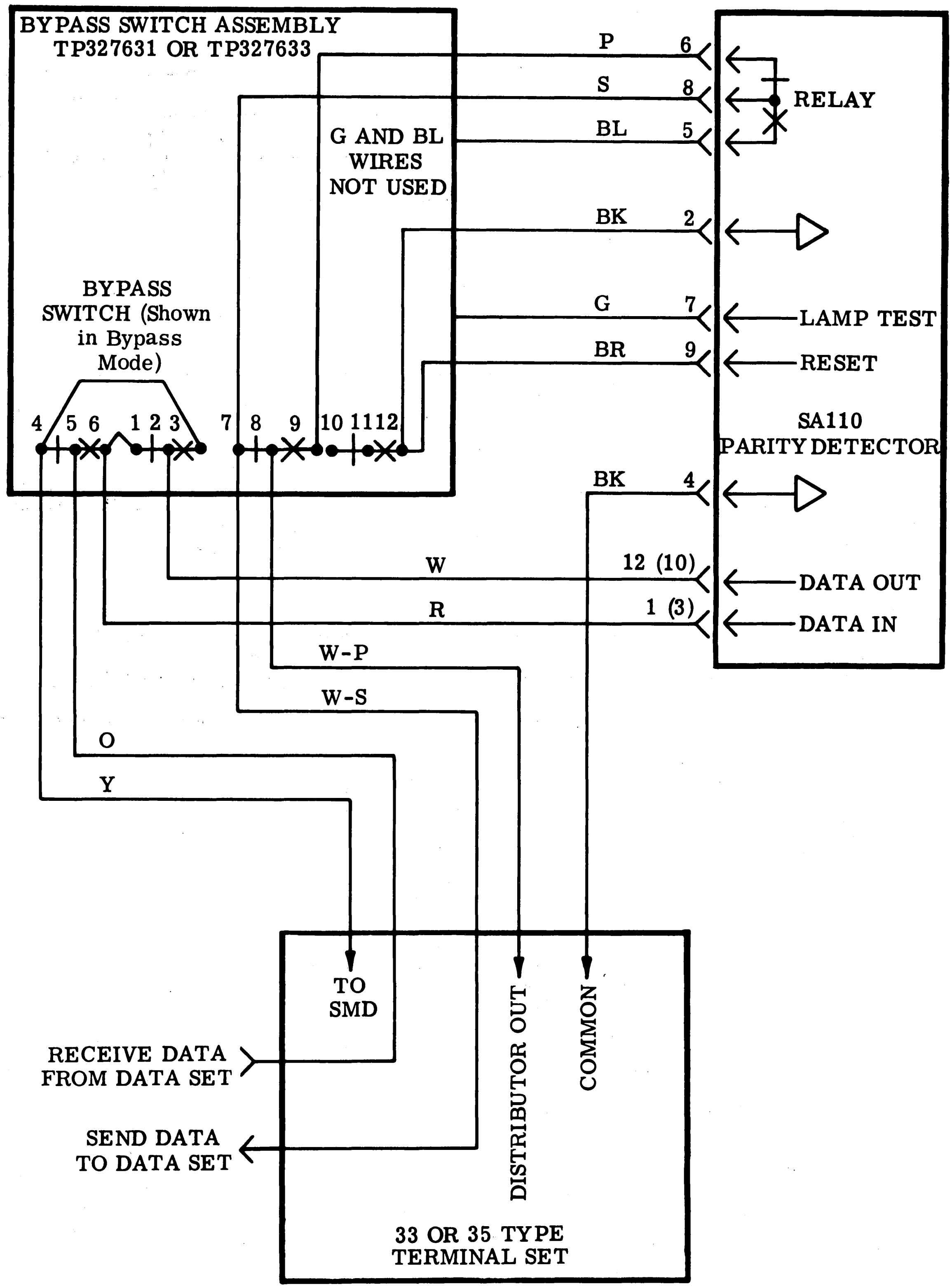


Figure 8 - Simplified Wiring for SA110 BA and SA110 CA

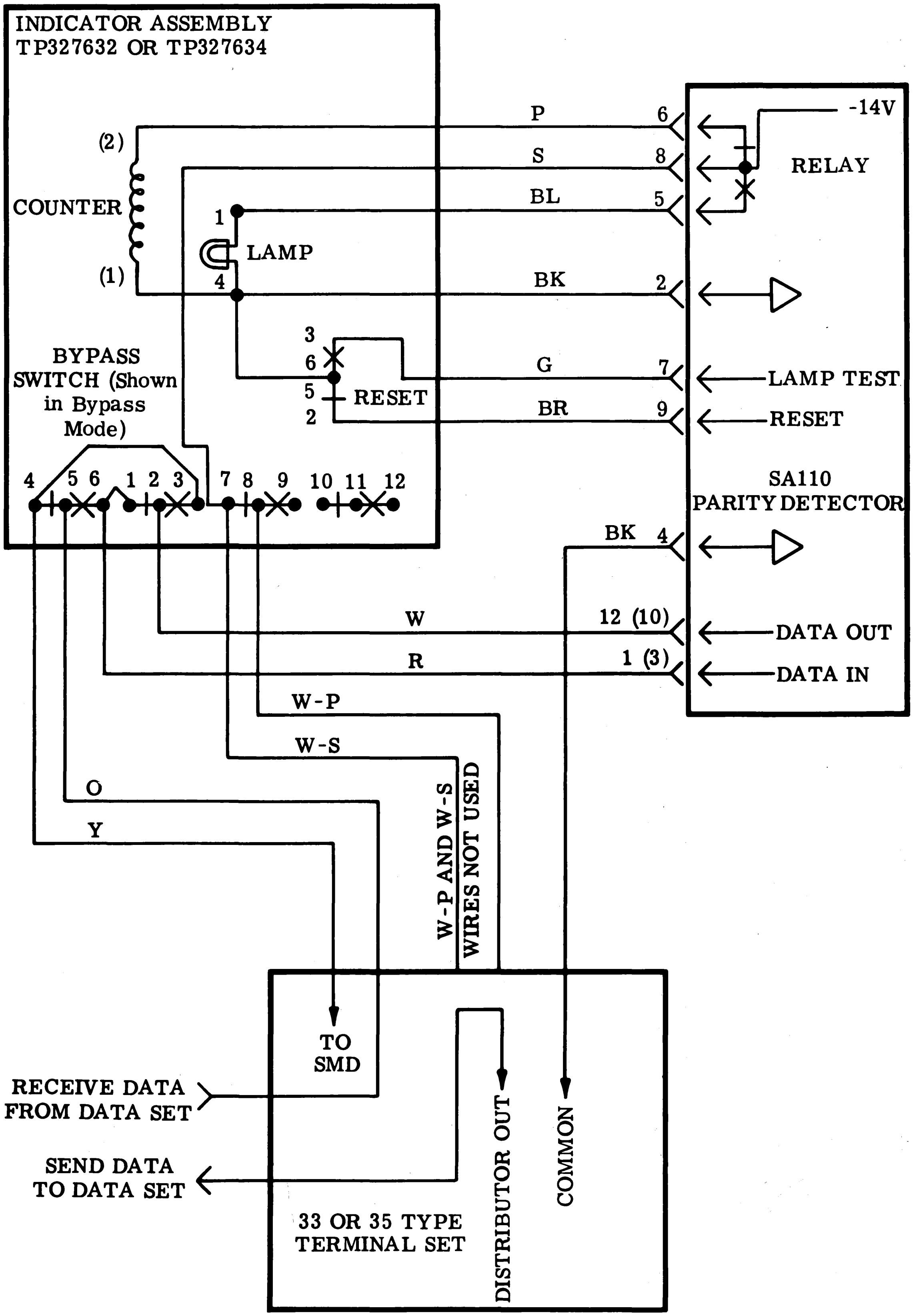


Figure 9 - Simplified Wiring for SA110 BB and SA110 CB

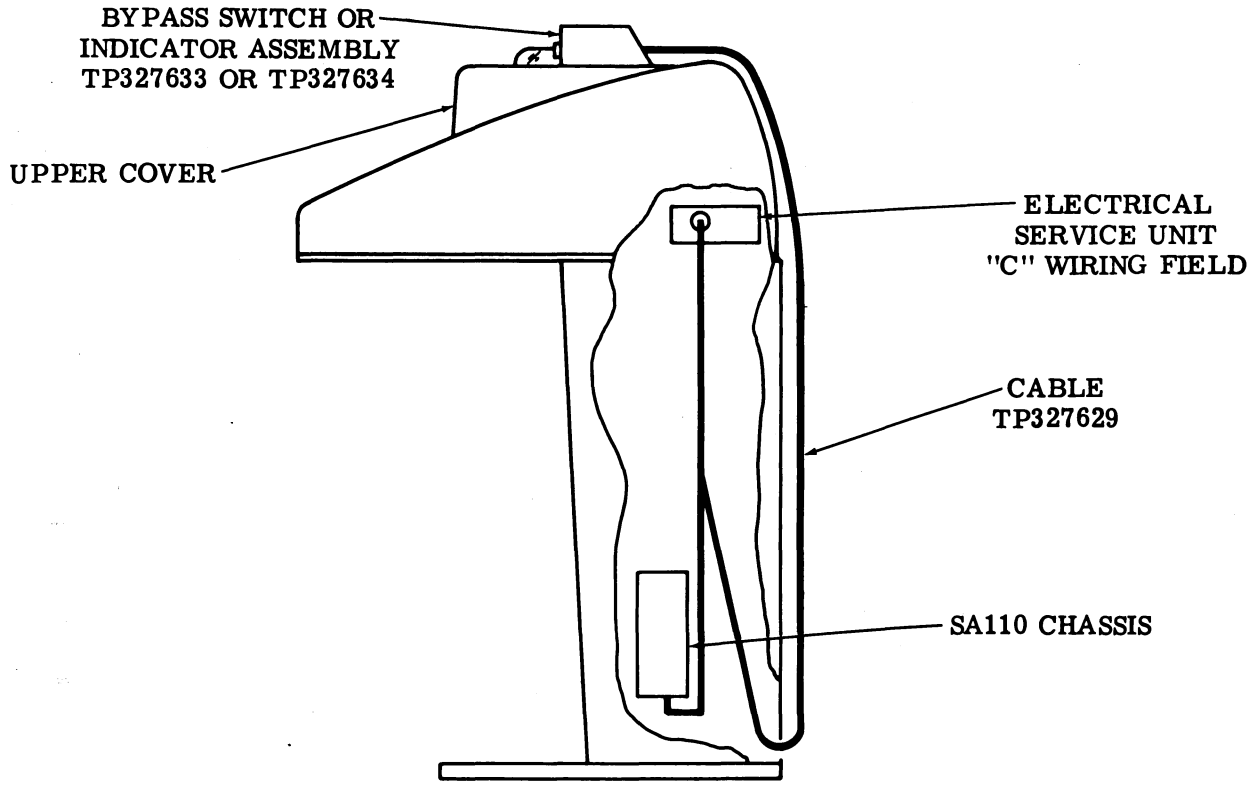


Figure 11 - Location of SA110 Chassis and Bypass Switch or Indicator Assembly on 35 Type Set

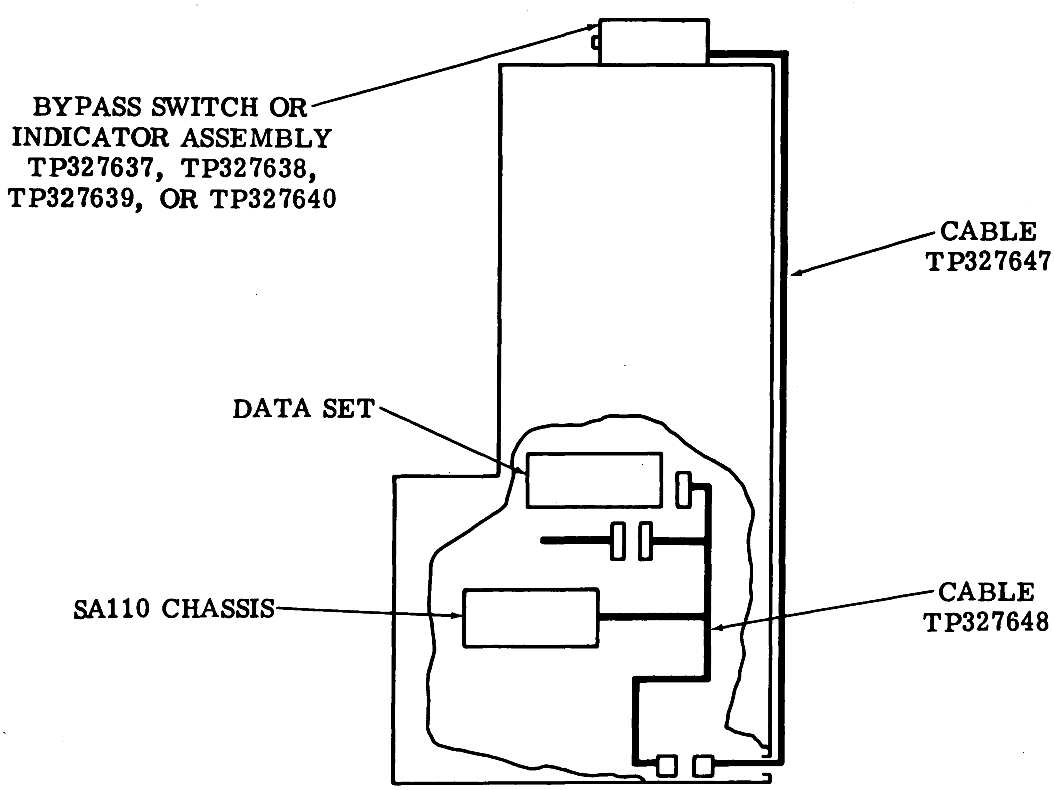


Figure 11 - Location of SA110 Chassis and Bypass Switch or Indicator Assembly on DATASPEED Receiver

form on Figure 12. Refer to 8717WD for a complete schematic and to 8567WD for actual wiring information.

(a) The bypass switch, SW1, is wired similarly to those for bypass switch assemblies TP327631 and TP327633. In the bypass position (as shown on Figure 12), the data set output is fed in at pin 5 on the orange wire, transferred to pin 4, and fed out to the receiving distributor input of the terminal on the yellow wire. Since pin 2 is closed to pin 6, the data output of the SA110 (white wire) is connected to the data input of the SA110 (red wire). The white-purple wire brings +17.5 volts from the data set (via the DATASPEED receiver) to pin 8, where it is transferred to pin 7 and connected by the white-slate wire to the supervisory transmitted data input of the data set, holding reverse channel on at all times. The slate and purple wires connect to the relay break contact in the SA110.

(b) When SW1 is activated, the data set output at pin 5 (orange wire) is transferred to pin 6 (red wire) where it is supplied to the data input of the SA110. The data output of the SA110 (white wire) at pin 2 is transferred to pin 4 (yellow wire) where it is supplied to the input of the receiving distributor. This places the SA110 in series with the incoming data stream between the data set and the terminal. Also, the white-slate and white-purple wires at pins 7 and 8 are disconnected and the break contact of the SA110 relay is inserted between them in series. When energized, this relay opens the path to the supervisory transmitted data input, thereby causing a break on reverse channel to be generated.

4.10 The wiring for bypass switch and indicator assembly TP327638, the SA110 chassis, the terminal, and the data set is shown in simplified form on Figure 13. Refer to 8717WD for a complete schematic and to 8567WD for actual wiring information.

(a) The bypass switch, SW1, has four transfer contacts but only three of them are used. In the bypass position (as shown on Figure 13), the data set output is fed in at pin 5 on the orange wire, transferred to pin 4, and fed out to the receiving distributor input of the terminal on the yellow wire. Since pin 2 is closed to pin 6, the data output of the SA110 (white wire) is connected to the data input of the SA110 (red wire). The white-purple wire brings +17.5 volts from the data set (via the DATASPEED receiver) to pin 7, where it joins the white-slate wire connected to the supervisory transmitted data input of a 202C data set. Reverse channel, if present, is therefore held on at all times regardless of the position of the bypass switch. (A 202A data set, which does not have reverse channel, has no connection to the pin that the +17.5 volts is wired to.)

(b) When SW1 is activated, the data set output at pin 5 (orange wire) is transferred to pin 6 (red wire) where it is supplied to the data input of the SA110. The data output of the SA110 (white wire) at pin 2 is transferred to pin 4 (yellow wire) where it is supplied to the input of the receiving distributor. This places the SA110 in series with the incoming data stream between the data set and the terminal, as for the TP327640 assembly. The low speed counter coil, DS2, and the lamp, DS1, are connected to the relay transfer contact in the SA110. When the relay is energized, this contact permits the counter to register the error (or error burst) and the lamp to light. Depending on the SA110 strapping (3.29 and 3.34), the lamp will flash on each error (or error burst) or latch on for the first error and flash off for each additional error (or burst). For each flash (on or off) of the lamp, the counter will register another count. As explained in 3.28 and 4.02, this count may be much less than the number of individual errors actually detected by the SA110 because the time required to activate and deactivate the counter is much longer than the duration of a character. The reset switch, SW2, extinguishes the lamp when the lamp housing is depressed; the counter is mechanically reset to zero by its own pushbutton.

4.11 The wiring for bypass switch and indicator assembly TP327639, the SA110 chassis, the terminal, and the data set is shown in simplified form on Figure 14. Refer to 8717WD for a complete schematic and to 8567WD for actual wiring information.

(a) Bypass switch SW1 is shown in the bypass position on Figure 14. The wiring for it is identical to that for bypass switch and indicator assembly TP327638 (4.10 (a)).

(b) When SW1 is activated, the data set output at pin 5 (orange wire) is transferred to pin 6 (red wire) where it is supplied to the data input of the SA110. The data output of the SA110 (white wire) at pin 2 is transferred

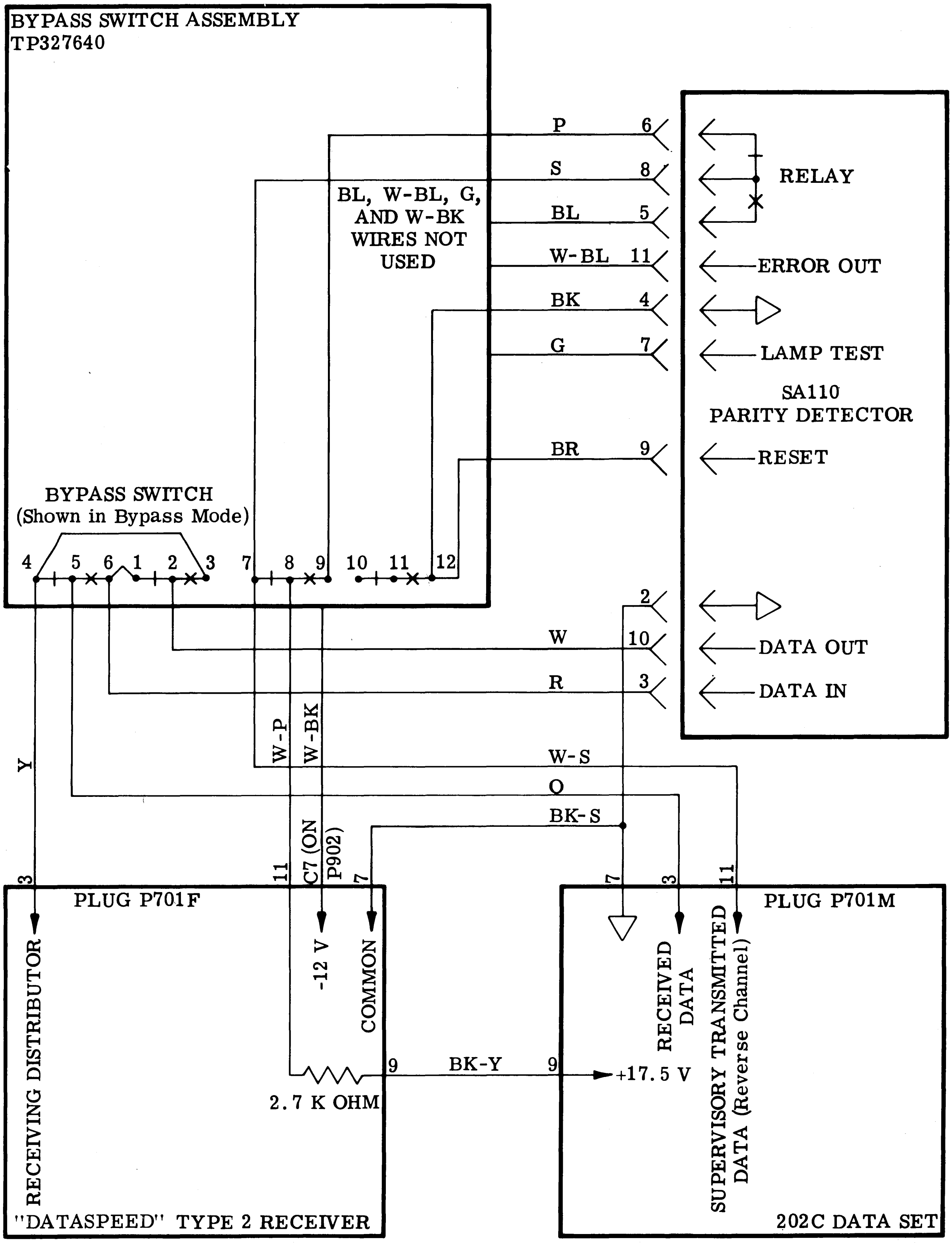


Figure 12 - Simplified Wiring for SA110 EA

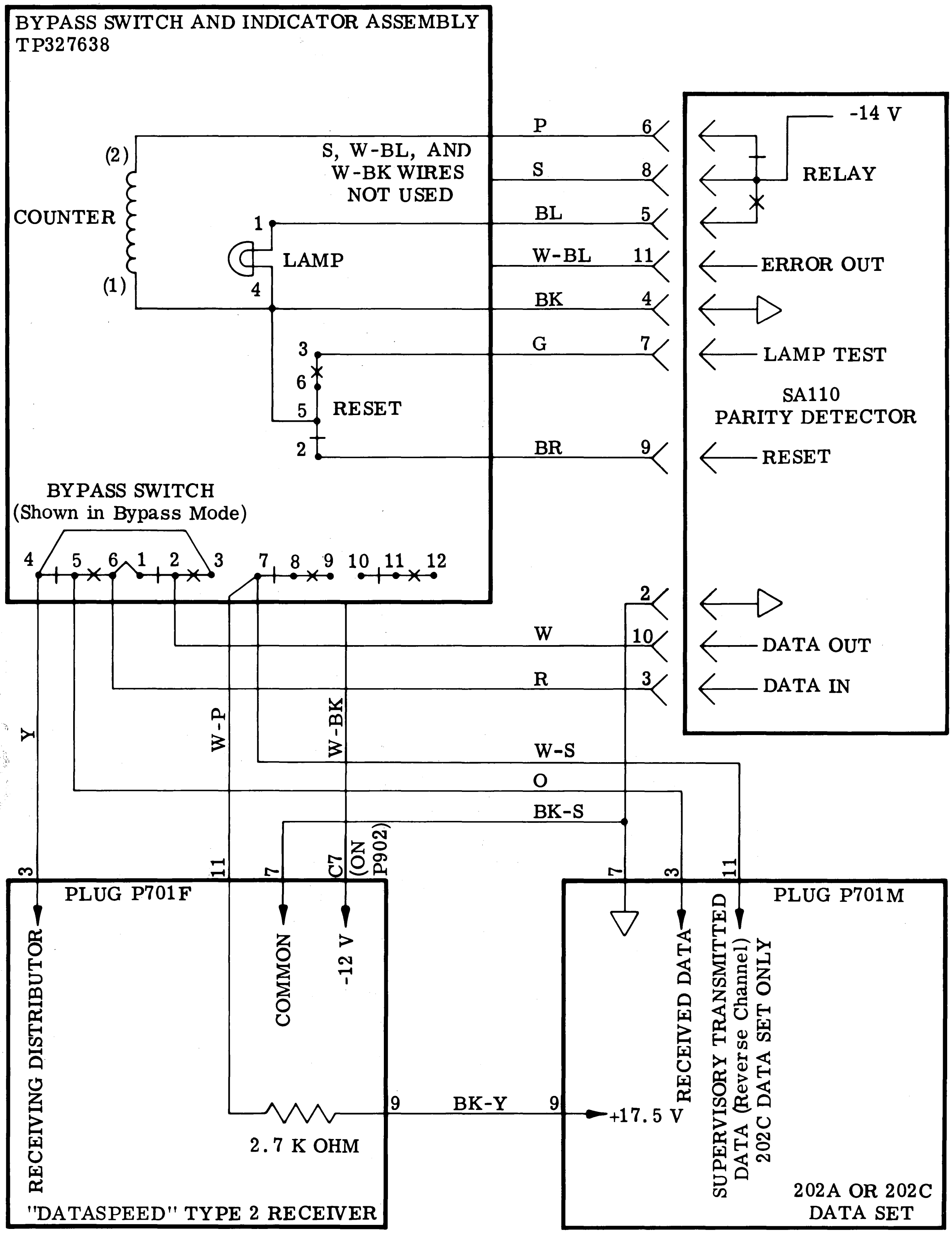


Figure 13 - Simplified Wiring for SA110 EB

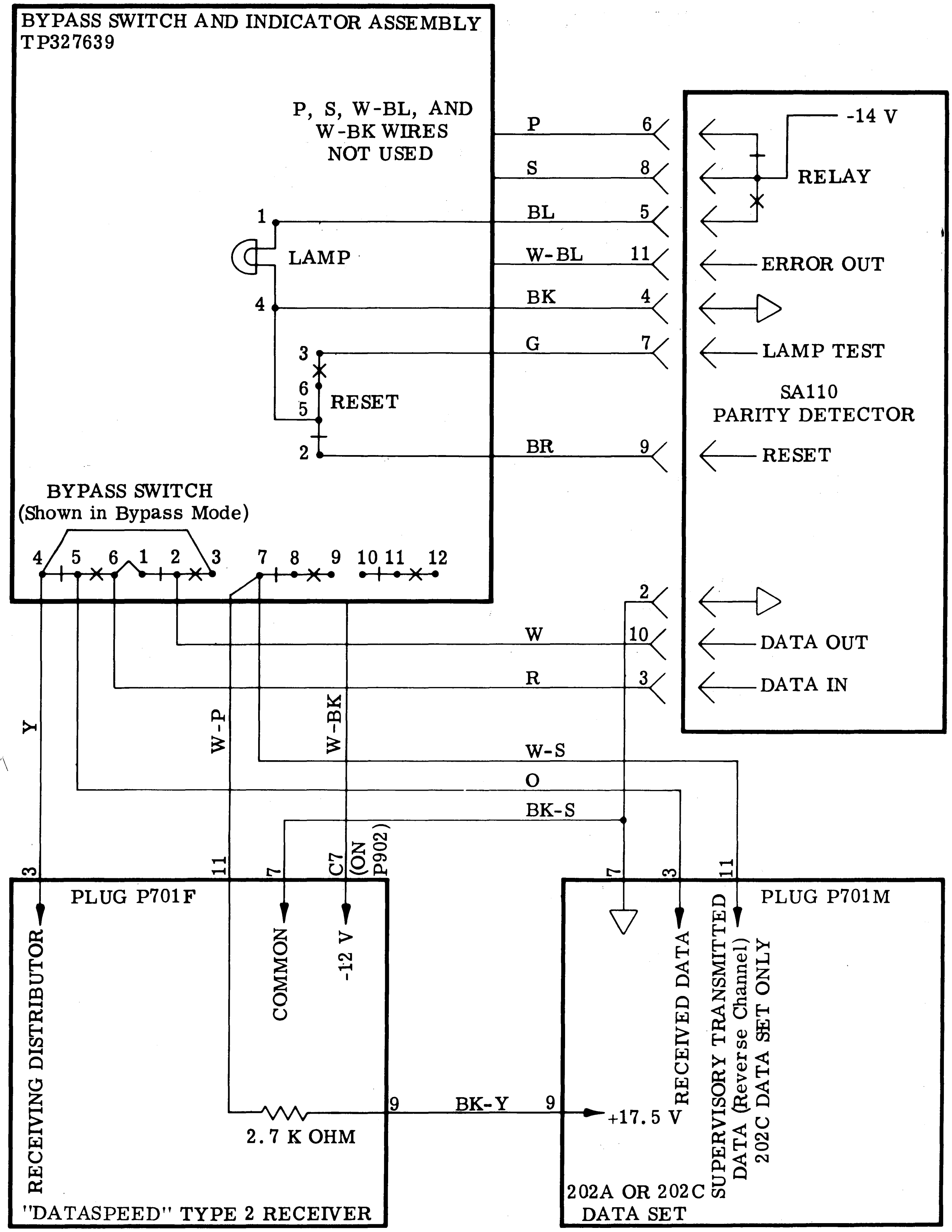


Figure 14 - Simplified Wiring for SA110 EC

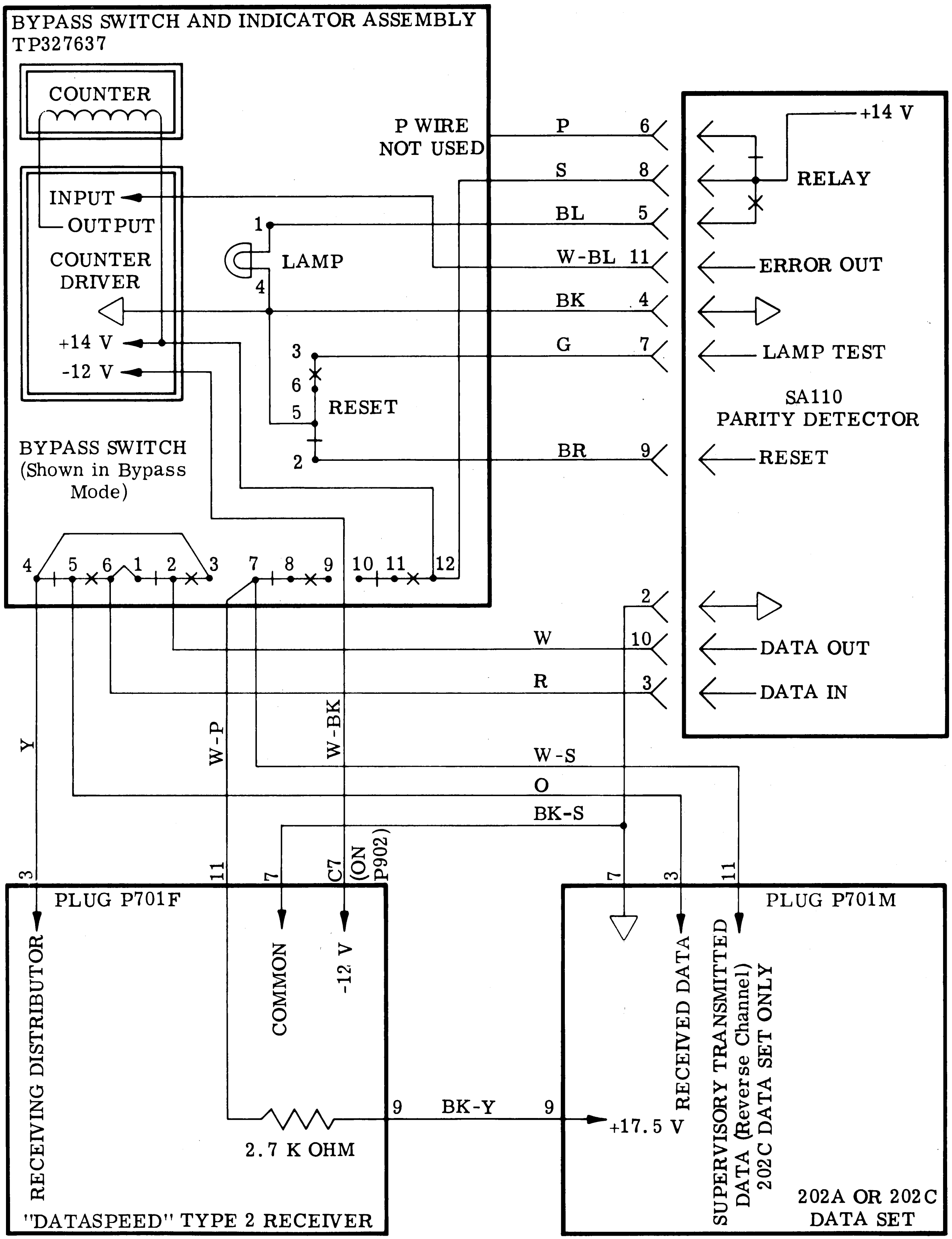


Figure 15 - Simplified Wiring for SA110 ED

to pin 4 (yellow wire) where it is applied to the input of the receiving distributor. This places the SA110 in series with the incoming data stream between the data set and the terminal, as for the TP327640 and TP327639 assemblies. The lamp, DS1, is connected to the relay transfer contact in the SA110. When the relay is energized for the first time, this contact lights the lamp to indicate that an error was received. The SA110 is strapped so that the relay latches on the first error (3.33), holding the lamp on until it is reset by depressing the lamp housing (SW2).

4.12 The wiring for bypass switch and indicator assembly TP327637, the SA110 chassis, the terminal, and the data set is shown in simplified form on Figure 15. Refer to 8717WD for a complete schematic and to 8567WD and 322423 for actual wiring information.

(a) Bypass switch, SW1, is shown in the bypass position on Figure 15. The wiring for it is identical to that for bypass switch and indicator assembly TP327638 (4.10 (a)).

(b) When SW1 is activated, the data set output at pin 5 (orange wire) is transferred to pin 6 (red wire) where it is supplied to the data input of the SA110. The data output of the SA110 (white wire) at pin 2 is transferred to pin 4 (yellow wire) where it is supplied to the input of the receiving distributor. This places the SA110 in series with the incoming data stream between the data set and the terminal, as for the other DATASPEED assemblies. The lamp, DS1, is connected to the relay transfer contact in the SA110 but the high speed counter coil, DS2, is not. Instead, the counter is driven by counter driver Z1, whose power comes from the DATASPEED receiver (-12 volts) and the SA110 chassis (+14 volts). When the first error is detected, the relay is energized and the energizing pulse is amplified and connected to the counter driver (via the white-blue wire) as the error out signal, causing the counter to register the error. The SA110 is strapped so that the relay latches for the first error and de-energizes and re-energizes for each additional error (3.34). The relay contact, therefore, lights the lamp for the first error and flashes it off and on again for each additional error. (This flash is so brief that it may not be seen.) For each flash of the lamp, the counter registers another count. The reset switch, SW2, extinguishes the lamp when the lamp housing is depressed; the counter is mechanically reset to zero by its own pushbutton.