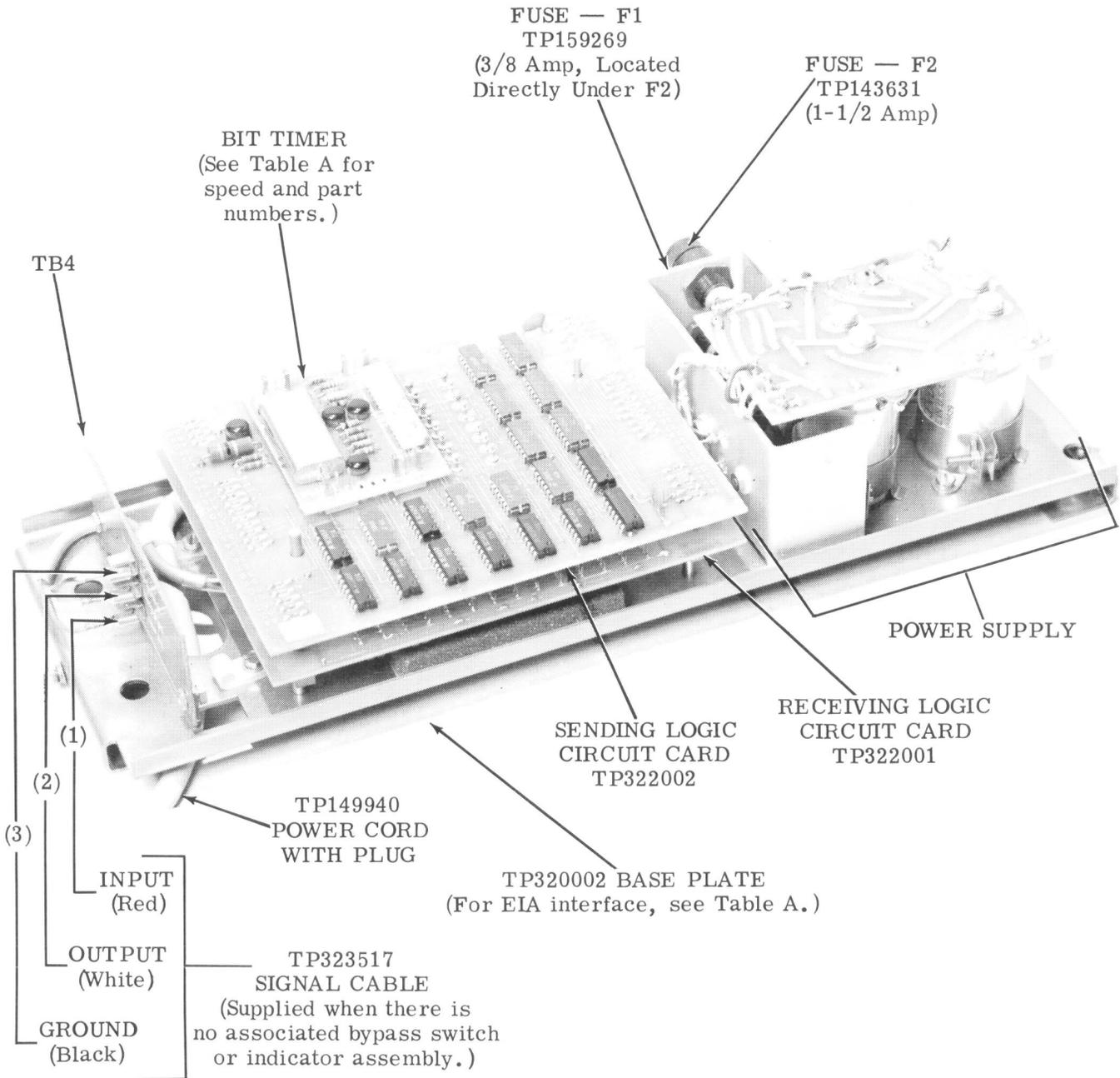PARITY FAILURE DETECTOR AND

SUBSTITUTE CHARACTER INSERTER (SA120)

DESCRIPTION AND PRINCIPLES OF OPERATION

## 1. GENERAL

1.01 This section provides the description and principles of operation for the SA120 parity failure detector and substitute character inserter (Figure 1). It also provides the associated bypass and indicator assemblies (Figure 2). Refer to Section 578-200-201 for installation information, Section 578-200-301 for checkout and troubleshooting procedures, Section 578-200-801 for parts, and to WDP0204 for complete wiring diagram package.

1.02 As a parity detector, substitute character inserter and regenerative repeater for a receiver, the SA120 may be applied to Model 33 and 35 type automatic send-receive or receive-only terminals or to Type 2 Tape-To-Tape Systems. As a parity inserter and/or regenerative repeater, one SA120 version may be used with a sender. The SA120 parity detector can be used with any eight-level serial-by-bit signal that provides a parity bit, at any speed up to 2400 wpm.

FUSE — F1
TP159269
(3/8 Amp, Located
Directly Under F2)

FUSE — F2
TP143631
(1-1/2 Amp)

BIT TIMER
(See Table A for
speed and part
numbers.)

TB4

POWER SUPPLY

(1)

(2)

(3)

RECEIVING LOGIC
CIRCUIT CARD
TP322001

SENDING LOGIC
CIRCUIT CARD
TP322002

TP149940
POWER CORD
WITH PLUG

TP320002 BASE PLATE
(For EIA interface, see Table A.)

INPUT
(Red)

OUTPUT
(White)

TP323517
SIGNAL CABLE
(Supplied when there is
no associated bypass switch
or indicator assembly.)

GROUND
(Black)

Note 1: Base plate TP320001 includes two interface amplifiers (in place
of TB4) on circuit card TP323513 and must be used for current/no current
input and/or output (see Table A and 8200WD, Sheets 5 and 6).

Note 2: If either (not both) TP322400 break generator/counter driver or
TP322422 parity card is used, it is inserted between TP322002 and
TP322001 (see Table A).

Figure 1 - Typical SA120 Parity Failure Detector and Substitute Character
Inserter With Cover Removed

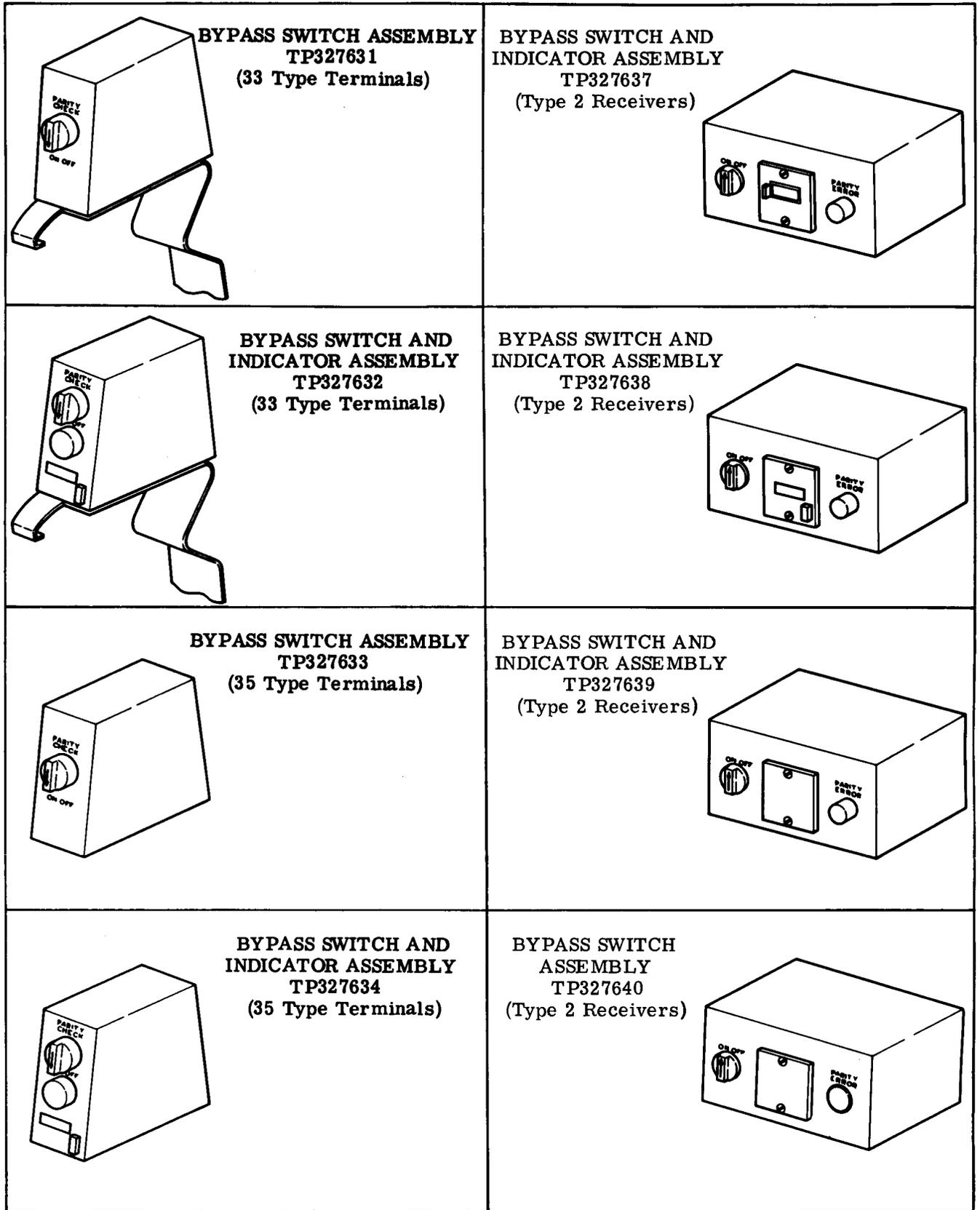| | |
|---|---|
| **BYPASS SWITCH ASSEMBLY**<br>**TP327631**<br>(33 Type Terminals) | BYPASS SWITCH AND<br>INDICATOR ASSEMBLY<br>TP327637<br>(Type 2 Receivers) |
| **BYPASS SWITCH AND**<br>**INDICATOR ASSEMBLY**<br>**TP327632**<br>(33 Type Terminals) | BYPASS SWITCH AND<br>INDICATOR ASSEMBLY<br>TP327638<br>(Type 2 Receivers) |
| **BYPASS SWITCH ASSEMBLY**<br>**TP327633**<br>(35 Type Terminals) | BYPASS SWITCH AND<br>INDICATOR ASSEMBLY<br>TP327639<br>(Type 2 Receivers) |
| **BYPASS SWITCH AND**<br>**INDICATOR ASSEMBLY**<br>**TP327634**<br>(35 Type Terminals) | BYPASS SWITCH<br>ASSEMBLY<br>TP327640<br>(Type 2 Receivers) |

Figure 2 - Bypass Switch and Indicator Assemblies

1.03 Error detection is accomplished ahead of the receiving device by checking each incoming character for parity. A character appearing with incorrect parity is converted into the code for a substitute character of the users choice (such as * or _) and strapped in by the installer. Therefore, the substitute character is printed instead of the errored one. A strap option provides for either even or odd parity detection.

1.04 Because the parity detector regenerates the incoming signal (from up to 45 percent distorted input to less than 5 percent at output) and checks the parity of the regenerated character, the error free message rate at the terminal is greatly improved. This method of error protection has the advantage of being applicable in any receiving situation without prearrangement with the sender(s) except for assurance of parity transmission. An SA120 equipped with a parity inserter card TP322422 may be used to insert parity in the sender signal line if required (4.06 and Figure 12). For users having a substantial amount of text traffic, the substitute character displayed for an errored character can permit the user to ignore the errors that can be read through, and to request a transmission repeat only when an error occurs in critical data. Errors may be counted and further indicated by a flashing lamp or the unit may be bypassed through use of a bypass and indicator assembly (Refer to Figure 2, Table B and Part 4 of this section).

PHYSICAL CHARACTERISTICS

1.05 The overall dimensions of the SA120 (Figure 3) are as follows: Length — 14-1/2 inches; width — 5-1/4 inches; and depth — 3-1/2 inches. Mounting brackets are supplied for mounting to a 19-inch vertical relay rack as provided in Model 35 cabinets. Otherwise, it may be mounted in any position, and since it has no controls or indicators located at the chassis, it does not have to be accessible to the operator.
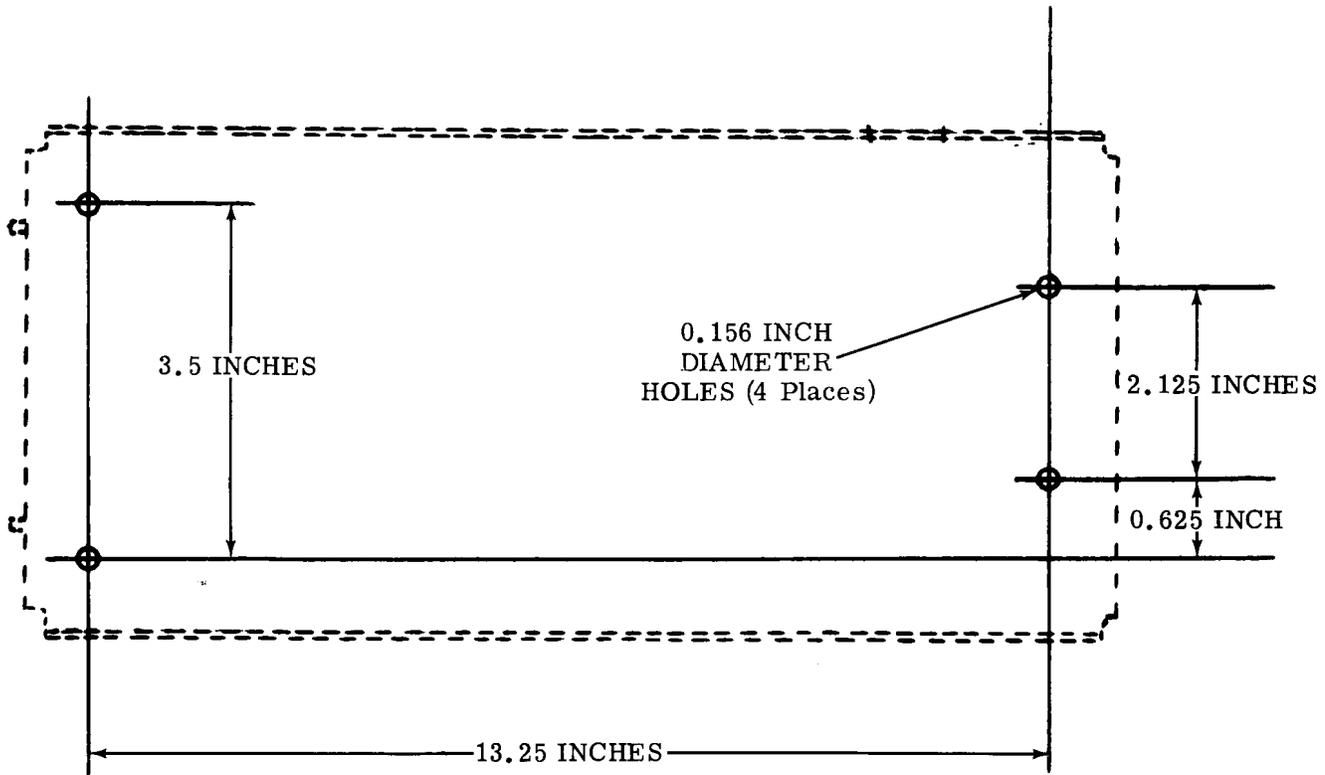


3.5 INCHES

0.156 INCH DIAMETER HOLES (4 Places)

2.125 INCHES

0.625 INCH

13.25 INCHES

Figure 3 - SA120 Base Plate Assembly

## ELECTRICAL CHARACTERISTICS

### A. Input

1.06 The parity detector is connected in series with the receive data lead in the terminal set. For its power requirements, it plugs into any outlet supplying 115 v ac +10%, 50-60 Hz +2%. The maximum current required from this source is 3/8 ampere. The SA120 may be ordered with an electrical interface designed to be compatible with data sets observing the EIA RS-232B standard voltages (polar) such as the 103E, or for terminals employing current/no current (neutral) signaling (101C and 105A data sets).

1.07 The EIA input complies with EIA RS-232B received data polar voltage levels on the receive data lead. These voltages are as follows:

SPACE = +3 to +25 volts

MARK = -3 to -25 volts

The input impedance is 3300 ohms (Figure 4).

### B. Output

1.08 The output (Figure 4) is a serial signal consisting of a start bit, eight information bits, and a stop bit. The information bits are regenerated by the parity detector. The length of each outgoing character is identical to its length as received. The stop signal is not regenerated. Whatever stop bit distortion the receiving terminal can accept from the signal line is unchanged by the insertion of the SA120 parity detector ahead of the terminal.

1.09 The EIA output meets the requirements of EIA RS-232B send data voltage levels (+5 volts minimum when terminated in 3000 ohms). These voltages are as follows:

SPACE = +6 ± 1 volt
                            into 3000 ohms
MARK = -8 ± 2 volt

Source impedances are 56 ohms and 2200 ohms, respectively.

1.10 The current/no current output is a switched transistor stage which is capable of providing a current/no current signal. The maximum voltage which may be applied is -48 volts dc. Maximum current switched (limited externally) is 30 ma.

## 2. DESCRIPTION

2.01 The SA120 parity detector is designed to accept a serial signal consisting of a start bit, eight information bits, and a stop bit of unity length or longer (Figure 5). It is available for receiving 110, 150, and 1050 baud signals (Table B). It may be specially ordered for other baud rates up to 2400 baud. It is factory wired for even parity detection, but may be restrapped for odd parity (Figure 7).

2.02 In normal operation, characters are transferred from the receiving register to a sending register when a space is present in the number 1 position of the receiving register and a mark is present in the number 10 position. When the transfer to the sending register is complete, the character is sent out bit by bit at the rate of the transmitting bit timer. If a character has been received but no valid stop pulse is detected, an out-of-synchronization sequence starts in which the input bit timer continues to operate (runs open) seeking the next bit sequence. Random bit sequences that appear as characters during the resynchronization process will be transferred if they comply with the parity requirement. Those that do not, will be transferred out as a substitute character. The out-of-synchronization period is evidenced in the printed copy by a series of substitute characters interspersed with random characters. Normally, the process will run for five or six characters before synchronization is re-established. A continuously spacing line will cause the bit timer to run open, and the output to remain in the mark-hold state.

## ASSOCIATED EQUIPMENT WIRING DIAGRAMS

2.03 The wiring diagrams and circuit card drawings listed below can be helpful for the following discussion. The diagrams and drawings are packaged with the respective equipment. All wiring diagrams for the SA120, associated bypass, and indicator assemblies may also be ordered as WDP0204.

| NUMBER | *TYPE | EQUIPMENT |
|--------|-------|-----------|
| 4702WD | A | Type 2 tape receiver terminal |
| 4733WD | S | Type 2 tape receiver terminal |
| 5822WD | A | 35 electrical service unit |
| 6000WD | S | 35 ASR set |

ASSOCIATED EQUIPMENT WIRING DIAGRAMS
(Continued)

| NUMBER | *TYPE | EQUIPMENT |
|---|---|---|
| 7881WD | S | 33 RO set |
| 7882WD | S | 33 ASR set |
| 7888WD | A | 33 call control unit |
| 7889WD | A | 33 RO set call control unit UCC-4 |
| 8142WD | A | 35 ASR (LESU 349) |
| 8200WD | S | SA120 parity detector |
| 8201WD | A | SA120 parity detector |
| 8202WD | A | SA120 parity detector current/no current |
| 8226WD | S | 35 ASR set |
| TP320019 | CCD | Partial power supply |
| TP322001 | CCD | Receiving logic |
| TP322002 | CCD | Sending logic |
| WDP0204 | | Complete wiring diagram package for SA120 |

*A = Actual wiring diagram; S = Schematic wiring
diagram; CCD = Circuit Card Drawing.

RECEIVING LOGIC

2.04    This circuit (TP322001) consists of a
        receiving shift register, a bit timer, and
a parity check flip-flop. The receiving shift
register is capable of accepting serial signals.
The bit timer provides the receive timing, while
the parity check flip-flop provides the even parity
check on an incoming character. With factory
strapping (even parity), odd parity counts indi-
cate an errored character. Operation on odd
parity, to indicate an error on even parity, can
be provided by a strap option, at time of instal-
lation.

2.05    When the storing of a received character
        in the receiving shift register is com-
pleted, either an even parity character detect
signal, or an odd parity character detect signal
will be present at the card connector terminal.
When strapped for even parity (factory strap-

ping), the even parity character detect signal is
used to effect a parallel transfer of the stored
character bits to the sending shift register,
circuit card (TP322002). In case of parity error,
the odd parity character detect signal is used to
insert preprogrammed character bits in parallel
into the sending shift register to replace the
stored errored character. The stored errored
character will be erased prior to the beginning
of the next character cycle.

Input Amplifier

2.06    The basic input amplifier (8200WD, Sheet
        1) common to all SA120s (Figure 3) oper-
ates as an interface capable of accepting polar
EIA inputs only. Its output is +6 volts for mark,
and 0 volts for space.

Receiving Bit Timer Control Gate (RBTC) -
(8200WD, Sheet 2)

2.07    Part of MLD2 and part of MLB1 consti-
        tute the receiving bit timer control gate
that controls the bit timer. The normal output
on pin 11 of MLB1 is +6 volts disabling the bit
timer. When a spacing signal (start) appears on
the signal line, a negative going voltage tran-
sition will be applied to pin 10 of MLD2. The
output of this gate will then go to 0 volts enabling
the bit timer. The bit timer is held on until an
incoming character is fully stored in the re-
ceiving shift register with its start bit in flip-
flop RST (Receive Start), and its stop bit in
flip-flop RSP (Receive Stop).

Character Control Flip-Flop (CCFF)

2.08    The 0 output on pin 9 of CCFF (8200WD,
        Sheet 2) is normally +6 volts (marking,
or 0 state). It will go to 0 volts as soon as the
bit timer delivers its first pulse. The first pulse
occurs in the center of the start signal of the
incoming character to the receiving shift regis-
ter. It will remain at 0 volts, holding the bit
timer on, independent of line signals until the
start signal of an incoming character is shifted
into flip-flop RST.

Receiving Bit Timer (RBT)

2.09    The receiving bit timer (8200WD, Sheet
        2) is the element that provides the internal
receive timing. Its output is a +5 volts pulse
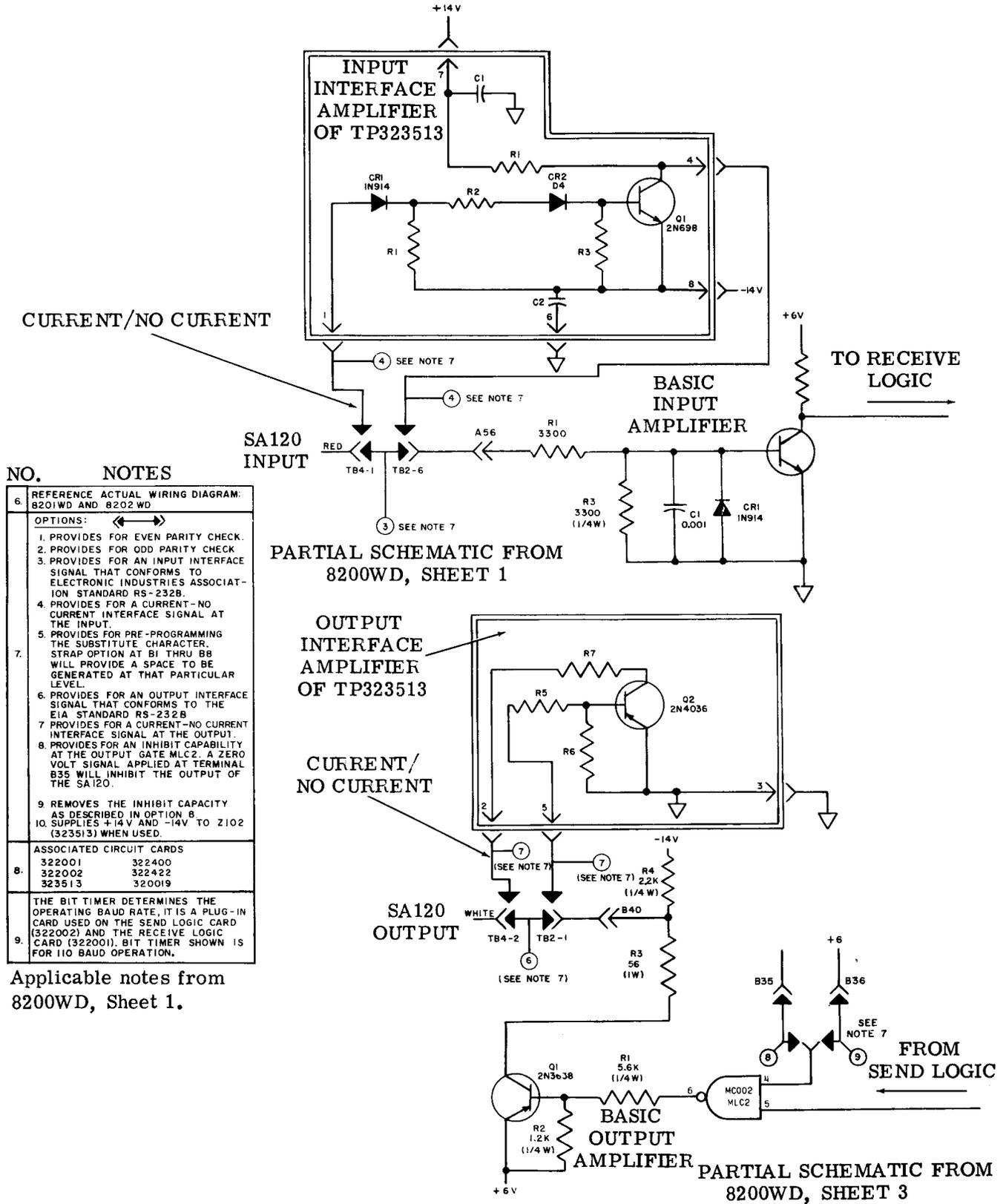which occurs at twice the desired bit rate.

+14V

INPUT
INTERFACE
AMPLIFIER
OF TP323513

C1

R1

CR1
1N914

R2

CR2
D4

Q1
2N698

4

R1

R3

8

C2

6

-14V

CURRENT/NO CURRENT

(4) SEE NOTE 7

(4) SEE NOTE 7

+6V

TO RECEIVE
LOGIC

BASIC
INPUT
AMPLIFIER

SA120
INPUT

RED

TB4-1

TB2-6

A56

R1
3300

R3
3300
(1/4W)

C1
0.001

CR1
1N914

(3) SEE NOTE 7

PARTIAL SCHEMATIC FROM
8200WD, SHEET 1

## NO.    NOTES

| 6. | REFERENCE ACTUAL WIRING DIAGRAM: 8201WD AND 8202WD |
|----|---|
|    | OPTIONS: ◁——▷ |
| 7. | 1. PROVIDES FOR EVEN PARITY CHECK. |
|    | 2. PROVIDES FOR ODD PARITY CHECK |
|    | 3. PROVIDES FOR AN INPUT INTERFACE SIGNAL THAT CONFORMS TO ELECTRONIC INDUSTRIES ASSOCIATION STANDARD RS-232B. |
|    | 4. PROVIDES FOR A CURRENT-NO CURRENT INTERFACE SIGNAL AT THE INPUT. |
|    | 5. PROVIDES FOR PRE-PROGRAMMING THE SUBSTITUTE CHARACTER. STRAP OPTION AT B1 THRU B8 WILL PROVIDE A SPACE TO BE GENERATED AT THAT PARTICULAR LEVEL. |
|    | 6. PROVIDES FOR AN OUTPUT INTERFACE SIGNAL THAT CONFORMS TO THE EIA STANDARD RS-232B. |
|    | 7. PROVIDES FOR A CURRENT-NO CURRENT INTERFACE SIGNAL AT THE OUTPUT. |
|    | 8. PROVIDES FOR AN INHIBIT CAPABILITY AT THE OUTPUT GATE MLC2. A ZERO VOLT SIGNAL APPLIED AT TERMINAL B35 WILL INHIBIT THE OUTPUT OF THE SA120. |
|    | 9. REMOVES THE INHIBIT CAPACITY AS DESCRIBED IN OPTION 8. |
|    | 10. SUPPLIES +14V AND -14V TO Z102 (323513) WHEN USED. |
| 8. | ASSOCIATED CIRCUIT CARDS |
|    | 322001   322400 |
|    | 322002   322422 |
|    | 323513   320019 |
| 9. | THE BIT TIMER DETERMINES THE OPERATING BAUD RATE, IT IS A PLUG-IN CARD USED ON THE SEND LOGIC CARD (322002) AND THE RECEIVE LOGIC CARD (322001). BIT TIMER SHOWN IS FOR 110 BAUD OPERATION. |

Applicable notes from
8200WD, Sheet 1.

OUTPUT
INTERFACE
AMPLIFIER
OF TP323513

R7

R5

Q2
2N4036

R6

2

5

3

CURRENT/
NO CURRENT

(7)
(SEE NOTE 7)

(7)
(SEE NOTE 7)

-14V

R4
22K
(1/4 W)

SA120
OUTPUT

WHITE

TB4-2

TB2-1

B40

(6)
(SEE NOTE 7)

R3
56
(1W)

+6

B35

B36

SEE
NOTE 7

8

9

FROM
SEND LOGIC

Q1
2N3638

R1
5.6K
(1/4W)

6

MC002
MLC2

5

R2
1.2K
(1/4W)

BASIC
OUTPUT
AMPLIFIER

+6V

PARTIAL SCHEMATIC FROM
8200WD, SHEET 3

Figure 4 - Input and Output Amplifiers and Interface Amplifiers
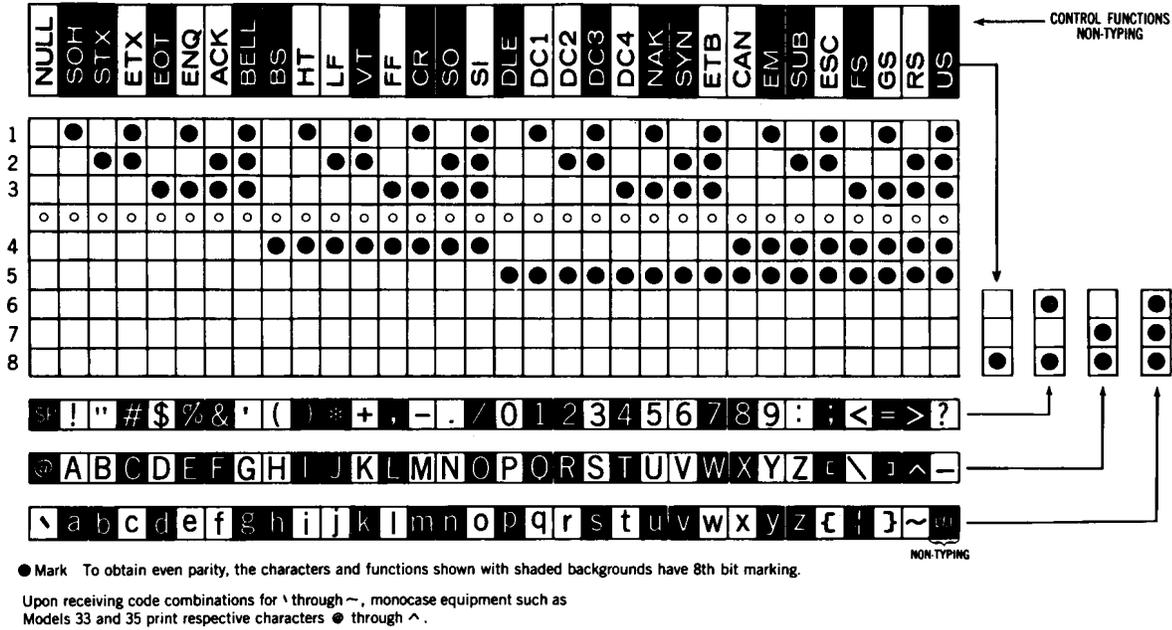for Current/No Current Signals

Figure 5 - Example of Eight-Level Code

**Receiving Binary Counter Flip-Flop (RBCFF)**

2.10    The binary counter (8200WD, Sheet 2) is a triggered flip-flop initially set in the marking state. Its 0 output on pin 9 changes state at one-half the frequency on its input. It is a +6 volts for one-half the time, and 0 volts for the other half.

**Inverter Receiving Clock Pulse Gate (RCP)**

2.11    Whenever the output of the receiving binary counter and the bit timer are both positive, the output of this gate (8200WD, Sheet 2) will be 0 volts.

**Receiving Clock Pulse Gate (RCP)**

2.12    The output voltage on pins 6 and 8 of this gate (8200WD, Sheet 2) provides the clock pulse necessary for shifting the register.

**Parity Check Flip-Flop (PCFF)**

2.13    The normal 1 output on pin 6 of this flip-flop (8200WD, Sheet 1) is set at 0 volts. It is wired so that its output changes state whenever a spacing bit in an incoming character is sensed. The clock pulse applied at pin 2 of this flip-flop is such that it arrives 1/2 bit after the clock pulse being applied to the receiving shift register.

**Even Parity Character Detect Gate (EPCD)**

2.14    When the output of this gate (8200WD, Sheet 1) goes to 0 volts, it indicates that an incoming character with even parity has been received and stored in the receiving shift register. The character bits can be transferred in parallel into the sending shift register.

**Inverted Even Parity Character Detect Gate (EPCD)**

2.15    This gate inverts the output of EPCD (8200WD, Sheet 1) (2.14). Its output may be used as a contact signal for an external circuit. When the output goes to +6 volts, it indicates that an incoming character with non-violated parity in the receiving shift register is available (even parity check operation). For odd parity check operation, a +6 volts output from this gate will indicate that this same incoming character has violated parity and is available in the receiving shift register.

**Odd Parity Character Detect Gate (OPCD)**

2.16    When the output of this gate (8200WD, Sheet 1) goes to 0 volts, it indicates that an incoming character containing odd parity has been received and stored in the receiving shift register.

Reset Condition Gate (RC)

2.17    The normal output of this gate (8200WD, Sheet 1) is 0 volts. A positive going voltage transition output indicates that an incoming character (with either even or odd parity) has been received and stored in the receiving shift register. The output will be held at +6 volts until either the stored character with no parity error is transferred to the sending shift register, or a preprogrammed character is inserted into the shift register as a replacement for an errored character.

Receiving Shift Register (RSR)

2.18    The receiving shift register (8200WD, Sheet 2) consists of clocked flip-flop elements labeled RST (Receive Start), RSP (Receive Stop) and eight data levels, R1 through R8. All the flip-flop elements are initially set in the marking state.

2.19    The receiving shift register performs the function of accepting and storing an eight-level serial signal, and paralleling the serial input signals. The elements are cascaded such that upon receipt of a narrow positive pulse (clock pulse) at pin 2 of each flip-flop, the state of one flip-flop will be shifted into the next flip-flop. The first shift pulse will occur in the approximate center of the start bit (space) of an incoming character. This pulse will cause the start bit to be shifted into the flip-flop element RSP. Since all flip-flop elements are in the marking state (except the RSP), the start bit (space) in RSP must be shifted down the entire register before the bit timer is released via the character control flip-flop (CCFF). This requires nine more shift pulses. After an incoming character is fully stored in the register, a +6 volts at pin 6 of any flip-flop element indicates a space set in that position.

SENDING LOGIC

2.20    The sending logic circuit card (TP322002) performs the function of accepting parallel input signals from the receiving shift register, or inserting a preprogrammed character into the sending shift register by means of a strap option if the received character is found with parity error. The transferred or preprogrammed character will then be shifted out serially to an external recording device via an output amplifier.

2.21    A bit timer is used to provide the sending timing. When a transferred or preprogrammed character is received in the sending shift register, a control signal will be provided to reset all flip-flop elements in the receiving logic to their initial marking states.

Correct Character Transfer Gate (CCT)

2.22    The normal output of this gate (8200WD, Sheet 3) is 0 volts. The output will go to +6 volts when an incoming character with no parity error is received and stored in the receiving shift register. It is used as a control signal to transfer the stored character bits in parallel, into the sending shift register. The output of this gate will remain at +6 volts until the flip-flop elements (RST and PCFF in the receiving logic circuit) are reset to their initial marking states.

Preprogrammed Character Insert Gate (PCI)

2.23    The normal output of this gate (8200WD, Sheet 3) is 0 volts. A positive going voltage transition from this output indicates that the stored character in the receiving shift register contains parity error. This positive voltage is used as a control signal for the insertion of preprogrammed parallel character bits into the sending shift register. The output will return to 0 volts as soon as the flip-flop elements RST and PCFF, in the receiving logic circuit, are reset to their initial marking states.

Sending Shift Register (SSR)

2.24    The sending shift register (8200WD, Sheet 3) consists of nine clocked flip-flop elements labeled SST (start) and eight data levels S1 through S8. All are initially set in marking states. Bit information on the stored character in the receiving shift register, or on a preprogrammed character, will be transferred or inserted respectively into the sending shift register on a parallel basis. When pin 6 of any flip-flop is +6 volts, a space is set in that position. The elements are cascaded such that a narrow positive pulse (clock pulse) applied to pin 2 of each flip-flop element will result in the shifting of the state of one flip-flop element into the next flip-flop element. The sending shift register, therefore, performs the function of serializing the parallel input signals.

Sending Bit Timer Control Gate (SBTC)

2.25    The normal output of this gate (8200WD, Sheet 4) is +6 volts with all flip-flop elements in the register marking. A 0 volt output from this gate indicates the presence of at least one space in the sending shift register enabling the bit timer.

Sending Bit Timer (SBT)

2.26    The sending bit timer (8200WD, Sheet 4) is the element that provides the send timing. Its output is a +5 volts pulse which occurs at twice the desired bit rate.

Sending Binary Counter Flip-Flop (SBCFF)

2.27    This triggered flip-flop (8200WD, Sheet 4) is initially set at the 1 state (spacing). Its 0 output (pin 9) changes states at one-half the frequency of its input. It is a +6 volts for one-half the time, and 0 volts for the other half.

Inverted Sending Clock Pulse (SCP)

2.28    Whenever the output of the sending binary counter and the bit timer are both positive, the output of this gate (8200WD, Sheet 4) will be 0 volts.

Sending Clock Pulse (SCP)

2.29    The output of this gate (8200WD, Sheet 4) provides the clock pulse necessary for shifting the register.

Reset Gate (RS)

2.30    The normal output of this gate (8200WD, Sheet 4) is +6 volts. A negative going voltage transition output from this gate indicates that a character, either transferred or preprogrammed, has been set into the sending shift register. This ground voltage will then reset all flip-flop elements in the receiving logic circuit to their initial marking states.

Output Amplifier

2.31    This amplifier (8200WD, Sheet 3) accepts 0 to +6 volt signals from the sending shift register and converts them into suitable bi-polar voltage signals for use by an external recording device. Its output is +5 volts to +25 volts for space, and -5 volts to -25 volts for mark.

3.    PRINCIPLES OF OPERATION

GENERAL

3.01    Integrated circuits used in the SA120 parity detector are to perform elementary logic operations. The signals in logic circuits can be represented by either of two voltage levels or by pulses. In the level representation, the two voltages are designated as positive (+6 volts) and negative (0 volts). Pulse representation consists of a pulse-no-pulse combination and requires a time interval between adjacent pulses.

3.02    The positive logic is used throughout the circuitry design. A positive signal is identified as "1" (space), and the negative signal as "0" (mark). A flip-flop element is said to be in a space state when its 1 output (pin 6) is +6 volts. A mark in a flip-flop element is represented by a +6 volts at its 0 output (pin 9).

OPERATING SEQUENCE

3.03    Refer to the timing diagram (Figure 6) and schematic wiring diagram 8200WD to aid in the following operating sequence discussion.

3.04    When the ac power to the SA120 parity detector is turned on, a ground dc signal is applied to the SD input (pin 10) of flip-flop elements RST, CCFF, and R1, setting them in the spacing states. A random character, which is determined by the random states of the flip-flop elements in the receiving register, will be transferred into the send shift register (if it complies with the parity requirement) and subsequently shifted out to an external recording device. If the random character does not comply with the parity requirement, it will then be transferred out as a preprogrammed substitute character. All flip-flop elements in the receiving logic circuit (circuit card TP322001) are now reset to marking, and the parity failure detector is ready for operation.

3.05    When a character is about to be detected by the SA120 parity detector, its spacing signal (start), appearing on the signal line, supplies the input (pin 10) of RBTC with ground. The output of RBTC, in turn, supplies the input of RBT with ground enabling the receiving bit timer.

3.06    The RCP gate will deliver its first shift pulse to the receiving shift register and CCFF in the approximate center of the start bit. This pulse causes the start bit to be shifted into RSP, and a mark from R1 to be shifted into CCFF as a space. The 0 output (pin 9) of CCFF will then supply ground input to RBTC (pin 11), holding RBT on independent of line signals. The shift pulse will continue at approximately the center of each signal bit until the start bit originally in RSP is shifted to RST as a space, and to CCFF as a mark. This requires nine more shift pulses, the last of which occurs in the approximate center of the tenth bit (first bit of the stop pulse).
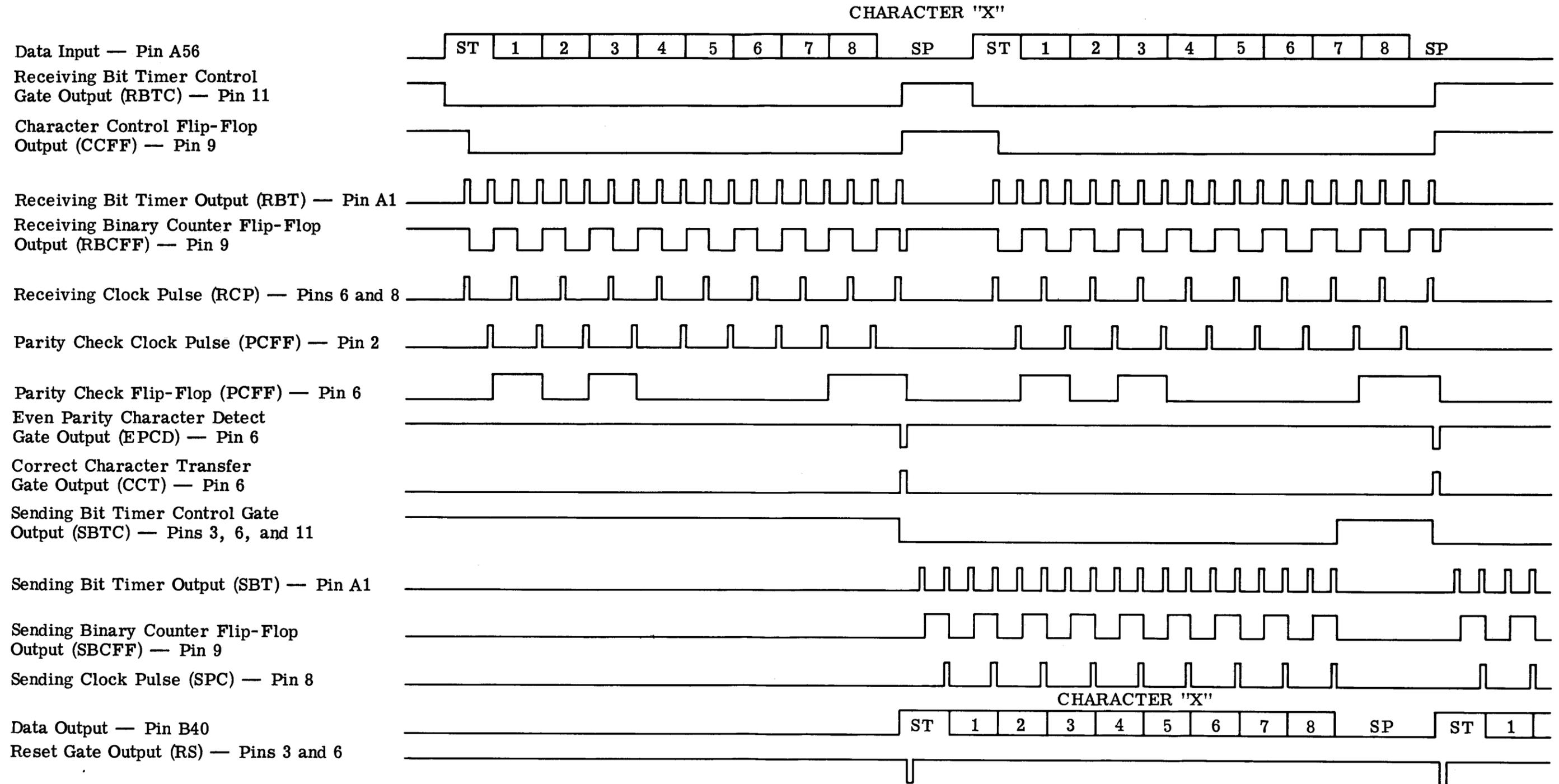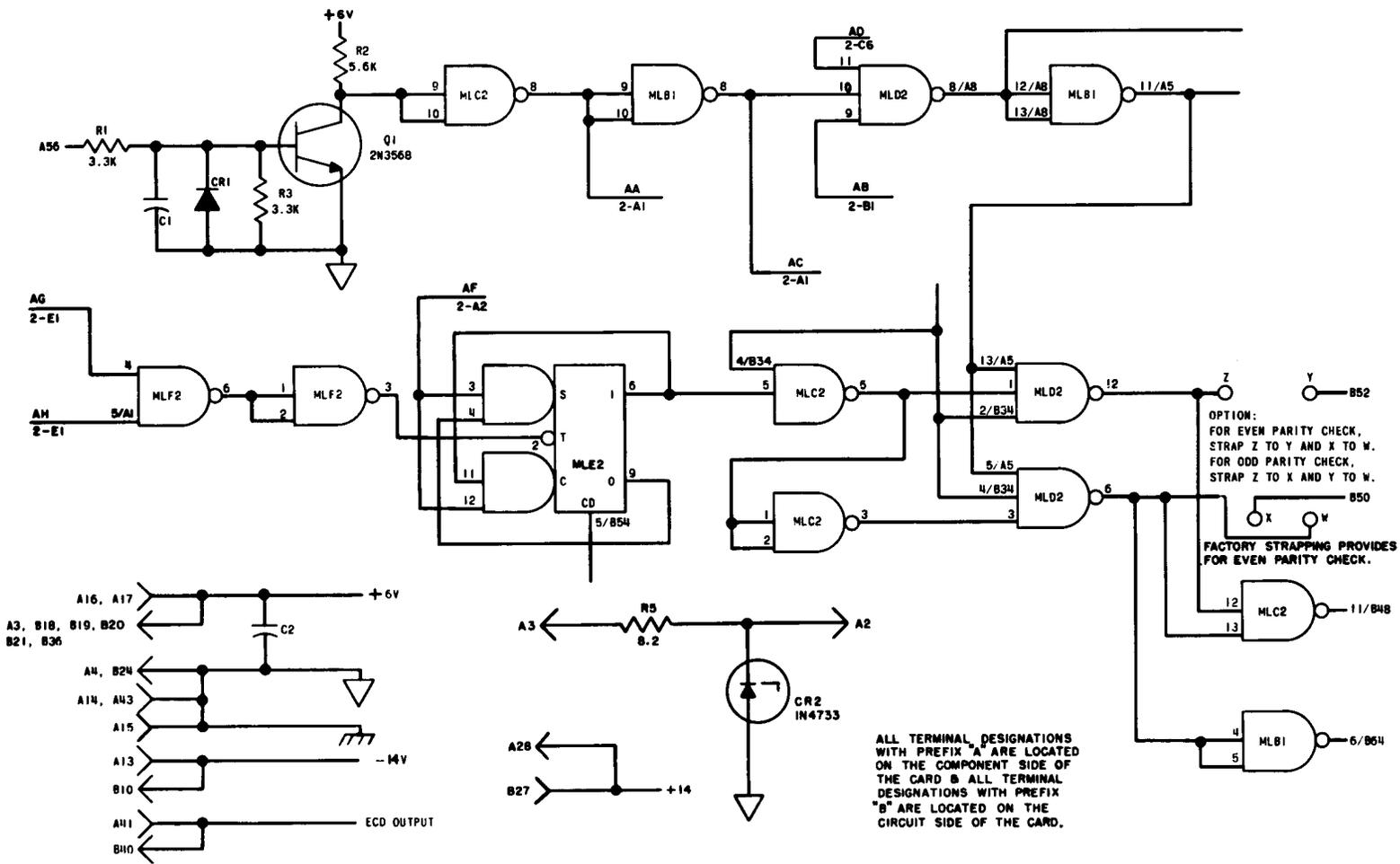
CHARACTER "X"

| Data Input — Pin A56 | ST | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | SP | ST | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | SP |

Receiving Bit Timer Control
Gate Output (RBTC) — Pin 11

Character Control Flip-Flop
Output (CCFF) — Pin 9

Receiving Bit Timer Output (RBT) — Pin A1

Receiving Binary Counter Flip-Flop
Output (RBCFF) — Pin 9

Receiving Clock Pulse (RCP) — Pins 6 and 8

Parity Check Clock Pulse (PCFF) — Pin 2

Parity Check Flip-Flop (PCFF) — Pin 6

Even Parity Character Detect
Gate Output (EPCD) — Pin 6

Correct Character Transfer
Gate Output (CCT) — Pin 6

Sending Bit Timer Control Gate
Output (SBTC) — Pins 3, 6, and 11

Sending Bit Timer Output (SBT) — Pin A1

Sending Binary Counter Flip-Flop
Output (SBCFF) — Pin 9

Sending Clock Pulse (SPC) — Pin 8

CHARACTER "X"

| Data Output — Pin B40 | ST | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | SP | ST | 1 |

Reset Gate Output (RS) — Pins 3 and 6

Figure 6 - Timing Diagram for
SA120 Parity Detector

Note: See Sheet 2 drawing TP322001 for complete schematic wiring diagram.

OPTION:
FOR EVEN PARITY CHECK,
STRAP Z TO Y AND X TO W.
FOR ODD PARITY CHECK,
STRAP Z TO X AND Y TO W.

FACTORY STRAPPING PROVIDES
FOR EVEN PARITY CHECK.

ALL TERMINAL DESIGNATIONS
WITH PREFIX "A" ARE LOCATED
ON THE COMPONENT SIDE OF
THE CARD & ALL TERMINAL
DESIGNATIONS WITH PREFIX
"B" ARE LOCATED ON THE
CIRCUIT SIDE OF THE CARD.

3.07    With the signal line marking and the 0
        output (pin 9) of CCFF and RSP at +6
volts, the output of RBTC will become +6 volts
disabling the receiving bit timer. At this time,
the start bit of the received character is stored
in RST with the stop bit in RSP, and bits 1 through
8 in R1 through R8 respectively. The 1 output
(pin 6) of each of these flip-flop elements (except
RSP) in the receiving shift register now present
a parallel output.

3.08    The parity check flip-flop, initially set in
        the marking state, is wired so that when-
ever a spacing signal in the incoming character
is shifted into the receiving shift register, the
clock pulse applied at pin 2 of PCFF will cause
its output to change state. This clock pulse is
applied 1/2 bit later than the clock pulse used to
shift the character into the receiving shift regis-
ter. At the end of the character cycle, a +6 volts
at its 1 output indicates the presence of a charac-
ter in the receiving shift register with even
parity; a ground output indicates odd parity.

3.09    Both OPCD and EPCD gates are generally
        under the control of the RST element of
the receiving shift register and the RBTC gate.
This inhibits each of the parity detect gates during
the time that the incoming character is being
shifted into the receiving shift register. When
the output of gate EPCD goes to 0 volts and the
output of gate OPCD remains at +6 volts, it indi-
cates that the stored character contains even
parity. If the stored character has odd parity,
the output of EPCD will remain at +6 volts and
the output of OPCD will go to 0 volts.

3.10    The strap option of the bottom circuit
        card (TP322001) for operation on even
or odd parity checking is shown in Figures 7 and
8. Assuming that the parity detector is wired
for even parity operation and that an incoming
character with even parity has been received
and stored in the receiving shift register, the
output of gate CCT (Correct Character Transfer)
will be connected to a set of nine bit transfer
gates. Each gate, upon receipt of a positive
going voltage input from CCT, will transfer a
space bit in flip-flop element RSR to its corre-
sponding flip-flop element in SSR. Meanwhile,
the output of PCI (Programmed Character Insert)
gate remains at ground inhibiting the insertion
of a preprogrammed character into the SSR.

3.11    The 0 output (pin 9) of each flip-flop ele-
        ment in the sending shift register is con-
nected to the SBTC gate. The normal output of

gate SBTC is +6 volts, but it will go to ground
when at least one flip-flop element in the sending
shift register is in the spacing state. The ground
output from SBTC will enable the sending bit
timer.

**FOR EVEN PARITY CHECK**
**(As Strapped at Factory)**

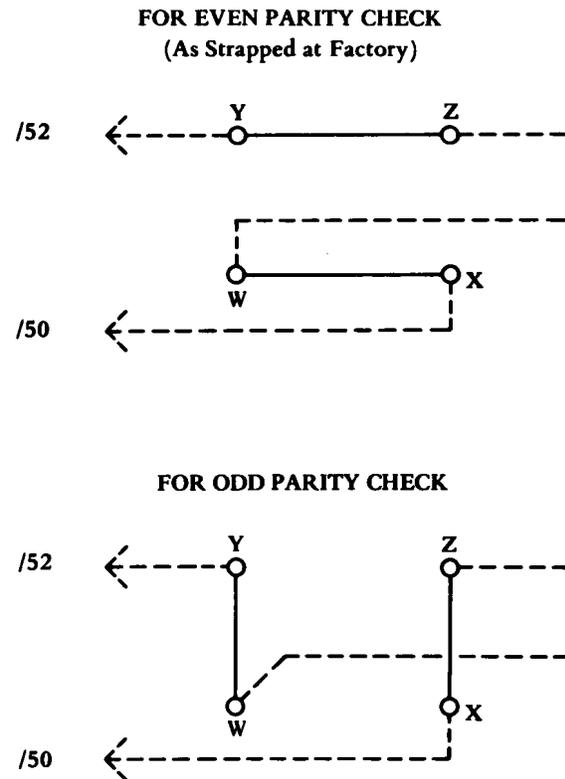

**FOR ODD PARITY CHECK**



Figure 8 - Odd and Even Parity
Strap Options

3.12    There are two inputs to the RS gate; one
        is from the output of the reset condition
gate, now being held at +6 volts, and the other is
the inverted signal of the output of SBTC, also
at +6 volts because of the presence of a trans-
ferred character in the sending shift register.
The output of RS will supply a ground signal to
the CD input of each flip-flop element in the re-
ceiving logic circuit and will return to its normal
+6 volts level after clearing the flip-flops.

3.13    The SCP (Send Clock Pulse) will deliver
        its first shift pulse to the sending shift
register one bit length after the SBT (Send Bit
Timer) is enabled. These pulses will continue
until the entire character is serially shifted out
of the register to an external recording device.

3.14    Assuming now that an odd parity charac-
ter has been received and stored in the
receiving shift register, and that the parity de-
tector is wired for even parity operation, the
character is recognized by the unit as being
errored.  In this case, the CCT gate output will
remain at ground inhibiting the character to be
transferred.  The output of PCI, however, will
go to +6 volts which, in turn, is applied to a set
of nine bit insert gates.

3.15    Each spacing bit of the preprogrammed
character will be set into its corre-
sponding flip-flop element, in the sending shift
register, by a strap option.  Examples of the
strapping and bit configuration of prepro-
grammed characters are shown on Figure 9.
Sequential operation will then be the same as
described earlier for a received character with
even parity.

POWER SUPPLY

3.16    The SA120 parity detector contains an ac
to dc multi-voltage power supply (Figure
10).  It supplies the following dc voltages to the
logic circuits in the parity detector and to the
various options available.

+6 v dc (nominal) regulated
-14 v dc (nominal) unregulated
+14 v dc (nominal) unregulated

Output voltages for the specified range of temper-
ature, ac input voltage, and line frequency are
as follows:  All output voltages use the same
terminal for common return.  The ac input and
the +6 volts dc output must be fused at 3/8 and
1-1/2 amperes respectively, so that the maxi-
mum rated currents are not exceeded.  See Table
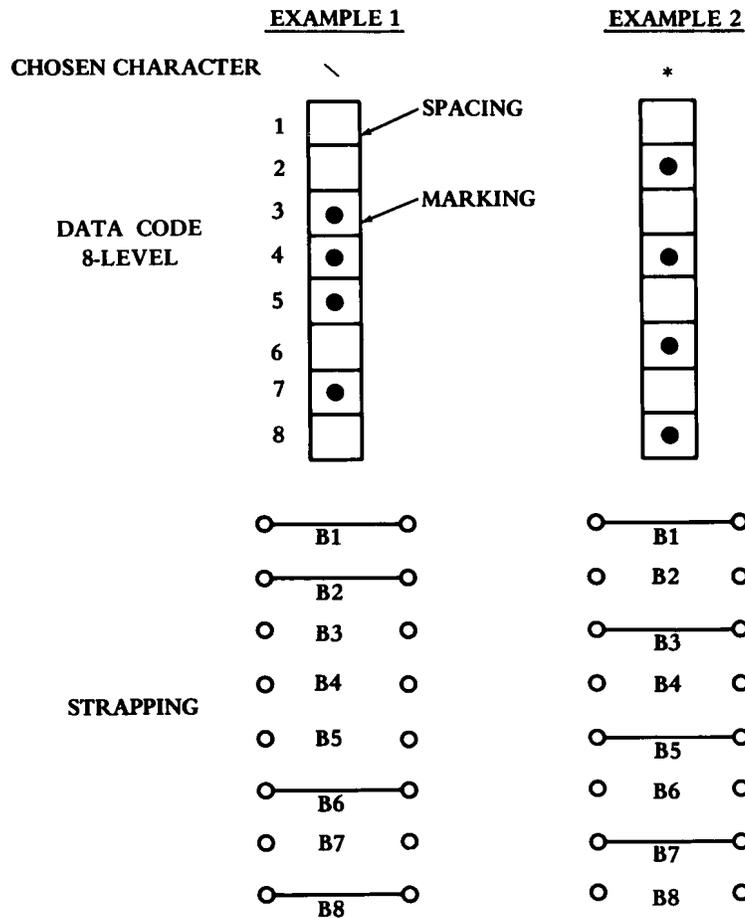A for power supply output voltages.



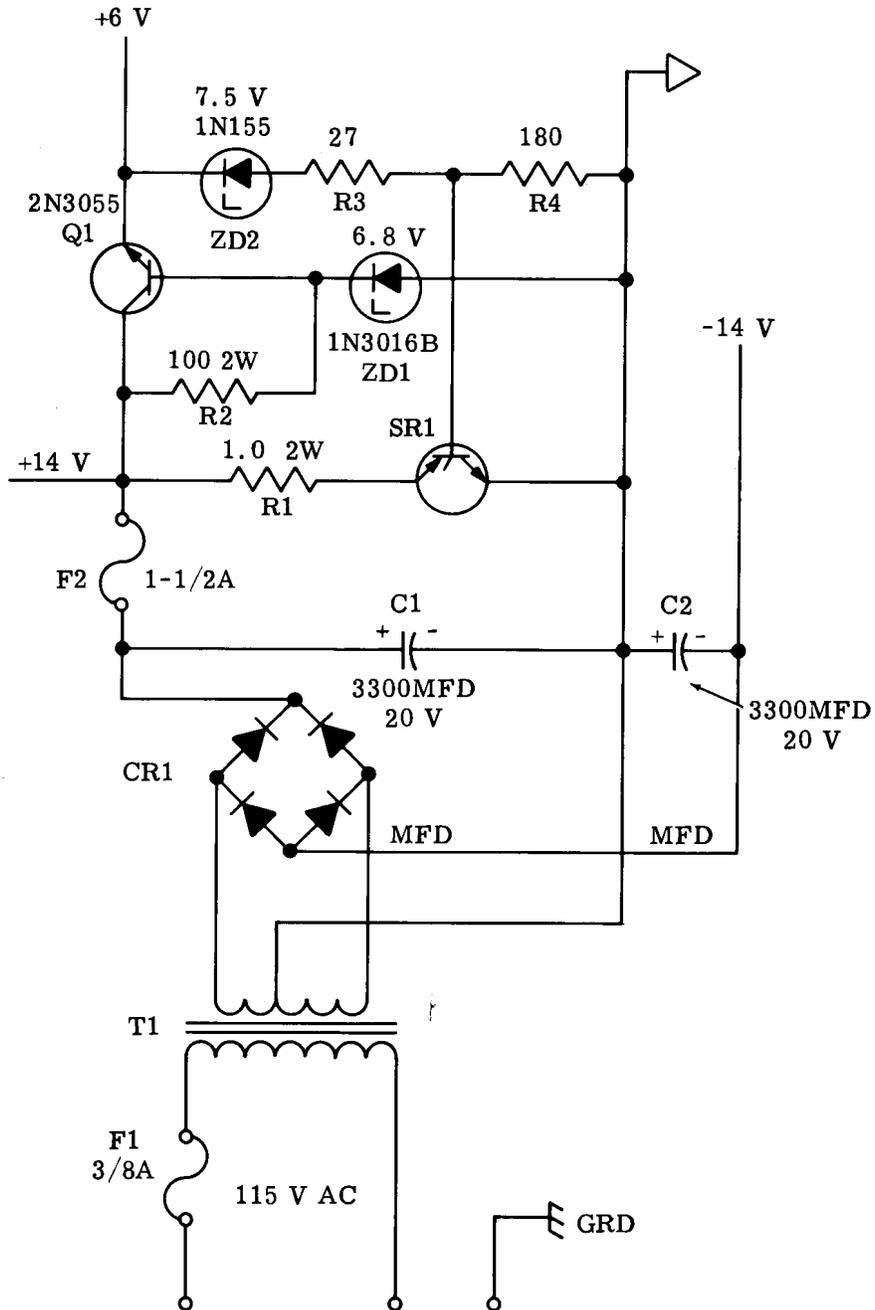Figure 9 - Typical Examples of Preprogrammed Substitute Character

Figure 10 - Power Supply Circuit Diagram

TABLE A
POWER SUPPLY OUTPUT VOLTAGES

| NOMINAL VOLTAGE VDC | VOLTAGE LIMITS VDC | | MAX LOAD CURRENT | MAX RIPPLE POINT TO POINT |
|---|---|---|---|---|
| | MIN | MAX | | |
| +6 v dc | +5.1 | +6.95 | 1.0 amp | 0.100 v pp |
| +14 v dc | +8.9 | +16.0 | 50 ma | 1.0 v pp |
| -14 v dc | -16.8 | -11.0 | 200 ma | 1.5 v pp |

3.17    The power supply consists of a step-down transformer, a full-wave bridge rectifier, a series regulating power transistor, zener diode voltage references, a silicon controlled rectifier, filter capacitors, associated resistor components, hardware, and terminals. The primary winding of T1 is connected to the ac power line cord, the hot lead through fuse F1, and the protective ground lead connected to the chassis. The secondary winding of T1 supplies the ac input voltages to a full-wave bridge rectifier (CR1), with its center tap lead connected to the common ground.

3.18    The rectified outputs are filtered by capacitor C1 for the +14 v dc and +6 v dc section, and capacitor C2 for the -14 v dc section. The main elements of the regulating circuitry for the +6 v dc section are the series regulating power transistor Q1 and the zener diode reference ZD1. The voltage on ZD1 is applied to the base of Q1. The output voltage from the emitter of Q1 to the common ground is maintained at a value of the voltage on ZD1 minus the base to emitter voltage drop on Q1. Resistor R2 provides the biasing current for Q1, and the current through ZD1 enables it to develop the reference voltage.

3.19    The ZD2, R3, R4, R1, and SCR1 constitute an overvoltage protective circuit in the +6 v dc section. Under condition of component failure (either Q1 short-circuited, or ZD1 open-circuited), the +6 v dc output will tend to rise to a value of the dc voltage at the plus (+) side of the CR1. However, when the output voltage reaches the ZD2 reference level (+7.5 volts), the ZD2 will conduct. The gate electrode of SCR1, which in its normal state will block an applied voltage in either direction, is now applied with a triggering voltage provided by R3 and R4. Therefore, excessive current will flow through SCR1 and R1 blowing fuse F2 preventing damage to any micrologic packages in the parity detector.

3.20    The +6 v dc supplied to each of the two bit timers located on the sending and receiving logic cards is reduced to a nominal +5.1 v dc by an associated resistor-zener diode network. These two networks are shown on 8200WD, Sheets 2 and 4.

4.    VARIABLE FEATURES

OPERABLE COMBINATIONS AND CODE ASSIGNMENTS

4.01    Table B lists the operating combinations of the SA120 with variable features and the two letter suffix code for each combination. This two letter code and table may be used for ordering new units or to understand and maintain units already in service. For a more detailed breakdown, refer to 8200WD, Sheets 5 and 6.
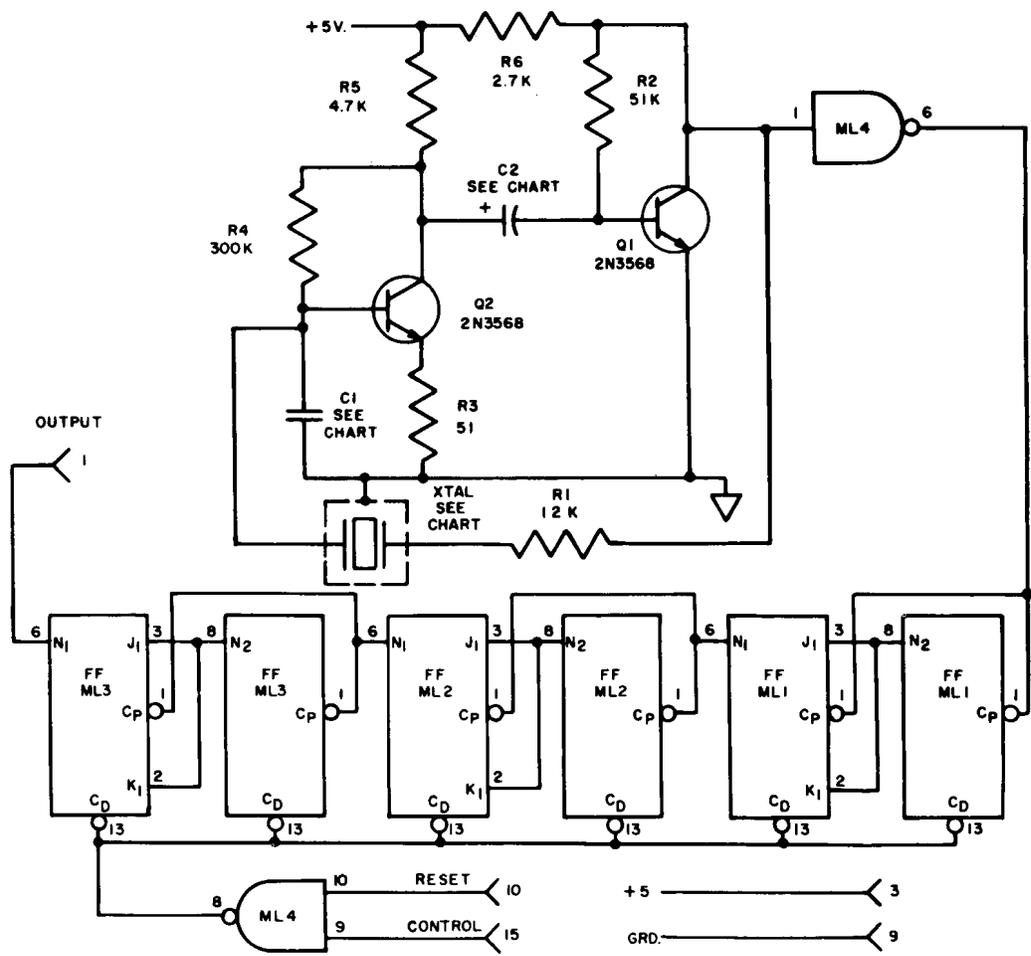
OPERATING SPEEDS AND BIT TIMERS

4.02    The SA120 parity detector is equipped with two identical bit timers which provide the receiving and sending timing. The operating speed can be varied by changing the plug-in bit timers. The bit timers that are available for the various speeds and unit codes are listed below and shown on the schematic wiring diagram of Figure 11.

| BAUD | WORDS PER MINUTE | UNIT CODE | ASSEMBLY NUMBER |
|---|---|---|---|
| 110 | 100 | 11 | TP322204 |
| 150 | 150 | 10 | TP322205 |
| 1050 | 1050 | 10 | TP322206 |

4.03    The bit timer consists of a multivibrator type, free running crystal oscillator. The output of the oscillator is supplied to power amplifier ML4 which is used to provide the input drive for ML1. ML1 is the first of three dual J-K flip-flops which are connected to provide a

| ELECTRICAL CHARACTERISTICS | | | | CURRENT |
|---|---|---|---|---|
| RESET PIN 10 CONTROL PIN 15 | "1" | 2.00 V MIN | $V_{CC}$ V MAX | |
| | "0" | 0 V. MIN. | 0 5 V.MAX. | 1.4 MA MAX |
| OUTPUT PIN 1 | "1" | 3.2 V.MIN. | $V_{CC}$ V.MAX. | |
| | "0" | 0 V. MIN. | 0 5 V.MAX. | 15 MA MAX |
| POWER SUPPLY | 100 MA MAX. | 4.75 V. MIN. | 6 6 V. MAX. | |



| ASSEMBLY NO | MC NUMBER | CRYSTAL PART NO. | WPM | UNIT CODE | OUTPUT FREQUENCY | CRYSTAL FREQUENCY | CAPACITOR C1 PART NO. | VALUE | CAPACITOR C2 PART NO | VALUE |
|---|---|---|---|---|---|---|---|---|---|---|
| 322204 | MC204 | 327275 | 100 | 11 | 220 HZ | 14 08 KHZ | 315976 | 470 PF | 310926 | .15 MFD. |
| 322205 | MC205 | 327276 | 150 | 10 | 300 HZ | 19.20 KHZ | 315976 | 470 PF | 310926 | 15 MFD. |
| 322206 | MC206 | 327277 | 1050 | 10 | 2100 HZ | 134.4 KHZ | 321518 | 68 PF | 327623 | 150 PF |
| | | | | | | | | | | |
| | | | | | | | | | | |

Figure 11 - SA120 Bit Timers for 100, 150, and 1050 Words Per Minute

## TABLE B
## SA120 CODE ASSIGNMENTS

| CONSISTS OF: | AA | AB | AC | AD | AE | AF | AG | AH | AJ | AK | AL | AM | AN | AP | AQ | AR | AS | BA | BB | BC | BD | BE | BF | CA | CB | CC | CD | CE | CF | EA | EB | EC | ED | EE | FA |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| No Bit Timers | X | | | | X | | | | X | | | | X | | | | | | | | | | | | | | | | | | | | | | |
| 110 Baud Bit Timer | | 2 | | | | 2 | | | | 2 | | | | 2 | | | | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | | | | | | |
| 150 Baud Bit Timer | | | 2 | | | | 2 | | | | 2 | | | | 2 | | | | | | | | | | | | | | | | | | | | |
| 1050 Baud Bit Timer | | | | 2 | | | | | | | | 2 | | | | | 2 | | | | | | | | | | | | | 2 | 2 | 2 | 2 | 2 | 2 |
| Current/No Current (Data Lead) | | | | | X | X | X | | | | | | X | X | X | | | | X | | X | | X | | X | | X | | X | | | | | | |
| EIA (Data Lead) (TP323517 Cable) | X | X | X | X | | | | | X | X | X | X | | | | | X | X | | X | | X | | X | | X | | X | | X | X | X | X | X | X |
| Used on Model 33 Terminal | X | X | | X | X | | | | X | X | | X | X | | | | | X | X | X | X | X | X | | | | | | | | | | | | |
| Used on Model 35 Terminal | X | X | | X | X | | | | X | X | | X | X | | | | | | | | | | | X | X | X | X | X | X | | | | | | |
| Used on Type 2 Terminal | X | | X | | | | | | X | | X | | | | | | X | | | | | | | | | | | | | X | X | X | X | X | X |
| TP327631 Bypass Switch | | | | | | | | | | | | | | | | | | X | X | X | X | | | | | | | | | | | | | | |
| TP327632 Indicator | | | | | | | | | | | | | | | | | | | | | | X | X | | | | | | | | | | | | |
| TP327633 Bypass Switch | | | | | | | | | | | | | | | | | | | | | | | | X | X | X | X | | | | | | | | |
| TP327634 Indicator | | | | | | | | | | | | | | | | | | | | | | | | | | | | X | X | | | | | | |
| TP327637 Indicator | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | X | |
| TP327638 Indicator | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | X | | | |
| TP327639 Indicator | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | X | | |
| TP327640 Bypass Switch | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | X | X | | | | X |
| TP322001 Receive Logic Card | X | X | X | X | X | X | X | | X | X | X | X | X | X | X | | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| TP322002 Send Logic Card | X | X | X | X | X | X | X | | X | X | X | X | X | X | X | | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| TP322400 Multifunction Card | | | | | | | | | X | X | X | X | X | X | X | | | | | X | X | X | X | | | X | X | X | X | | | X | X | X | |
| TP322422 Parity Insert Card | | | | | | | | | | | | | | | | | X | | | | | | | | | | | | | | | | | | X |

divide by 64 circuit. A second half of ML4 is used to reset the dual J-K flip-flops and inhibit the output at pin 1 of the card.

4.04    Q1 and Q2 are arranged as common emitter inverting amplifiers with R2 and R4 respectively, providing base bias with collector feedback. R3 increases the input impedance of Q2 and provides some stabilization. C2 is used to couple the output of Q2 to the input of Q1. The crystal is used to provide feedback from the collector of Q1 to the base of Q2. The feedback is in the form of the critical frequency of the crystal and Q1 will be driven from saturation to cut-off at that frequency. The purpose of R1 is to reduce the power dissipation in the crystal. C1 is used to decouple oscillations of a higher harmonic mode that might occur due to the stray capacitances associated with the crystal.

4.05    When the control input pin 15, and the reset pin 10, are in the logical "1" state (positive), the dual J-K flip-flops are held on the zero count and the output pin 1, is in the logical "0" state (ground). When the reset input is in the logical "0" state, the output pin 1, will switch states at 1/64 of the crystal frequency. Output pin 1, is normally in the logical "0" state. It changes to the logical "1" state at exactly 50 percent of the period. The maximum error in the first bit due to the reset going to the "0" state out of phase with the free running oscillator is -1.67 percent, +0.1 percent. This error figure includes the frequency stability of +0.1 percent over a temperature range of $+5^{\circ}\bar{C}$ to $+65^{\circ}C$.

4.06    Reset to the zero count is inhibited when the control input on pin 15 is 0 volts. This action eliminates the possibility of shortening the last pulse at the output pin 1, as a result of the reset going to the "1" state while the output pin 1, is positive. The reset is enabled when the full count of 64 oscillations has occurred and the output pin 1, has returned to the "0" state. Storage temperature is $-55^{\circ}C$ to $+125^{\circ}C$.

PARITY INSERT CIRCUIT CARD

A.    Description

4.07    The parity insert circuit card (TP322422) is designed to provide the SA120 parity detector with the capability of examining outgoing signals from a send terminal for even parity. If parity is found incorrect, the parity insert card will insert a parity bit prior to send terminal transmission.

4.08    The parity insert circuit card (TP322422) works in conjunction with the two circuit cards (TP322001 and TP322002) that are part of the SA120 parity detector. The parity insert circuit card mounts in between and on the two parity detector circuit cards.

4.09    Parity insertion can be provided in the sixth, seventh, or eighth bit levels of a character by the programming arrangement of straps on the parity insert card. Programming arrangements for parity insertion in the various levels are described as follows:

PARITY INSERTION IN SIXTH LEVEL

| STRAPS IN | STRAPS OUT |
|-----------|------------|
| A | B |
| E | C |
| F | D |
| H | J |
| N | K |
|   | L |
|   | M |

PARITY INSERTION IN SEVENTH LEVEL

| STRAPS IN | STRAPS OUT |
|-----------|------------|
| B | A |
| D | C |
| F | E |
| J | H |
| M | K |
|   | L |
|   | N |

PARITY INSERTION IN EIGHTH LEVEL

| STRAPS IN | STRAPS OUT |
|-----------|------------|
| C | A |
| D | B |
| E | F |
| K | H |
| L | J |
|   | M |
|   | N |

B.    Principles of Operation

4.10    The following discussion is for parity insertion in the eighth-level. As an aid to this discussion, reference should be made to the logic diagram shown on Figure 12. In the discussion, a space is high, and a mark is low.

Figure 12 - Parity Insert Logic Diagram
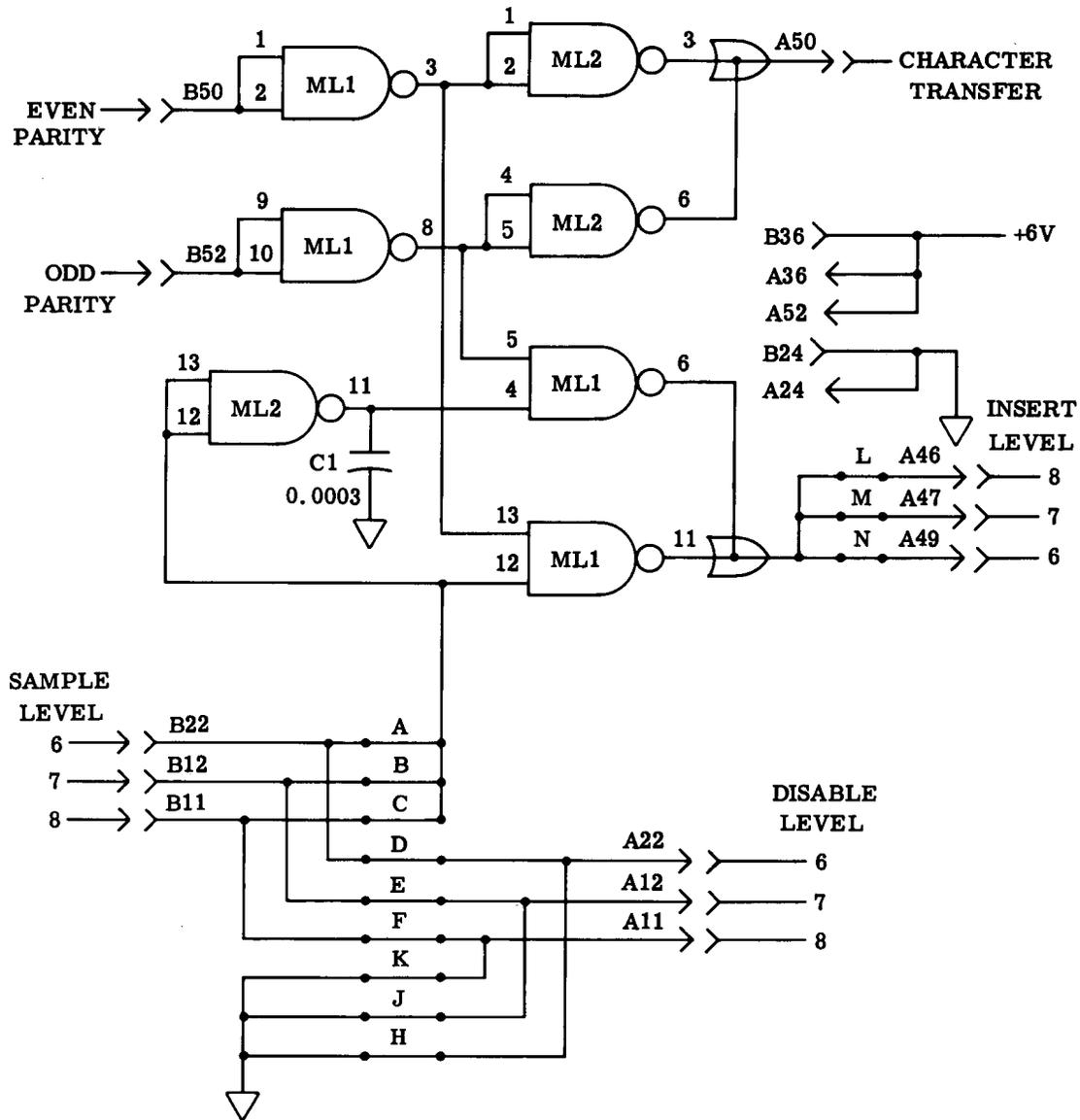
Note 1: Terminal designations with prefix A
are located on the component side of the
circuit card, and terminal designations with
prefix B are located on the circuit side of the
card.

Note 2: Refer to sheet 2 drawing TP322422
shipped with equipment (part of WDP0204)
for complete description and instructions.

4.11 The input at pin B50 is driven low for every even parity character received in the register of the receive circuit card (TP322001) of the SA120 parity detector. The input at pin B52 is also driven low for every odd parity character received in the same register. Therefore, for every character received, either even or odd parity, pin A50 will be driven low by gates ML1-3, ML2-3, or ML1-8, and ML2-6. Specifically, a low input at pin B50 is applied to pins 1 and 2 of ML1-3. The output of ML1-3 goes high and is applied to the input (pins 1 and 2) of ML2-3. The output of ML2-3 is then driven low and applied to pin A50.

4.12 A low input at pin B52 performs the same function as described for pin B50, but makes use of gates ML1-8 and ML2-6. The outputs of gates ML2-3 and ML2-6 are connected together to perform an OR function. Therefore, a low input at either pin B50 or pin B52 results in a low output at pin A50.

4.13 The output at pin A50 which is applied to the send card (TP322002) in the parity detector, allows bits 1 through 7 of the character in the receive register (circuit card TP322001 in the parity detector) to be transferred to the send register (circuit card TP322002) in the parity detector. When a character is received with even parity, gate ML1-11 will transfer the signal in the eighth flip-flop of the receive register on the TP322001 card, to the eighth level flip-flop of the send register on the TP322002 card. This happens because the output of ML1-3 is high with an even parity character.

4.14 The high output of ML1-3 is applied to the input, pin 13, of ML1-11. The other input to ML1-11, pin 12, is supplied from pin B11 which samples the output of the eighth level flip-flop in the receive register on the TP322001 card.

4.15 With a space in the eighth level, pin 12 of ML1-11 would be high. With both pins (13 and 12) of ML1-11 high, the output is low. This low indication is applied to pin A46 where it is then transferred to the send register of card TP322002 and a space inserted in the eighth level flip-flop. If the eighth level had been a mark, pin B11 would have been low driving pin 12 of ML1-11 low. A low at pin 12 of ML1-11 would prevent the output (pin 11) from going low, and preventing a space from being inserted into the eighth level flip-flop of the send register. The result of this is that when an even parity character is received, the signal sense of the eighth level is not changed.

4.16 When a character is received with odd parity, gate ML1-6 transfers the opposite state of the eighth level flip-flop of the receive register on card TP322001 into the eighth level flip-flop of the send register on card TP322002. With an odd parity character, the output of ML1-8 is high. This high is applied to ML1-6 at pin 5. The other input to ML1-6 is supplied from ML2-11. Gate ML2-11 receives its input from pin B11 which samples the output of the eighth level flip-flop in the receive register on the TP322001 card.

4.17 With a space in the eighth-level, pins 12 and 13 of ML2-11 will be high driving the output (pin 11) low which is applied to pin 4 of ML1-6. With a low at one of the inputs, the output of ML1-6 is held high. The output of ML1-11 is also held high by the low at input pin 13. With a high at pin A46, a space will not be transferred to the eighth-level flip-flop in the send register of the TP322002 card.

4.18 If the eighth-level had been a mark, pin B11 would have been low driving pins 12 and 13 of ML2-11 low. A low at pins 12 and 13 of ML2-11 drives the output, pin 11, high which is applied to pin 4 of ML1-6. With a high at both input pins 4 and 5 of ML1-6, the output, pin 6, is driven low. A low at pin 6 of ML1-6 is applied at pin A46, and inserts a space into the eighth-level flip-flop in the send register of the TP322002 card. As a result, when a character with odd parity is received, the signal sense of the eighth-level is changed during the transfer from the TP322001 card to the TP322002 card in the parity detector.

INTERFACE CIRCUIT CARD FOR CURRENT/NO CURRENT DATA SETS (101C OR 105A) AND 33 OR 35 TERMINALS

A. Description

4.19 The interface circuit card (TP323513) accepts current/no current data from either a 101C or 105A data set and converts it into suitable bi-polar voltage signals for use by the SA120 parity detector. In addition, it accepts bi-polar voltage data from the SA120 parity detector and converts it into current/no current signals for use by the 33, 35, or high speed terminal equipment.

4.20    All data signals between the data set and the receiving terminal set are neutral dc signals (current/no current). The signals are as follows:

MARK = 20 milliamperes (nominal)
SPACE = 0 current

All polar data signals at the SA120 parity detector are negative for mark and positive for space.

4.21    Interconnection between the TP323513 interface amplifiers and the parity detector is accomplished by a three wire signal cable (input, output, and ground) provided by the parity detector. Interconnection between the TP323513, data set, and receiving terminal is accomplished on the apparatus wiring field by a 5-1/2 feet long cable provided with the parity detector, or by the bypass and indicator assembly if used.

4.22    The TP323513 uses the dc power from the SA120 parity detector. Interconnection between them is provided by a two wire cable. The dc power requirements from the parity detector are as follows:

+14 v dc (nominal) at 20 ma (nominal)
-14 v dc (nominal) at 40 ma (nominal)

B.    Principles of Operation

4.23    The circuit card TP323513 consists of two interface amplifiers (Figure 13). The input interface amplifier (Q1), an NPN transistor, accepts current/no current signal data from either the 101C or 105A data set and converts it into suitable bi-polar voltage signals for use by the SA120 basic input amplifier (Figure 4). The output interface amplifier (Q2), a PNP transistor, accepts bi-polar voltage signals from the SA120 basic output amplifier (Figure 4) and converts it into current/no current signals for use by the receiving terminal equipment.

4.24    The circuit card is equipped with eight male stationary terminals. The terminal assignments are given in 4.26.

Marking Signal Line

4.25    With the signal line (at terminal 1) in the marking condition (Figure 13), Q1 is turned on by base current supplied through resistor R2. The potential at the collector (terminal 4) of Q1 will be near the negative dc supply voltage, -14 v (nominal). At the same time, Q2

will be turned on by base current supplied through resistor R5 because of a negative voltage at terminal 5. At this time, the potential at the collector of Q2 will be near zero. The collector resistor R7 (terminal 2) must be connected to a -20 v dc (nominal) supply source through a nominal resistive load of 680 ohms. Therefore, with the collector potential nearing zero, a nominal 20 ma current will flow through the 680 ohms load.

Spacing Signal Line

4.26    In the spacing condition (Figure 13), Q1 is turned off. The potential at the collector of Q1 will be +8 v dc (nominal). Also, Q2 will be turned off preventing current from flowing in the collector circuit. Terminal assignments for the TP323513 are as follows:

| TERMINAL NUMBER | DESCRIPTION |
|---|---|
| 1 | Accepting current/no current signals from the data set. |
| 2 | Sending current/no current signals to receiving terminal set. |
| 3 | Signal and frame ground. |
| 4 | Sending bi-polar voltage signals to the SA120 parity detector. |
| 5 | Accepting bi-polar voltage signals from the SA120 parity detector. |
| 6 | Signal and frame ground. |
| 7 | +14 v dc (nominal) |
| 8 | -14 v dc (nominal) |

BREAK GENERATOR/COUNTER DRIVER CIRCUIT CARD

A.    General

4.27    The break generator/counter driver circuit card (TP322400) (Figures 14 and 15) provides the SA120 parity detector with the additional means of indicating the detection of a parity errored character. In addition to the substitute character indication provided by the basic SA120 parity detector, the circuit card provides the elements for activating a counter, lighting a lamp, or producing a timed line break when used with a bypass and indicator assembly
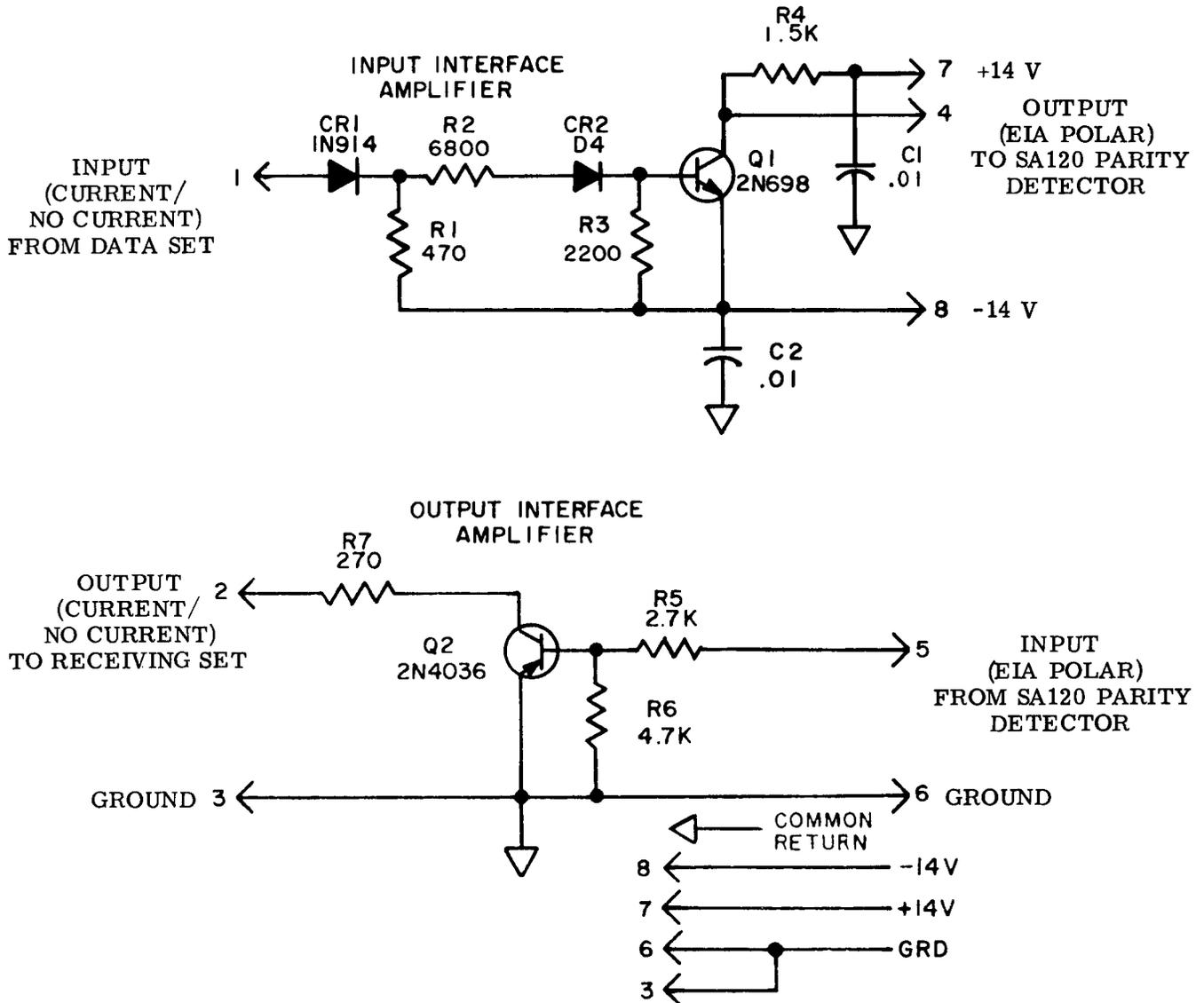
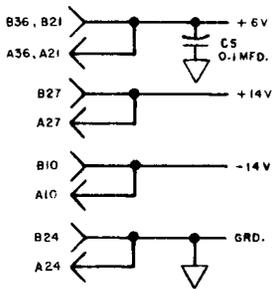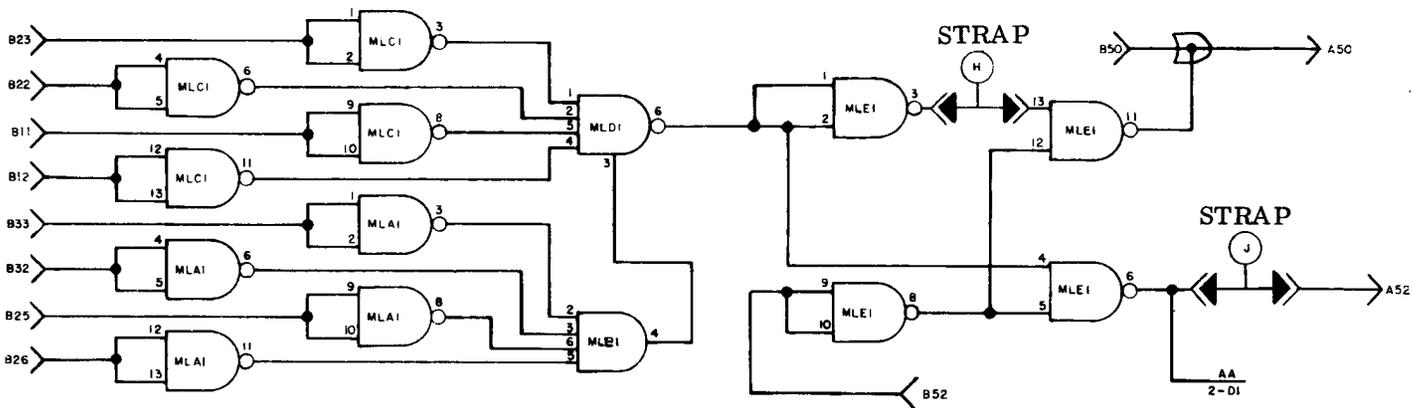Figure 13 - Interface Amplifier Terminal and Circuit Card TP323513

(Figure 2). Refer to sheet 2 drawing TP322400, shipped with the equipment, for complete schematic wiring diagram.

4.28 The circuit card may be used with even or odd parity systems. Also, for systems employing the 7-level BCD code (7-level odd parity), the circuitry is such that rubout (all 8 levels marking) will be detected and transferred through the SA120 parity detector. No substitution is made for this character in odd parity systems.

4.29 Upon detecting a parity errored character, the circuitry of the break generator/counter driver circuit card is triggered. When triggered, 'two outputs are provided; one is a positive going pulse (-14 volts to +14 volts), and the other is a set of form C (transfer) relay contacts.

B.  Description

4.30 The break generator/counter driver circuit card (TP322400) receives its power (+6 v, +14 v, and -14 v) from the SA120

Figure 14 - TP322001 Partial Schematic Wiring Diagram With Terminal Pin Designations and Substitution Inhibit Straps

Note 1: To inhibit substitution of character on error and copy errored character as received, remove straps H and J.

Note 2: See drawing TP322001 shipped with equipment for complete schematic wiring diagram.

Note 3: All terminal designations with prefix A are located on the component side of the card and all terminal designations with prefix B are located on the circuit side of the card.

Note: Refer to Section 578-200-201 for preparation and installation instructions. Refer to sheet 2 drawing TP322400 shipped with the SA120 for complete schematic wiring diagram.



Figure 15 - Straps and Terminals on TP322400 (Component A Side)
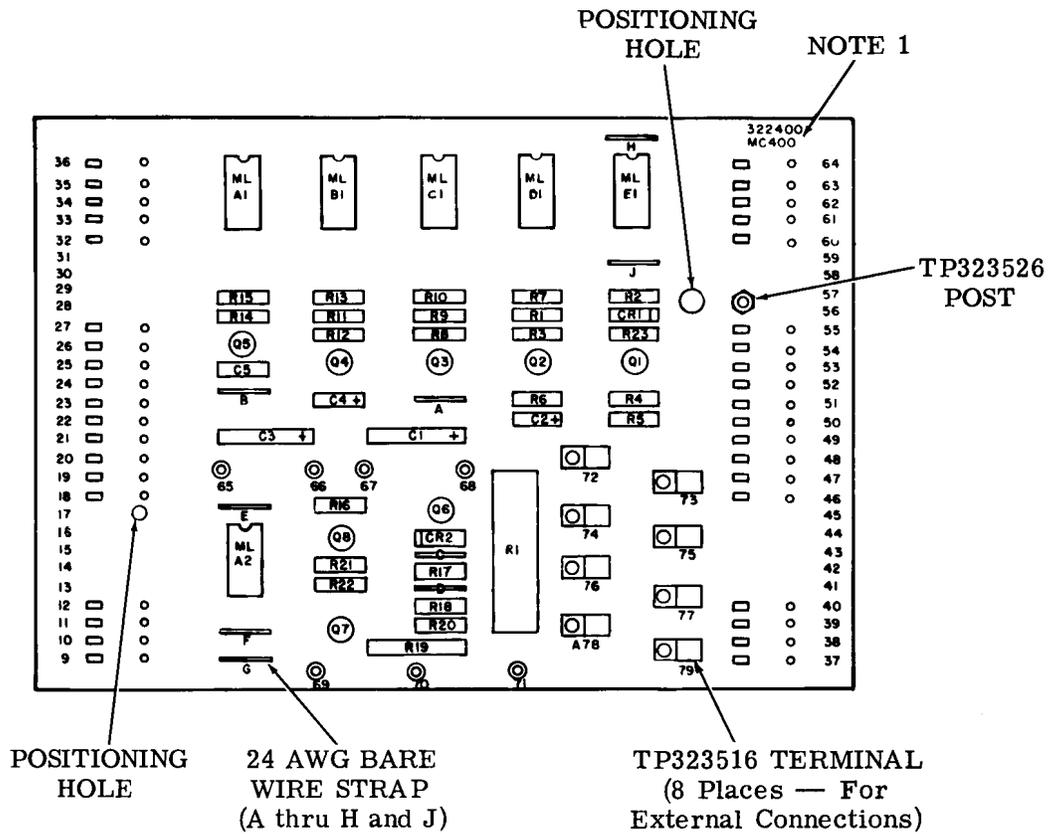
| | STRAP A | STRAP B | OUTPUT PULSE | INHIBIT BETWEEN PULSES |
|---|---|---|---|---|
| NOTE 1. | IN | IN | 250 MS | 250 MS (FACTORY WIRING) |
| | OUT | IN | 250 MS | NONE |
| | IN | OUT | 3.5 MS | 500 MS |
| | OUT | OUT | 3.5 MS | NONE |
| NOTE 2. | REMOVE STRAP C TO ENERGIZE RELAY DURING OUTPUT PULSE. REMOVE STRAP D TO REMOVE RELAY FROM CIRCUIT. RELAY WILL NOT RESPOND TO 3.5 MS OUTPUT PULSE. | | | |
| NOTE 3. | REMOVE STRAPS F AND G TO PROVIDE RELAY CONTACT CLOSURE AND OUTPUT PULSE ON EVERY ERROR DETECTED. REMOVE STRAP E TO PROVIDE LATCH ON FIRST ERROR AND BLINK (RELAY DROP-OUT AND PICK-UP) ON SUCCEEDING ERRORS. REMOVE STRAPS E AND F TO PROVIDE LATCH ON FIRST ERROR. | | | |
| NOTE 4. | REMOVE STRAPS H AND J TO INHIBIT SUBSTITUTION OF CHARACTER ON ERROR AND COPY ERRORED CHARACTER AS RECEIVED. | | | |
| NOTE 5. | ALL RESISTORS ARE 1/4 WATT AND VALUES ARE IN OHMS UNLESS OTHERWISE SPECIFIED. | | | |

parity detector. Signals between the parity detector and the circuit card are neutral dc signals (+6 v and 0 v) of 200 to 400 nanosecond duration. The card consists of an input interface amplifier, two one-shot multivibrators, a relay driver and relay, an output amplifier, integrated logic circuitry for the detection of rub-out, and a latching circuit.

4.31    The two one-shot multivibrators are connected in series so that a change in state of the first (initiated by an error pulse from the SA120 parity detector) causes a change in state of the second. The time-out period of the second one-shot multivibrator controls the duration of the output pulse and the time that the relay is energized. If the time-out period of the first one-shot is longer than that of the second, triggering of the second one-shot will be inhibited for a time equal to the difference between the two periods. Strapping options on the circuit card (Figures 14 and 15) provide the combinations of output and inhibit. Times intermediate to those listed may be obtained with add-on capacitors of the proper value.

4.32    A parity error detected by the SA120 parity detector provides an error signal that triggers the one-shot multivibrators in the break generator circuitry. During the time-out period, a positive going pulse (-14 volts to +14 volts) appears at the output terminal of the circuit card and energizes the relay. At the end of the time-out period, the relay is de-energized and the output line returns to -14 volts.

4.33    For systems using the BCD code (7-level odd parity), a rub-out (delete) detect circuit is incorporated so that a substitute character is not inserted when the delete character (all levels marking) appears in the receive register of the parity detector. The end-of-line character is the only one in the BCD code that uses the eighth level. By punching delete (rub-out), in tape, over the end-of-line character, a legitimate even parity character may be produced in an otherwise odd parity system.

4.34    Because most processors are programmed to ignore delete (rub-out), it may be transferred through the parity detector in odd parity systems. When the rub-out character is detected by the circuitry of the break generator card, the error signal is inhibited, and the break generator circuitry is not triggered.

4.35    Following is a list of strap options available for various modes of operation of the relay on circuit card TP322400:

(a)    Relay energized at the beginning of the time-out period and de-energized at the end of it. Because the relay cannot be pulsed at a rate corresponding to consecutive errors at 2400 words per minute, an additional strapping option allows the relay coil to be removed from the circuit without interfering with the pulse output. This change also disables the error lamp.

(b)    Relay energized and latched on the first error received. The relay remains latched until reset manually.

(c)    Relay energized and latched on the first error received. Subsequent errors cause the relay to de-energize at the beginning of the time-out period, and re-energize at the end of it. Using the relay contacts, an indicator lamp may be made to go on with the first error, and blink off and on with subsequent errors.

4.36    A strap option on the card, TP322400, allows the terminal equipment to copy all errored characters as received and indicate the detection of the errors by a lamp on an indicating device.

C.    Principles of Operation

4.37    As an aid to the following discussion, refer to the logic and schematic drawings, 322400, packaged with the break generator/counter driver circuit card, TP322400. If the circuit card is factory installed, the drawings are included in the complete set of (WDP0204) with the SA120.

Rub-Out Detect Circuitry

4.38    The inputs to gates MLA1 and MLC1 of the break generator card are connected to the elements of the receive shift register of the SA120 parity detector. When a character is shifted into the register, the inputs are high (+6 volts) for a space, and low (0 volts) for a mark. A rub-out character (delete) stored in the register causes all the inputs to MLA1 and MLC1 to be low, and all the inputs to MLB1 and MLD1 to be high. At this time, MLD1-6, the controlling output, is low. Any character, other than rub-out, causes at least one input to MLD1 to be low. This low input is sufficient to maintain a high output at MLD1-6.

4.39 When a character possessing the proper parity is shifted into the receive register of the SA120 parity detector, a 200 to 400 nanosecond negative going signal (+6 volts to 0 volts) appears at terminal B50 of the break generator/counter driver card. This signal also appears at terminal A50, and is used to transfer the stored character to the send register of the parity detector.

4.40 When a character with improper parity is shifted into the receive register of the parity detector, a 200 to 400 nanosecond negative going signal appears as a positive going pulse at MLE1-8, 5, and 12. If the character with improper parity is rub-out (delete), MLD1-6 is low. This low level also appears at MLE1-1, 2, and 4. A low at MLE1-4 maintains a high output at MLE1-6, thereby inhibiting the transfer of the substitute character. The low input at MLE1-2 produces a high output at MLE1-3, and a high input at MLE1-13. The positive pulse appearing at MLE1-12 now appears as a negative going pulse at MLE1-11 and terminal A50. The rub-out character is, therefore, transferred to the send register of the parity detector.

4.41 If the character with improper parity is not the rub-out character, MLD1-6 and MLE1-1, 2, and 4 are high. The high inputs at MLE1-1 and 2 produce a low input at MLE1-13. This low input at MLE1-13 maintains a high level at terminal A50 to inhibit transfer of the received character to the send register. The high input at MLE1-4 allows the positive pulse at MLE1-5 to be coupled through and appears as a negative going pulse at MLE1-6, terminal A52, and the input to the break generator circuitry. The preprogrammed substitute character is transferred to the send register of the parity detector, and the break generator is triggered.

4.42 As noted on the schematic drawing, 322400, if straps H and J are removed, an error pulse at terminal B52 will trigger the break generator circuitry. However, the errored character will be transferred to the send register, in the parity detector, as received.

Break Generator Circuitry

4.43 Interface amplifier Q1 is held on by the normally high output of MLE1-6. The negative going pulse (+6 volts to 0 volts) produced at MLE1-6, upon the detection of an errored character, causes Q1 to become nonconductive.

4.44 Stages Q2 and Q3 constitute a one-shot multivibrator whose time-out period is controlled by R8, C1, and/or C2. Since Q1 is normally conducting, the potential at the collector is approximately 0 volts holding Q2 off. The base-emitter junction of Q3 is forward biased, and base current flowing through R8 keeps this stage on. When Q1 is cut off at the detection of a parity error, Q2 is brought into conduction, and a negative going transition is produced at the collector. This transition is capacitively coupled to the base of Q3 by C1 and/or C2. Stage Q3 is turned off, and the multivibrator begins its time-out period. The capacitor begins to charge, and continues to do so, until the base of Q3 becomes positive enough to allow it to conduct again. With both capacitors in the circuit (factory wiring), the time-out period of one-shot multivibrator Q2-Q3 is approximately 500 ms. Removing strap A so that only C2 is in the circuit reduces the time-out period to approximately 1 ms. Time-out periods intermediate to these two may be obtained by connecting a capacitor of proper value between terminals A67 and A68 (strap A removed).

4.45 Stages Q4 and Q5 also form a one-shot multivibrator. The controlling elements are R14, C3, and/or C4. Operation is the same as one-shot multivibrator Q2-Q3. With both capacitors in the circuit (factory wiring), the time-out period of Q4-Q5 is approximately 250 ms. By removing strap B so that only C4 is in the circuit, the time-out period is reduced to approximately 3.5 ms. Time-out periods intermediate to these two may be obtained by connecting a capacitor of proper value between terminals A65 and A66 (strap B removed).

4.46 The time-out period of one-shot multivibrator Q4-Q5 controls the break generator output pulse and the relay. One-shot Q2-Q3 controls one-shot Q3-Q4 so that if the time-out period of Q2-Q3 is longer than Q4-Q5, Q4-Q5 cannot be retriggered until Q2-Q3 returns to its stable state. In this way, error indications may be inhibited for a time equal to the difference of the two time-out periods.

Relay Driver and Output Amplifier

4.47 In order to allow relay K1 to be energized when Q6 conducts, strap C must be removed. The relay coil may be replaced with a resistive load (R17) by removing strap D, leaving strap C in place. This option is provided because

the relay coil interferes and the relay cannot respond to consecutive error pulses when operating at 2400 words per minute.

4.48    Relay driver Q6 is held off by a 0 volt input from the collector of Q5, which is normally conducting, or from the latching circuit MLA2. When a parity error is detected by the SA120 parity detector and the one-shot multivibrators are triggered, Q6 is turned on and relay K1 is energized for a period equal to the time-out period of one-shot Q4-Q5 (latching circuit disabled).

4.49    Because stage Q6 is normally off, the positive potential at its collector holds output amplifier Q7 off. The output of the circuit card at terminal A79 is normally -14 volts. When Q6 is turned on, upon the detection of a parity error, Q7 is turned on raising the output to +14 volts. The output will remain positive for the duration of the Q4-Q5 time-out period.

Relay Latch Circuit

4.50    Operation of this circuit (strap E closed, straps F and G open) is the same as the relay driver and output amplifier circuit. The relay driver Q6 is controlled by the signal at the collector of Q5. The relay will be energized every time one-shot multivibrator Q4-Q5 is triggered.

Permanent Latch Option

4.51    In order to use the latch circuit (strap G closed, straps E and F open), the emitter of Q8 (terminal A72) must be returned to circuit common (terminal A73 or A75) through a normally closed set of contacts. The contacts can be opened momentarily to provide the resetting condition.

4.52    When the permanent latch option is used, the relay is energized when the first error is detected by the SA120 parity detector, and remains energized until the latch is reset. In the quiescent state, Q5 is normally conducting, and the potential at its collector is approximately 0 volts. This low input at MLA2-12 and 13 results on a high output (+6 volts) at MLA2-11. A low output at MLA2-8 holds Q8 off and produces a high output at MLA2-3. This high output, in turn, produces a low output at MLA2-6 to hold the relay driver Q6 off.

4.53    Upon the detection of an error, one-shot multivibrator Q4-Q5 is triggered and the potential at the collector of Q5 rises toward +6 volts. The high input at MLA2-12 and 13 produces a low output at MLA2-11 which, in turn, produces a high output at MLA2-8. This positive potential allows Q8 to conduct. The resulting low potential at the collector is applied to MLA2-9 to maintain a high output at MLA2-8. The high output at MLA2-8 produces a high output at MLA2-6, which allows Q6 to conduct, the relay to be energized, and the output at terminal A79 to rise to +14 volts. The relay remains energized until the emitter circuit of Q8 is opened with the reset contacts. When the emitter circuit is opened, input MLA2-9 goes high, output MLA2-8 goes low, output MLA2-6 goes low, Q6 becomes nonconductive, and the relay is de-energized.

Permanent Latch with Blink Option

4.54    When this mode of operation is used (straps F and G closed, strap E open), the relay is energized on the first error and remains energized until it is reset. Succeeding errors, however, de-energize and re-energize the relay as one-shot multivibrator Q4-Q5 goes through its time-out period. If a lamp is used as an indicator and is powered through the relay contacts, it will turn on with the first error, and blink off and on with succeeding errors. To provide this blink feature, strap B in the Q4-Q5 one-shot multivibrator must be removed and a 2 mfd capacitor connected between terminals A65 and A66.

4.55    In the quiescent state, relay driver Q6 is held off as described in 4.51 and 4.52. Upon the detection of a parity error, one-shot multivibrator Q4-Q5 is triggered, and Q8 is latched on as described in 4.51. The low output at MLA2-11 produces a low output at MLA2-6, and the relay is held de-energized during the Q4-Q5 time-out period. When the time-out period is complete, Q5 conducts, MLA2-11 goes high, MLA2-3 goes low, MLA2-6 goes high, and the relay is energized. When one-shot multivibrator Q4-Q5 times-out on succeeding errors, output MLA2-11 changes from high to low at the beginning of the time-out period, and returns high at the end of it. This change, applied to MLA2-2, produces a corresponding change at MLA2-6, and causes the relay to be de-energized at the beginning of the time-out period and re-energized at the end of it.

BYPASS SWITCH AND INDICATOR ASSEMBLIES

A.  General

4.56    Versions of the SA120 are available for installation on 33 or 35 type receivers, Type 2 Senders or Receivers, or other equipment. For each type of terminal two or four optional bypass or indicator assemblies are available (Table A and Figure 2) which are connected to the SA120 chassis by a cable. Those for 33 and 35 type terminals mount adjacent to the call control unit or copyholder, while those for Type 2 Tape Receivers have magnetic bases for mounting on top of the cabinet.

4.57    Three of the optional assemblies (TP327631, TP327633, and TP327640) provide a bypass switch only. They are used in applications in which the substitute character error indication is used by itself, a line break on a half duplex line or on reverse channel is generated (in addition to the substitute character,) or in which parity is inserted at a sender. Bypassing the accessory with the switch is necessary for a receiving terminal to receive messages from nonparity senders, and is also desirable for testing. One assembly (TP327639) provides a bypass switch and indicator lamp to notify the operator of the receiving station that an error has been detected. (A break cannot be generated when this assembly is used.) The other assemblies all provide a bypass switch, indicator lamp, and error counter (either low or high speed) to enable the receiving operator to decide, on the basis of the number of errors counted and the length and content of the message, and whether to accept the message or request a retransmission. These assemblies are also useful for maintenance purposes, since they allow transmission errors to be distinguished from machine errors.

Note: When the low speed counter is used in high speed operation (SA120EC), only the number of widely-separated individual errors or error bursts will be recorded. The counter is capable of registering consecutive errors at a maximum rate of 150 wpm. When operating at 1050 wpm the count registered may be as low as 15 percent of the number of errors detected by the SA120. In cases when consecutive errors are received, however, all errors detected by the SA120 will be substituted for in the received tape.

B.  Bypass Switch and Indicator Assemblies for 33 Type Sets

4.58    Assemblies TP327631 and TP327632 are designed to be mounted on 33 type ASR, KSR, or RO sets. They are attached to a bracket which clips on the cover underneath the ivory lid and hooks around on the bottom edge at the rear (Figure 16). A single cable connects the assembly to the SA120 chassis, placed inside the stand or mounted on an adjacent wall or table.

4.59    The wiring for bypass switch assembly TP327631, the SA120 chassis, and the terminal is shown in simplified form on Figure 17 for units having card TP322400. Refer to 8716WD for a complete schematic and to 8566WD for actual wiring information.

(a)  The bypass switch, SW1, has four transfer contacts but only three of them are used. In the bypass position (as shown) on Figure 17), the data set output is fed in at pin 5 on the orange wire, transferred to pin 4, and fed out to the SMD input of the terminal on the yellow wire. Since pin 2 is closed to pin 6, the data output of the SA120 (white wire) is connected to the data input of the SA120 (red wire). The white-slate and white-purple wires are in series with the break contact of the terminal (if present) and are tied together at pin 7 and 8. The slate and purple wires connect to the relay break contact in the SA120.

(b)  When SW1 is activated, the data set output at pin 5 (orange wire) is transferred to pin 6 (red wire) where it is supplied to the data input of the SA120. The data output of the SA120 (white wire) at pin 2 is transferred to pin 4 (yellow wire) where it is supplied to the input of the SMD. This places the SA120 in series with the incoming data stream between the data set and the terminal. Also, the white-slate and white-purple wires at pins 7 and 8 are disconnected and the break contact of the SA120 relay is inserted between them in series. When energized, this relay opens the output data line, thereby causing a break to be generated.

4.60    The wiring for bypass switch assembly TP327631, the SA120 chassis, and the terminal for units not equipped with card TP322400 is somewhat different from that described in 4.59. Only four wires are necessary to connect the SA120 to the bypass switch and the terminal in this case. The white and red wires connect the bypass switch to the SA120 output and

BYPASS SWITCH ASSEMBLY (TP327631)
OR INDICATOR ASSEMBLY (TP327632)
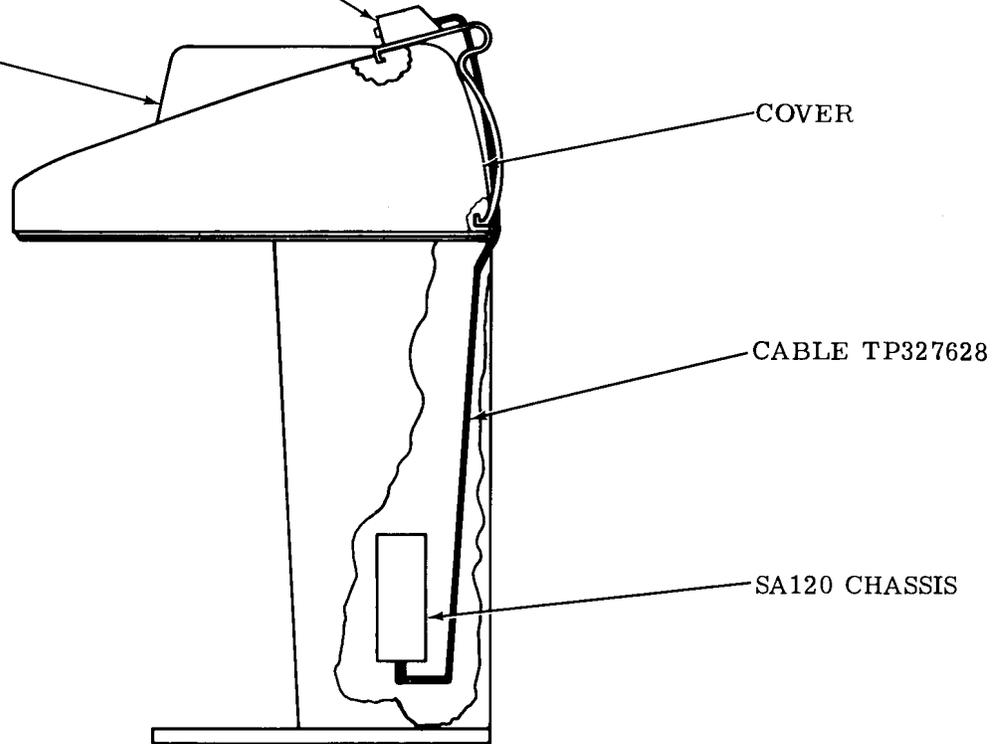
IVORY LID

COVER

CABLE TP327628

SA120 CHASSIS

Figure 16 - Location of Bypass Switch and Indicator Assembly on Model 33 Set

input at TB4-2 and TB4-1, as shown in Figure 17, but the two black wires are connected to TB4-3 instead of A73 and A75. The other wires are not used. Consequently, only the data set output is switched.

4.61    The wiring for bypass switch and indicator assembly TP327632, the SA120 chassis, and the terminal is shown in simplified form on Figure 18. Refer to 8716WD for a complete schematic and to 8566WD for actual wiring information.

(a)    The bypass switch, SW1, has four transfer contacts but only three of them are used. In the bypass position (as shown on Figure 18), the data set output is fed in at pin 5 on the orange wire, transferred to pin 4, and fed out to the SMD input of the terminal on the yellow wire. Since pin 2 is closed to

pin 6, the data output of the SA120 (white wire) is connected to the data input of the SA120 (red wire). Since the bypass and indicator assembly does not have break generation capability, the white-slate and white-purple wires are tied back at the terminal.

(b)    When SW1 is activated, the data set output at pin 5 (orange wire) is transferred to pin 6 (red wire) where it is supplied to the data input of the SA120. The data output of the SA120 (white wire) at pin 2 is transferred to pin 4 (yellow wire) where it is supplied to the input of the SMD. This places the SA120 in series with the incoming data stream, as for the TP327631 assembly. The counter coil, DS2, and the lamp, DS1, are connected to the relay transfer contact in the SA120. When the relay is energized, this contact permits the counter to register the error and the lamp to
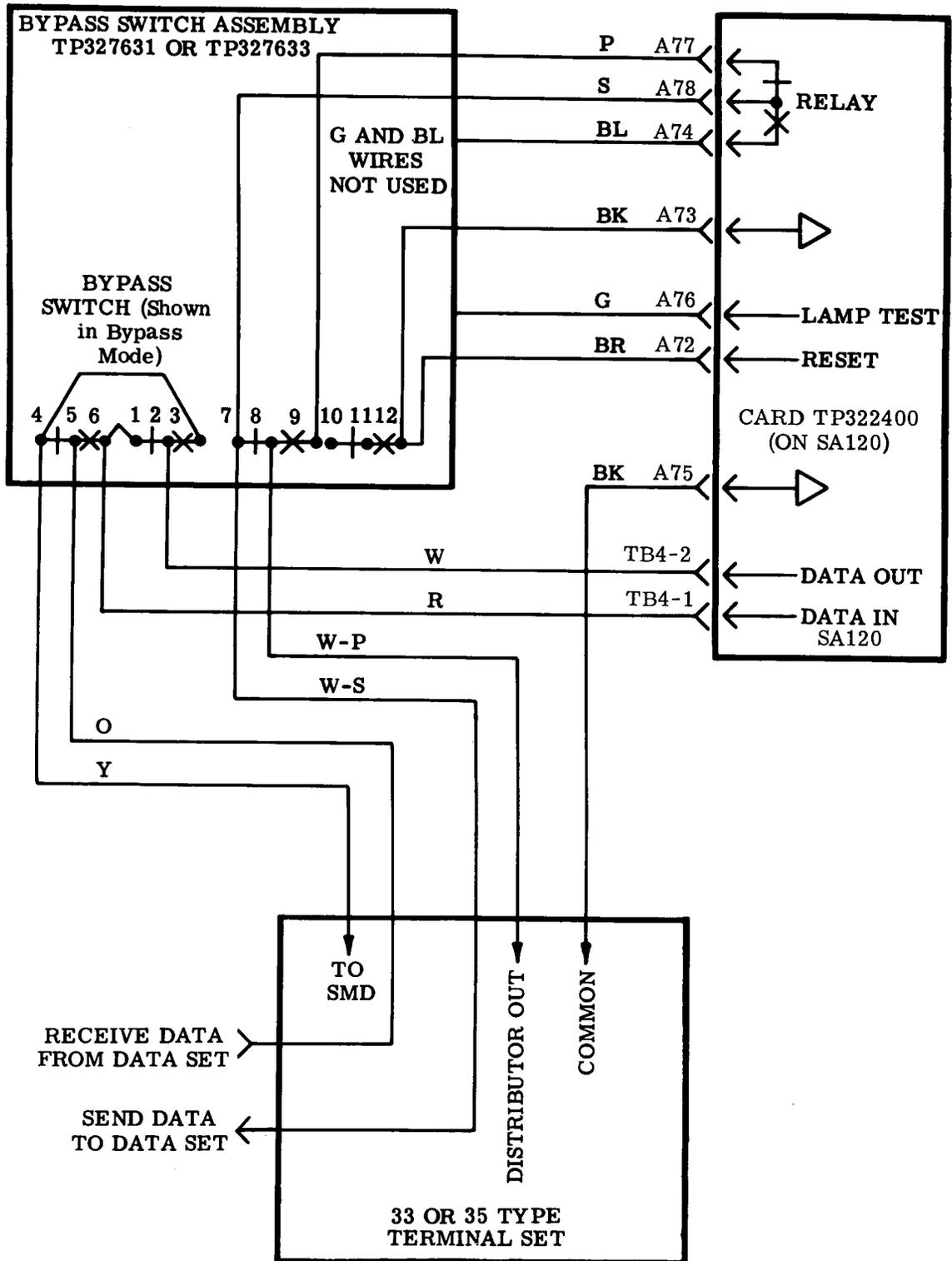
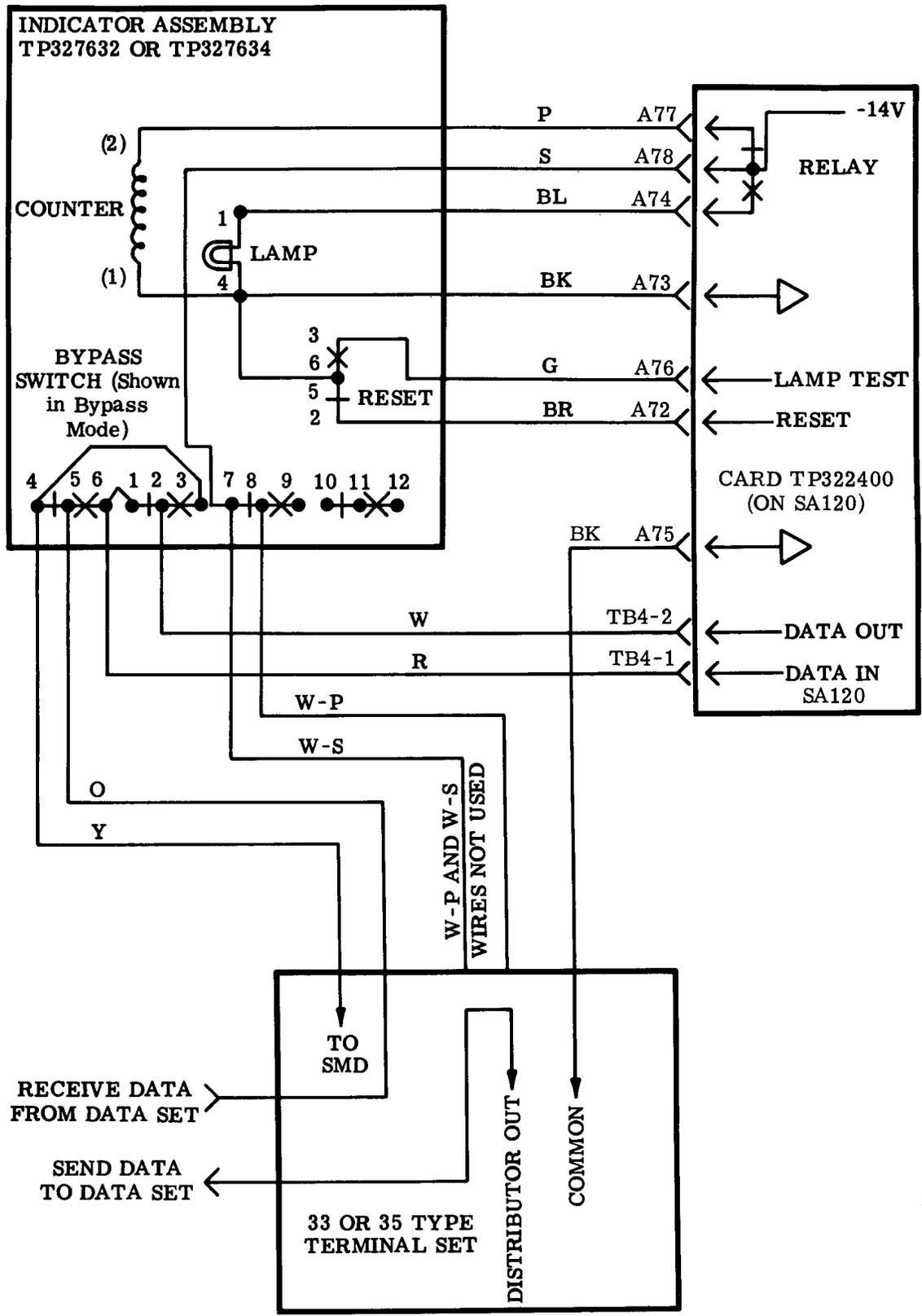Figure 17 - Simplified Wiring for SA120BC, SA120BD, SA120CC and SA120CD

Figure 18 - Simplified Wiring for SA120BE, SA120BF, SA120CE and SA120CF

light. Depending on the SA120 strapping, the lamp will flash on for each error or latch on for the first error and flash off for each additional error. For each flash (on or off) of the lamp, the counter will register another count. The reset switch, SW2, extinguishes the lamp when the lamp housing is depressed; the counter is mechanically reset to zero by its own pushbutton.

C. Bypass Switch and Indicator Assemblies for 35 Type Sets

4.62 Assemblies TP327633 and TP327634 can be mounted on 35 type ASR, KSR, or RO sets. Two holes are drilled in the upper cover of the terminal and the bypass or indicator assembly attached with screws and lockwashers (Figure 19). A single cable connects the assembly to the electrical service unit "C" wiring field and the SA120 chassis, which is placed inside the pedestal or mounted on an adjacent wall or table.

4.63 The wiring for assemblies TP327633 and TP327634 is identical to that for assemblies TP327631 and TP327632, respectively (4.59 through 4.61).

D. Bypass Switch and Indicator Assemblies for Type 2 Tape Senders and Receivers

4.64 Assemblies TP327637 through TP327639 are for use on Type 2 receivers, and assembly TP327640 is for use on either Type 2 Tape Senders or receivers. These assemblies are held on the top of the cabinet by means of two magnets attached to the bottom of the assembly (Figure 20). Two cables are supplied to connect the assembly to the data set and the SA120 chassis, which is placed on a shelf inside the cabinet.

4.65 The wiring for bypass switch assembly TP327640, the SA120 chassis, a Type 2 tape receiver, and its data set is shown in simplified form on Figure 21 for units having card TP322400. Refer to 8717WD for a complete schematic and to 8567WD for actual wiring information. The wiring for bypass switch assembly TP327640 and a Type 2 Sender is described in 4.70.

(a) The bypass switch, SW1, is wired similarly to those for bypass switch assemblies TP327631 and TP327633. In the bypass position (Figure 12), the data set output is fed in at pin 5 on the orange wire, trans-

ferred to pin 4, and fed out to the receiving distributor input of the terminal on the yellow wire. Since pin 2 is closed to pin 6, the data output of the SA120 (white wire) is connected to the data input of the SA120 (red wire). The white-purple wire brings +17.5 volts from the data set (via the Type 2 tape receiver) to pin 8, where it is transferred to pin 7 and connected by the white-slate wire to the supervisory transmitted data input of the data set, holding reverse channel on at all times. The slate and purple wires connect to the relay break contact in the SA120.

(b) When SW1 is activated, the data set output at pin 5 (orange wire) is transferred to pin 6 (red wire) where it is supplied to the data input of the SA120. The data output of the SA120 (white wire) at pin 2 is transferred to pin 4 (yellow wire) where it is supplied to the input of the receiving distributor. This places the SA120 in series with the incoming data stream between the data set and the terminal. Also, the white-slate and white-purple wires at pins 7 and 8 are disconnected and the break contact of the SA120 relay is inserted between them in series. When energized, this relay opens the path to the supervisory transmitted data input, thereby causing a break on reverse channel to be generated.

4.66 The wiring for bypass switch assembly TP327640, the SA120 chassis, a Type 2 Receiver, and its data set for units not equipped with card TP322400 is somewhat different from that described in 4.65. Only five wires are necessary to connect the SA120 to the bypass switch and the terminal in this case. The white and red wires connect the bypass switch to the SA120 output and input at TB4-2 and TB4-1, as shown in Figure 21, but the black wire and the two black-slate wires are connected to TB4-3 instead of A73 and A75. The other wires are not used. Consequently, only the data set output is switched.

4.67 The wiring for bypass switch and indicator assembly TP327638, the SA120 chassis, the receiver, and the data set is shown in simplified form on Figure 22. Refer to 8717WD for a complete schematic and to 8567WD for actual wiring information.

(a) The bypass switch, SW1, has four transfer contacts but only three of them are used. In the bypass position (as shown on Figure 22), the data set output is fed in at pin 5 on the orange wire, transferred to pin 4,
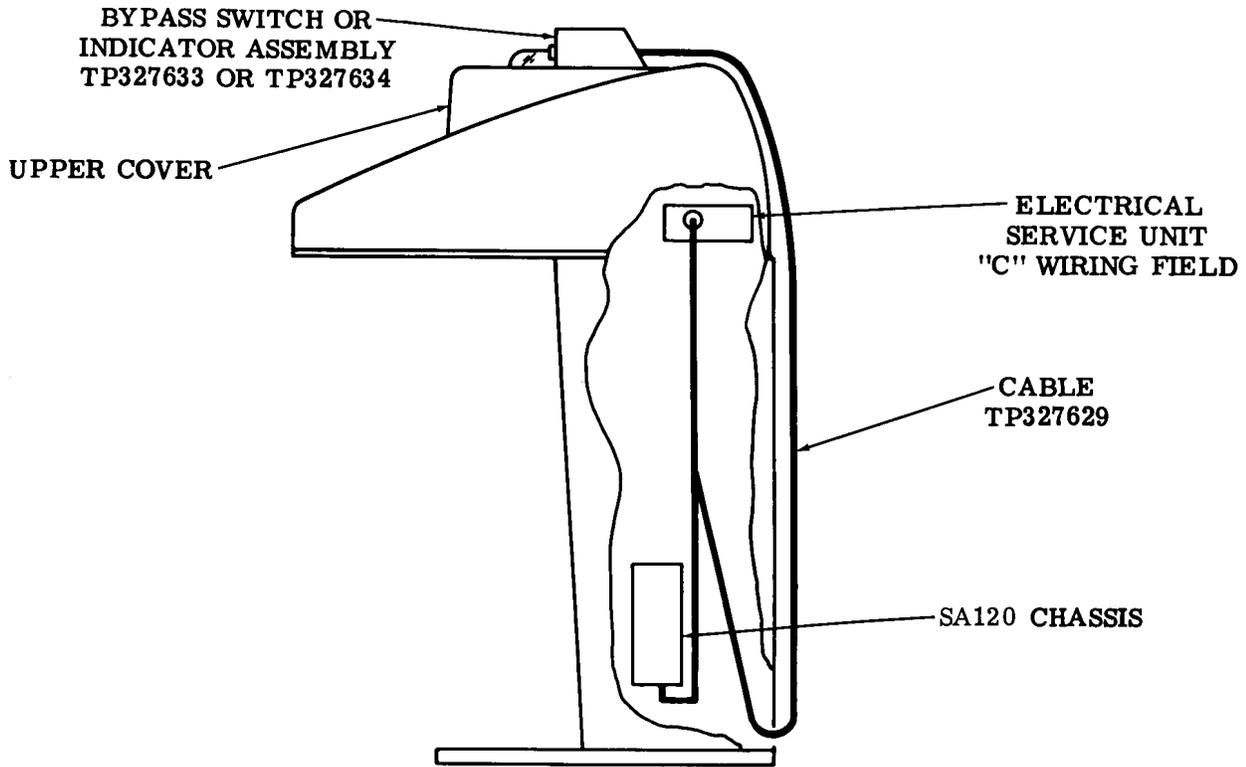
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BYPASS SWITCH OR
INDICATOR ASSEMBLY
TP327633 OR TP327634

UPPER COVER

ELECTRICAL
SERVICE UNIT
"C" WIRING FIELD

CABLE
TP327629

SA120 CHASSIS

Figure 19 - Location of SA120 Chassis and Bypass Switch or
Indicator Assembly on 35 Type Set

BYPASS SWITCH OR
INDICATOR ASSEMBLY
TP327637, TP327638,
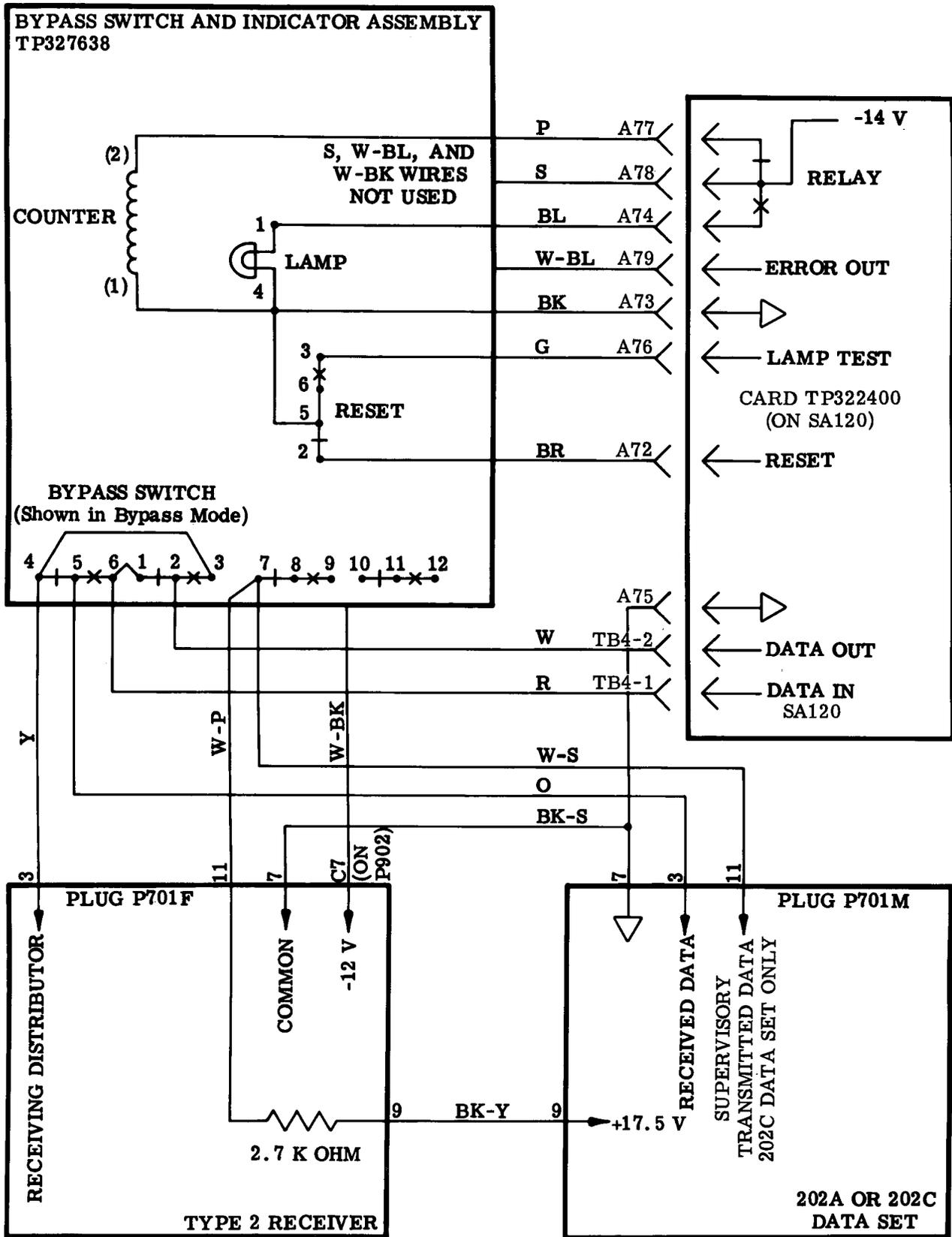TP327639, OR TP327640

CABLE
TP327647

DATA SET

SA120 CHASSIS

CABLE TP327648
OR TP327669
(Sender Only)
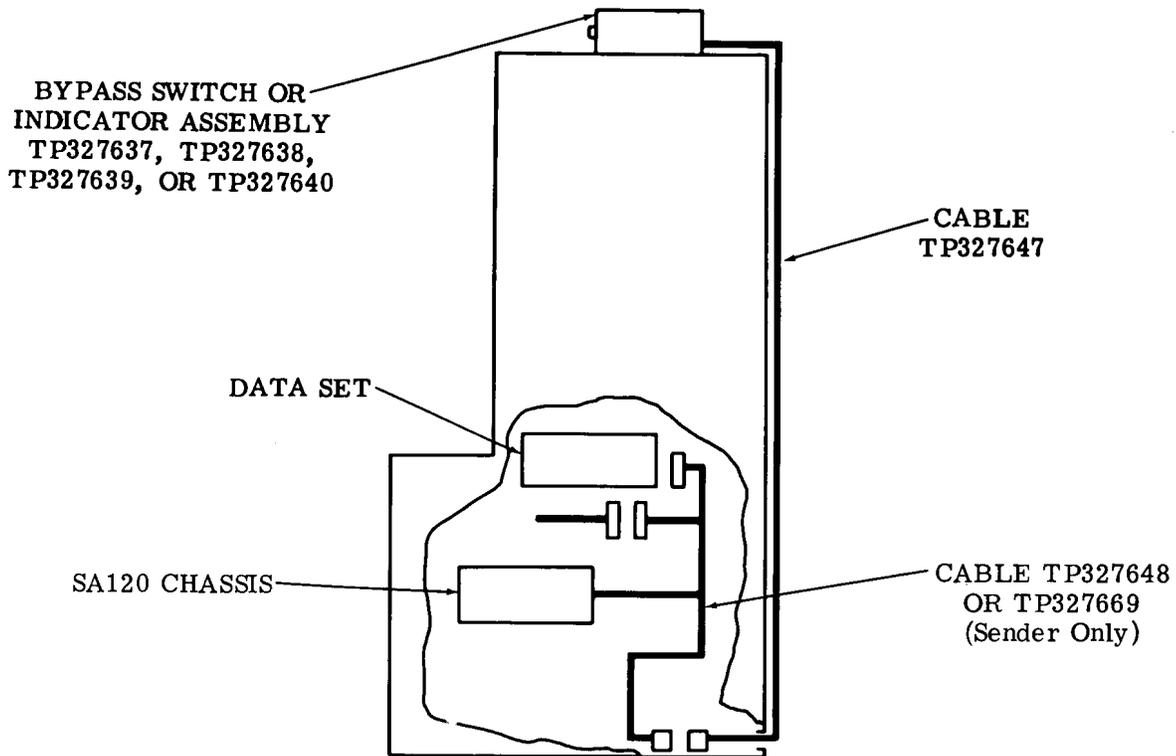
Figure 20 - Location of SA120 Chassis and Bypass Switch or
Indicator Assembly on Type 2 Sender or Receiver
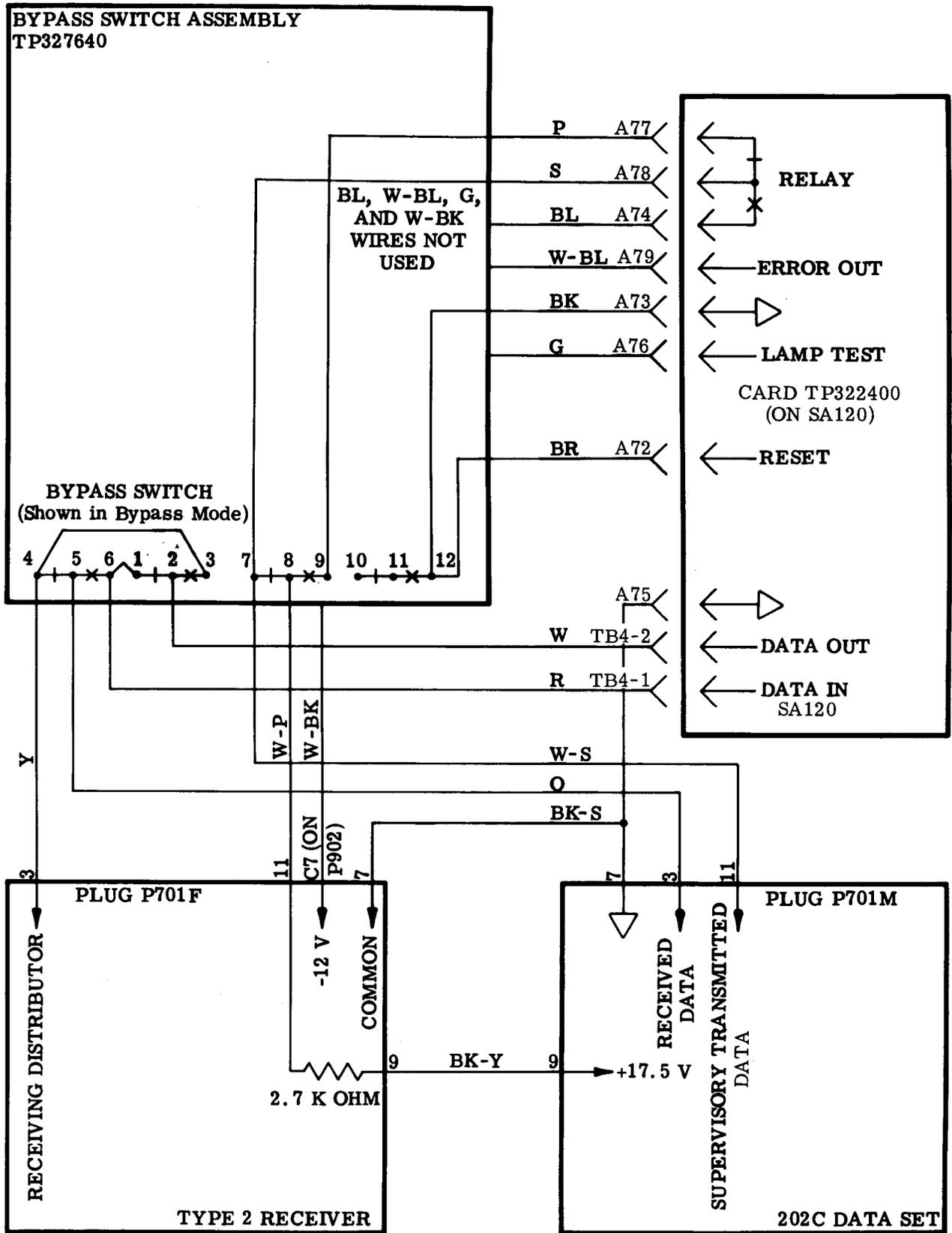
Figure 21 - Simplified Wiring for SA120EB

Figure 22 - Simplified Wiring for SA120EC

and fed out to the receiving distributor input of the terminal on the yellow wire. Since pin 2 is closed to pin 6, the data output of the SA120 (white wire) is connected to the data input of the SA120 (red wire). The white-purple wire brings +17.5 volts from the data set (via the Type 2 Receiver) to pin 7, where it joins the white-slate wire connected to the supervisory transmitted data input of a 202C data set. Reverse channel, if present, is therefore held on at all times regardless of the position of the bypass switch. (A 202A data set, which does not have reverse channel, has no connection to the pin that the +17.5 volts is wired to.)

(b) When SW1 is activated, the data set output at pin 5 (orange wire) is transferred to pin 6 (red wire) where it is supplied to the data input of the SA120. The data output of the SA120 (white wire) at pin 2 is transferred to pin 4 (yellow wire) where it is supplied to the input of the receiving distributor. This places the SA120 in series with the incoming data stream between the data set and the terminal, as for the TP327640 assembly. The low speed counter coil, DS2, and the lamp, DS1, are connected to the relay transfer contact in the SA120. When the relay is energized, this contact permits the counter to register the error (or error burst) and the lamp to light. Depending on the SA120 strapping, the lamp will flash on each error (or error burst) or latch on for the first error and flash off for each additional error (or burst). For each flash (on or off) of the lamp, the counter will register another count. As explained in 4.57, this count may be much less than the number of individual errors actually indicated by the SA120 because the time required to activate and deactivate the counter is much longer than the duration of a character. The reset switch, SW2, extinguishes the lamp when the lamp housing is depressed; the counter is mechanically reset to zero by its own pushbutton.

4.68    The wiring for bypass switch and indicator assembly TP327639, the SA120 chassis, the terminal, and the data set is shown in simplified form on Figure 23. Refer to 8717WD for a complete schematic and to 8567WD for actual wiring information.

(a) Bypass switch SW1 is shown in the bypass position on Figure 23. The wiring for it is identical to that for bypass switch and indicator assembly TP327638 (4.67 (a)).

(b) When SW1 is activated, the data set output at pin 5 (orange wire) is transferred to pin 6 (red wire) where it is supplied to the data input of the SA120. The data output of the SA120 (white wire) at pin 2 is transferred to pin 4 (yellow wire) where it is applied to the input of the receiving distributor. This places the SA120 in series with the incoming data stream between the data set and the terminal, as for the TP327640 and TP327639 assemblies. The lamp, DS1, is connected to the relay transfer contact in the SA120. When the relay is energized for the first time, this contact lights the lamp to indicate that an error was received. The SA120 is strapped so that the relay latches on the first error, holding the lamp on until it is reset by depressing the lamp housing (SW2).

4.69    The wiring for bypass switch and indicator assembly TP327637, the SA120 chassis, the terminal, and the data set is shown in simplified form in Figure 24. Refer to 8717WD for a complete schematic and to 8567WD and TP322423 for actual wiring information.

(a) Bypass switch SW1 is shown in the bypass position on Figure 24. The wiring for it is identical to that for bypass switch and indicator assembly TP327638 (4.67 (a)).

(b) When SW1 is activated, the data set output at pin 5 (orange wire) is transferred to pin 6 (red wire) where it is supplied to the data input of the SA120. The data output of the SA120 (white wire) at pin 2 is transferred to pin 4 (yellow wire) where it is supplied to the input of the receiving distributor. This places the SA120 in series with the incoming data stream between the data set and the terminal, as for the other Type 2 Receiver assemblies. The lamp, DS1, is connected to the relay transfer contact in the SA120 but the high speed counter coil, DS2, is not. Instead, the counter is driven by counter driver Z1, whose power comes from the Type 2 Receiver (-12 volts) and the SA120 chassis (+14 volts). When the first error is detected, the relay is energized and the energizing pulse is amplified and connected to the counter driver (via the white-blue wire) as the error out signal, causing the counter to register the error. The SA120 is strapped so that the relay latches for the first error and de-energizes and re-energizes for each additional error. The relay contact, therefore, lights the lamp for the first error and flashes it off and on again for each additional error. (This flash is so
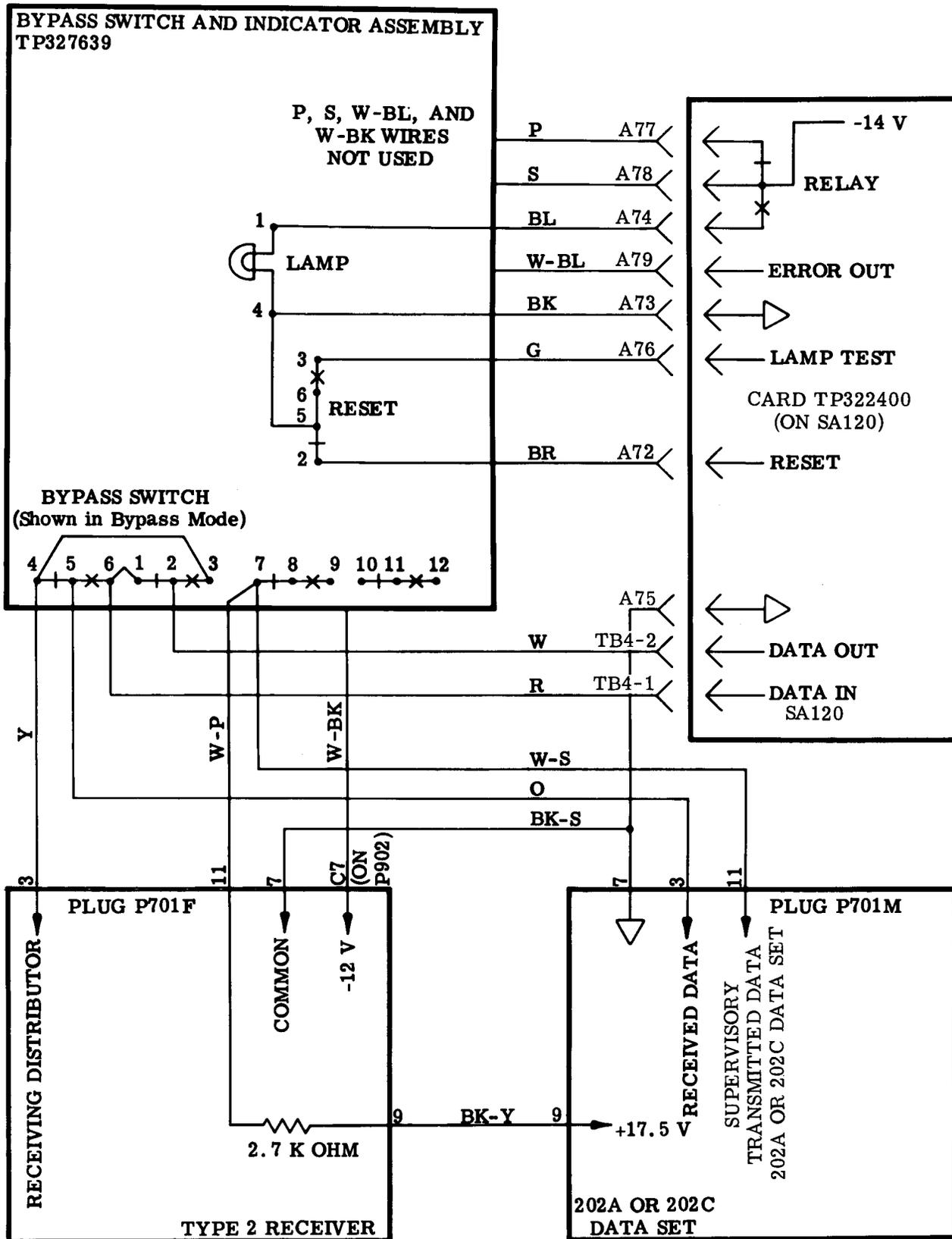
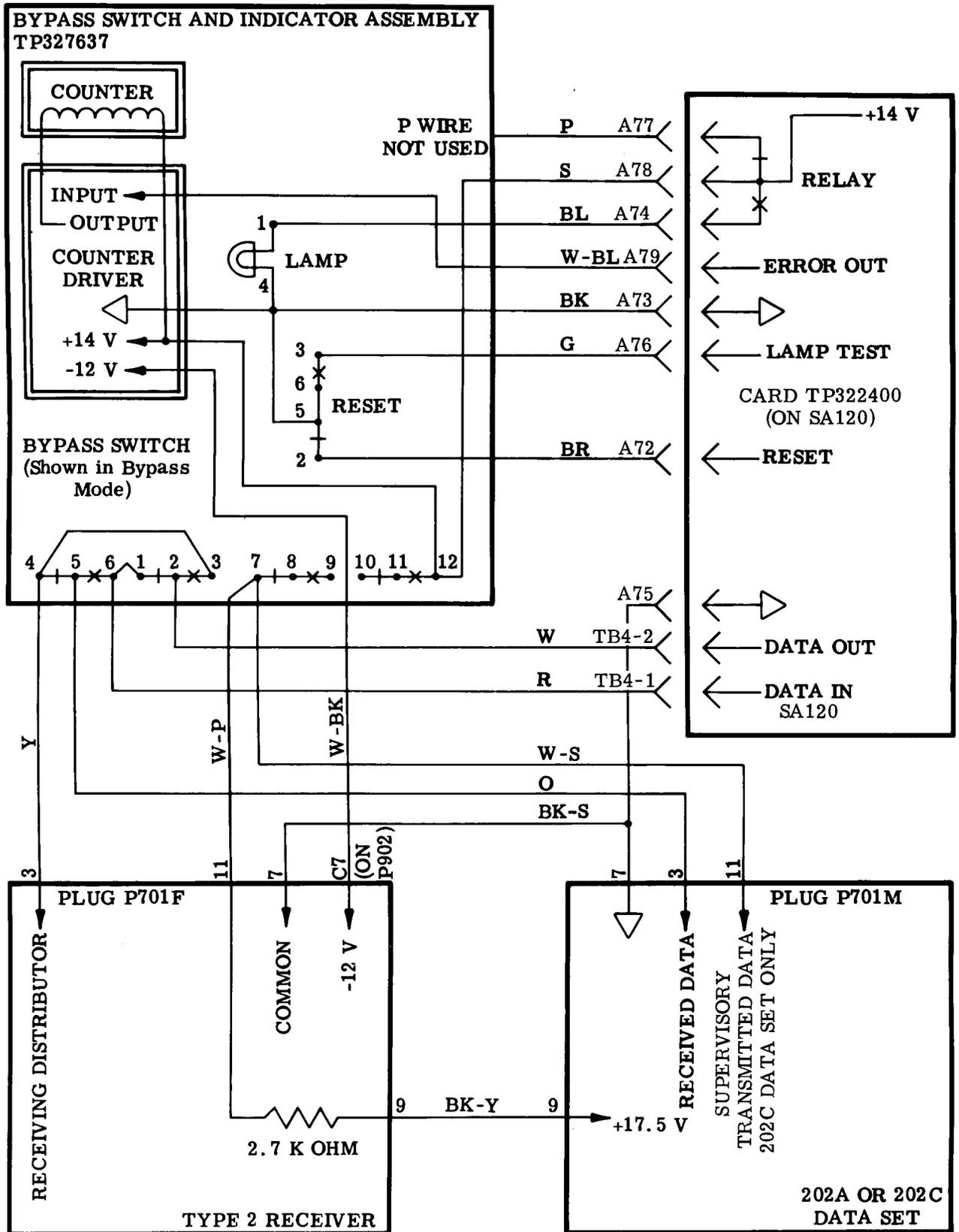Figure 23 - Simplified Wiring for SA120ED
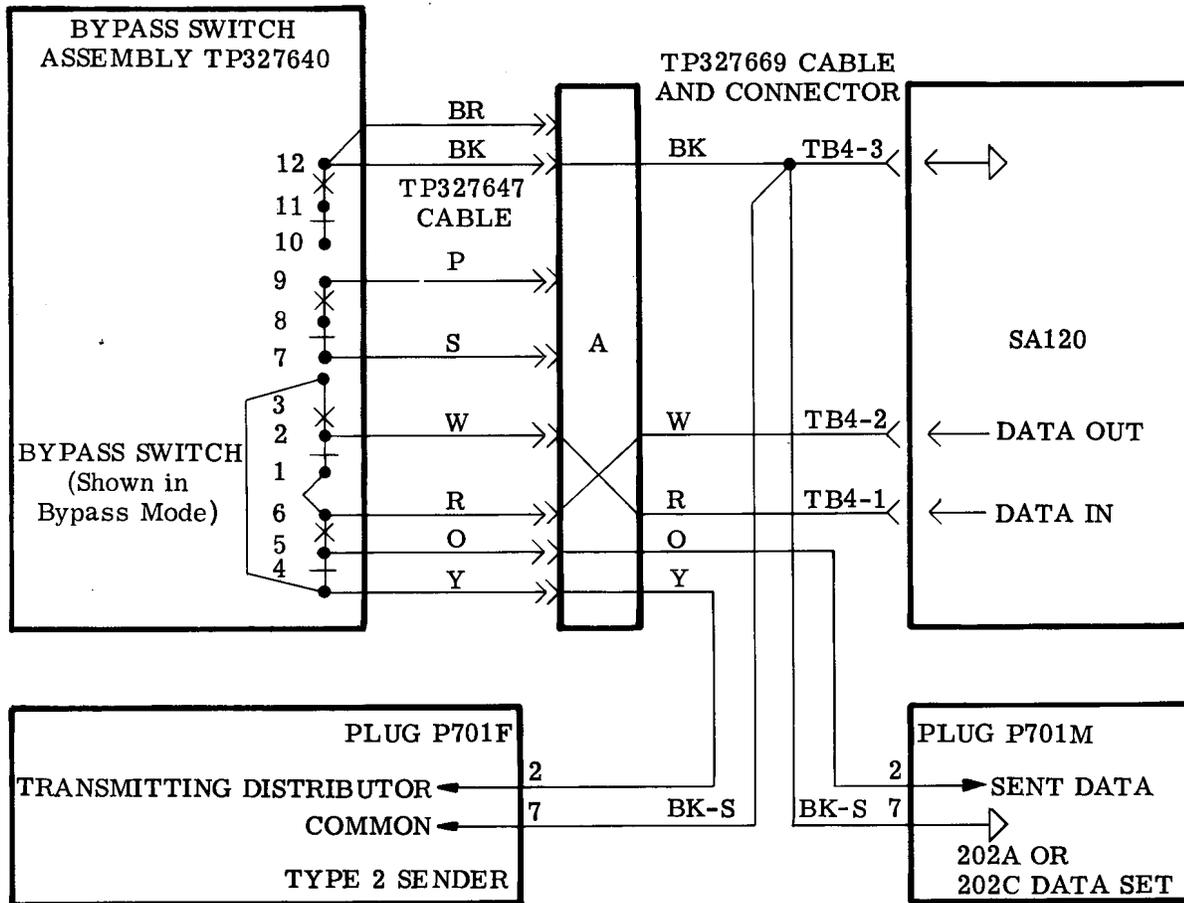
Figure 24 - Simplified Wiring for SA120EE

Figure 25 - Simplified Wiring for SA120FA

brief that it may not be seen.) For each flash of the lamp, the counter registers another count. The reset switch, SW2, extinguishes the lamp when the lamp housing is depressed; the counter is mechanically reset to zero by its own pushbutton.

4.70    The wiring for bypass switch assembly TP327640, the SA120 chassis, a Type 2 Sender, and its data set is shown in simplified form on Figure 21. Refer to 8717WD for a schematic and to 8567WD for actual wiring information.

(a)    Bypass switch SW1 is wired the same as for use on a receiver (4.65 and Figure 21). In the bypass position (Figure 25), the transmitting distributor output is fed in at pin 4 on the yellow wire, transferred to pin 5, and fed out to the data set input on the orange wire. The data output of the SA120 (white wire) is

connected to the data input of the SA120 (red wire) because the white wire of the TP327669 cable is connected to the red wire of the TP327647 cable by the TP327669 cable connector, A; this red wire is connected to pin 6 which is closed to pin 2, and the white wire connected to pin 2 is connected to the red wire of the TP327669 cable by connector A.

(b)    When SW1 is activated, the transmitting distributor output at pin 4 (yellow wire) is transferred to pin 2 (white wire) where it is supplied to the data input of the SA120 on the red wire. The data output of the SA120 (white wire) is supplied to the red wire connected to pin 6, where it is transferred to pin 5 and supplied to the input of the data set on the orange wire. This places the SA120 in series with the outgoing data stream between the terminal and the data set.