"DATASPEED®" PRINTER (RECEIVE-ONLY)

ELECTRONIC CIRCUITS

DESCRIPTION AND PRINCIPLES OF OPERATION

CONTENTS PAGE

1. GENERAL

1.01 This section contains the description and operating principles of the DATASPEED printer operator controls, data set interface, character generator, printer drive, power supply, ink heater and line feed bracket assembly, data simulator, and discrete calling generator modification kit. It is reissued to incorporate recent engineering and technical comments not previously presented. These engineering changes include a new built-in test character generation circuitry, redesign of the paper jam/paper-out alarm circuit to substitute a paper-out switch for detection of a paper-out condition using electronic logic, redesign of the line feed motor regulator circuit to allow increasing the fuse valve in the paper brake circuit, redesign of circuitry on the input logic card to reduce noise sensitivity, redesign of circuitry on the output logic card to reduce noise sensitivity and improve operation, redesign of the power supply to shut off the high voltage when the +6 v dc fuse is blown and to permit the high voltage to come on immediately after the interlocks are closed, and redesign of the paper winder circuit card to improve reliability. Since this is a general revision, marginal arrows ordinarily used to indicate changes and additions are omitted.

1.02 The DATASPEED printer operates from a signal source at 750, 1050, or 1200 words per minute (75, 105, or 120 characters per second) either directly or over telephone facilities. To interface with telephone facilities it may have its own data set (Figures 1 and 2) or it may be

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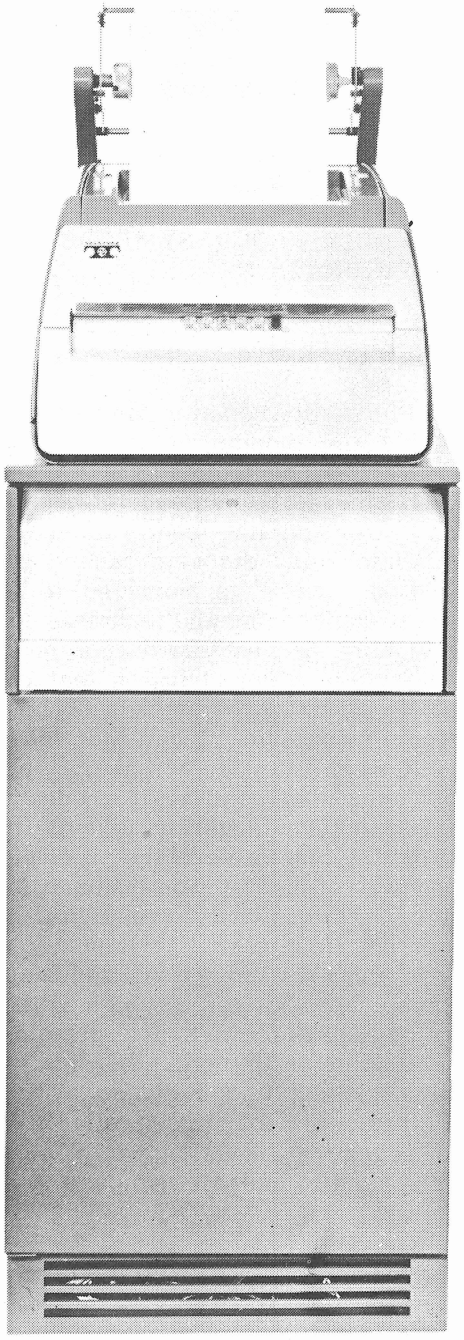


Figure 1 - DATASPEED Printer (Receive-Only) With Blank Front Panel

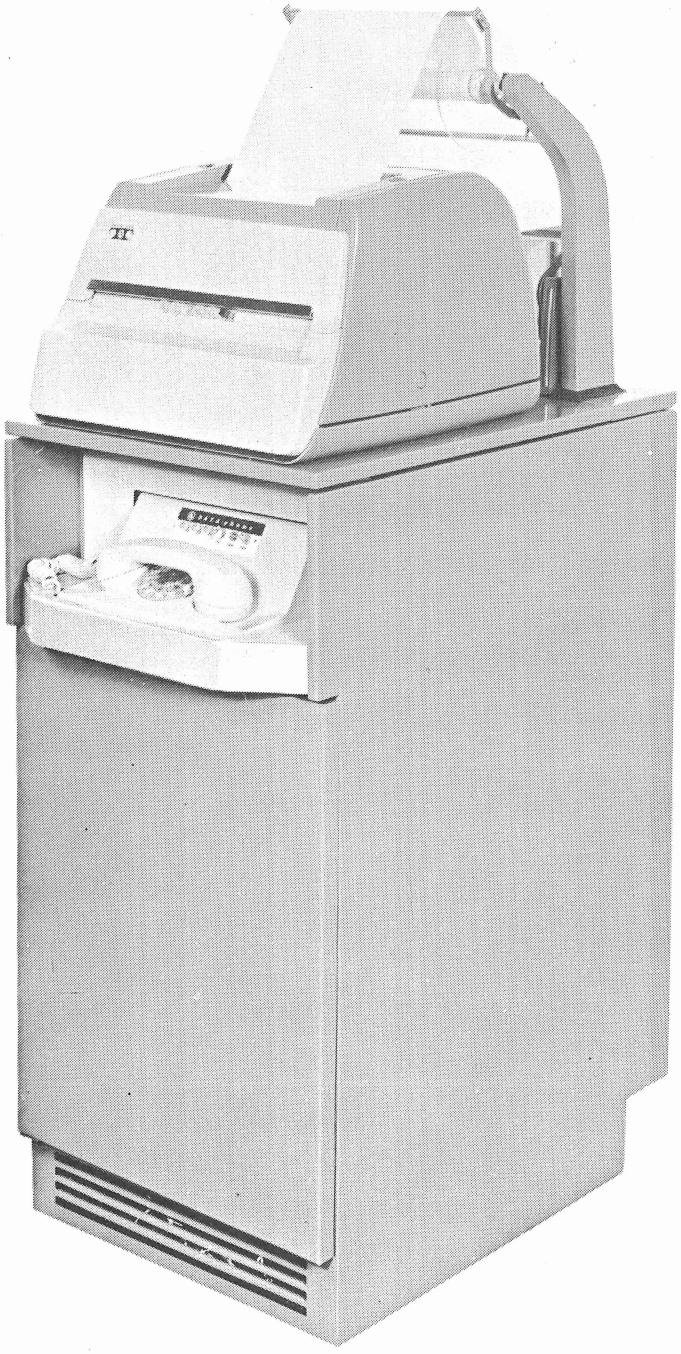


Figure 2 - DATASPEED Printer (Receive-Only) With Shelf for 202C Data Set or 804A Data Auxiliary Set

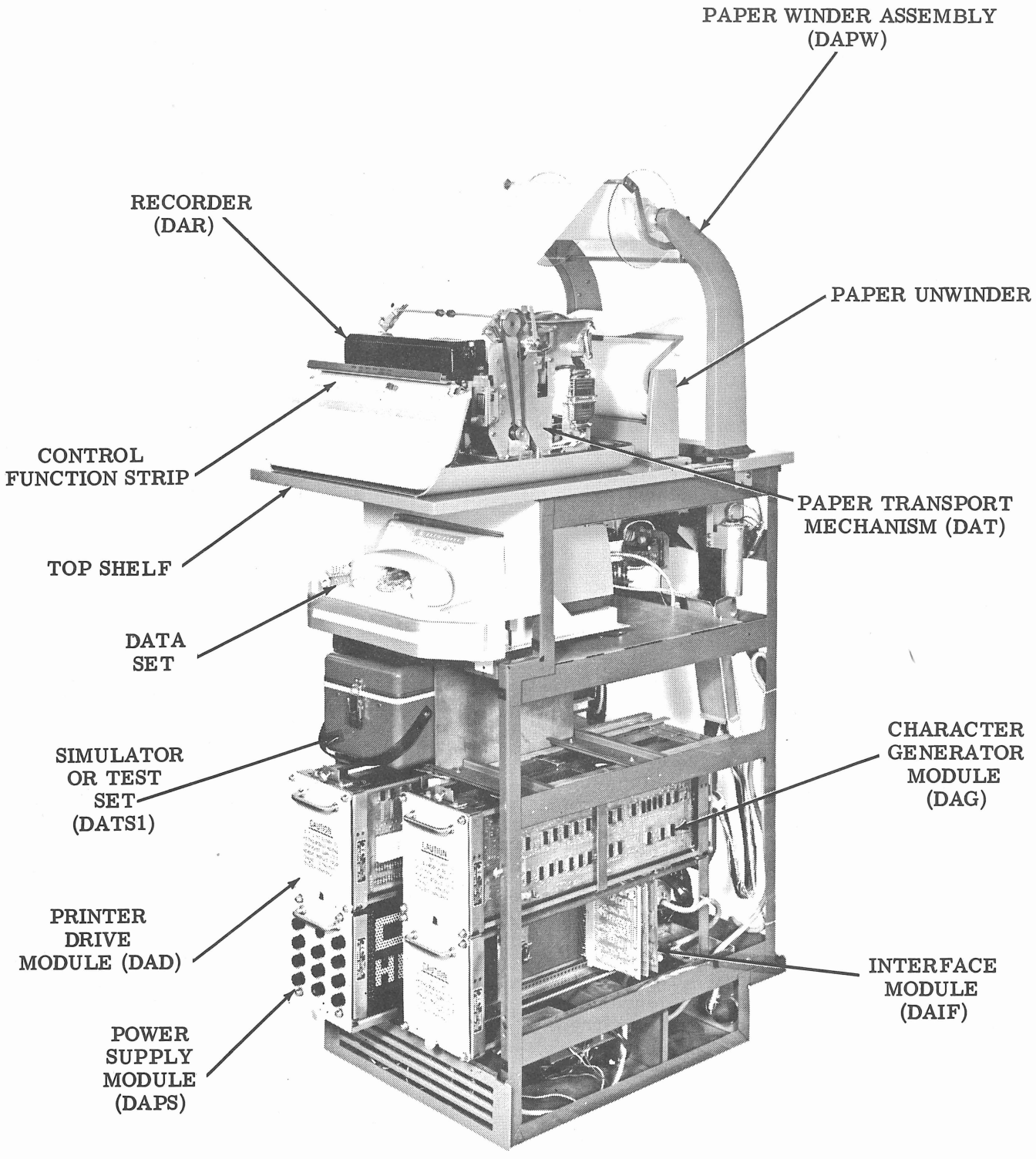


Figure 3 - DATASPEED Printer With Cabinet Panels and Cover Removed and Top Shelf and Modules Extended

connected to an external data set in a DATASPEED sender or receiver. The data set is not furnished with the printer in either case. Sets used with a serial interface operate at 1050 or 1200 wpm, and those with a parallel interface operate at 750 wpm.

1.03 The set consists of a cabinet containing the power supply and electronic modules plus space for a data set, with the page recorder and paper transport housed in a separate cover on top (Figure 3). A paper winder and unwinder are mounted outside the cabinet at the rear. Operator controls are located on a strip at the front of the cover. There are additional controls on the data set (if present) and inside the cabinet.

1.04 Power is supplied to the set from a 117 v ac line. High voltage is used in the recorder for printing. As a safety feature, two magnetic reed interlock switches are located inside the cover and one is located at the top center of each door opening to shut off the high voltage when any part of the cover is raised or the front or rear door is opened.

2. COMPONENTS

2.01 Most of the electronic circuits are contained in the following four modules: DAIF serial or parallel interface (may also contain discrete calling generator modification kit), DAG character generator, DAD printer drive, and DAPS power supply. The DAD and DAPS modules and DAG and DAIF modules are attached to each other vertically when installed in the set so they are drawn out together (Figure 3). Other circuits are located in the ink heater and line feed bracket assembly, which is mounted on the data set shelf (not visible in Figure 3).

2.02 Components are mounted on etched circuit cards of various sizes (except for the power supply), some extending the entire length of the module. Besides discrete components such as resistors, capacitors, and diodes, many cards contain miniature integrated circuits identified by ML numbers. These cards have MC designations while cards with only discrete components have EC designations.

2.03 Integrated circuits used in the modules are of two types: Logic functions (gates and flip-flops) and operational amplifiers (op amps). Logic circuits are digital devices; that is, they respond to and produce as outputs high or low voltage levels, or high-to-low or low-to-high transitions only. Op amps are linear devices and respond to a continuous range of voltages. All digital circuits used are compatible with the diode-transistor logic (DTL) family and all linear circuits are "709" type op amps. Schematic symbols, truth tables, and configurations of the various components are shown in Part 4.

3. OPERATION

3.01 Reference documents useful to understand the operation of the electronic circuits are listed on WDP0194.

3.02 Operation is described in the order a character follows from the time its signal appears at the interface until it is printed on the page. Refer to Figure 4 for a block diagram of electronic operation.

CONTROLS AND INDICATORS

3.03 The function strip of the DATASPEED printer is shown in Figure 5. The operator controls and indicators are as follows:

BREAK — A momentary pushbutton switch that turns off reverse channel when depressed to indicate that a break in transmission is desired. The button lights while it is depressed.

TRANS START — A momentary pushbutton switch that starts the discrete calling generator accessory (if present) which sends a discrete code sequence to start an unattended transmitter. The button lights while it is depressed and goes out when the sequence is finished.

PRINTER ON — An indicator and momentary pushbutton switch that lights when not depressed if the printer has all conditions necessary for printing (a supply of paper and all interlocks closed) and has its motors and high voltage on. The indicator lights when depressed if all interlocks are closed, whether the printer is ready to receive or not.

READY — An indicator and momentary pushbutton switch that lights when not depressed if the printer has all conditions necessary for printing and the high voltage is capable of turning on or is on. If an overvoltage condition should occur (excessive plate voltage on one or more high voltage tubes), the high voltage will be shut off and the READY lamp will go out. Operating the pushbutton resets the circuit, so the lamp will go on again if the overvoltage condition was temporary. How-

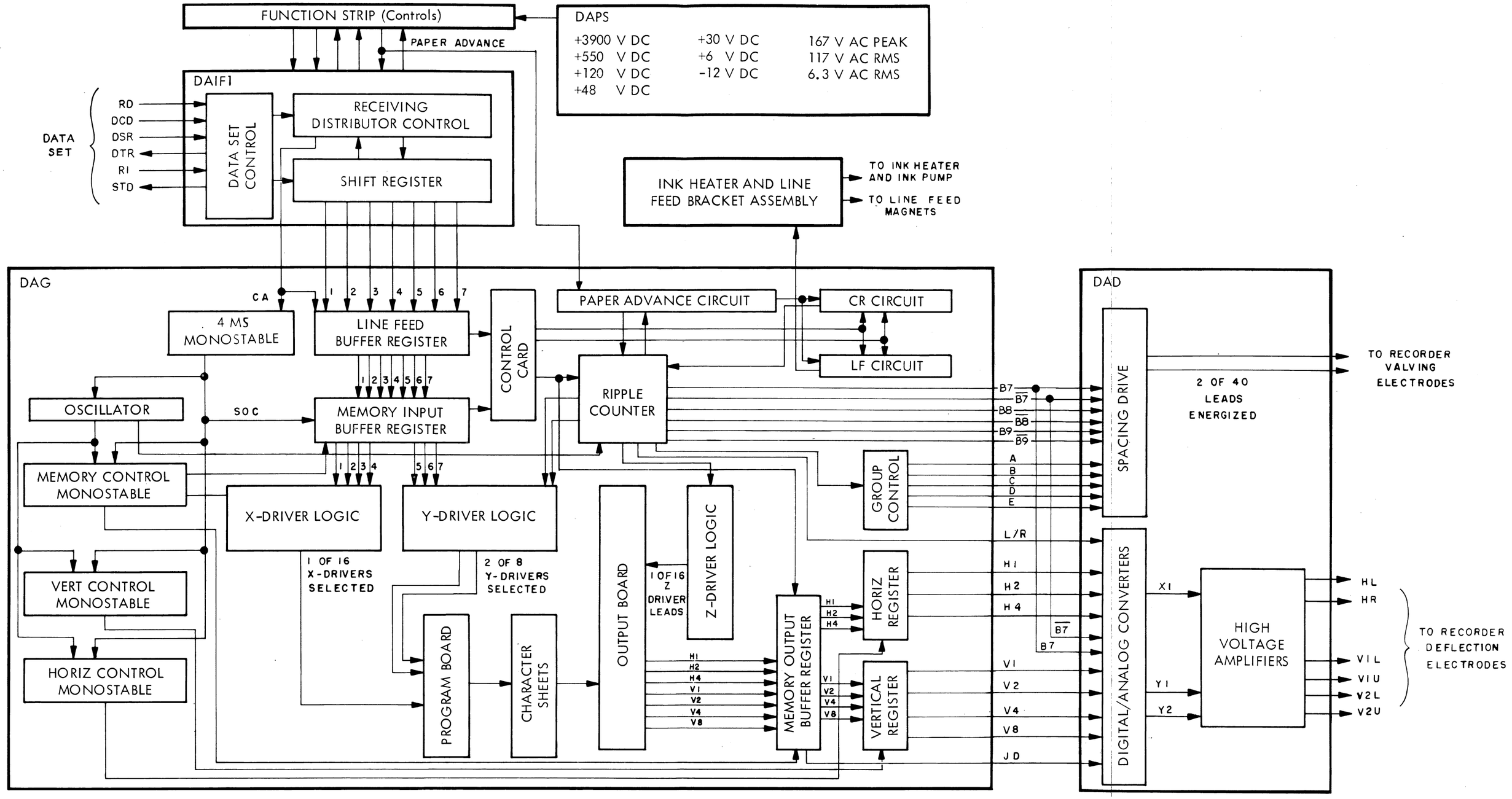


Figure 4 - Block Diagram of DATASPEED Printer (Receive-Only) Electronic Circuits (Serial Interface)

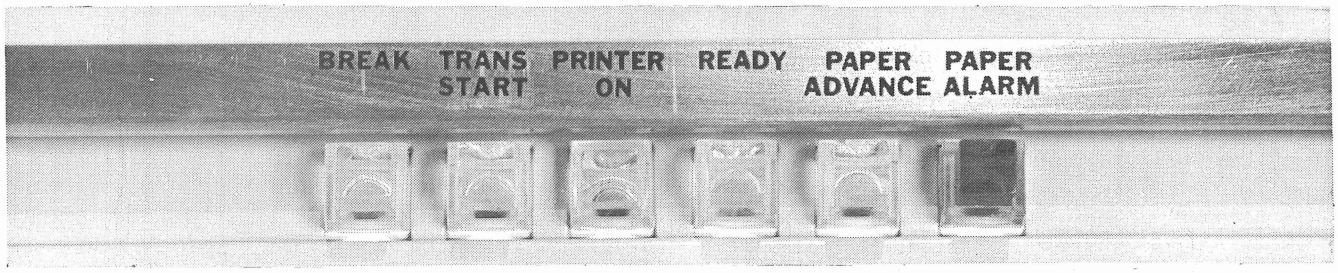


Figure 5 - Operator Controls (At Front of Cover)

ever, the READY lamp always lights while depressed to indicate that it is not burned out.

PAPER ADVANCE — A momentary push-button switch that feeds out paper. The button lights while it is depressed.

PAPER ALARM — A red indicator which lights when the paper supply drops below a specified level. The lamp may be tested by depressing the button; on late design units, depressing the button causes W test characters to be generated repeatedly.

The BREAK and TRANS START buttons are not used in private line installations.

3.04 In addition to the controls and indicators on the function strip, there are five others located as follows:

MAIN POWER — A toggle switch, located on the cabinet frame below the DAPS module. This switch turns on the 117 v ac power to cabinet.

NORM./TEST — A slide switch, located on the side of the DAIF module frame. This switch allows the printer to operate, when in the TEST position, regardless of the condition of the data set.

PAPER JAM/PAPER OUT ALARM — A red lighted pushbutton, located on top of the left side frame of the paper transport. The lamp lights to indicate a paper line feed failure, caused by paper being allowed to run out, breaking, or jamming. (On early design units, failure of the pre-paper puller motor will also cause an alarm to be indicated.) This alarm occurs on early design units if the paper storage loop is not renewed within 28 to 29 line feed steps (normally the pre-paper puller motor renews the paper storage loop after 18 line feed steps, resetting the alarm circuit) or the pre-paper puller motor runs more than 480 milliseconds; on late design units, this alarm occurs if the paper-out switch operates or the pre-paper puller motor runs more than 1.2 seconds. In either case, when an alarm condition occurs the READY light on the control strip will go out, the paper jam/paper-out alarm lamp will light, and the printer will become inoperative. The PAPER ALARM lamp may be lighted also. Depressing the paper jam/paper-out alarm pushbutton after the condition has been corrected resets the printer and extinguishes the red light.

OVERRIDE — A pull switch located on the lower front of the cabinet frame, by the lower door hinge, in back of the front door. The switch overrides (bypasses) the interlock switches for the front and rear doors when extended forward, permitting the printer to be turned on manually for servicing when the front door is open or removed.

HIGH VOLTAGE POWER ON — A red indicator, located on the faceplate of the DAPS module. It is behind the front door and will be visible only when the door is open and the override switch is operated. This indicator lights when the high voltage is on.

INTERFACE

3.05 The printer is available with either of two interfaces, serial or parallel, housed in the DAIF module. The serial interface (DAIF1) is used where the transmitted data is in serial

form. It provides operation at 1050 and 1200 wpm when used with a 202C or 202D data set or equivalent. The parallel interface (DAIF2) is used in installations where the incoming data is in parallel form. It provides operation at 750 wpm when used with a 402D data set or equivalent. Modification kits are necessary to interface with type 2 or type 5 DATASPEED sets, and an accessory is available to provide the discrete calling feature. Late design units include a test character generator circuit.

A. DAIF1 Serial Interface

General

3.06 The DAIF1 interface has one mode of operation, serial receive only. It provides the station controls and signal conversion necessary to enable data interchange between a signal source such as a 202C or 202D data set or equivalent and elements of the high speed printer. The interface converts data from polar serial start-stop form to neutral parallel (voltage) form. The baud rate is fixed by the interface crystal oscillator frequency. The data output of the interface, applied to the character generator module (DAG), consists of a seven-bit parallel data signal plus a character available signal.

3.07 Both the printer and the sender are controlled by the interface in either the attended or unattended mode of operation. The interface signals the printer to turn on its motors and enables data to flow only if the printer indicates that it is ready to receive. If the printer cannot receive, the interface signals the sender that no data should be sent.

3.08 The interface is insensitive to character code and can be wired for 5-, 6-, 7-, or 8-level characters enclosed in a 7.00-, 7.42-, 8-, 9-, or 10-unit frame. Its parallel output can be shifted to handle the 5-level code for typesetting by means of a jumper clip arrangement so that levels 2 through 6 are received in level positions 1 through 5.

3.09 Power requirements for the interface are as follows:

+6.0 ± 0.6 v dc at 0.500 amp
-12.0 ± 1.2 v dc at 0.150 amp
+18.0 ± 1.8 v dc at 0.060 amp
+48.0 ± 6.0 v dc at 0.200 amp
117 ±10 v ac, 60.0 ±0.5 Hz at 1.0 amp

3.10 Input signals from the signal source must conform to EIA Standard RS232-B (+5 to +25 v for a space or on condition and -5 to -25 v for a mark or off condition). Output signals to the printer are +6.0 ±0.6 v for a mark or off condition and 0.0 ±0.5 v for a space or on condition. These signals will have less than 45 percent distortion per bit and 5 percent distortion per character. Output signals to the signal source are +6.0 ±0.6 v for a space or on condition and -12.0 ±1.2 v for a mark or off condition.

3.11 There are six options for the DAIF1 interface, excluding variations in bit timers for different operating speeds. All are strapping options, as follows:

DU — for operation on a dial-up or switched network

PL — for operation on a private line or dedicated network and direct interface to a DATASPEED Type 2 Sender

XW — for operation with ASCII (United States of America Standard Code for Information Interchange) or with 7.00- or 7.42-unit Baudot code and 10-unit Baudot code not compatible with DATASPEED senders and receivers

XX — for operation with 10-unit Baudot code, DATASPEED compatible

The other two options, AW and BW, are present only on late design units equipped with the test character generator card MC192:

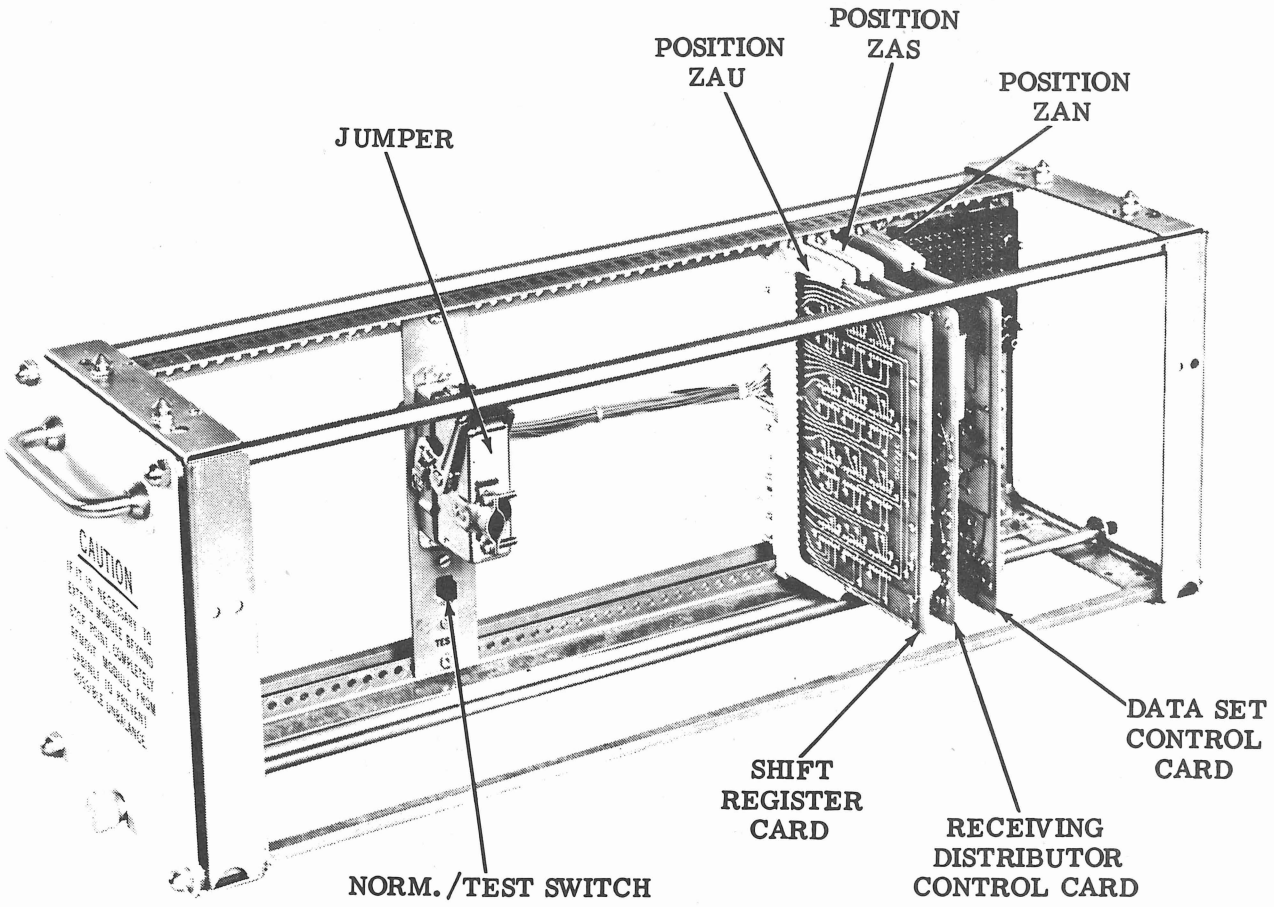
AW — ASCII W

BW — Baudot W, 2

Physically, the interface consists of three etched circuit cards with integrated circuit and discrete components (in positions ZAU, ZAS, and ZAN) and a NORM./TEST switch (Figure 6). On late design units an additional circuit card is present in position ZAW (not shown in figure).

Dial-Up Operation

3.12 If the data sets at the printer and remote sender are equipped with handsets, calls may be originated manually at either the printer or remote sender. With both data sets in the talk mode, the calling station dials the other station. When the called station answers, if the operators agree to go into the data mode, the



(Right Side View)

Figure 6 - DAIF1 Serial Interface Module

called station must go into the data mode first. When the calling operator hears the 2025 Hz recognition tone, the calling station must be placed into the data mode before the tone ends or the call will be dropped.

3.13 In the data mode, the printer data set turns on the data set ready (DSR) lead to the DAIF1 interface. The interface then turns on the receive message (RM) lead to the printer and starts the 15-second on-hook timer in the interface. When the sender turns on its data carrier, the printer data set turns on the data carrier detector (DCD) lead to the interface, disabling the 15-second timer and enabling the receive data (RD) input to the interface. The DCD lead must turn on before the timer times out or the call will be dropped.

3.14 When the printer turns on, it enables the ready lead to the interface. This turns on the supervisory transmitted data (STD) lead to the data set, which turns on reverse channel sender (RCS) to the printer if the data set is so equipped. Data transmissions may now take place.

3.15 For unattended operation, the data set must be in the auto mode and the printer must be capable of receiving data (DTR lead on). When the incoming ring signal appears on the line, the data set turns on the ring indicator (RI) lead to the interface and switches to the data mode. The data set turns on the DSR lead to the interface and sends a 2025 Hz recognition tone to the sender. The rest of the turn-on sequence is as described for manual on-line operation.

3.16 Turn-off for either manual or unattended operation occurs when the data carrier is absent for more than about 15 seconds. The data set turns off the DCD lead to the interface about 15 milliseconds after the data carrier ceases. This starts the 15-second timer in the

interface, which times out and shuts off the DTR lead to the data set. The data set drops the call, turning off its RCS and DSR leads, so the interface turns off the RM lead to the printer. The printer shuts off its motors, high voltage, and PRINTER ON lamp. This turns off the ready lead to the interface, so the interface turns off the STD lead to the data set. The printer is now ready for another call.

Private Line Operation

3.17 In private line operation, no handset is used with the data set. Consequently, the data set is permanently on line and the data set ready (DSR), data terminal ready (DTR), and ring indicator (RI) signals are not used. Data carrier detector (DCD) is the main controlling signal. The sender activates the printer by placing the carrier on line, causing DCD to come on to the interface. Line feed signals must not be sent for at least 1/3 second in order to give the motors time to reach operating speed.

3.18 When DCD turns on, it causes the interface to enable the receive data (RD) input and turn on the private line-receive message (PL-RM) lead to the printer. The printer responds by turning on its motors, high voltage, and PRINTER ON lamp. This turns on the ready lead to the interface, enabling the supervisory transmitted data (STD) lead and providing reverse channel to the sender, if the data set is so equipped.

3.19 At the end of the message, the sender turns off the carrier. This disables the DCD and PL-RM leads, and the printer shuts off. The printer is now ready for another message.

Detailed Circuit Description

3.20 For details of the circuitry, refer to wiring diagrams 8251WD (serial interface schematic), 8263WD (serial interface master reference), 322130 (MC130 shift register card), 322180-87 (MC180-87 receiver distributor control cards), 322132 (202C and 202D data set control RO card), 322192 (MC192 test character generator card — late design units only), and 8260WD (timing diagram). Wiring diagram 8251WD is not a complete schematic, and must be supplemented by the master reference wiring diagram (containing notes) and the three individual circuit card drawings (containing the schematics for the circuitry on the cards).

3.21 References to components in this description are abbreviated as follows: XZAN, XZAU, XZAS, and XZAW (late design units only) refer to the terminals on the cards in positions ZAN, ZAU, ZAS, and ZAW, respectively, and ML1, ML2, etc, refer to specific integrated circuit components. The number following an XZ or ML designates an associated terminal or pin. For example, "XZAN-18, ML2-3, MC132" refers to terminal 18 on card MC132, located in position ZAN, which is connected directly to pin 3 on circuit ML2. The drawing of card MC132 shows that circuit ML2 is three three-input NAND gates. All "gates" mentioned in the description are NAND gates unless stated otherwise, and all references to MC180 apply to cards MC181 through MC187 as well. Refer to the appendix (Part 4) for schematic symbols and truth tables for the integrated circuits.

3.22 Logic signals, unless otherwise noted, are either +6 v (high) or 0 v (low). The on or off condition of a circuit element varies with its function and is defined separately.

Turn On Sequence

3.23 The NORM./TEST switch must be in the NORM. position. This enables the receive message (RM) lead, XZAN-18, MC132, which connects to the auto on relay driver input.

3.24 The DAIF/AAA interface turns on (+6 v) the data terminal ready (DTR) lead, XZAN-33, if:

(1) Disconnect lead XZAN-32 is high (positive) at ML1-4, MC132. This indicates a general ready condition at the printer; cabinet closed, some paper available for printing.

(2) Selectable lead XZAN-12 is low (zero) at ML1-10, MC132. This indicates that there is a predetermined amount of paper on the supply roll. The low at ML1-10 produces a high at ML1-8. This high is applied to ML1-3.

Note: If the paper supply is below the predetermined level the selectable lead goes high (positive) and turns the DTR lead off (-12 v) before the printer answers a new data call. However, the selectable lead cannot turn off the DTR lead once a call has been established.

(3) The on-hook timer (OP1-6, MC132) is high (+6 v) at ML1-5. (OP1-6 is high when the timer is initially set.)

With high signals at all three input leads, ML1-6 is low and Q2 saturates to provide +6 v at the DTR lead.

3.25 The high at ML1-8 also appears at ML2-1. Thus, a data set ready (DSR) signal from the data set, applied to ML2-2, will cause ML2-3 to go low. The RM lead, XZAN-18, goes low, turning on the printer.

3.26 The low at ML2-3 causes ML2-11 to go high, placing a high on ML3-1. With no data carrier detector (DCD) signal from the data set, XZAN-25 is low, forcing ML2-8 high to place a high on ML3-2. With highs on both of its inputs, ML3-3 goes low. This forces ML2-6 high and causes OP1-6 to start timing out.

3.27 The DCD lead, XZAN-25, must be turned on (positive) within 15 seconds after the DSR lead turns on. ML2-8 then goes low, causing ML3-3 to go high and ML2-6 to go low, resetting OP1-6. If the DCD lead does not turn on within the 15-second interval, OP1-6 will time out and produce a low at ML1-5. This forces ML1-6 high, cutting off Q2 and turning off the DTR lead.

3.28 Assuming the DCD lead has turned on within the timing limit, it forces ML3-11 high. The high at ML3-11 is gated with ML3-8, which is high unless the data set is in an answering sequence. These two highs enable ML1-12, so that the output receive data (RD) lead, XZAN-16, is dependent on the incoming data at ML1-13.

3.29 The ring indicator (RI) lead, XZAN-26, is normally off (negative) and goes on (positive) only when the data set is ringing. Gated with the high from ML3-11, the RI signal forces ML3-8 low. This inhibits the RD gate, ML1-12, during the answering sequence of the data set or associated equipment. Once the call is answered the RI lead goes off (negative), forcing ML3-8 high and enabling ML3-6 and ML1-12. Thus, to permit a data transfer from the RD input (XZAN-24) to the RD output (XZAN-16) of the control unit, XZAN-26 (or XZAN-4 in private line installations), must be held low.

3.30 In installations where it is desirable for the data set to inform the sending station that it is ready to receive data, a signal may be obtained for this purpose at the supervisory transmit data (STD) lead, XZAN-29. The auto-on relay in the printer grounds the ready lead, XZAN-28, causing Q1 to conduct and thus turning on the STD lead to the data set.

Bit Timer

3.31 A bit timer on the MC180-187 control card consists of a free-running crystal oscillator, four control gates, six J-K flip-flops, which provide a divide-by-64 logic function, and a clocked flip-flop for pulse shaping.

3.32 The output of the oscillator, at the collector of Q1, card MC180, is applied to ML8-3, which provides isolation and pulse shaping. ML8-4 is applied to the clock pulse input of ML2, the first stage of the divide-by-64 counter. With no incoming information on the RD line, XZAS-B3, counter stages ML2, ML1, and ML3 are disabled by the low applied to their clear direct (CD) inputs by ML8-6. Thus, the output at ML3-8 is low. Flip-flop ML6 is also disabled by a low applied to its CD input by ML14-3, so the ML6-6 output is low.

3.33 To initiate the bit timer operation, ML8-6 must go high and remain high for the duration of the bit timer cycle. Once this condition is satisfied, the timer begins a counting sequence. Gate ML14-3 goes high and unclamps the clear direct of ML6. Gate ML14-6 now controls the clear direct of ML6. The output at ML6-6 remains low. The first negative transition of the oscillation at ML8-4 will shift the state of ML2-6, and each ensuing negative transition at ML8-4 will advance the counter one count. At a 1050 baud rate the output of the last counter stage, ML3-8, will go low exactly 476 microseconds after the first negative transition appears at ML8-4. The low at ML3-8, applied to the clock pulse input of ML6, causes the flip-flop to change states. ML6-6 goes high and remains high. The clear direct on ML6-5 was disabled by the initial action of the counter. At the instant ML3-8 goes low, all binary outputs of the counter are low. The next negative transition at ML8-4 resets ML2-6 high. The following high at ML8-4 is gated with the high at ML2-6 through ML14-6 to produce a low at ML6-5, resetting the flip-flop so that ML6-6 is low.

3.34 To stop the counter and associated circuitry, ML8-6 must go low.

3.35 The oscillator and associated counter is essentially free running and generates pulses approximately 11 microseconds in duration every 476 microseconds for operation at a 1050 baud rate. This rate is established by the frequency of the crystal used in the oscillator circuit. The crystal can be changed to provide the pulse delays and pulse durations required for other baud rates.

Receive Data

3.36 With no input data the RD lead, XZAN-24, MC132, is low, corresponding to a stop pulse (mark) from the data set. This is gated through ML1-12 to provide a high at XZAN-16. This high is applied to the RD lead of the receiving distributor control card, XZAS-B3, MC180, preventing the distributor from generating any control signals.

3.37 When a start pulse (space) is applied to XZAN-24, MC132, the XZAN-16 lead goes low. This low is applied to XZAS-B3, MC180, and also to XZAU-B29, MC130. The low at XZAS-B3 forces ML14-11 high. This causes ML8-8 to go low, which forces ML8-10 high. The SE lead, XZAS-B2, is strapped to ground, giving a high at ML8-12, so the signal at ML8-10 is in control of the wired OR gate and ML14-10 at all times. XZAS-A34, the receive message (RM) lead is also strapped to ground, giving a high at ML4-6 and at the R+ lead, XZAS-A35, at all times. With both ML14-9 and ML14-10 high, ML14-8 goes low and forces ML8-6 high. This starts the operation of the bit timer as explained in 3.32.

3.38 When ML8-8, MC180 is low, due to a low at XZAS-B3, the CD input to ML5 is enabled (high). ML6-6 goes from low to high, and this high appears at ML4-13. Gated with the high at ML4-12, it forces ML4-11 low. This low causes ML10-6 and ML10-8 to go high. The high at ML10-8 is applied to ML12-10, and is gated with the highs at ML12-12 and ML12-13 to force ML12-8 low. This low, applied to ML7-13, forces ML7-11 high. It is also transferred to XZAU-A30, MC130, the register reset (RR) lead of the shift register, where it resets all of the register flip-flops except ML4. The outputs (pin 6) of all flip-flops except ML4 on the MC130 card are now high.

3.39 The nine highs from the flip-flops of the shift register are gated together on the MC180 card by ML11-2, 3, 5, 6, 9, 10, 12, and 13, and ML12-2. This forces ML12-6 low. The low at ML12-6 appears at ML12-13 and causes ML12-8 to go high, removing the reset. Approximately 300 nanoseconds elapse from the time the reset is initiated to the time the reset is decoded and removed.

3.40 Approximately 10 microseconds after ML6-6 on card MC180 goes high, ML8-4 and ML2-6 are high and ML14-6 goes low. This places a low on the clear direct of ML6, forcing ML6-6 low. ML6-6 going low forces ML4-11 high, and this high causes ML10-6, the clock pulse (CP) lead, to go low. The pulse is applied to XZAU-B30, MC130, transferring the start signal, the low at XZAU-B29, and the high at XZAU-B31 into ML9. When this occurs, ML9-6 goes from high to low. The clock pulse also transfers the high at ML8-6 to ML4-4. ML4-9, $\overline{ST}$ is now low, and this low is applied with the low at ML9-6 to terminals 1 and 13 of gate ML13 on card MC180. This forces ML13-12 high.

3.41 When ML6-6 of card MC180 goes low, it also flips ML5-9 from high to low. This low appears at ML4-12 and holds ML4-11 high until ML6-6 goes through another high-to-low transition. The result is a high-to-low transition (a clock pulse) at ML10-6 for every other cycle of ML6-6. Thus, ML6-6 operates at twice the bit rate and ML5-9 effectively divides this rate in half to match the bit rate of the incoming information.

3.42 As long as ML13-12, MC180 is high, ML8-2 will be low, ML14-8 low, and ML8-6 high, keeping the bit timer on. At the same time, ML13-8 is low, forcing ML7-8 high and holding the character available timer (Q4) off by producing a low at ML9-6. The low at ML13-8 disables the RR lead, ML12-8.

3.43 When a start bit (space) is shifted into ML4, MC130, and a stop bit (mark) is shifted from the RD input (XZAU-B29) into ML9, the SP and $\overline{ST}$ inputs at pins 1 and 13 of ML13, MC180, are both high. This forces ML13-12 low, so ML13-8 and ML8-2 are forced high. With ML8-2 high, the mark (stop bit) on the RD lead (XZAS-B3) forces ML8-8 and ML8-11 high. This causes a low at ML8-10 and a high at ML14-8. The high at ML14-8 also holds ML14-1 high, and the second crystal output after it appears turns ML14-2 high also. When this occurs it forces ML14-3 low, placing a low signal on the direct clear input (5) of ML6, causing ML6-6 to go low. Before ML6 is cleared, both

inputs (13 and 12) of ML4-11 are high, making its output low, but when ML6-6 becomes low, ML4-11 goes high. This causes ML10-8 to remain low, preventing a reset of the input register. The high at ML13-8 is gated with the high at ML7-6 to produce a low at ML7-8, forcing ML9-8 and ML9-6 both high (through an external strap).

3.44 The high at ML9-6 triggers the 100 microsecond timer, Q4 and associated components, which times out and then produces a brief positive pulse (approximately 5 microseconds). This positive pulse is inverted by Q3, producing a negative pulse at ML9-1 and ML4-2 (early design units only). On early design units, the corresponding high at ML4-3 is gated with the high at ML12-12 to force ML4-8 low. This produces a character available (CA) signal at XZAS-B26. Although the low is present at ML4-8 for only about 5 microseconds, the high at ML4-3 and the resultant low at ML4-8 are held for approximately 20 microseconds because of the charge time of C5 at ML4-1. The low at the Q3 collector also forces ML9-3 high, and ML9-11 then goes low to prevent another pulse from the 100 microsecond timer. On late design units, the high at ML9-8 is gated with the high from ML9-11 to cause a low at ML4-3. This produces a character available (CA) signal at XZAS-B26. When the 100 microsecond timer, Q4 and associated components, completes its timeout period, ML9-1 goes low causing ML9-3 to go high. This sets the flip-flop, making ML9-11 low and ML4-3 high and removing the character available signal. The high output of ML9-3 is inverted by ML4-8 to prevent another pulse from the 100 microsecond timer. (The significance of this change is that on early design units, the CA pulse is delayed by 80 microseconds (typically) and is approximately 20 microseconds long, while on late design units, the CA pulse is not delayed and is approximately 80 microseconds long.) On both early and late design units, the ML9-3, ML9-11 flip-flop is reset when the next start pulse appears at the RD input. ML7-8 goes high when ML12-8 goes low, and the cycle begins again to present a new character in parallel form.

Turn Off

3.45 When the DCD lead, XZAN-25, MC132, turns off, it causes ML2-6 to go high. The on-hook timer, OP1, times out and forces ML1-5 low, turning off (-12 v) the DTR lead, XZAN-33. The low on the DCD lead also disables the RD gate by placing a low on ML1-1. Thus, the RD output at XZAN-16 goes high and remains high. This high stops MC130 and MC180 from cycling.

3.46 When DTR turns off, it causes the DSR lead, XZAN-27, MC132, to go low (-12 v). DSR low forces ML2-11 high, turning off the RM lead. The DSR low also resets OP1 by forcing ML2-6 low. With OP1 reset, DTR can once again go high, provided the NORM./TEST switch is still in NORM. The terminal is now ready for another call.

Test Character Generation

3.47 On late design units a test character generator circuit is located in the DAIF1 interface. Its purpose is to simplify cleaning of the recorder nozzles and electrodes by enabling the results of cleaning to be tested immediately, without waiting for an incoming message or connecting the DATS1 simulator. It does this by generating continuous W (or 2, with Baudot code in figures mode) characters whenever the PAPER ALARM button on the control panel is depressed, whether an incoming message is being received or not.

3.48 Depressing the PAPER ALARM button supplies ground, through 3NO and 3C, to pin 21 on the control panel connector, CP1. This signal, generate test character, is connected via DAIF/AA1-41 to XZAW-35, where it is connected to ML1-13 on test character generator card MC192 (TP322192). The output of this gate, ML1-11, will go high since gate ML2-8 is held low through strap A. This high causes ML2-2, XZAW-26, to go low, supplying T.R.M. to the receive message input of the printer drive, DAD/C209 (via DAIF/AA1-26), and card MC132, XZAN-18 or XZAN-23 (via a DU or PL strap). This turns on the high voltage and permits printing.

3.49 The high on ML1-11 causes ML2-6 (XZAW-23) and ML2-10 (XZAW-21) to go low. These two leads, reset 2 and reset 1, are connected to B28 and B11, respectively, on card MC180-87. They serve the dual purpose of removing the character that is stored in the serial register and preventing the set from storing any additional characters coming in on line. This accomplished by holding the register in the reset condition. A low on ML12-8 will cause the input register to be held in the reset condition. This can be accomplished by holding all the inputs to ML12-8 high. The low (produced

by the test character generator card) on B28 (ML10-12) causes ML10-8 to go high and thus ML12-9 and ML12-10 to go high. The low (produced by the test generator card) on B11 (ML13-9) causes ML13-8 to go high and thus ML12-12 to go high. The input, ML12-13, will be high unless the register is already in the reset condition. The register will then be reset by the small pulse produced at ML12-8.

3.50 The high at ML1-11 of card MC192 also appears at ML3-2. This gate allows the test character generator card to generate a substitute character available pulse. The test character available (T.C.A.) pulses are generated with the aid of Q1, Q2, and their associated components. Capacitor C3 and diode D2 are used to increase the test character available (T.C.A.) pulse to a minimum of 30 μ sec. Capacitor C3 will effectively hold ML1-5 low longer by charging to the slicing level of ML1-6 with a low-to-high transition on ML1-4. Diode D2 is used to eliminate resistor R9 from the charging circuit of C1 and thus helps increase the width of the T.C.A. pulse. The unijunction oscillator is constantly generating pulses but they do not appear at ML3-3 (XZAW-20) because there is normally a low on ML3-2 (not generating a test character).

3.51 When the PAPER ALARM button is pushed, ML1-13 will go low, ML1-11 high and ML3-2 high. This high at ML3-2 permits the C.A. to appear at ML3-3 (XZAW-20). The test character is factory-programmed by cutting straps 1 to 7. Strap one is cut if the desired character has a spacing first bit. Strap two is cut if the desired character has a spacing second bit, etc. When ML1-11 goes high, ML1-3 goes low and ML2-12 goes high. This allows the input to gates ML3-6, ML3-8, ML4-3, ML4-6, ML4-8, ML4-11, and ML3-11 to sense the condition of straps 1 to 7. If the strap is closed, a ground will be sensed at the input of the gate thus causing a high (mark) at the output of its associated gate. If the strap is open, two highs will be sensed at the input of the gate and hence producing a low (space) at the output.

3.52 When the PAPER ALARM button is released, ML1-13 will go high thus permitting the next T.C.A., which is seen at ML1-9, to reset the flip-flop (ML1-11, ML1-8). Resistor R10 is a pull-up resistor used to help keep the flip-flop (ML1-11, ML1-8) from being set due to noise on the ML1-13 to switch contact lead. Capacitor C1 is also used to keep noise from setting this flip-flop. When ML1-11 is low, a small negative noise spike appearing on ML1-13 must be wide enough to overcome the R-C rise time of C1 in order to set the flip-flop (ML1-11, ML1-8) erroneously.

B. DAIF2 Parallel Interface

General

3.53 The DAIF2 interface has one mode of operation: parallel receive only. It provides the station controls and signal conversion necessary to enable data interchange between a signal source such as a 402D data set or equivalent and elements of the high speed printer. The interface converts data from parallel contact closures or equivalent to neutral parallel (voltage) form. The baud rate is fixed by the sender, but may not exceed the data set maximum (750 for a 402D). A 402D data set must be mounted external to the printer cabinet.

3.54 Both the printer and the sender are controlled by the interface in either the attended or unattended mode of operation. The interface signals the printer to turn on its motors and enables data to flow only if the printer indicates that it is ready to receive. If the printer cannot receive, the interface will signal the sender that no data should be sent.

3.55 The interface is insensitive to character code and can be wired for 5-, 6-, 7-, or 8-level characters enclosed in a 7.00-, 7.42-, 8-, 9-, or 10-unit frame. Its output can be shifted to handle the 5-level code for typesetting by means of a jumper clip arrangement so that levels 2 through 6 are received in level positions 1 through 5.

3.56 Power requirements for the interface are as follows:

+6.0 ±0.6 v at 0.125 amp
-12.0 ±1.2 v at 0.050 amp
+48.0 ±6.0 v at 0.200 amp
117 ±10 v ac, 60.0 ±0.5 Hz at 1.0 amp

3.57 Input signals for a mark or on condition must be ground (0.0 ±0.5 v) capable of sinking 4 ma dc resistive, and for a space or off condition must be open or very high resistance (100 k ohms or higher) capable of withstanding +6.6 v. The timing lead must be on for a minimum of 5 milliseconds and should occur simultaneously with the beginning of each new character.

3.58 Output signals to the printer are +6.0 ±0.6 v through a 6 k ohm impedance for a mark or off condition and 0.0 ±0.5 v for a space or on condition, capable of sinking 10 ma dc resistive. The data signals will have the same duration as the incoming timing signal, and the output timing signal will be present for about 30 microseconds near the midpoint of the data signals.

3.59 There are six strapping options for the DAIF2 interface. Four are strapping options, as follows:

DU — for operation on a dial-up or switched network.

PL — for operation on a private line or dedicated network and direct interface to a DATASPEED Type 5 Sender or Receiver.

XW — for operation with ASCII or with Baudot code not compatible with DATASPEED senders and receivers.

XX — for operation with DATASPEED-compatible Baudot code (bits 1 through 5 of code presented by sender in bit positions 2 through 6).

The other two options, AW and BW, are present only on late design units equipped with the test character generator card MC192:

AW — ASCII W

BW — Baudot W, 2

Physically, the interface consists of an etched circuit card with integrated circuit and discrete components and a NORM./TEST switch. On late design units an additional circuit card is present in position ZAR.

Dial-Up Operation

3.60 If the data sets at the printer and remote sender are equipped with handsets, calls may be originated manually to either the printer or remote sender. With both data sets in the talk mode, the calling station dials the other station. When the called station answers, if the operators agree to go into the data mode, the called station must go into the data mode first. When the calling operator hears the 2025 Hz recognition tone, the calling station must be placed into the data mode before the tone ends or the call will be dropped.

3.61 In the data mode, the printer data set turns on the data set ready (DSR) lead to the DAIF2 interface. (This lead is also referred to as receive message (RM) in the DAIF2 interface.) The printer turns on its motors, high voltage, and PRINTER ON lamp, and starts the 15-second on-hook timer in the interface. The ready lead from the printer to the interface is turned on, and the interface turns on the supervisory transmitted data (STD) lead to the data set, if the data set is so equipped.

3.62 The data set must turn on the data carrier detector (DCD) lead within 15 seconds of the DSR (or RM) lead in order to disable the on-hook timer before it times out. If the timer is permitted to time out, it turns off the data terminal ready (DTR) lead to the data set, and the call is dropped. With the DCD lead on, the interface is ready to receive data.

3.63 For unattended operation, the data set must be in the auto mode. When the incoming ring signal appears on the line, it turns on the ring indicator (RI) lead. This places the data set in the data mode, and it is held there by the DTR lead from the interface. The rest of the turn-on sequence is as described for manual online operation.

3.64 Turn-off for either manual or unattended operation occurs when the data carrier is absent for more than about 15 seconds. The interface turns off the DTR lead to the data set, and the data set opens the DSR (or RM) lead to turn off the printer. The 15-second timer is reset, and the printer station is ready to accept another call.

Private Line Operation

3.65 If the printer has no handset (402D data set without an 804A data auxiliary set), the printer station is unable to place calls but has the ability to answer calls and receive data when called by a sending station. The sender activates the printer by placing the carrier on line, causing the data carrier detector (DCD) lead to come on to the interface. This enables the receive message (RM) lead of the printer. When the printer turns on its motors, a ready signal is sent to the interface and the supervisory transmitted data (STD) lead is enabled. This serves as a reverse channel indication to the sender if the data set is so equipped. If the data set is not equipped for reverse channel, the sender must not transmit a line feed signal for at least 1/3 second after the DCD lead is turned

on. At the end of the message the carrier is turned off by the sender, causing the DCD and RM leads to go off and shut off the printer.

Detailed Circuit Description

3.66 For details of the circuitry, refer to wiring diagrams 8267WD (parallel interface master reference), 8268WD (parallel interface schematic), 8274WD (parallel interface actual wiring diagram), 322134 (MC134 control card), and 322192 (MC192 test character generator card — late design units only). Wiring diagram 8268WD is not a complete schematic, and must be supplemented by the master reference wiring diagram (containing notes) and the control card wiring diagram (containing the schematic for the circuitry on the card).

3.67 Reference to components in this description are abbreviated as follows: XZAN and XZAR (late design units only) refer to the terminals on the cards in positions ZAN and ZAR, respectively, and ML1, ML2, etc, refer to specific integrated circuit components. For example, "XZAN-20, ML1-4" refers to terminal 20 on card MC134, located in position ZAN, which is connected directly to pin 4 of circuit ML1. The description of card MC134 shows that circuit ML1 is three three-input NAND gates. All gates mentioned in the description are NAND gates unless otherwise stated. Refer to the appendix (Part 4) for schematic symbols and truth tables for the integrated circuits.

3.68 Logic signals, unless otherwise noted, are either +6 v (high) or 0 v (low). The on or off condition of a circuit element varies with its function and is defined separately.

Turn On Sequence

3.69 The NORM./TEST switch must be in the NORM. position. This enables the receive message (RM) lead, XZAN-21, which connects to the auto on relay driver input.

3.70 The DAIF2/AAB interface turns on (0 v) the data terminal ready (DTR) lead, XZAN-35, if:

(1) Disconnect lead XZAN-24 is high (+6 to +54 v). This indicates a general ready condition at the printer; cabinet closed, some paper available for printing.

(2) Selectable lead XZAN-22 is low (0 v). This indicates that there is a predetermined amount of paper on the supply roll.

Note: If the paper supply is below the predetermined level, the selectable lead goes high (positive) and turns the DTR lead off (negative) before the printer answers a new data call. However, the selectable lead cannot turn off the DTR lead once a call has been established.

(3) The on-hook timer (OP1-6) is high. (OP1-6 is high when the timer is initially set.)

These three conditions result in highs at ML1-9, 10, and 11, causing a low at ML1-8. This reduces the conduction of Q3, causing its collector voltage to rise, and Q5 therefore saturates to produce the low at the DTR lead.

3.71 DTR on allows the data set to answer an incoming call. When the telephone circuit is complete, the data set grounds the RM lead, XZAN-21, turning on the printer. The low at XZAN-21 is applied to ML4-2, causing ML4-3 and ML4-4 to go high. This results in a low at ML4-6 and ML4-9, causing ML4-8 to go high. The high at ML4-8 releases timer OP1. When the printer turns on it grounds the ready lead, XZAN-30, which reduces the conduction of Q4 and therefore saturates Q6. This results in a low at the collector of Q6, which also appears at XZAN-31, the supervisory transmitted data (STD) lead. This lead may be used for reverse channel indication if the data set is so equipped.

3.72 The data carrier detector (DCD) lead, XZAN-20, must be turned on (0 v) within 15 seconds after the RM signal has initiated the timing cycle of OP1. This low DCD signal forces ML4-6 high, causing ML4-8 to go low and thus discharging C3 to clamp the timer. DCD on also forces ML2-11 high to enable ML2-10 and ML3-10.

Note: If the timer is permitted to time out, the resultant low at OP1-6 will force ML1-9 high, causing Q3 to conduct heavily and Q5 to cut off, thus producing a high (off) on the DTR lead which causes the data set to drop the call.

Receive Data

3.73 The timing lead, XZAN-18, turns on (0 v) and starts the character available timer. Since the DCD signal removed the clamp on ML2-3 during turn-on, ML2-3 goes high. This

high is gated with the high at ML3-8 to produce a low at ML2-8, forcing ML2-6 high, and C2 begins to charge to this positive voltage. The unijunction transistor, Q1, fires from 1.8 to 4.0 milliseconds after the timing signal appears at XZAN-18. The positive pulse across R1 is applied to Q2, and the Q2 collector goes low. This low forces ML3-3 high, which forces ML3-11 and the character available (CA) lead, XZAN-19, (early design units only), low. This also forces ML3-6 high, and this high is gated with the high from ML2-3 to force ML3-8 low, ML2-8 high, and thus ML2-5 high. In early design units, this forces ML2-6 low, preventing another cycle of the character available timer. The CA pulse is approximately 20 microseconds long. In late design units, the low pulse from the collector of Q2 is gated into ML2-4 to keep the unijunction timer from turning off until one full character available pulse has been generated. After this occurs, ML2-4 will go high, forcing ML2-6 low and thus preventing another cycle of the character available timer. The CA pulse width is increased to a minimum of 30 microseconds with the aid of CR10 and C7. When the low-to-high transition occurs at ML3-2, ML3-1 is held low until C7 charges to the slicing level of ML3. This effectively increases the pulse width to about 80 microseconds. As in early design units, CA appears at XZAN19.

3.74 When the timing lead, XZAN-18, returns to high, ML2-3 goes low and forces ML3-8 high. This enables the ML2-9 input, and the generation of the CA pulse is complete. The timing lead must be low for at least 5 milliseconds and high for at least 20 microseconds for each character.

3.75 The eight input data leads, XZAN-3, 5, 6, 8, 10, 12, 14, and 16, must be low (zero) to produce marks (+6 v) at output leads XZAN-2, 4, 7, 9, 11, 13, 15, and 17. The input data leads must be open or above +3 v to produce spaces (0 v) at the outputs.

Turn Off

3.76 When data transmission is completed, the DCD lead is opened, and the resultant high at ML4-5 causes ML4-6 to go low. This forces ML4-8 high, and the on-hook timer, OP1, is enabled. When the timer times out, OP1-6 goes low (zero), forcing ML1-8 high and turning off Q5. This opens the DTR lead (XZAN-35) to the data set, so the data set drops the call and opens the data set ready (DSR) lead, XZAN-21. ML4-3 goes low, forcing ML4-6 and ML4-8 low, resetting timer OP1. The interface is now ready to accept another call.

Test Character Generation

3.77 On late design units a test character generator circuit is located in the DAIF2 interface. Its purpose is to simplify cleaning of the recorder nozzles and electrodes by enabling the results of cleaning to be tested immediately, without waiting for an incoming message or connecting the DATS1 simulator. It does this by generating continuous W (or 2, with Baudot code in the figures mode) characters whenever the PAPER ALARM button on the control panel is depressed, whether an incoming message is being received or not.

3.78 Depressing the PAPER ALARM button supplies ground, through 3NO and 3C to pin 21 on the control panel connector, CP1. This signal, generate test character, is connected via DAIF/AA1-41 to XZAR-35, where it is connected to ML1-13 on test character generator card MC192 (TP322192). The output of this gate, ML1-11, will go high since gate ML2-8 is held low through strap A. This high causes ML2-2, XZAR-26, to go low, supplying T.R.M. to the receive message input of the printer drive, DAD/C209 (via DAIF/AA1-26), and card MC134, XZAN-21. This turns on the high voltage and permits printing.

3.79 The high on ML1-11 causes ML2-6 (XZAR-23) and ML2-10 (XZAR-21) to go low. These two leads, C.A. stop and blind, are connected to B23 and B27, respectively, on card MC134. The low on B23 (ML3-8) of card MC134 keeps any character available pulses from being generated. The low on B27 (ML5-10, ML5-13, ML6-10, ML6-13, ML6-5, ML6-2, ML5-2, and ML5-5) of card MC134 blinds the set from receiving any incoming data.

3.80 The high at ML1-11 of card MC192 also appears at ML302. This gate allows the test character generator card to generate a substitute character available pulse. The test character available (T.C.A.) pulses are generated with the aid of Q1, Q2, and their associated components. Capacitor C3 and diode D2 are used to increase the test character available (T.C.A.) pulse to a minimum of 30 μ sec. Capacitor C3 will effectively hold ML1-5 low longer by charging to the slicing level of ML1-6 with a low-to-high transition on ML1-4. Diode D2 is used to eliminate resistor R9 from the charging circuit of C1 and thus helps increase

the width of the T.C.A. pulse. The unijunction oscillator is constantly generating pulses but they do not appear at ML3-3 (XZAR-20) because there is normally a low on ML3-2 (not generating a test character).

3.81 When the PAPER ALARM button is pushed, ML1-13 will go low, ML1-11 high and ML3-2 high. This high at ML3-2 permits the C.A. to appear at ML3-3 (XZAR-20). The test character is factory-programmed by cutting straps 1 to 7. Strap 1 is cut if the desired character has a spacing first bit. Strap 2 is cut if the desired character has a spacing second bit, etc. When ML1-11 goes high, ML1-3 goes low and ML2-12 goes high. This allows the input to gates ML3-6, ML3-8, ML4-3, ML4-6, ML4-8, ML4-11, and ML3-11 to sense the condition of straps 1 to 7. If the strap is closed, a ground will be sensed at the input of the gate thus causing a high (mark) at the output of its associated gate. If the strap is open, two highs will be sensed at the input of the gate and hence producing a low (space) at the output.

3.82 When the PAPER ALARM button is released, ML1-13 will go high thus permitting the next T.C.A., which is seen at ML1-9, to reset the flip-flop (ML1-11, ML1-8). Resistor R10 is a pull-up resistor used to help keep the flip-flop (ML1-11, ML1-8) from being set due to noise on the ML1-13 to switch contact lead. Capacitor C1 is also used to keep noise from setting this flip-flop. When ML1-11 is low, a small negative noise spike appearing on ML1-13 must be wide enough to overcome the R-C rise time of C1 in order to set the flip-flop (ML1-11, ML1-8) erroneously.

C. Discrete Calling Generator

3.83 The TP325200 discrete calling generator consists of a TP199570 signal generator assembly and a relay bracket assembly, mounted within the DAIF1 or DAIF2 module frame. The signal generator assembly has a 20 rpm, 117 v ac motor and clutch, a TP199580 programmable code disc, and a set of stationary sensing brushes. A dual wire spring relay and terminal strip are mounted on the relay bracket. When programmed, the discrete calling generator permits the printer to enable an unattended type 2 or type 5 DATASPEED sender equipped with an identically programmed recognizer.

3.84 Depressing the TRANS START pushbutton on the printer function strip (after the PRINTER ON light has come on) operates the discrete calling generator relay, placing the associated data set in the send or answer-back mode and engaging the clutch. This starts the code disc turning and generates the discrete 14-bit code. When the code disc completes one revolution it stops and restores the data set to its original mode.

3.85 The TP325200 discrete calling generator is almost identical to the TP199550 protected unattended transmitter modification kit for Type 2 DATASPEED Receivers. It differs from the TP199550 kit in that it mounts in the interface module instead of having its own frame and cabling and uses a positive instead of a negative voltage supply. There is no difference as far as operation with type 2 equipment. Refer to Section 592-806-101 for additional information. The discrete calling generator is also similar to the TP199784 station identifier for Type 5 DATASPEED Receivers. There are packaging and electrical differences, but operation with type 5 equipment is identical. Refer to Section 592-808-101 for additional information.

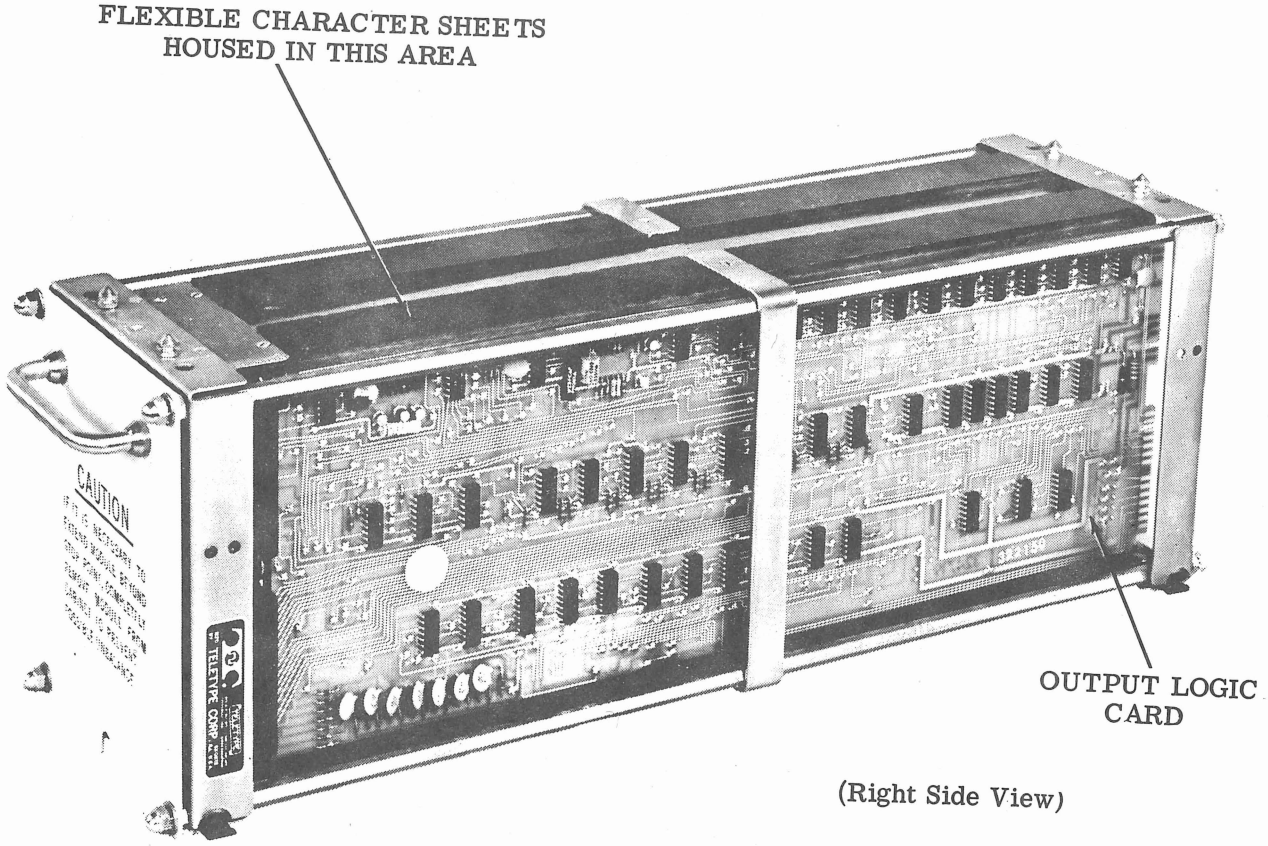
CHARACTER GENERATOR

3.86 The character generator is a memory and logic system which translates incoming codes from the interface into the signals necessary for the printer drive to direct the generation of characters by the recorder. It controls both the tracing of each individual character and the spacing of characters on a line, plus additional functions such as line feed. The character generator is housed in the DAG module (Figure 7).

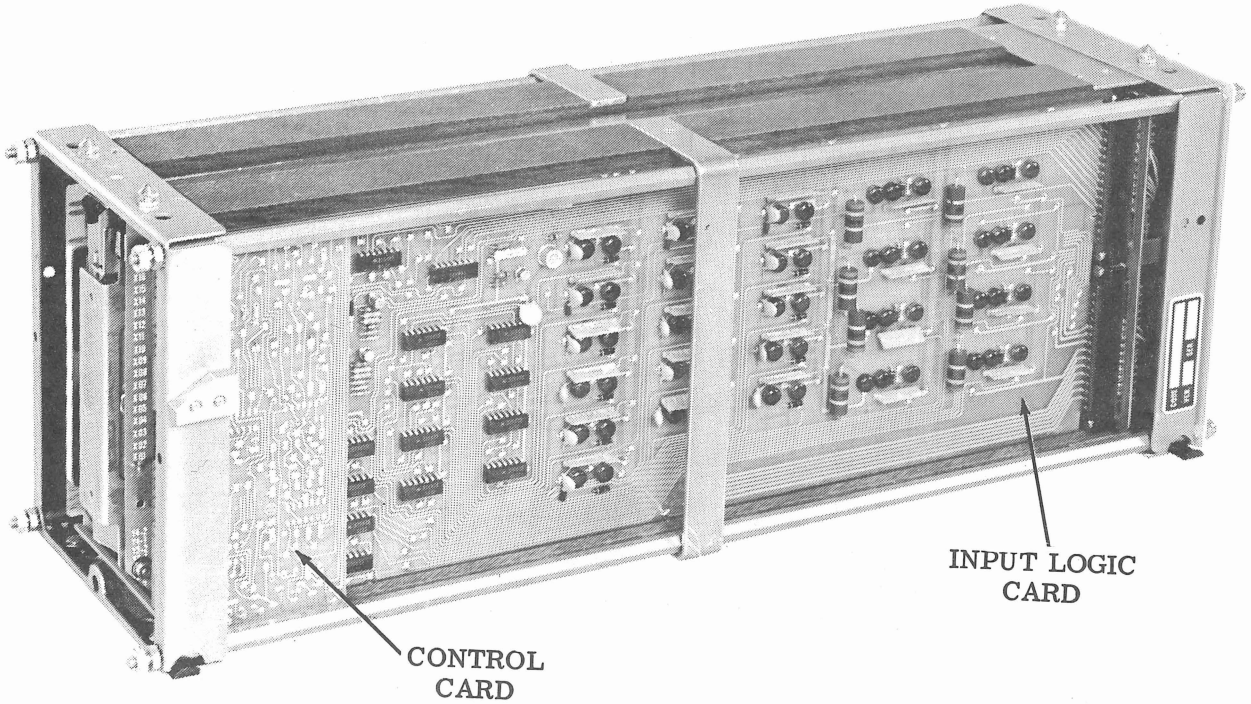
A. General

3.87 The character generator receives digital information input signals (seven bits for ASCII; five for Baudot) and a start signal from the interface, in parallel form. Together, these signals define a character. Each character is stored for 8 milliseconds while the logic selects and processes the appropriate memory subroutine. This consists of sequentially interrogating the memory while storing the character until the tracing drive processes it. When the character is printed the generator locates to the next printing position.

3.88 The character generator has provisions for generating 64 different characters, with each character being composed of a maximum of 32 dot positions (Figure 8). Dot positions

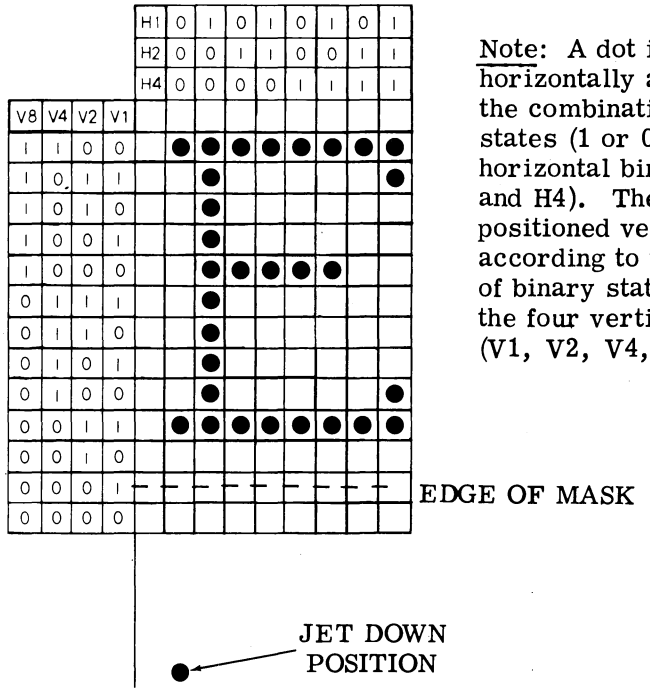


(Right Side View)



(Left Side View)

Figure 7 - Character Generator (DAG) Module



Note: A dot is positioned horizontally according to the combination of binary states (1 or 0) of the three horizontal binaries (H1, H2, and H4). The dot is positioned vertically according to the combination of binary states (1 or 0) of the four vertical binaries (V1, V2, V4, and V8).

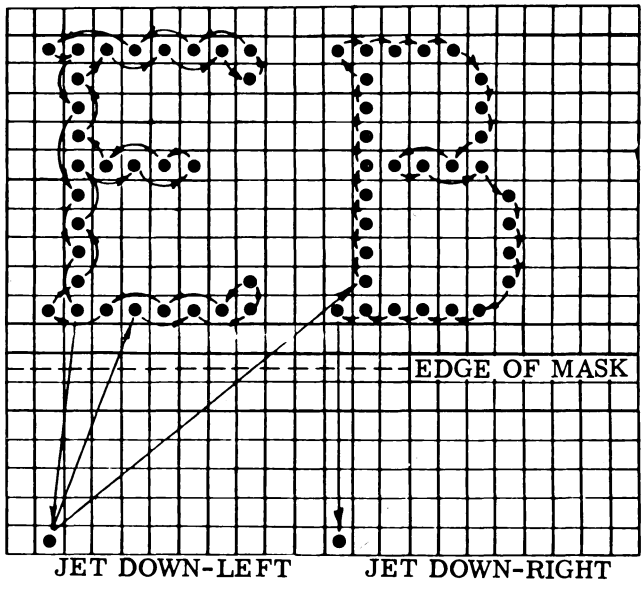


Figure 8 - Basic Tracing Pattern of Typical Electrode Assembly

are defined by up to 32 seven-bit words which control the actual tracing of the character, and the outputs of seven binaries, used to position characters on a line.

3.89 The memory consists of a matrix of 112 transformer cores together with input and output windings. Two U-sections make up a core and establish a closed magnetic circuit. The memory works on transformer action, with a primary of one turn and a secondary of eight turns. The primaries are on 64 flexible plastic etched circuit sheets 0.003 inch thick, one for each character. Each sheet has a unique conductor path which distinguishes it from the sheets for all other characters. A character sheet contains two separate conductors, as shown in Figure 9. Each conductor acts as a primary for half of a character, and the memory is scanned twice per character. As a result, the number of cores needed to store a character is reduced from 32 times 7, or 224, to 16 times 7, or 112. The secondaries are on an etched circuit card arranged in 16 groups of 7, one secondary for each core. Each group of seven secondaries produces the information for two dots of the character; one dot on the first scan and the other dot on the second scan.

3.90 Depending on the memory program board and the character sheets it contains, the memory can store up to 64 characters of ASCII, all of communications Baudot, or all of weather Baudot. The character generator code and individual character sheet part numbers are the same for all codes; variations are accommodated in the memory program board codes, DAG2/AAB, DAG2/AAC, and DAG2/AAE.

3.91 Power requirements for the character generator are as follows:

5.3 v to 7.3 v dc
41.5 v to 53.0 v dc
13 watts maximum power

3.92 There are two independent optional features in the character generator. The time required to feed out one line of paper when the PAPER ADVANCE button is depressed may be reduced from the standard 64 milliseconds to 32 or 16 milliseconds so that paper will be fed out two or four times as fast. Normally, CR initiates carriage return only and LF initiates line feed only, but the character generator may be programmed for simultaneous carriage return and line feed on receipt of CR (for ASCII only) or simultaneous carriage return and line feed on receipt of LF.

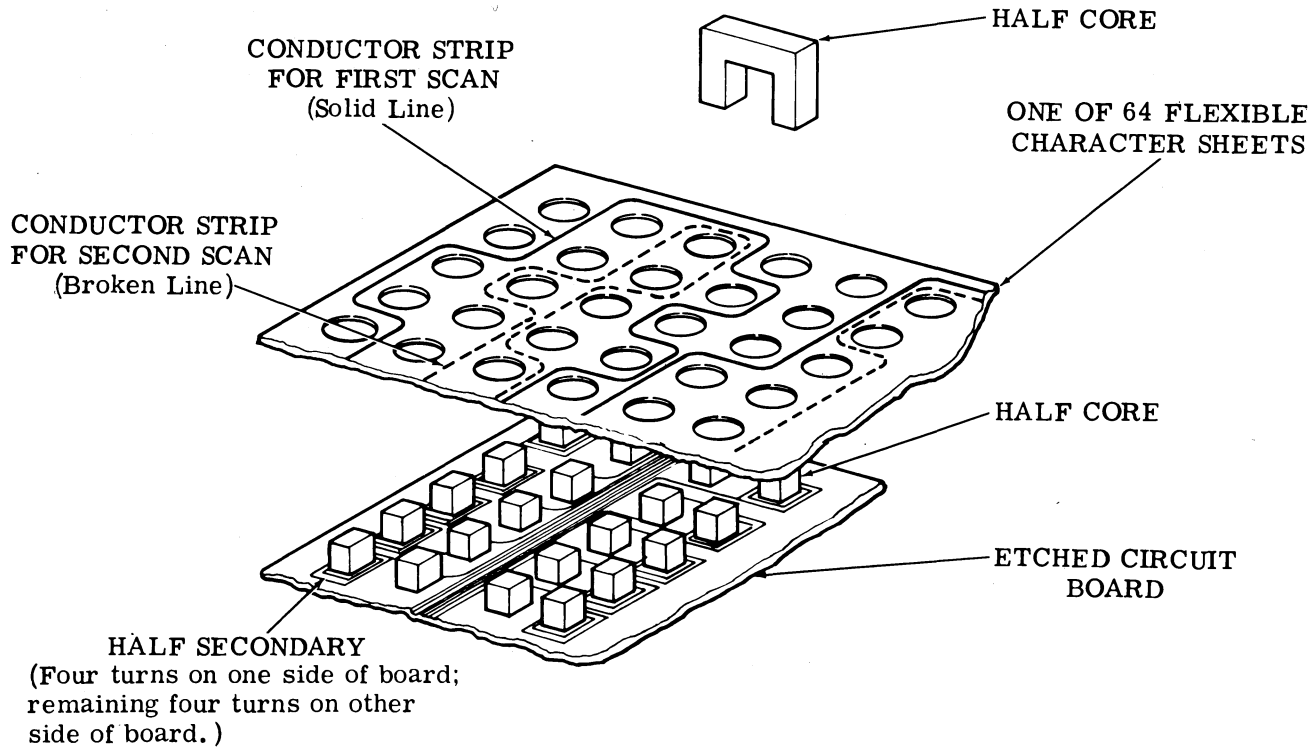


Figure 9 - Core Arrangement and Conductor Routing on Character Sheets

B. Detailed Circuit Description

3.93 The detailed description of this unit is divided into seven parts: the line feed buffer and controls; the memory input buffer and controls; the timing signals; the character positioning binaries and associated gates; the memory drivers and controls; circuits peculiar to control functions; and programming for ASCII and Baudot codes.

3.94 For details of the circuitry, refer to wiring diagrams 8252/AAA/WD (character generator schematic), 8252/AAB/WD (ASCII program board), 8252/AAC/WD (communications Baudot program board), 8252/AAE/WD (weather Baudot program board), 322151 (MC151 input logic card), 322150 (MC150 output logic card), 322152 (MC152 ASCII control logic card), 322153 (MC153 Baudot control logic card), 303927 (EC927 ASCII program board), 303928 (EC928 Baudot program board), 303929 (EC929 output board assembly), and 8260WD (timing diagram).

3.95 The following discussion is directed toward ASCII operation. Therefore, a start signal and a seven-bit signal defining a character must be supplied to the generator from the interface. The start signal is referred to as the character available signal. It is nominally a low pulse of approximately 20 or 80 microseconds duration, as explained in 3.44 for serial interface and 3.73 for parallel interface.

Line Feed Buffer and Controls

3.96 The character available signal (a low at 201 of card MC151) controls the line feed buffer, shown on Sheet 2 of TP322151. It clears register ML2-5 through ML8-5 and simultaneously enables transfer gates ML2-2 through ML8-2 via a high signal generated by inverting gate ML1-13. Because the propagation time of this gate is about 10 nanoseconds, the transfer signal is high longer than the clear to the register is low. Utilizing this fact, one signal and one inverting gate are used to both clear and transfer information into the register. The purpose of this register is to supply the line feed mechanism with 12 milliseconds of operating time on receipt of a line feed signal. This exceeds the normal character time for printing functions (8 milliseconds) because of the cycling time required by the line feed mechanism. A line feed signal can be generated by any of three control characters as decoded by gate ML1-8, ML2-6, or ML1-6 on card MC152. These control characters are line feed, vertical tab, and form feed, respectively. The line feed signal (which is the result of a wired OR connection of the above gates) drives a line feed network on card MC150 as described in 3.102 (c).

Memory Input Buffer and Controls

3.97 This same character available signal triggers a 4-millisecond monostable network, established by diodes CR1 and CR2 and transistor Q1, by setting a dc flip-flop (ML17-11, 6) on MC151 that reverse-biases diode CR3, permitting capacitor C1 to charge to the threshold of the network. When this point is reached, transistor Q1 saturates and flip-flop ML17-11, 6 is reset. The positive-going edge of this 4-millisecond signal is sensed by a differentiating network consisting of R7, C3, R8, R9, and Q3 and amplified by an emitter follower consisting of R43 and Q60. This signal, designated start of cycle (SOC) is nominally low for 4 microseconds and is used to clear the memory input buffer register, which consists of ML10-12 through ML16-12 on card MC151. Its transfer gates, ML2-8 through ML8-8, are simultaneously enabled by the inverted SOC signal (high) from gate ML1-8. The propagation time of this gate permits the transfer signal (high) to exist longer than the register clear signal (low), so that the signal first clears and then transfers information into the register. The purpose of the 4-millisecond delay is to allow for the 12-millisecond line feed time mentioned in 3.96. Thus, printing signals are delayed 4 milliseconds before they are processed by the character generator, whereas line feed signals are fed directly to the line feed circuitry and are allowed a duration of 12 milliseconds.

Timing Signals

3.98 The SOC signal initiates the internal timing of the character generator. The timing elements include three monostable networks and a unijunction oscillator. There are 32 timing frames (250 microseconds each) within a character interval (8 milliseconds), and each timing frame defines the operations needed to print one dot. The first frame is initiated by the SOC signal, which also starts the unijunction oscillator. The oscillator initiates the remaining 31 frames. The three monostable networks will be referred to in the following discussion as the memory control monostable, the vertical control monostable, and the horizontal control monostable.

(a) The memory control monostable consists of ML22-12, ML17-8, CR4, CR5, CR6, C2, R4, R5, R6, and Q2 on card MC151. On receipt of the SOC signal (low on ML22-2) or the oscillator signal (low on ML22-1), dc flip-flop ML22-12 and ML17-8 is set and diode CR6 is reverse-biased. This permits capacitor C2 to charge through resistor R6 to the threshold of this monostable network, which is established by CR4, CR5, and Q2. When this point is reached, transistor Q2 turns on and flip-flop ML22-12 and ML17-8 is reset. The output signal from this network is a high 10-microsecond pulse. This signal is gated with the normal and inverted level 1 signals from the memory input buffer register (ML10-6 and ML10-8) via NAND gates ML1-3, 6 and inverters ML9-8, 6. Output signals MRL #1 (memory register level 1) and MRL $\overline{\#1}$ (memory register level 1 inverted) are thus always opposite in sign (high, low or low, high). They are supplied to the X-drivers as a sequence of 32 ten-microsecond pulses. The output of the X-drivers is used to read the memory (via program board EC927) as described in 3.99. The memory output buffer register on MC150 is also cleared as soon as the reading of the memory begins. This clear signal ($\overline{MC}$) is propagated through three gates: ML1-3 or ML1-6, and ML17-3 on MC151 and ML29-8 on MC150. This propagation delay is necessary to insure that signals in the vertical and horizontal registers (3.98(b) and (c)) are not disturbed by new information being processed by the memory output buffer register.

(b) The vertical control monostable consists of CR7 through CR9, R11 through R13, C2, and Q4, all on MC150. The SOC signal produces a low at ML3-1, forcing the vertical register control lead (ML3-12) high. This high is applied to ML29-1, and the resulting low at ML29-3 inhibits the vertical transfer gates (ML41-3, ML42-11, ML44-3, and ML45-11). With ML3-12 high, the vertical control monostable begins to time out. After approximately 20 microseconds, Q4 conducts and its collector voltage goes low, forcing ML4-11 high. This high forces ML3-12 low, enabling the vertical transfer gates. Information stored in the vertical portion of the memory output register (ML4-11, ML42-3, ML44-11, and ML45-3) is now transferred to the vertical register, and appears at ML40-8, ML43-6, ML43-8, and ML46-6. This information remains on the output leads of the vertical register (V1, V2, V4, and V8) for the remainder of the 250-microsecond timing interval.

(c) The horizontal control monostable consists of CR4 through CR6, R8 through R10, C3, and Q5, all on MC150. This circuit operates in essentially the same manner as the vertical control monostable, but produces a 200 microsecond delay, compared to the 20-microsecond delay of the vertical monostable. (The additional 180 microseconds compensates for the time it takes the ink droplets to move from the vertical deflection electrode to the horizontal deflection electrode on their way to the platen.) The SOC signal produces a low at ML3-4, forcing the horizontal register control lead (ML3-6) high. This high is applied to ML29-5, and the resulting low at ML29-6 inhibits the horizontal transfer gates (ML36-11, ML38-3, and ML39-11). With ML3-6 high, the horizontal monostable begins to time out. After approximately 200 microseconds, Q5 conducts and its collector voltage goes low, forcing ML4-3 high and ML3-6 low. The low at ML3-6 enables the horizontal transfer gates. Information stored in the horizontal portion of the memory output register (ML36-3, ML38-11, and ML39-3) is now transferred to the horizontal register, and appears at ML37-6, ML37-8, and ML40-6. As explained for the vertical register, this information remains on the output leads (H1, H2, and H4) for the remainder of the 250-microsecond timing interval.

(d) As mentioned, the SOC signal starts the 250-microsecond oscillator, which consists of CR1, R2 through R7, C1, Q1, and Q2. The SOC signal produces a low at ML3-11, forcing ML3-8 high and latching ML4-6 low. This low, applied to the base of Q3, cuts off Q3 and produces a high at its collector. C1 begins to charge through R2 and R7, until its voltage reaches the firing point of Q2. When the UJT fires, C1 discharges rapidly through R6, producing a positive pulse across R6. This pulse is applied through R3 to the base of Q1, which conducts heavily to produce a negative-going pulse at its collector. C1 quickly discharges to a point where it can no longer maintain conduction of Q2, which then cuts off. C1 begins to charge again, and the cycle is repeated. As long as ML4-6 remains latched, the oscillator continues to generate pulses at a 250-microsecond rate. The pulses (lows) are applied to ML3-2 and ML3-3, producing inverted pulses (highs) at ML3-12 and

ML3-6 to control the vertical and horizontal registers. They are also applied to ML22-1 on MC151 to trigger the memory control monostable. The pulses at ML3-6 also serve as a clock for ML5-2, the clock pulse input of the first Z-driver binary. On the 31st pulse after the SOC pulse, ML9-9 delivers a high to ML10-5, causing ML10-6 to go low and ML4-8 to go high. This high is applied to ML2-11, forcing ML2-8 low. The low at ML4-4 resets the latch, forcing ML4-6 high and turning on Q3 so that its collector voltage goes low and prevents further oscillations.

Character Positioning Binaries

3.99 A ripple counter of seven binaries on card MC150 controls the positioning of characters on a line. These binaries are designated ML11 through ML17. Their ultimate outputs to the printer drive are five group signals (A, B, C, D, and E) and seven binary signals (L/R, B7, $\overline{B7}$, B8, $\overline{B8}$, B9, and $\overline{B9}$), which together determine all 80 character positions on a line.

(a) The last three binaries, ML15 through ML17, drive five decoding gates: ML33-8, ML34-6, ML34-8, ML35-6, and ML35-8. The outputs of these gates are inverted by gates ML47-6, ML47-8, ML48-6, ML48-8, and ML49-8 and presented to the spacing drive portion of the printer drive as groups E, D, C, B, and A, respectively. They control five intervals on a line which are in turn divided into sixteen character positions, determined by the last six binary signals. The five decoding gates are also controlled by a network consisting of gates ML22-6 and ML22-8 on card MC151. These two gates monitor the 4-millisecond interval as established by the 4-millisecond monostable, the printing interval as established by the oscillator reset gate, and a nonprint or horizontal tab mode as established by decoders on MC152. Consequently, the five MC150 decoding gates will be inhibited during nonprint characters or intervals.

(b) The inverted output of the first binary, ML11, is coupled to the tracing drive portion of the printer drive via line driver ML30-6 as L/R, and the inverted and normal outputs of the next three binaries, ML12 through ML14, are coupled to the spacing drive portion via line drivers ML31-6, ML30-8, ML32-6, ML31-8, ML33-6, and ML32-8 as B7, $\overline{B7}$, B8, $\overline{B8}$, B9, and $\overline{B9}$, respectively. These last 6 binary signals determine 16 character positions which, together with the 5 group signals, define the 80-character line. L/R is used by the tracing drive to control the character position — left or right — in which one of the 40 ink jets will print. (B7 and $\overline{B7}$ are also connected to vertical switches in the tracing drive.)

(c) A nonprint condition inhibits the stepping of the binaries. This print inhibit condition can be generated either by an incoming code that defines a nonprint character (and is decoded on MC152) or the operation of the paper advance network. Should either of these conditions exist, gate ML10-3 is inhibited, and binary ML9 is inhibited from stepping binaries ML11 through ML17. The source of the print inhibit signal, located on MC152, is described in 3.103 (a). The paper advance network works in conjunction with these seven binaries and must have control of the binaries at all times. Therefore, should a print inhibit exist the binaries can still operate via an alternate gate ML10-11 that will be enabled when the paper advance network is triggered. This circuit is described in 3.102 (a).

Memory Drivers and Controls

3.100 A matrix of 16 X-drivers and 4 pairs of Y-drivers on MC151 allows the selection of any one of the 64 character sheets in the memory. The 16 X-drivers decode bit levels 1 through 4 of the memory input buffer register. The 4 Y-driver pairs decode the last three levels of this register. Therefore, any character information in this register will select only one X-driver and one pair of Y-drivers, which in turn will select only one character sheet in the memory. Each Y-driver in conjunction with an X-driver produces the information for 16 dots. Therefore, the Y-driver pair and this X-driver will produce a maximum of 32 dots necessary to print a character. When a Y-driver is enabled, its output rises to +48 volts for half the print cycle (4 milliseconds). A binary, ML9 on MC150, produces the controlling signals (B5 and $\overline{B5M}$) that determine which Y-driver of any Y-driver pair is to be on and for how long. The X-driver is enabled by the input signals and by a sequence of 32 ten-microsecond clock pulses from gate ML9-8 or ML9-6 on MC151, as described in 3.98 (a). When an X-driver is enabled, its output is grounded and permits current to flow through one sheet.

3.101 By pulsing the memory and then stepping the 16 Z-drivers, ML21-6 through ML28-8 on MC150, the information for 16 dots is sequentially read out. The control of these Z-drivers is a function of four binaries, ML5 through ML8 on MC150. As information for the positioning of each dot is read from the memory (in parallel), it is stored in the memory output buffer register ML45-3, ML44-11, ML42-3, ML41-11, ML39-3, ML38-11, and ML36-3. This information will remain in the register until the memory is pulsed again. It is then selectively applied to another set of registers. The first register stores vertical information. It consists of ML46-6, ML43-8, ML43-6, and ML40-8 and behaves as a register for 20 microseconds from the time the memory is pulsed. After this interval, this register behaves as a set of inverting gates monitoring the information in the memory output buffer register. Horizontal information is handled identically to vertical information, with one exception. The horizontal register, ML40-6, ML37-8, and ML37-6, behaves as a register for 200 microseconds after the memory is pulsed and as a set of inverters for the remaining 50 microseconds of each character. A jet down signal (JD) is also supplied via NAND gate ML46-8 and diode CR14, which monitors the outputs of the vertical register and the inverted vertical control monostable output from ML29-3, and NAND gates ML1-8 and ML1-11. On late design units, the print interval signal from ML2-8 is connected (via diode CR26) to the JD signal output to hold jet down on at all times when the set is not printing, even if noise spikes should set any one of the vertical register latches. These eight signals — V1, V2, V4, and V8 from the vertical register; H1, H2, and H4 from the horizontal register; and JD from ML1-8 and ML1-11 — are supplied to the tracing drive portion of the printer drive, along with L/R, B7, and $\overline{B7}$, to control the tracing of each character.

Control Function Circuits

3.102 Three circuits on MC150 control modes other than those associated with the tracing and spacing of characters: The paper advance circuit, the carriage return circuit, and the line feed circuit.

(a) The paper advance circuit consists of a dc flip-flop, ML1-6 and ML1-3, which is controlled by the PAPER ADVANCE button on the function strip. When this button is operated, a low signal changes the state of the flip-flop, enabling gate ML1-11 and allowing the character positioning binaries, ML11 through ML17, to step at the character rate as determined by the oscillator and binaries ML5 through ML9. By programming the input (422) of gate ML19-12 to the output of either binary ML12 (416), ML13 (412), or ML14 (408), the paper advance will operate at a 16-, 32-, or 64-millisecond rate. Since gate ML19-3 is enabled and the oscillator that controls character time enabled by a signal via ML17-3 and ML3-8, binaries ML11 through ML17 will step at the character rate (8 milliseconds) until the programmed position is located. At this instant, the line feed and carriage return networks are operated via gate ML19-11, and binaries ML11 through ML17 are reset, repeating this operation. Flip-flop ML1-1 is reset by the low signal from line feed driver ML20-6.

(b) A carriage return signal resets the character-positioning binaries to a quiescent state defined as the first character position on a line. The carriage return circuit consists of ML18-8, ML19-6, and ML20-8. Four inputs are capable of triggering this circuit: The carriage return or line feed signal (119), brought in if the character generator is programmed for line feed on receipt of carriage return or carriage return on receipt of line feed; the output of the carriage return decoder, ML2-8 on MC152 (123); the output of the paper advance circuit, via gate ML19-11; and the output of the automatic carriage return and line feed circuit from gate ML2-6, which senses the binary condition (normal output of ML11, ML15, and ML17 high) indicating that 81 characters have been received without a carriage return or line feed (two characters are lost when this condition occurs). Any of these signals will set flip-flop ML18-8 and ML19-6 and cause a carriage return by placing a low on the set direct leads, SD (pins 5), of binaries ML11 through ML17. This flip-flop and the line feed flip-flop described in the following paragraph are reset by the low signal from oscillator Q1 on MC150.

(c) The line feed circuit consists of a dc flip-flop, ML18-6 and ML19-8, and gate ML20-6. This circuit can be triggered by a signal from the line feed decoder, ML1-8, on MC152 (125); the CR or LF signal (119), brought in if the character generator is programmed for line feed on receipt of CR or carriage return on receipt of LF; the output of the automatic CR/LF gate, ML2-6; and the

output of the paper advance network via gate ML19-11. The output of this circuit, LF (low), is connected to the ink heater and line feed bracket assembly.

Programming for ASCII and Baudot Code

3.103 ASCII code was assumed throughout the preceding description of the character generator. This required that it contain control card MC152 and program board EC927. In a character generator for Baudot code, these components are replaced by control card MC153 and program board EC928. Operation of these code-sensitive components is as follows:

(a) The ASCII control card, MC152, decodes functions peculiar to ASCII and is used to supply a line feed signal (which also indicates vertical tab and form feed), a carriage return signal, a horizontal tab signal, and a print inhibit signal — plus two straps to condition the input buffer into the ASCII mode. This board is connected via 45 pin connections (9 groups of 5) to input logic board MC151. Three decoders — line feed ML1-8, vertical tab ML2-6, and form feed ML1-6 — have their outputs connected as a wired OR gate to generate a common line feed signal. These three decoders monitor the outputs of the line feed buffer register and supply the line feed mechanism with 4 milliseconds of additional operation time. The carriage return decoder can be programmed to be initiated by the line feed buffer register. This is necessary in order to initiate carriage return and line feed simultaneously if the character generator is programmed to provide these two operations on receipt of a carriage return signal. In ASCII there are 36 nonprinting control characters in which code levels 6 and 7 are spacing, and there is one nonprinting character (delete) in which all 7 levels are marking. A print inhibit signal must be generated on receipt of any of these characters to prevent the recorder from advancing to the next printing position. Horizontal tab, however, is an exception; it is not now used by the printer, so if it should be received the print inhibit signal must be suppressed so that a horizontal tab signal is converted into a space. Also, printing of the character stored in the memory output buffer register when the PAPER ADVANCE button is depressed must be inhibited. All this is accomplished by the print inhibit circuit on MC152. Gate ML3-6 detects horizontal tab and presents it to MC151 (for future use) and to gate ML3-8. The output of ML3-8 is low when levels 6 and 7 are spacing, except when the character received is horizontal tab. Gate ML4-6 inverts the output of ML4-3, whose inputs are the paper advance signal and an input reserved for future use. Gate ML5-6 and diodes CR1, CR2, and CR3 detect the delete character. The outputs of ML3-8, ML4-6, and ML5-6 are connected as a wired OR gate to produce the low print inhibit signal. The program board matrices the X and Y drivers to the appropriate character sheets.

(b) The Baudot control card, MC153, contains gates to decode the following characters: Horizontal tab (ML2-6), line feed (ML2-8), carriage return (ML1-6), a letters (ML3-6) or figures (ML3-8) shift, and a print inhibit signal generated by these nonprint characters (ML4-8 and ML4-6). All of these outputs, with the exception of the output for a letters or figures shift and the second line feed decoder, initiate other logic networks already described in 3.102. A signal from decoder ML3-6 (letters shift decoder) will drive the output of flip-flop ML15-6 on MC151 low and the output of flip-flop ML16-6 high. This combination will select the Y-drivers associated with the code field for letters. The detection of a signal from decoder ML3-8 (figures shift) conditions the above mentioned flip-flops in the opposite states, and the Y-drivers associated with the code field for figures are selected.

Note: Late design MC153 cards include circuitry to integrate the figures-letters latches (ML15-6, 8 and ML16-6, 8 on MC151) to reduce false shifts caused by noise pulses.

PRINTER DRIVE

3.104 The printer drive converts digital electronic signals from the character generator into high voltage analog signals used to drive the recorder electrodes that trace out the characters. It also provides the valving signals that determine the position of the character on the line. The printer drive is housed in the DAD module (Figure 10).

A. General

3.105 The printer drive receives 11 input signals from the character generator (six outputs of a three-stage binary counter and five group signals) to determine in which column

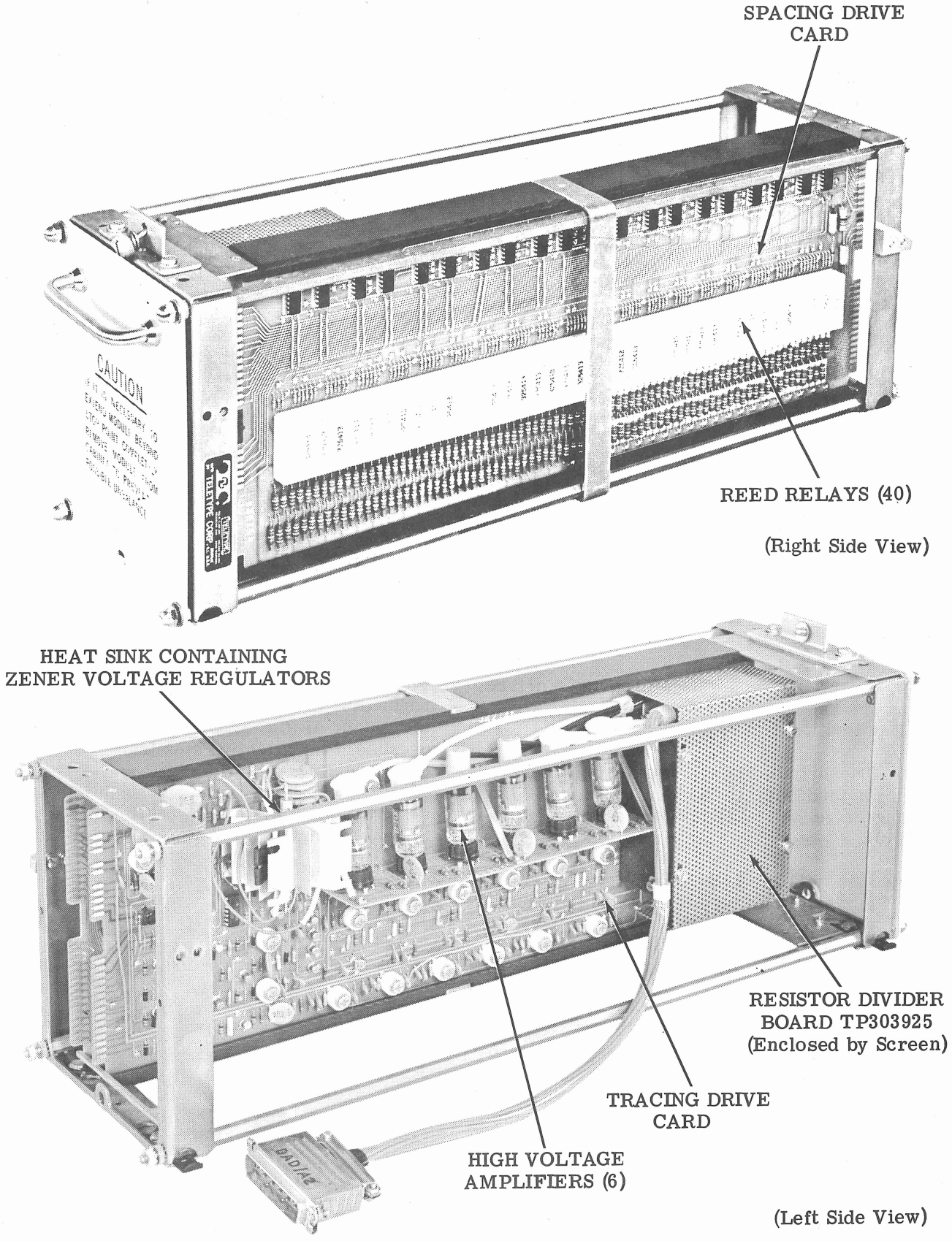


Figure 10 - Printer Drive (DAD) Module

out of 40 printing will take place. It also receives 11 signals to control the tracing of character shapes (four for vertical information, three for horizontal information, one left-right shift, and three vertical amplifier selection inputs). These are all 0 to +6 volt digital signals. An input for control of the power supply is also required.

3.106 Output signals consist of 40 valving signals (+550 v dc) from the spacing drive, of which only two adjacent ones are energized at any one time, and six high voltage analog signals (four vertical, two horizontal) from the tracing drive. Drive signals are independent of the character generator used.

3.107 Power requirements for the printer drive are as follows:

-12 v dc ±1.2 v at 0.25 amp
+6 v dc ±0.6 v at 0.25 amp
6.3 v ac ±10% at 1.0 amp
+30 v dc ±3.0 v at 0.25 amp
+48 v dc ±4.8 v at 0.10 amp
(from interface)
+120 v dc ±10 v limited to 12 ma
(3 inputs)
+550 v dc ±20 v limited to 3 ma
+3900 v dc ±200 v limited to 5 ma
(6 inputs)

3.108 There are no options in the printer drive.

B. Detailed Circuit Description

3.109 The detailed description of this unit is divided into two independent parts: The spacing drive (MC145) and the tracing drive (MC146).

3.110 For details of the circuitry, refer to wiring diagrams 322145 (MC145 spacing drive), 322146 (MC146 tracing drive), 303925 (EC925 resistor divider card), 8254WD (printer schematic), and 8260WD (timing diagram).

Spacing Drive

3.111 The spacing drive converts six binary inputs and five group inputs from the character generator into a +550 v signal which is applied to the valving electrode of the column to be printed and to the next valving electrode across the line.

3.112 Operation of a typical valving circuit is as follows. Circuit number one is energized by applying a signal of greater than +2.6 v on pins D313 (group A), D306 ($\overline{B9}$), D308 ($\overline{B8}$), and 310 ($\overline{B7}$). This causes inputs 9, 13, 12, and 10 of ML20 to be at a voltage greater than +2.6 v. The output, pin 8 of ML20, goes to 0 v. This causes reed relay RR40 to be energized through diode CR119. A low output at pin 8 of ML20 also allows reed relay RR38 to be energized through diode CR114. When RR40 is energized, it couples +550 v through current-limiting resistors R79 and R159 to D429. D429 corresponds to valving electrode 1. When RR38 is energized, it couples +550 v through current-limiting resistors R75 and R155 to D425, which corresponds to valving electrode 2. The purpose of the current-limiting resistors is to limit the inrush current to the stray capacitance to a safe limit for the reed relay (about 2 ma). When a reed relay is not energized, its output is returned to ground through a high resistance. This resistance gives the stray capacitance a path through which it can discharge. R80 and R160 form this return path for RR40, and R76 and R156 form the path for RR38.

3.113 When pin 8 of ML19 is low, RR38 and RR36 are selected and valving electrodes 2 and 3 are raised to +550 v. As the decoding proceeds, the selected reed relay and the one ahead of it are always energized at the same time (8260WD, Sheet 4). There is a diode connected to the output of each reed relay driver which is returned to ground through a 7-volt zener diode (CR121). Its purpose is to prevent the output of the driver from exceeding +8 v because of the inductive kick from the reed relay coil. There is also a pi filter network, made up of C1, C2, and L1, in the +6 v supply to the reed relay coils. This is used to filter out any noise from the contacts which may be coupled into the coil.

Tracing Drive

3.114 The tracing drive consists of four parts: The digital-to-analog converters, the high voltage amplifiers, the relay driver-overvoltage protection circuit, and two power supplies.

3.115 Digital-to-Analog Converters: Eleven digital signal inputs are used to produce three analog signals (X1, Y1, and Y2) which are used to trace the shape of a character (Figure 8). There are three horizontal binary inputs and one left/right control input (H1, H2, H4, and L/R on pins C229, C227, C225, and C223, respectively) which control four NAND gates consisting of Q15, Q16, Q17, and Q18 and associated components.

These gates, in conjunction with their collector load resistors (R92, R94, R96, and R98), form digital current sinks weighted according to the binary level they represent; ie, the current sink corresponding to the 1-level is a 0.1 ma sink, the one corresponding to the 4-level is a 0.4 ma sink, and the one corresponding to the L/R-level is a 1.05 ma sink. The gates are either on or off as determined by the input signals. The current levels are determined by the collector load resistors and the input voltage to the inverting input of the operational amplifier (OP17-2). The sum of the currents through these current sinks is the input current to the operational amplifier. In order to maintain a constant differential (0 v) across the two inputs (OP17-2 and OP17-3), this input current is matched by a current through the feedback resistor (R100) and level resistor (R104). The output voltage (OP17-6), then, is proportional to the sum of the current sources, and hence is the analog equivalent of the digital inputs (8260WD, Sheet 3).

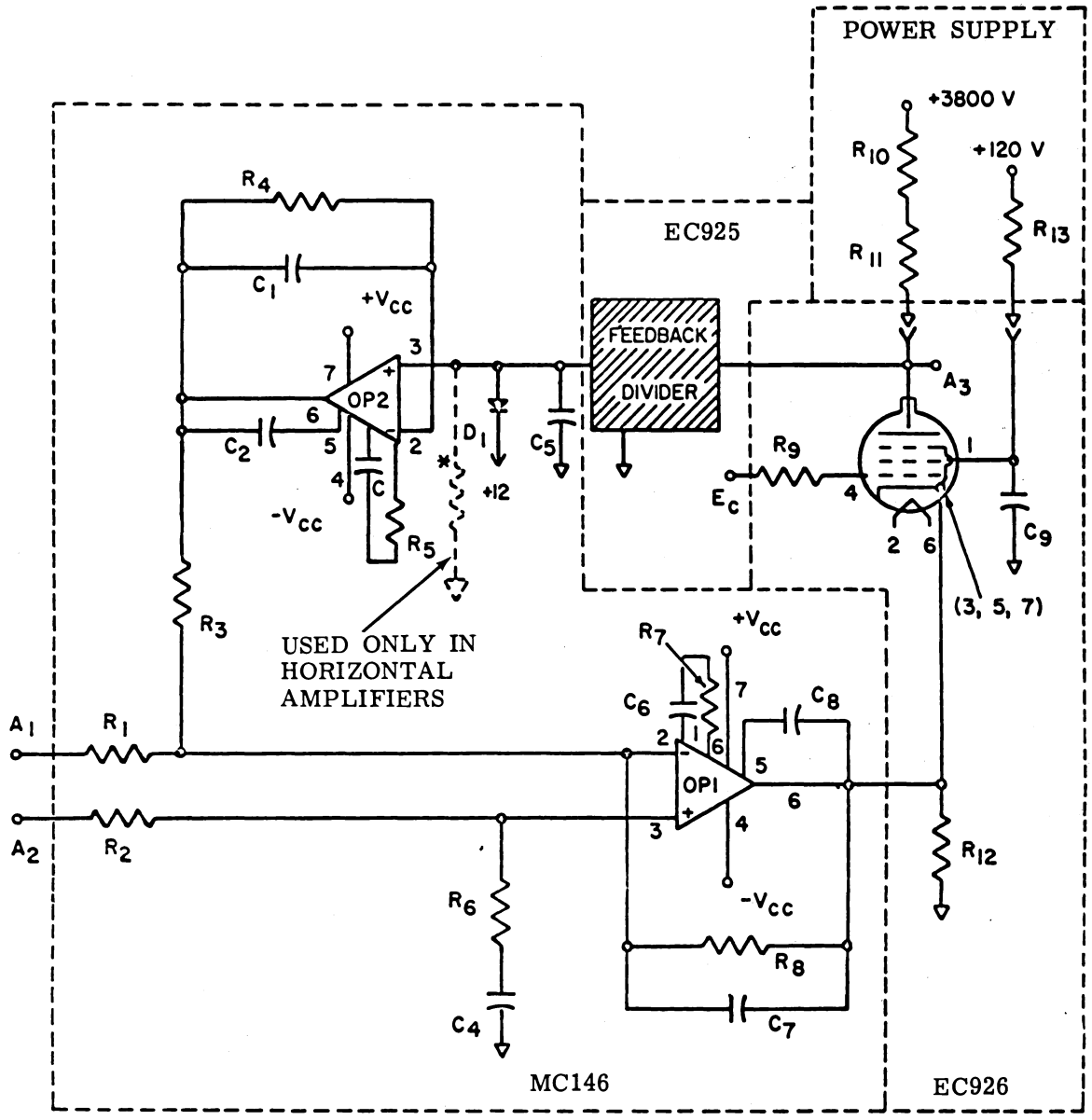
3.116 The level is determined by the feedback resistor (R100) and level resistor (R104). At this level all of the current sources are off and the output voltage (at OP17-6) will go to a level such that the voltage at the junction of the feedback and level resistors will maintain the constant differential (0 v) across the two inputs of the operational amplifier. The feedback resistor determines the size of each step. The input resistor (R102) connects the noninverting input of the operational amplifier to a reference voltage. This reference voltage determines the crossover voltage level, which will be between 6.400 and 7.333 volts. The analog output of the horizontal digital-to-analog converter is coupled directly to the horizontal high voltage amplifiers. Each set of deflection electrodes on the recorder is used to print two characters, left and right. In order to do this, there must be a shift in the horizontal deflection voltage between printing levels for a left character and printing levels for a right character. This shift is introduced in the horizontal digital-to-analog converter by a NAND gate controlled by the L/R signal, pin C223, from the character generator. This input is treated in the same manner as changes in the binary inputs, which produce steps in the output voltage.

3.117 There are four vertical binary inputs and three control inputs that control NAND and field-effect transistor (FET) gates, respectively (V1, V2, V4, V8, B7, $\overline{B7}$, and JD at pins C221, C219, C217, C215, C213, C207, and C222). The vertical digital-to-analog converter is the same as the horizontal digital-to-analog converter with one exception: The left-right shift signal (L/R) is replaced by a number 8 binary level that represents a 0.8 ma sink.

3.118 The analog output of operational amplifier OP16-6 is fed to the inputs of two vertical switches, Q7S and Q9S. The purpose of these switches is to switch the analog signal to one of two sets of vertical high voltage amplifiers and also to introduce the jet down signal. The two sets of vertical high voltage amplifiers (V1 - V2 and V3 - V4) are connected to alternate sets of vertical deflection electrodes on the recorder through the power supply. Since two valving electrodes are on at one time, it is necessary to switch the vertical analog information from one set of the vertical high voltage amplifiers to another during printing. The vertical switches perform this function. It is also necessary to enable printing by only one set of deflection electrodes at a time. To do this, the ink is deflected down below the mask on the recorder for the nonprinting electrodes. The level needed to cause this (8260WD, Sheet 3) is introduced in vertical switches Q8 and Q10.

3.119 The vertical switches are controlled by a binary output signal, its complement, and the jet down signal (B7, $\overline{B7}$, and JD at pins C213, C207, and C222) from the character generator. Each vertical switch is turned on or off by these signals via the FET gates. Each vertical switch is composed of a two-channel FET commutator. For the first vertical switch, the digital-to-analog channel Q7 is controlled by the normal control signal (B7), and the JD channel Q8 is controlled by the inverted control signal ($\overline{B7}$). In the second vertical switch the digital-to-analog channel Q9 is controlled by the inverted control signal ($\overline{B7}$), and the JD channel Q10 is controlled by the normal control signal (B7).

3.120 High Voltage Amplifiers: The high voltage amplifiers are operational amplifiers with gains of 4400. The high voltage output stage is a pentode tube amplifier stage. The plate load resistors are located in the high voltage power supply. The output voltage is coupled to a feedback divider network which is accurate to $\pm$0.50 percent. For a vertical amplifier the divider output voltage is 1/201 of the input voltage. The output from this divider is connected to the noninverting input of the operational amplifier OP2. A typical amplifier is shown in Figure 11. This operational amplifier has unity gain, is noninverting, and is an im-



Note: The operational amplifiers in this figure correspond to those in the six high voltage amplifiers as follows:

AMPLIFIER	OP1	OP2
V1U	OP2 (noninverting)	OP1
V1L	OP4 (inverting)	OP3
V2U	OP6 (noninverting)	OP5
V2L	OP8 (inverting)	OP7
HR	OP10 (noninverting)	OP9
HL	OP12 (inverting)	OP11

Figure 11 - Typical High Voltage Amplifiers with Operational Amplifiers for Vertical and Horizontal Deflection Electrodes

pedance transformer. The operational amplifier output is equal to the feedback voltage for the high voltage amplifier.

3.121 The input for an inverting high voltage amplifier is applied at A1. The feedback resistor R3 is equal to R1 but, effectively, a feedback resistor 4400 times greater is present due to the feedback divider network. A reference voltage is applied at A2 to ensure the crossover voltage level of the high voltage deflection output signal. Operational amplifier OP1 is an inverting amplifier with a gain of 4400 and is used to cathode modulate the high voltage output stage. The high voltage output is taken from point A3. An inverting high voltage amplifier is used to drive the vertical lower electrode (or the left electrode for the horizontal) on the recorder (8260WD, Sheet 2).

3.122 The input for a noninverting high voltage amplifier is applied at A2. The crossover level of the output is controlled by the crossover level of the input. The remainder of the circuitry is the same as that for an inverting amplifier. The noninverting high voltage amplifier is used to drive the vertical upper electrode (or the right electrode for the horizontal) on the recorder.

3.123 Relay Driver — Overvoltage Protection Circuit: To prevent possible damage to the recorder, the deflection signals at the plate load outputs are sensed via an OR gate (CR7 through CR12) for an overvoltage condition. The sensed levels are tied to the inverting input of differential amplifier OP13-2. With the noninverting input tied to a 10 v reference voltage (OP13-3), the output of the differential amplifier will be high when the inverting input is less than 10 v. When the inverting input goes higher than 10 v, the output goes low, causing the output (8) of dc flip-flop ML1 to go low. The output of the dc flip-flop is used to control two power drivers. One driver is used to turn off the READY indicating lamp (via CR15). This driver can be controlled by an alternate input signal at C201. The other driver is clamped in the off condition at its input to the output stage (collector of Q2) for overvoltage conditions, causing all motors and high voltage to turn off. This second driver is normally controlled by an input signal (at C209) from the interface circuitry for automatic turn-on. The outputs (C203 and C205) can sink up to 60 ma and withstand 60 volts. The dc flip-flop is reset from the READY button on the function strip. R60 and CR8 are used to insure that the flip-flop output ML1-8 is high after power turn-on.

3.124 Power Supplies: The low voltage reference supply on MC146 produces the required reference voltages from the +30 v and -12 v outputs of the high voltage supply (DAPS). Two voltages, +18 v and -6 v, are produced from the +30 v and -12 v inputs, respectively. These voltages are zener-regulated at 200 ma. Two voltage-dropping resistors (R89 and R90) are used to drop the voltage from +30 v to +18 v, and from -12.0 v to -6 v. Zener diodes CR23 and CR24 are used as the regulators. These voltages are the supply voltages for the operational amplifiers.

3.125 By the use of a zener reference diode (CR25) and an operational amplifier (OP15), dc output reference voltages of +12.000 v, 10.000 v, 9.500 v, 7.000 v, 6.750 v, 6.200 v, and 4.000 v are produced. The zener diode provides a reference voltage at the noninverting input of the operational amplifier. It is biased by resistor R105 connected to the output which is the most stable voltage source available. Part of the output voltage, the amount determined by the variable divider (R106, R107, and R108) at the output, is fed back to the inverting input of operational amplifier OP15. Hence, the output voltage will stabilize at a value at which this feedback voltage equals approximately the zener reference voltage. By adjusting potentiometer R107, the output can be regulated within ± 0.5 v and is set so that the output is 12.000 ± 0.050 v. A resistor divider network (R109 - R115) produces the remaining reference voltages. The divider current is approximately 10 ma, which is much greater than the load currents, so regulation is not affected by the load currents.

POWER SUPPLY

3.126 The power supply furnishes multivoltage outputs for the other modules of the set. Both low and high dc voltages plus three ac voltages are supplied. The power supply is housed in the DAPS module, which is shown with its protective cover in Figure 12 and with the cover removed in Figure 13.

CAUTION: BECAUSE OF THE SHOCK HAZARD PRESENT, THE COVER SHOULD NOT BE REMOVED FROM THE POWER SUPPLY.

A. General

3.127 The power supply receives 117 v ac, 60 Hz from the line and transforms, rectifies, and filters it to supply +3900 v, +550 v, +120 v, +48 v, +30 v, +6 v, and -12 v dc. It fuses the 117 v ac (nominal) line voltage and

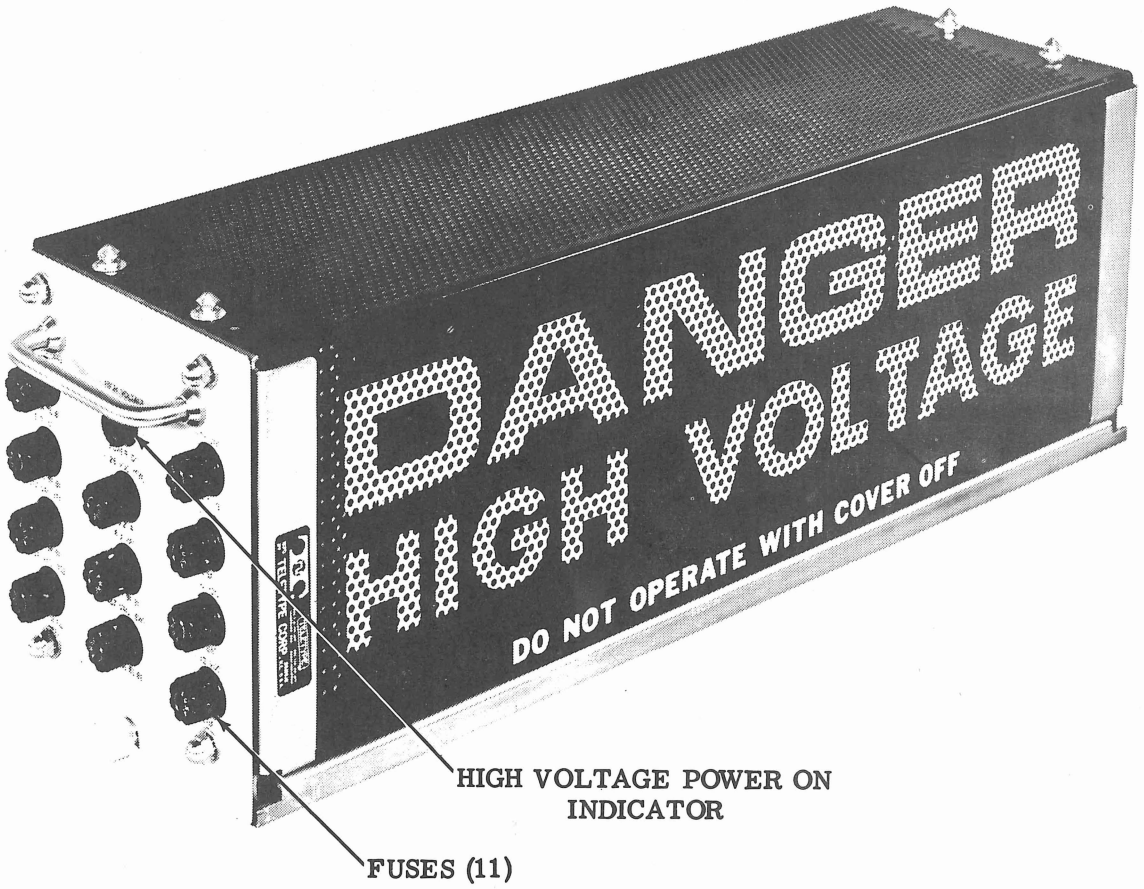
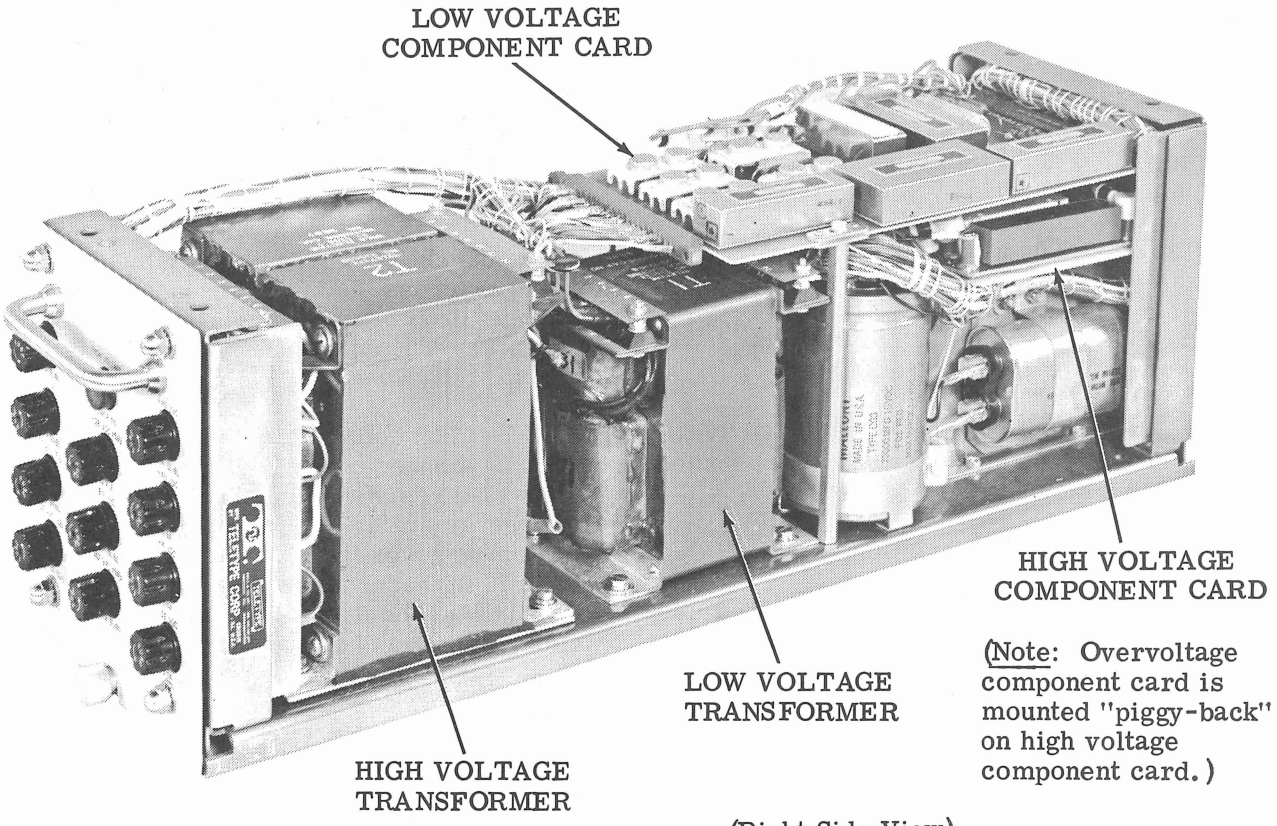


Figure 12 - Power Supply (DAPS) With Cover

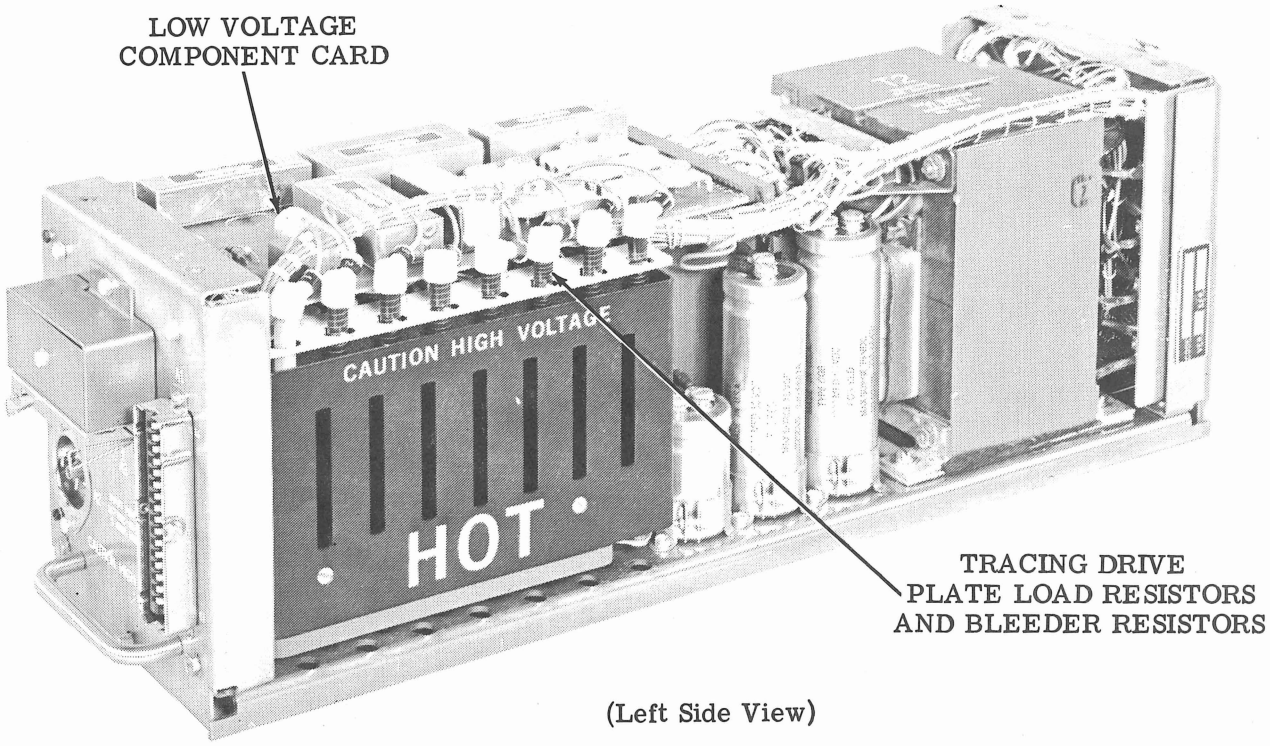
supplies it unchanged, and it steps down the line voltage to supply 6.3 v ac rms. It also provides a fused 167 v ac peak output.

3.128 The two high voltage outputs are supplied to the printer drive module, where +550 v is switched to two adjacent valving electrodes (out of 40) and +3900 v is connected to the plates of the six high voltage amplifiers used in tracing character shapes (the plate load resistors for these amplifiers are located in the power supply). Of the low voltage outputs, +120 v is connected to the screen grids of the high voltage amplifiers in the printer drive; +48 v is connected to the interface (for the control panel and a connection to the printer drive) and the character generator (for the X-drivers, Y-drivers, and Z-drivers); +30 v is connected to the printer drive (to produce +18 v for internal use) and the ink heater and line feed bracket assembly (to drive the paper transport escapement magnet drivers); +6 v is connected to all modules for use of the logic gates; and -12 v is connected to the interface (for the data set and data set control and receiving distributor cards) and the printer drive (to produce -6 v for internal use). The ac voltages have the following uses: 6.3 v ac is used to heat the filaments of the high voltage amplifier tubes; 117 v ac is used for the data set, the paper transport motors, the recorder ink heater, and the discrete calling generator motor (if present); and 167 v ac peak is presented to an auxiliary power supply which is part of the paper transport to be converted to +10,000 v for the platen, +5000 v for the recorder mask, and -2500 v for a regulator which supplies -1900 v to the recorder manifold.

3.129 In addition to the power circuitry, the DAPS module also contains the auto on relay and four other relays which indicate that the high voltage is capable of turning on or is on.



(Right Side View)



(Left Side View)

Figure 13 - Power Supply (DAPS) with Cover Removed

3.130 Voltage and current ranges are as follows:

+3600 to +4000 v dc at 0 to 30 ma
+530 to +570 v dc at 0.0 to 2.6 ma
+90 to +130 v dc at 0 to 6 ma
+46.5 to +53.0 v dc at 0.0 to 1.0 amp
+25 to +39 v dc at 0.0 to 2.5 amp
+6.0 to +7.0 v dc at 0.0 to 3.0 amp
-10.5 to -13.5 v dc at 0.0 to 0.5 amp
164 to 171 v ac peak at 0 to 50 ma
105 to 230 v ac rms at 0.0 to 0.5 amp
5.7 to 6.7 v ac rms at 0 to 2 amp

3.131 Eleven fuses and a red HIGH VOLTAGE POWER ON indicator lamp are mounted on the module faceplate.

B. Detailed Circuit Description

3.132 The following description is divided into several parts: The high voltage section, low voltage section, control relay circuitry, and overvoltage section.

3.133 Refer to wiring diagrams 8255WD (schematic wiring diagram), 8261WD (actual wiring diagram), 325595 (overvoltage component board) and 325623 (low voltage component board).

High Voltage Section

3.134 The high voltage section of the power supply is basically a transformer-operated full wave voltage tripler. The ac input is supplied by the high voltage secondary of transformer T2, which provides 1200 v rms between either of its end terminals (8, 12) and the center tap (10). The center tap is grounded. The high voltage output is approximately 3900 v dc, the combined voltages of C2 and C4.

3.135 With power applied to the primary of T2, capacitor C2 charges through CR5 to the peak voltage across the upper half of the secondary on one alternation, and through CR7 to the peak voltage across the lower half of the secondary on the opposite alternation. Resistor R5 limits the charge current to a safe value.

3.136 C1 charges through CR6 and CR5 to the peak voltage across the lower half of the secondary on one alternation, and C3 charges through CR4 and CR7 to the peak voltage across the upper half of the secondary on the opposite alternation. The voltage across C1 is applied series aiding with half the secondary voltage to charge C4 to twice the peak half-secondary voltage on one alternation. The voltage across C3 is applied similarly, with the other half of the secondary voltage, to charge C4 to twice the peak half-secondary voltage on the opposite alternation. The voltages across C2 and C4 are series aiding with respect to the grounded center tap of T2. Thus, the dc voltage at the junction of R1, CR8, and CR9 is approximately three times the voltage across half the secondary (minus the voltage drops across the power supply components). The dc output is approximately +3900 volts.

3.137 The output of the high voltage supply is connected through reed relay KB2 to the plate load resistors (R1 through R6) of the high voltage amplifier tubes. The KB2 switching system removes the high voltage from the amplifiers if any hazardous operating conditions exist. The unswitched output is applied to bleeder resistor R7, which helps to improve the regulation of the supply and also serves as a discharge path (along with R1) for the capacitors if relay contacts KB2-3 and KB2-4 open.

3.138 Pins 2 and 7 of connector DAPS/A3 provide an interlock which removes the high voltage if DAPS/A3 is not in its socket. These two pins are connected through a wire strap in the printer drive module. With the connector in place, +48 v is applied to the coils of KB1 and KB2 on the high voltage circuit board. With these coils energized, the switched +3900 v and +550 v outputs are available.

3.139 The voltage across C2 is used to develop the +550 v output of the supply. Three zener diodes (CR1, CR2, and CR3) are connected in series with resistors R3 and R4 to the positive terminal of C2. The diodes are rated to provide a total voltage drop of 550 v. This voltage is switched through control relay terminals KB1-1 and KB1-2. Bleeder resistor R2 serves as a dummy load for the +550 v output.

3.140 Terminal K of connector J2 on the low voltage component board connects to terminal 6 of transformer T2. This supplies 120 v ac to the anode of CR14 on the low voltage component board. Capacitor C5 charges to the peak voltage between terminals 6 and 10 of T2 on the alternation during which CR14 conducts. Bleeder resistor R5 is used to discharge C5 when the supply is turned off. The +120 v output is applied to the screen grids of the deflection amplifiers through current limiting resistors R6, R7, and R8.

3.141 The secondary between terminals 13 and 14 of T2 provides 167 v ac peak for the power supply on the paper transport. The common side of this winding (terminal 13) is fused by F5. The hot side (terminal 14) connects to terminal P of connector J2 on the low voltage component board and is switched by contacts 5 and 6 of relay KB2. The switched 167 v ac at terminal U of J2 is connected to the power supply of the paper transport.

3.142 The secondary connected to terminals 5, 7, and 11 of T2 serves as an ac source for the +28 v dc supply, and also supplies 6.3 v ac (rms) for the filaments of the deflection amplifier tubes and the coil voltage for reed relay KB1 on the low voltage component board. Terminals 5 and 7 of this winding connect to terminals E and V of connector J1 on the low voltage component board. This ac voltage is rectified by a full-wave bridge circuit in which CR8 and CR10 conduct on one alternation and CR7 and CR9 conduct on the other alternation. Capacitor C1, between terminals X and U of connector J1, charges to the peak ac voltage between terminals 5 and 11 of T2 during each alternation of secondary voltage. The +28 v output is applied from terminal U of J1 through fuse F10 to pin 3 of connector DAPS/A1. This voltage is used for the line feed and tracing drive circuitry.

3.143 The voltage between terminals 5 and 11 of T2 (6.3 v ac rms) is used to energize relay KB1 on the low voltage component board, and as filament voltage for the deflection amplifier tubes. Terminal 11 connects through fuse F6 to terminal D of connector J1 on the low voltage component board. This voltage energizes relay KB1. The 6.3 v ac is also connected to terminals 17 and 18 of DAPS/A1, and is fed to the filaments of the deflection amplifier tubes.

Low Voltage Section

3.144 The low voltage section of the power supply uses a step down transformer (T1) to provide the ac supply voltage for the rectifier circuit of the +6 v, -12 v and +48 v power sources. There are two tapped secondaries on T1, and the center taps of the two windings are tied together internally.

3.145 Terminals 6, 10, and 11 of T1 provide the ac voltage for the +48 v source on the low voltage component board. The anodes of diodes CR5 and CR6 connect to terminals 10 and 11, respectively, of T1. These diodes conduct alternately to provide full wave rectification and charge capacitor C4 to the peak voltage across half of the secondary. The center tap (6) of the T1 secondary connects to terminal Y of connector J2 on the low voltage component board, so the center tap is grounded. The +48 v output is taken from terminal 4 of DAPS/A1. Resistor R2 is a bleeder resistor used to discharge C4 when the power supply is turned off, and to improve the regulation of the supply. This voltage is fused by F9.

3.146 The other secondary of T1 provides the ac supply voltage for the +6 v and -12 v sources. Terminals 1 and 4 of T1 connect to terminals J and K of connector J1 on the low voltage component board. CR1 and CR2, in conjunction with R4 and C3, form a full-wave rectifier circuit similar to that of the +48 v supply. However, the cathodes of CR1 and CR2 are connected to the transformer terminals so that C3 is charged to a negative potential at its ungrounded terminal. Terminal H of connector J1 provides -12 v which is fused by F7 and applied to pin 1 of DAPS/A1.

3.147 Terminals 5 and 7 of T1 are connected to terminals R and L, respectively, of J1 on the low voltage component board. Diodes CR3 and CR4 form a full-wave rectifier to charge capacitor C2 to +6 v (early design units), which is applied from terminal P of connector J1 through fuse F8 to pin 2 of DAPS/A1. On late design units, diodes CR17 and CR18 are in series with CR3 and CR4, and the control relays are wired to interrupt the interlocks whenever this fuse is blown.

Control Relay Circuitry

3.148 The control relay circuitry is used to switch the +3900 v and +550 v dc, and the 167 v ac peak and 117 v ac rms, and to provide a ground for the PRINTER ON lamp. A control closure to ground is also provided to indicate that the relays have been energized.

3.149 Reed relay KB1 on the low voltage component board is energized by 6.3 v ac from terminals 5 and 11 of transformer T2. This voltage is applied between terminals D and E of connector J2 on the low voltage component board. With all interlock switches closed and no paper jam alarm, the voltage at terminal 16 of connector DAPS/A1 is +48 v. This terminal connects to terminal A of connector J1 on the low voltage component board, and +48 v therefore appears at KB1-3. On early design units, with

KB1 energized, the voltage also appears at KB1-4, KB3-3, KB4-3, KB3-5, and KB3-7. The +48 v is transferred through the closed contacts KB3-3, 4 to terminal 2 of relay coil KB4. Relay KB4 is a time delay relay, which energizes after 30 seconds +15 seconds. When KB4 energizes, contacts KB4-3 and KB4-4 close, and the +48 v is applied to terminal 1 of relay KB3. As soon as KB3 energizes, its normally closed contacts (KB3-3, 4) open and remove the voltage from KB4-1. This opens contacts KB4-3 and KB4-4 which initially energized KB3. However, contacts KB3-5 and KB3-6 are now closed to keep KB3 energized. R9 and C6 prevent KB3 from dropping out when KB4 de-energizes. On late design units, the control relay circuitry is arranged to enable KB4 only after main power is interrupted, so that the high voltage will come on immediately after the interlocks are closed. The +48 v dc source is used in place of the +48 v interlock signal at KB1-3, 4, and KB8-1, 2 is added in series with it. Relay KB8 is de-energized when fuse F8 blows.

3.150 With KB3 energized, +48 v is transferred through contacts KB3-7 and KB3-8 to terminal 2 of KB2, and to contact KB2-4. Terminal 1 of KB2 connects to terminal D of connector J2 and to terminal 16 of connector DAPS/A1. If the auto on provides a closure to ground, KB2 energizes. This transfers the +48 v through KB2-4 and KB2-3 to terminal H of connector J2, the ungrounded side of the high voltage indicator lamp.

3.151 Terminal H of connector J2 on the low voltage component board is also connected to terminal 2 of connector DAPS/A3 on the high voltage component board. The +48 v is therefore applied to terminal 1 of KB2 and terminal 3 of KB1 on the high voltage component board, energizing these two relays. The closed contacts of KB1 and KB2 provide the +550 v and +3900 v outputs at the high voltage supply terminals.

3.152 The voltage at KB2-2 on the low voltage component board is applied to terminal S of connector J2, and from this terminal to terminal 12 of connector DAPS/A1, the disconnect lead. If the interlock switches and the paper out switch are closed, there should be a +48 v reading at this point. This gives a check of switch conditions.

3.153 The 167 v ac peak voltage is switched through contacts 5 and 6 of relay KB2. This voltage, obtained from terminal 14 of T2, is transferred from terminal P to terminal U of connector J2 on the low voltage component board, and from this point to terminal 32 of connector DAPS/A1.

3.154 The +48 v at contact KB3-8 on the low voltage component board energizes relay KB7. Contacts KB7-3 and KB7-4 ground the low tape selectable lead at terminal R of connector J2.

3.155 With contacts KB2-3 and KB2-4 closed, relay KB5 is energized through CR13 by the +48 v. This closes contacts KB5-3 and KB5-4, providing a ground for the ready lead (terminal F of connector J2 and terminal 11 of DAPS/A1) and the PRINTER ON lamp (terminal A of J2 and terminal 15 of DAPS/A1).

Overvoltage Section

3.156 The main purpose of this section is to remove the high voltage from the output of the power supply if an overvoltage condition exists.

3.157 Under normal conditions relay KB2 on the low voltage component board is energized and +48 v is applied to terminal 5 of the high voltage component board. This energizes relays KB1 and KB2 on the high voltage component board, and the +3900 v output of the supply is distributed through the plate load resistors (R1-R6) to terminals 10, 8, 6, 5, 3, and 1 of connector DAPS/A3. These terminals supply high voltage to the plates of the vertical and horizontal amplifier tubes.

3.158 The voltages at the plate load resistors are also fed to terminals 1, 10, 2, 3, 9, and 8 of the overvoltage component board as an overvoltage monitor. With normal operating voltages in the deflection amplifier circuits, there is only a small leakage current through zener diodes CR1-CR4, and a small voltage appears across CR4. If a malfunction in one of the horizontal deflection amplifiers causes the voltage at terminal 10 or 8 of DAPS/A3 to exceed approximately +3075 v, diode CR10 or CR5 conducts and zener diodes CR1, CR2, and CR3 turn on if the overvoltage interlock (terminals 9 and 4 of DAPS/A3) is intact. Zener diode CR4 places +12 v at terminal 4 of the overvoltage component board, and at terminal 23 of connector DAPS/A1. Resistor R1 on the overvoltage component board is used to limit the current through the zener diodes, and to serve as a voltage divider with the plate load resistors when the diodes conduct.

3.159 If the voltage at terminal 6, 5, 3, or 1 of connector DAPS/A3 exceeds approximately +2050 v, due to a malfunction in one of the vertical amplifier circuits, zener diodes CR2, CR3, and CR4 turn on to again produce the +12 v at terminal 4 of the overvoltage board and terminal 23 of DAPS/A1.

3.160 The +12 v at terminal 23 of DAPS/A1 is detected by external logic circuits which open the ground lead at terminal D of connector J2 on the low voltage component board. This de-energizes relay KB2 and disables the power supply output.

Miscellaneous Outputs

3.161 The power supply provides ac operating voltages for the copylights and the ink heater. Terminal 2 of connector DAPS/A2 is the common side of the ac line voltage input to the power supply. The hot side of the line is applied through fuse F4 to terminal E of connector J2 on the low voltage component board, and through a strap to terminal B of J2. This terminal connects to terminal 30 of DAPS/A1, which is the hot side for the copylights. The hot side of the line also connects through fuse F3 to terminal 28 of connector DAPS/A1, which is the hot side for the ink heater.

CONTROL CIRCUIT CARDS

3.162 Three printed circuit cards on a three-tier card mounting assembly at the rear of the transport contain the electronic circuits for the pre-paper puller motor control, line feed motor regulator, and paper jam/paper out alarm. This assembly is illustrated in Figure 14. Refer to wiring diagrams 331197 (pre-paper puller motor control or paper brake), 330173 (line feed motor regulator), and 330152 (paper jam/paper out alarm) for the following explanations.

A. Pre-Paper Puller Motor Control (Paper Brake)

3.163 The pre-paper puller motor control (or paper brake) (circuit card TP331197) is the top card in the mounting assembly. In conjunction with the loop forming and loop sensing switches, it controls the turn-on and turn-off of

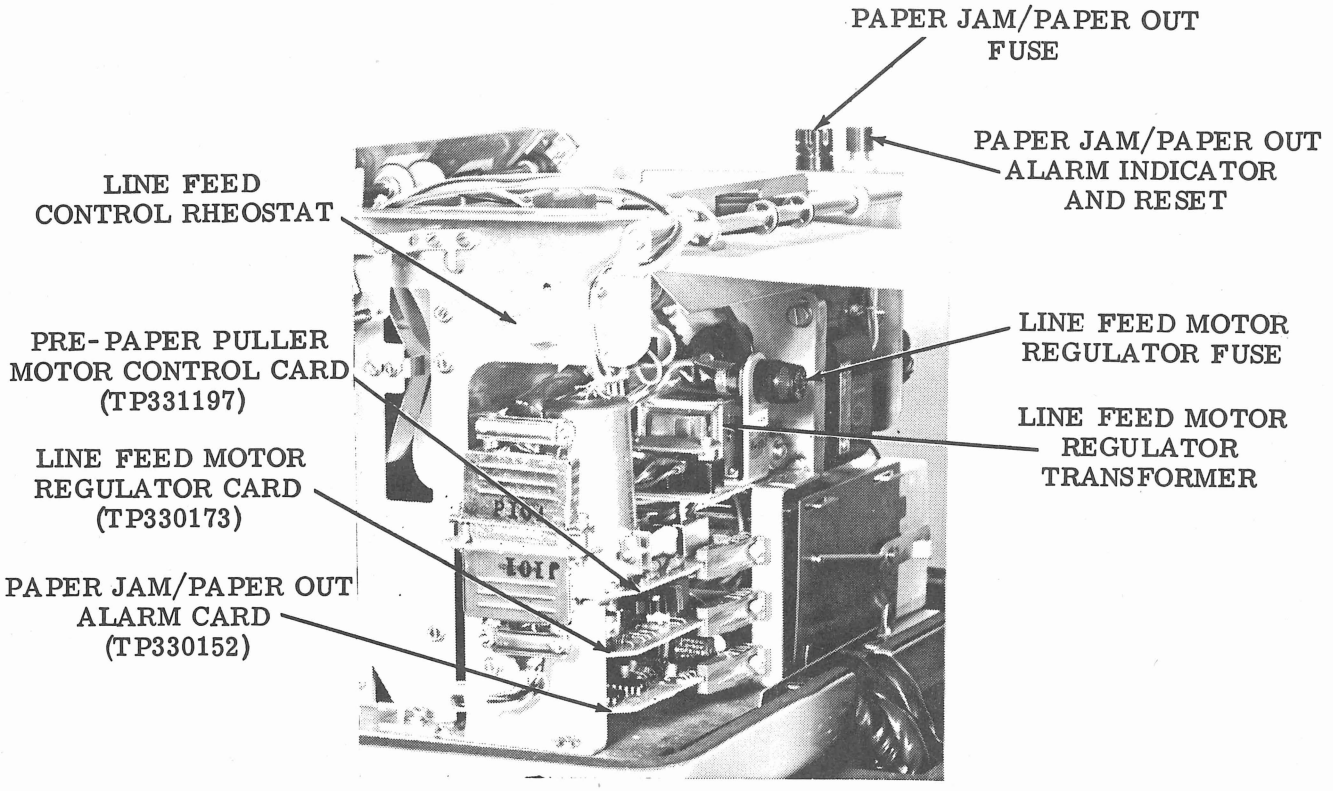


Figure 14 - Control Circuitry at Rear of Transport Base

the pre-paper puller motor, which forms and maintains a reservoir of paper to isolate the step-by-step line feed action from the inertia of the paper supply roll. The circuit also provides dynamic braking when the motor turns off.

3.164 The pre-paper puller motor is connected in series with triac TR1 across the ac line, which is connected between terminals L and S of the circuit card. The common contactors of the loop forming and loop sensing switches are normally in the N. C. positions shown in the schematic diagram. With both switches in the N. C. position the gate circuit of the triac is open, the triac is nonconductive, and the motor is disconnected from the ac line.

3.165 When the pressure roller bail is closed after threading the paper in the printer, the loop forming switch shifts to the N. O. position and connects the gate circuit of the triac to one side of the ac line. In early design units, the triac conducts, impressing the line voltage across the motor winding, and the pre-paper puller mechanism begins to strip paper from the supply roll. With the triac conducting, the gate circuit of SCR1 is effectively tied to one side of the ac line, and SCR1 conducts to quickly charge C1 to the polarity indicated.

3.166 TR1 continues to conduct until the paper loop no longer contacts the loop forming switch arm, and the common contactor reverts to the N. C. position. This removes the gate voltages from TR1 and SCR1, so the triac and the SCR both turn off. The pre-paper puller motor is now disconnected from the line, and the C1 charge path is also opened. The gate circuit of SCR2 is now connected to one side of the line, and SCR1 conducts, forming a discharge path for C1 through the motor winding, SCR2, and R9. The dc voltage across C1 is therefore applied to the motor to provide a dynamic braking action that brings the motor to an immediate stop.

3.167 As the line feed mechanism draws paper from the loop, the loop diminishes in size until it reaches a point where it no longer contacts the loop sensing switch arm. The loop sensing switch then shifts to the N. O. position, connecting the gate circuit of the triac to one side of the ac line. The triac conducts and the motor turns on to strip more paper from the supply roll. SCR2 is also gated to recharge C1. When the loop reaches its maximum size, the loop sensing switch reverts to the N.C. position, de-energizes the motor, and applies the dynamic braking voltage to the motor winding.

3.168 In late design units, operation is similar to that described for early design units except that SCR1 is not used for charging C1. Instead, the triac is used to charge C1. This change allows the brake circuit fuse to be increased from 0.3 amp to 0.5 amp slow blow.

3.169 Notice that the loop forming switch operates only to form the loop when the paper is initially threaded. Once the loop is formed, the pre-paper puller mechanism is under control of the loop sensing switch.

B. Line Feed Motor Regulator

3.170 The line feed motor regulator (circuit card TP330173) is the middle card in the mounting assembly. A transformer mounted on top of the circuit card assembly steps down the 117 v, 60 Hz ac line voltage to provide the operating voltage for a full-wave rectifier in the regulator circuit. The regulator samples the amplitude of the pulsating output of the rectifier to detect changes in line voltage. The output of the regulator controls the conduction interval of the triac in series with the line feed motor. As a result, the average motor current, and thus the motor torque, remains reasonably constant despite variations in line voltage.

3.171 The regulator action begins in the Q1 stage, which receives a pulsating, unfiltered signal from the output of a full-wave rectifier (CR1, CR2) operating from the center-tapped secondary of a step down transformer. The ac voltage from either end of the transformer secondary to the grounded center tap is 12 volts rms at a line voltage of 117 volts rms, so the peak value of the rectifier output is approximately 17 volts. This voltage is applied to a voltage divider consisting of R1 and R2. The voltage across R2 is used as a driving signal for the base of Q1.

3.172 The pulsating voltage is filtered by C1 to provide a dc voltage of approximately 17 volts across zener diode CR4 and emitter resistor R3 in series. With a zener rating of 13 volts, the drop across R3 is 4 volts, which serves as a reverse bias for the base-emitter junction of Q1.

3.173 Transistor Q1 conducts only when the voltage across R2 exceeds 4 volts. The collector signal of Q1 is amplified by Q2 and Q3, and applied to the gate of triac Q4. The anode current of Q4 is carried by the line feed motor. By regulating the conduction interval of Q4, and

consequently the average anode current, the regulator circuit stabilizes the motor torque. The line feed control rheostat can be set to provide the desired torque under normal line voltage conditions.

3.174 To illustrate the regulator action, suppose the line voltage increases. This results in an increase in secondary voltage, and a corresponding increase in the reverse bias in the base-emitter circuit of Q1, so the voltage across R2 must rise to a higher level to cause Q1 to conduct. This narrows the pulse of Q1 collector current, which in turn narrows the pulse of anode current supplied to the line feed motor by the triac. Although the line voltage has increased, which tends to increase the peak amplitude of the motor current, there is a compensating decrease in the duration of motor current which keeps the average motor current reasonably constant. Since torque is proportional to average motor current, the torque is stabilized within reasonable limits.

3.175 Relay K1 is energized by the +48 v output of the power supply. If all conditions for operation of the printer are satisfied, the +48 v output is present from the supply and K1 energizes to permit normal operation of the line feed control circuitry. If the +48 v output is not present, due to a paper jam, open interlock, etc, K1 de-energizes to prevent conduction of Q4, and the line feed motor will not run.

C. Paper Jam/Paper Out Alarm

3.176 The paper jam/paper out alarm circuit card (TP330152) is the bottom card in the mounting assembly. It serves to turn off the printer and give a visual alarm (red indicator lamp on left side frame of transport) if the pre-paper puller motor does not turn on to replenish the paper loop within 28 or 29 line feed steps (early design units) or if the paper-out switch closes (late design units). Thus, it serves to detect a paper jam or a lack of paper on the supply reel.

3.177 The heart of the alarm circuit on early design units is a binary counter, which consists of two dual J-K flip-flops, MLB1 and MLB2. One output of each flip-flop is connected to a separate input of a four-input NAND gate (MLG1-5, 4, 2, 1). When the line feed count reaches 28 or 29, the normal (N) output of the first flip-flop and the inverted (I) outputs of the other three flip-flops will be high, placing highs on all four inputs of the NAND gate.

3.178 The input signals to the alarm are positive pulses from one of the line feed magnet drivers. Since the magnet driver is a binary circuit, this positive pulse occurs on every other line feed. Also, depending on the initial state of the driver when the count begins, the first pulse may occur on the first line feed, or it may occur on the second line feed. (This is why the alarm may occur at either 28 or 29 line feeds.) The pulses are applied at lead N of the circuit card, through a pulse shaping network to the base of transistor Q1. The negative-going pulses at the Q1 collector are applied to clock pulse input CP1 of MLB1. Each drive pulse advances the count stored in the counter.

3.179 If the pre-paper puller motor does not turn on before the count advances to 14 (the equivalent of 28 line feeds), due to a jam or a lack of paper on the supply roll, highs appear at MLG1-5, 4, 2, and 1. This forces MLG1-6 low, MLG2-6 high, and MLG2-3 low. The low at MLG2-3 is applied to MLG1-9, forcing MLG1-8 high. This high forward biases Q5, energizing relay KB1. The normally closed contacts of KB1 (terminals A and C of the circuit card) are in series with the interlock string, and with KB1 energized, the interlock string is opened to remove power from the transport. With Q5 conducting heavily, lead B is grounded to turn on the paper jam alarm lamp on the left side frame of the transport.

3.180 On late design units, the binary counter is replaced by a paper-out switch on the paper transport which is normally open. If paper runs out, this switch closes, supplying ground from pin K on late design card TP330152 to pin B on this card. This energizes relays KB1 and KB2. When KB1 energizes, its normally-closed contact opens and interrupts the interlock string (via pins A and C, as explained in 3.179). When KB2 energizes, its normally-closed contact opens and removes 117 v ac from the pre-paper puller motor (via pins P and M, in series with the loop sensing switch).

3.181 Once the jam has been corrected, or a new roll of paper has been installed, the operator can restore circuit operation by pressing the manual reset button (illuminated by the alarm lamp) on the left side frame of the transport. On early design units, this grounds lead F to remove the forward bias of transistor Q2. The resultant increase in Q2 collector voltage saturates Q3, producing a drop in Q3 collector voltage. This represents a low at MLG2-12, forcing MLG2-11 high and MLG2-8 low. The low

at MLG2-8 resets all four stages of the binary counter, and MLG1-6 goes high. This high causes MLG2-6 to go low, MLG2-3 to go high, and MLG1-8 to go low, removing the forward bias from Q5 and de-energizing KB1 to close the interlock string and energize the transport. The paper jam alarm also turns off. Late design units are reset by the paper-out switch opening when the new roll of paper is installed. Depressing the manual reset button is not necessary in this case.

3.182 With the paper supply system functioning normally, the counter on early design units is automatically reset before the line feed count reaches 28, so the alarm circuit does not trigger. The automatic reset is provided by relay KB3, which is connected across the pre-paper puller motor and is therefore energized each time the motor is turned on by the loop sensing switch. This closes the KB3 contacts in the base circuit of Q4, forward biasing Q4 and causing its collector voltage to go low. The low is applied to the clear direct inputs of all four counter stages, restoring the count to zero.

3.183 On early design units, relay KB2 is a time delay relay used to disable the paper transport if the pre-paper puller motor does not shut off within 480 milliseconds. The relay coil is connected across the pre-paper puller motor and is energized whenever the motor turns on. However, there is a 480-millisecond delay before the KB2 contacts close. If the pre-paper puller motor stops within this interval, as is the normal case, the KB2 contacts do not close and the circuit functions normally. If the motor is on for longer than 480 milliseconds, the KB2 contacts close and ground MLG1-6. This low at MLG1-6 is gated through MLG2-6, MLG2-3, and MLG1-8 to turn on Q5 and energize KB1, disabling the transport.

3.184 On late design units, relay KB3 and one-shot MLA1 are used to disable the paper transport if the pre-paper puller motor does not shut off within 1.2 seconds. The relay coil is connected across the pre-paper puller motor and is energized whenever the motor turns on. When it is energized, the KB3 contacts close and ground MLB1-2. The high output of this gate is connected to the input of one-shot MLA1, which begins its 1.2 second time-out period. If the pre-paper puller motor stops within this interval, as is the normal case, the relay drops out, the high is removed from MLB1-6, and the one-shot is automatically reset. If the motor is on for longer than 1.2 seconds, the one shot times out and fires. The low output of MLA1-8 is then gated through MLC1-3, MLC1-11, and MLB1-8 to turn on Q2 and energize KB1 and KB2, disabling the transport as in 3.180. However, in this case the paper jam/paper-out alarm is not self-resetting when the trouble is corrected; the operator must depress the manual reset button.

INK HEATER AND LINE FEED BRACKET ASSEMBLY

3.185 The ink heater and line feed bracket assembly (TP325801) has two functions: It supplies the operating voltage for the ink heater and ink pump in the recorder, and it provides the drive current for the line feed magnets in the paper transport. This assembly (Figure 15) is mounted above the modules, to the left of the data set.

3.186 The ink heater and ink pump in the recorder (DAR) operate at 26 v ac supplied by the transformer on the ink heater and line feed bracket assembly. The primary of this transformer is connected to the 117 v ac line, and the line voltage is stepped down to provide the 26 v across the secondary. Refer to 8488WD for the schematic diagram.

3.187 The circuit card (TP303930) on this assembly develops the 1 amp driving current for the line feed magnets. Refer to wiring diagram 303930 for the following explanation of the circuit.

3.188 The card contains a medium power flip-flop (Q1, Q2) which drives the power transistors (Q3, Q4) that energize the line feed magnet coils mounted inside the left frame of the paper transport. The supply voltage for this circuit is the +30 v output of the DAPS power supply. The signal input is a -6 v line feed pulse from the character generator (DAG) module.

3.189 With the supply voltage present, but with no line feed signal at the input, the flip-flop will assume one of its stable states; Q1 conducting and Q2 cut off, or vice versa. If Q1 is conducting, its collector voltage is low and there is no driving signal for the base of Q4. As a result, Q4 conduction is very low and its collector current is not sufficient to energize the magnet in its collector circuit. With Q2 cut off, its collector voltage is high. This high positive voltage applied to the base of Q3 causes Q3 to conduct heavily, energizing the magnet in the

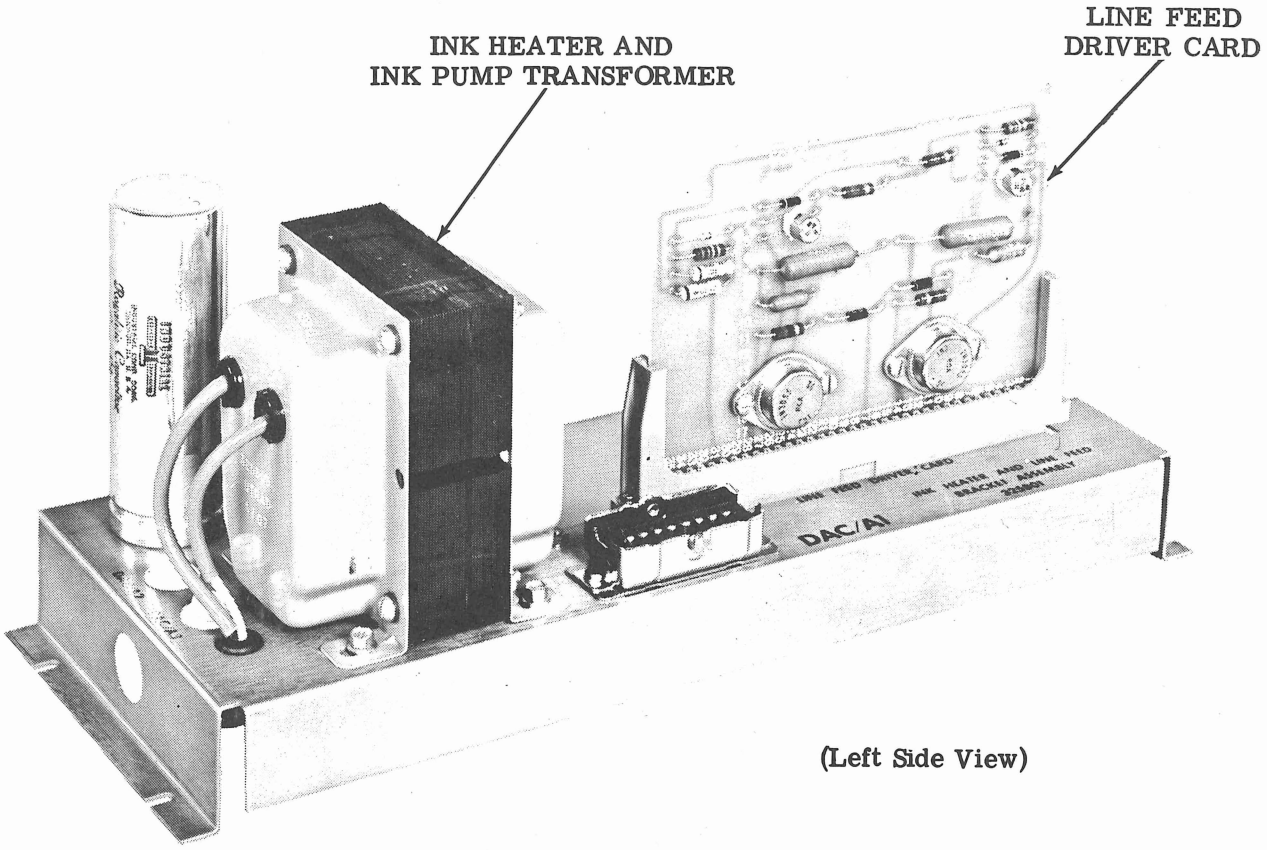


Figure 15 - Ink Heater and Line Feed Bracket Assembly

Q3 collector circuit. The circuit remains in this state until a line feed pulse appears at the input.

3.190 A -6 v line feed pulse at the input is fed to the conductive transistor by steering diode CR1 or CR2. Assuming Q1 is conductive at the time the pulse arrives, CR1 feeds the pulse to Q1, and CR2 blocks the pulse from Q2. The line feed pulse changes the state of the flip-flop, which in turn changes the states of the power transistors and magnet coils. Each line feed pulse triggers the flip-flop so that the magnets are alternately energized and de-energized.

3.191 The 100 mfd electrolytic capacitor and two 25 ohm resistors mounted on this assembly serve as a filter in the magnet circuit.

PAPER WINDER (Optional Feature)

3.192 An automatic paper winder is an optional feature of the DATASPEED Page Printer. The winder itself mounts at the rear of the top shelf of the cabinet, with the motor and control circuit card (TP331200) mounted on the underside of the rear of the top frame (Figure 16). The on/off rocker switch and the automatic control switch are mounted in the right bracket assembly of the winder.

3.193 As the paper leaves the printing position (the face of the platen), it passes between the paper tensioner idler rollers and drive roller, up over the paper slack arm to the paper winder spindle. The pivoted end of the paper slack arm is spring loaded so that the resting position of the slack arm is upward as shown in Figure 16. However, tension on the paper between the paper tensioner rollers and the take-up reel forces the free end of the paper slack arm downward.

3.194 As paper is stepped through the paper tensioner, the length of paper between this point and the tape-up reel increases, and the slack arm is drawn upward by the springs in both

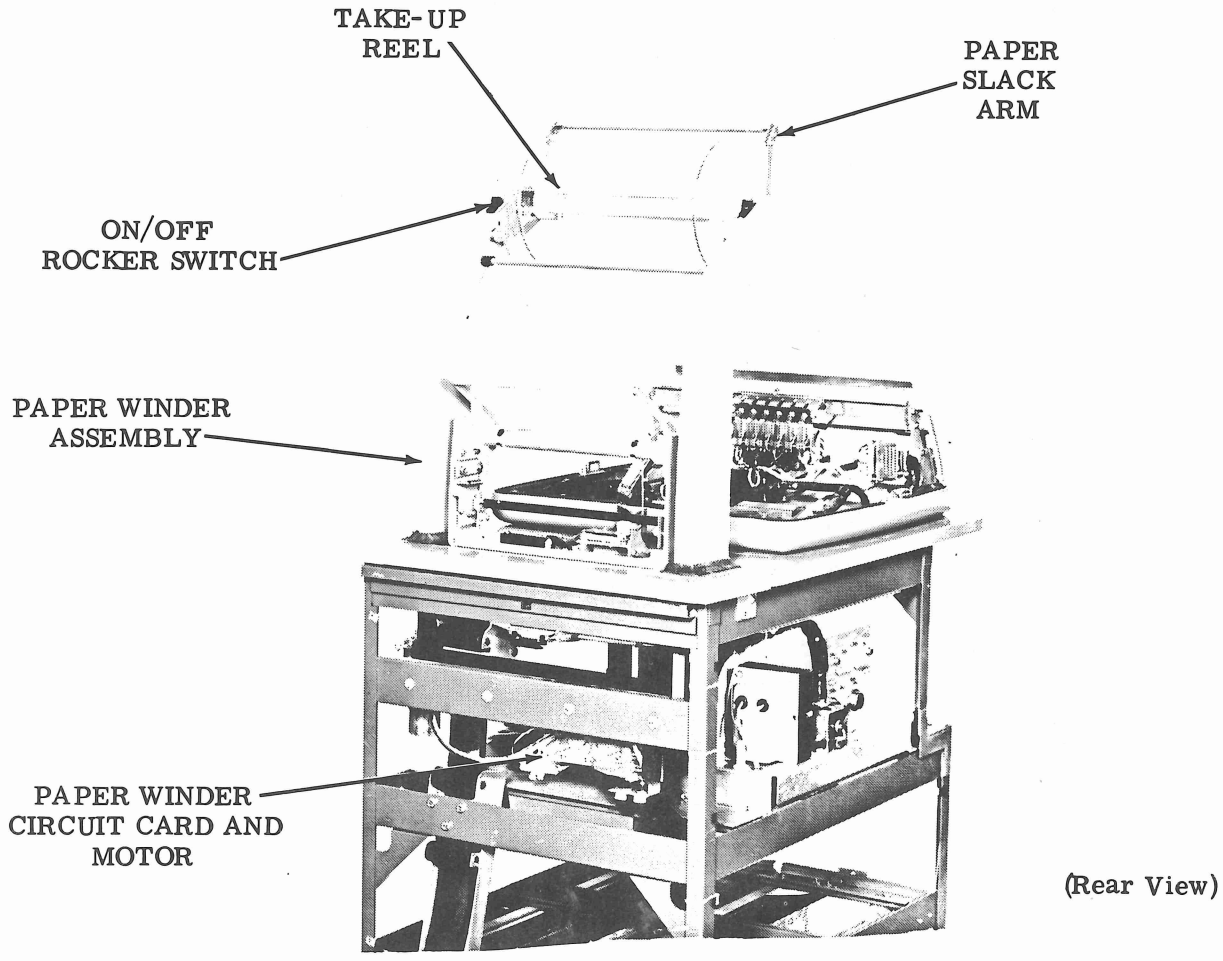


Figure 16 - Top Frame of DATASPEED Printer Showing Paper Winder Assembly

paper winder brackets. When the slack arm reaches its upper position, a cam on its pivot end actuates the switch that energizes the paper winder circuit. The paper winder motor turns on, winding the paper on the take-up reel and reducing the length of paper between the paper tensioner and take-up reel. This forces the slack arm down, deactivating the control switch. The control circuitry de-energizes the paper winder motor, and also applies a dynamic braking voltage that brings it to a quick stop to prevent tearing the paper.

3.195 Refer to wiring diagram 331200 for the following explanation.

3.196 The paper winder motor is connected in series with triac TR1 across the ac line. With the actuating switch in the position shown in the schematic diagram (paper slack arm down), the gate circuit is open and the triac is nonconductive, opening the motor circuit.

3.197 When the switch is actuated by the paper slack arm, it connects the gate circuit of TR1 to one side of the ac line (L), and the triac conducts. This energizes the motor, and the take-up reel begins to turn. At the same time, the gate circuit of SCR2 is connected through a fuse and the triac to one side of the ac line. SCR2 conducts, charging a large electrolytic capacitor (mounted separately).

3.198 As paper is wound onto the take-up reel, the paper slack arm is forced downward until the cam disengages from the switch. The switch reverts to the position shown in the schematic diagram, opening the gate circuits of TR1 and SCR2. This de-energizes the motor and opens the capacitor charge path.

3.199 With the switch in this position, the gate circuit of SCR1 is connected to one side of the line. SCR1 conducts to complete a discharge path for the capacitor through the motor winding and current limiting resistor R3. The capacitor voltage brakes the motor, preventing it from coasting and possibly tearing the paper. Late design units have an improved component mounting arrangement to prevent potential failure of triac TR1.

DATS1 SIMULATOR

A. General

3.200 The DATS1 simulator (Figure 17) is a test set which serves as a signal source for the DATASPEED Page Printer Set, and as an adapter to permit use of a conventional voltmeter in measuring voltages throughout the printer. The data output of the DATS1 may be applied directly to the input control circuits of the character generator (DAG) module to trouble-shoot or check the operation of the printer. There is a choice of single character output, or repeat character output at approximately 1100 wpm. Any code character signal can be selected by changing the settings of the CODE LEVEL switches.

3.201 The DATS1 is equipped with a low voltage and high voltage probe, and with binding posts to connect a voltmeter for voltage measurements. The high voltage probe incorporates a 1000:1 voltage divider which permits the use of a low voltage meter in measuring the high voltages at various points in the printer. The same meter can be used, through the simulator, to measure low voltage pulses.

Note: These probes may not be used unless the DATS1 is properly connected to the DATASPEED printer and all supply voltages are present.

3.202 The simulator is a self-contained, portable unit which obtains its power from the printer to which it is connected. The electronic circuitry is contained on a single circuit card housed in an aluminum case with cover. An attached cable is terminated in a TP325720 connector which mates with the DAIF/AA1 connector of an DATASPEED printer. The low voltage and high voltage probes are part of the cable assembly.

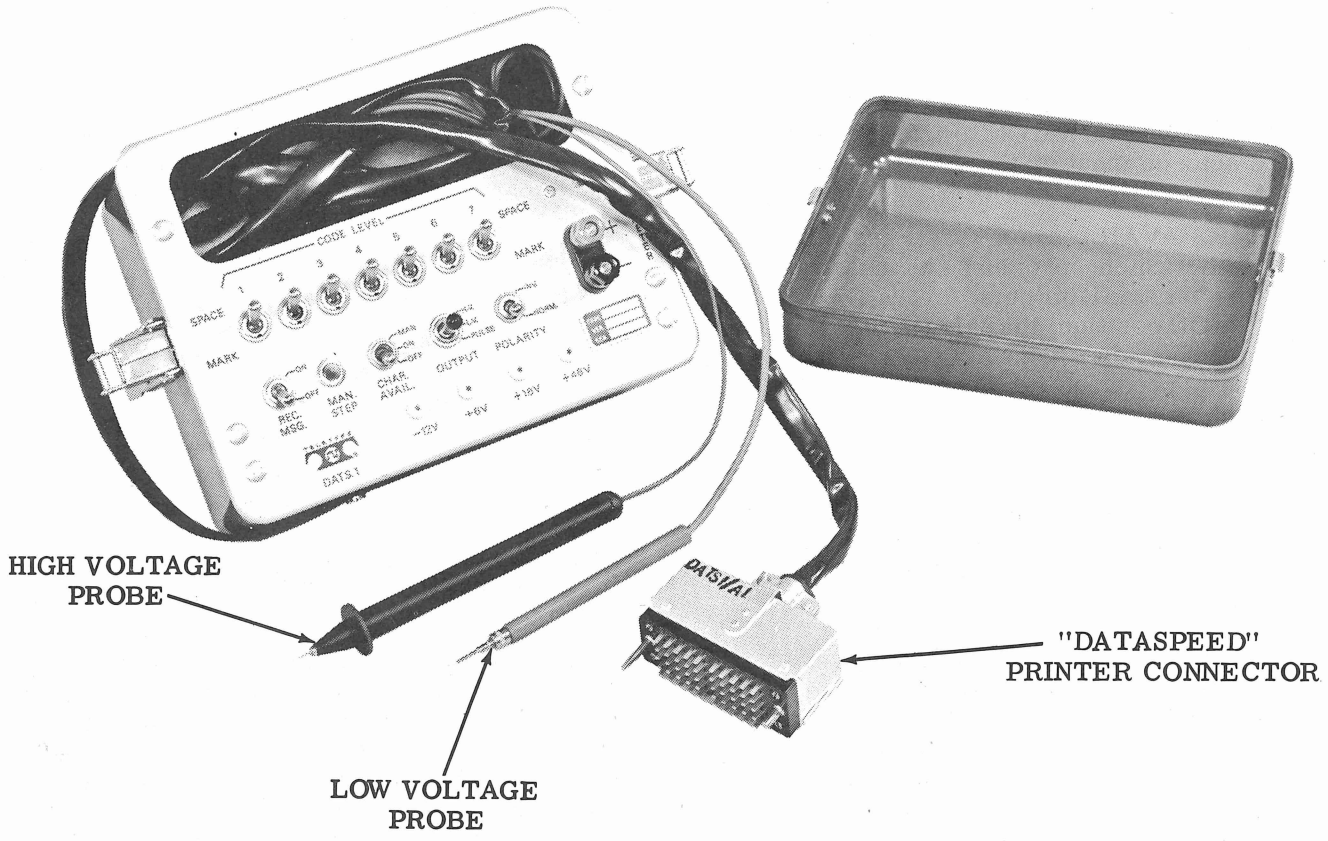


Figure 17 - DATS1 Simulator

3.203 The following output signals are provided:

Data — A parallel seven-bit signal which may be applied to the input of the DAG module to simulate the data signals normally received from the interface. A switch closure to common represents a space, and an open circuit represents a mark.

Character Available — A negative-going pulse (+6 v to 0 v) applied to the input of the DAG.

Receive Message — A switch closure to common applied to the auto-on input of the power supply (DAPS) to turn on the high voltage.

Four jacks are provided along the bottom of the panel to monitor the low dc voltage of the printer.

3.204 The panel controls and their functions are as follows:

CODE LEVEL — Seven toggle switches used to set up the desired data character. MARK and SPACE positions are indicated on the panel.

REC. MSG. — A two-position toggle switch which may be turned ON to provide a signal for the auto-on input of the DAPS power supply.

CHAR. AVAIL. — A three-position toggle switch which provides a negative-going character available pulse for the DAG module. In the ON position, the pulse is repeated every 9 milliseconds. In the MAN position, a single pulse is produced each time the MAN. STEP switch is depressed.

MAN. STEP — A momentary contact push-button switch which develops a single character available pulse when depressed and released, provided the CHAR. AVAIL. switch is in the MAN position.

OUTPUT — A three-position lever switch which directs the desired voltage to the METER terminals on the panel. In the H.V. position it connects the output of the high voltage divider circuit to the METER terminals. In the L.V. position it connects the low voltage probe directly to the METER terminals. In the PULSE position it connects the input of the pulse detection circuitry to the low voltage probe, and the output to the METER terminals.

POLARITY — A two-position toggle switch which reverses the connections to the + and - METER terminals to permit measurement of positive or negative voltages without changing the meter connections. With the ground lead of the simulator connected to the ground point in the printer, the NORM. position is used to measure positive voltages, and the INV. position is used to measure negative voltages.

B. Detailed Circuit Description

3.205 The DATS1 simulator contains a single circuit card and attached cable. Refer to the schematic wiring diagrams of the TP322179 circuit card on wiring diagram 322179 for the following explanation.

Receive Message

3.206 With the REC. MSG. switch in the ON position, a contact closure to ground is presented to the auto-on input of the DAPS module in the printer. This turns on the high voltage to ready the printer for operation.

Character Selection

3.207 Any desired character may be programmed into the simulator by positioning the appropriate CODE LEVEL switches to their MARK or SPACE positions. In the MARK position the switch presents an open circuit for the input of the DAG module of the printer. In the SPACE position the switch provides a closure to circuit common.

Character Available

3.208 Once the REC. MSG. switch has turned on the high voltage in the printer, and the CODE LEVEL switches have been set to provide the desired character, a character available pulse must be presented to the control logic of the DAG module in order to print the character.

3.209 Repeating character available pulses at a specified rate (CHAR. AVAIL. switch ON) are generated by unijunction transistor Q3 in conjunction with flip-flop ML2-9. Q3 and its associated components form a unijunction oscillator with its pulse output applied to the clock pulse input (13) of ML2-9. With the CHAR. AVAIL. switch in the ON position, ML2-9

changes state on every cycle of the unijunction oscillator. The oscillator output is gated with the ML2-9 output to produce a negative pulse (from +6 v to 0 v) at ML1-6. This negative pulse also appears at the output of emitter follower transistors Q1 and Q2, where it is applied to terminal 9 of the DATS1/A1 connector. The pulses are continuous and appear at a character rate of approximately 1100 wpm. Resistor R1 in the oscillator circuit is adjusted for a period of 9 milliseconds between pulses.

3.210 With the CHAR. AVAIL. switch in the OFF position, the set direct input (10) of ML2-9 is connected to circuit common. This inhibits the flip-flop and prevents it from changing state, so there is no character available pulse at the output.

3.211 When the CHAR. AVAIL. switch is in the MAN position, flip-flop ML2-9 is inhibited by a zero at ML2-5, which is applied through the switch to the set direct input of ML2-9. Depressing the MAN. STEP pushbutton closes contact A and applies 0 v (circuit common) to ML1-1. This forces ML1-12 and clock input ML2-1 high (+6 v). When the pushbutton is released, the ground is removed from ML1-1, and ML1-12 goes low. This low, which also appears at ML2-1, causes ML2-5 to change states, releasing ML2-9 and allowing a negative-going character available pulse to appear at the output. The negative-going transition of the first pulse, which appears at ML1-2, forces ML1-12 and ML2-1 high. The positive transition of the output pulse forces ML1-2 high, forcing ML1-12 and ML2-1 low, and returning ML2-5 to its original state (ML2-5 low). This low at ML2-5 inhibits ML2-9 to prevent any additional pulse output. Thus, only one pulse is generated for each operation of the MAN. STEP pushbutton.

Pulse Detect Circuitry

3.212 When the OUTPUT switch is in the PULSE position, the low voltage probe of the simulator can be used to monitor low voltage pulses. The pulses are applied through the switch to the base circuit of Q4, and the amplified pulses at the collector of this transistor are used as a clock signal for ML3-5. Flip-flop ML3-5 changes state once for every pulse applied to the low voltage probe. The pulse at ML3-5 is applied to the base of Q5, and the amplified pulse at the Q5 collector is coupled through another section of the switch to the meter circuit.

3.213 With no pulses at the input of the pulse detect circuit, the output at the METER terminals is either +6 v or 0 v, depending on the state of ML3. A voltmeter connected to the output will register this reading. A single pulse applied to the input causes the flip-flop to change states, and the meter reading changes from +6 v to 0 v, or vice versa. A succession of pulses at the input causes the flip-flop to continuously change state. Because the inertia of the meter coil prevents it from following rapid voltage changes, the meter will read some intermediate value; for example, +3 v.

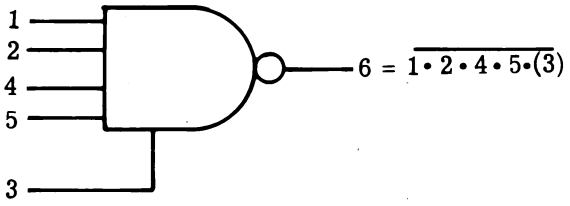
Note: The DATS1 simulator must not be used in this mode of operation if the indicated supply voltages are not present at the test point tip jacks along the bottom of the panel.

High Voltage Divider Network

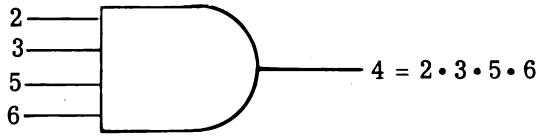
3.214 The high voltage test probe contains a 100 megohm resistor which, with 100 k ohm resistor R15, forms a voltage divider with a ratio of approximately 1000:1. With a voltage applied between the high voltage probe and ground, the portion of the voltage across R15 is applied to the noninverting input (3) of operational amplifier OP1. The output of OP1, at the junction of R16 and R17, is applied to the high voltage section of the OUTPUT switch. With the switch in the H.V. position, a voltage equal to approximately 1/1000 of the voltage at the high voltage probe is applied to the METER terminals of the simulator. This permits a low voltage meter to be used in measuring high voltages in the printer circuits.

Note: The DATS1 simulator must not be used in this mode of operation if the indicated supply voltages are not present at the test point tip jacks along the bottom of the panel.

4. APPENDIX - LOGIC SYMBOLS AND CONFIGURATIONS



NAND Gate (Extendable)



Extender (AND Gate)
(Also shown as four diodes connected together at outputs)

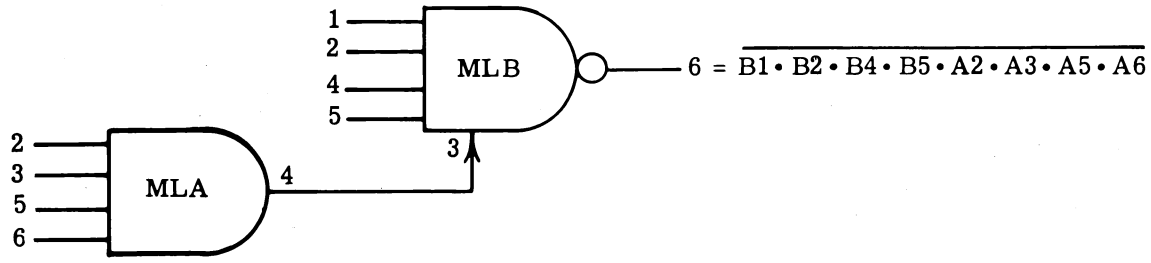
INPUTS					OUTPUT
1	2	4	5	3	6
1	1	1	1	(1)	0
0	X	X	X	(X)	1
X	0	X	X	(X)	1
X	X	0	X	(X)	1
X	X	X	0	(X)	1
X	X	X	X	(0)	1

(Output is low when all inputs are high and high when any or all inputs are low. Input 3 is for extender use only.)

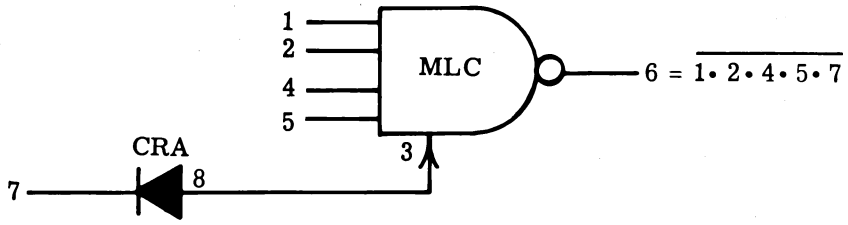
INPUTS				OUTPUT
2	3	5	6	4
1	1	1	1	1
0	X	X	X	0
X	0	X	X	0
X	X	0	X	0
X	X	X	0	0

(Output is high when all inputs are high and low when any or all inputs are low.)

Legend: 1 = High State (More Positive)
0 = Low State (More Negative)
X = State of Input Does Not Affect Output

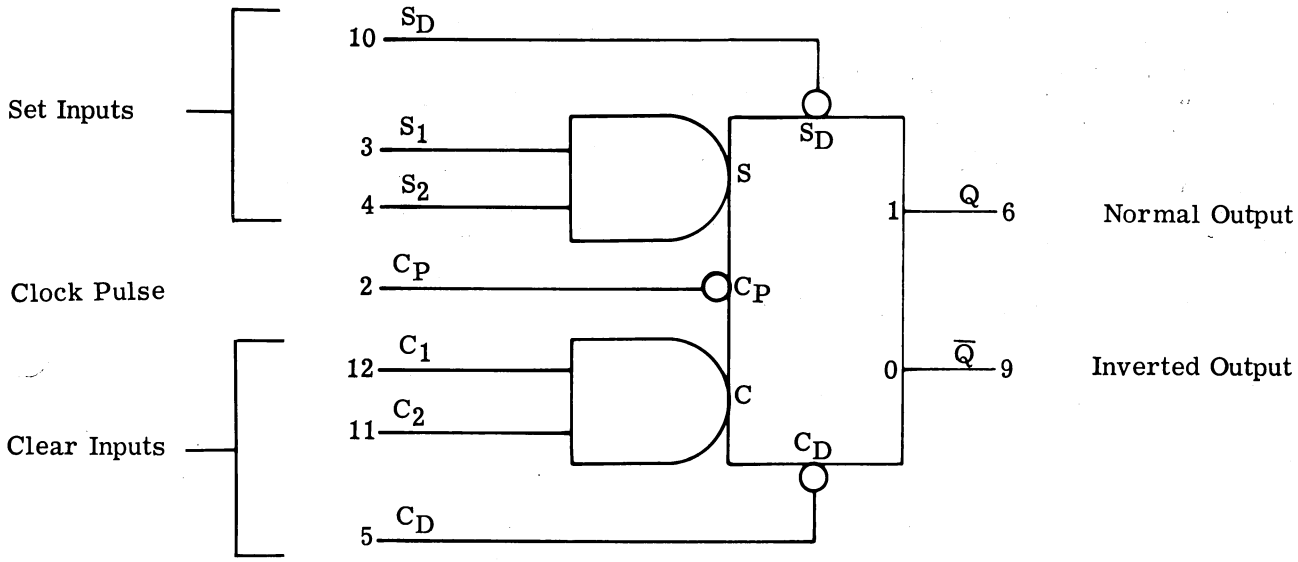


NAND Gate With Extender to Provide Four Additional Inputs



NAND Gate With Diode to Provide Additional Input

Figure 18 - NAND Gates and Extenders — Logic Symbols on Schematic Wiring Diagrams and Truth Tables



Clocked Flip-Flop

T_N				T_{N+1}
S_1	S_2	C_1	C_2	Q
0	X	0	X	NC
0	X	X	0	NC
X	0	0	X	NC
X	0	X	0	NC
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

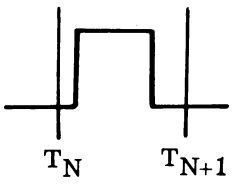
Synchronous Operation Truth Table

(T_{N+1} is the state of the flip-flop after arrival of the Clock Pulse (C_P), not shown.)

S_D	C_D	Q	$\overline{Q}$
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	1	1

Asynchronous Operation Truth Table

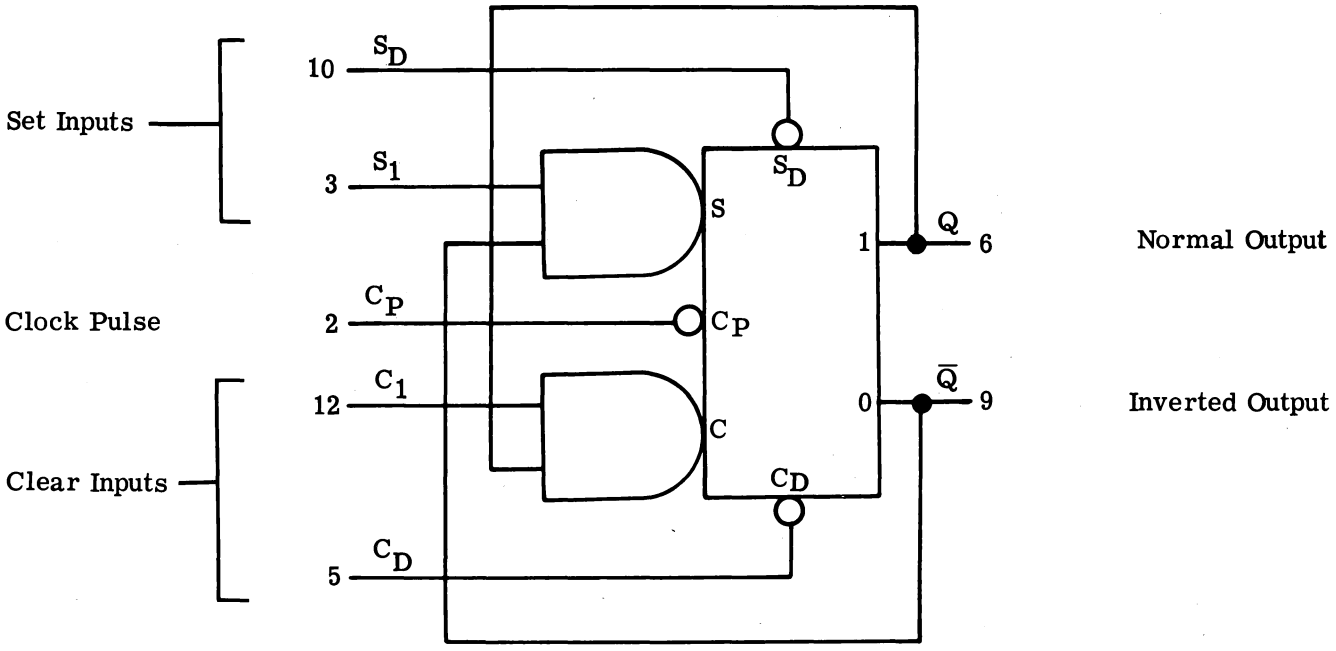
(The asychronous inputs, Direct Set (S_D) and Direct Clear (C_D), override the synchronous inputs, Set 1 and Set 2 (S_1 and S_2) and Clear 1 and Clear 2 (C_1 and C_2); they are independent of all other inputs.)



Clock Pulse Waveform

Legend:
- 1 = High State (More Positive)
- 0 = Low State (More Negative)
- X = State of Input Does Not Affect Output
- NC = No Change in State When Clock Pulse Arrives
- U = Indeterminate State (1 or 0)

Figure 19 - Clocked Flip-Flop — Synchronous and Asynchronous Operation



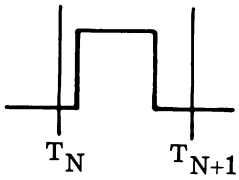
Clocked Flip-Flop Connected for J-K Operation
(Q Connected to C_2, $\overline{Q}$ Connected to S_2)

T_N		T_{N+1}
S_1	C_1	Q
0	0	Q_N
1	0	1
0	1	0
1	1	$\overline{Q}_N$

J-K Operation Truth Table

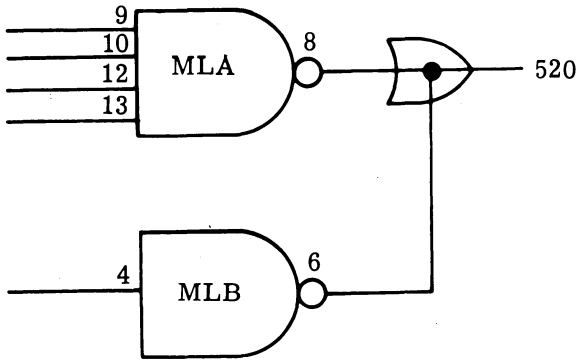
(T_{N+1} is the state of the flip-flop after arrival of the Clock Pulse (C_P), not shown.)

Legend:
1 = High State (More Positive)
0 = Low State (More Negative)
Q_N = State of Q at Time N (No Change in State)
$\overline{Q}_N$ = Inverse of State of Q at Time N (Change in State)



Clock Pulse Waveform

Figure 20 - Clocked Flip-Flop — J-K Operation



Wired OR Gate (At Interconnection of MLA and MLB)

INPUT		OUTPUT
8	6	520
1	1	1
0	1	0
1	0	0
0	0	0

Legend: 1 = High State (More Positive)
0 = Low State (More Negative)

(Output is high when all inputs are high and low when any or all inputs are low, the same as for an integrated circuit AND gate. When +6 v and 0 v are applied to the same wire, the 0 v always overrides the +6 v.)

Figure 21 - Wired OR Gate — Logic Symbol and Truth Table

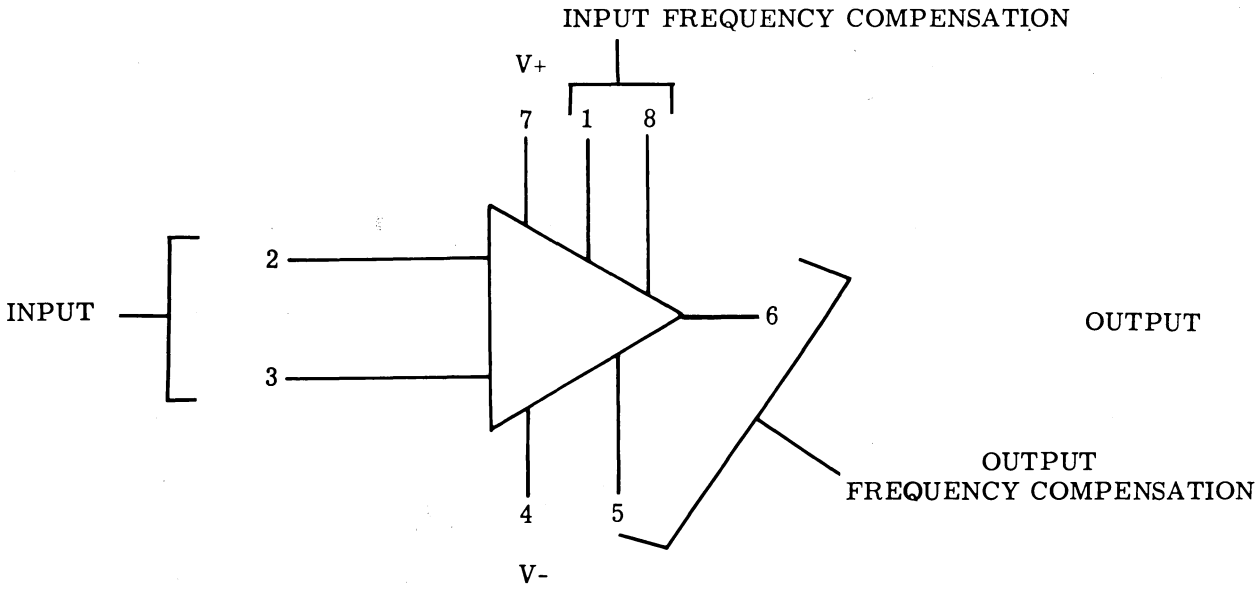
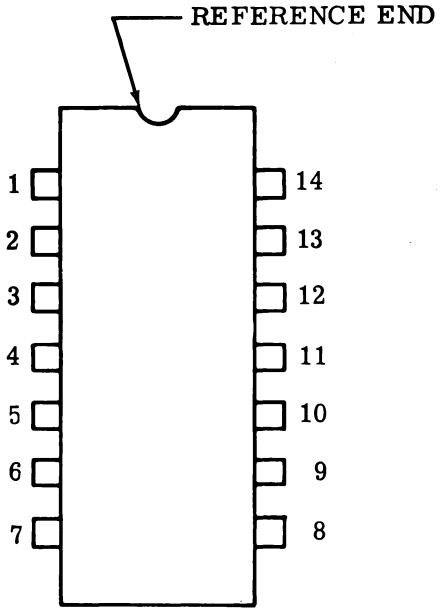
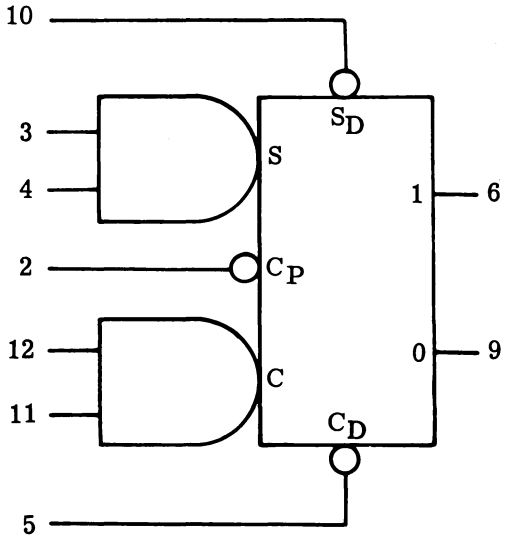


Figure 22 - Operational Amplifier (Op Amp)

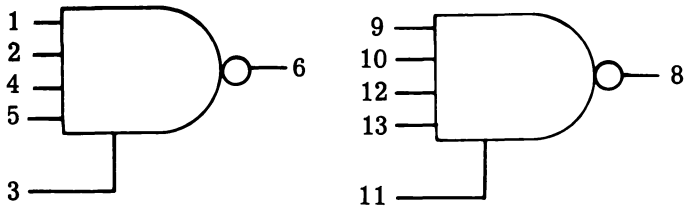


Dual-in-Line Integrated Circuit Package
(Top View)

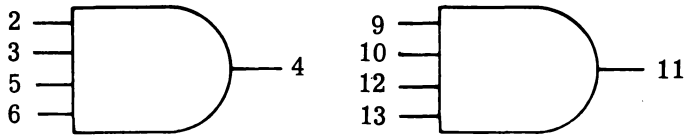


ML845 - Clocked Flip-Flop

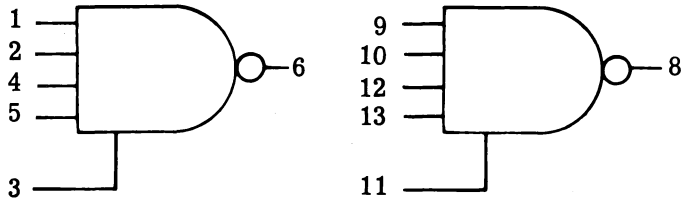
Note: Numbers refer to terminals on package. Ground is applied to pin 7, +6 v to pin 14.



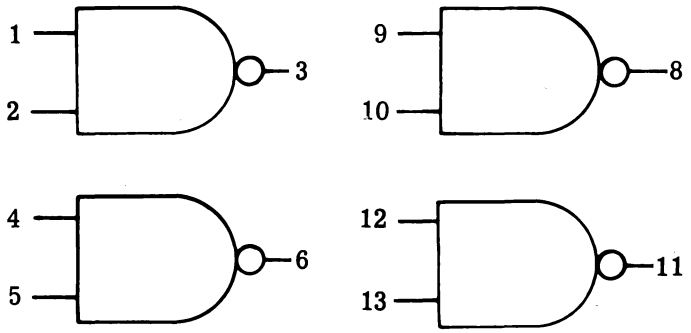
ML830 - Dual 4-Input NAND Gates (Extendable)



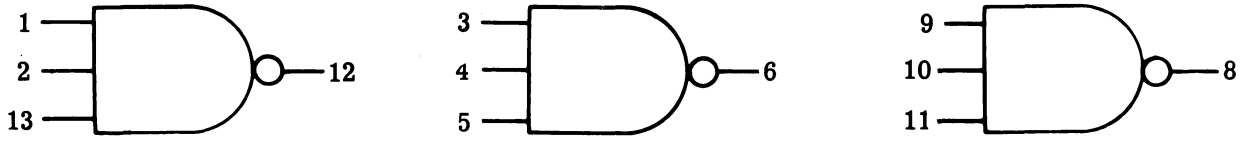
ML833 - Dual 4-Input Extenders



ML844 - Dual 4-Input Power NAND Gates
(Extendable)

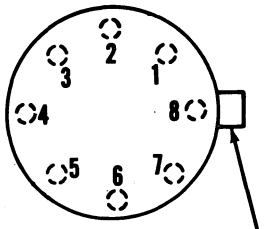


ML846 - Quad 2-Input NAND Gates



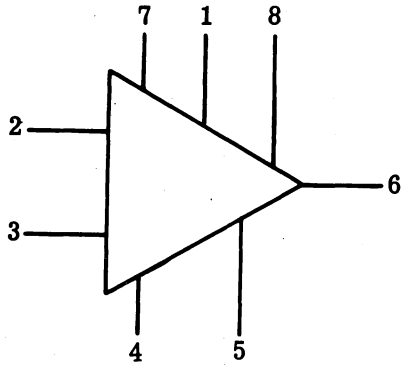
ML862 - Triple 3-Input NAND Gates

Figure 23 - Package and Configurations for Digital Integrated Circuits



(Top View)

TO-Type Integrated Circuit Package



Note: Numbers refer to terminals on package.

Figure 24 - Package and Configuration for Operational Amplifier