35A LINE CONTROLLER FOR

8A1 DATA SELECTIVE CALLING SYSTEM

GENERAL DESCRIPTION AND PRINCIPLES OF OPERATION

CONTENTS PAGE

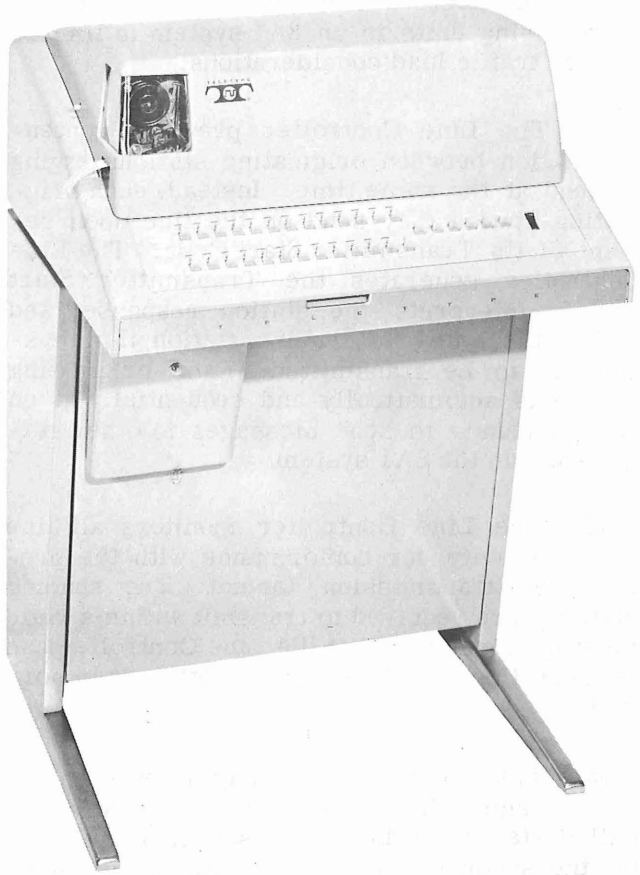


Figure 1 - 35A Line Controller

Prepared for American Telephone and Telegraph Company by Teletype Corporation

1. GENERAL

1.01 This section provides the operating features, physical description, and circuit description of the 35A Line Controller (Figure 1). The Line Controller is the controlling element in an 8A1 (Half-Duplex) Data Selective Calling System. Data is exchanged at 100 words per minute using ASCII (American National Standard Code for Information Interchange). This section is being reissued to change the designation 35A-1 Line Controller to 35A Line Controller, include the latest addendum, and incorporate all engineering changes. Marginal arrows are used to indicate these changes except where 35A-1 Line Controller has been changed to 35A Line Controller.

1.02 The Line Controller is capable of polling up to a maximum of 25 originating stations. The originating or polled station is then permitted to transmit messages from either a keyboard or a tape reader. The Line Controller does not place a restriction on the number of Receive-Only (RO) Sets; the number of receiving units in an 8A1 system is limited only by traffic load considerations.

1.03 The Line Controller prevents contention between originating stations trying to send at the same time. Instead, each originating station may send on the line upon receipt of its Transmitter Start Code. The Line Controller generates the Transmitter Start Codes, interprets the station response, and yields the line to a sending station if a message is to be transmitted. Each originating station is automatically and sequentially given an opportunity to send messages to other stations within the 8A1 system.

1.04 The Line Controller monitors all line activity for conformance with the prearranged transmission format. The sending stations are required to transmit within a rigid message format so that the Line Controller can recover the line if activity is other than normal.

1.05 The Line Controller may intercept messages which can not be received at the called station. (The called station is selected by the sending station.) An intercepted message is punched in tape by the Line Controller; however, tape reading and transmission facilities must be made available to retransmit the message on the signal line.

2. DESCRIPTION

2.01 The following paragraphs include the operating features of the 35A-1 Line Controller in the 8A1 (Half Duplex) Data Selective Calling System. Subsequent paragraphs will describe the circuitry of the various components.

OPERATING FEATURES

A. Basic Function

2.02 The basic function of the Line Controller is to prevent contention between stations operating on a private line. Each originating station is polled in sequential order using Transmitter Start Codes. The Line Controller has facilities for polling a maximum of 25 originating stations. If traffic is to be sent, the polled station will select one or more receiving units within the system, by transmission of Call Directing Codes. Each called station must answer with a response if the station can receive traffic. Otherwise, the Line Controller will generate a response and intercept the message (if possible), returning the signal line to the polled station for continued message transmission.

2.03 The Line Controller does not have facilities for sending messages on the line. It is assumed that an originating station of the ASR (Automatic Send-Receive) type will be associated with the Line Controller to provide transmission facilities for intercepted tapes. Relaying facilities between systems are not provided in the Line Controller.

B. Control Codes and Responses

2.04 The control codes are used to facilitate the polling and selective calling processes in an 8A1 Data Selective Calling System. The Line Controller generates a separate, two-character Transmitter Start Code (TSC) for each transmitting device in the system. The TSC's are generated in a programmed order; heavy traffic stations may be programmed to respond more than once per polling cycle. Each polled station may, upon receipt of its TSC, transmit a message to one or more stations in the system.

2.05 The polled station selects receiving units in the system, one at a time, by means of Call Directing Codes (CDC's). Each CDC must be acknowledged before the next one

can be sent. If a called station does not respond to its CDC, the Line Controller will respond and capture the subsequent message text in the intercept.

2.06 After all CDC's have been transmitted, a Start-of-Text (STX) code, message text, and an End-of-Transmission (EOT) code are sent. The Line Controller will poll the next station in the system upon receipt of the EOT code. If traffic is not available at a polled station, the polled station will automatically respond with a \ ACK sequence indicating no traffic, and the Line Controller will continue the polling cycle.

2.07 Transmitter Start Code (TSC): The TSC is a two-character sequence consisting of the DC_0 character and a variable (alpha-block graphic) character. Six of the eight bits of the variable character are programmed in the TSC program board. The sixth and seventh bits are prewired (6 space, 7 mark) so that only alpha-block characters (32 possibilities, only a maximum of 25 required) can be used. The eighth bit of the code is used for even parity and must be programmed marking if the total number of marks in bits 1 through 5 is odd.

2.08 Call Directing Code (CDC): A CDC is transmitted by the polled station to select a called station. The CDC consists of two graphic characters. A graphic is defined as a character with either the sixth or seventh bit marking, but not both. There are 32^2 or 1024 combinations possible. If message transmission from the polled station is automatic, ie, originated from a tape reader, the CDC sequence must consist of two graphic characters followed by a DELETE and an idle line. The Line Controller will detect the two graphic characters and check to make certain that the DELETE and idle line follow in that order. If the Line Controller detects a deviation from this order, it will generate the BREAK (BK)-pause-EOT sequence. This will stop the tape reader by disconnecting the polled station and will reset the Line Controller. A different format is allowable for keyboard entry.

2.09 Response to a CDC: A traffic response from the polled station will consist of transmission of a tape leader followed by a CDC. The Line Controller will store the CDC and check for format deviations. If the called station fails to respond within the permissible idle line period, the Line Controller will respond. With regard to a group CDC, the Line Controller will generate an answer-back response only when the station which was selected to respond to the group CDC, fails to do so. A response from the Line Controller for an unanswered CDC will normally consist of an * ACK. The * on the page copy at the polled station indicates that the called station did not answer and that the CDC and text will be intercepted. When the Line Controller responds with a # ACK, the sequence indicates that the called station did not respond, and the Line Controller is unable to intercept the message. (ACK is a nonprint function character.) Under these circumstances, the operator at the polled station must prepare and resend a new tape addressed to the unanswered CDC('s).

2.10 No-Traffic Response: A no-traffic response from a polled station consists of the transmission of a \ ACK in its initial response to a TSC. The initial response is defined as the first "busy line-idle line" sequence following a TSC.

2.11 Maintenance Alarm Response: A maintenance response from a polled station consists of the transmission of a BELL BELL sequence in its initial response to a TSC.

2.12 Keyboard Operation Response: A Start of Message (SOM SOM) character response from a polled station in its initial response to a TSC, will cause the Line Controller to switch to the keyboard mode of operation. In this mode the timing circuits in the Line Controller are modified to allow a greater idle line interval between characters.

2.13 Start-of-Text (STX): Upon completion of the address portion of the message, consisting of at least one CDC, the polled station must use the STX DELETE code sequence to indicate the beginning of message text.

2.14 End-of-Transmission (EOT): Upon completion of message text, the polled station must use the EOT DELETE code sequence. The Line Controller also uses an EOT to reset the logic of the polled and called station in case of a system error.

2.15 Line Break: The line break signal is used to stop a transmitter or to make certain that it is stopped. The BK-pause-EOT sequence consists of 300 ms of open line (space), 200 ms of idle line (mark), and an EOT, and is used to return control of the system to the Line Controller.

2.16 Tape Leader: A tape leader is interpreted by the Line Controller as the continuous transmission of DELETE characters during the initial response of a polled station to its TSC. An interruption in the transmission by a character other than DELETE, will end the tape leader.

2.17 Inhibit Codes: The Line Controller will accept a control code group or a NULL character to modify its timing pattern of message control. Any character in a group having bit 4 marking and bits 5, 6, and 7 spacing or a NULL character will effect this change.

2.18 The first characters are in a group known as Form Effectors. They include horizontal and vertical tabulation, form feed, etc. The Line Controller will accept these characters, to change its timing pattern, only during the text of a message. The timing change in the Line Controller allows the transmitter to stop while these functions occur. Each of the characters must be followed by a DELETE character. As soon as the station transmitter restarts after the function is performed, the Line Controller's timing pattern will return to its original form.

2.19 The NULL character is intended for use by high-to-low converters. The Line Controller will accept this character from a station any time during its transmission. It must, therefore, be generated under controlled conditions. Its affect upon the timing pattern of the Line Controller is the same as that of a Form Effector.

C. Polling

2.20 Upon receipt of a no-traffic response, a maintenance alarm response, or an EOT, the Line Controller will generate a TSC. The generation of a BK-pause-EOT sequence by the Line Controller, caused by an error in the system or in a transmitting tape, will automatically lead to the generation of the next TSC.

2.21 When a TSC is generated by the Line Controller, the polled station may respond with a \ ACK (no traffic), BELL BELL (maintenance), SOM SOM (keyboard transmission), or DELETE's (tape leader of a message). If a polled station responds with \ ACK or BELL BELL, the Line Controller will generate the next TSC. In the case of BELL BELL (maintenance), the MTC ALARM lamp on the Line Controller will flash green, and the buzzer will be energized.

2.22 If the polled station does not respond to its TSC within 1.0 second, the Line Controller will generate a BK-pause-EOT sequence, leading to the next TSC. A no-response will cause the lamp in the associated skip station key, to flash green, and the buzzer will be energized. The buzzer, accompanying a no-response or MTC ALARM, can be suppressed by operating the alarm cutoff (ACO) key.

Poll Rest Free Condition

2.23 If the Line Controller has completed the polling of all stations in the polling cycle (25 maximum), and none of these stations had transmitted a message, the Line Controller will enter a poll rest free condition. In this condition polling will stop, but the Line Controller will continue to monitor the signal line. During poll rest free, a spacing line signal longer than one-half of a bit length will cause the Line Controller to generate a BK-pause-EOT sequence, thus restarting the polling cycle. A station wishing to send a message during the poll rest free condition, can start the polling cycle by generating any character after the line has been idle for one minute (8 seconds - optional). The polling cycle may also be started locally by operating either the START or BREAK key on the Line Controller. After the Line Controller has been in the poll rest free condition for approximately eight minutes, it will automatically generate a BK-pause-EOT sequence to start the polling cycle. This operation maintains a constant monitor of line conditions even in periods of little or no traffic.

Poll Rest Locked Condition

2.24 When the STOP key is operated, the Line Controller will enter the poll rest locked condition at the time it would normally generate the next TSC. In this condition normal polling will stop and may not be restarted by the signal line as in the poll rest free condition. In the poll rest locked condition (STOP key operated) the polling cycle may be stepped manually by use of the BREAK and STOP keys.

(a) If the Line Controller is in a polling cycle as the STOP key is operated, the stations remaining in that polling cycle may be polled manually by repeated operation of the START key.

(b) If the Line Controller is at the end of a polling cycle when the STOP key is operated, the BREAK key must be operated once before the Line Controller will enter a subsequent polling cycle. Then the stations in that polling cycle may be polled manually by repeated operation of the START key.

D. Monitoring

2.25 Since either tape reader or keyboard transmission is permitted in an 8A1 Data Selective Calling System, the Line Controller must monitor two modes of system operation. When keyboard entry occurs, both automatic and manual modes will apply during the complete transmission. The initial response of a polled station will be automatic as the SOM SOM is transmitted. The SOM will signify a change in the timing pattern for a subsequent keyboard (manual) transmission. However, all answer-back responses to manual transmission of CDC's will be monitored as in the automatic mode. The subsequent keyboard transmissions from the polled station will be monitored in the manual mode. If the complete message is transmitted from a tape reader, the Line Controller will monitor in the automatic mode.

Automatic Transmission

2.26 Automatic transmission originates from the station controller or from tape. In these transmissions one character appears on the signal line every 100 ms. The receiving selector in the Line Controller will detect an idle signal line if a start signal does not occur within 10 ms after the end of the stop bits of an 11 unit character. For a transmission to be automatic, the Line Controller should not detect an idle line of more than 1.0 second between characters. If the Line Controller does detect an idle line in excess of 1.0 second between characters, the transmission pattern will not conform with the format, and the Line Controller will take action to disconnect the polled station.

2.27 Transmission Time Limits: The Line Controller will limit the length of transmissions to one second during the address portion of a message and while polling. The exception to this is a tape leader. If one of these transmissions should exceed one second, the Line Controller will generate a BK-pause-EOT sequence and continue polling.

2.28 Idle Line Time Limits: The Line Controller will, with the exception of poll rest and following the transmission of a Form Effector or a NULL, limit the length of an idle line to 1.0 second. If the line is idle for more than 1.0 second as defined above, the Line Controller will take some form of action. This action depends upon the system condition at that time and consists of either the generation of a BK-pause-EOT sequence or an * ACK.

2.29 Tape Leader Limits: The tape leader as defined in 2.16 is not limited to one second, but to 30 seconds. At 100 words per minute, this is 300 characters. As soon as the Line Controller receives a character other than DELETE, the one second transmission limit is applied.

2.30 Format Checking: The Line Controller requires that the CDC sequence consists of two graphic characters, a DELETE character and an idle line. If the third character transmitted were other than a DELETE, it might combine with the second graphic to form a false CDC, resulting in a system failure. The idle line is required to permit a station controller to start transmitting immediately upon receipt of its CDC; a station controller does not wait for an idle line. If the transmitter at the polled station did not stop immediately, a system failure would result. If the Line Controller detects a deviation from the CDC sequence, it will generate a BK-pause-EOT sequence and poll the next station. The Line Controller also inhibits the improper use of a STX. If at least one CDC has not been transmitted before a STX, the Line Controller will generate a BK-pause-EOT sequence and poll the next station.

2.31 Text Monitoring: During the text of a message, the Line Controller will limit the number of continuous identical characters. If the number of identical characters exceeds a set limit, the Line Controller will assume that the tape being transmitted is jammed or torn. It will then generate a BK-pause-EOT sequence. The number of characters so limited is normally set at 30, but may be adjusted up to 120.

2.32 Special Timing Limits: Transmission of a NULL or a Form Effector will change the idle line timing limits of 2.28. Following the transmission of a NULL character during any portion of the message, the Line Controller will allow the line to be idle

for 3 seconds before generating a BK-pause-EOT sequence. If the line does not go idle following the transmission of the NULL, the Line Controller will revert to the regular idle line time interval.

2.33 Since the use of a NULL character is not limited by the Line Controller, it must be generated under controlled conditions to avoid the possibility of generating a BK-pause-EOT sequence or the loss of a CDC.

2.34 The use of Form Effector codes to extend the idle time limit is confined to the text of the message (between a STX and an EOT). Transmission of these characters is usually followed by a DELETE character, which the Line Controller will allow. If the transmitter does not stop following the DELETE character or a character other than DELETE is transmitted before the signal line goes idle, the Line Controller will revert to the regular idle line timing interval.

2.35 The Line Controller may be programmed to allow certain stations in the polling sequence to transmit more than one message. A station so programmed, upon completion of its first message, will be immediately repolled. If another message is available, it may then be transmitted. This repolling will continue until the station responds with a no traffic response or has transmitted six messages. Polling will then continue on to the next station in sequence.

Keyboard Transmission

2.36 Since manual operation of a keyboard into the system is erratic and does not follow the standard pattern of tape transmission, the Line Controller cannot exercise the same degree of control as it does during automatic transmission. Many of the features of automatic transmission are suppressed. Upon receiving its TSC, a polled station wishing to operate in the keyboard mode will automatically generate an SOM SOM. Receipt of an SOM in the initial response to a TSC will switch the Line Controller into the keyboard operating mode.

2.37 Idle Line Time Limits: In the keyboard mode of operation, the polled station is allowed 30 seconds between the transmission of characters. If this time limit is exceeded, the Line Controller will generate a BK-pause-EOT sequence. Idle line time limits for transmission from the called station remain at 1.0 second. This may be done since these responses are automatically generated.

2.38 Transmission Time Limits: No transmission time limits are placed upon the polled station in the keyboard mode of operation. The length of the responses from the called stations are limited to one second.

2.39 CDC's and Format Checking: Since the called station starts its response to a CDC upon receipt of the second graphic in the two-graphic sequence, the keyboard operator cannot reliably insert the DELETE character used in automatic transmission. For this reason, the DELETE character is not used and the format checking of Paragraph 2.30 is not performed. The DELETE character does appear in the intercept tape, however. This allows a keyboard message which has been intercepted to be transmitted back into the system with the proper format.

E. Message Intercept

2.40 The Line Controller will temporarily store the two graphic characters of a CDC. If the called station does not respond, the Line Controller will generate an * ACK. It will then transmit the two graphics in storage plus an inserted DELETE character to the intercept typing reperforator. If the called station responds, the CDC in storage is dropped, as no intercepting action takes place and the CDC is not needed.

2.41 If the Line Controller has intercepted a CDC, it will also intercept the associated text. The resulting message can be reentered into the system from an associated ASR at a later time. The Line Controller will automatically feed out a trailer of DELETE characters at the end of the intercept tape, upon completion of the message. If a line break is generated either by the Line Controller or receiving station during an intercept, the tape will also feed out.

Intercept Nonoperative

2.42 If the intercept reperforator loses power, is electrically disconnected in any way, or has a power failure in its SMD (selector magnet driver), the Line Controller will generate a BK-pause-EOT sequence, if it is committed to intercepting a message. Its response to future unanswered CDC's will be # ACK rather than * ACK.

2.43 If a low paper condition occurs or the INTERCEPT DISABLE switch (located on the electrical service assembly) is operated, the Line Controller will be conditioned to generate the # ACK following the next TSC. If either of these conditions occur during a message intercept, it will have no affect upon the transmitting station. When the intercept is disabled, the INCPT OFF lamp on the Line Controller will be illuminated, and the buzzer will be energized.

COMPONENTS

2.44 The major components of the 35A Line Controller are shown in Figure 2. The intercept reperforator, electrical service assembly, and multiple wire distributor are mounted on the base pan of the cabinet. The dc power supply is suspended from a set of rails attached to the bottom of the upper compartment base. The control module is attached to the front panel of the pedestal.

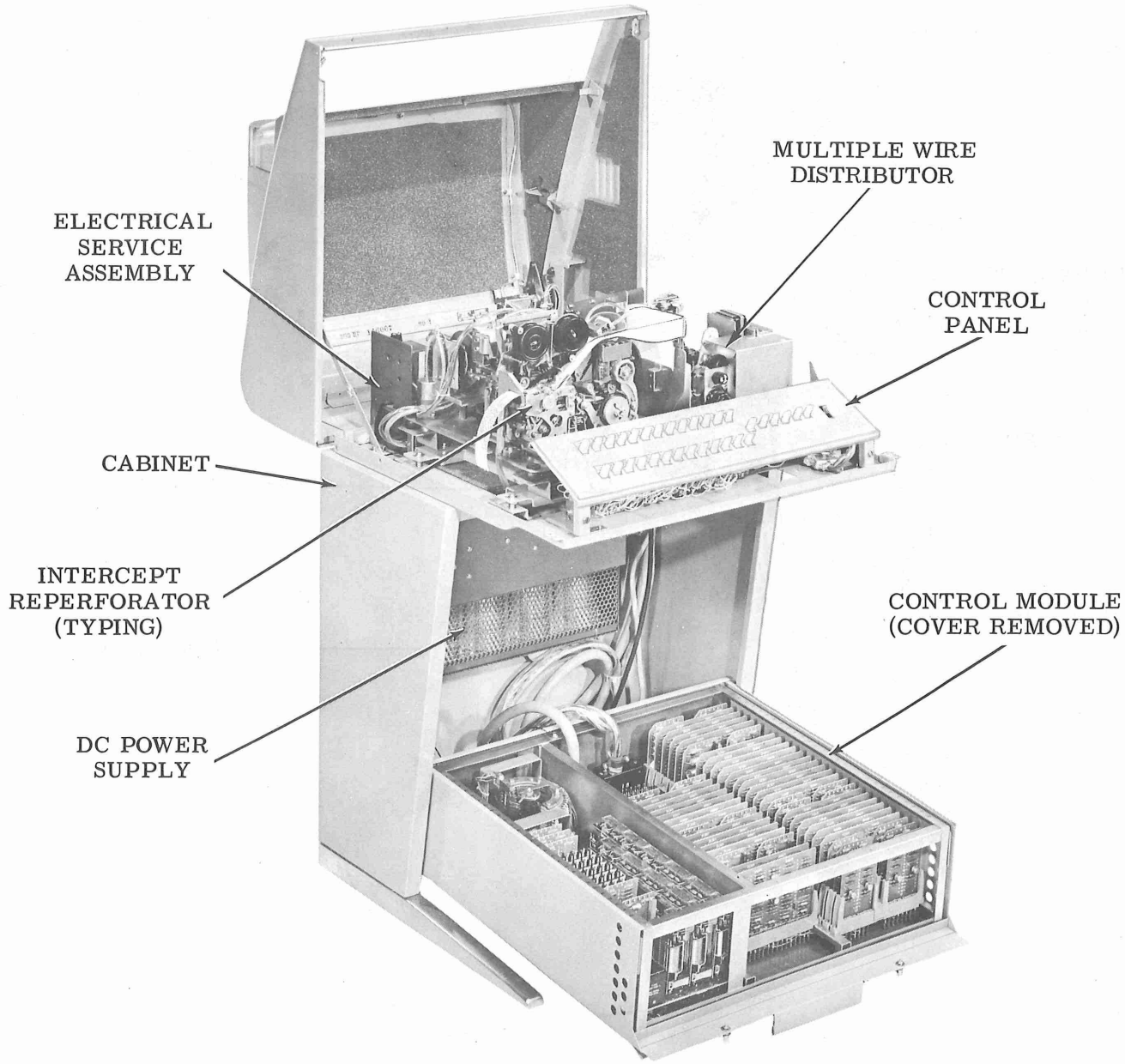


Figure 2 - Major Components of 35A Line Controller

A. CABINET

2.45 The cabinet (Figure 3) provides the mounting facilities and enclosure for the mechanical and electrical components which comprise the set. The cabinet consists of an upper cover, lower cover, pedestal, and feet. The chad box is mounted on the front panel of the pedestal. A copy light is located within the upper cover to provide illumination for the intercept typing reperforator tape.

2.46 The upper cover is opened by depressing the two release buttons (one on each side) and raising the upper cover. The upper cover release buttons, when depressed, disengage the associated upper cover latches. The upper cover may be raised and latched in the partially opened position or be raised to the fully opened position. The lower cover is opened by releasing the lower cover latch securing the front right corner to the compartment base; the upper cover must be partially

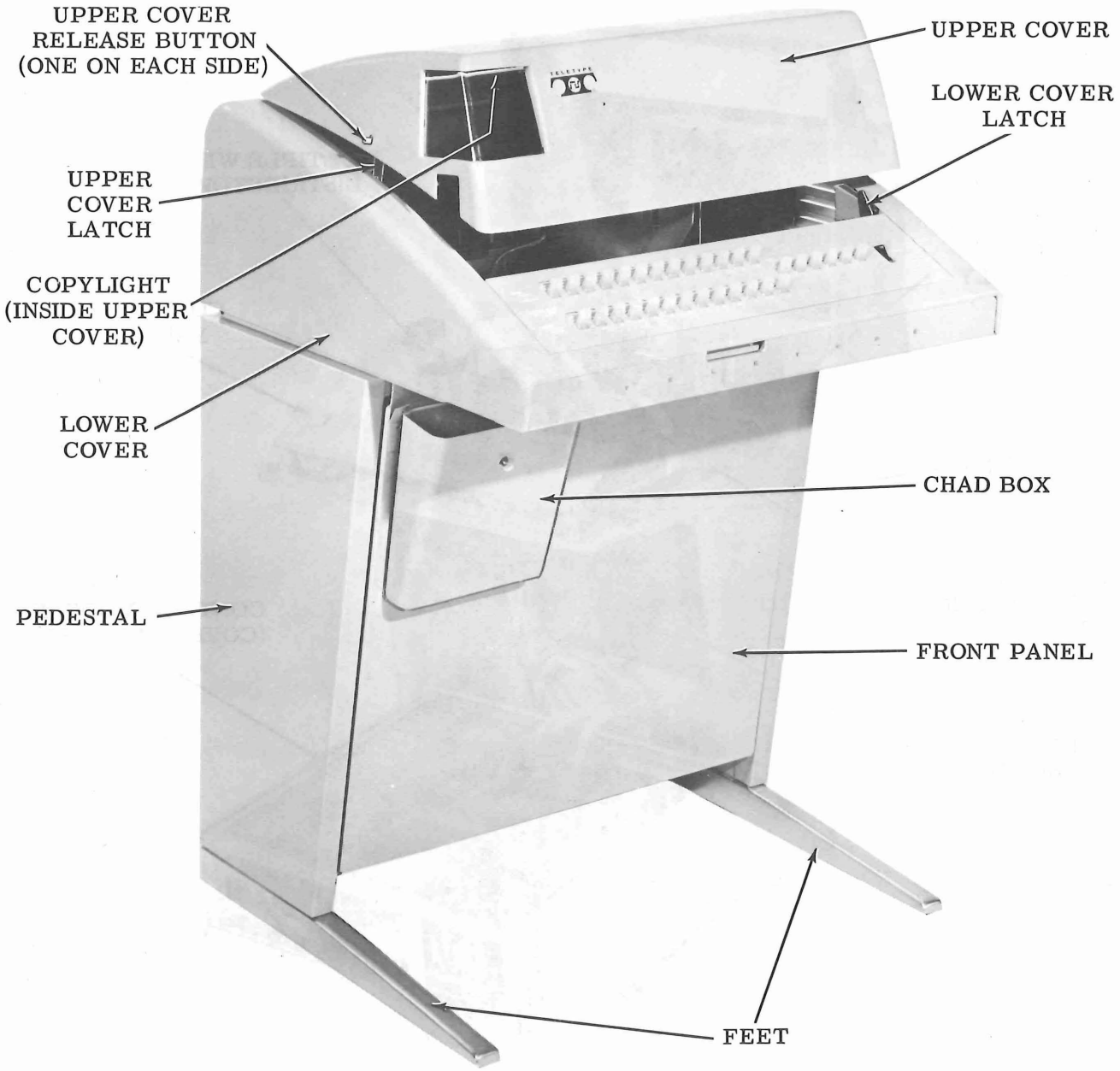


Figure 3 - Line Controller Cabinet (Upper Cover Latched Opened)

opened in order to gain access to the lower cover latch.

2.47 A set of rails is provided under the upper compartment base for suspending the power supply module. An enclosure is attached to the front panel of the pedestal to contain the control module. The panel, supported on a pair of pivots near the bottom of the pedestal, is fastened to the upper part of the pedestal with two panel lock pins.

B. Local Controls and Indicators

2.48 The control keys (Figure 4) are located on the front panel of the Line Controller. These are three-position keys but are operated in only two of the three positions. The key position toward the rear of the cabinet (away from the operator) has no electrical or mechanical function. An indicator lamp is enclosed within each key except the START and RESET keys. The lamps for the most part are not directly controlled by the keys but rather indicate a function associated with the key. In the normal (center) position, the key will be green when illuminated. In the operated (toward the operator or front) position, the key will be illuminated amber.

2.49 Skip Station Keys (Locking): The skip station keys are numbered 1 through 25; each key corresponds to one station in the polling sequence. The proper name of each station may be placed in the appropriate tag holder for ease of identification. In the normal position, the skip station key will be illuminated with a steady green light if the associated station is being polled or is transmitting a message. If a station does not respond to its TSC, the associated skip station key will be illuminated with a flashing green light. If a station in the polling sequence is to be skipped, the associated skip station key is operated; it will then be illuminated with a steady amber light.

2.50 STOP Key (Locking): In the normal position, the STOP key will be illuminated with a steady green light when the Line Controller has entered the poll rest free condition (2.23). In this condition the Line Controller has automatically stopped polling. If the STOP key is operated, the Line Controller will enter the poll rest locked condition (2.24), and the STOP key is illuminated with a steady amber light. In this condition, polling is restricted to manual operation.

2.51 ALARM CUT OFF Key (Locking): When an alarm condition occurs, such as no-response, maintenance, or intercept disabled, a buzzer will sound. Operation of the ALARM CUT OFF key will silence the buzzer and cause the key to be illuminated with a steady amber light.

2.52 RESET Key (Nonlocking): There is no internal lamp associated with this key. Operation of this key will reset all no-response or maintenance alarms.

2.53 BREAK Key (Nonlocking): This key will be illuminated with a steady green light when the signal line is open. Operation of the key will cause the generation of a BK-pause-EOT sequence. If the key is held operated,

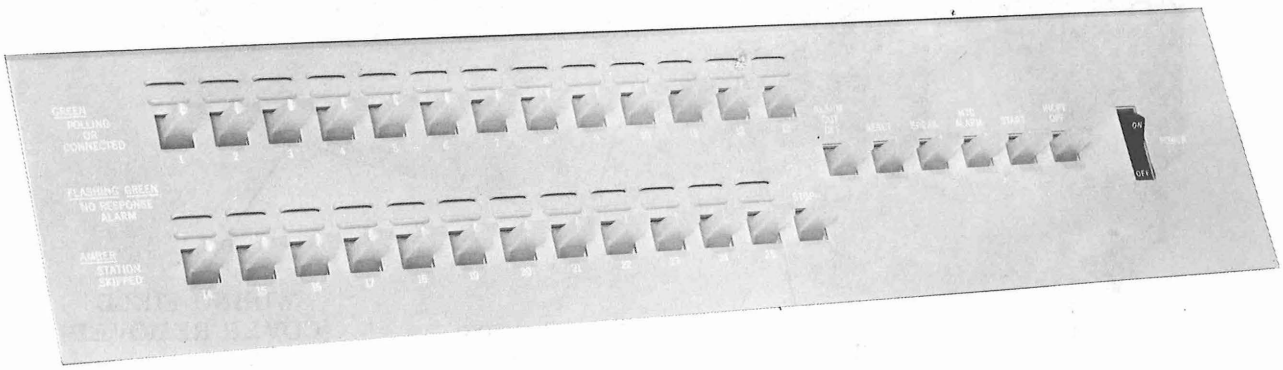


Figure 4 - Control Panel

the Line Controller will continue to generate this sequence.

2.54 MTC (Maintenance) ALARM Key (Nonlocking): If a polled station responds to a TSC with the maintenance code sequence, BELL BELL, the MTC ALARM key will be illuminated with a flashing green light. Operation of this key will reset a maintenance alarm only.

2.55 START Key (Nonlocking): This key has no lamp. Operation of this key will only be valid during either a poll rest free or poll rest locked condition. If operated during the poll rest free condition, the Line Controller will start the polling cycle. If operated during the poll rest locked condition (STOP key operated), the Line Controller will poll the next station only.

2.56 INCPT (Intercept) OFF: This key is used as an indicator lamp only. If the Line Controller cannot intercept a message for reasons described in 2.42 and 2.43, this key will be illuminated with a steady green light. This light indicates that the Line Controller requires some form of servicing.

C. Electrical Assemblies

2.57 The major electrical assemblies include the electrical service assembly, dc power supply, and control module.

Electrical Service Assembly

2.58 The electrical service assembly (Figure 5) accepts the external signal line and 117 volt ac power inputs, and provides mounting facilities for auxiliary components required to interconnect the major components of the Line Controller. The wiring field serves as a major distribution center for the internal power, signal, and control circuits. The Line Controller fuse and the dc power circuit fuses are located in the fuse field. In addition, the assembly contains the selector magnet driver for the typing reperforator, the intercept disable switch, the alarm buzzer, and the fail alarm relays.

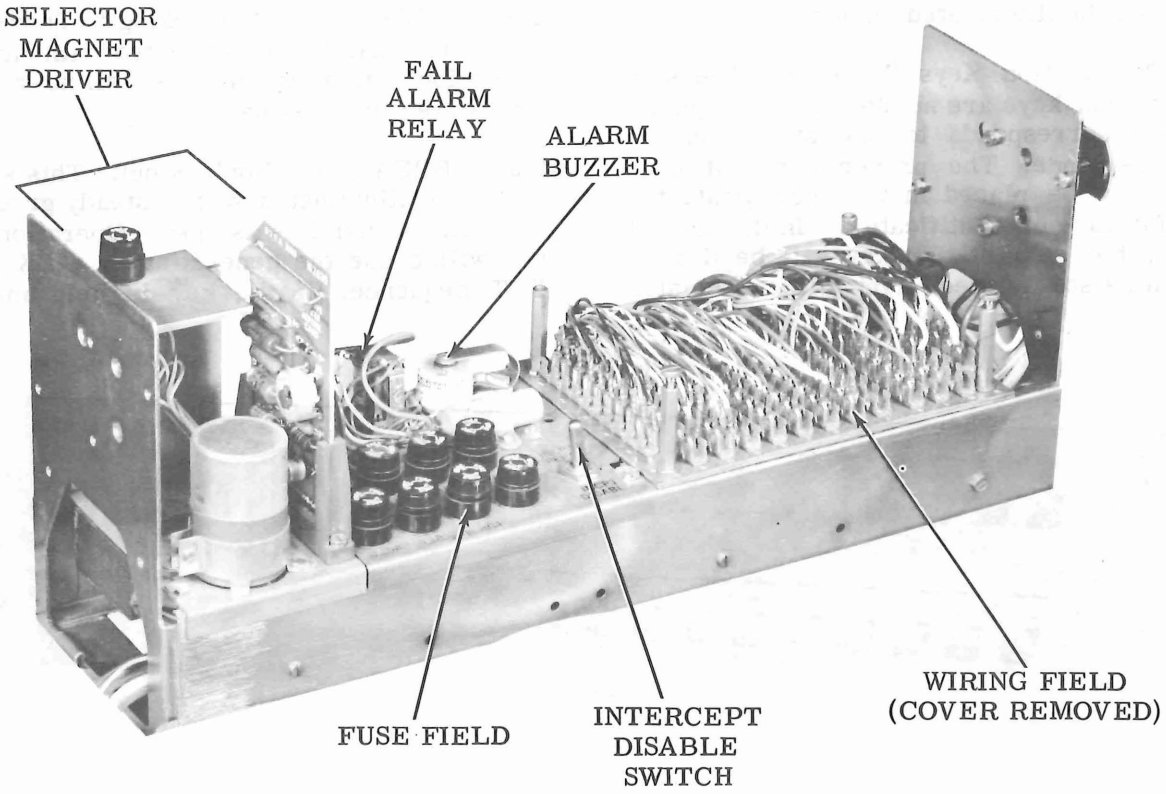


Figure 5 - Electrical Service Assembly

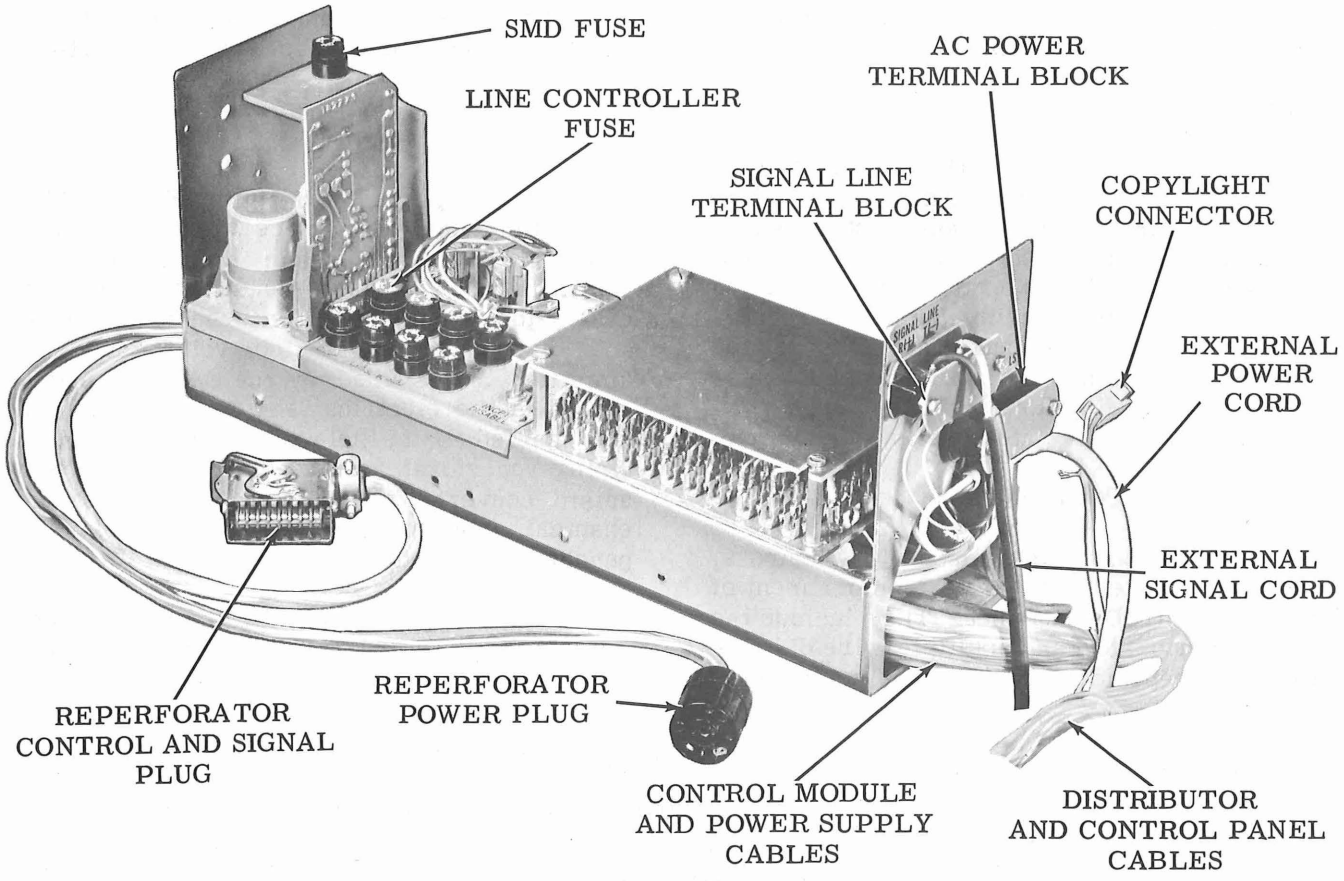
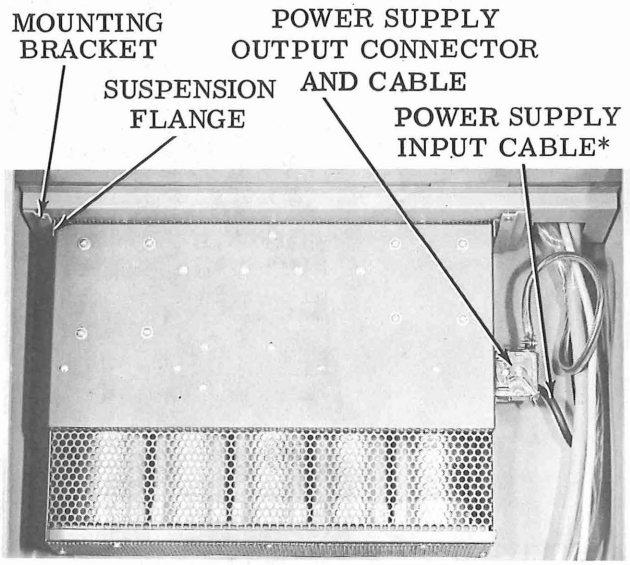


Figure 6 - Cables, Connectors, and Terminal Blocks of Electrical Service Assembly

2.59 The various cables and connectors for the control panel, power supply, control module, distributor, and reperforator are shown in Figure 6. The external power and signal line cords are brought into the Line Controller cabinet through an opening in the bottom of the pedestal. The cords are attached to the ac power and signal line terminal blocks. All cables originating from the electrical service assembly are terminated with connector plugs. The cables have adequate length to extend from the service assembly to their respective major component.

Dc Power Supply

2.60 The dc power supply (Figure 7) is suspended from a set of rails (mounting brackets) on the under side of the upper compartment base. It receives 117 volts ac from the electrical service assembly by way of the power supply input cable. The dc voltages are routed back to the electrical service assembly via the power supply output cable. The dc



*INPUT CONNECTOR (TWIST TYPE) BEHIND OUTPUT CONNECTOR

Figure 7 - Dc Power Supply

voltage circuits are then properly fused in the electrical service assembly.

Control Module

2.61 The control module (Figure 8) contains the receiving relay, logic relays, polled station no-response relays, polling step switch, TSC program board, and printed circuit cards. The receiving relay operates in conjunction with the signal line activity and is the receiving link of the Line Controller. The printed circuit cards contain the solid state logic elements such as flip-flops, NAND gates, NOR gates, Exclusive OR gates, relay drivers, etc.

D. Mechanical Components

2.62 The mechanical components (Figure 9) are located in the upper compartment of the Line Controller cabinet. They include the typing reperforator and multiple wire distributor. The reperforator, tape supply container, and distributor are mounted on the cradle. The cradle is secured to the upper compartment base.

Typing Reperforator

2.63 The typing reperforator (Figure 10) is the receiving device which produces a tape copy of each message intercepted by the Line Controller. When the intercept is to operate, the input signals are received, stored, and distributed by the control module, are amplified and shaped by the selector magnet driver in the electrical service assembly, and are applied to the selector mechanism of the typing reperforator unit. The selector mechanism converts the electrical signals to mechanical motions for producing a combined punched and typed message tape.

2.64 The typing reperforator unit, motor unit, and intermediate drive assembly are mounted on the reperforator base. The

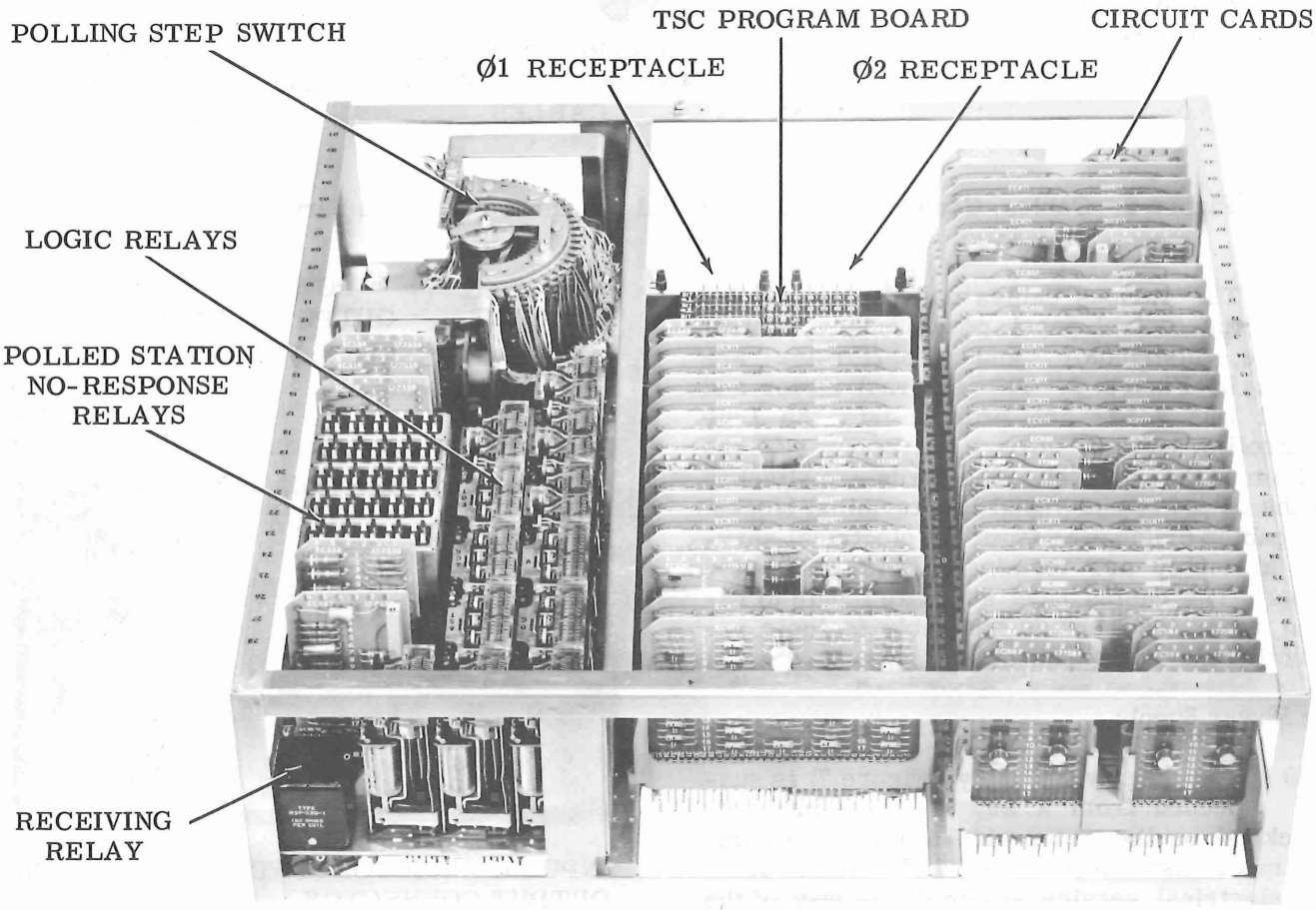


Figure 8 - Control Module

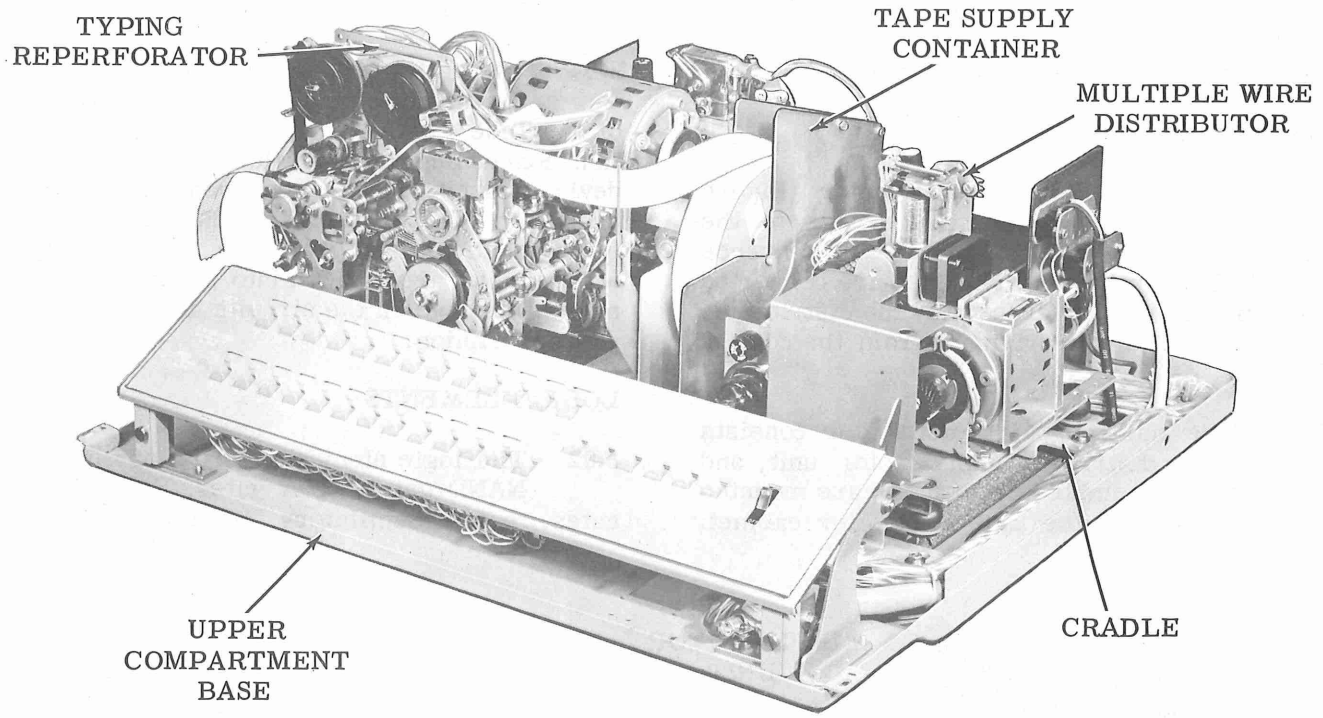


Figure 9 - Mechanical Components

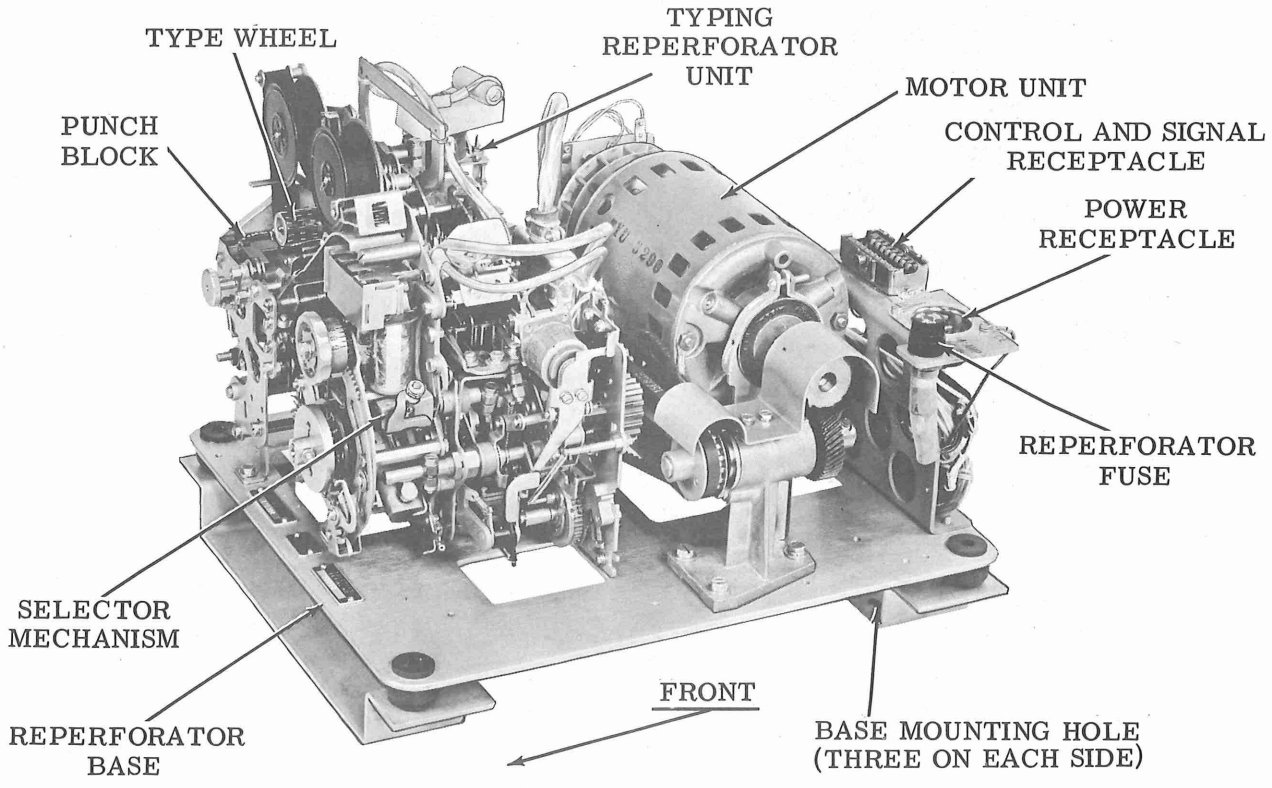


Figure 10 - Typing Reperforator Components

base is mounted to the cradle of the Line Controller cabinet with mounting screws which pass through the base mounting holes.

Multiple Wire Distributor

2.65 The multiple wire distributor (Figure 11) is the transmitting device of the Line Controller. The BK-pause-EOT sequence and all Transmitter Start Codes are converted from parallel to serial form by the distributor. The parallel inputs originate from the control module.

2.66 The multiple wire distributor consists of a distributor unit, motor unit, and base. The assembled components are mounted to the cradle of the Line Controller cabinet.

3. PRINCIPLES OF OPERATION

3.01 The following discussion is limited to the circuits and electrical components of the Line Controller. For detailed information concerning the operation of the mechanical devices, such as the typing reperforator (tape punch) and the distributor, refer to the appropriate sectionalized literature. The principles of operation are divided into (1), the logic elements which form the circuits and (2), the circuit description.

LOGIC ELEMENTS

3.02 The logic elements consist of flip-flops, NAND gates, NOR gates, Exclusive OR gates, gated oscillators, bit oscillators and

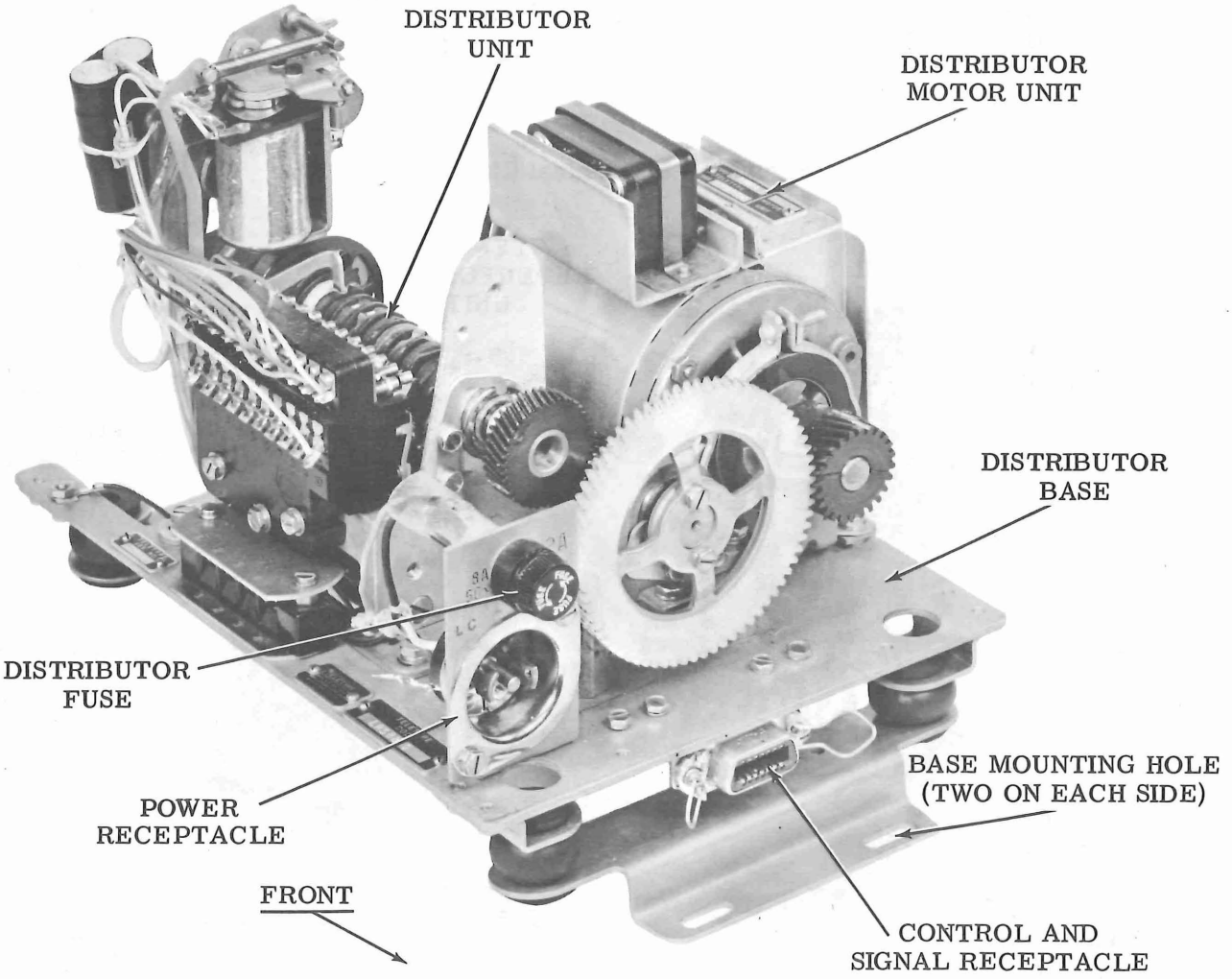


Figure 11 - Multiple Wire Distributor Components (Gear Guard Removed)

control, and relay drivers. The selector magnet driver is also covered. A Card Printed Schematic (CPS) for each logic element and the selector magnet driver, is located in the appropriate section. The logic elements whose operational characteristics are evident (such as relays, voltage dividers, etc) have been omitted from the following text.

A. Flip-Flop Elements

3.03 The flip-flop element is composed of capacitors, diodes, resistors, and transistors; the electrical components are mounted on a printed circuit card. Each flip-flop circuit card contains as many as three flip-flop elements and is located in the control module of the Line Controller.

Note: For additional information concerning the components and circuit cards of a flip-flop element, refer to CPS-1 of 7150WD in Section 581-121-400.

3.04 The flip-flop element is used as a memory device in the logic circuits. When combined with control gates and pulse generators (oscillators), groups of flip-flop elements are used to form a distributor, shift registers, and counters. Individual flip-flop elements are used to detect control codes and system conditions.

3.05 The flip-flop element may be described as a single throw, double output switch whose operated position (or state) is dependent upon the input characteristics. The two outputs are called Normal (N) and Inverted (I). The two positions are called state 1 and state 0. When in state 1, the N and I outputs of the flip-flop are ground and -6 volts, respectively. When in state 0, the N and I outputs are just reversed, ie, -6 volts and ground, respectively. The N and I outputs for state 1 and state 0 are summarized in Table 1.

3.06 The switching characteristics of a flip-flop element are shown in Figure 12. For purposes of illustration, only a minimum number of input leads is shown to switch the flip-flop from state 1 to state 0 or from state 0 to state 1. When power is available, the flip-flop element will remain in its existing state (state 0 or state 1) until a pair of input conditions change that state. In order to change the state, the prime input must be positive (ground in this case) before the matching set input goes positive. The set input must be a voltage transition from -6 volts to ground in one microsecond or less. The inputs for going from state 0 to state 1 include the prime (P1) and the set (1); ground must exist on input P1 before and during the time that a -6 volt to ground transition is received on input 1. For going from state 1 to state 0, ground must exist on input P0 before and during the time that a -6 volt to ground transition is received on input 0. Any other order or type of input will not affect the state of the flip-flop.

TABLE 1 - STATES OF FLIP-FLOP

STATE	OUTPUT	
	LEAD	VOLTAGE
1	N	grd
	I	-6 v
0	N	-6 v
	I	grd

3.07 When self-priming is used, the number of independent inputs required to change the state of a flip-flop element, is reduced. A prime input is connected directly to a flip-flop output. Single self-priming is shown in Figure 13; double self-priming is shown in Figure 14. When a positive transition occurs on the matching set input, the flip-flop element will go to that state if it is not already there. If a flip-flop is already in the primed state, a matching set input will have no affect. When self-priming is used, a P1 input is connected to the I output, and a P0 input is connected to the N output.

3.08 In actual use, a flip-flop element can have a maximum of eight inputs or four active matched pairs. Such an element is illustrated in Figure 15. Each matched pair consists of one prime and one set input. Two separate circuits, A and B, can be used to bias the flip-flop element into state 1 or state 0. For the Line Controller logic, the A circuits are generally used for a normal change of state, but if additional circuits are required, the B circuits may be used to change the state. The inputs to the flip-flop element are explained in Table 2.

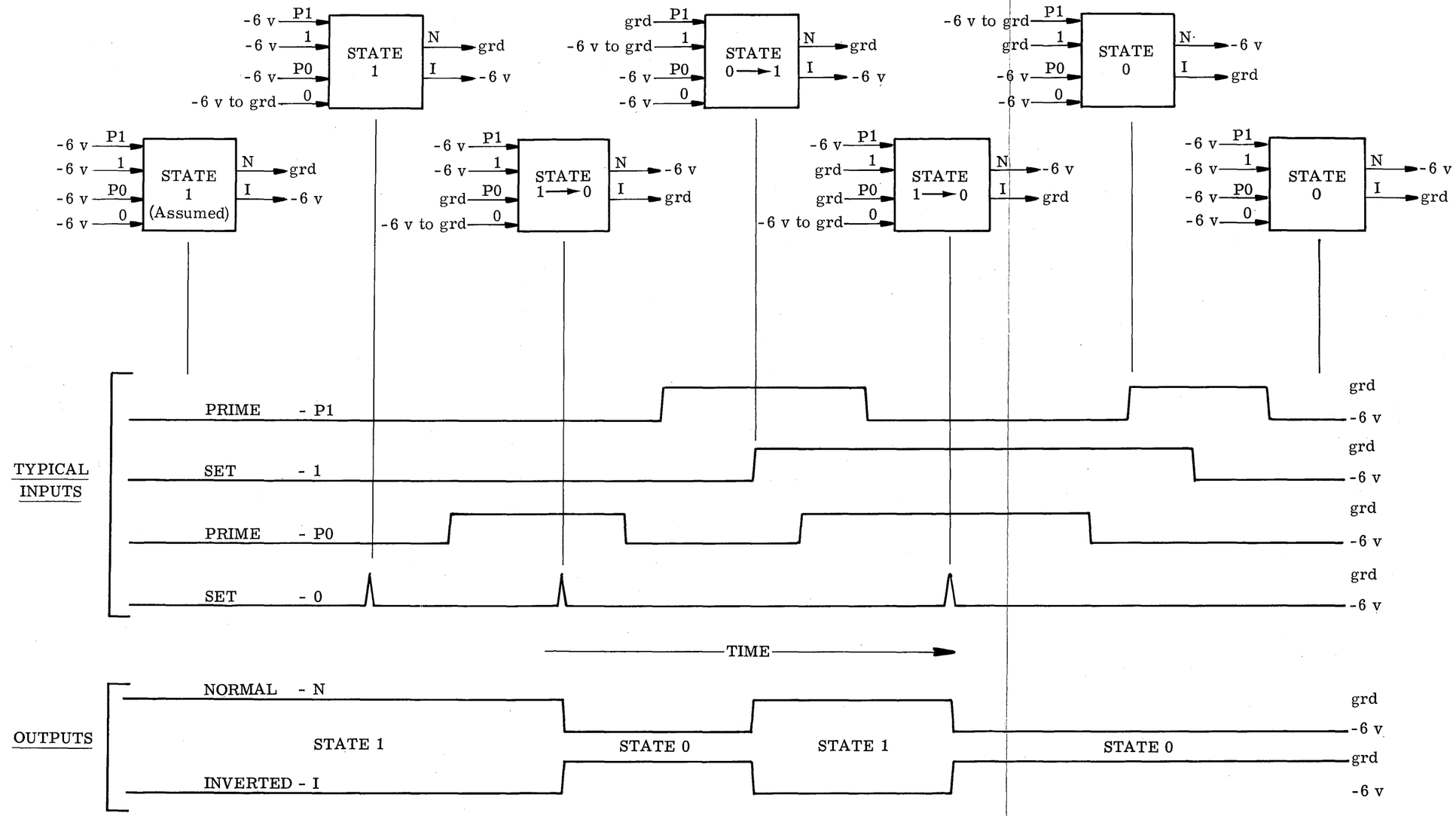


Figure 12 - Switching Characteristics of Flip-Flop Element

*Assume voltage level before change of state.

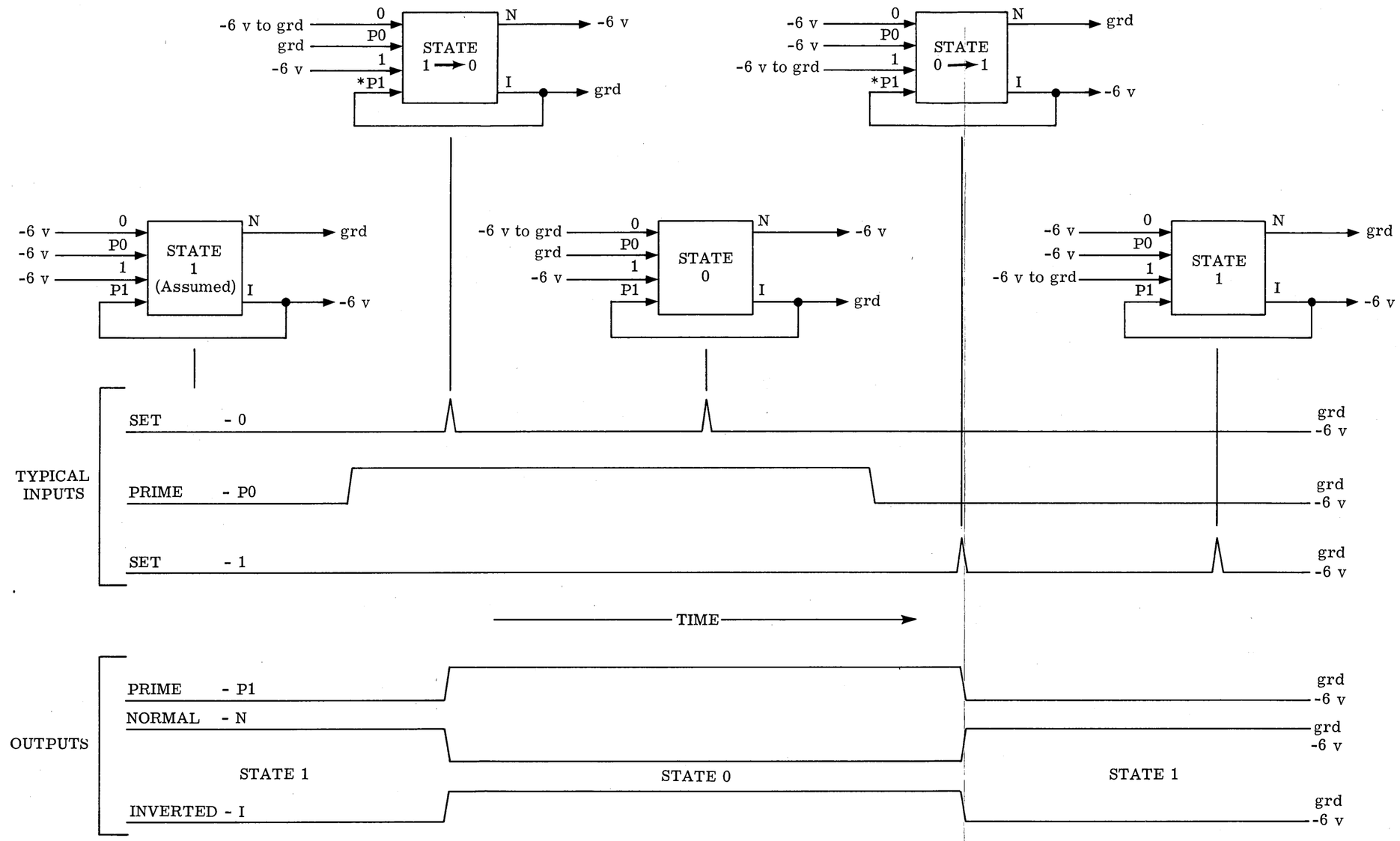


Figure 13 - Switching Characteristics of Flip-Flop Element with Single Self-Priming

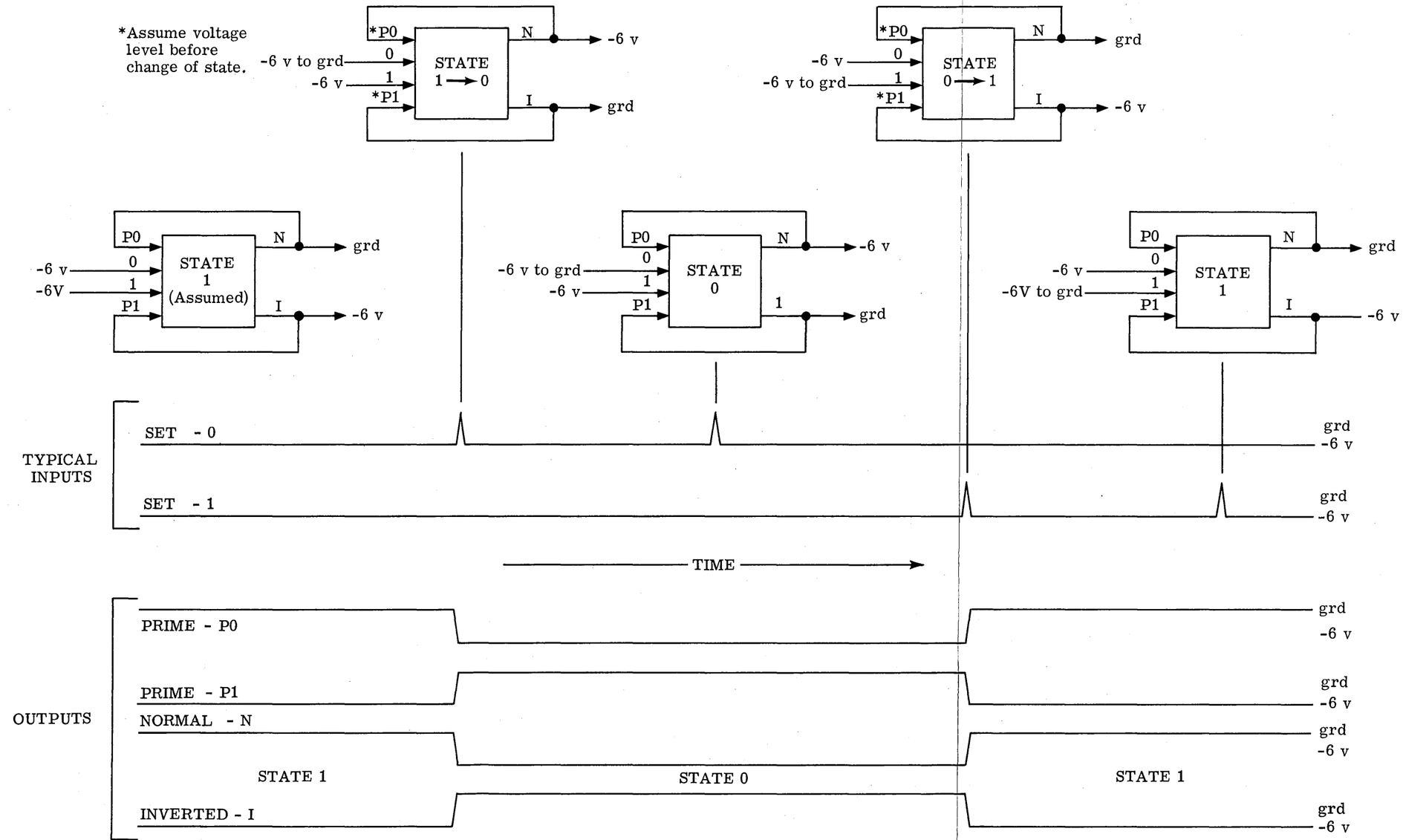
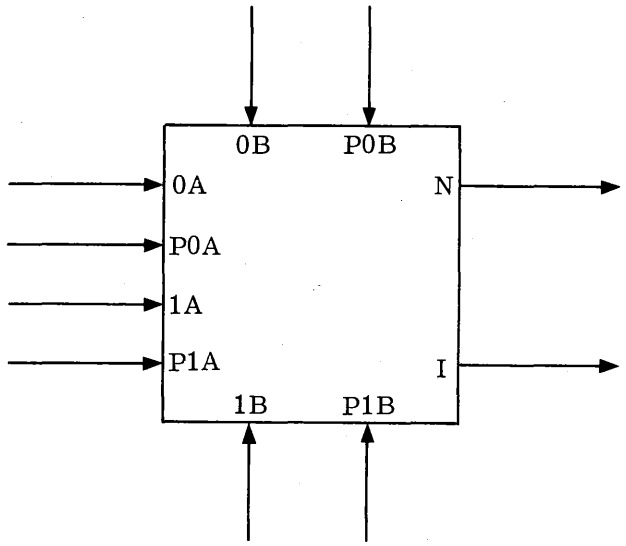


Figure 14 - Switching Characteristics of Flip-Flop Element with Double Self-Priming

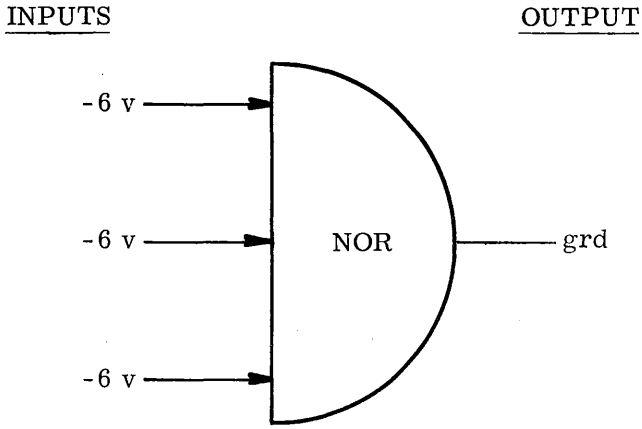
TABLE 2 - INPUTS TO FLIP-FLOP

GENERAL NAME	SYMBOL	DEFINITION		FOR STATE
Prime	P0A	(Prime) (state 0) (circuit A)	Matched Pair	0
Set	0A	(state 0) (circuit A)		
Prime	P0B	(Prime) (state 0) (circuit B)	Matched Pair	0
Set	0B	(state 0) (circuit B)		
Prime	P1A	(Prime) (state 1) (circuit A)	Matched Pair	1
Set	1A	(state 1) (circuit A)		
Prime	P1B	(Prime) (state 1) (circuit B)	Matched Pair	1
Set	1B	(state 1) (circuit B)		



NOTE: INPUTS AND OUTPUTS NEED NOT APPEAR IN ORDER SHOWN. UNUSED INPUTS AND OUTPUTS MAY BE OMITTED FROM THE SYMBOL.

Figure 15 - Flip-Flop Element



NOTE: A GRD APPLIED TO ONE OR MORE INPUTS WILL CAUSE THE OUTPUT TO BE -6V. INPUTS NOT CONNECTED DO NOT AFFECT THE CONDITION OF THIS GATE.

Figure 16 - NOR Gate Symbol and Operation

B. NOR Gates

3.09 The NOR gate (Figure 16) is used as a control gate for comparing two or three inputs from other control gates or logic elements. When only one input is employed, the NOR gate is used as a signal inverter. The voltage level of the inputs, as well as the output, is either ground or -6 volts. If all connected inputs are -6 volts, the output will be ground. If one or more of the connected inputs is ground, the output will be -6 volts. All inputs are shown on the functional schematics,

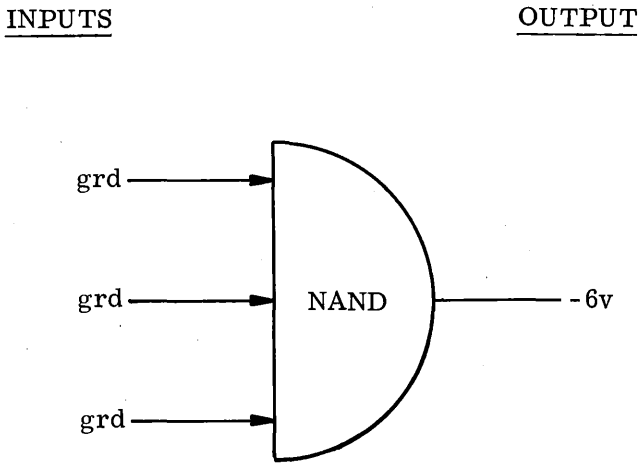
but those not connected will have no affect upon the logic performed.

Note: Refer to CPS-2 of 7150WD in Section 581-121-400 for detailed information on NOR gate components and circuits.

C. NAND Gates

3.10 The NAND gate (Figure 17) is also used as a control gate for comparing two or three inputs from other control gates or logic elements. When only one input is employed, the NAND gate is used as a signal inverter. The voltage level of the inputs, as well as the output, is either ground or -6 volts. If all connected inputs to the NAND gate are ground, the output is -6 volts. If one or more of the connected inputs is -6 volts, the output will be ground. All inputs are shown on the functional schematics, but those not connected will have no affect upon the logic performed.

Note: Refer to CPS-3 of 7150WD in Section 581-121-400 for detailed information on NAND gate components and circuits.



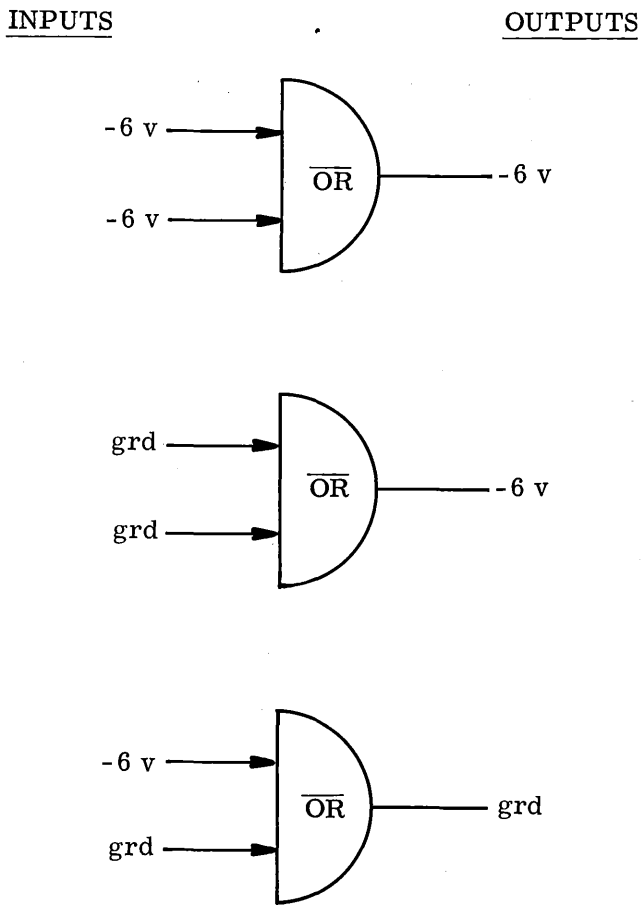
NOTE: A -6V APPLIED TO ONE OR MORE INPUTS WILL CAUSE THE OUTPUT TO BE GRD. INPUTS NOT CONNECTED DO NOT AFFECT THE CONDITION OF THIS GATE.

Figure 17 - NAND Gate Symbol and Operation

D. Exclusive OR Gates

3.11 The Exclusive OR gates are used to compare two circuits (usually the outputs of two flip-flops). If the inputs to an OR gate are both ground or both -6 volts, the gate output will be -6 volts. The output of this gate is designed to drive only a NOR gate. The outputs of many Exclusive OR gates may be accumulated through NOR gates. The Exclusive OR gate symbol is shown in Figure 18.

Note: Refer to CPS-4 of 7150WD in Section 581-121-400 for detailed information on Exclusive OR gate circuits.



NOTE: LIKE INPUTS PRODUCE A -6V OUTPUT. UNLIKE INPUTS PRODUCE A GRD OUTPUT.

Figure 18 - Exclusive OR Gate Symbol and Operation

E. Relay Drivers

3.12 The relay drivers are designed to operate a relay from a -48 volt power source and will conduct 250 ma. They are not designed to withstand the inductive spikes which are generated when the current flow through a relay coil is broken. Therefore, a diode arc suppressor or other isolating device is used to protect the driver. The relay drivers may also be used to provide a ground path for the indicator lamps. The lamps used in the Line Controller, draw 200 ma at -5.7 volts rms which is within the operating limits of the relay drivers.

3.13 The relay driver symbol is shown in Figure 19. When ground is applied to the input, the relay driver will conduct or provide ground to the associated circuit. When a -6 volt input is applied, the relay driver will not conduct.

Note: Refer to CPS-5 of 7150WD in Section 581-121-400 for detailed information of relay driver circuits. ←

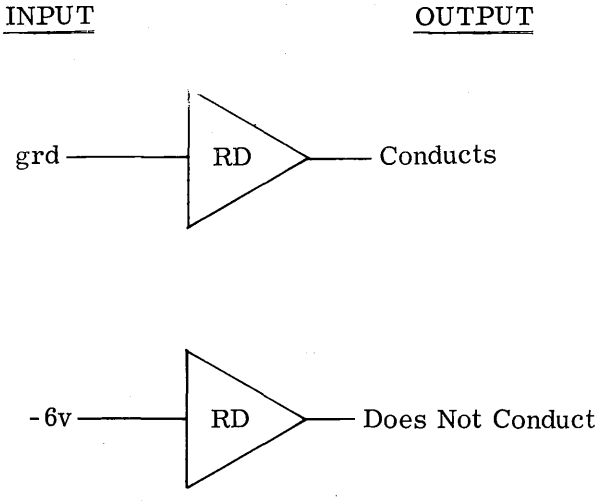
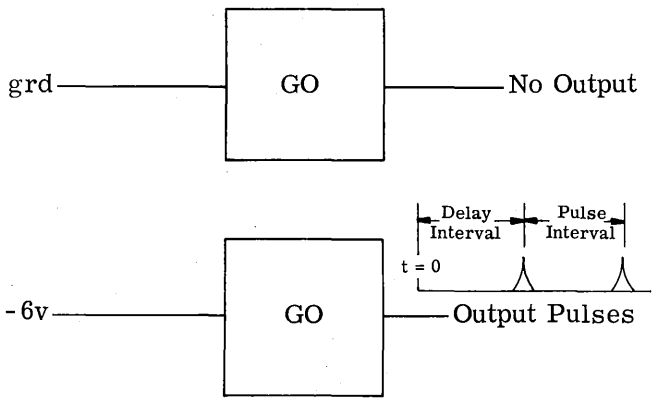


Figure 19 - Relay Driver Symbol and Operation

F. Gated Oscillators

3.14 The gated oscillator is used to obtain pulses at constant intervals after a delay interval which may be equal to, or greater than, the pulse interval (depending upon the characteristics of the particular gated oscillator circuit). A typical gated oscillator symbol showing input-output conditions is given in Figure 20.

Note: Refer to CPS-6 of 7150WD in Section 581-121-400 for detailed information on gated oscillator components and circuits. ←

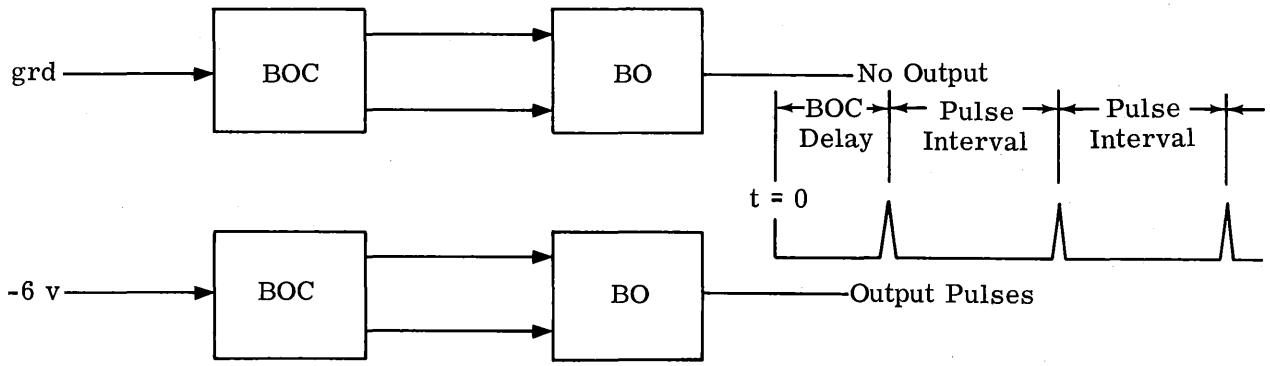


NOTE: TIME ZERO (T = 0) OCCURS WHEN THE INPUT BECOMES -6V. AN INPUT OF GRD WILL STOP AND RESET THE GATED OSCILLATOR.

Figure 20 - Gated Oscillator Symbol and Operation

G. Bit Oscillators and Control

3.15 The bit oscillator is used to generate accurately spaced output pulses. One bit oscillator (Figure 21) is used in conjunction with a bit oscillator control for the purpose of generating output pulses after a fixed time delay interval. A ground input will prevent the bit oscillator control from timing out and releasing the associated bit oscillator. A -6 volt input will permit the bit oscillator control to time out and, in turn, release the bit oscillator. When released, the bit oscillator will deliver the first pulse; subsequent pulses will follow at constant time intervals. In this case, the BOC is required to provide a deliberate delay.



NOTE: TIME ZERO (T = 0) OCCURS WHEN INPUT BECOMES -6V. AFTER BOC DELAY, BIT OSCILLATOR GENERATES ACCURATELY SPACED OUTPUT PULSES UNTIL INPUT TO BIT OSCILLATOR CONTROL BECOMES GRD. A GRD INPUT TO BIT OSCILLATOR CONTROL WILL STOP AND RESET BOTH BIT OSCILLATOR CONTROL AND BIT OSCILLATOR.

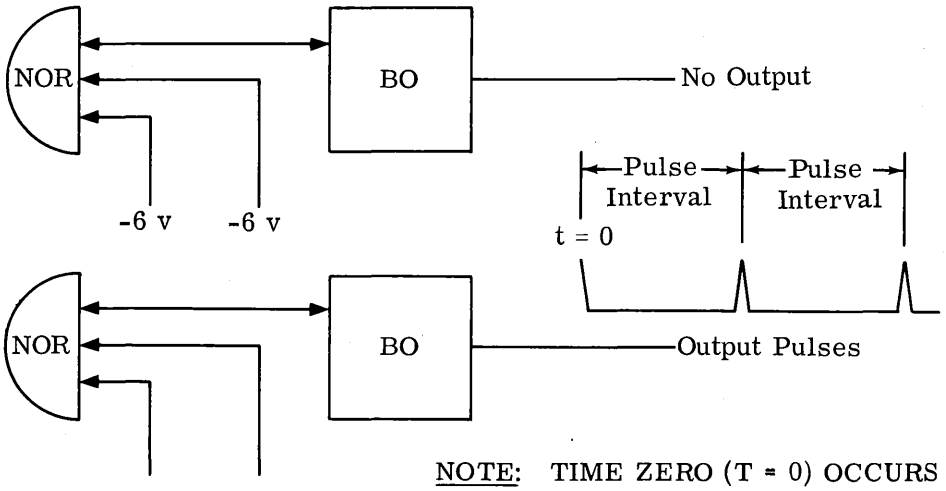
Figure 21 - Bit Oscillator and Bit Oscillator Control

3.16 Another bit oscillator (Figure 22) uses a NOR gate for control. When one or both inputs to the NOR gate becomes ground, the bit oscillator will deliver the first pulse; subsequent pulses will follow at constant time intervals. The bit oscillator will be stopped and reset when both inputs to the NOR gate become -6 volts.

Note: Refer to CPS-7 and CPS-8 in Section 581-121-400 for detailed information on the components and circuits of the bit oscillator control and bit oscillator.

H. Selector Magnet Driver

3.17 The selector magnet driver (SMD) for the typing reperforator, consists of a printed circuit card (refer to CPS-13 in Section 581-121-400) mounted on a frame (see equipment drawing 304200 in Section 581-121-400). The frame contains additional components, such as power transformer, a filter capacitor, a fuse, and a power transistor mounted on a heat sink. The SMD contains its own power supply to provide isolation from remote signal sources. The



OPERATE COMBINATION	grd	-6 v
	-6 v	grd
	grd	grd

NOTE: TIME ZERO (T = 0) OCCURS WHEN ONE OR BOTH INPUTS TO CONTROL GATE BECOME GRD. WHEN BOTH INPUTS TO CONTROL GATE BECOME -6V, BIT OSCILLATOR WILL STOP AND BE RESET.

Figure 22 - Bit Oscillator and Control Gate

power supply is made up of transformer T1, diodes CR1 and CR2, and filter capacitor C2. The output of this power supply varies widely from a spacing signal to a marking signal. The mean output is approximately -20 volts.

3.18 The SMD circuit is essentially an electronic switch. Line signals (current) are applied across CR5 and R3. Input bias current to control the switch point (at 10 ma) is supplied from a regulated voltage source through R1. The zener diode, CR6, is used to generate the stable reference voltage of -4.7 volts.

3.19 When the signal line is open (spacing), Q1 will be turned on by the regulated current flowing through R1 into its base. With Q1 conducting, Q2 will be off since the potential at the base of Q2 will be more positive than at the emitter. In this condition, only a small leakage current will flow through the selector magnets in the collector circuit of Q2.

3.20 As a space to mark transition begins, the negative bias current flowing to the base of Q1 is diverted into the signal line circuit. When signal line current approaches the total current supplied to the base of Q1, Q1 begins to turn off. Q2 will then begin to receive forward bias current from R8 and begin to turn on. The current supplied to the base of Q2 is amplified and a current which is a multiple of the base current appears in the emitter circuit. This increase in emitter current causes an increase in the negative potential, measured across R3. The increase at the emitter of Q1 will cause it to be further cut off. This feed-back process continues until the current in the selector magnet driver reaches a value which is determined by the voltage at the reference point. The voltage at the base and therefore the emitter of Q2 is clamped by CR4. This clamping action limits the amount of current flowing in the emitter and therefore the collector of Q2. The collector current of Q2 is limited to 0.500 of an ampere and may be adjusted to compensate for component variations by means of R4.

Note: The adjustment of R4 is a factory setting which is accurate to 2 per cent and is set for optimum performance of 0.500 ampere selector. It is unlikely that this adjustment will have to be changed during the life of the unit. However, should an adjustment be required, it should not be attempted without a current meter accurate to 1 per cent and the selector magnet driver in the marking condition for at least 10 minutes.

When the signal line current reaches 0.020 amperes, the voltage drop across CR5 and R3 will be approximately 0.60 volts. This voltage will bias Q1 off.

3.21 When the signal line current begins to fall as the signal line goes spacing, Q1 will begin to turn on, and the process described in 3.16 will occur in reverse until Q2 is turned off. The inductive arc generated by the selector magnets when the current is shut off, is suppressed by CR3, C1, and R9.

CIRCUIT DESCRIPTION

3.22 The logic, signal line, and power circuits of the Line Controller are classified and discussed with detailed reference to the functional schematics (FS's). Each paragraph heading designated with an upper case letter, eg, A., B., C., etc, includes the referenced functional schematic. The functional schematics; a block diagram showing the functional relationship of the functional schematics; an equipment drawing showing the physical location of the circuit cards, relays, step switch, and TSC program board; wave patterns and timing requirements; are located among the SD's in Section 581-121-400. ←

A. Receiving Selector (FS-1)

3.23 All signal line activity is monitored by the receiving selector. The marking and spacing conditions relevant to a busy, idle, or open signal line are detected by the receiving relay (RR) coil (FS-15). The associated RR contact (FS-1) duplicates the marking and spacing conditions in the receiving selector. The RR contact is normally open when the signal line is spacing. In the discussion to follow, the receiving selector is subdivided into the input signal logic, shift register, shift pulse generator, open line detector, character received, gated oscillator, and idle line detector.

Input Signal Logic

3.24 The input signal logic includes contact RR, voltage divider D4M, gate Z108C, and gate Z109A. The normally open RR contact

is operated between a -48 volt source and voltage divider D4M. A space or a mark on the signal line is reflected as a ground or a -5 volt output, respectively, from D4M.

3.25 The output from D4M provides an input to control gate Z110J of the gated oscillator and an input to an inverter and signal amplifier gate, Z108C. The output of Z108C provides inputs to R19-P1A of the shift register, CR-P0A of character received, and control gate Z109A; the output is ground for a mark and -6 volts for a space.

3.26 Gate Z109A supplies inputs to R19-P0A of the shift register, Z109B of the shift pulse generator, and OLD-P0A of the open line detector. Z109A provides a signal inversion under normal circumstances, ie, signal line busy. The Z109A output is -6 volts for a mark and ground for space. Input Z109A-18, originating from the open line detector, will blind the output of Z109A (always -6 volts) when an open line is detected. When this occurs, the signal line appears marking to the circuits depending upon the output of Z109A.

Shift Register

3.27 The shift register consists of flip-flop elements R10 through R19 and provides storage for ten of the eleven bits which comprise a character. The eleventh bit (second bit of the two bit stop pulse) does not enter the shift register. When a complete character is received, element R10 provides storage for the start (space) bit, elements R11 through R18 provide storage for code levels 1 through 8, respectively, and element R19 provides storage for the first bit (mark) of the two bit stop pulse.

3.28 Input signals are applied to the P0A and P1A inputs of R19 from the outputs of Z109A and Z108C, respectively. A ground is required to prime either input to R19. A space bit will appear on R19-P0A as ground, or a mark bit will appear on R19-P1A as ground. Since the same signal from Z108C is either applied directly to R19-P1A or inverted before being applied to R19-P0A, ground cannot appear on R19-P0A and R19-P1A simultaneously. With R19 primed, a shift pulse applied to the matching set inputs, R19-0A and R19-1A, will set R19 to state 0 for space or state 1 for mark.

Shift Pulse Generator

3.29 The shift pulse generator consists of control gate Z109B, bit oscillator control Z106, and bit oscillator Z206. Upon detection of a character on the line, the generator supplies the pulses to all 0A and 1A set inputs of the shift register. The shift pulse generator is started approximately 4.54 ms after the start bit of a new character appears on the line; it generates subsequent pulses in the approximate center of each bit on the signal line; and it is stopped when the start bit arrives in element R10.

3.30 The Z109B control gate provides the on or off control for the associated bit oscillator control and bit oscillator. The control gate compares the inputs from Z109A and R10-I which represent one input and one output of the shift register. Before a new character is detected by the input signal logic, flip-flop element R10 is always left in a state 1 (space) condition. The R10-I output is -6 volts. An idle line, open line, or stop pulse of a previous character maintains a -6 volt output from Z109A. Therefore, with both inputs to Z109B being -6 volts, the output of Z109B is ground, and the bit oscillator control is held in the off condition. When a new character is received, the space bit provides a ground input to Z109B-23. The output of Z109B becomes -6 volts, releasing the bit oscillator control, Z106.

3.31 The bit oscillator control, Z106, provides a timed delay before releasing the associated bit oscillator. When the input to the oscillator control is ground, the bit oscillator is prevented from oscillating. When the input becomes -6 volts, bit oscillator Z206 is released after 4.54 ms (center of the 9.09 ms start bit) to generate accurately timed pulses.

3.32 Bit oscillator Z206, when released, will generate pulses that are spaced at timed intervals of 9.09 ms. Since the bit oscillator control, Z106, had provided a delay of 4.54 ms, each pulse is generated in the center of each character bit on the signal line. After the first shift pulse, R10-I will supply ground to gate Z109B, thus holding the bit oscillator on, independent of line signals. Since all elements of the shift register are marking except R19, the space in R19 must be shifted down the entire register before R10 will again be state 1 and release the oscillator. This requires nine more shift pulses, the last of which occurs in

the center of the tenth bit (first bit of the stop pulse).

Operation of the Shift Register

3.33 When R19 is state 1, the N (Normal) and I (Inverted) outputs are ground and -6 volts, respectively. When R19 is state 0, N is -6 volts and I is ground. The N and I outputs of R19 are connected to R18-P1A and R18-P0A so that a shift pulse will transfer the state of R19 into R18. Examination of flip-flop elements R19 through R11, shows that the state of one element is shifted to the succeeding element when a shift pulse is applied. However, the last element, R10, is connected to R11 in such a way that a state 1 in R11 will be shifted into R10 as a state 0, or a state 0 in R11 will be shifted into R10 as a state 1. Normally, during an idle line or at the end of a character, all the elements of the register are in state 1.

3.34 The N and I outputs of flip-flop elements R11 through R18 provide inputs to other storage elements and decoding gates. The inverted outputs are also connected to the P1B inputs of each element. Elements in state 0, indicating a space bit, are restored to state 1 when a pulse is applied to the matching set inputs, 1B. The pulse occurs 13 ms after the CR flip-flop goes to state 0 and originates from the gated oscillator.

Open Line Detector

3.35 Element R10 can become state 1 only when the start bit (space) or an open line condition enters R10. Prior to the entry of a spacing bit, R10 is state 0 as adjacent marking conditions in R11 (state 1) are shifted into R10. (The R11-N output is connected to the R10-P0A input, and R11-I is connected to R10-P1A.) When R10 becomes state 1, an instantaneous comparison of register input R19-P0A and register output R10-N, is made by the Open Line Detector (OLD) flip-flop. The comparison, as follows, determines whether or not a state 1 entering R10 is a continuous extension of an open line:

(a) If the OLD-P0A input (same as R19-P0A) is ground (spacing bit) as the state of R10 changes from 0 to 1, a -6 volt to ground transition on R10-N (input to OLD-0A) will set flip-flop OLD to state 0, indicating an open line.

(b) If the OLD-P0A input is -6 volts (marking bit) as the state of R10 changes from 0 to 1, a -6 volt to ground transition on R10 will not affect flip-flop OLD.

3.36 The open line detector includes flip-flop OLD, control gate Z122B, relay driver Z127A, and the BREAK lamp. The OLD-N output provides inputs to gate Z108B of the gated oscillator, a control gate in another logic circuit, and gate Z122B. The OLD-I output is applied to input OLD-P1A, and to flip-flop elements in other logic circuits. When the signal line is busy or idle, flip-flop OLD is in state 1. When an open line is detected, flip-flop OLD enters state 0; the output of gate Z122B becomes ground, causing the following:

(a) Relay driver Z127A conducts, providing ground to illuminate the BREAK lamp.

(b) Control gate Z109A is blinded to prevent the shift register from responding to a false start bit. Z109A remains blinded until flip-flop OLD is restored to state 1.

3.37 A pulse applied to input OLD-1A while flip-flop OLD is state 0, will set OLD to state 1. OLD-P1A is ground when OLD is state 0. The pulse input on OLD-1A originates from gated oscillator Z101 in the gated oscillator circuit. When the signal line goes marking, the gated oscillator will start its timing cycle. At the end of 13 ms (signal line must be marking for at least 13 ms), the gated oscillator will deliver an output pulse. The pulse will set flip-flops OLD, ILD, and R19 through R11 to state 1. The OLD-N output extinguishes the BREAK lamp, removes the blind from control gate Z109A, and turns off the gated oscillator, Z101, through control gate Z108B.

Character Received

3.38 Since element R10 can become state 1 only when the start bit or an open line enters R10, an additional comparison of register input R19-P1A and register output R10-N, is made by the Character Received (CR) flip-flop element. This comparison, as follows, determines whether or not a state 1 entering R10 establishes a character:

(a) If the CR-P0A input (same as R19-P1A) is ground as the state of R10 changes from 0 to 1, a -6 volt to ground transition on R10-N (input to CR-0A) will set flip-flop

CR to state 0, indicating a character received and stored in the shift register.

(b) If the CR-P0A input is -6 volts as the state of R10 changes from 0 to 1, a -6 volt to ground transition on R10-N will not affect flip-flop CR.

CR-N is connected to the ILD-P1A input of the idle line detector and to gate Z110J of the gated oscillator. The CR-N and CR-I outputs also condition other decoding and storage elements for receipt of a character which might be in the shift register. CR-I provides the CR-P1A input to flip-flop CR.

3.39 When a character is received, CR becomes state 0 providing a -6 volt input to control gate Z110J. (The -6 volt input to ILD-P1A removes the prime from flip-flop ILD so that the first pulse from the gated oscillator will not change the state of ILD.) The -6 volt input to Z110J causes the gated oscillator to start its 13 ms timing cycle. When the gated oscillator delivers its first pulse (0.5 ms before the end of the 11th bit), the input on CR-1A will reset flip-flop CR to state 1. CR-P1A was primed from the CR-I output.

Gated Oscillator

3.40 The gated oscillator consists of control gates Z108B, Z108A, Z110J, and gated oscillator Z101. The output pulse from Z101 is distributed to the 1B set inputs of elements R11 through R19 of the shift register, OLD-1A input of the open line detector, ILD-1A input of the idle line detector, CR-1A input of the character received, and to the set inputs of other flip-flop elements. If allowed to time out by the control gates, the gated oscillator will deliver its first pulse after a 13 ms delay interval. If allowed to continue as in the case of an idle line, the gated oscillator will deliver a second pulse after a pulse interval of 10 ms. A continuous -6 volt input to Z101 is necessary to cause the gated oscillator to time out and deliver a pulse. A ground input during either the delay or pulse interval will stop and reset the gated oscillator.

3.41 NAND gate Z108A is the primary control gate whose three inputs must be ground in order to provide a -6 volt output and release the gated oscillator. The three inputs originate from R10-N, control gate Z108B, and control gate Z110J. During receipt of a character or an open line, R10-N is always -6 volts; only when a spacing bit arrives in R10 will R10-N become ground. Control gate Z108B is used to hold the gated oscillator during an idle line. The OLD-N input from the open line detector is to assure that the gated oscillator will continue to operate and set OLD to state 1 if an idle line and an open line are indicated simultaneously; this condition may occur when the unit power is first turned on. The ILD-N input assures that the gated oscillator will stop after generating a second pulse and setting ILD to state 1 (line idle). The other input to Z108B from Z125C, will cause the gated oscillator to start when the signal line is neither idle nor open; this input is associated with the start key. Control gate Z110J is used to hold the gated oscillator when an open line is detected, or turn off the gated oscillator if the line remains busy following a character received. The inputs to Z110J originate from CR-N and the signal line.

Idle Line Detector

3.42 The idle line detector, ILD, is state 0 when the line is busy or open, and is state 1 when the line is idle. With ILD in state 0, an idle line is detected as follows:

(a) The shift pulse generator advances the character bits in the shift register.

(b) The start bit (space) enters R10, changing R10 from state 0 to state 1.

(c) The -6 volt output from R10-I combined with a -6 volt output from Z109A (mark), will turn off the associated bit oscillator control and bit oscillator. With a ground input applied to CR-P0A, the -6 volt to ground output from R10-N applied to CR-0A will set CR to state 0, indicating a character received.

(d) The collective inputs from the line (D4M to Z110J-27), flip-flop CR (CR-N to Z110J-29), and the shift register (R10-N to Z108A-20) will release the gated oscillator, Z101. With all inputs unchanged for 13 ms, the gated oscillator will deliver a pulse. The pulse will set flip-flops R19 through R11 to state 1 (if not already in state 1), and CR to state 1. (OLD is already state 1 and ILD-P1A was not primed.)

(e) The CR-N output to the ILD-P1A input will prime flip-flop ILD. If the next start signal does not appear on the line following delivery of the first pulse, the gated oscillator will continue to time out toward a second pulse. In approximately 10 ms, the gated oscillator will deliver a second pulse which primarily sets flip-flop ILD to state 1 (line idle) through the ILD-1A input.

(f) The ILD-N output will apply ground to the Z108B-24 input, changing the Z108B output from ground to -6 volts. A -6 volt output, applied to Z108A-19, will cause the gated oscillator to stop and be reset.

3.43 Presuming that the signal line had been idle (ILD is state 1) and the start bit of a new character is present, the following events occur:

(a) The space bit applies a ground input to Z109B of the shift pulse generator, releasing the bit oscillator control.

(b) If the space bit is longer than 4.54 ms, the bit oscillator will deliver its first shift pulse, causing the state of each element of the shift register to be advanced.

(c) Element R10 becomes state 0 (mark bit shifted from R11 to R10), producing a -6 volt to ground output on R10-I.

(d) The input from R10-I applied to ILD-0A (ILD-P0A is primed from the ILD-N output) sets ILD to state 0, indicating a busy line.

B. Control Character Decoder (FS-2)

3.44 The control character decoder performs a function identical to a mechanical stunt box. It decodes, two bits at a time, seven characters and two partial characters (Form Effector and graphic). See Table 3. The control character decoder also provides memory elements (flip-flops) for some of these characters. Inputs to, and control of the decoder, is from the receiving selector. The elements of the shift register supply decoding inputs, and character received, CR, provides the on-off control. Decoding occurs only during the character storage interval, ie, the 13 ms period before the shift register is cleared.

Decoding

3.45 Initial decoding is done by gates Z108D and Z108E only after a character is received, ie, CR is state 0. The inputs to these

TABLE 3 - CHARACTERS DECODED

CHARACTER		CODE LEVEL						
FUNCTION	GRAPHIC	7	6	5	4	3	2	1
NULL		S	S	S	S	S	S	S
SOM		S	S	S	S	S	S	M
EOA		S	S	S	S	S	M	S
EOT		S	S	S	S	M	S	S
BELL		S	S	S	S	M	M	M
FORM EFFECTOR		S	S	S	M	-	-	-
ACK		M	M	M	M	M	S	S
DELETE		M	M	M	M	M	M	M
	GRAPHIC	S	M	-	-	-	-	-
	GRAPHIC	M	S	-	-	-	-	-

gates are from CR-I, R16, and R17. Subsequent decoding depends upon an output of -6 volts from either gate Z108D or Z108E. An output of -6 volts signifies that either levels 6 and 7 are marking or levels 6 and 7 are spacing (Figure 23). Both levels marking or spacing indicates that the character just received is a function (nontyping), not a graphic (typing). The control function will be further decoded by other control gates.

3.46 The outputs of Z108D and Z108E supply the two inputs to gate Z108F. If both inputs are ground, the character is not a function (level 6 marking and 7 spacing or vice versa), and the output of Z108F will be -6 volts. If either output of Z108D or Z108E is -6 volts, the output of Z108F will be ground. A ground output from Z108F indicates that the character decoded is not a graphic. The output of Z108F is used as one of the controls in detecting Call Directing Codes (CDC).

3.47 Bits 4 and 5 along with the previously decoded bits 6 and 7 are further decoded by gates Z109C, D, and E. If the control function is a Form Effector, level 4 is marking and levels 5 through 7 are spacing. The inputs to Z109C must be -6 volts if a Form Effector is detected; the output from Z109C will be ground. If levels 4 through 7 are spacing, all inputs to Z109D must be -6 volts; the output will be ground. As indicated in Table 3, the control function may be a NULL, SOM, STX, EOT, or BELL. If levels 4 through 7 are marking, all inputs to Z109E must be -6 volts; the output will be ground. Either ACK or DELETE have levels 4 through 7 marking.

3.48 Gates Z110A, B, and C decode bit 3 together with the outputs of gates Z109D and E. If all inputs to any one of these gates are ground, the output will be -6 volts. According to the table of characters to be decoded, levels 3 through 7 are spacing if the control function is a NULL, SOM, or STX. Level 3 is marking and 4 through 7 are spacing if the function is an EOT or BELL character. And levels 3 through 7 are marking if the character is ACK or DELETE. The output of gate Z110A is -6 volts if levels 3 through 7 are spacing; Z110B is -6 volts if level 3 is marking and 4 through 7 are spacing; or Z110C is -6 volts if levels 3 through 7 are marking.

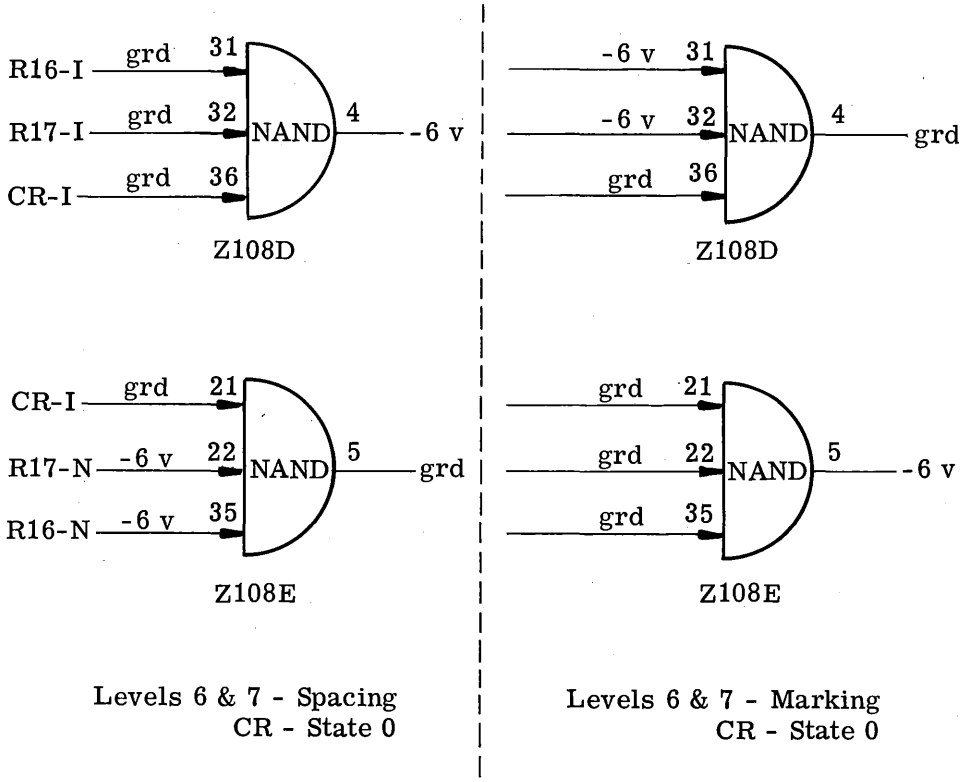


Figure 23 - Conditions of Control Gates When Decoding a Function Character

3.49 Bits 1 and 2 are decoded by gates Z110D and E and Z109F and H. Levels 1 and 2 are spacing for a NULL, EOT, or ACK. Levels 1 and 2 are marking for a BELL or DELETE.

3.50 Gates Z109F and H do the final decoding of STX and SOM. All the inputs to either of these gates must be -6 volts in order to get a ground output. The inputs of Z109F are from Z110A, R11-N, and R12-I. The output of Z109F will be ground when the character stored has bits 1 and 3 through 7 spacing and bit 2 marking. This defines a STX character. The output of gate Z109F is connected to an amplifier inverter, Z124H. Gate Z109H has inputs from Z110A, R11-I, and R12-N. The output of this gate will be ground when the character stored has bits 2 through 7 spacing and bit 1 marking. This is an SOM character.

3.51 Gates Z111A, B, C, D, and E combine the output of gates Z110A, B, C, D, and E to form the character remaining to be decoded. The inputs to a Z111 gate must all be -6 volts in order to get a ground output. Gate Z111A has inputs from Z110A and D. The output will be ground when the character stored has all bits spacing or is a NULL character. Gate Z111B has inputs from Z110B and Z110D. The output will be ground when the character stored in the shift register is an EOT. Gate Z111C has inputs from Z110B and E and will have a ground output when the character stored is a BELL. Gate Z111D has inputs from Z110C and D and will have a ground output when the character stored is ACK. Gate Z111E has inputs from Z110C and E and will have a ground output when the character stored is DELETE. The output of Z111E is connected to the inverter Z110F and provides a -6 volt output for DELETE.

Storage

3.52 The decoding storage elements consist of five flip-flops. These elements are state 0 by their associated decoding gate. Each will hold a decoded character for future use.

3.53 The FE (Form Effector) is state 0 (code stored) by either one of two inputs. It may be state 0 by means of the 0A input from the output of Z109C. The output of Z109C goes to ground when a Form Effector is stored in the receiving selector. The P0A input is connected to TM-I which is ground only during the text of a message. Therefore, a Form Effector will set FE to state 0 only if it occurs during a message text. FE may also be state 0 via its 0B input (P0B is self-primed) from the output of Z111A which goes to ground when a NULL character is received. FE may be state 1 via its 1A input from CR-N. The CR-N output returns to ground at the end of each character received (0.5 ms from the end of the stop pulse on the signal line). Input P1A is connected to the output of gate Z124J. The output of Z124J will be ground only if a Form Effector, NULL, or DELETE is not stored. Therefore, FE will return to state 1 by the first character received following a Form Effector or a NULL, that is not a Form Effector, NULL, or DELETE.

3.54 The remaining storage elements may be state 0 by their associated decoding gate whose output goes to ground when the associated code is received. SOM, BEL, and ACK flip-flops have their inputs connected to IR-I (initial response-inverted). The IR-I output is ground during the initial response of a polled station to its TSC (Transmitter Start Code). The three flip-flops (SOM, BEL, and ACK) can be state 0 only at this time. The P0A input of EOT is self-primed, and an EOT is accepted at any time.

3.55 The EOT, BEL, and ACK flip-flops have their 1A inputs (P1A inputs are self-primed) connected to ILD-I. The ILD-I output will go to ground when the signal line becomes busy, and will set the EOT, BEL, and ACK flip-flops to state 1. SOM is state 1 via its 1A input (P1A is self-primed) from the output of the EOT decoding gate, Z111B. SOM may also be state 1 via its 1B input (P1B is self-primed) from OLD-I. The OLD-I output goes to ground when an open line is detected.

C. System Condition Logic (FS-3)

3.56 The system condition logic monitors signal line activity after polling a station for traffic. The system condition logic enters the address mode upon detection of the second character of a TSC. If a message is to be sent from the polled station and the station adheres to the acceptable transmission format, the address mode remains active until a STX code is received. Otherwise, the address mode becomes inactive when a polled station responds with a maintenance or no traffic response, or does not respond at all. If message

text begins (ie, a STX is transmitted by the polled station), the system condition logic departs from the address mode and enters the text mode. The text mode ends when an EOT is received.

Mode Indicators

3.57 Address Mode, AM, Indicator: Flip-flop AM will enter state 0 after the second character of a TSC is generated, it remains in this condition as the polled station is transmitting CDC's. AM will go to state 1 when the system condition logic enters the text mode. AM can also become state 1 if the polled station responds with a BELL BELL (maintenance), \ ACK (no traffic), or fails to respond.

(a) State 0: AM may be state 0 through its 0A input from CR-I. CR-I goes to ground at the end of each selection cycle when a character is detected. The P0A input is connected through the D4N voltage divider to a normally closed contact of the V relay. If the second (variable graphic) character of a TSC is being generated, the V relay contact will be open, providing a ground output from D4N to P0A. AM will then be state 0 at the end of transmission of the second character of the TSC.

(b) State 1: AM will be state 1 when its 1A input (P1A is self-primed) from the output of Z124F is ground. The output of Z124F goes to ground when the TM flip-flop is state 0 or when the Line Controller goes into the text mode.

(c) State 1: AM may also be state 1 when its 1B input (P1B is self-primed) from Z123F is ground. The Z123F output will go to ground if an EOT, BELL, or ACK code is detected during the initial response. An EOT can occur if the polled station fails to respond within the tolerable time period (0.6 second), and the Line Controller generates a BK-pause-EOT code sequence. The BELL or ACK result from a maintenance or no traffic response by the polled station.

3.58 Text Mode, TM, Indicator: Flip-flop TM can enter state 0 upon receipt of a STX or when an open line is detected. TM will go to state 1 when an EOT is received. An inverter amplifier, Z124F, is associated with a TM-N output.

(a) State 0: Normally, TM is state 0 via its 0A input from the output of decoding gate, Z109F. Z109F goes to ground when a STX is decoded. TM-P0A is connected to the CDCR-I output. TM will enter state 0 if a STX occurs after at least one CDC is received.

(b) State 0: TM will also go to state 0 by means of its 0B input (P0B is self-primed) from OLD-I. The inverted output from OLD will go to ground when an open signal line is detected.

(c) State 1: TM will go to state 1 when an EOT is received. The 1A input of TM (P1A is self-primed) is connected to EOT-I. The I output of flip-flop EOT will go to ground when an EOT is in storage.

The TM flip-flop is then state 0 between receipt of a STX or a line break and an EOT.

Event Indicators

3.59 Initial Response, IR, Indicator: Flip-flop IR is state 0 at the end of transmission of a TSC. IR can be state 1 by either one of two means, ie, when the signal line goes idle following a transmission from a polled station, or following a line break or transmission of a STX.

(a) State 0: IR is state 0 by way of its 0A input (P0A is self-primed) from AM-I. AM-I goes to ground after the second character of a TSC is generated.

(b) State 1: IR is state 1 through the 1A input (P1A is self-primed) from PSS-N. PSS-N will become ground when the signal line goes idle following a transmission from a polled station.

(c) State 1: IR can be state 1 via the 1B input (P1B is self-primed) from TM-I. TM-I will go to ground following the transmission of a STX or a line break.

3.60 Polled Station Sending, PSS, Indicator: Flip-flop PSS will be state 0 when the polled station starts transmitting. PSS will normally be state 1 when the signal line goes

idle following the reception of a CDC. PSS may also be state 1 when the controller goes into the text mode.

(a) State 0: PSS may be state 0 via its 0A input from ILD-I. The ILD-I output goes to ground each time the signal line becomes busy. The P0A input is connected to the output of Z111F. The output of Z111F will be ground while AM is state 0 and CDCS is state 1. CDCS is state 1 when a CDC is not stored.

(b) State 1: Normally, PSS may be state 1 via its 1A input from ILD-N. Each time the signal line goes idle, ILD-N goes to ground. Input P1A is connected to Z110H. The output of Z110H will be ground when flip-flop SOM is state 1, or IR is state 0, or CDCS is state 1. The function of Z110H is to control the operation of PSS following the reception of an SOM (keyboard mode of transmission). Normally, SOM is state 1, and the output of Z110H is ground. If an SOM is received in the initial response, the output of the gate, Z110H, will be ground during the initial response and upon receipt of a CDC. Therefore, PSS will normally be state 1 when the signal line goes idle following the reception of a CDC.

(c) State 1: PSS may also be state 1 via its 1B input (P1B is self-primed) from the output of Z124F. When the controller goes into the text mode, the output of Z124F goes to ground.

3.61 Tape Leader, TL, Indicator: Flip-flop TL will be state 0 upon detection of the first busy line following the transmission of a TSC. TL will go to state 1 after the polled station has transmitted all the DELETE characters in the tape leader, preceding the first CDC. Or in the case of an SOM (keyboard entry), TL will go to state 1 when the line goes idle following transmission of the DELETE character. TL may also be state 1 if the controller goes into the text mode.

(a) State 0: TL is state 0 via its 0A input from ILD-I. P0A is connected to IR-I. IR-I is ground when the second character of a TSC is detected in the receiving selector. ILD-I goes to ground when the line goes busy following the first idle line after transmission of the TSC. TL will then be state 0 on the first busy line following the transmission of a TSC.

(b) State 1: TL may be state 1 via its 1A input from Z101L, the output of the gated oscillator in the receiving selector. P1A is connected to the decoding gate, Z110F. When a DELETE character is decoded, the output of Z110F is -6 volts. When anything but a DELETE character is impressed on gate Z110F, the output goes to ground. Therefore, TL will not be state 1 as long as DELETE characters are received during the initial start of transmission from the polled station.

(c) State 1: TL may also be state 1 via its 1B input (P1B is self-primed) if the output of Z124F goes to ground, ie, when TM is in state 0.

3.62 Graphic Counter, GC, Indicator: Flip-flop GC will be state 0 when the first graphic of a CDC is received from the polled station during the message preamble. GC will be state 1 when the polled station transmits the second graphic of a CDC, transmits a function, or the Line Controller is in the text mode. GC is a graphic counter whose set inputs, 0A and 1A, are connected to the N output of CR. A positive transition from -6 volts to ground will occur on CR-N, approximately 13 ms after a character is detected in the receiving selector.

(a) State 0: The prime input, P0A, of GC is connected to the output of control gate Z111H. The output of Z111H will be ground only if the polled station is sending during the address mode (PSS is state 0), GC is state 1, and a graphic is decoded by gate Z108F. When these conditions are met, a transition to ground (applied to 0A) will cause GC to go to state 0.

(b) State 1: The reception of any character other than the first graphic of a CDC will cause GC to be state 1. If the first graphic has been received (GC-I is ground), the polled station is sending (PSS-N is -6 volts), and a second graphic is received (Z108F is -6 volts), the output of Z111H will be -6 volts. Hence, a positive transition to ground on CR-N (occurring 13 ms after a character is received) will cause GC to go to state 1 via its 1A input (P1A is self-primed).

3.63 CDC Stored, CDCS, Indicator: Flip-flop CDCS will go to state 0 when the second character of a CDC is received. CDCS is normally state 1 when an ACK character is received. CDCS may also be state 1 when TM is state 0 (controller is in the text mode).

(a) State 0: The prime input, P0A, of CDCS is connected to gate Z111J whose output is ground if a graphic is decoded and PSS is state 0. The 0A input to CDCS is connected to GC-N. A positive transition to ground will occur on GC-N when GC goes from state 0 to state 1. If the P0A input is ground when GC goes to state 1, CDCS will go to state 0. This will occur if two graphics are received in sequence during the address mode.

(b) State 1: CDCS is normally state 1 via its 1A input (P1A is self-primed) from the output of the ACK decoding gate, Z111D. The output of Z111D will go to ground when an ACK character is received.

(c) State 1: CDCS may also be state 1 via its 1B input (P1B is self-primed) from the output of Z124F whose output goes to ground when TM is state 1 (controller is in the text mode).

The receipt of the first graphic of a CDC will set GC to state 0. The next character received will set GC to state 1, and its output will set CDCS to state 0 if that character is a graphic. In this way a CDC is detected. If the two graphics are not transmitted, one following the other during the address mode, CDCS will not be state 0.

3.64 CDC Received, CDCR, Indicator: CDCR will enter state 0 when at least one CDC is received. CDCR may be state 1 when the controller goes into the text mode (TM is state 0).

(a) State 0: CDCR is state 0 via its 0A input (P0A is self-primed) by the output of Z108J. The output of Z108J goes to ground (positive transition) when CDCS goes from state 0 to state 1. The positive transition normally occurs after an ACK character to a CDC, is received.

(b) State 1: CDCR is state 1 via its 1A input (P1A is self-primed) when TM is state 0 (when the controller enters the text mode).

(c) State 1: CDCR may also be state 1 via its 1B input (P1B is self-primed) which goes to ground when an EOT is received. This input resets CDCR if an EOT is received before a STX.

3.65 Format Deviation Detector, FDD: Flip-flop FDD is used in conjunction with other elements to detect errors in the format of a CDC sequence. FDD is disabled when the polled station is in the keyboard mode of transmission. FDD will be state 0 at the end of the character following a CDC. This is at the time when a DELETE character of the CDC sequence should be stored in the receiving selector. FDD will become state 1 when the signal line next goes idle.

(a) State 0: FDD may be state 0 via its 0A input from CR-N which goes from -6 volts to ground approximately 13 ms after a character is detected in the receiving selector. The P0A input is tied to the output of Z109J. The output of Z109J is ground if the polled station is sending from tape (PSS is state 0 and SOM is state 1) and a CDC is stored (CDCS is state 0). When primed, FDD will be state 0 after the following character is received.

(b) State 1: FDD will be state 1 via its 1A input (P1A is self-primed) from ILD-N. ILD-N is ground when the signal goes idle.

D. Timing Control Logic (FS-4)

3.66 The timing control logic is used to determine when the line controller should take a form of action other than generating a TSC. It consists of control gates, gated oscillators, and flip-flops. The flip-flops determine when the Line Controller should disconnect a polled station or intercept a message.

System Errors

3.67 Control gates Z117A, B, C, and D are used to detect errors in system operation that require the Line Controller to immediately respond with a BK-pause-EOT sequence. A -6 volt output from the signal accumulator gate, Z117D, will cause the BK-pause-EOT sequence to be generated. A -6 volt output from Z117D will occur if the output of Z117A, B, or C is ground.

3.68 Z117A permits the use of a STX only following a CDC or in the text of a message. The inputs to Z117A are from CDCR-I, TM-I, and Z124. The output of this gate will be ground if a STX occurs (Z124H is -6 volts)

before a CDC is received (CDCR is state 1) and the controller is not in the text mode (TM is state 1).

3.69 Z117B will determine if the tape reader at the polled station, has stopped following the transmission of a CDC. The inputs to Z117B are from FDD-N and R10-N. The output of this gate will be ground if the receiving selector is busy (R10 is state 0) before an idle line occurs following the graphic-graphic-DELETE sequence of a CDC (FDD is state 0).

3.70 Z117C will be ground after 0.60 second of idle line if a CDC is not stored. The inputs to Z117C are from FTI-N and CDCS-I. The N output of FTI will become -6 volts after 0.6 second of idle signal line. If a CDC is not stored, CDCS-I is -6 volts (CDCS is state 1).

Timer Control Gate

3.71 Gate Z122H is a signal accumulator for gated oscillators Z118, Z218, and Z119. Since an input pulse is generated only after a gated oscillator has timed out, each input to Z122H is normally -6 volts, and the normal output of Z122H is ground. A positive output pulse from any one of the three gated oscillators, Z118, Z218, or Z119, will cause the output of Z122H to become -6 volts. A -6 volt output from Z122H will cause a BK-pause EOT sequence to be generated.

3-Second Timer

3.72 Control gates Z117E, F, and H and gated oscillator Z118 are used to place a 3-second time limit on certain operations of the system. The output of Z118 is connected to control gate, Z122H (3.71). Gated oscillator Z118 will start its 3-second timing cycle when its input from Z117H is -6 volts. Z117H will have an output of -6 volts if either one of the inputs from Z117E or Z117F is ground.

3.73 Z117E determines when an idle line exists after a form effector code is received. The inputs to Z117E are connected to FE-N and Z122J. Z122J is an inverter amplifier whose input is connected to ILD-N. The output of Z122J will be -6 volts when the signal line is idle. The output of the control gate Z117E will then be ground while the signal line is idle following the reception of a form effector or NULL (FE is state 0). If this condition persists for a period of 3 seconds, the gated oscillator will deliver an output pulse, and the output of gate Z122H will go to -6 volts, causing a BK-pause-EOT sequence to be generated.

3.74 Z117F detects the transmission of identical characters from a tape reader during the text of a message. When two identical characters exist in registers R1 and R2 (during the text mode and originating from a tape reader), the output of Z117F will go to ground, causing Z117H to release the 3-second gated oscillator. If identical characters continue to appear on the line for more than 3 seconds (or 30 identical characters), the gated oscillator will deliver an output pulse, causing a BK-pause-EOT sequence to be generated. If less than 30 identical characters are received, the gated oscillator will be stopped and reset. The inputs to Z117F are connected to CI-N, TM-N, and SOM-I. The output of Z117F will be ground while the comparison indicator, CI, is state 0, text mode, TM, is state 0, and SOM is state 1 (not keyboard operation).

1-Second Timer

3.75 Control gates Z117J, Z123A, and Z123B and gated oscillator Z218 are used to place a 1-second time limit on certain transmissions between an EOT and STX. The output of gated oscillator Z218 is connected to Z122H (3.71). The input to Z218 is from the output of Z123A. If both inputs to Z123A are ground, the 1-second gated oscillator will start its timing cycle. The inputs to Z123A are from Z123B and Z117J.

3.76 The inputs to Z123B are from SOM-I and CDCS-N. The output of Z123B will be ground if one of the following three combinations occur:

(a) A CDC is stored (CDCS is state 0) while transmitting from tape (SOM is state 1). SOM-I and CDCS-N are both -6 volts.

(b) A CDC is stored (CDCS is state 0) while transmitting from the keyboard (SOM is state 0). SOM-I is ground and CDCS-N is -6 volts.

(c) A CDC is not stored (CDCS is state 1) while transmitting from tape (SOM is state 1). SOM-I is -6 volts and CDCS-N is ground.

3.77 The output of Z117J will be ground when the inputs from TM-I, TL-I, and Z108H are -6 volts. Therefore, if TM is state 1 (between an EOT and STX), TL is state 1 (not tape leader), and ILD is state 0 (line busy), Z117J is ground.

3.78 The output of Z123A will be -6 volts (gated oscillator on) while the signal line is busy if:

(a) The controller is not in the text mode or receiving tape leader, or

(b) If in the keyboard mode, only while a CDC is stored.

30-Second Timer

3.79 Control gate Z122A and gated oscillator Z119 are used to place a 30-second time limit upon tape leaders and all idle line periods. Specifically, the 30-second idle line period will apply to keyboard operation when an SOM disables the 0.60-second gated oscillator during anticipated manual transmissions. Also, the 30-second idle line output of Z119 is used to drive shift register R2 for the purpose of counting 16 pulses. This provides the 8-minute delay period for a poll rest free condition of the Line Controller.

3.80 The output of the gated oscillator, Z119, is connected to Z122H. When the gated oscillator delivers an output pulse, a BK-pause-EOT sequence will be generated via control gate Z122H (3.71). The input to Z119 is connected to the output of Z122A. The output of Z122A must be -6 volts for 30 seconds in order for the gated oscillator to deliver an output pulse. If either one of the inputs to Z122A is ground, the output will be -6 volts.

3.81 Z122A will be ground while either the signal line is idle or a tape leader of DELETE characters is being transmitted. The inputs to Z122A are from ILD-N and TL-I.

→ Idle Line 1.0 Second Timer

3.82 Control gate Z123J and gated oscillator → Z219 provide a 1.0 second idle line period under certain circumstances. The output of Z219 is connected to the 0A input of FTI (fail time indicator). The input to Z219 is connected to Z123J. The output to Z123J must be → -6 volts for 1.0 second in order for Z219 to deliver an output pulse.

3.83 All inputs to Z123J must be ground in order to have a -6 volt output. The inputs to Z123J are connected to ILD-N, FE-N, and the output of Z123B. The output of Z123J will be -6 volts when the signal line is idle (ILD is state 1), a form effector was not the last character received (FE is state 1), and if one of the three following conditions exist:

(a) A CDC is stored (CDCS is state 0) while in the tape mode (SOM is state 1). This applies to idle line periods before transmission of the answer-back sequence to a CDC.

(b) A CDC is not stored (CDCS is state 1) while in the tape mode (SOM is state 1). This applies to idle line periods during message text.

(c) A CDC is stored (CDCS is state 0) while in the keyboard mode (SOM is state 0). This applies to idle line periods before transmission of the (automatic) answer-back sequence to a CDC.

Line Break Generator, LBG

3.84 Flip-flop LBG will cause the generation of a BK-pause-EOT sequence when biased to state 0 by an abnormal condition or by exceeding certain timing limits. LBG may be state 0 when anything but a DELETE character follows the two graphic CDC in automatic (tape) transmission. LBG may go to state 1 when an open line is detected or may go to state 1 when the line goes busy.

(a) State 0: LBG is state 0 via its 0A input (P0A is self-primed) from Z123C. Gate Z123C serves as a signal accumulator for outputs from Z117D (system errors - 3.67) or Z122H (timing limits - 3.71).

(b) State 0: LBG may also be state 0 via its 0B from FDD-I. The output of FDD-I will go to ground after the reception of the character following the two graphic sequence of a CDC (tape transmission, only). P0B is connected to the output of decoding gate Z111E via inverter Z110F. The output of Z110F is -6 volts if a DELETE character is received. If any other character or condition exists, Z110F is ground and LBG will then be state 0.

(c) State 1: LBG will go to state 1 (if not already there) when the signal line goes busy. The 1A input (P1A is self-primed) is connected to the output of Z122J which goes to ground when the signal line goes busy.

(d) State 1: LBG may also be state 1 via its 1B input (P1B is self-primed) from OLD-I. The output of OLD-I goes to ground when an open line is detected.

Fail Time Indicator, FTI

3.85 Flip-flop FTI will cause an * ACK code sequence to be generated when a CDC is stored, or a BK-pause-EOT sequence to be generated under all other circumstances. FTI may go state 1 when an open line is detected or may go to state 1 when the line goes busy.

(a) State 0: FTI will be state 0 via its 0A input (P0A is self-primed) from the output of gated oscillator Z219 (3.82 and 3.83).

(b) State 1: FTI will go state 1 (if not already there) when signal line goes busy. The 1A input (P1A is self-primed) is connected to the output of Z122J which goes to ground when the signal line goes busy.

(c) State 1: FTI may also be state 1 via its 1B input (P1B is self-primed) from OLD-I. The output of OLD-I goes to ground when an open line is detected.

E. Polling Control Logic (FS-5)

3.86 The polling control logic determines if and when a TSC should be generated. It also determines whether the next or the same TSC should be generated. The polling control logic contains a message counter and one arc of the Poll SS (step switch) to control multiple polling.

Polling Control Gates

3.87 The Line Controller will generate the next TSC in the polling sequence if the line is idle, an EOT is received or an ACK or BELL is received on initial response only, and a multipoll is not requested. The control gate associated with the generation of the next TSC is Z122F.

3.88 The output from Z122F will be ground (generate TSC) when all inputs from LBG-I, Z123H, and Z122E, are -6 volts. LBG-I is -6 volts when no line break is indicated, ie, LBG is state 1. The output from Z123H is -6 volts when both inputs from Z108H and Z123F are ground. The output from Z108H will be ground when the line is idle, ie, ILD-I is -6 volts. The output of Z123F will be ground if any one of its three inputs is -6 volts. The inputs to Z123F are EOT-N, ACK-N, and BEL-N. When any one of these characters is received (ACK or BELL on initial response only), its respective flip-flop goes to state 0 causing the normal, N, output to be -6 volts. The other two flip-flops remain in state 1. The output of Z122E is -6 volts if the input from Z122D is ground (input from Z123H must be -6 volts). The output from Z122D is ground when the message counter flip-flops, MC1, MC2, and MC3, are state 1.

3.89 The Line Controller will repeat the same TSC if the output from Z122E is ground. The inputs to Z122E from Z123H and Z122D must be -6 volts for an output of ground from Z122E. The output from gate Z122D will be -6 volts if at least one message counter flip-flop is state 0.

Multipoll Selection

3.90 The stations which are to be polled more than once during a single polling sequence, are selected by programming the last row on the TSC program panel. If a station has been preselected for multiple polling, the circuit is closed between the output of the Poll SS and PPG-26. When the Poll SS is resting on the position associated with the preselected station, the output of D4P will then be -8 volts. This output is connected through 2 inverters, Z123D and Z125J. The output of Z125J will then be -6 volts for a multipoll station and ground for those not programmed.

Message Counter

3.91 Flip flops MC1, 2, and 3 plus gates Z122C and D, Z123E and Z125H form the message counter. MC1, 2, and 3 are interconnected as a shift register. When a shift pulse is applied to the 0A and 1A inputs of each of these elements, the state of one is shifted to the next.

3.92 The output of MC3 is connected to the input of MC1 in a reverse fashion. If MC3 is in state 0, a shift pulse will set MC1 to state 1, or if MC3 is in state 1, a shift pulse will set MC1 to state 0. Normally, all elements are state 1. The output of Z125H is connected to the 0A and 1A inputs of each of the elements. This output is normally -6 volts until the first CDC of a message is received. When the first CDC is received, CDCR goes from

state 1 to state 0 causing a ground to -6 volt transition on CDCR-N. The transition becomes positive, ie, -6 volts to ground, when inverted by gate Z125H.

3.93 Gate Z122C has inputs from Z125J, SOM-I, and MC3-I. The output of this gate must be ground in order to set MC1 to state 0 and start the count. All inputs to Z122C must be -6 volts to have a ground output. A ground output will occur when the station just polled is selected for multipolling, an SOM is not stored, and MC3 is state 1.

3.94 If the output of Z122C is ground, the first ground transition (when the first CDC is received) from the output of Z125H, will cause MC1 to be state 0. The remaining elements will still be state 1. The next shift signal (occurring when the first CDC of the second message is received) will shift state 0 into MC2 and MC1. The third shift signal will shift state 0 into MC1, 2, and 3. The fourth shift signal will shift state 1 into MC1 and state 0 into MC2 and 3. The fifth shift signal will shift state 1 into MC1 and 2, and state 0 into MC3. The sixth and final shift signal will shift state 1 into all elements.

3.95 The inputs to gate Z122D are from the I outputs of MC1, 2, and 3. In order for the output of this gate to be ground, all the inputs must be -6 volts or all the counting elements must be state 1. A ground output from Z122D indicates that the count is not occurring or that the count has been completed.

3.96 The output of gate Z123E is connected to the 1B inputs (P1B inputs are self-primed) of the MC flip-flops. If the output of Z123E goes to ground, all the elements of the counter will be state 1. Z123E will go to ground if any one input goes to -6 volts. The inputs of Z123E are connected to OLD-N, ACK-N, and BEL-N. If an open signal line occurs or if an ACK or BELL character is received (on the initial response only), the output of Z123E will go to ground. Therefore, an open line or a no traffic or maintenance response will cancel additional polling of a multipoll station.

F. Register 2 (FS-6)

3.97 Register 2 is used to store the second character of a CDC. The register includes a character comparison circuit to detect the transmission of identical characters. It also includes the means for counting 16 pulses (at 30-second intervals from the timing control logic) to establish an 8-minute idle line period during the poll rest free condition of the Line Controller.

Register 1 Load Indicator and Associated Gates

3.98 Flip-flop R1L is the load indicator for register R1; it is used to indicate the presence of a new character in the receiving selector. R1L is state 0 when a character is available in register 1 and is state 1 when the character has been shifted into register 2. Gates Z317A and Z317B are associated with R1L.

(a) State 0: R1L may be state 0 via the 0A input from CR-I. The output from CR-I goes to ground each time a character is stored in the receiving selector. The P0A input to R1L is connected to Z317B. The output of Z317B will be ground if either one of its two inputs from TM-N and Z317A, is -6 volts. The inputs to Z317A are connected to CDCS-N and PSS-I. The output of Z317A will be -6 volts when the polled station is sending and a CDC has not been received. The output of Z317B will, therefore, be ground while the polled station is sending before a CDC is received or during message text. R1L will be state 1 upon receipt of a character in the receiving selector if the P0A input is ground.

(b) State 1: R1L is state 1 via its 1A input (P1A is self-primed) from the output of the gated oscillator Z318. A pulse occurs when the character is transferred to register 2.

Register 2 Load Indicator and Associated Controls

3.99 Flip-flop R2L is the load indicator for register R2. The associated controls consist of gate Z317D and gate oscillator Z318. When R2L is state 0, a character is stored in register 2. The inputs to gate Z317D are from R1L-I and R2L-N. If the output of Z317D is -6 volts for approximately 2 ms, the gated oscillator, Z318, will deliver an output pulse. Both inputs must be ground to produce this -6 volt output. This requires that a character be

stored in register 1 and that register 2 is empty.

(a) State 0: The output of the gated oscillator is connected to the 0A input of R2L. When the output pulse occurs, R2L will be state 0 (P0A is self-primed).

(b) State 0: R2L may also be state 0 via the 0B input (P0B is self-primed) from RTS-N. The output from RTS-N goes to ground when a rest condition is cleared. (Since register 2 is used as a counter, the count already stored must be cleared. This is done by treating it in this register as a superfluous character transmitted by the polled station.) When RTS is state 1, it will set R2L to state 0.

(c) State 1: R2L may be state 1 via its 1A input from Z418-L. This is the output of a gated oscillator which delivers an output pulse when the character stored in register 2 is shifted into register 3. The P1A input is connected to ACC-N. The output of ACC-N (address character counter — normal) is -6 volts only when the second character of the CDC is shifted out of register 2 and on its way to the interceptor tape. R2L will then be state 1 via its 1A input, in all cases except when the DELETE character of the CDC, which is not stored, is to be regenerated (when the output of ACC-N is -6 volts).

Storage Elements

3.100 The storage elements consist of flip-flops R28 through R21. These elements are used as a storage register via the A inputs and as a shift register via the B inputs. The storage register has parallel inputs from shift register R1 of the receiving selector. The elements of R2 are used as a counter when operated as a shift register.

3.101 Storage Register: If R1L is state 0 (full) and R2L is state 1 (empty), the gated oscillator, Z318, will time out. The output pulse of Z318 will set R1L to state 1 (empty), R2L to state 0 (full), and apply a pulse on the 0A inputs to R28 through R21, causing the character stored in R1 of the receiving selector, to be duplicated in register 2.

(a) State 0: The P0A inputs of the elements of R2 are connected to the associated I outputs from R1. Normally, all elements of R2 are state 1. If a space (state 0) is stored in one or more of the elements of R1, its I output and associated P0A input to R2 will be ground. A pulse applied to the 0A inputs of R2 will set the associated elements to state 0. In this way the character in the receiving selector is duplicated in register 2 and stored.

(b) State 1: A stored character is removed from register 2 (all elements are state 1) via the 1A inputs (P1A inputs are self-primed) from the output of Z418, a gated oscillator, Z418 serves a function identical to Z318, ie, the output of Z318 causes information to the transferred from R1 to R2; the output of Z418 causes information to be transferred from R2 to R3. Z418 also resets register 2 (the receiving selector resets R1). When an output pulse occurs from Z418, R28 through R21 and R2L are state 1.

3.102 Shift Register (Counter): Elements R28 through R21 are interconnected as a shift register via their B inputs. Shift pulses are applied via the 0B and 1B inputs from the output of Z119, the 30-second delay gated oscillator. The gated oscillator, Z119, will time out only while the signal line is idle. Register 2 will be emptied within 200 ms following an idle signal line. All of the elements will be state 1 at the start of the counting process (Table 4). If the count is completed during the poll rest free condition, the output of R21, which occurs after 8 minutes of idle signal line, will restart the polling sequence. If the polling sequence is started while a count is occurring in register 2, R2L will be state 0 via its 0B input from RTS-N. The existing count will then be handled as a standard stored character and be cleared by register 3.

(a) State 0 and State 1: The N and I outputs of R21 are connected to the P0B and P1B inputs of R28. A state 1 in R21 will become a state 0 in R28 when a pulse is applied to the 0B and 1B inputs. The state of R28 is then shifted to R27, etc, as R28 becomes state 0 via the inputs from R21. When R21 becomes state 0, the inputs to R28 will cause R28 to become state 1. The output of the counter is taken from R21-N which will go to ground following the 16th pulse of Z119.

TABLE 4 - COUNTING PROCESS OF REGISTER 2

SHIFT PULSE	STATE OF FLIP-FLOP ELEMENTS								ELAPSED TIME (MINUTES)
	R28	R27	R26	R25	R24	R23	R22	R21	
Start Poll Rest	1	1	1	1	1	1	1	1	0.0
1	0	1	1	1	1	1	1	1	0.5
2	0	0	1	1	1	1	1	1	1.0
3	0	0	0	1	1	1	1	1	1.5
4	0	0	0	0	1	1	1	1	2.0
5	0	0	0	0	0	1	1	1	2.5
6	0	0	0	0	0	0	1	1	3.0
7	0	0	0	0	0	0	0	1	3.5
8	0	0	0	0	0	0	0	0	4.0
9	1	0	0	0	0	0	0	0	4.5
10	1	1	0	0	0	0	0	0	5.0
11	1	1	1	0	0	0	0	0	5.5
12	1	1	1	1	0	0	0	0	6.0
13	1	1	1	1	1	0	0	0	6.5
14	1	1	1	1	1	1	0	0	7.0
15	1	1	1	1	1	1	1	0	7.5
16	1	1	1	1	1	1	1	1	8.0

Character Comparison

3.103 The character comparison circuits consist of flip-flop CI, Exclusive OR gates Z311A, B, C and Z411A, B, C, and gates Z316A, B, Z317C, and Z322H. CI is state 0 when the character received and stored in R1 is identical to the character stored in R2. CI is state 0 when the comparison occurs and will remain there until a comparison does not occur.

3.104 Exclusive OR gates Z311A, B, C, and Z411A, B, C, have I inputs from registers R1 and R2. Each gate compares a pair of associated inputs, eg, R16-I and R26-I, to determine like or unlike inputs. The output of each OR gate will be -6 volts if the two elements supplying the inputs are in identical states, but if the inputs are not identical, the output of each OR gate will be ground. The inputs to Z316A and Z316B accept the outputs from the six Exclusive OR gates. If all the inputs to Z316A and B are -6 volts (characters compare), the output of both gates will be ground. The output of Z316A and B are inputs to Z317C. The output of Z317C will be -6 volts if both inputs are ground (characters compare).

(a) State 0 and State 1: The output of Z317C is connected to the P1A input of CI and to the input of inverter Z322H. The

output of Z322H is connected to the P0A input of CI; it will be ground for a comparison and -6 volts for no comparison. In other words, input P0A will be ground for like characters or P1A will be ground for unlike characters. The 1A and 0A inputs are connected to the output of gated oscillator, Z418. An output pulse will be generated from this gate each time information is to be cleared from register 2.

During the message text of an automatic transmission (from tape), the output pulses of Z418 occur while a character is stored in the receiving selector (R1) waiting to be transferred into register 2. The output of CI is used only at this time and is connected to gate Z117F (3.72). This gate will allow the 3-second gated oscillator to run only during the text portion of a tape message, if a character comparison is detected.

G. Register 3 (FS-7)

3.105 Register 3 consists of a storage and shift register and its associated controls. R3 also contains controls to allow operation as a transmitting distributor and gates to decode two control characters.

Register 3 Load Indicator and Associated Controls

3.106 Flip-flop R3L is the register 3 load indicator. Associated with R3L are gates Z316E, Z317E, and gated oscillator Z418. The function of R3L is almost identical to that of R1L and R2L. When it is state 0, R3L indicates that a character (or part of a character, as described later) is stored in register 3. The N output of R3L is connected to the input of Z317E. The other input to this gate is from R2L-I. If R3L is state 1 (empty) and R2L is state 0 (full), the output of Z317E will be -6 volts. This output will allow gated oscillator Z418 to run. After 2.5 ms, Z418 will deliver an output pulse to the 0A input of R3L and will set it to state 0 (P0A is self-primed). The output of Z418 also sets the elements of R2 to state 1 as described in 3.101 (b).

3.107 R3L may be state 1 by either one of two means. The 1A input is connected to the output of the gated oscillator, Z323. Gated oscillator Z323 serves as a character timer for the transmitting distributor. Each time an output pulse occurs from Z323, R3L is state 1 (P1A is self-primed). The 1B input of R3L is connected to the I output of R1L which goes to ground when a character to be stored is received by the receiving selector. The P1B input is connected to the output of Z316E. If both inputs to Z316E from R2L-N and R3L-N are -6 volts, the output is ground. R2L-N and R3L-N are -6 volts when both of the registers are full. R3L will then be state 1 (empty) via its 1B input when a character is received for storage and registers 2 and 3 are full. This mode of operation will unload the third register when a new character is received and must be stored. It also serves as character timing when the transmitting distributor is running in synchronism with the signal line.

Storage Elements

3.108 The storage elements consist of flip-flops R38 through R31. These elements are used as a storage register via the A inputs and as a shift register via the B inputs. The storage register has parallel inputs from register 2 (R2). The elements of R3 also serve as a shift register of a transmitting distributor.

3.109 Storage Register: The P0A inputs of each element of register 3 are connected to their associated I output of each element of register 2. All of the elements of R3 are normally state 1. When a pulse is applied to the 0A inputs, the character stored in register 2 is reproduced in register 3. The 0A inputs are connected to the output of gated oscillator, Z418. When the pulse from Z418 occurs, R28 through R21 and R2L are state 1 while R3L and spacing elements of R38 through R31 are state 0. The 1A inputs of R38 through R31 are connected to the inverter amplifiers, Z316C and D. The outputs of Z316C and D will go to ground when R3L is state 1 (empty). A ground output from Z316C and D will set R38 through R31 to state 1 (the P1A inputs are self-primed).

3.110 Shift Register (Transmitting Distributor): The B inputs of R38 through R31 are connected as a shift register. Upon application of a shift pulse to the 1B and 0B inputs, the state of one element will be shifted into the next adjacent flip-flop element. The character bits are shifted from the higher numbered to the lower numbered flip-flop element, eg, R38 to R37, R37 to R36, etc. The P1B input of R38 is self-primed. The shift pulse is applied to

the 1B input, setting R38 to state 1. The state 1 (mark) condition (inserted in R38 each time a shift pulse is applied) is shifted along the register following the character bits. By this means, all the register elements will be left in a state 1 condition following the transmission of a character. The outputs of R31 are connected to R30 which is part of the transmitter controls.

Transmitter Controls

3.111 The transmitter controls consist of start (space) bit R30, output element OE, transmit switch TS, bit oscillator Z423, gated oscillator Z323, and a group of control gates. The output of the bit oscillator, Z423, supplies shift pulses to R38 through R31 of the storage register and flip-flops R30 and OE. The inputs to R30 and OE are via 1B and 0B. The prime inputs are connected in such a manner as to continue the shift register that ends with R31. R30 is state 0 via its 0A input from the gated oscillator, Z418. Each time a character is shifted into register 3, R30 will be state 0 (space). R30 is used to insert the start bit into the transmitted signal. The first shift pulse from bit oscillator Z423, will shift the start bit (space, state 0) from R30 into OE and start the output line signal. The subsequent bits of the character will be shifted, in turn, through R30 and appear as outputs from OE.

3.112 The input to bit oscillator Z423 is connected to the input of gate Z322C (Figure 24). The emitter of unijunction transistor, Q1 on Z423, has a voltage swing, while oscillating, of approximately -1 to -9 volts. If the input to one of the diodes CR12 or CR14 is ground, CR13 will be back biased. While back biased, CR13 will have no effect upon the oscillation occurring at the emitter of Q1. If both inputs are -6 volts, the voltage at the cathode of CR13 will be -6 volts, and the emitter of Q1 and the timing capacitor C2 will be held at -6 volts. Therefore, if the two inputs (from OE-I and Z322B) to Z322C are -6 volts, the equivalent output to Z423 will be ground, and the bit oscillator will be held off.

3.113 The two inputs to Z322C are from OE-I and Z322B. If a space appears in OE (state 0 with I output ground) or if the output of Z322B is ground, the oscillator will continue to run. The output of Z322B will be ground if both of its inputs are -6 volts. The inputs to gate Z322B are from Z322A and TS-N.

3.114 Gates Z322A, Z317F, and Z317H are used to determine if any spacing bits, ie, some elements are state 0, remain in R36 through R30. The inputs to gates Z317F and H are from the N outputs of R36 through R31. If any one of these outputs is -6 volts (space), the output of one of the gates will be ground.

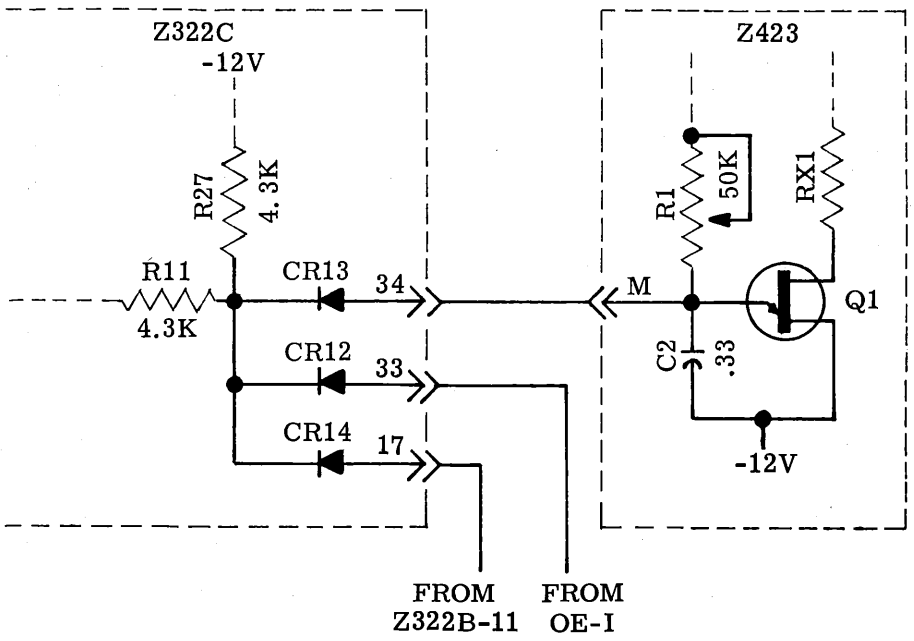


Figure 24 - Control Connection Between Gate Z322C and Bit Oscillator Z423

Gate Z322A will have a -6 volt output if any one of its inputs is ground. The inputs to Z322A are connected to Z317F, H, and R30-I. Therefore, if a space appears in one or more elements of R36 through R30, the output of Z322A will be -6 volts.

3.115 The second input to Z322B is from TS-N. If the character in register 3 is to be transmitted to the intercept reperforator, TS-N will be ground. The output of Z322B will be ground if there is any portion (space) of a character in elements R36 through R38 and if the controller is to intercept that character. The presence of a space in elements R38 and R37 is not required. When TS is state 0 and the transmitter starts, R30 is already state 0. Two shift pulses are required from Z423, to first move the start bit into OE and secondly, replace the start bit in OE with the following bit. The two shift pulses would move bit 8 to R37 and then to R36. Since marks (state 1) are inserted in R38, both R38 and R37 will be state 1 following the second pulse.

3.116 The transmit switch, TS, is used to convert the storage register into a transmitting distributor. Associated with TS is a gated oscillator, Z323, and control gates Z125D, E, F, and Z322D. TS is state 0 via its 0A input (P0A is self-primed) from TA-I (transmit address-inverted). The I output of TA will go to ground when the CDC stored in registers 2 and 3 is to be intercepted. TS may also be state 0 via its 0B input which is connected to the output of Z316E and will go to ground when registers 2 and 3 are full following the command to intercept text. Input P0B is connected to TT-I (transmit text-inverted). TT-I will be ground when the text appearing in register 3 is to be intercepted.

3.117 TS may be state 1 via its 1A input from the output of the gated oscillator, Z323. Gated oscillator Z323 serves as a character timer when the transmitting distributor is not running in synchronism with the signal line. Control gate Z125F provides the input to the gated oscillator. Z323 will run when the output of Z125F is -6 volts. In order to have a -6 volt output, both inputs, connected from R3L-I and Z125E, must be ground. The input from R3L-I will be ground if a character is stored in register 3. The output of Z125E will be ground if either one of its inputs is -6 volts, ie, TS is state 0 or the output of Z125D is -6 volts. Z125D will have a -6 volt output if TM and AM are state 1 (neither text nor address modes). The gated oscillator, Z323, will deliver an output pulse 110 ms after register 3 is loaded and TS is state 0 or AM and TM are state 1. It will run, therefore, if a character is available in register 3 and is to be intercepted or the Line Controller is in the free line condition (neither text nor address modes).

3.118 The output of gated oscillator Z323 is connected to the 1A input of R3L. If a character appears in R1L every 100 ms while a message is being intercepted, R3L will be state 1 via its 1B input. The I output of R3L will shut off the gated oscillator, Z323, via gate Z125F and recycle it (the time cycle of Z323 is 110 ms and would not deliver an output pulse). When gated oscillator Z418 delivers an output pulse 2.5 ms later, a new character will be set into register 3 and R3L will be state 0 via its 0A input. The output of R3L will turn on gated oscillator Z323 via gate Z125F. When the next character is received in 100 ms and R3L is again state 1, gated oscillator Z323 will again shut off and reset. Z323 will deliver an output only when the line signal is not available to reload register 3.

3.119 The output of Z323 is also connected to the 1A input of TS. The P1A input is connected to the output of gate Z322D. The output of Z322D will be -6 volts when the intercept logic wishes to intercept characters. If either TA or TT is state 0, the output of gate Z322D will be -6 volts and characters will continue to be intercepted. When both TA and TT are state 1, the output of Z322D will be ground and the output pulse of gated oscillator Z323 will set TS to state 1. The output of TS will then shut off the bit oscillator via gate Z322B. When text is being intercepted, the gated oscillator, Z323, will always clear (be used as a character timer) the last two characters transmitted. Z323 also acts as a character timer for intercepted CDC's.

Decoding Gates

3.120 Gates Z316F, H, J and Z317J are character decoding gates. The output of Z316F will be ground when a STX is shifted into register 3. The output of Z316H will be ground for an EOT. The outputs of Z316F and Z316H are used to control the intercept logic.

3.121 If bits 5, 6, and 7 are spacing, the output of gate Z316J will be ground. The output of Z316J together with R34-I and R31-I

supply inputs to Z317J. The output of Z317J will be -6 volts if bits 1 and 4 through 7 are spacing.

3.122 Gates Z316F and H decode bits 2 and 3 together with the output of gate Z317J. Gate Z316F has inputs from Z317J, R33-N, and R32-I. The output of gate Z316F will be ground when all of the inputs are -6 volts, ie, when bits 1 and 3 through 7 are spacing and bit 2 is marking. Gate Z316H has inputs from Z317J, R33-I, and R32-N. The output of gate Z316H will be ground when bits 1, 2, and 4 through 7 are spacing and bit 3 is marking.

→ 3.123 Since bit 8 is marking in both STX and EOT, decoding may be controlled conveniently. The output of the decoding gates will not occur until either the character is cleared from the register (R3L is state 1) or the transmitter starts (Z423 starts to distribute the character). In the case of clearing the character from the register, all elements are state 1 and there will not be a ground output from either gate. When the first shift pulse occurs (in the case of a distributed character), the state 1 in R38 is shifted to R37. A state 1 in R37 will inhibit a ground output from both Z316F and H.

H. Intercept Control Logic (FS-8)

3.124 The intercept control logic is used to start and stop the transmitting distributor, and provide control of the tape feed-out mechanism of the intercept typing reperforator.

Transmit Address Indicator and Address Character Counter

3.125 The transmit address, TA, indicator is state 0 at the command to intercept a stored CDC. The address character counter, ACC, is used to count the characters transmitted to the intercept reperforator.

3.126 TA may be state 0 via its 0A input from the I output of FTI. Output FTI-I will go to ground each time the line is idle for → more than 1.0 second. P0A is connected to CDCS-I which will be ground when a CDC is stored in registers 2 and 3. TA will then be → state 0 if the signal line is idle for 1.0 second following the receipt of a CDC. TA is state 1 via its 1A input (P1A is self-primed) from ACC-N.

3.127 Gate Z322E controls the operation of ACC. If both inputs from TA-N and ACC-I are -6 volts, the output of Z322E which is connected to the P0A input of ACC, will be ground. Therefore, if TA is state 0 and ACC is state 1, the output of Z322E will be ground.

3.128 The I output of TA connected to the 0A input of TS (P0A is self-primed) will set TS to state 0 when TA goes to state 0. This will start the transmitter, and the character stored in register 3 will appear sequentially in flip-flop OE. While this and the following characters are being transmitted to the intercept reperforator, the Line Controller is generating the * ACK response. The input to the storage registers is closed (output of gate Z317A on FS-6 is -6 volts) during this time. The 110 ms gated oscillator, Z323, will be used as a character timer, and its output is used to reload register 3 with a new character.

3.129 The 1A and 0A inputs to ACC are connected to the 110 ms gated oscillator, Z323 (FS-7). Following the transmission of the first character of the CDC, Z323 will deliver an output pulse which will set ACC to state 0 (P0A is still ground). The N output of ACC connected to the P1A input of R2L (FS-6), will become -6 volts. The output pulse from Z323 will also empty register 3 and set ACC to state 0. Approximately 2.5 ms later, an output pulse from gated oscillator Z418 will reload register 3 with the second character of the CDC. The pulse from Z418 will also set all the elements of register 2 to state 1. Since the P1A input of R2L is -6 volts from the output of ACC-N, Z418 will not set R2L to state 1. Therefore, R2L will continue to indicate a character stored, and this character will have all bits marking (all elements of register 2 are state 1). By this means the DELETE character following the second graphic of the CDC is regenerated in register 2.

3.130 Following the transmission of the second character of the CDC, another pulse from Z323 will occur. This pulse will set ACC to state 1. The N output of ACC is connected to the 1A input of TA, and goes to ground. This will set TA to state 1 (P1A is self-primed). With TA in state 1, the P1A input of TS via Z322D, will be ground. Following the transmission of the third character (DELETE) of the CDC sequence, the output pulse of Z323 will set TS to state 1. This will turn off the transmitter, and R3 will revert to a storage register.

Intercept Text, IT, and Transmit Text, TT, Indicators

3.131 Flip-flop IT is used to indicate that a CDC has been intercepted. TT controls the transmitter while the text is being intercepted. The N output of TA goes to ground as the last character (DELETE) of the CDC sequence is being transmitted to the intercept reperforator. TA-N will then set IT to state 0 via the 0A input (P0A is self-primed), thus indicating that a CDC has been intercepted.

3.132 Characters transmitted from the polled station will continue to appear in register 3 following the interception of a CDC. When STX appears in register 3, the output ← of gate Z316F (FS-7) connected to the 1A input of IT and the 0A input of TT, will go to ground. P1A of IT is self-primed while P0A of TT is connected to IT-I. When the output of gate Z316F goes to ground (a STX in register 3), ← IT will be state 1 and TT will be state 0, if IT had been state 0.

3.133 The I output of TT will apply ground to the P0B input of TS (FS-7). When register 2 becomes full (2.5 ms later), the output of gate Z316E will go to ground and set TS to state 0 via its 0B input. The transmitter will then start and send the message text headed by the STX, to the intercept reperforator. ←

3.134 TT may be state 1 via its 1A input from the bit oscillator, Z423. P1A is connected to the output of gate Z316H (FS-7), which will go to ground when an EOT is shifted into register 3. When an EOT is shifted into register 3, the first output pulse of the bit oscillator will set TT to state 1. The I output of TT is connected to gate Z322D (FS-7). The output of Z322D will go to ground supplying ground to P1A of TS. At the end of transmission of the EOT, an output pulse from gated oscillator Z323 will set TS to state 1, and the transmitter will turn off.

3.135 The 1B input of IT is connected to the output of decoding gate Z316H (EOT). The P1B input is self-primed. A ground input on 1B will reset IT in case the Line Controller generates a line break before the start of text.

Tape Feed-Out Control

3.136 Tape feed out is controlled by gate Z322F; the output of this gate is connected to the input of relay driver, Z128B. The output of the relay driver energizes the feed-out magnet of the typing reperforator. Diode D3P is used as an arc suppressor to protect Z128B.

3.137 The feed-out mechanism of the typing reperforator is noninterferring and is actuated by the operation of the feed-out magnet. The relay driver will turn on if its input is ground. The output of gate Z322F will be ground if all the inputs are -6 volts. The inputs are from the I outputs of TA, IT, and TT. Tape will be fed out whenever all of these elements are state 1, such as at the end of a text or following an interruption of an intercepted message (at any point in the message).

Intercept Transmitter Output

3.138 The N output of OE (output element) is connected to the input of Z228A. This relay driver is used to drive the input of the selector magnet driver (SMD). If OE is state 1, the N output will be ground which, applied to the input of Z228A, will cause the output of Z228A to conduct. Current flow will cause the selector magnets to energize (marking). The current path is from the -12 volt source, through the selector magnet driver, and to ground in the relay driver. When OE is state 0, the N output will be -6 volts, cutting off the relay driver and causing a spacing signal.

I. Stop Control Logic (FS-9)

3.139 The purpose of these circuits is to control the operation of the poll step switch in order to generate subsequent TSC's. It provides facilities for inputs from the START, STOP, and BREAK keys and the associated logic elements for their proper operation.

Step Switch Control Relay

3.140 The P relay is used to control the movement of the poll step switch. The input to operate P is from the output of relay driver, Z126A. The input to this relay driver is from gate Z122F (FS-5). The output of Z122F, will go to ground if the signal line is idle and an EOT, ACK, or BELL response has been received (ACK or BELL on initial response to a TSC only). Relay driver, Z126A, will provide a ground for the P relay when the input is ground. The operate path includes a normally closed STOP key contact,

BREAK key contact, POLL SS interlock, and the normally closed contacts of relays EOT, DC, and P. When relay P energizes, contact 5P transfers, and the relay is held to ground via P5M and the normally closed INT contacts of the POLL SS. Operation of P will cause the DC and POLL SS relays to operate (FS-11 and 12). Associated contacts 4DC and 3INT (of POLL SS) will open and cause relay P to de-energize. Open contact 4DC prevents the P relay from being reoperated by relay driver Z126A.

STOP and START Key Control

3.141 A make contact of the START key operates between a -48 volt source and voltage divider D4S. The output of D4S is connected to the input of inverter amplifier Z125A. In the normal position of the START key, the output of Z125A will be -6 volts. When the START key is operated, the output Z125A will be ground. A break contact of the STOP key is connected from a -48 volt source, through the POLL SS interlock, to the input of D4R. The output of D4R is connected to inverter amplifier Z125B. In the normal position of the STOP key, the output of Z125B is ground. When the STOP key is operated, this output will be -6 volts.

3.142 The outputs from Z125A and B supply both inputs to gates Z124A and Z125C. The output of gate Z124A will be ground if both inputs are -6 volts. An output of ground from Z124A will occur if the STOP key is operated and the START key is not. The output of Z124A is connected to the input of inverter Z124C. Therefore, the output of Z124C will be -6 volts if the STOP key is operated and the START key is not. The output of Z125C will be -6 volts if both inputs from Z125A and B are ground. A -6 volt output from Z125C will occur if the START key is operated and the STOP key is not. The output of Z125C is connected to the input of gate Z108B (3.41) which provides a control for the gated oscillator, Z101 (FS-1). If the output from Z125C goes to -6 volts while the signal line is idle, the gated oscillator, Z101, will time out (13 ms) and deliver an output pulse.

3.143 Controls DC-7M and A-11M provide an alternate path from a -48 volt source to gate Z125A. When the first character of the TSC is being generated, these contacts will be closed and duplicate the operation of the START key.

Rest Time Switch and Associated Circuits

3.144 Flip-flop RTS is the rest time switch. Associated with RTS is relay driver Z126B. The function of RTS is to stop the generation of a BK-pause-EOT sequence when the Line Controller goes to a poll rest condition. RTS also provides a visual indication of a poll rest condition through relay driver Z126B and the STOP lamp.

3.145 RTS may be state 0 via its 0A input from the I output of flip-flop FTI. FTI-I will go to ground when the signal line has been idle for 1.0 second. The P0A input is connected to the output of gate Z122F which is ground when a poll of the next station is required. RTS will then be state 0 if a poll is requested and does not occur in 1.0 second. The suppression of polling may be accomplished in two ways. The P relay will not operate (and the next TSC will not be generated) if the STOP key is operated. The CB contacts of the STOP key will open the operate path between relay driver Z126A and the P coil. Polling will not occur when the POLL SS steps on to position 26. If it stops on this position (end of polling cycle), RTS will also be state 0.

3.146 RTS may be state 1 via its 1A input from the output of R21-N. This output originates from the counter formed by register 2 (3.79 and 3.102). R21-N will go to ground if the signal line has been idle for 8 minutes. The P1A input is connected to the output of Z125B. The output of Z125B will be ground if the STOP key is not operated. RTS will then be state 1 after 8 minutes of idle signal line if the STOP key is not operated.

3.147 RTS may also be state 1 via its 1B input, connected to the output of the gated oscillator, Z101, in the receiving selector. A pulse will occur at this output at the end of a signal line character, the clearing of an open line, or if the START key is operated during an idle signal line (via gate Z125C). The P1B input is connected to the output of Z124C. This output will be -6 volts if the STOP key is operated and the START key is not. RTS will then be state 1 if the signal line becomes busy and the STOP key is not operated, or if the START key is operated during an idle signal line while the STOP key is operated.

3.148 The I output of RTS is connected to the input of relay driver Z126B. When RTS is state 0 (poll rest condition), the output

of the relay driver will conduct (provide ground) and turn on the STOP lamp via diode D3F. If the STOP key is operated, a path from the output of Z126B to the P relay coil is conditioned via the STOP key contacts AB. If the START key is now operated, the P relay will be energized, and the next TSC will be generated. When the following TSC is to be generated, RTS will again be state 0, and the START key must again be operated to generate another TSC. This operation allows the polling cycle to be manually stepped by the START key. When the end of the polling cycle is reached and the POLL SS stops on step 26, operation of the START key will not cause the generation of the next TSC since contact DC-4B will remain operated to open the operate path of the P relay.

Note: Removal of the POLL SS (for maintenance) will not permit manual polling by operation of the START key. However, removal of the POLL SS will not produce an adverse effect upon a message that might be occurring on the signal line at the time of removal.

J. Line Break Control (FS-10)

3.149 The line break control circuit provides the logic for the generation of the BK-pause-EOT sequence. Circuits are also provided to detect failure in the intercept reperforator; the logic is included to determine whether a BK-pause-EOT sequence must be generated as a result of this failure.

Line Break and EOT Relays

3.150 The operation of the LB (line break) relay will cause a 0.300 second break signal to be generated. The operation of the EOT relay will cause the generation of an EOT character 0.200 second after the EOT relay has operated. Thus, a BK-pause-EOT sequence is generated.

3.151 The input to operate the LB relay is from relay driver Z226A. The input to the relay driver is from gate Z124B. If both inputs to Z124B are -6 volts, its output will be ground. The inputs to Z124B are connected to RTS-I and LBG-N. The output of gate Z124B will be ground if flip-flop LBG is state 0 and RTS is state 1. A ground output from gate Z124B will cause relay driver Z226A to conduct (provide ground) which operates the LB relay via the EOT-2B and LB-5B contacts. The LB relay may also be energized by operating the BREAK key.

3.152 When the LB relay operates, it is held to ground via contacts LB-5M and EOT-3B. The BK-pause-EOT sequence is generated on the signal line via the mechanical distributor and associated relays (FS-13). Following the generation of the BREAK, the C1 relay will operate. The EOT relay will then operate via contacts C1-4M, LB-4M, and EOT-5B; relay EOT will lock via contacts EOT-5M and LB-3M. (The LB relay is still held operated via contact LB-5M, diode D3B, and contact C1-4M.) Operation of the EOT relay will cause the C1 relay to be released (FS-13). When C1 releases, the hold path to relay LB is broken, and LB will release. The hold path for relay EOT is now via contacts EOT-5M and C1-4B. At the end of the EOT generation, C1 will again operate, releasing relay EOT.

Reperforator Failure Detection Circuits

3.153 Relay IN is the intercept nonoperative relay and is normally energized. Relay IN operates as a detection relay for certain malfunctions in the circuits associated with the reperforator. Relay MI is the message intercept indicator.

3.154 Normally, the IN relay is held operated via contacts IN-8M, V-2B, 3 and 4 of FA2, 2 and 3 of MOTOR RUN, and IN-10M. When the second character of the TSC (variable) is being generated, the V relay is operated. The hold path is then via contacts 1 and 2 of the INTERCEPT DISABLE switch, 4 and 6 of the LOW TAPE switch, 3 and 4 of FA2, 2 and 3 of MOTOR RUN, and IN-10M. When the first character of the TSC (DC_O) is being generated, the DC relay is operated; contact DC-9M shunts contact IN-10M in the hold path.

3.155 The MOTOR RUN and LOW TAPE contacts are associated with the typing reperforator. The MOTOR RUN contact is part of a centrifugal switch mounted on the shaft of the reperforator motor. Contacts 2 and 3 (of MOTOR RUN switch) are closed while the shaft is rotating. The LOW TAPE switch on the tape container assembly is mounted next to the reperforator; contacts 4 and 6 are closed when there is tape in the container. The FA2 relay and INTERCEPT DISABLE switch

are mounted in the electrical service assembly. The FA2 relay coil is connected across the power supply of the SMD (FS-8). Contacts 3 and 4 of the FA2 relay are closed if the power supply is delivering its output voltage. The INTERCEPT DISABLE switch is intended for use while a tape roll is being changed or maintenance is being performed on the reperforator.

3.156 If either the motor of the reperforator stops or the power supply of the SMD fails, the hold path to IN will be broken and the IN relay will release. If the INTERCEPT DISABLE switch is operated or the LOW TAPE contacts open, relay IN will release at the next operation of the V relay (V-2B opens). If IN is released, it may be reoperated only when the DC relay operates. The reoperate path of the IN relay is then via contacts INTERCEPT DISABLE, LOW TAPE, FA2, MOTOR RUN, and DC-9M.

3.157 The MI (message intercept) relay operates through contacts IN-8M, AST-2M, and MI-8B. Its hold path is via contacts LB-3B, DC-10B, and MI-8M. When a CDC is intercepted and the Line Controller generates an * ACK sequence, the AST relay operates. If IN is operated (in normal state), a path to ground is established to the coil of relay MI, thereby energizing relay MI. If a BREAK is generated or the next station is polled, relay LB or DC will operate, opening the hold path of relay MI and causing it to release.

3.158 If the IN relay has released before the AST relay operates, the operate path to the coil of MI will be held open by contact IN-8M. Contact IN-8B will close to cause the INTERCEPT OFF lamp to light. If the MI relay operates and then IN releases, the LB relay will operate via contact IN-8B, diode D3D, contact MI-10M, and contact LB-5B. A BK-pause-EOT sequence will be generated if the reperforator fails (relay IN releases) when the Line Controller is committed to intercept a message (relay MI operated).

K. TSC and Response Encoding Logic (FS-11)

3.159 The relays in the TSC and response encoding logic are used primarily to encode the signal line during the generation of their associated characters. The DC and V relays are used in the generation of TSC's. The AST and ACK relays are used to encode a response to an unanswered CDC. The four relays are broken into two identical counter type circuits.

Relay Operation

3.160 The input to relay driver Z226B is from the output of gate Z122E. The output of gate Z122E will be ground when a station is to be repolled (3.89). The ground input to Z226B will turn on the output transistor and close a path to operate the DC relay via contacts DC-5B and V-6B. If the next station is to be polled, the P relay will operate and provide a path to operate the DC relay via contacts P-1M, DC-5B, and V-6B. The holding path for relay DC is via contacts B1-3B, DC-5M, and V-6B. Operation of the DC relay will cause the signal line distributor to start (FS-13). At the completion of the transmission cycle, the A1 relay will operate (via the distributor auxiliary contact). A path to operate the V relay will be closed via contacts A1-2M, DC-2M, and V-5B. Relay V will operate and hold via contacts B1-3B and V-5M. Contact V-6B will open, breaking the hold path to release relay DC. Following the transmission of the second character of the TSC, relay B1 will operate. Contact B1-3B will open, breaking the hold path for relay V, and V will release.

3.161 The operation of the AST and ACK relays are also controlled by the A1 and B1 relays. The AST relay is operated from the output of relay driver Z127B via contacts AST-5B and ACK-2B. The input of Z127B is connected to the output of gate Z124D. Relay driver Z127B will conduct (provide ground) when the output of Z124D is ground. Both inputs from FTI-N and CDCS-N must be -6 volts for a ground output from Z124D. Both of these inputs will be -6 volts if the signal line is idle for 1.0 second while a CDC is stored. When Z127B turns on, AST will operate and lock via contacts B1-3B, AST-5M, and ACK-2B. Following the transmission of the * character, relay A1 will operate (via the distributor auxiliary contact). The ACK relay will then operate, releasing the AST relay. Following the transmission of the ACKNOWLEDGE character, the B1 relay will operate (via the distributor auxiliary contact), releasing the ACK relay.

L. Polling Step Switch Control (FS-12)

3.162 The polling step switch control circuits are associated with the POLL SS relay coil. These circuits govern the operation of

this coil, and therefore, the station to be polled. Included in these circuits are the SKIP keys and the relay to allow polling to continue following the polling of the 25th station (end of polling cycle).

POLL SS Coil Operation

3.163 The normal path to operate the POLL SS coil is via the P-2M contact. The P relay is operated from a relay driver and is released by a normally closed INT contact of the POLL SS (3.140). Operation of the P relay will close contact P-2M to energize the POLL SS coil. Operation of the POLL SS will open the normally closed INT contacts and release the P relay. In this manner the step switch is moved to the next position (station).

3.164 The SK relay, associated with the POLL SS, determines when the step switch has stopped stepping. Relay SK is normally held operated via contact DC-3B. Relay DC is operated when P operates. SK will then be held via contact P-2M, contact POLL SS INT, and diode D2K. When the POLL SS is operated, the INT contacts will open, breaking the hold path to both P and SK. The diode arc suppressor, CR6, around the SK coil, will increase the release time of SK to about 30 ms. Following the transmission of the DC_0 character, relay DC will release; relay SK will again operate via contact DC-3B.

Skipping Circuits

3.165 The skip station keys are connected through arc 1 of the POLL SS in such a manner, that if one of these keys is operated, the POLL SS will step over that position (station). When the P relay is released allowing the POLL SS coil to release, the arc brush will advance to the next position. If the skip key associated with that position is operated, a path to ground for the POLL SS coil will be established. The ground path is via the station skip key, through arc 1 of the POLL SS, and contact POLL SS INT. The alternate ground path will immediately reoperate the POLL SS coil (and also hold relay SK). When the POLL SS coil is operated, the INT contact will open the ground path and release the POLL SS coil. The brush on arc 1 will then move to the next station. In this way station skipping is achieved.

Continue Polling

3.166 Relay CP is used to achieve continued polling. That is, CP allows the step switch to advance beyond position 26 without stopping and placing the Line Controller in a poll rest condition.

3.167 Normally when the step switch moves to position 26, the O.N. contacts 5 and 6 will close and hold relay SK operated. With relay SK operated, the operation of the distributor will be inhibited, and the count cycle of relays DC and V will not occur. DC will remain operated. In order to continue polling, the step switch must be moved off position 26. This may be done by first operating the B1 relay to release relay P, and then reoperating relay P (P may not be reoperated until DC is released, see FS-9). This requires that the Line Controller generate a BK-pause-EOT sequence. The generation of a break will operate B1, releasing DC; and the EOT will cause the next station to be polled (operate P).

3.168 The step switch may also be moved off position 26 by operating the coil directly. This may be accomplished via contacts CP-10M and O.N. 2 and 3. The CP relay is operated from the output of relay driver Z227A. The input to Z227A is from CDCR-I which will turn on (and operate the CP relay) if a CDC is received during the polling sequence. CP will hold via contacts O.N.-1M and CP-8M. When the POLL SS steps to position 26, the O.N. contacts will transfer, and O.N.-3B will be closed. A ground path will then be provided to the POLL SS and cause it to operate. The hold path for relay CP is now via contact CP-8M, diode D2R, and contact INT-3B (FS-9). When the coil operates, contact INT-3B will open, releasing the CP relay. When CP releases, CP-10M will open, breaking the ground path to the POLL SS coil. The POLL SS coil will then release and move the brushes to position 1. In this manner, if a message is started during a polling sequence (at least one CDC transmitted), the Line Controller will not enter the poll rest free condition at the end of the polling cycle.

M. Transmitter Control Logic (FS-13)

3.169 The transmitter control logic consists of a three unit counter operating in conjunction with the auxiliary contact and clutch magnet of the mechanical distributor.

The mechanical distributor is used as the line transmitting device for the Line Controller. Inputs and partial control of the counter are from relays ACK (FS-11), AST (FS-11), EOT (FS-10), DC (FS-11), LB (FS-10), SK (FS-12), and V (FS-11).

Counter Operation

3.170 Normally, all relays are released and the path to the clutch magnet is open. If a TSC is to be generated, the DC relay will operate. When the POLL SS comes to rest, the SK relay will release. A ground path to the clutch magnet will then exist via contacts SK-1B, DC-1M, and A-12B. The clutch magnet will energize and the distributor will start. As the transmission cycle starts, the auxiliary contact will close and provide a ground path to relay A via contacts B1-2B and A1-1B. With relay A operated, the path through contact A-12B to the clutch magnet will be open, and the magnet will release. The A-12M contact will supply ground to the 2L side of the A1 relay coil.

3.171 At the end of the first character transmission cycle, the auxiliary contact will open. Current flow through the A relay coil will now flow through the A1 relay coil to ground via contacts A-12M, DC-1M, and SK-1B. Operation of the A1 relay will cause the operation of the V relay, followed by the release of relay DC (see FS-11). When V operates, a ground path to the clutch magnet will be closed via contacts V-1M and B-12B. A hold path for relays A1 and A will be supplied via contact V-1M, diode D3H, and contact A-12M, following the release of relay DC.

3.172 The operation of the clutch magnet is followed by the closure of the auxiliary contact. This will provide a ground path for the B relay via contacts B1-2B and A1-2M. Operation of relay B will open the ground path to the clutch magnet via contact B-12B. At the end of the second character transmission cycle, the auxiliary contact will open again. The current flowing through relay B will also flow through relay B1 via contacts B-12M and V-1M, and relay B1 will operate. Operation of relay B1 will cause relay V to release (see FS-11). The V-1M contact will then open and release relays A, A1, B, and B1. This ends the transmission of a TSC.

3.173 The operation of this circuit to generate an * ACK is identical to the generation of a TSC, except that the AST and ACK relays would control its operation.

3.174 BK-pause-EOT Sequence: If a BK-pause-EOT sequence is to be generated, the LB relay will operate. A ground path to the clutch magnet will be closed via contacts LB-2M, EOT-1B, and C-12B, and the clutch magnet will energize. As the distributor runs, the auxiliary contact will operate and release. The A, A1, B, and B1 relays will operate on the first two open and closures of the auxiliary contact (first two cycles of the distributor). When the third closure of the auxiliary contact occurs (third cycle of the distributor), a ground path to relay C is closed via contact B1-2M. Relay C will operate and break the ground path, via contact C-12B, to the clutch magnet, causing the clutch magnet to release. When the auxiliary contact opens, relay C1 will operate via contact C-12M in the same manner as relays A1 and B1. Operation of C1 will cause relay EOT to operate (FS-10) and open the hold path through contact EOT-1B to relays A, A1, B, B1, C, and C1, causing them to release. Release of relay C1 will cause the release of relay LB (FS-10). During the sequential operation of the counter and LB relays, the distributor rotates through three cycles of operation, or for a time period of 300 ms. During this period, contact LB-1B (FS-15) holds the signal line open to provide a BREAK for 300 ms.

3.175 When relay LB releases after relay EOT operates, a ground path to the clutch magnet is then closed via contacts LB-2B, EOT-1M, and C-12B. The clutch magnet will then operate to start the next transmission cycle. Since contacts B1-1B and EOT-12M shunt the signal line (FS-15), a pause (or idle line) will occur until relay B1 is operated. Relays A, A1, B, and B1 will operate in sequence during the first two revolutions of the mechanical distributor. Therefore, the signal line will be idle for 200 ms preceding the distribution of the EOT. When relay B1 operates, contact B1-1B will remove the shunt from the signal line. As relay C operates, the EOT is distributed on the signal line. When the C1 relay operates, contact C1-4B will release relay EOT (FS-10). Release of relay EOT will break the hold path to the count relays and they will all release.

3.176 The distributor clutch magnet circuit includes a -48 volt source, the distributor clutch magnet with arc suppressor networks, and resistor R2. R2 is a current limiting resistor for the clutch magnet.

N. External Alarm Logic (FS-14)

3.177 The external alarm logic provides most of the circuits used to operate visual and audible alarms. It contains a group of dry reed relays used to hold the No-Response alarms, and other elements to provide flashing lamp indications.

Maintenance Alarm Circuits

3.178 The MT relay is used to indicate a maintenance alarm condition. The MT relay is operated via contact MT-8B from the output of relay driver Z128A. The input of Z128A is connected to BEL-I. This input will go to ground causing relay Z128A to operate (provide ground) when a BELL character is received in the initial response from a polled station to its TSC. Relay MT will hold via contacts B and C of the RESET key, B and C of the MTC key, and contact MT-8M. Operating either the RESET or MTC key will then release the MT relay and clear the alarm condition. The MTC lamp is illuminated when the MT relay is operated via contact MT-12M and the power flasher. The alarm buzzer is also turned on via contact MT-11M.

No-Response Alarm Memory

3.179 The inputs to gate Z124E are from FTI-N and IR-N. If both of these inputs are -6 volts, the output of gate Z124E will be ground and the relay driver Z227B will turn on (provide ground). Both inputs to gate Z124E will be -6 volts if the signal line is idle for 0.60 second following the transmission of a TSC by the Line Controller. The output of the relay driver is connected to the coil of the AL relay via diode D2L and contact AL-5B. When relay AL operates, its hold path is via contact AL-5M and contacts B and C of the RESET key. The relay driver, Z227B, also provides ground to one of the NR relays via diode D2J and a step of arc 3 of the POLL SS. If a polled station does not respond, relay driver Z227B will provide ground to operate the NR relay associated with that station. An NR relay will lock via contacts B and C of the RESET key and contact A associated with the operated NR relay. Operation of the RESET key will release the AL relay and any NR relays that may be operated.

Control of Station Lamps

3.180 The lamp associated with each station may be illuminated by any one of three ways.

(a) If the skip station key is operated (locking), a ground path for the associated station lamp is provided via the D and E contacts of the skip key.

(b) The POLL SS provides a ground path to each station lamp as its associated station is using the signal line. This path is provided via arc 2 of the POLL SS.

(c) If a station fails to respond to its TSC and its associated NR relay operates, an alternate ground path is provided to its station lamp. The ground path is from the output transistor, Q1, of the power flasher, through the B contact of the associated NR relay, and through an isolating diode. This path provides a flashing station lamp associated with a no-response alarm.

Alarm Buzzer

3.181 The alarm buzzer may be energized by any one of three inputs. They are:

(a) No-response — relay AL operates to close contact AL-1M in the buzzer circuit.

(b) Maintenance response — relay MT operates to close contact MT-11M in the buzzer circuit.

(c) Intercept inoperative — relay IN releases to close contact IN-11B in the buzzer circuit.

If the alarm cut-off key is operated, contacts B and C of the ACO key will open to silence the buzzer. Contacts D and E will provide a ground path for the ACO lamp causing it to light when the ACO key is operated.

O. Transmitter Encoder (FS-15)

3.182 The transmitter encoder consists primarily of a group of relay contacts and step switch arcs. These provide a system

of parallel bits for the contacts of the mechanical distributor. Associated with the step switch arcs is the TSC program panel which provides facilities for programming the variable character of each TSC. The receiving relay, RR, operating in conjunction with signal line activity, is also included.

Normal Signal Path

3.183 The normal signal line path is from TB SIGNAL LINE 3, through contact LB-1B, the SS (Stop-Start) contact of the mechanical distributor, the coil of the RR relay, and to TB SIGNAL LINE 1. The SS contact may be shunted by contacts EOT-12M and B1-1B in series. Normal signal line current flows through relay RR. The -48 volt source supplies approximately 10 ma of bias current for the RR relay, through the R4 resistor and RR coil resistance. The 2200 ohm resistor, R3, is used to supply a local line battery of 20 ma for test purposes.

Encoding of BK-pause-EOT

3.184 When the LB relay operates, the LB-1B contact will open the signal line, independent of the distributor operation. The distributor does operate, but only to provide timing for the BREAK via the transmitter control logic (FS-13). Following the third character cycle (300 ms), relay LB releases, the count relays of FS-13 release, and relay EOT operates. The signal line will be shunted past the distributor via contacts EOT-12M and B1-1B. At the second opening of the auxiliary contact of the distributor (while the EOT relay is operated), relay B1 will operate, opening the shunt path. During the interval between the release of relay LB and the operation of relay B1, the signal line is idle (pause) for 200 ms. After relay B1 operates, the signal line current flows through the SS contact of the distributor.

3.185 During the third operation of the distributor, signal line current must flow sequentially through the bit contacts of the distributor. Current can flow through EOT-11M, which is associated with bit contact 3, and V-12B, which is associated with bit contact 8. The character generated, which has bits 3 and 8 marking and all others spacing, is an EOT. Operation of the EOT relay will then produce two character cycles of marking signal (pause) followed by an EOT.

Encoding of DC_O, AST, #, ACK

3.186 When the DC relay is operated, a closed path to the return leg of the signal line is provided for bits 5 and 8 by contacts DC-12M and V-12B. The character generated, which has bits 5 and 8 marking and all other bits spacing, is a DC_O character.

3.187 When the AST relay is operated, either an * or # character may be generated, depending upon the state of relay IN (intercept nonoperative). If IN is operated (normal), a return path is provided for bits 2, 4, 6, and 8 via contacts AST-10M, IN-12M and AST-11M, AST-12M, and V-12B, respectively. The character generated is an *. If the IN relay is released, the character generated will have bits 1, 2, 6, and 8 marking. This character is #.

3.188 When the ACK relay is operated, a closed path to the return leg of the signal line is provided for bits 3, 4, 5, 6, 7, and 8 by the make contacts ACK 7, 9, 10, 11, and 12 and contact V-12B. All bits will be marking except 1 and 2; the character generated is ACK.

Encoding of the Variable Character

3.189 With the V relay operated, bit contacts 1 through 5 and 8 are connected to the brushes of arcs 5 through 10, respectively, of the POLL SS. Bit 7 (always marking for an alpha-block graphic) is connected to the signal line via contact V-11M. Steps 1 through 25 of arcs 5 through 10 are connected to the TSC program panel. To program a mark for a given bit, a closed path through the TSC program panel is provided by depressing the particular pin on the program panel. When the step switch selects a station, the mechanical distributor will scan the program pins associated with that station, following the generation of DC_O. A character will be produced having bit 6 spacing, bit 7 marking, and bits 1 through 5 and 8 dependent upon the programming at that position of the POLL SS.

P. Power Circuits (FS-16)

3.190 These circuits provide for the distribution of 117 v ac to the selector magnet driver, typing reperforator and base, distributor base, and power supply module. Power to

the Line Controller is received from a local 117 v ac source and is distributed to the various electrical components via the electrical service assembly.

3.191 The electrical service assembly includes a selector magnet driver and intercept disable switch (FS-10) for the typing reperforator, fuse field, fail alarm relays, alarm buzzer, terminal board assembly, and terminal blocks. The LC connector to the distributor base originates from the terminal board assembly; the LC connector provides power for the distributor motor. The CE connector to the typing reperforator base also originates from the terminal board in the electrical service assembly, and provides power for the reperforator motor and ribbon shift (print suppression) magnet. The power supply module receives 117 v ac via the terminal board and PSA connector. Connector PSD accepts the several voltage outputs from the power supply module. The voltage outputs are routed through the fuse field of the electrical service assembly and some are extended to the control module of the Line Controller via connector Ø1.

4. WIRING DIAGRAM REFERENCE CHART

4.01 The following chart serves to correlate the references made in this section to the 7150WD in Section 581-121-400. All other areas of the 7150WD not referenced in this section will also be listed.

WIRING DIAGRAM REFERENCE CHART

TITLE	7150WD SHEET NO.
Apparatus Index	A3
FS-1 Receiving Selector	B1
FS-2 Control Character Decoder	B2
FS-3 System Condition Logic	B3
FS-4 Timing Control Logic	B4
FS-5 Polling Control Logic	B5
FS-6 Register 2 (With Counter and Character Comparison)	B6

WIRING DIAGRAM REFERENCE CHART (Continued)

TITLE	7150WD SHEET NO.
FS-7 Register 3 (With Transmitting Distributor and Control)	B7
FS-8 Intercept Control Logic	B8
FS-9 Stop Control Logic FS-10 Line Break Control	B9
FS-11 TSC and Response Encoding Logic FS-12 Polling Step-Switch Control	B10
FS-13 Transmitter Control Logic	B11
FS-14 External Alarm Logic	B12
FS-15 Transmitter Encoder	B13
FS-16 Power Circuits	B14
CPS-1 Flip-Flop	B15
CPS-2 NOR-Gates	B16
CPS-3 NAND-Gates	B17
CPS-4 Exclusive OR Gates CPS-5 Relay Drivers	B18
CPS-6 Gated Oscillator	B19
CPS-7 Bit Oscillator Control CPS-8 Bit Oscillator	B20
CPS-9 Diode Card CPS-10 Voltage Divider Networks	B21
CPS-11 High Current Flasher	B22
CPS-12 Filter	B23
CPS-13 Selector Magnet Driver	B24
App. Fig. 1 App. Fig. 2	C1

WIRING DIAGRAM REFERENCE CHART
(Continued)

TITLE	7150WD SHEET NO.
App. Fig. 3	C1
App. Fig. 4	C2
App. Fig. 5	
App. Fig. 6	
App. Fig. 7	
App. Fig. 8	
App. Fig. 9	
App. Fig. 10	
App. Fig. 11	C3
App. Fig. 12	
App. Fig. 13	
App. Fig. 14	C4
App. Fig. 15	
App. Fig. 16	
App. Fig. 17	
App. Fig. 18	
App. Fig. 19	
App. Fig. 20	C5
App. Fig. 21	
App. Fig. 22	
App. Fig. 23	C6
App. Fig. 24	
App. Fig. 25	C7
App. Fig. 26	
App. Fig. 27	

WIRING DIAGRAM REFERENCE CHART
(Continued)

TITLE	7150WD SHEET NO.
App. Fig. 28	C7
App. Fig. 29	
App. Fig. 30	
App. Fig. 31	
App. Fig. 32	
App. Fig. 33	C8
App. Fig. 34	
App. Fig. 35	
App. Fig. 36	
App. Fig. 37	
App. Fig. 38	
App. Fig. 39	C9
App. Fig. 40	
App. Fig. 41	
App. Fig. 42	
App. Fig. 43	
App. Fig. 44	
App. Fig. 45	
Circuit Notes 101 to 104 Equipment Notes 201, 202, and 203	D1
Information Notes 301 and 302	D2
Information Note 303	D3
Information Note 304	D4
Information Note 305	D5

WIRING DIAGRAM REFERENCE CHART
(Continued)

TITLE	7150WD SHEET NO.
Information Note 306	D6
Information Note 307	D7
Information Note 308	D8
SC-1 Line Controller Sequence Chart	E1
SC-2 Automatic (Tape Transmission) Message Transmission Sequence	E2
SC-3 Keyboard Message Transmission Sequence	E3
Circuit Requirement Tables — Relays	F1
Timing Requirements Table	F2
Wiring — Fuse Panel Assembly	W1
Wiring — Service Assembly	W2
Wiring — Service Assembly — Cont.	W3
Wiring — Control Switch Assembly	W4

WIRING DIAGRAM REFERENCE CHART
(Continued)

TITLE	7150WD SHEET NO.
Wiring — Control Switch Assembly — Cont.	W5
Wiring — Control Switch Assembly — Cont.	W6
Wiring — Control Module	W7
Wiring — Control Module — Cont.	W8
Wiring — Control Module — Cont.	W9
Wiring — Control Module — Cont.	W10
Wiring — Control Module — Cont.	W11
Wiring — Control Module — Cont.	W12
Wiring — Control Module — Cont.	W13
Wiring — Control Module — Cont.	W14
Wiring — Control Module — Cont.	W15
Wiring — Control Module — Cont.	W16
Wiring — Control Module — Cont.	W17
Wiring — Control Module — Cont.	W18