

“DATASPEED*” TAPE-TO-TAPE SYSTEM TYPE 1 AND TYPE 2
TAPE SENDERS AND RECEIVERS ELECTRONIC CIRCUITRY
GENERAL DESCRIPTION AND PRINCIPLES OF OPERATION

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1. INTRODUCTION

1.01 This section presents both a general and detailed description of the electronic circuitry (with the exception of the power supply modules) used in the DATASPEED 1A and 2A Tape Senders and 1B and 2B Tape Receivers. This section was formerly 592-800-101. No TCNs have been issued for or added to this section, since its last issue.

1.02 This section is reissued to add information on unit options for the sender and the send-receive stations.

1.03 The circuit description within this section assumes that the tape sender and/or tape receiver are operated with a 202A or 202C Data Set. Provisions have been made for mounting these data sets directly within the tape sender or tape receiver cabinet.

2. GENERAL DESCRIPTION

TAPE SENDER

2.01 The tape sender converts the parallel output signals generated by the tape reader into a serial start-stop signal for driving the modulator contained in the data set. Refer to block diagram of complete tape sender terminal (Figure 1). The electronic components required to convert the parallel output signals from the reader into serial start-stop form are a transmitting signal converter and a transmitter distributor. The transmitting signal converter and the transmitter distributor are each housed in separate electronic modular assemblies.

TAPE RECEIVER

2.02 The tape receiver converts the start-stop serial code from the data set to a parallel signal which will operate the tape reperformator. Refer to block diagram of complete tape receiver terminal (Figure 1). The electronic components required to convert the

start-stop serial code into parallel form are a receiving signal converter and a receiving distributor. The receiving distributor and the receiving signal converter are each separately housed in electronic modular assemblies.

ELECTRONIC MODULES

2.03 The modules which house the electronics associated with the tape senders and receivers are designed to provide easy access to the circuitry. They are of steel frame construction, and are 5-1/2 inches by 7 inches by 15 inches in dimension.

2.04 The electronic circuitry is contained on plug-in etched circuit cards. Each circuit card is equipped with accessible test points for voltmeter and oscilloscope checking. The modules are equipped with 15-pin connectors to accept each circuit card. Each connector is interconnected by surface wiring. All circuit components are contained on the pluggable circuit cards. All signal connectors and power supply connections are made through a connector mounted on the rear of each module.

POWER AND SIGNAL REQUIREMENTS

A. Power Requirements

2.05 Power required for the above units is obtained from the power supply mounted in the lower enclosure of each terminal (TP177149 multivoltage rectifier). Voltage and current requirements are listed in Table A.

- (a) Ac power — 120 v ac (103-127) 60 Hz
250 watts (nominal max) sender
300 watts (nominal max) receiver

- (b) Dc power (Table A).

B. Output Signal Requirements — Tape Sender

2.06 The tape sender terminal output signal has the following characteristics.

- (a) Start-stop type polar signal.
- (b) Nominal output signal voltage across a load of 1000 ohms.
 - (1) Space: +6 volts
 - (2) Mark: -6 volts

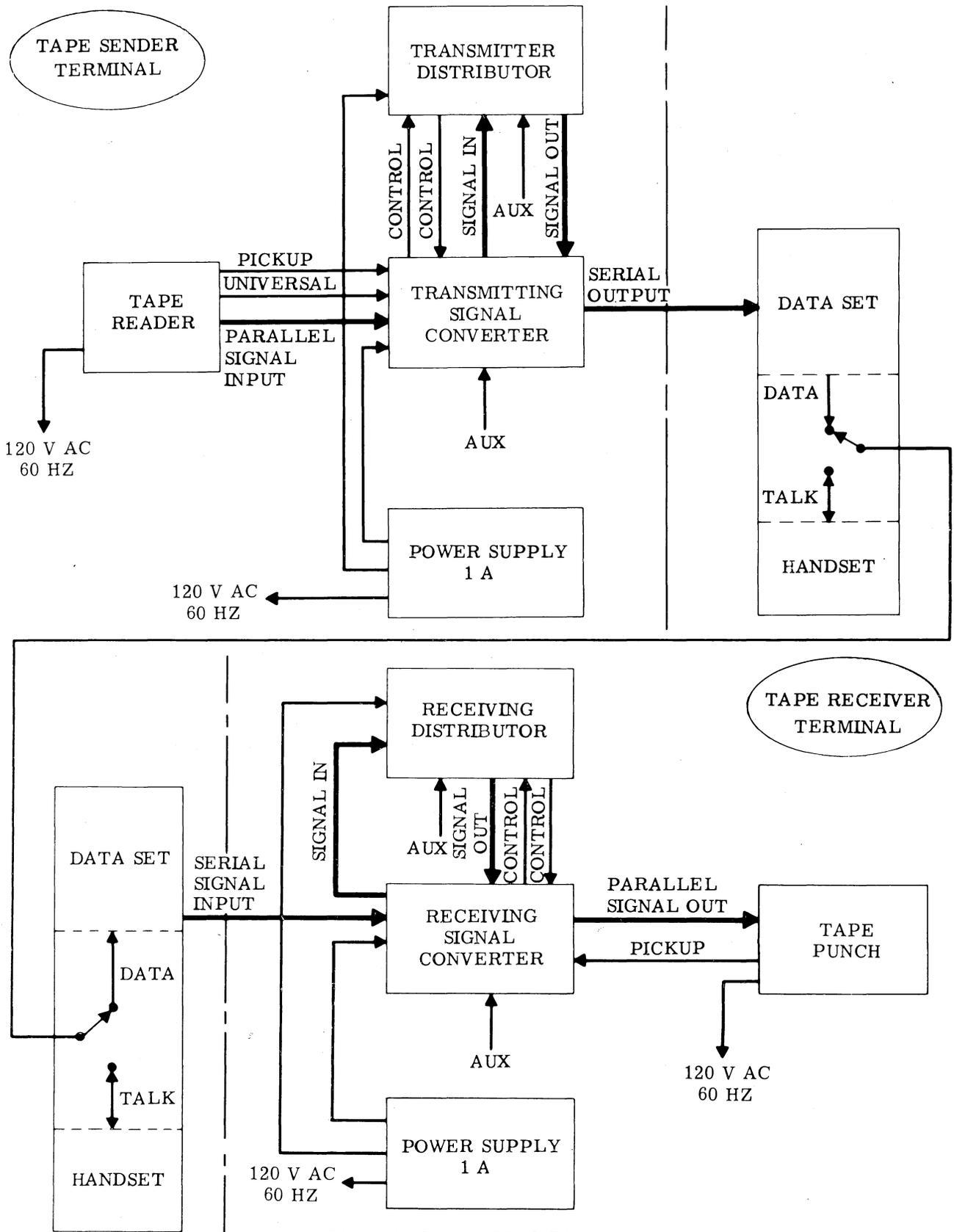


Figure 1 - System Block Diagram

TABLE A
MAXIMUM DC CURRENT DRAIN

Nominal Voltage	Transmitter Distributor (TTD)	Transmitting Signal Converter (TTSC)	Tape Sender Total Drain	Receiving Distributor (TRD)	Receiving Signal Converter (TRSC)	Tape Receiver Total Drain
+6	-	37MA	37MA	-	75MA	75MA
+1.5	131MA	4MA	135MA	130MA	135MA	265MA
-6	-	-	-	-	200MA	200MA
-6R	21MA	6MA	27MA	25MA	30MA	55MA
-12	170MA	51MA	221MA	230MA	240MA	470MA
-28	-	1900MA	1900MA	-	2200MA	2200MA

TABLE B
SIGNAL CHARACTERISTICS

UNIT	TYPE	CODE LEVELS	BAUD	WPM
Transmitter Distributor	1	5	1050	1050
	2	5 to 8	1050	1050
Transmitting Signal Converter	1	5	1050	1050
	2	5 to 8	1050	1050
Tape Reader	1	5	1050	1050
	2	5 to 8	1050	1050
Receiving Distributor	1	5	1050	1050
	2	5 to 8	1050	1050
Receiving Signal Converter	1	5	1050	1050
	2	5 to 8	1050	1050
Tape Reperforator	1	5	1050	1050
	2	5 to 8	1050	1050

(c) Unit codes, code levels, baud (bits per second), and wpm (words per minute) are listed in Table B.

C. Input Signal Requirements — Tape Receiver

2.07 The tape receiver terminal is designed to operate from an input signal with the following characteristics.

(a) Start-stop polar signal.

(b) Nominal input signal voltage from a 1,000-ohm source:

(1) Space: +3 v or more positive (+25 v maximum).

(2) Mark: -3 v or more negative (-25 v maximum).

(c) Unit codes, code levels, baud (bits per second), and wpm (words per minute) are listed in Table B.

3. TAPE SENDER — PRINCIPLES OF OPERATION

GENERAL THEORY

A. Overall Operation

Note: Refer to tape sender terminal block diagram (Figure 2).

General

3.01 Electronic circuitry of tape sender terminal is physically and functionally divided into two parts: a transmitting signal converter and a transmitter distributor. The transmitting signal converter is represented by schematic diagram 3831WD and the transmitter distributor by 4439WD. All circuits are shown in symbolic logic. Each circuit is indicated by an EC number, an etched circuit board number, and a Z number which represents an element number. A detailed description of each circuit board can be obtained by referring to the respective part drawing. For information concerning power supply, refer to Section 582-100-415.

3.02 The function of the transmitting signal converter is to receive multi-level parallel signals from the tape reader, and convert them to an equal number of standard output pulses. Type 1 units utilize 5-level code, while type 2 (universal) units may utilize 5- to 8-level code, depending on operator option. The transmitting signal converter also converts the standard output of a transmitter distributor to signals suitable for driving the modulator of a data set.

3.03 The function of the transmitter distributor is to convert parallel input pulses to a multi-level binary start-stop code. The type 1 distributor contains six register elements and generates a 10-bit (1050 baud) code. The zero (0) level bit (which is the first bit after the start bit signal) is always transmitted as a mark. Bit levels 1 through 5 are used to transmit the serial information. After level 5 has been transmitted, a 3-bit stop pulse will follow where normally levels 6 and 7 along with the unity stop pulse bit are transmitted. The type 2 distributor contains eight register elements, and will accept up to eight information pulses.

If level zero (0) is not used, it will be transmitted as a space pulse. If levels 6 and 7 are not used, each will be transmitted as a mark pulse along with the unity stop pulse.

Operation

3.04 The heart of the circuit operation is the signal register in the transmitter distributor. This group of circuit elements, known as a shift register, is arranged so that each element of the register accepts one code information bit at the same time the respective level in the tape is sensed by the tape reader. This information is accepted in parallel form. Since only one bit can be transmitted at a time, the information is then shifted out of the register, each bit in succession, until all the bits have been transmitted. This occurs during the time the tape is being advanced to the next character. Before the next character is read, the register is reset to accept the new information.

3.05 The basic block diagram (Figure 2) is arranged to illustrate the functions of the various sections of the tape sender terminal. Note that there are two sources of timing in this unit. One timing signal is developed in a magnetic pickup on the tape reader, and is used to initiate the stop pulse for each character. This pulse, then, occurs at the character rate. The other timing signal operates at the bit rate and is used to advance the code in the shift register. This timing signal is generated by the start-stop oscillator (Figure 2). During the stop interval, the start-stop oscillator is stopped, and is then restarted at the beginning of the next start pulse. This assures that the deviation in the bit rate will not be cumulative and that the first code bit will always occur at the proper instant with regard to the machine character rate.

B. Transmitting Signal Converter

3.06 The transmitting signal converter contains signal inhibit gates, pickup pulse amplifier, and output signal amplifier.

3.07 The pickup pulse amplifier shapes and amplifies the magnetic pickup output, and sends it to the signal delay in the transmitter distributor.

3.08 The inhibit gates pass the signal from the reader contacts to the signal register in the transmitter distributor.

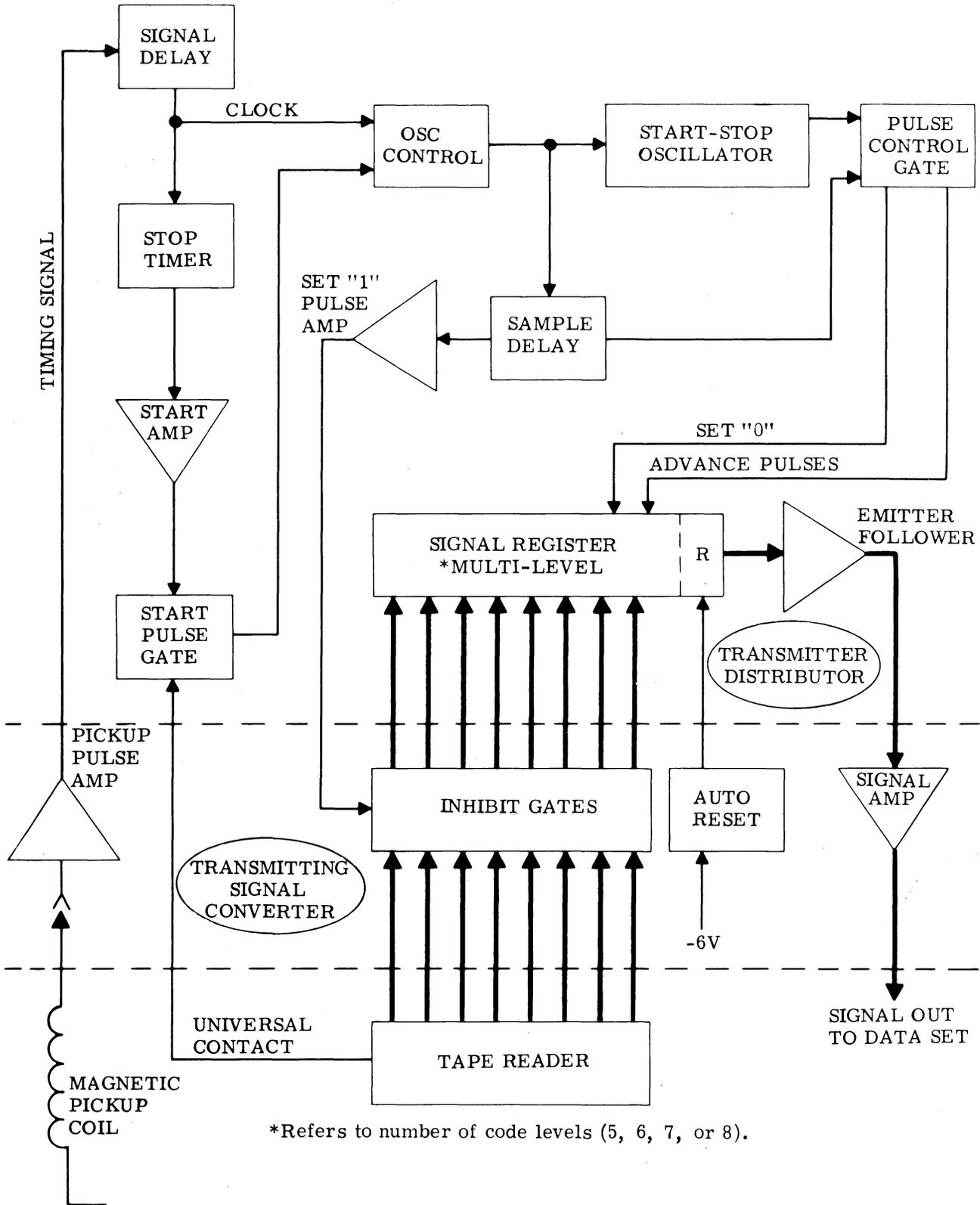


Figure 2 - Tape Sender Block Diagram

3.09 The output amplifier converts the signal from the transmitter distributor to a signal having the characteristics necessary to drive the data set EIA (Electronic Industries Association) polar signal ± 6 volts.

C. Transmitter Distributor

3.10 When the unit is initially turned on, a reset pulse is automatically generated to reset the output element of the signal register. The start-stop oscillator (advance pulse generator) is controlled by a bi-stable circuit called the oscillator control. The stop condition is initiated by the timing signal from the magnetic pickup. The timing signal is applied to the stop timer, a mono-stable device which develops a signal approximately equal in duration to the desired stop pulse. This signal is then applied to the start pulse gate through the start amplifier. If the gate is open, it will pass the trailing edge of the stop pulse (beginning of start) to the oscillator start lead of the oscillator control to provide the start condition. The start pulse gate is under the control of the universal contact in the tape reader. This contact closes for every character position on the tape as it is being pulled through the reader. Thus, if tape is being read, the oscillator will start; but if tape is not being read, the gate will remain closed, the oscillator will not start, and the unit will generate a continuous stop signal.

3.11 The sample delay circuit, which is also triggered at the end of the stop pulse, develops a pulse to control the inhibit gates in the transmitting signal converter, and to control the pulse control gate. This control pulse is delayed approximately one-half a bit, since the signal register must have time to generate a start signal before the new character code is set into it. When this set "1" pulse is applied to the inhibit gates, the information from the reader contacts is supplied through the gates to set the elements of the signal register to record the code. When the contact is closed, it represents a MARK condition (a hole in the tape) and the corresponding shift register element is set to the "1" condition. If it is SPACE (no hole in tape) the register element remains in the "0" condition. When the sample delay is applied to the pulse control gate, it enables the set "0" side, providing a set "0" pulse for the signal registers, and inhibits the "advance pulses" side to prevent a false signal from being sent on the line. Upon relaxing, the set "0" is inhibited and the "advance pulse" side is enabled so information can be shifted through the register.

3.12 The last element of the signal register (labeled R on the block diagram, Figure 2) does not receive a code pulse. At the end of the previous character, this element was left in the "1" condition as will be shown below. When the set "0" pulse arrives, element R will be shifted to the "0" condition, causing a space to be generated representing the start pulse. Immediately following this, the information is set into the register. The next advance pulse shifts this entire code one element to the right, bringing the first bit of the code from element 1 to element R. This produces an output signal corresponding to the first bit. With the next advance pulse, the code is advanced another position to the right so that now the second bit is in element R, producing an output signal which represents that bit. This action continues until all bits have been advanced out of the register, each bit producing its output signal in turn.

3.13 Element R is continuously primed in such a way that it will be shifted to the "1" state by the first advance pulse following reset, and will remain that way until the next set "0" pulse. This condition is transferred down the shift register, causing each element to go to the "1" state as the last code bit is shifted out of it. Thus, the stop pulse is generated in element R when the last bit is shifted out of it, since it will be set to the "1" state. It will remain in this state until the next set "0" pulse causes it to shift to SPACE to create the start pulse of the next character. If no code is to be transmitted, due to no tape in the reader or the reader having been stopped, advance pulses would not be generated since no start pulse would be received by the oscillator control (universal contact open). Thus, element R would remain in the "1" state generating a continuous mark or stop signal until the code transmission is resumed.

DETAILED CIRCUIT DESCRIPTION

A. Transmitting Signal Converter

Note: Refer to schematic wiring diagram 3831WD.

Initial Conditions

3.14 The first action which takes place in the transmitting signal converter is automatic reset. This occurs when the power switch is turned on. At this time -6 volts is applied to terminal H of the Z210 integrator pulse shaper. This circuit, after a delay of about 300 milliseconds, provides a negative-going pulse

on terminal K. The pulse is applied to the input terminal D of Z211B pulse amplifier circuit. The pulse amplifier produces a positive-going -6 volt to 0 volt pulse and sends it to terminal C6 of connector J201. From terminal C6, the signal is sent to the reset of the output element of the signal register.

3.15 The timing signal from the magnetic pickup of the reader is applied to terminal C1 of connector J201 and from there to terminal A of Z209A. The lead on terminal B1 of J201 applies a -6 volt bias to the pickup coil and pickup amplifier. The timing signal leaves terminal L of the pickup amplifier, and is inverted by Z209B. The output of Z209B is sent to the transmitter distributor through terminal C2 of connector J201.

Reader Input

3.16 The tape reader mark contacts are connected to Z201A-E through Z202A-D integrators. The integrators are used to clean up any noise which may be caused by the mechanical switching of the tape reader contacts. The outputs of the integrators are applied to the prime input of Z203 through Z206 inhibit gates, and a sample pulse is sent from the transmitter distributor via connector J101, terminal F2, to the drive side of the inhibit gates. At this time, all inhibit gates which are primed by the integrators pass a positive-going -6 volt to 0 volt pulse to Z207A-D through Z208A-D OR gates, and from them via J201 to the transmitter distributor. The function of the OR gate is described in 3.35.

Universal Input

3.17 The universal signal from the reader is applied to terminal E of Z202D integrator, through connector J201, terminal H9. The output, terminal P of Z202D, appears on terminal C4 of J201. Subsequently, this signal is applied to the transmitter distributor.

Polar Signal Output

3.18 The parallel input signal is transferred from the transmitting signal converter to the transmitter distributor, and the serial output signal from the distributor is applied to the data set. It is necessary, therefore, to convert the dc neutral signal from the transmitter distributor to a polar signal capable of driving the data set. This signal conversion is accomplished by a Z212A amplifier. The signal from the transmitter distributor is applied to terminal C10, connector

J201; from there it goes to terminal B of Z211A inverter. The signal output of the inverter is applied to terminal F of Z212A output amplifier, which converts the signal to a +6 volts and -6 volts polar signal. The output of the amplifier, terminal P, is sent to the data set through terminal D10, connector J201.

Request-to-Send

3.19 The data set requires a signal to inform it that the transmitter distributor is ready to send. This signal is called the request-to-send. On high speed tape-to-tape system senders without discrete calling, the data set request-to-send lead is permanently biased on with +17.5 volts.

Power Requirements

3.20 Power is applied through connector J201 to the module from the dc power supply. Minus 6 volts is found on terminal A4, +1.5 volts on terminal B8, -12 volts on terminal B7, and +6 volts on terminal B3. From these points the voltages are passed through Z213A-B through Z214A-B filter elements, which filter out extraneous noise. Terminal B4 has -28 volts; terminal B6 is circuit ground and terminal B5 is frame ground.

B. Transmitter Distributor

Note: Refer to schematic wiring diagram 4439WD and timing diagram (Figure 3).

Initial Conditions

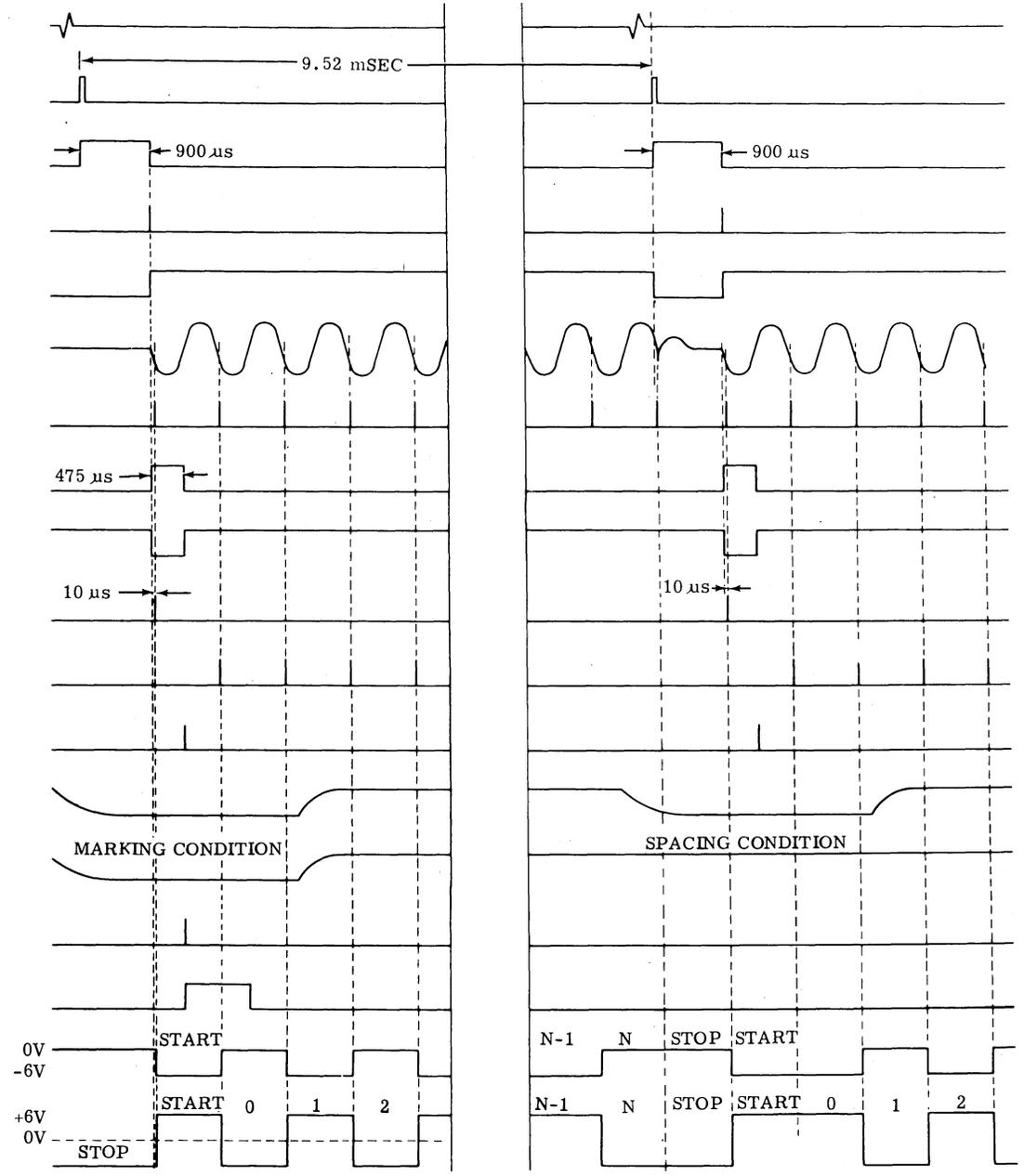
3.21 The first action to occur in the transmitter distributor is automatic reset. When the power switch is put in the ON position, a -6 volt to 0 volt pulse is generated in the transmitting signal converter (3.14) and applied to terminal C6, connector J101. This pulse is presented to the set "1A" input of Z110 output element, terminal C, in the signal register switching the normal output, terminal L, to 0 volt. This places a stop signal on the line, keeping it closed.

Clock Pulse

3.22 While the reader motor is running, a clock pulse, shaped in the transmitting signal converter, is applied through terminal C2, connector J101, to the signal delay input. The signal delay output, which is identical to its input only delayed about 50 microseconds, is applied to

Figure 3 - Tape Sender Timing Diagram

MAGNETIC PICKUP OUTPUT
 CLOCK PULSES (Delayed 50 Microseconds)
 STOP TIMER
 START AMP
 OSCILLATOR CONTROL
 START-STOP OSCILLATOR (0.952 mSEC Each)
 SQUARING AMP
 SAMPLE DELAY (Normal Output)
 SAMPLE DELAY (Inverted Output)
 SIGNAL REGISTER SET "0"
 ADVANCE PULSES
 SAMPLE
 UNIVERSAL CONTACT SIGNAL
 CONTACT SIGNAL, CODE LEVEL NO. 2
 SAMPLE GATE NO. 2, SET "1" PULSE
 SIGNAL REGISTER LEVEL NO. 2 (Normal Output)
 TTD OUTPUT
 SPACE
 MARK
 SIGNAL OUTPUT (Figure 6, Note)



the stop timers set "1" input and the oscillator controls set "0A" input. The clock pulse applied to terminal D of Z104 oscillator control, switches the normal output, terminal L, to -6 volts to turn off the Z108 start-stop oscillator. The clock pulse is also applied to the set "1" input of Z101 stop timer, terminal C, causing the output, terminal L, to go from -6 volts to 0 volt and remain at that potential for a period of time a little less than a bit in length.

Stop Timer

3.23 When the Z101 one-shot times out, its normal output will relax and produce a negative transition from 0 to -6 volts. This negative transition is applied to terminal B of Z102A start amplifier, a pulse amplifier, which generates a positive-going -6 volt to 0 volt pulse on its output, terminal K.

Oscillator Control

3.24 The positive pulse from Z102A is applied to Z103B inhibit gate, terminal N. If there is no tape in the reader, the universal contact will be open and zero volt appears on terminal D of Z103B inhibit gate. If a tape is in the sensing head and the reader is operating, the universal contact is closed and a -6 volts or greater signal is sent from the transmitting signal converter to connector J101, terminal C4, and from there to terminal D of the inhibit gate. The presence of this signal on terminal D permits the positive signal applied on terminal N to pass through the inhibit gate and on to the oscillator control flip-flop.

3.25 The Z104 oscillator control flip-flop receives the positive-going pulse on terminal C. The pulse causes the circuit to switch and the normal output, terminal L, goes to 0 volt. This signal is now applied to the Z105 sample delay circuit and the Z108 start-stop oscillator.

Sample Delay

3.26 The positive-going signal from the Z104 oscillator control is received on the set "1" input, terminal C, of the Z105 sample delay. This one-shot serves two functions.

- (a) It provides the initial signal for the sample lead.
- (b) It provides one pulse for the signal register reset. The sample delay one-shot goes negative on its inverted output,

terminal K, and positive on its normal output, terminal L. The negative transition primes the set "0" side of the Z106A pulse control gate, terminal B and permits the first pulse from the squaring amplifier to pass through this gate to set "0" all the signal registers (Z110 through Z115, Z116, Z117, or Z118 depending on number of levels). When the Z105 sample delay one-shot relaxes, its inverted output goes to 0 volt and removes the prime from the set "0" side of the Z106A pulse control gate. Simultaneously, the normal output of Z105 goes to -6 volts and primes the advance pulse side of Z106B pulse control gate, terminal D, allowing pulses from the squaring amplifier to pass through. The negative transition from the normal output is also sent to the input of the set "1" Z102B amplifier, terminal D.

Start-Stop Oscillator

3.27 The Z108 start-stop oscillator receives a -6 volt to 0 volt signal from the oscillator control flip-flop (3.25). The oscillator begins to oscillate as soon as the 0 volt signal is applied to its input terminal. The output appears as sinusoidal oscillations on terminal A, and is sent to the input of the Z109 squaring amplifier, terminal H. The squaring amplifier shapes the sine-wave in such a way as to produce a positive-going -6 volt to 0 volt transition every cycle. Thus, one pulse is produced in every period of the sine-wave cycle. The time interval between the clock pulses and the frequency of the start-stop oscillator will permit only N+2 pulses on terminal A of Z109.

Squaring Amplifier

3.28 The pulses from the squaring amplifier are applied to Z106A and Z106B pulse control gates on terminal A and terminal N, respectively. The sample delay one-shot primes terminal B of the pulse control gate long enough to permit the first pulse from the squaring amplifier to pass through to terminal K. This positive-going pulse is applied to the set "0A" input, terminal D, of the signal register, and resets all the registers to the set "0" condition prior to their receiving information from the transmitting signal converter.

Pulse Control Gate

3.29 The positive signal from the sample delay closes the advance pulses side of the Z106B pulse control gate, terminal D, long

enough to prevent the first pulse from the squaring amplifier from passing through the gate. The remaining pulses are passed through the gates output, terminal L, and on to the set "1B" and set "0B" inputs on all the signal registers and the output element (terminals E and F, Z110 through Z118).

3.30 The negative-going signal which occurs when the Z105 sample delay one-shot relaxes, appears on terminal L. This signal is applied to terminal D of Z102B pulse amplifier, which generates a positive-going pulse, -6 volts to 0 volt, on its output at terminal L. The pulse is sent to terminal B of Z103A emitter follower. The output of Z103A is wired to connector J101, terminal C3, and is designated as the sample lead. The positive-going pulse on the sample lead is sent to the transmitting signal converter to trigger the inhibit gates passing the reader information into the signal register elements (3.16).

Sample Pulse

3.31 When the sample pulse is sent from the set "1" Z102B and Z103A amplifiers in the transmitter distributor to the inhibit gates in the transmitting signal converter, any inhibit gate which has a MARK condition on its input (-6 volts on terminal B or D) will pass a positive-going pulse to the transmitter distributor via connector J101, terminals D2 through D9, and from there to the storage registers set "1A" input, terminal C or Z111 through Z115, Z116, Z117, or Z118 (depending on number of code levels). Thus, if a MARK condition appears in the reader, the corresponding signal register flip-flop switches to a set "1" condition (terminal L of flip-flops at 0 volt).

Signal Register

3.32 For purposes of description, assume that a MARK input is appearing only in the 4th level. Thus, only Z114 flip-flop will go into the set "1" condition; in this condition, its normal output, terminal L, will be at 0 volt and its inverted output, terminal K, will be at -6 volts. The normal output is wired to the prime "1B" input of the 3rd level Z113 flip-flop, terminal J, and the inverted output is wired to the prime "0B" input of Z113, terminal H. In this particular example, the 3rd level flip-flop will have its prime "1B" input primed, and when the 1st advance pulse arrives at the set "1B" input, terminal E, this flip-flop switches from the set "0" state to the set "1" state.

3.33 When the MARK pulse is passed from the 4th level to the 3rd level (that is, from Z114 to Z113), the 2nd level prime "1B" terminal is primed and the prime "0B" terminal remains at -6 volts. Thus, when the second advance pulse arrives at terminals E and F of Z112, and as each advance pulse comes in, this MARK signal is passed from the 3rd element to the 2nd element and so on until the advance pulse for the stop pulse arrives. At this time the MARK signal is transferred into the output element of the register and then to the data set. The Z107 emitter follower passes the output signal from element Z110 to terminal C10 of connector J101.

C. Auxiliary Connections

3.34 All auxiliary connections, needed to operate in conjunction with supplementary equipment, are available at connector J202 of the transmitting signal converter.

3.35 Additional levels 0 through 7 are available (terminals F3, F4, F5, F6, F7, F8, F9, and G2) to permit insertion of additional characters in the signal registers through OR gates (Z207A to D through Z208A to D).

3.36 The sample lead is connected to terminal F2 of connector J201, and is used to let the auxiliary equipment know that the information has been passed into the signal registers.

3.37 Terminals G3, G4, and G5 on J201 in the transmitting signal converter are used to provide -28 volts, signal ground, and frame ground connections.

3.38 A start lead is connected to terminal C5, J101 in the transmitter distributor. This lead is wired to the output of Z102A start amplifier, terminal K, and will permit the auxiliary equipment to use the clock pulse as described in 3.15.

3.39 The oscillator control is connected to terminal C1 of connector J101 in the transmitter distributor. This lead is wired to the set "1B" input of the Z104 oscillator control flip-flop, terminal E. It provides a means for equipment to turn on the oscillator.

4. TAPE RECEIVER — PRINCIPLES OF OPERATION

GENERAL THEORY

A. Overall Operation

Note: Refer to tape receiver terminal block diagram (Figure 4).

General

4.01 The electronic circuitry of the tape receiver terminal is physically and functionally divided into two parts: a receiving signal converter and a receiving distributor. The receiving signal converter is shown on the schematic wiring diagram 3833WD, and the receiving distributor by 4441WD. Each circuit is indicated by an EC (etched circuit card) number and a Z number which represents an element number. A detailed description of each circuit is given on the respective etched circuit card drawing. For information concerning the power supply, refer to Section 582-100-415.

4.02 The function of the receiving distributor is to separate the multi-level serial input telegraph code into a parallel binary output signal with the same number of code levels. The function of the receiving signal converter is to provide buffer storage and change the parallel binary signals into a driving signal for the tape reperfocator. Type 1 units utilize 5-level code, while type 2 (universal) units may utilize 5- to 8-level code at the operators option.

Operation

4.03 Like the tape sender terminal (3.04), the operation of the receiving terminal centers around the signal register. In the receiving terminal, however, the code is advanced into the register as it arrives, and then is shifted out of each element simultaneously to a storage register as shown in the block diagram (Figure 4). The code remains in the storage register until the punch is ready to operate, and is then transferred into magnet pulsers which cause the proper punch position to be energized.

4.04 The operation of this system depends upon synchronizing the punch at the receiving terminal with the tape reader at the sender terminal. To assure that a new character always has a position available on the tape, the tape punch runs slightly faster than the tape reader.

4.05 The major control function in the receiving distributor is accomplished by the control register. The output lead of the control register has been labeled control bus to show its importance in the operation of this equipment (Figure 4). The control register is responsible for the following:

- (a) Starting and stopping the sensing operation of the receiving signal register.
- (b) Shifting the code from the signal register to storage in the receiving signal converter.
- (c) Priming the storage register to allow transfer of the code to the magnet pulsers.

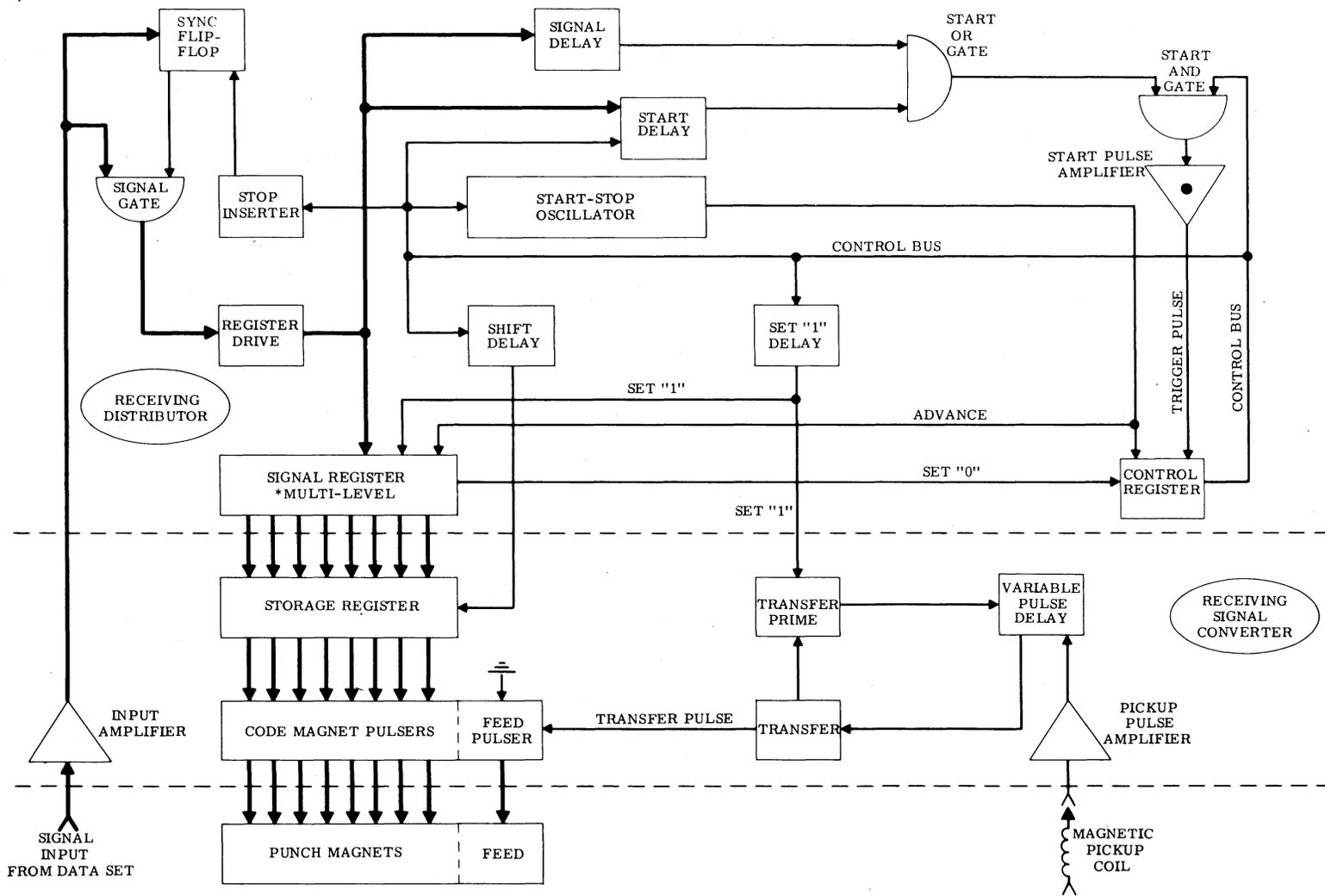
4.06 The basic operation of the receiving distributor and the receiving signal converter can be understood by following the sequence of events which occurs as a code group for a character arrives. The following conditions exist prior to receiving the character.

- (a) Signal register: Set "1"
- (b) Advance pulse generator: Off
- (c) Control register: Set "0"
- (d) Signal gate: Open
- (e) Transfer prime: Set "1"
- (f) Storage register: Storing last character
- (g) Input gate: Open
- (h) Start OR gate: Closed
- (i) Start AND gate: Open

4.07 Two distinct timing operations occur in the receiver terminal. These are related to the basic operating actions (ie, code punching and code registering), and occur throughout the same interval.

B. Receiving Signal Converter

4.08 The first operation to be considered is the punching process. Following the reception of the last complete character (4.06), shows that the character is stored in the storage register. A timing pulse generated in the magnetic pickup on the punch is converted to a pulse by



*Refers to number of code levels (5, 6, 7, or 8).

Figure 4 - Tape Receiver Block Diagram

the pickup pulse amplifier and presented to the variable delay circuit. The variable delay acts like a one-shot whose delay time changes as a function of the transfer primes condition. Since the transfer one-shot is primed by the transfer prime, the trigger pulse will be passed through the transfer pulse generator to operate the magnet pulsers. The magnet pulsers are so arranged that the feed magnet is energized together with the code magnets that are primed from the code in the storage register. Thus, holes are punched in the tape representing the code stored in the storage register.

4.09 The punching operation must take place within the character interval following the shifting of code into the storage register. Thus, the punch period must be less than this time (about 95 to 98 percent of the character interval).

C. Receiving Distributor

4.10 During the punching operation waiting period, a new code group may be forming in the signal register. This action, code registering, will be considered next. An input signal applied to the signal gate, finding the gate open, passes through this gate and actuates the register drive circuit. The register drive circuit reshapes the input signal so that the transitions between bits display the rapid rise time desired, and corrects for some of the deterioration of the signal that may have occurred along the line. The output of the register drive is applied to the signal register, where it is advanced into the register one bit at a time under the control of the advance pulses.

4.11 The start-stop oscillator is turned off between code groups and must, therefore, be turned on again before the signal can be registered. The start-stop oscillator determines the bit rate. Since this is one of the circuits controlled by the control register, the control register must be in the "1" state in order to get the start-stop oscillator started. The incoming code group, after being shaped in the register drive, is applied to one of the inputs on the now open input gate. The first element (bit) of this code group is the start pulse, which triggers the start delay circuit after it passed through the input gate. The signal developed is equal to approximately one-half bit in length, and is used to delay the sampling of each bit until about its midpoint. This position was selected as being the most reliable under poor transmission conditions.

4.12 The output of the start delay is applied to the start OR gate which was opened when the start pulse passed through the signal delay circuit. This delay is provided to aid in the prevention of false starts, since only pulses of long duration will pass through it. Thus, short noise pulses ("hits") on the line will not be applied to the start gate, and this gate will not open to a false start. When a true start pulse is applied through the delay to the start gate, the gate will open and the pulse from the start delay circuit will pass through the start gate. The trailing edge of this pulse is formed into a trigger pulse in the start pulse amplifier, and applied to the control register.

4.13 Upon receipt of the trigger pulse, the control register shifts to its "1" state and causes the following actions.

- (a) Start-stop oscillator starts.
- (b) Start AND gate closes.
- (c) Prime is removed from start delay.

The first advance pulse is generated about 50 microseconds after the start-stop oscillator is turned on, and causes the start pulse to register in the first element of the signal register. Since this is a space, it causes this element to return to the "0" state. (All signal register elements were set to the "1" state before the code arrived.)

4.14 The closing of the start AND gate and removal of the prime from the start delay prevents any further transitions in the code input from feeding through to the control register and causing it to operate too soon.

4.15 All the register elements will receive a shift pulse, but no shift takes place since all but the first (Nth) element in the signal register are in the "1" state and the prime is in the "1" state.

4.16 About the middle of the first code bit, the second advance pulse occurs causing the "0" condition of the Nth element to advance to element N-1, and the code bit to be registered in the Nth element. With the arrival of the next advance pulse, the "0" condition in element N-1 moves to element N-2; the state of element N moves to element N-1, and the new code bit is registered in the Nth element. This continues as each advance pulse arrives until, with the N-1 code bit, the start pulse, registered as state "0", will have advanced to element 1, and

the N registered bits will be recorded in elements 2 through N. The next advance pulse moves all code bits and the start pulse one position to the right, advancing the start pulse into the control register and registering the last code bit in element N. The control register, upon receipt of the start pulse, shifts from the "1" state to the "0" state, causing the following actions.

- (a) Start-stop oscillator stops.
- (b) Stop inserter develops signal, priming synchronizer flip-flop.
- (c) Synchronizer flip-flop triggers, closing signal gate.
- (d) Start delay is primed.
- (e) Start AND gate opens.
- (f) The 100-microsecond shift delay circuit is triggered.
- (g) The 200-microsecond set "1" delay circuit is triggered.

4.17 With the signal gate closed, no further transitions on the line will affect the operation of the receiver until the stop inserter acts to open the signal gate. After an elapse of 100 microseconds, the signal applied to the shift delay circuit emerges and causes each element of the storage register to shift to the same state as its corresponding element in the signal register. Thus, the information is cleared from the signal register and stored in the storage register. There, 200 microseconds after the last advance pulse, the set "1" pulse emerges from the set "1" delay circuit. This pulse is used to reset the signal register to its "1" condition, and the transfer prime to its "1" condition. The signal register is now prepared to accept a new code.

4.18 The transfer prime circuit, together with the variable delay, determines the amount of time the transfer pulse is delayed from the pickup pulse. This delay is necessary to prevent loss of a character due to the jitter of the incoming signal.

4.19 The synchronizer flip-flop, which is triggered by the stop inserter, keeps the signal gate closed during the stop time. The gate then opens, and is ready to accept a start signal at any time after this. With the next start pulse, the cycle will begin over again, and the same sequence of operation will be repeated to register and punch the next code character.

DETAILED CIRCUIT DESCRIPTION

A. Receiving Signal Converter

Note: Refer to schematic wiring diagram 3833WD.

Initial Conditions

4.20 Initially, when the power switch is turned ON, -6 volts is applied to terminal H of Z405 integrator pulse shaper. After a delay of about 100 to 300 milliseconds, Z405 provides a negative going transition on its output, terminal K. This signal is applied to the input of Z408B pulse amplifier, terminal D, which produces a positive-going pulse, -6 volts to 0 volt, on its output, terminal L. This positive pulse is sent to terminal E4 of connector J401, and from there to the receiving distributor to reset the control register (4.37).

Storage Register

4.21 The normal and inverted sides of the signal register in the receiving distributor are applied through connector J401 to the prime "1B" and prime "0B" inputs of the signal converter storage register elements, terminals E and F of Z411 through Z418. Thus, if a particular bit is a MARK in a signal register element, that element will be in the set "1" condition and its normal output will prime the "1B" input of the corresponding flip-flop in the storage register. When the shift pulse from the receiving distributor, which comes in on terminal C1 of connector J401, is applied to the set "1B" input of this storage register element, it switches to the set "1" condition. If a SPACE condition exists in a signal register element, the corresponding storage register element will shift to the set "0" condition when the shift pulse comes in on its set "0B" lead, terminal F of Z411, Z412, or Z413 through Z418, depending on the number of code levels used.

4.22 If any of the elements in the storage register are in the set "1" condition, this provides a prime for their respective magnet pulsers on terminal E. A transfer pulse on the input of the magnet pulser, terminal B, will cause the primed magnet pulsers to fire and remain on for a period of approximately 4.5 milliseconds. The output of this card, terminal A, Z419 through Z427, is applied to the punch magnets. When triggered, the output of the magnet pulser, terminal A, switches from -28 volts to ground.

Transfer Circuitry

4.23 One hundred (100) microseconds after the information is passed from the signal register into the storage register, a transfer prime pulse from the set "1" delay appears at terminal B1 of connector J401. This pulse is sent to the set "1A" input of the transfer prime flip-flop, terminal C of Z403, causing this flip-flop to switch to the set "1" condition. The normal output, terminal L, goes to 0 volt and is sent to the prime "1" input of Z407 transfer one-shot. The inverted side of the transfer flip-flop, terminal K, goes to -6 volts and is applied to the bias input of the variable pulse delay circuit, terminal A of Z406. The pickup pulse is received from the punch on terminal D1 of connector J402 and is sent to Z404A pickup amplifier, terminal A. The output of the pickup amplifier, terminal L, is applied to the input of Z404B pickup inverter circuit, terminal F. The output of Z404B produces a positive-going pulse (-6 volts to 0 volt) which is applied to the set "1" input of the variable pulse delay, terminal C.

4.24 The variable pulse delay circuit now acts like a one-shot triggered by the output of the pickup inverter; however, the time duration of the variable pulse delay circuit depends on the amount of time the bias signal exists on terminal A of Z406, and the pickup pulse is applied to the set "1" input, terminal C. Thus, after a period of time, the variable pulse delay relaxes and produces a positive-going pulse on its inverted output, terminal K. This output is applied to terminal C of Z407, the transfer one-shot, causing it to fire. The time-out of the pulse delay varies between 0.4 to 1.2 milliseconds.

4.25 A positive transition occurs initially on the normal output of Z407, terminal L, and is applied to the set "0A" input of the transfer prime flip-flop, terminal D of Z403, switching it to the set "0" condition. A negative transition occurs on the normal output of the transfer one-shot 100 microseconds after the receipt of a pulse from the variable pulse delay, and is applied to the input of Z408A pulse amplifier, terminal B. See 4.28 through 4.34 for a detailed description of the variable pulse delay circuit, and 4.35 through 4.36 for a detailed description of the transfer circuitry timing.

Magnet Pulsers

4.26 The pulse amplifier produces a positive-going pulse, -6 volts to 0 volt, and applies it to the input of Z402B inhibit gate,

terminal N. The pulse is passed through the gate and is applied to the input of Z409 emitter follower, terminal B. The output of Z409 is applied to terminal B of Z419 through Z427 magnet pulsers, causing all the magnet pulsers primed by the set "1" condition of the storage registers to fire. Since the Z419 feed magnet pulser is continuously primed (ground on terminal E), it always fires upon the receipt of a transfer pulse. The firing of the magnet pulsers provides a ground path for the corresponding magnets in the punch, which causes the magnets to energize, punching the stored information into the tape.

Incoming Signal

4.27 The incoming signal from the data set is received on terminal D10 of connector J401 in polar form. This input is converted to a -6 volt to 0 volt signal by passing it through the Z401 receiver input amplifier. The output of Z401 appears at terminal C10 of connector J401. From here, the signal is applied to the signal input of the receiving distributor.

B. Variable Pulse Delay Circuit

General

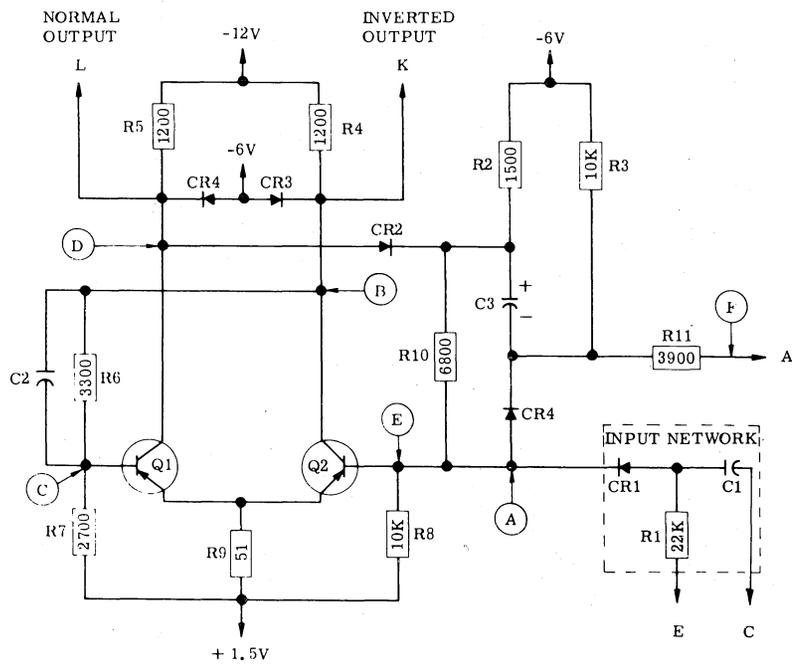
4.28 The variable delay is used in the tape receiver terminal for two reasons. First, to develop a proper time relationship between the pickup and the transfer prime, and second, to generate a transfer pulse for the magnet pulsers. The reader, at the tape sender terminal, has inherent mechanical jitter which appears on the signal, causing the start pulse to occur at slightly different times each cycle. At a critical time in the punching operation, this jitter could possibly cause the loss of a whole character. The variable delay circuit prevents this from occurring.

4.29 The variable delay circuit is a stable-state device which may be switched to a semistable condition. It will remain in its semistable state for a length of time determined by a bias prime which acts to effect the time-out of the circuit (Figure 5 (A)). Its element number is Z406 (EC351), and it is used in the receiving signal converter (3833WD).

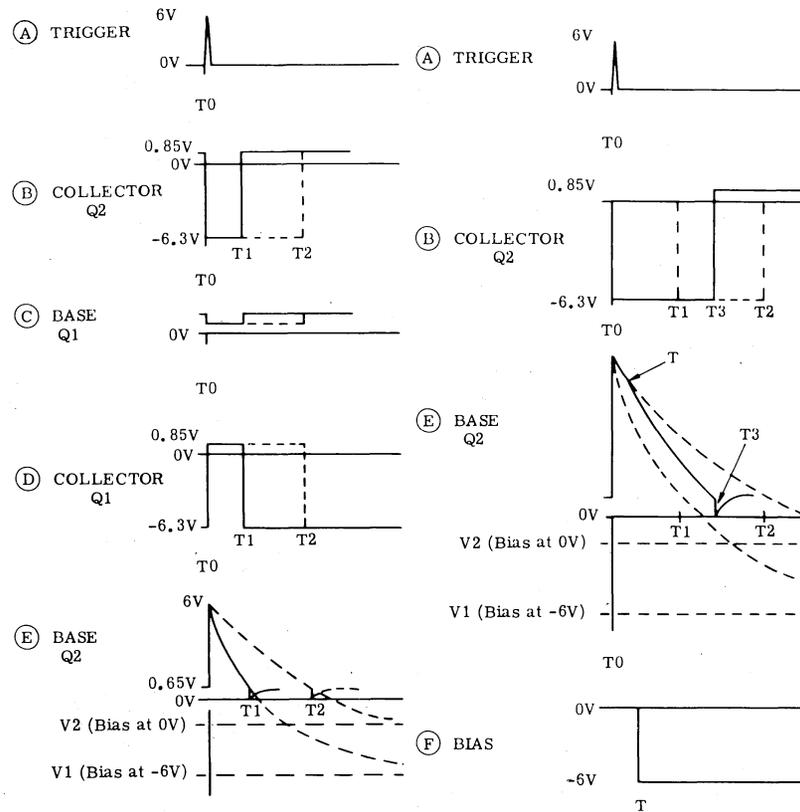
Operation — Fixed Bias Prime

4.30 Stable State: In the normal stable-state condition of the circuit, Q2 is forward biased and Q1 is reverse biased. Q2 is forward biased by virtue of the -6 volt potential on its

Figure 5 - Variable Pulse Delay



(A) Variable Pulse Delay Circuit



(B) Variable Delay Waveforms, Fixed Bias Condition

(C) Variable Delay Waveforms, Variable Bias Condition

base through R10 and R2. Its collector potential, about 0.85 volt, holds Q1 in the OFF condition. The 0.85 volt potential at the collector of Q2 is derived from the emitter side of R9 and, therefore, also appears at the emitter of Q1.

4.31 Triggering:

Note: Waveforms in Figure 5 (B) are associated with those encircled in Figure 5 (A).

A positive-going square wave applied at input C of the differentiator network produces a positive pulse at point A. This pulse reverse biases Q2, turning it OFF. The collector of Q2 drops to -6 volts (point B), clamped at that potential by CR3. The negative transition is coupled to the base of Q1 (point C) forward biasing that transistor. When Q2 conducts, its collector voltage rises to 0.85 volt (point D) from its -6 volt clamp level. The base of Q2 now swings positive at point E, due to the previously changed condition of C3 (plus to minus) (Figure 5 (A)). Capacitor C3 immediately begins to discharge toward the voltage level V1 or V2, depending on the prime voltage level at the bias input A. Levels V1 and V2 are established by the voltage divider action of R11 and R3. The rate of discharge of C3 is determined by R11, R3, and R2.

4.32 Time-Out: Assuming a -6 volt bias input, C3 begins to discharge toward that level. The time the circuit remains in this semistable state is determined by the time required for C3 to discharge to a level which allows Q2 to turn ON. The discharge of C3 follows the exponential decay shown for point E until a level more negative than about 1 volt is reached at t1. When this point is reached, Q2 turns ON and Q1 turns OFF. Capacitor C3 recharges to its 6 volt potential during the stable-state condition. Diode CR2 is reverse biased while C3 charges, preventing any distortion of the Q1 collector waveform. If the bias input voltage level had been 0 volt instead of -6 volts, it would have taken C3 a longer time (t2) to discharge to the level where Q2 turned ON, resulting in a longer time-out for the circuit.

Operation — Variable Bias Prime

4.33 General: The fixed bias prime operation considers the cases when the bias is fixed at either -6 volts (V1) or 0 volt (V2) throughout a complete operating cycle. This, however, is not the normal operating condition of the circuit. Normally, the bias input will switch

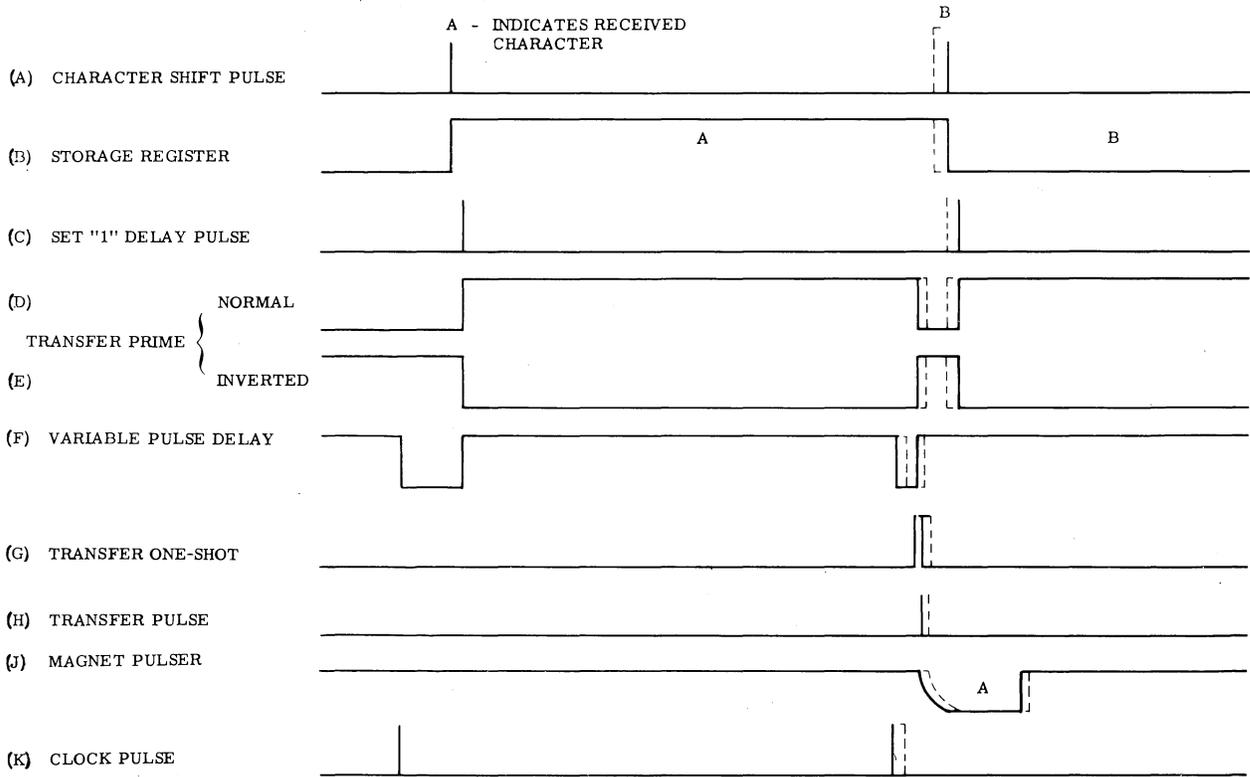
from 0 volt to -6 volts somewhere between times t1 and t2. This will cause the circuit to operate in its semistable state for a period of time (t3) occurring between t1 and t2.

4.34 Operation: Waveforms in Figure 5 (C) are associated with those encircled in Figure 5 (A). During normal operation, the bias prime switches from 0 volt to -6 volts between t1 and t2. When the trigger pulse at point A switches Q2 OFF; C3 discharges toward the 0 volt bias prime level (V2). At some time, t, the bias prime level switches to -6 volts (V1), causing C3 to change its discharge rate. The voltage at the base of Q2 now reaches the forward bias level (about 1 volt) at time t3 — before t2, but after t1. Transistor Q2, therefore switches ON at this time. Times t1 and t2 (Figure 5 (C)) indicate the time durations for C3 to discharge to about 1 volt if the bias had been fixed at either -6 volts or 0 volt.

C. Transfer Circuitry Timing

4.35 Refer to timing diagram (Figure 6) of the transfer circuitry during the critical time after a character has been inhibited and remains in storage until the next cycle. A shift pulse (A) transfers the information from the signal register to the storage register. After 100 microseconds, the shift occurs; the set "1" delay pulse (C) sets the Z403 transfer prime flip-flop to the set "1" condition (normal output, (D) goes positive). The clock pulse (K), which triggers the Z406 variable pulse delay circuit (F), has come in and the variable pulse delay begins its time out. The inverted output (E), of the transfer prime flip-flop provides bias for the variable pulse delay circuit. Since the transfer prime is in the set "0" condition, the variable pulse delay circuit times out to its longest pulse width. The normal output of the transfer prime flip-flop primes Z407 transfer one-shot (G), and the positive transition of the variable pulse delay triggers the one-shot. The first character, A, has been shifted, the variable pulse delay has timed out, and the transfer prime flip-flop is still in the set "0" condition (normal output at -6 volts) (Figure 6). Thus, the transfer prime one-shot will not be triggered, a transfer pulse (H), will not be generated, and character A will not be punched. The character will remain in storage until the next punch cycle. The set "1" delay pulse comes in and the transfer prime flip-flop goes to the set "1" condition.

4.36 When the next clock pulse comes in, the Z406 variable pulse delay circuit times out to its shortest pulse width and triggers



Note: Bit Width

BAUD	OSCILLATOR FREQUENCY	BIT WIDTH MILLISECONDS
600	600 Hz	1.66
750	750 Hz	1.33
900	900 Hz	1.11
1050	1050 Hz	0.95

Figure 6 - Transfer Circuitry Timing Diagram (One Cycle of Operation)

the Z407 transfer one-shot. The positive transition of the transfer one-shot is used to reset the transfer prime flip-flop to the set "0" condition. The negative transition, which occurs 100 microseconds later, generates a transfer pulse which triggers the magnet pulser (J). Character A is punched. The dotted signals in the timing diagram indicate the worst possible condition if the start pulse of the next character, B, appeared earlier in the cycle and the motor speed reduced causing jitter in the clock pulse. As indicated, character A will be punched and character B will remain in storage until the next punch cycle. Timing diagram of the transfer circuitry (Figure 7), also illustrates several cycles of operation.

D. Receiving Distributor

Note: Refer to schematic wiring diagram 4441WD and receiving terminal timing diagram (Figure 8).

Initial Conditions

4.37 Approximately 150 to 300 microseconds after the power switch is operated to the ON position, the -6 volt to 0 volt reset pulse generated in the receiving converter appears at terminal E4 of connector J301, the set "1B" terminal of Z310 control register, and the set "0A" terminal of Z320 element. The reset pulse places Z320 element in the set "0" condition, and the control register flip-flop in the set "1" condition. The actions are as follows:

- (a) The start-stop oscillator turns on for one cycle, generating one advance pulse.
- (b) The control register is triggered after completion of one cycle of oscillation, and the oscillator is turned off.

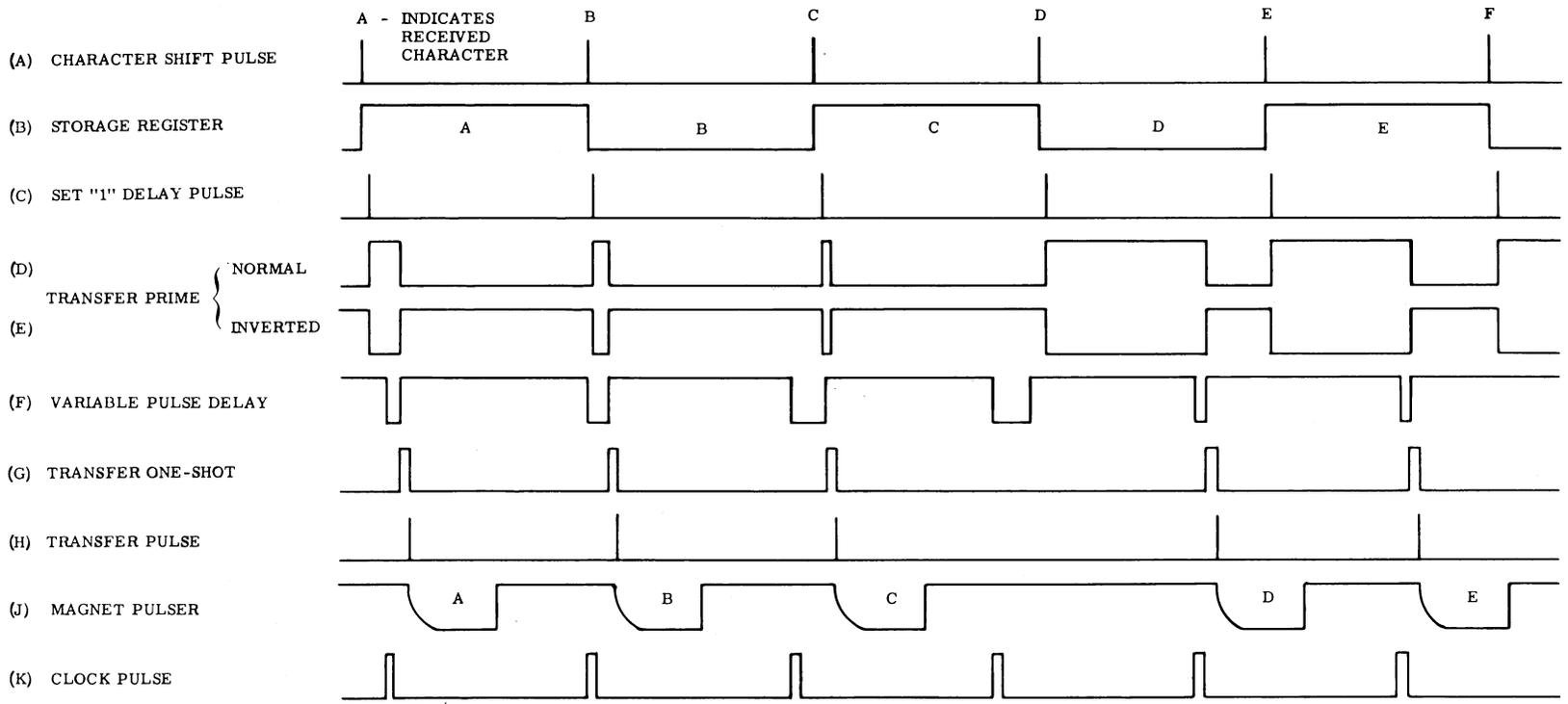


Figure 7 - Transfer Circuitry Timing Diagram (Several Cycles of Operation)

- (c) The stop inserter one-shot is turned on and starts its time out.
 - (d) At the completion of the stop inserter time out, the synchronizer flip-flop is triggered to the set "1" condition.
 - (e) The Z310A start OR gate is opened to accept a start pulse.
 - (f) The Z301 start AND gate is opened.
 - (g) The input gate on the start delay is primed.
- (b) To the input terminal of the Z304 signal delay.

Signal Input

4.38 The receiving distributor receives a +1 volt to -6 volt start signal from the receiving signal converter on terminal C10 of connector J301. This start signal is applied through the operate switch to terminal C of the Z301A signal gate. The start signal is also applied to the set "1B" and prime "1A" input of the synchronizer flip-flop. The signal will pass through the Z301A gate on terminal A provided the Z324 synchronizer flip-flop (output on terminal K) is in the set "1" condition.

Register Drive

4.39 From the output of the signal gate, the signal is sent to the input of Z320A emitter follower, terminal D, and from terminal N of Z302A, to the first inverter of Z303A register drive, terminal B. The output of Z303A, terminal K, applies the inverted signal to:

- (a) The prime "0B" side of the last element in the signal register, terminal H (Z313, Z314, or Z315 element depending on number of code levels).
- (b) The input of the next Z303B inverter, terminal D.
- (c) The input of the Z305 start delay, terminal C.

4.40 The second inverter, Z303B, inverts the signal so that it is back to normal. From the output of Z303B, terminal L, the signal is applied to:

- (a) The prime "1B" side of the last flip-flop of the signal register (Z313, Z314, or Z315 element depending on number of code levels).

4.41 A start transition consists of a +1 to -6 volt transition lasting for a period of one bit. When this transition passes through the first inverter it becomes a -6 to 0 volt pulse. This pulse is sent to the set "1" input of the Z305 start delay one-shot, terminal C, causing it to begin a time-out for approximately one-half bit. The normal output of this one-shot, terminal L, goes from -6 to 0 volt and is applied to terminal N of Z301B start OR gate.

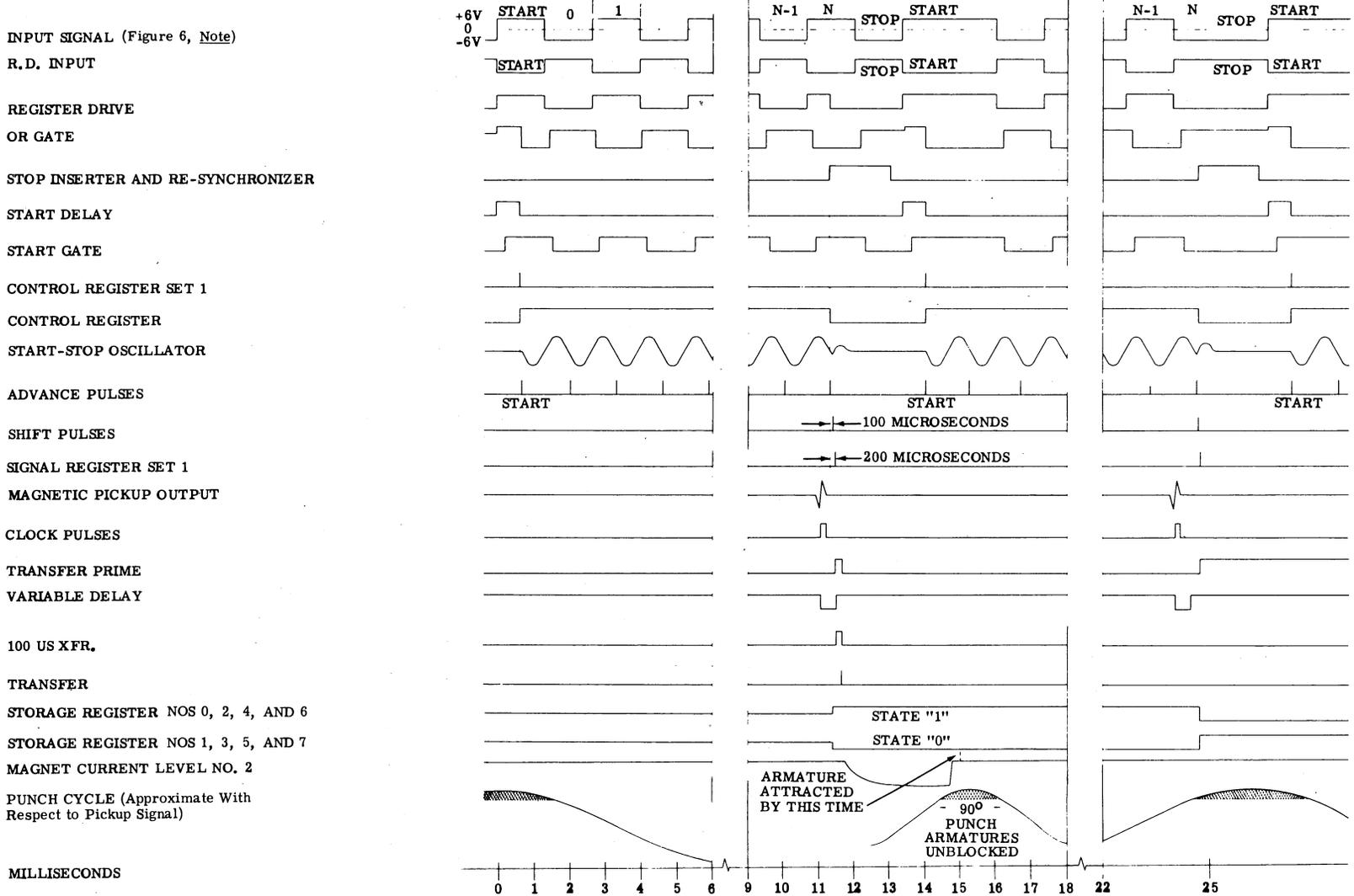
4.42 The second inverter, Z303B, brings the -6 to 0 volt transition from the output of the first inverter, Z303A, terminal K, back to the original 0 to -6 volt transition, and applies it to the input of Z304 signal delay, terminal C. The output of the signal delay, terminal L, delays the 0 to -6 volt transition by 40 microseconds, to prevent a false start, and sends this delayed transition to terminal M of Z301B.

Start Circuits

4.43 The output of Z301B start OR gate is 0 volt, if 0 volt appears on any of its inputs; and -6 volts, if -6 volts appears on all of its inputs. This is an important fact to remember while trying to understand how the start OR gate performs its function in the circuit. If a true start signal has been sent, then 40 microseconds after the signal is received, terminal M of Z301B goes to -6 volts for a period of one bit. Terminal N of Z301B goes from -6 volts to 0 volt as soon as the start transition is received, and remains at 0 volt until Z305 start delay timer relaxes (about one-half bit time duration). The start delay relaxes before terminal M of the OR gate has a chance to return to 0 volt. This results in a 0 to -6 volt transition on terminal N of the OR gate, which will appear on the output, terminal L. If a false start is received (ie, a short 0 to -6 volt transition), terminal M of the OR gate will be at 0 volt when the false start arrives on terminal N of the OR gate, preventing the 0 to -6 volt transition from appearing on the output (Figure 8).

4.44 Negative transition from terminal L of start OR gate is passed through Z301C start AND gate, terminal F, to the input of Z302B start pulse amplifier, terminal B. The start pulse amplifier shapes the negative transition on its input into a positive-going -6 to 0 volt pulse on its output, terminal K. This pulse is applied to set "1A" input of Z310 control register, terminal C, switching it to set "1" condition.

Figure 8 - Tape Receiver Timing Diagram



4.45 When Z310 control register switches to the set "1" condition, the following actions take place.

- (a) Z311 start-stop oscillator starts, due to the 0 volt potential appearing on its input, terminal H, from the normal output of the control register.
- (b) Z301C start gate closes due to the -6 volt potential on its input, terminal E, from the inverted output of the control register.

Start-Stop Oscillator

4.46 The Z311 start-stop oscillator receives a -6 volt to 0 volt signal from the control register flip-flop (4.45). The oscillator begins to oscillate as soon as a 0 volt signal is applied to its input, terminal H, and the output appears as a sinusoidal oscillation on terminal A. This output is sent to the input of Z312 squaring amplifier, terminal H. The squaring amplifier shapes the sine wave to produce a positive-going -6 to 0 volt advance pulse every cycle. One advance pulse is produced for each period of the sine wave output. The advance pulses are applied to both the set "1B" and set "0B" inputs of the signal register flip-flops, terminals E and F of Z313 through Z320, and to the set "0B" input of Z310 control register, terminal F.

Signal Register

4.47 The signal input is applied to prime inputs of Z313, Z314, Z315, or Z316 Nth register element depending on the level of operation (8, 7, 6, or 5 respectively) being considered. Although 8-level operation is assumed in the following, theory of the other levels is similar; the signal input priming the correct element of the signal register.

4.48 The input signal advances through the signal register bit by bit. To analyze operation of the register, consider what happens as a start pulse is shifted through the register.

- (a) The start pulse, after passing through Z301A and Z302A, appears at the input of the first of two register drive inverters, Z303A and Z303B. The first inverter output applies a 0 volt prime signal to the "POB" input of the Nth element in the signal register (terminal H of Z313 for 8-level operation).

(b) This same 0 volt signal is applied to the input of the second inverter, Z303B. Its output, a -6 volt signal, is applied to the "P1B" input of the Nth element, terminal J.

(c) The Nth element is now primed for set "0." When the first advance pulse arrives at terminal F, the Nth element flip-flop switches. Its inverted output, terminal K, applies a prime to the "POB" input of the next register element, and its normal output, terminal L, applies a prime to the "P1B" input of the same Z314 register element.

(d) When the second advance pulse appears at the set "0B" input of Z314, this register element switches to the set "0" condition. Simultaneously, the next bit passes through Z303A and Z303B double inverters, priming the Nth signal register element as described in (a).

(e) Thus, the signal is inserted into the signal register bit by bit until the N+1 advance pulse shifts the start pulse into Z310 control register. The start pulse primes the "POB" input of Z310, and the advance pulse causes this flip-flop to switch to the "0" state.

4.49 When the control register flip-flop switches to the set "0" condition, the following actions take place.

- (a) The start-stop oscillator stops and suspends further generation of advance pulses.
- (b) The 100-microsecond Z307 shift delay one-shot begins to time out.
- (c) The 200-microsecond set "1" Z306 delay one-shot begins to time out.
- (d) The Z301C start AND gate opens.
- (e) The Z305 start delay one-shot is primed.
- (f) The start inserter one-shot starts its time out.
- (g) The synchronizer flip-flop is triggered.

Shift Delay

4.50 The Z307 shift delay one-shot becomes active on receiving the -6 to 0 volt transition on its set "1" input, terminal C, from

the control register. After a period of 100 microseconds, the circuit relaxes and sends a negative going pulse from its normal output, terminal L, to the input of Z308A pulse amplifier. The Z308A pulse amplifier provides a positive going -6 to 0 volt pulse on its output, terminal K. This pulse is applied to the input of Z309A emitter follower circuit, terminal B, which provides power amplification of the pulse. From the output of the emitter follower, terminal A, the pulse is sent to terminal C1 of connector J301. From there it passes to the signal converter to shift the information in the signal register into the storage register.

Set "1" Delay

4.51 After 200 microseconds, the positive transition from the control register triggers the set "1" Z306 delay one-shot, a negative transition is generated at its normal output, terminal L. This transition is fed to Z308B pulse amplifier, terminal D, and appears as a positive -6 to 0 volt transition on the output, terminal L. The pulse is sent to Z309B emitter follower, terminal D, for power amplification, and from the output of the amplifier, terminal N, to the set "1A" input of all the signal register flip-flops (Z313 through Z320 elements, terminal C). The positive transition on the set "1A" input of flip-flops causes them to reset to the set "1" state, since all elements are primed with +1.5 volts on terminal M, "P1A" input.

4.52 Thus, 100 microseconds after the control register goes into the set "0" condition, the shift delay transmits a pulse to the signal converter to shift the information in the signal register into the storage register; and 200 microseconds after the control register goes into the set "0" condition, the set "1" delay transmits a pulse to reset the signal registers to the set "1" condition. In addition to reset, the set "1" delay performs another function. The output of Z309B emitter follower is also applied to terminal B1 of connector J301. From there the output of Z309B (-6 to 0 volt transition) is sent to Z403 transfer prime in the signal converter. This informs the signal converter that the signal is in the storage register and is ready to be punched.

4.53 The -6 to 0 volt transition from the inverted output of the control register is applied to terminal E of Z301C start AND gate, keeping the gate open. The purpose of this gate, which closes while the control register is in the set "1" state, is to prevent signals from being applied to the control register while the start-stop oscil-

lator is in operation. The same positive transition, when applied to the prime "1" input of the start delay one-shot, primes the start delay gate so that it can be triggered to generate a start pulse when the start-stop oscillator is not oscillating.

Synchronizing Flip-Flop

4.54 The positive transition from the control register is also applied to the set "1" input of Z321 stop inserter, terminal C. This element triggers, producing a -6 to 0 volt transition on its normal output, terminal L. This signal is applied to the set "0A" input of the synchronizer flip-flop, triggering this circuit to the set "0" condition. For a detailed description of the resynchronizer circuit, refer to 5.32 through 5.37.

Test Conditions

4.55 With the TEST-OPERATE switch in the TEST position, a -12 volt bias is applied to terminal C of Z301A input gate. This simulates an open line condition.

4.56 In the TEST position, the circuit path from the resynchronizer circuit to terminal D input of the signal gate is opened, and an alternate path is provided from the stop inserter. This condition results in local regeneration of blank characters; the stop inserter applying the stop pulse. Local electronic testing can, therefore, be performed. Note that the resynchronizer circuit will not be triggered; it will remain in the set "0" condition.

4.57 A J302 jack is provided to facilitate local testing and to permit receiving margins to be taken using a 905A or 905B Data Test Set. The test signal applied shall be -6 volts for SPACE and 0 volt for MARK working into a 1200-ohm load. With a test signal applied, the resynchronizer circuit will be triggered randomly.

E. Auxiliary Connections

4.58 Receiving Distributor:

- (a) Set "1" delay, terminal E2, connector J101 informs the auxiliary equipment that the character in the signal register has been transferred to the storage register.
- (b) Start-stop control lead, terminal E3, connector J301 is used to permit the auxiliary equipment to turn the start-stop oscillator on and off.

4.59 Signal Converter:

- (a) Signal blind, terminal E9, connector J401, is used to permit the auxiliary equipment to prevent the receiver from receiving the incoming signal.
- (b) Clock, terminal F1, connector J401, is used to monitor the shaped magnetic pickup and to provide timing in the auxiliary equipment.
- (c) Transfer inhibit, terminal E7, connector J401, is used to inhibit the punch magnets.
- (d) Transfer, terminal E6, connector J401, is used to monitor the transfer pulse for use in the auxiliary equipment.
- (e) Terminals E2 and E3, connector J401, are used in conjunction with auxiliary equipment for vertical parity checks.

5. OPTIONAL FEATURES

TAPE SENDER

A. Transmitting Signal Converter With Rubout Delete

General

5.01 The transmitting signal converter with rubout delete feature is basically identical to the transmitting signal converter described in 3.02, 3.06 through 3.09, and 3.14 through 3.20. The important difference between these units is the rubout delete feature — a feature which prevents the transmission of an all MARK signal from the tape sender to the tape receiver.

5.02 In certain data systems the operator, while preparing a message tape, may insert errors into the tape. To "erase" these mistakes, the errored characters are deleted by punching all levels (rubout) of the entire group of characters involved. The correct message is then repunched into the tape in a new location.

5.03 When the tape is transmitted, the receiving station would normally receive all information sensed by the tape reader at the sending station, including the all MARK or rubout characters. If, however, a transmitting signal converter with rubout delete is utilized at the sending station, the all MARK (rubout)

signals will be suppressed. Consequently, only the valid data information will be reproduced by the tape receiver.

Detailed Circuit Description

Note: Refer to schematic wiring diagram 5917WD.

5.04 General: Since the circuit analysis of this transmitting signal converter is similar to that already covered (5.01), reference will be made to the applicable paragraphs whenever possible.

5.05 The rubout delete function of the transmitting signal converter is controlled by Z215A, Z215B, Z216A, Z216B, and Z217A logic elements. These elements function to control operation of the start-stop oscillator in the transmitter distributor.

5.06 Initial Conditions: Refer to 3.14 and 3.15.

5.07 Reader Input: Refer to 3.16.

5.08 Rubout Delete: The universal contact signal from the reader is applied to Z202D integrator via terminal H9 of J201. The output of Z202D, terminal P, is applied to Z215B OR gate, terminal P. This signal is gated with the inverted output of Z215A, and is applied to terminal R of Z216B emitter follower. The output of Z216B is connected to terminal C4 of J201, and is applied to the start inhibit gate in the receiving distributor. When the output from Z216B is 0 volt, the start-stop oscillator in the distributor is prevented from starting (3.24).

(a) SPACE and MARK Input: If any one of the levels sensed by the reader is SPACE, the corresponding integrator output is about 0 volt. A MARK signal, on the other hand, produces a -10 volt signal. When the MARK and SPACE signals are gated together in Z215A OR gate, its output, terminal B, will assume the most positive potential (0 volt). This 0 volt signal is amplified through Z216A emitter follower, and applied to pin B of Z217A inverter. The inverter output, terminal K, goes to -6 volts and is gated with the universal input in Z215B, causing the output of Z215B to go to -6 volts. This -6 volt level is amplified by Z216B and applied, via terminal C4 of J201, to the start inhibit gate in the distributor. A -6 volt input to the

start inhibit gate allows the start-stop oscillator to start, and the character sensed by the reader to be transmitted to the receiving station.

(b) All MARK Input: If all levels are MARK, however, the output of Z215A will go to -6 volts, and Z217A inverter will present a 0 volt signal to Z215B OR gate. The output of Z215B remains at 0 volt even though the universal contact closes. Consequently, the start-stop oscillator in the distributor will be inhibited, and the all MARK character will not be transmitted to the receiving station.

5.09 Polar Signal Output: Refer to 3.18.

5.10 Request-to-Send: Refer to 3.19.

5.11 Power Requirements: Refer to 3.20.

B. Line Break and Automatic Answer Kit

General

5.12 The line break and automatic answer feature allows a tape sender terminal to automatically transmit its message tape in answer to a call placed by a tape receiver terminal. Operation of both terminals is controlled by the operator at the receiver location. This feature is available in kit form (TP146527) for field or factory installation.

5.13 Proper operation of the line break and automatic answer feature depends upon use of a data set with the following features.

(a) Unattended answering

(b) Reverse channel carrier

These data set features are available with 202C and 202D Data Sets. The automatic answer feature may then be added to existing tape senders.

Note: Another modification kit — interim unattended answer — is available which allows tape senders equipped with the line break and automatic answer feature to make use of that feature, on data set not equipped with reverse channel feature (5.22).

Detailed Circuit Description

Note 1: The following assumes availability of reverse channel carrier and unattended answering.

Note 2: Refer to schematic wiring diagrams 3843WD, 4772WD, and 5941WD.

5.14 Manual Operation With Line Break:

The tape sender is prepared to operate in the manual mode when the following conditions exist.

Power on.

Tape reader loaded with a message tape; tape-out contact closed.

Tape reader and tape winder motor switches OFF.

Data set in TALK condition; telephone receiver on hook.

Interlock and line break outputs at 0 volt and -8 volts respectively.

TEST-OPERATE switch, S101A and S101B, in OPERATE position.

AUTO-MANUAL switch in MANUAL position.

Normally open tape-out contact closed.

Tape reader RUN-STOP switch in STOP position (open).

(a) A call may be placed by the operator at either the receiver or sender location. When verbal agreement is reached to start transmission, the operator at the sender location starts the tape reader and winder motors by placing their respective switches in the ON position. The operator then depresses the DATA button. The data set goes into the DATA mode, placing the sender on line and switching the voltage level on the interlock output (terminal 6 of J601) from 0 volt to +8 volts. Since the AUTO-MANUAL switch is in the MANUAL position (breaking the circuit between Z601B relay driver and motor start relay), the motor start relay will not energize on this +8 volt input.

(b) When the operator at the receiver location places the data set in the DATA mode, a reverse channel (supervisory received data — 387 hertz tone) is transmitted continuously. In the data set at the sender location, a detector recognizes this signal and causes the reverse channel

received to switch from -8 volts to +8 volts. The +8 volt signal is applied through S101A to terminal F of Z601A relay driver. The relay output, terminal J, switches from -28 volts to 0 volt, energizing the line break relay via the tape-out contacts. When the line break relay energizes, normally closed contact C4 opens and normally open contact C5 closes.

(c) The tape sender operator (after a few seconds wait to allow the tape receiver operator time to place data set in the DATA mode) operates the RUN-STOP switch on the reader to the RUN position. This completes the energizing circuit to the reader clutch coil; from ground, through the run-stop contacts, through the normally closed B9 contact and through the normally open C5 contact, to one side of the clutch magnet. The tape reader starts sensing tape. Note that the tape reader will not start sensing tape unless contact C5 is closed. Contact C5 is controlled via the data set at the receiver location; if the tape receiver is not in the DATA mode, or the line is disconnected, contact C5 is opened and contact C4 is closed. If this is the case, and if the RUN-STOP switch is in the RUN position, then the alarm relay (L) will energize, actuating the audible and visual alarms to indicate a line break condition. The reader will not start, pending receiver action.

(d) When an end-of-message (EOM) condition occurs (in this case, end-of-tape), the tape-out contacts open. The line break relay de-energizes, and contacts C4 and C5 return to their normal conditions. Contact C5 opens the energizing path to the reader clutch coil, stopping the reader, and contact C4 completes the energizing path to the alarm relay; from ground, through the RUN-STOP switch, through the normally closed B9, B10, and C4 contacts, then through the alarm relay to -28 volts. Both the audible and visual alarm indicators are energized, and the auxiliary alarm circuit is conditioned to operate.

(e) The alarms are disabled when the operator at the sender location moves the RUN-STOP switch to the STOP position. The reader and winder motors can now be de-energized. If verbal confirmation to disconnect is required, the sender operator may contact the receiver operator via the telephone handset after depressing the TALK

button. If no verbal confirmation is necessary, the disconnect can be made in the normal manner.

5.15 Operation of Line Break: If for some reason (eg. trouble at the tape receiver location) the receiver operator wants to stop transmission and contact the sender operator, just remove the telephone handset from the hook and depress the TALK button. This breaks the reverse channel tone, causing the line break output from the sender data set to switch to -8 volts. The output of Z601A relay driver, terminal J, switches to -28 volts, and the line break relay de-energizes operating contacts C4 and C5 (5.14 (d)). The alarms are disabled when the RUN-STOP switch is operated to the STOP position. The sender operator may talk to the receiver operator by lifting the telephone handset off hook and depressing the TALK button. Transmission may be restarted at the discretion of the operators.

5.16 Automatic Answer and Line Break:
The tape sender is prepared to operate in the AUTO mode when the following conditions exist.

AUTO-MANUAL switch in AUTO position.

Tape reader and tape winder motors OFF.

Tape reader loaded with a message tape; tape-out contact closed.

Data set AUTO key depressed (if strapped for key controlled automatic answering) or wired for permanent automatic answering; telephone receiver on hook.

(a) If conditions are met, the automatic answer relay will be energized via the tape-out contact and the AUTO-MANUAL switch. When energized, the automatic answer relay closes normally open contact B11, shorting the remote control common and ready leads to the data set. This primes the tape sender data set to automatically answer an incoming call.

(b) A call is originated by the operator at a tape receiver location. The tape sender data set will answer this call (1200 hertz tone) and, after several seconds, go into the DATA mode. When it does, its interlock data set ready output switches from -8 volts to +8 volts. This +8 volt signal causes the output of Z601B relay driver to switch from

-28 volts to 0 volt, energizing the motor start relay via the AUTO-MANUAL switch. Normally open contacts K1 and K3 close, energizing the tape reader and winder motors.

(c) Upon hearing the answer tone from the sender data set, the receiver operator places data set in the DATA mode. A reverse channel signal (387 hertz tone), transmitted from the receiver terminal data set to the sender terminal data set, causes the reverse channel received output at the sender location to switch from -8 to +8 volts. A +8 volt input to Z601A relay driver switches its output to 0 volt, energizing the line break relay which operates contacts C4 and C5. The energizing path for the reader clutch coil is from ground; through normally open contacts B9 and C5, the reader clutch coil, and the 25 ohm resistor to -28 volts. The tape receiver operator can control transmission, therefore, depending upon the operating mode of the receiver data set.

5.17 End-of-Message: When the message tape is exhausted, the tape-out contact opens de-energizing the automatic answer and line break relays. These relays return their associated contacts to their normal conditions, causing disconnect of the automatic answer prime (removal of the data terminal ready signal) to the sender data set (contact B11) and stopping the tape reader (contacts B9 and C5). The data set ready output at the sender terminal switches from +8 volts to 0 volt, causing the output of Z601B relay driver to switch from 0 volt to -28 volts. The motor start relay de-energizes, disconnecting the tape reader and winder motors. The receiver operator can now disconnect the terminal. Future calls placed to the sender terminal will not activate the sender terminal. Since the automatic answer relay is de-energized, contact B11 is open and the initial automatic answer conditions are not satisfied (5.16). To complete the automatic answer conditions, a message tape must be loaded into the tape reader.

5.18 TEST-OPERATE Switch: The TEST-OPERATE switch must be in the OPERATE position for normal operation in both the manual and automatic modes. When in TEST position, this switch places a +6 volt bias on the Z601A and Z601B relay driver inputs. This simulates the data set ready and reverse channel received signals of the data set, permitting local testing and troubleshooting.

Note: When installed in tape senders equipped with data sets that do not use reverse channel feature — and with the interim unattended answer modification kit not installed — the TEST-OPERATE switch must be in the TEST position.

C. Operate Time Delay Kit

General

5.19 The TP315900 operate time delay kit provides a minimum 200 millisecond delay for the line break relay (C) in the line break and automatic answer assembly. This delay will keep relay (C) de-energized during most short duration random noise on the telephone circuit which may otherwise be recognized as a reverse channel received signal. The delayed operation also eliminates premature start-up of the tape reader.

Detailed Circuit Description

5.20 This kit functions when the following conditions exist at the tape sender.

- (a) Power on.
- (b) Tape reader loaded with a message tape (tape-out pin down and tape-out contacts closed).

5.21 With the reverse channel received lead off, Z601A relay driver does not conduct and relay (C) is de-energized. The make side of contact C1 is closed and both sides of capacitor C601 are at -28 volts. When the reverse channel received lead turns on, Z601A relay driver conducts, setting the output at pin J to approximately 0 volt. The C601 capacitor changes through resistor R1, thereby, permitting the potential of point 2L to slowly rise toward ground. If the reverse channel received lead goes off again within 200 milliseconds (spurious signal due to noise on the telephone circuit), relay (C) will not energize, preventing the tape reader from starting prematurely. If the reverse channel received lead remains on, the potential across the coil of relay (C) increases sufficiently, in a minimum of 200 milliseconds, to energize the relay. Contact C1 then transfers, removing the capacitor from across the relay coil and discharging the capacitor through current-limiting resistor R2. As long as the reverse channel signal stays on and the tape-out contact at the sender is closed, relay (C) will remain energized. Relay (C)

will drop out approximately 10 milliseconds after the reverse channel signal goes off. The timing capacitor will discharge during the operate cycle of relay (C) and a time delay of 200 milliseconds is required before relay (C) will again energize for another reverse channel on condition.

D. Interim Unattended Answer Kit (Private Line)

General

5.22 The interim unattended answer feature, when used in conjunction with the line break and automatic answer kit (5.12), provides facilities for automatically starting an unattended tape sender from a remote receiver location. It was specifically designed to be used with the line break and automatic answer kit until the data set reverse channel carrier and unattended answer features become available (5.13). The TP148161 interim unattended answer kit is now used only on private line installations not requiring the reverse channel feature. The TP199551 recognizer kit (used with TP199550 generator kit) supersedes TP148161 and also provides additional features for the system.

Detailed Circuit Description

Note: Refer to schematic wiring diagrams 3843WD, 4772WD, and 5941WD, TP177543 etched circuit board drawing and Figure 9.

5.23 Unattended Automatic Answer: The following conditions should exist at the tape sender for unattended automatic answer.

Power on.

TEST-OPERATE switch in OPERATE position.

Tape reader loaded with a message tape.

Tape reader RUN-STOP switch in RUN position.

AUTO-MANUAL switch in AUTO position.

Data set in AUTO mode; telephone receiver on hook.

(a) A call is originated by the operator at the receiver location in the normal manner. If the above initial conditions are satisfied, the automatic answer relay will be energized: from ground, through the relay,

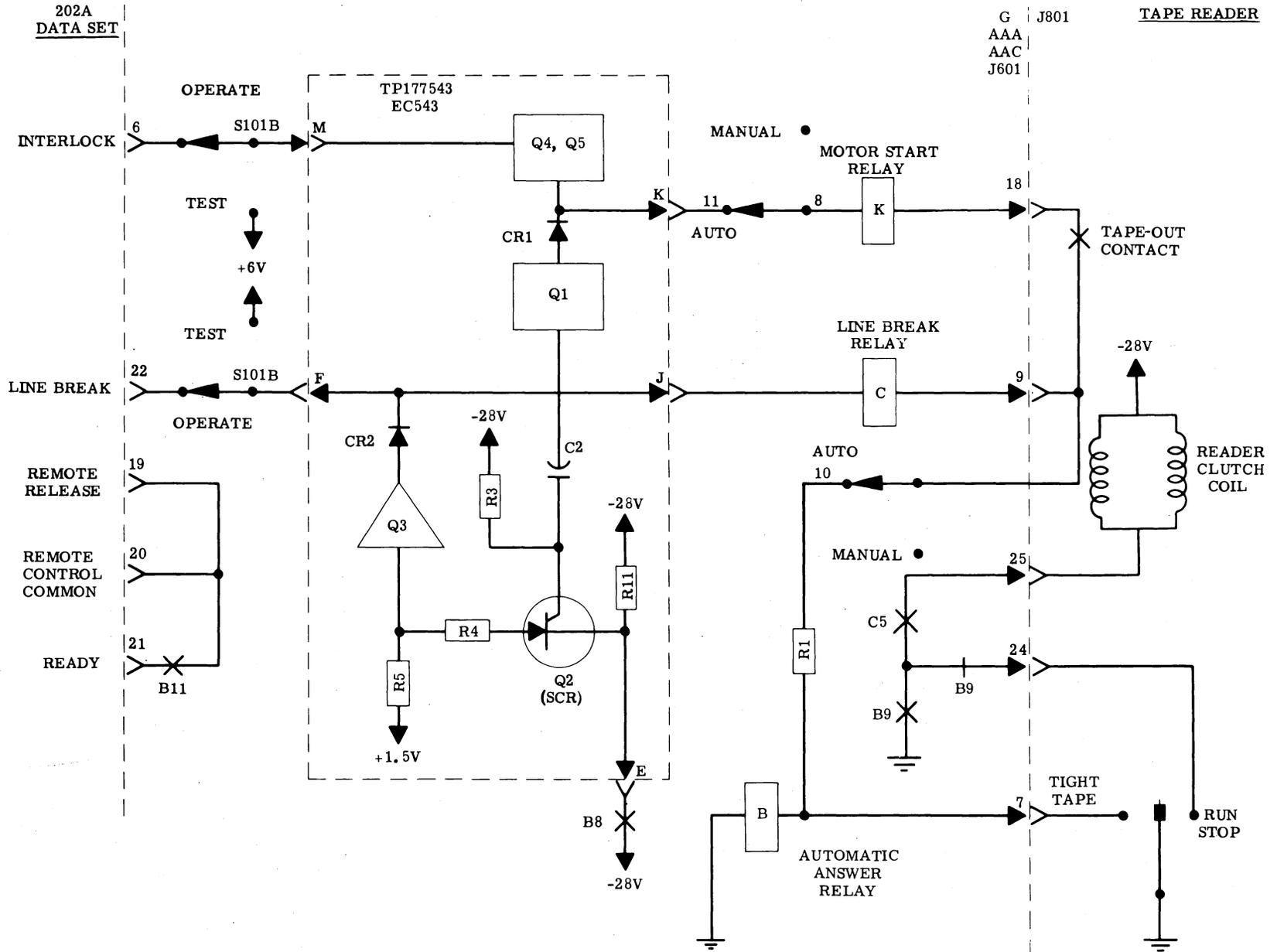
the 250 ohm resistor, the AUTO-MANUAL switch, and the tape-out contacts (closed when reader is loaded with tape) to -28 volts. Normally open contacts B8, B9, and B11 will be closed, conditioning the circuit for automatic answer. The sender terminal 202A Data Set automatically answers the incoming call (contact B11 closed), transmitting a 1200 hertz tone. Within four seconds after hearing this tone, the receiver operator must depress the DATA button on the data set, placing the receiver terminal on line.

(b) The sender 202A Data Set, after a period of several seconds, automatically goes into the DATA mode, and its interlock output switches from 0 volt to +8 volts. This +8 volts is applied through the TEST-OPERATE switch, to the input, terminal M, of the motor start relay driver (Q4 and Q5). The relay driver turns on, and the motor start relay energizes to activate the tape reader and winder motors.

(c) The output of the relay driver (0 volt) is applied to the emitter of Q1, a unijunction transistor, which is part of a time delay circuit. Between 4.5 and 8.5 seconds after the trigger from the relay driver is applied (time-out determined by the size of C1 and R1), a positive pulse is coupled from the base of Q1 to the gate of Q2, a silicon controlled rectifier (SCR). The SCR turns on (contact B8 closed), turning on amplifier Q3. The output of Q3, terminal J, switches to 0 volt, energizing the line break relay (C) via the tape-out contact. When the line break relay energizes, normally open contact C5 closes and completes the energizing path for the tape reader clutch coil: from ground, through normally open contacts B9 and C5, the clutch coil, and the 25 ohm resistor to ground. The reader starts to sense tape.

(d) When the tape is exhausted, the tape-out contact opens causing the automatic answer relay (B) and the line break relay (C) to de-energize. Normally open contacts B8, B9, B11, and C5 are returned to their normal state. Contact B8 causes the SCR to turn off, which in turn switches amplifier Q3 off. Contact B11 disconnects the data set, and contacts B9 and C5 operate to disconnect the tape reader clutch circuit. The tape reader stops sensing tape.

Figure 9 - Interim Unattended Answer Circuit (Early Design)



(e) When the tape reader stops transmitting, the receiver operator should disconnect terminal. The sender terminal 202A Data Set will automatically disconnect, and its interlock output will switch from +8 volts to 0 volt. This causes the motor start relay driver to turn off, motor start relay to de-energize, and the tape reader and winder motors to turn off. The sender terminal will not automatically answer any future incoming calls until the tape reader is reloaded with a message tape.

5.24 Manual Operation: The tape sender may be operated manually in the normal manner (see the appropriate section) by not depressing the data set AUTO button, and leaving the AUTO-MANUAL switch in the AUTO position. When the sender operator depresses the DATA button, the tape reader will start after a 4.5 to 8.5 second delay.

5.25 The unattended automatic answer feature can be disabled by operating the TEST-OPERATE switch to the TEST position. This switch bypasses the relay driver and time delay circuitry on the TP177543 circuit board (EC543), and operates the line break relay. This switch also provides a means for local testing and troubleshooting of the sender terminal.

5.26 When reverse channel carrier is used, substitute TP146520 circuit board (EC520) for TP177543 circuit board (EC543). Operation of the line break and automatic answer feature is described in 5.12 through 5.18.

E. Discrete Calling Recognizer Kit

General

5.27 The TP199551 recognizer kit is the recommended method for unattended service at a sender terminal operating on the switched network, and it replaces the arrangement described in 5.22. The disconnect function is part of the discrete calling modification kit for send stations. Use TP199610 "Y" cable kit with recognizer kit to couple send-receive set to data set.

Theory of Operation (Figures 10, 11 and 12)

Note: Refer to schematic wiring diagrams 7027WD, 7029WD, TP172497, TP303650, and the actual wiring diagrams for circuit description.

5.28 A protected unattended transmitter tape sender set of parts provides security against an unauthorized call triggering the sender into action when the unit is placed in its unattended mode of operation. The companion set of parts is required at the remote receiver to provide the identification signals which must be recognized by the sender before a bona fide request to send is allowed to initiate the transmission. A tape sender is placed in the unattended mode of operation when the controls have been positioned as follows.

- (a) AUTO-MANUAL switch in AUTO position.
- (b) Tape reader RUN-STOP switch set in RUN position.
- (c) Tape (perforated with message to be transmitted) present and threaded into its normal tape path (tape-out switch closed).

Note: When any of the above conditions are not met, the sender is in the MANUAL mode of operation.

5.29 The logic which establishes the unattended mode of operation consists of relay K-835L. This relay is operated directly from relay B of TP146527 line break and automatic answer assembly through contacts 11 and 11M. Contact 11 of relay B is grounded by way of the TP199556 cable assembly.

5.30 In the unattended mode of operation, relay K-835L remains in its operated position until a tape-out condition appears. With the manual mode of operation selected, the recognizer logic is not activated.

5.31 The recognizer logic consists of a Z828 signal generator assembly, EC650/Z829 and EC497/Z830 etched circuit board assemblies, and K-814, K-817L, K-817U, and K-835U relays. The signal generator is an electromechanical device consisting of a coded disc driven by a 20 RPM synchronous motor. It provides sequential code signals to initiate the recognition and cycle. One rotation of the disc through its control segments and 14 coded elements provides the signal, that is checked, with the incoming start signal. The sender disc must be coded identically to the coded disc at the remote receiver. The locally generated start signal is compared bit by bit with the start signal of the remote terminal

and when the incoming signal is in full agreement with the local signal, the transmitter is permitted to start. In this manner the sender is protected against the receipt of an unauthorized call (wrong number) triggering the transmitter when it is in the unattended mode of operation.

5.32 The relay drivers located on the etched circuit boards may be conditioned to turn on and energize the relay when its return (ground) is completed through the sample segment on the revolving disc. The K-814, K-817L, K-817U, and K-835U relays provide the switching and signal comparison functions. The K-814 relay is a double-coil mechanical latching relay with a separate winding to release the latched up armature. When a nonvalid transmitter start signal is detected, K-814 relay is latched up and remains latched until the disc nears the end of its rotation. The K-817L relay operates the motor clutch on the signal generator drive motor.

5.33 The break feature is controlled by an ON/OFF switch (S801) attached to a +6 volt power source. When this feature is not in use, a +6 volt potential is supplied to the reverse channel received input of the TP146527 automatic answer assembly to allow the reader to send when reverse channel is absent. When the break feature is used, the reader clutch will be operated by the reverse channel signal from the data set. A +6 volt potential (reverse channel received) allows the reader to operate. Conversely, a -6 volt potential (absence of reverse channel signal) will stop the reader.

5.34 Two separate output connections are provided for the data set control circuit to allow unattended send-receive operation of units equipped with TP199610 send-receiver terminal modification kit. These connections are:

- (a) Request-to-send (A/M) provides a +6 volt potential for a send-only station.
- (b) Request-to-send (A) provides a +6 volt potential for a data set at an unattended send-receive station.

5.35 The disconnect logic circuit consists of EC497/Z830 etched circuit board and K-813 thermal sensitive time delay switch. The circuit board contains a Z830A emitter-follower amplifier and a Z830B relay driver having a two-input gate. When a positive potential of approximately 8 volts appears at the C2/J801 interlock terminal, a standard voltage of +6 volts is obtained at the output of Z830A. This output

is directed to terminal D of Z830B. The other input to the gate (terminal N) is connected to C4/J801 carrier detect lead from the data set. A -8 volt potential at the latter terminal coincident with the positive input at C2/J801 causes the Z830B relay driver to conduct. When Z830B relay driver is turned on, the K-813 thermal relay will open its normally closed contacts after approximately a 30 second delay. In this manner, the data set release leads are open circuited after a 30 second interval. This will place the data set at the unattended station in the "on hook" mode of operation. The break contacts return to their normally closed condition about ten seconds after a call has been dropped.

5.36 Manual Operation:

- (a) The K-814, K-817L, K-817U, K-835L, and K-835U relays remain in their unoperated position.
- (b) With K-835L relay unoperated, the data terminal ready lead is open circuited so as to inhibit the data set from automatically answering a manual call.
- (c) The terminal marked request-to-send (A/M), C1/J801 is at a +6 volt level and the terminal marked request-to-send (A), B9/J801 is at a -6 volt level.

5.37 Unattended Operation: Refer to timing diagrams (Figures 10, 11, and 12) for the recognizer logic.

- (a) Relay B of the TP146527 line break and automatic answer kit operates when the conditions of unattended mode of operation are established (5.28). Then the make contacts of K-835L relay close to provide continuity to the data set A8/J801 ready lead for automatic answering.
- (b) The EC497/Z830A emitter-follower amplifier will accept a +8 volt interlock signal from the data set at C2/J801 terminal. The output is directed to EC497/Z830B relay driver as mentioned in 5.35 and to EC650/Z829H relay driver. Thus, the K-817U relay is locked up until the interlock signal is dropped so as to initiate the following functions.

- (1) The normal +6 volt potential is removed from C1/J801 terminal, request-to-send (A/M) connection to the data set.

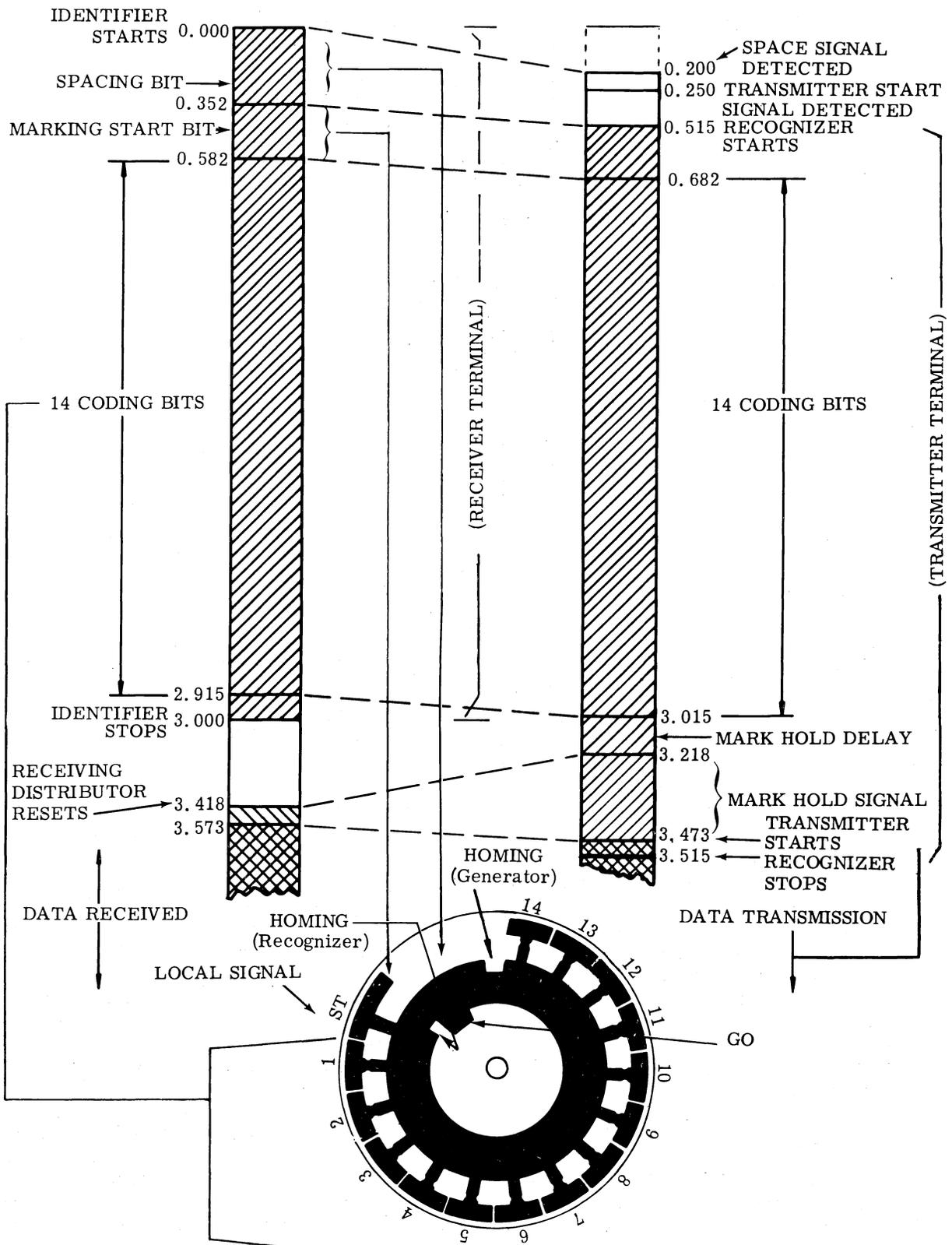


Figure 10 - Timing Diagram for Tape-to-Tape System With the Protected-Unattended Transmitter Feature

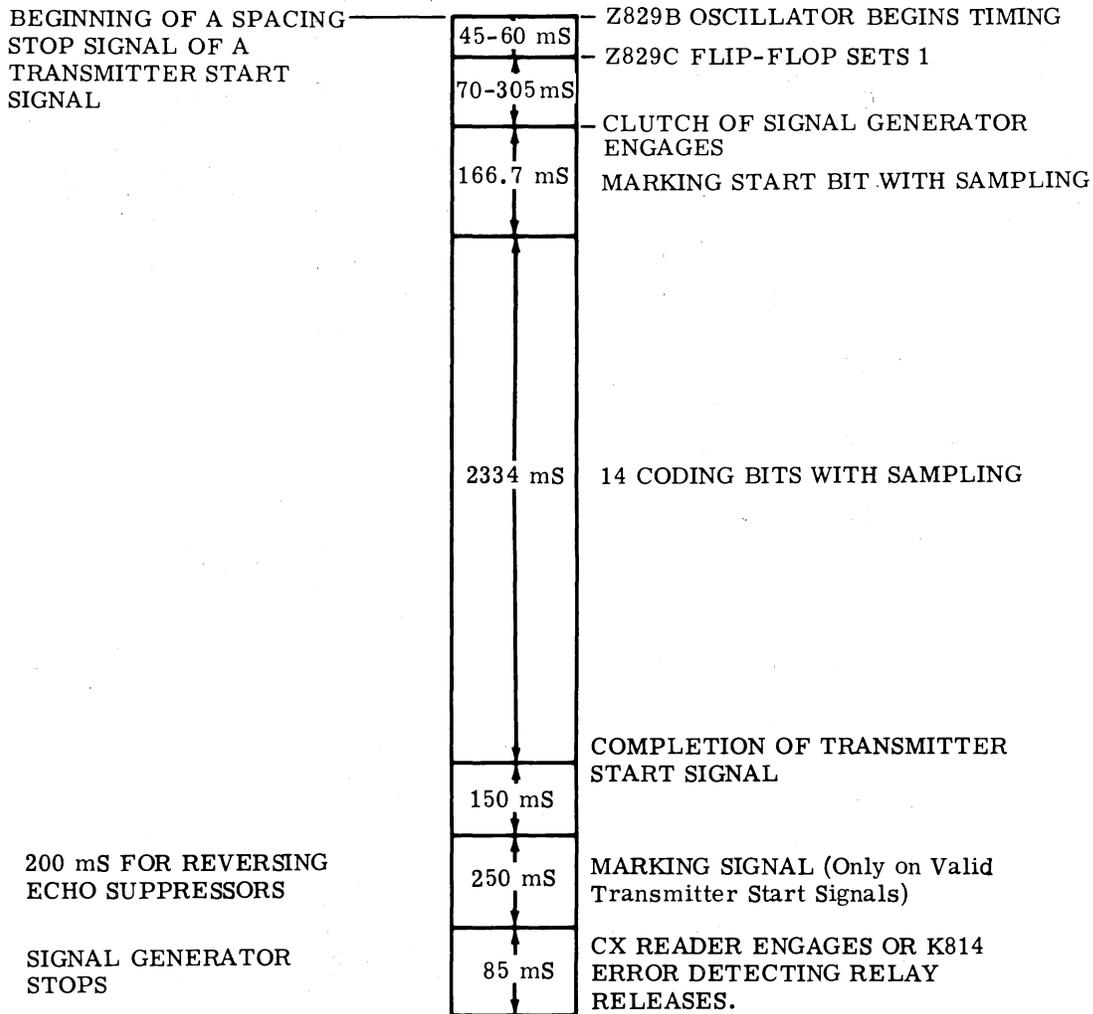


Figure 11 - Timing Diagram for Discrete Calling (Unattended Transmitter)

(2) Contacts 12M and 12 are closed to energize the clock motor and release its clutch/brake mechanism. One rotation of the motor drive shaft moves the disc through its cycle of operation in three seconds. The Z828 signal generator provides the control pulses and 14 code bit recognition sequence for comparison with the received signal.

(3) Connects the data set A2/J801 received data input lead to the recognizer logic EC650/Z829 etched circuit board. The function of the normally open contacts is to prevent the signal generator from starting when a transmitter signal is being transmitted by a receiver of a send-receive terminal.

5.38 EC497 and 650 Recognizer Logics:
 Z829A inverter accepts a ± 8 volt input signal from the A2/J801 received data terminal of the recognizer module (7027WD, Section 582-100-400). The output of the inverter is a -12 volt potential for a spacing signal (spacing is positive from data set) and a 0 volt output for a marking input. At the beginning of a transmitter start signal, the input to Z829B oscillator is a -12 volt potential which turns the oscillator on in order to initiate a time-out sequence of approximately 45 milliseconds. A 0 volt input to the oscillator control (Q5) causes the oscillator (Q4) to recycle and shut off oscillation. The output at base number one of the unijunction transistor triggers the (primed) Z829-C flip-flop to its set "1" state. The normal output (Q7, 0 volt) of the flip-flop is gated with an output from Z829A inverter. When the incoming signal goes marking

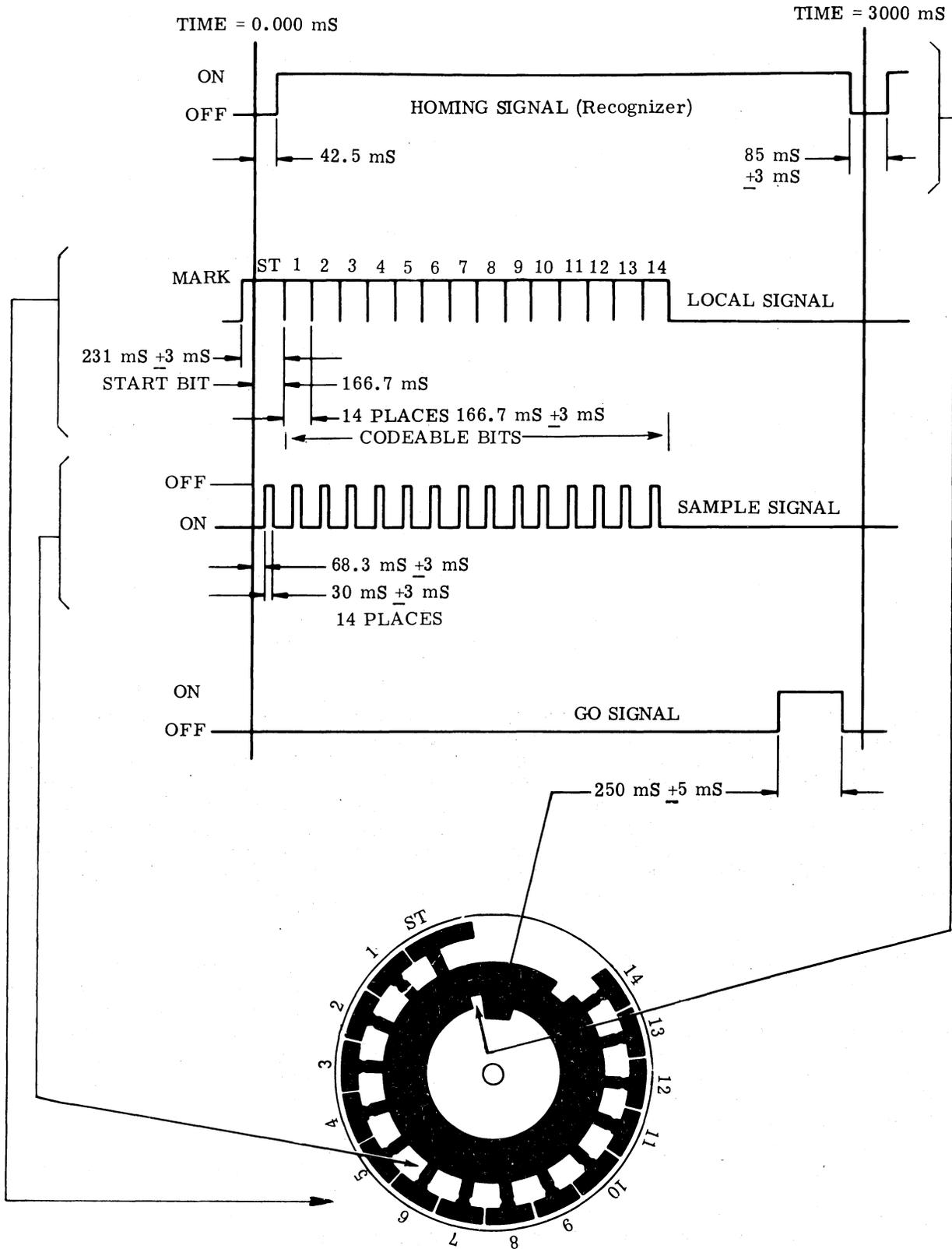


Figure 12 - Recognizer Signal Pattern (Sender Unit)

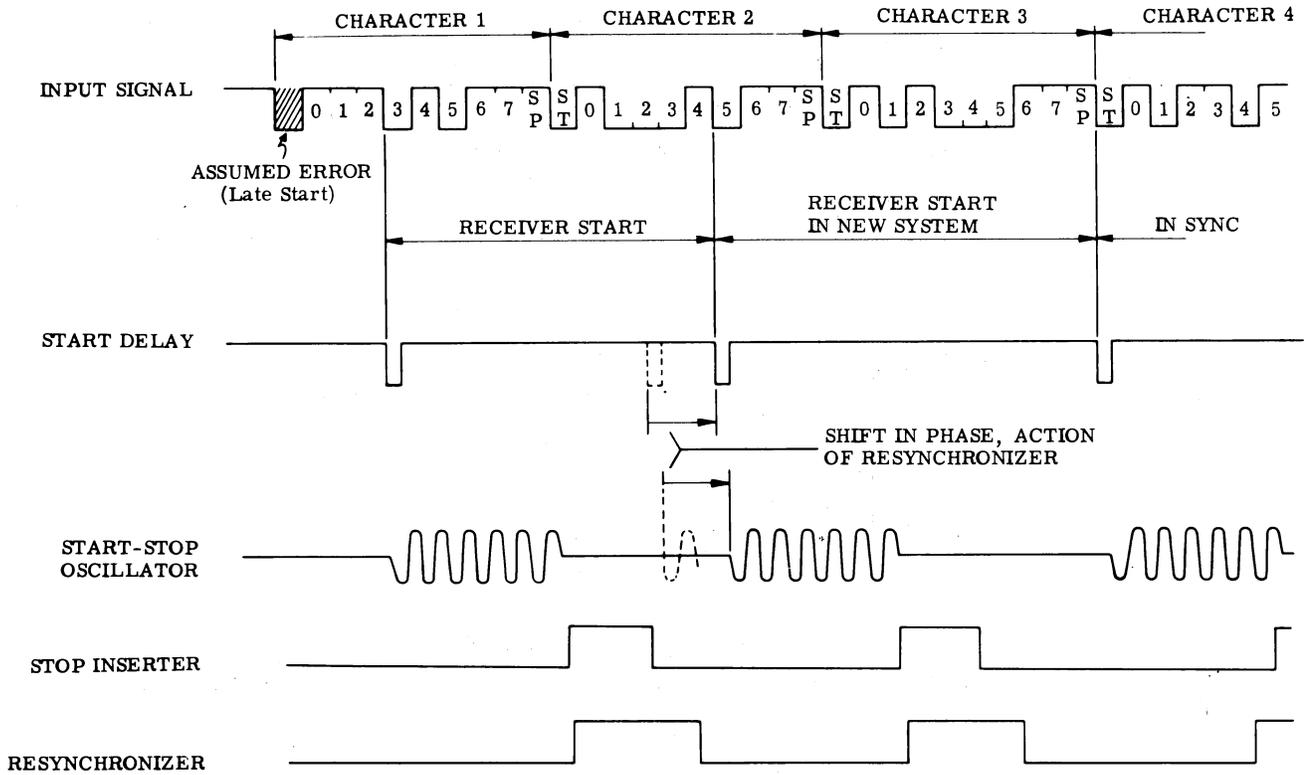


Figure 13 - Resynchronizer Circuit Timing Diagram

and the flip-flop output is 0 volt, the output of Z829D AND gate is 0 volt. The Z829E inverter provides a -12 volts or 0 volt (inverse of its input) to one input of the Z829F AND gate. The other input is a -28 or +6 volt level. When both inputs are positive the input to Z829G relay driver is positive. A negative output voltage turns the relay driver on. With K-817L relay operated, the clutch (break) coil of the Z828 clock motor (signal generator) is energized to initiate one revolution of the coded disc. Parallel brushes sense the continuity of the multipath circuits that are momentarily bridged by the various segments of the revolving disc. The 3000 millisecond interval for one rotation of the disc provides the timing sequence for the respective elements (Figure 11). This initial control signal, recognizer homing, is generated to lock up K-817L relay for one recognition cycle. After approximately 2915 ms, the recognizer homing pulse is cut off and K-817L relay drops out.

5.39 On K-814 relay, coil number one (local signal) and coil number two (received signal) are opposed windings (bucking) which compare each of the coding bits of both transmitter start signals. A sample pulse is impressed

upon the common terminal of the relay at the midpoint of each bit (Figure 13). Thus, an unauthorized call will cause the relay to pick up and latch since the received transmitter start signal will not compare identically (element by element) with the locally generated transmitter start signal. As long as both coils are either marking or spacing which is the condition when identical signals are present, then the relay does not operate and latch up.

5.40 The Z828 signal generator also provides a control signal (GO) after the transmitter start signal has been received. The control signal operates K-835U relay if K-814 recognizer relay did not operate and latch up on the received signal. The K-835U relay locks up until a tape-out condition occurs.

5.41 The closure of the make contacts on K-835U relay provides both the request-to-send (A/M) lead connection and the request-to-send (A) lead connection to the data set with a +6 volt potential for a duration of 250 milliseconds. This signal (GO) will cause the data set to generate a mark-hold signal. The purpose of the 250 ms mark-hold signal is to turn the echo

suppressors (associated with telephone lines) around.

5.42 The Z828 signal generator will release the control signal (GO) and the recognizer homing control signal as the coded disc completes its cycle. The K-817L relay drops out causing one of two things to happen.

- (a) The release of the K-814 latched recognizer relay on a nonvalid transmitter start signal, or
- (b) the engagement of the reader clutch on a valid transmitter start signal.

Note 1: It is necessary that the disc at the remote receiver have the same coding as the disc at the sender, since the discs are compared (element by element) at approximately the same time. Exercise care in handling the disc so that the surface of the segments is not damaged or dirtied.

Note 2: The TP199556 cable assembly connects the TP199555 protected-unattended transmitter recognizer module to the data set, TP146527 line break and automatic answer assembly, and the ac power. The cable assembly also contains a 2.7K resistor which connects the +17.5 volt lead and the reverse channel lead of the data set together. This arrangement generates a continuous reverse channel tone when a reverse channel type data set is used.

F. Send-Receive Mode Control Kit

General

5.43 The TP320296 modification kit provides the ability to control the send-receive modes of a station equipped with a TP199551 recognizer unit and a TP199610 "Y" cable assembly, by turning the reverse channel on and off. Without this feature, it is necessary to terminate a call to return a station to the send mode (after it has already gone from the send mode to the receive mode).

Detailed Circuit Description

Note: Refer to wiring and timing information Figures 14, 15, and 16.

5.44 When a call is established between two send-receive stations, the called station will initially be in the receive mode, the K-835L

relay is unoperated and the called stations data set receives its own transmitted reverse channel signal. After the discrete calling code is transmitted and verified (by depressing the TRANSMITTER START button at the calling station), the K-835U relay at the called sender is operated, (placing the send-receive station in the send mode). The request-to-send signal (Figure 15) is then applied and the data set of the called station goes into the send data and reverse channel receive modes.

5.45 The time required for the called stations data set to receive reverse channel signal from the calling station can be up to eight seconds after the request-to-send signal has been applied. During this time, reverse channel detection is off and K-835U relay must remain operated. The TP303294 circuit card must not complete its time out in this interval or K-835U relay will drop out, causing the station to revert to its original receive mode. For this reason, the time for a data set to receive reverse channel should be determined to insure proper time out (strap selection is at the data set). The recommended time-out period is eight seconds.

5.46 By monitoring reverse channel at the sender the mode switch feature controls the operation of the K-835U relay. The reverse channel signal causes the output of the transistor on the TP303294 circuit card to be inserted into the ground path of K-835U relay. With reverse channel at +6 volts on the input (pin M), capacitor C1 will charge to +6 volts through R1 and CR3 holding Q1 off and Q2 on (pin B must be connected to circuit common to provide a return path for load current).

5.47 If K-835U relay is operated and the unit is in the send mode, the reverse channel signal is dropped for a period of time (4, 8, or 12 seconds) determined by the strapping of the TP303294 circuit card. With reverse channel off, -6 volts is applied to the input, so capacitor C1 will discharge toward a -6 volt through R1, 2, 3, and 4 (Figure 17). When the potential at the base of Q1 reaches approximately -0.4 volts, Q1 will turn on, turning Q2 off after the time delay.

5.48 The time-out period is the off time of the reverse channel signal before sender-to-receiver switching occurs. As time out occurs the output transistor turns off and causes K-835U relay to de-energize. The release of K-835U relay opens the holding circuit contact to prevent accidental turn on of the request-to-send lead. The station has now reverted to the receive

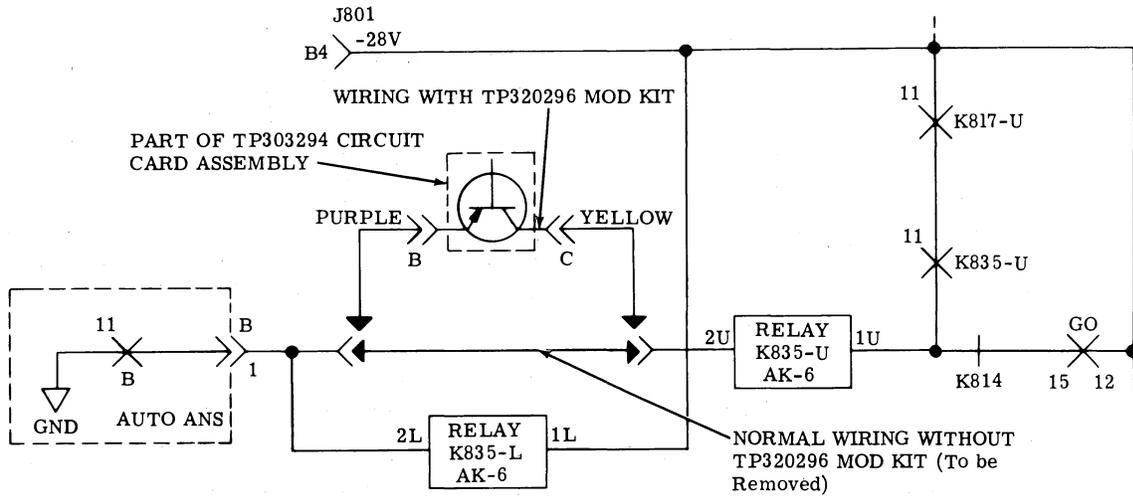


Figure 14 - TP320296 Mode Switch Feature Schematic Wiring Diagram

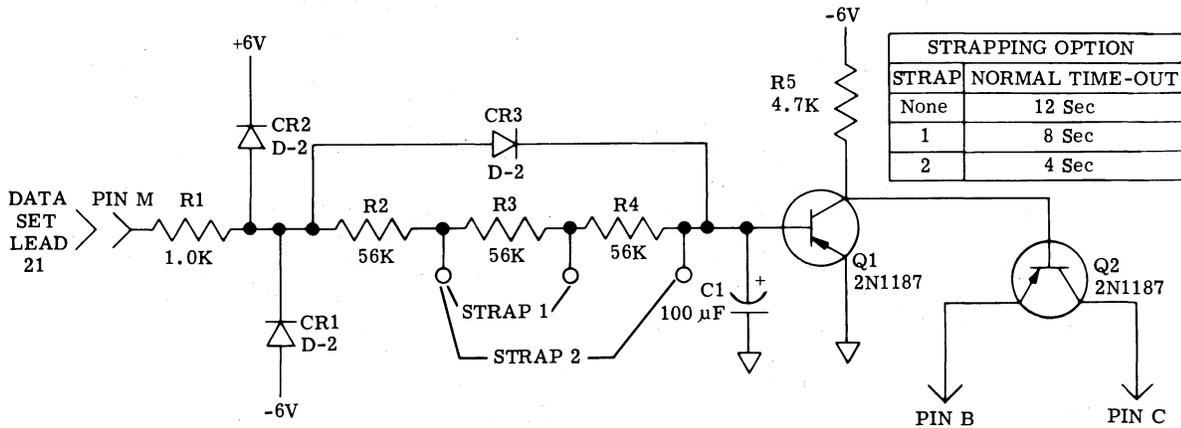


Figure 15 - TP303294 Circuit Card Schematic Wiring Diagram

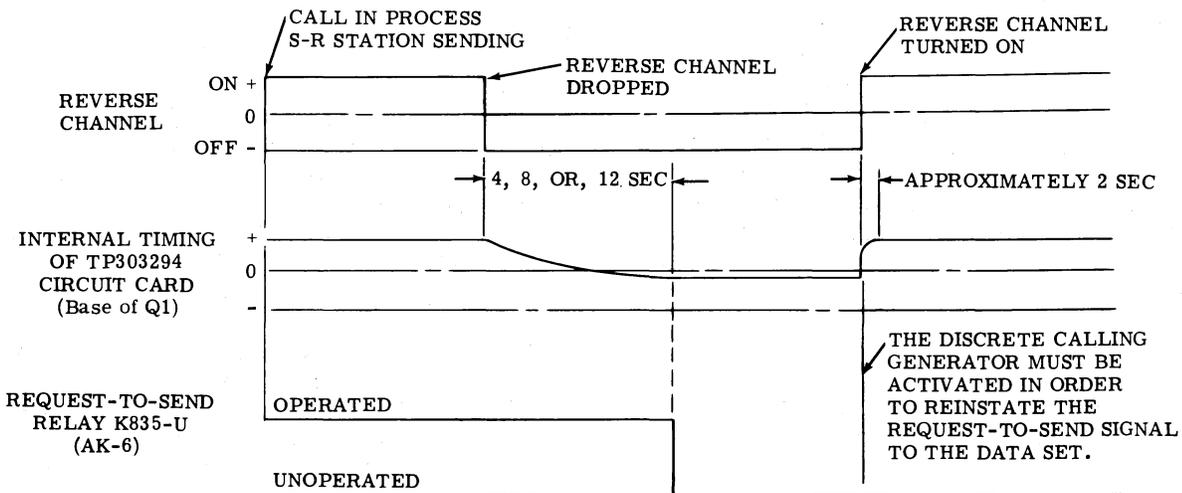


Figure 16 - TP320296 Mode Switch Feature Timing Diagram

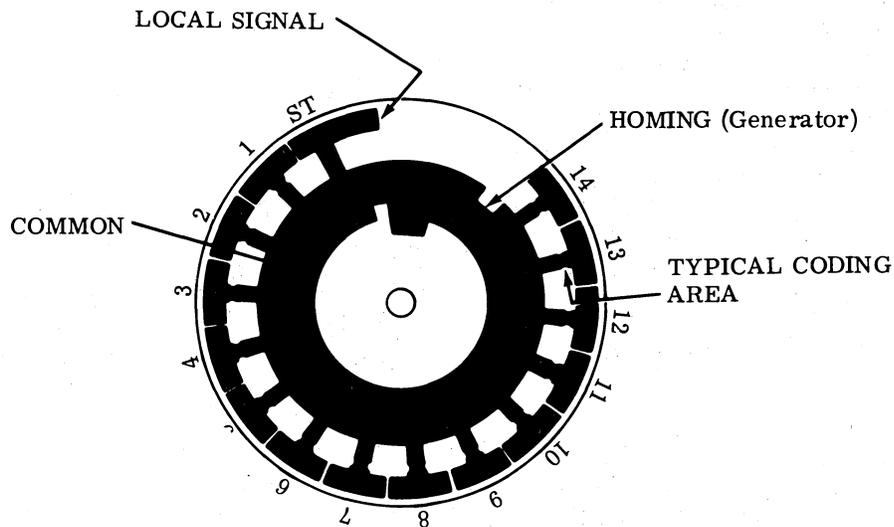
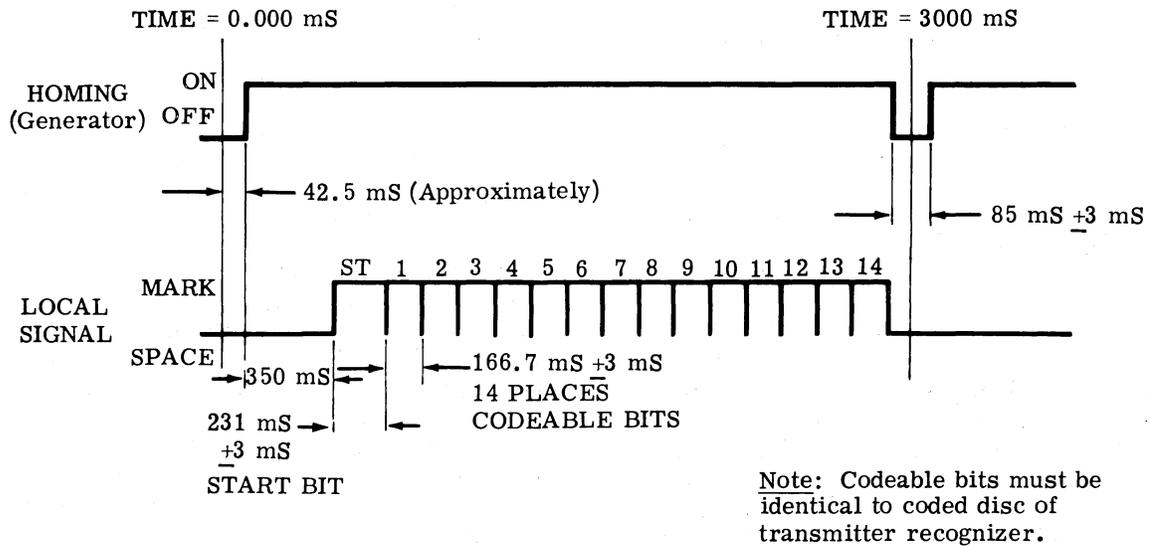


Figure 17 - Identifier Timing Diagram (Receiver)

mode. If a discrete calling code is transmitted again, the station returns to the send mode. Should no traffic be received for 30 seconds after the reverse channel is dropped, disconnect will occur.

TAPE RECEIVER

A. Automatic Answer Kit

General

5.49 The automatic answer feature allows a tape receiver terminal to automatically answer to a call placed by a tape sender terminal. Operation of both terminals is controlled by the

operator at the sender location. This feature available in kit form (TP146528) for field or factory installation is superseded by TP199593 modification kit (5.54).

Detailed Circuit Description

Note: Refer to schematic wiring diagrams 3845WD and 4773WD.

5.50 Automatic answer, or unattended operation, of the tape receiver requires that the following conditions exist at the receiver locations.

Data set in AUTO condition; telephone receiver on hook.

Data set properly wired (see the appropriate section).

Sufficient tape supply.

5.51 A call is originated by the operator at the sender location in the normal manner. The receiver data set automatically answers the call, and goes into the DATA mode (terminals 19, 20, and 21 of J501 strapped together). When in DATA mode, the data set transmits a brief 1200 hertz tone to the sender terminal data set. Simultaneously, the interlock output switches from 0 volt to +8 volts. This +8 volt level is applied to the input of Z501A motor control relay driver, terminal F, causing its output, terminal J, to go to 0 volt. The motor control relay (B) energizes, closing the tape punch and tape winder motor contacts (B3 and B1), turning the punch and winder motors on. The receiver Z501B input amplifier acts to blind the receiver Z401 signal amplifier in the receiving signal converter (3833WD, terminal E9 of J401). The output of Z501B is determined by the condition of the carrier on-off signal from the data set. When in the OFF condition (ie, no transmission in process) -8 volts is applied to the input, terminal N of Z501B. Its output, about +1.5 volts, holds the output of Z401 (EC355) at a positive potential simulating a MARK (or stop) condition.

5.52 Upon hearing the answer-back tone from the receiver data set, the sender operator places data set in the DATA mode. The receiver data set carrier detector recognizes the 1200 hertz tone now being transmitted by the sender data set, and switches the carrier signal from OFF to ON (+8 volts). This +8 volt input to Z501B causes its output to go to -6 volts, unblinding the receiver Z401 signal amplifier in the receiving signal converter. The receiver terminal is now prepared to accept data.

5.53 At the end-of-message, the sender operator disconnects data set by lifting the telephone receiver off hook, depressing the data set TALK button, and replacing the receiver on hook. The receiver data set disconnects automatically, returning the interlock output to 0 volt — to turn off the winder and punch motors — and returning the carrier on-off signal to OFF — to blind the receiver signal input. The receiver is now prepared to accept the next incoming call.

B. Automatic Answer and Disconnect

General

5.54 The TP199593 automatic answer modification kit causes an unattended receiver to automatically answer and terminate incoming calls. Termination of a call is sensed by monitoring the data set data carrier detector lead. After a 30 second interval in which the data carrier detector is OFF, the call is automatically terminated. Since the disconnect feature senses the data carrier detector lead output, reliable operation of the disconnect cannot be assured with the 202A and 202B Data Sets in all locations. Therefore, 202C or 202D Data Sets should be used when a disconnect problem is encountered.

Theory of Operation

Note: Refer to schematic wiring diagram 7279WD.

5.55 The automatic answer logic consists of etched circuit board combination (EC521/Z501, EC497/Z502) and K-501 relay. The circuit board combination contains the electronic logic to function with the type 202 Data Set. The normally opened contacts of K-501 relay are actuated by this logic to energize the tape punch motor and the tape winder motor.

5.56 The automatic disconnect feature consists of EC497/Z502B etched circuit board and K-502 thermal actuated contacts to provide 30 seconds of ON time before the release lead connection is opened. Also, EC521/Z501B amplifier is connected to the same input to provide a standard output for blinding the receiving distributor when there is no carrier detect signal.

5.57 Automatic Answer Logic: When a +8 volt potential appears on the interlock terminal lead of the data set, terminal 6 of 501, EC497/Z501A emitter-follower consisting of Q1 and Q2 (EC521). This circuit operates with inputs of +8 volts and 0 volt levels. Transistor Q1 is cut off with the +8 volt input potential and the resulting -6 volt output turns on Q2 to energize the K-501 relay. With the normally opened contacts of K-501 closed, the 120 volt input leads to the tape punch motor and the tape handling motor are energized. However, the punch is not enabled until the carrier signal is detected.

5.58 **Blinding Logic:** The EC521/Z501B input amplifier senses the potential at terminal 8 of P501, the carrier detect lead to the data set. This input is either at a +8 volt level or a -8 volt level. When the +8 volt signal is present (carrier), Z501B is biased to cutoff and its output becomes a standard value of -6 volts. With -8 volts at input (N) the transistor conducts and its output shifts to a standard 0 volt level. Thus, the 0 volt potential used to blind the receiving distributor (data set not detecting carrier on the line) is removed to enable the punch when the carrier is detected.

5.59 The automatic disconnect logic consists of EC497/Z502B circuit board (relay driver) and a K502 thermal sensitive switch. The relay driver has two gated inputs. Input N is attached to terminal 8 of P501, carrier detect lead to the data set and input D is attached to terminal 6 of P501, interlock lead connection to the data set. The relay driver will conduct only when the input at D (interlock) is approximately +8 volts and input N (carrier detect not present) is approximately -6 volts. Under this condition, inhibit gate Q1 output will be approximately +6 volts (normally -12 volts) and the inverter Q2 is turned off to allow Q3 to conduct. With Q3 conducting K-502 relay is energized. After approximately 30 seconds the break contacts (K-502) will open circuit the data set release leads. This procedure places a manually operated or unattended data set "on hook". The break contacts close ten seconds after a call has been dropped.

C. Resynchronizer Modification Kit

General

5.60 The purpose of the resynchronizer circuit feature is to guarantee resynchronization of a tape receiver with the incoming signal, when a synchronization error has occurred due to a noise burst on the line. The circuit will achieve positive resynchronization under all random code structures or transmission conditions.

5.61 This feature is available in kit form (TP148123) for field or factory installation.

Detailed Circuit Description

Note: Refer to schematic wiring diagram 4441WD.

5.62 **Normal Operation:** Operation, as described below, assumes the following conditions.

TEST-OPERATE switch in OPERATE position.

Unit receiving traffic.

(a) The Z321 stop inserter is a one-shot circuit which, when triggered, will turn on and remain on for a preadjusted time interval (eg, the time out for 5-level units is adjusted to 2.9 ± 0.1 milliseconds; for universal 5- to 8-level units, the stop inserter time out is 0.95 ± 0.1 milliseconds). In the following, a 5-level unit is considered.

(b) The function of the stop inserter is to locally regenerate a stop pulse, at the end of each received character cycle, to prevent the premature start of the receiving distributor due to line noise. When a pulse is received, the Z305 start delay one-shot is triggered and times out for one-half a bit (475 microseconds at 1050 baud). The output, terminal L of Z305 triggers Z301B OR gate which, in turn, triggers the Z301C AND gate to produce a 0 volt to -6 volt transition. This negative going pulse triggers Z302B start pulse amplifier generating a -6 to 0 volt pulse. This pulse is applied to the set "1A" input of Z310 control register flip-flop, placing it in the set "1" condition. The normal output (L) of Z310 goes to 0 volt turning on the start-stop oscillator which generates advance pulses. The pulse, followed by information bits, is shifted down the signal register until it reaches the last element (Z320). This element (0 level) primes POB control register input so that the next advance pulse generated by the oscillator will place the control register in the set "0" condition.

(c) The oscillator will turn off and simultaneously, the Z321 stop inserter will be triggered. The normal output (L) of the stop inserter goes from -6 to 0 volt. This signal is applied to the set "0A" input of the Z324 synchronizing flip-flop.

(d) The inverted output signal (K) of the synchronizing flip-flop goes from -6 to 0 volt. This positive pulse passes through the TEST-OPERATE switch to terminal D of Z301A signal gate. The output of Z301A goes to 0 volt and remains at this level (or

slightly more positive) until the incoming transition of the next character, or until the synchronizing flip-flop goes to the set "1" condition. The latter action takes place when the stop inserter completes its time out and the inverted out (K) switches from -6 volts to 0 volt. This signal, when applied to the set "1A" input of the synchronizing flip-flop, triggers it to set "1" only if the prime 1A input is at 0 volt, or if a MARK signal appears at terminal C10 of J301. The synchronizing flip-flop action follows the stop inserter whenever the received unit is in synchronization with the incoming signal.

5.63 Resynchronization: In the timing diagram (Figure 13), character 1 contains an errored start pulse. The next MARK to SPACE transition occurs on receipt of the third bit. The receiver accepts this SPACE signal (ie, bit 3) as a start pulse, resulting in a "late start" or "out of sync" condition. At the end of the character cycle, the stop inserter begins its time out during the middle of the start pulse of character 2. The resynchronizer flip-flop is also triggered at this time. However, it is not reset when the stop inserter finishes timing out because a SPACE bit (bit 2 of character 2) is present at the signal input. This SPACE signal is applied to inputs M (prime "1A") and E (set "1B") of the synchronizing flip-flop, while the prime "1B" input (J) is primed by the output (K) of the stop inserter. The overall effect of the above action is to move the next start signal to the right. The fifth bit of character 2 is now recognized as the start signal. In character 3, similar action takes place, and by character 4 the receiver is resynchronized with the incoming signal. During correction (or resynchronization) of the above error condition, two incorrect characters would have been recorded by the unit.

5.64 Automatic Reset: If power is interrupted for some reason and restored, the synchronizer flip-flop could possibly be triggered to the set "1" condition. This would place a 0 volt signal on the input gate, preventing passage of a start pulse through the gate. To eliminate this problem, the automatic reset is utilized. When power is turned on, a reset pulse is generated and applied to the set "0A" input of the 0-level flip-flop and also to the set "1B" input of the control register flip-flop. This turns the start-stop oscillator on for one cycle to generate one shift pulse. The control register is triggered to the set "0" condition, and its inverted output (K) goes from -6 volts to 0 volt. This signal is applied to the stop inverter. The normal output (L) of the

stop inserter is applied to the set "0A" input of the synchronizer flip-flop, resetting the circuit and preparing the unit to receive data.

5.65 Test Conditions: With the TEST-OPERATE switch in the TEST condition, a -12 volt bias is applied to pin C of Z301A OR gate to simulate an open-line condition. In the TEST position, the circuit path from the synchronizer circuit to the pin D input of the signal gate is opened, and an alternate path is provided from the stop inserter. This allows local regeneration of blank characters (the stop inserter applying the stop pulse), so that local electronic testing can be carried out. Note that the synchronizer circuit will not be triggered; it will remain in the set "0" condition. A J302 jack has been provided to facilitate local testing and to determine receiving margins. Using a TSG801 or 800 (905A or 905B) Data Test Set, working into a 1200 ohm load, apply a -6 to 0 volt (SPACE to MARK) test signal at this point. With the test signal applied, the synchronizer circuit will be triggered randomly.

D. Discrete Calling Generator Kit

General

5.66 The TP199550 discrete calling feature guards against tapes being released from unattended tape senders on unauthorized calls. The purpose of the receiver modification kit is to generate a valid call, therefore, the calling station must generate the correct discrete 14-bit character for recognition at the unattended station before the tape will be released.

Operating Procedure to Initiate a Call

5.67 Procedure:

- (a) Place a call to the unattended sender.
- (b) When the unattended sender terminal goes to the DATA mode on the completion of the 1200 hertz beep tone, depress the DATA button on the data set at the receiving station to establish the DATA mode of operation.
- (c) Depress the transmitter start switch located on the new TP199554 panel.
- (d) Data will be received at the receiver terminal following the three second recognizer cycle, provided that the sender and receiver terminals have been coded identically.

Detailed Circuit Description

Note: Refer to schematic wiring diagram 7025WD.

5.68 Refer to the sequence of operation of the discrete calling feature (Figure 11). A call is placed and the sending terminal data set answers. It responds with a marking tone if a 202A Data Set is used, or a 2025 hertz beep tone if a 202C Data Set is used and then reverts to the receiving mode. The calling data set is then placed in the DATA mode by depressing the DATA button. The operator depresses the TRANSMITTER START button at the receiver terminal which turns on the data set request-to-send function and starts the Z732 generator. This is time 0.000 (Figure 10). The generator sends a 0.352 second space followed by a 0.230 second mark which is used to start the recognizer at the sending terminal. A sequence of 14 bits (0.167 seconds each) is then sent and compared at the recognizer on a bit by bit basis. At the end of this sequence the generator stops, the request-to-send function is turned off and the receiver is now prepared to receive. At the sender, if the recognizer found that all bits were valid, the request-to-send function is turned on and after a brief delay (timed by continued rotation of disc), the reader will be activated and the recognizer disc will stop. Should any received bit be invalid during the sequence of 14 bits, the reader will not be engaged and no transmission will begin. Thus, an unauthorized caller will not be able to start an unattended sender. When the calling party hangs up, the sender will disconnect automatically after a 30 second time-out period.

5.69 The identifier logic consists of TP199570 electromechanical signal generator, and K-716L and K-716U relays. The Z732 signal generator is identified in wiring diagram 7025WD. The multisegment disc of Z732 is rotated by a clock motor to provide the three second (current/no current) pattern for the coded signal and relay switching functions. One cycle of the TP199580 disc provides the long space and 14-element coded signal (local signal) as the respective brush rides against the successive segments. Another brush makes contact with an inner circle of the disc to provide the (identifier) homing signal. In this manner, a start-stop identification pattern is generated to key the data set which in turn supplies the outlying unattended transmitter with the transmitter start signal for the comparison check.

5.70 During one cycle of the disc, the local signal segments pulse the K-716U relay. The initial element is a long spacing signal (no current) followed by a 231 ms marking pulse and fourteen codeable elements of unit length. When the normally open contacts 5 and 5M of K-716L relay are closed, the local signal sequence is directed to terminal A1 of J701, the send data lead to the data set. The K-716L relay is also used to energize the motor and release the clutch/brake and to activate the receiving distributor.

5.71 The Z732 signal generator consists of an ac synchronous motor which drives a codeable etched circuit board commutator (Figure 17) having multiple levels or concentric rings of segments. Multiple (stationary) brushes make contact with the respective rings to sense the intelligence set up. The 20 RPM motor is energized by a 120 volt ac potential through contacts 1 and 1M of K-716L and the common lead. Note the clutch/brake release feature of the motor to restrain overtravel. Refer to Figure 18 for the timing diagram of the generator output.

5.72 When a call is initiated through the data set to the unattended station and the transmitter start switch located on the new panel is depressed, K-716L relay is energized. This relay is held in its operated position for the duration of the (identifier) homing pulse (Figure 17). This relay starts the motor and energizes the clutch/brake to allow the disc to rotate. The relay drops out after the disc completes one cycle (approximately three seconds).

5.73 With K-716L relay operated, contacts 4 and 4M close to energize terminal C1 of J701, the request-to-send lead (+6 volts) to the data set.

5.74 A 15-bit transmitter start signal is generated by the (local signal) slip connection with the outer ring of the disc. This signal consists of a long spacing stop bit (350 ms — no current) followed by a marking start pulse and 14 mark or space coding bits. A marking signal is generated when continuity exists between the respective codeable segments (14 total) and the associated sample segment to the common slip connector and the -28 volt supply. A spacing pulse occurs on coded segments not joined by the narrow ribbon. Thus, K-716U relay is energized on the marking pulses of the transmitter start signal. When this relay operates, the normally closed contacts 8 and 8B are opened to remove the +6 volt potential directed through

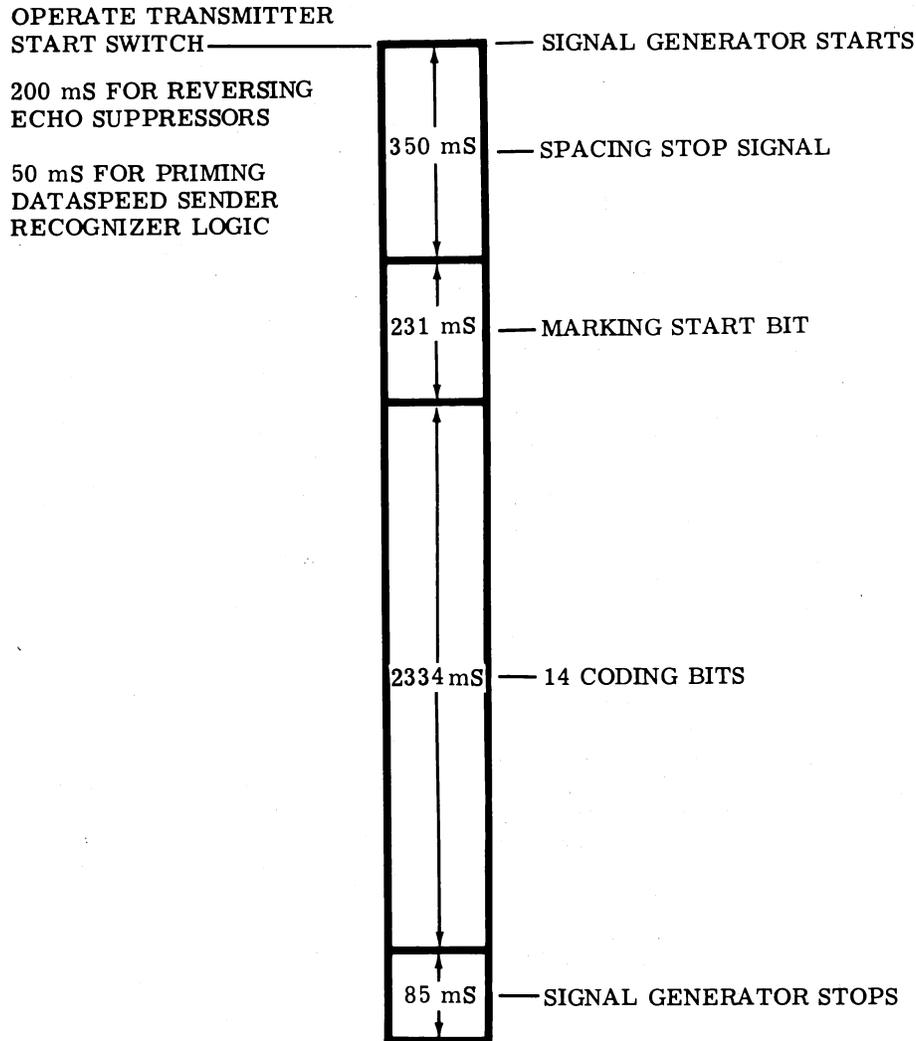


Figure 18 - Timing Diagram for Discrete Calling (Attended Receiver)

K-716L toward terminal A1 of J701, the send data lead to the data set. Absence of a positive potential at the data set will provide a marking pulse to the line.

5.75 The receiving distributor and reperfector are blinded during the generation of a transmitter start signal. This is achieved by open circuiting the blind lead of the receiving distributor through K-716L relay.

5.76 The TP199553 cable assembly connects the protected-unattended transmitter identifier module, the TP146528 automatic answer assembly, the transmitter start switch, and the ac power to the data set. The cable assembly also contains a 2.7K resistor. The resistor connects the +17.5 volt lead and the reverse channel

send lead of a data set. This will generate a continuous reverse channel tone when a reverse channel type of data set is used.

E. Break Feature

5.77 The break feature makes use of the reverse channel feature, on 202C2 and 202D2 Data Sets, for circuit assurance and the break function. This feature is used to stop transmission automatically if circuit continuity is lost. The receiving operator may interrupt transmission for a low tape condition, etc, by pressing the data set TALK button. Sending stations in a customers system that are arranged for the break feature can only transmit to receivers also equipped with this feature.

Note: The addition of a 2700 ohm resistor in the plug connectors to the data set may be required if not present. Also a rearrangement of the connections to terminals 4 and 9 on the sender plug and terminals 9 and 11 on the receiver plug might be required.

TAPE SENDER AND RECEIVER

A. Transmit-Receive Terminal Kit (Early Design)

General

5.78 The transmit-receive terminal modification kit provides a means of connecting a tape sender terminal and a tape receiver terminal (located at the same installation) to a common model 202A or 202B Data Set. This feature allows both terminals to be serviced alternately by one data set.

5.79 Switching of the common data set from one terminal to the other terminal is facilitated by a three-position switch mounted on the front of the tape sender cabinet. Either terminal may be selected to operate with the data set. It is not possible, however, to operate both terminals at the same time. This feature available in kit form (TP146532) for field or factory installation is superseded by TP199610 modification kit.

Detailed Circuit Description

Note: Refer to schematic wiring diagram 4799WD.

5.80 The selector switch mounted on the front of the tape sender cabinet has three positions: TEST, RECEIVE, and SEND. Depending upon which position the switch is in, either the sender or receiver terminal is connected to the data set, or the terminals are tied together for test purposes.

(a) In the TEST position, the interlock signal path is completed to both the sender and receiver terminals and the request-to-send path is completed to the data set, turning on the modulator. In this condition, the sender terminal can transmit to the receiver terminal for local test purposes. The remote control common path to the receiver terminal is also open, disabling the automatic answer feature.

(b) In the RECEIVE position, the interlock signal path is completed to the receiver terminal only, turning on the tape punch and tape winder motors. The request-to-send path to the data set is open, disabling the modulator in the data set. The remote control common path to the receiver is completed, enabling the automatic answer circuit at the receiver terminal.

(c) In the SEND position, the interlock signal path is completed to the sender terminal only, turning on the tape reader and tape winder motors. The request-to-send path to the data set is completed, enabling the modulator. The remote control common path is completed to the sender, enabling the line break and automatic answer feature at the sender terminal.

5.81 For automatic operation, the tape sender line break and automatic answer TEST-OPERATE switch must be in OPERATE position, and the AUTO-MANUAL switch must be in AUTO position. The data set AUTO and DATA pushbuttons must be depressed.

5.82 Until the line break feature is incorporated in the 202A and 202B Data Sets, the tape reader motor and tape winder motor must be manually turned on, and the tape reader manually started. To manually energize these motors, the AUTO-MANUAL switch must be in the MANUAL position. The respective motor switches may then be operated to their ON position. The tape reader is started by first loading the reader with tape, and then operating the RUN-STOP switch in the RUN position.

5.83 Full duplex operation with the 202B Data Set is available when the transmit-receive selector switch is in the TEST position.

B. Send-Receive Terminal Kit (Later Design)

General

5.84 The "Y" connector differs from the old one in that a new Send-Receive (S-R) switch position is added. The test position is retained for use in the following.

(a) Reperforating tapes locally by sending intelligence through the data set and back to its send-receive station.

(b) Full duplex operation on 4-wire facilities. The TP199610 kit replaces the TP146532 cable connector kit.

Theory of Operation

5.85 The TP199620 "Y" cable assembly is used to connect a sender and a receiver together to a common type 202A, B, C or D Data Set. The cable assembly contains the S-R switch, two optional resistors, and two optional straps.

5.86 The S-R switch is a four position rotary switch. The position designations are SEND, RECEIVE, SEND-RECEIVE, and TEST clockwise respectively.

(a) In the SEND position, the terminal will allow manual or unattended send-only operation. In this position the sender terminal is operated by the data set ready lead. The data set send data, request-to-send, ready, and data terminal ready leads are controlled by the sender terminal. The request-to-send lead is controlled by the sender terminal interface lead 4, request-to-send (A/M). This interface lead is used when the sender terminal is operated in the unattended (automatic) or manual modes.

(b) In the RECEIVE position, the terminal will allow manual or unattended receive-only operation. In this position, the receiver terminal is operated by the data set ready lead. The send data, request-to-send, ready, and data terminal ready leads are controlled by the receiver terminal.

(c) In the SEND-RECEIVE position, the terminal will allow unattended send or receive (half-duplex) operation. In this position, the sender and the receiver terminals are operated by the data set ready lead. The send data and request-to-send leads are controlled by the sender terminal. The ready and data terminal ready leads are controlled by the receiver terminal.

(1) The request-to-send lead is controlled by the sender terminals interface lead 14, request-to-send (A). This interface lead is used when the sender terminal is operated in the unattended (automatic) mode.

(2) A data set with a contact interface for automatic answering will automatically answer a call if terminals 20 and 21 of the receiver terminal connector RT are connected together. (The AUTO button of the data set must be

depressed also.) After a call has been answered by a data set, it is necessary for terminals 20 and 21 to remain connected on the receiver terminal connector RT and for terminals 19 and 20 to be connected together on the sender terminal connector ST. This will prevent the data set from dropping a call. At end of transmission, the sender terminal must open the connection between 20 and 21 of the sender terminal connector ST in order to automatically drop a call.

(d) In the TEST position, the terminal will allow terminal testing (two-wire transmission), or manual or unattended send and receive (full duplex) operation (four-wire transmission). In this position, the sender and the receiver terminals are operated by the data set ready lead. The data set send data and request-to-send leads are controlled by the sender terminal. The ready and data terminal ready leads are controlled by the receiver terminal. The request-to-send lead is controlled by the sender terminal interface lead 4, request-to-send (A/M). This interface lead can only be used when a sender terminal permanently applies a request-to-send signal.

5.87 The data set receive data, clear-to-send, signal ground, and ring indicator leads are connected to both sender and receiver terminal connectors ST and RT respectively. The data set carrier detect and reverse channel receive and release are leads connected to the sender terminal connector ST. Because the release lead is connected to the sender terminal only, an automatic disconnect can only be initiated by a sender terminal. The data set reverse channel send lead is connected to the receive terminal connector RT.

5.88 Two optional resistors are provided. They terminate on the S-R switch and are connected to the data set +17.5 volt lead. The R2001 resistor is used to supply a permanent request-to-send when the S-R switch is in the SEND or TEST positions. This resistor is not necessary and must be removed when the sender terminal is equipped with the TP199551 protected-unattended transmitter modification kit. The R2002 resistor is used to supply a permanent reverse channel send and is intended to be optional.

5.89 Two optional straps are provided. They terminate on the S-R switch and are used to provide appropriate receiver terminal blinds. Strap A is used to connect the data set carrier detect lead to the receiver terminal connector RT. This strap must be removed when the sender terminal is equipped with the TP199551 protected-unattended transmitter modification kit. Strap B is used to connect the sender interface lead 13, blind to the receiver terminal interface lead 8, carrier detect. This strap is intended to be optional.

Operating Procedures

5.90 Two-Wire Transmission:

- (a) Manual Operation: Select either SEND or RECEIVE position before or after depressing the DATA button on the data set. It is necessary for the terminals to be in the MANUAL mode of operation.
- (b) Unattended Operation: Select either SEND, RECEIVE, OR SEND-RECEIVE position before depressing the AUTO button on the data set. It is necessary for the terminals to be in the unattended (AUTO) mode of operation.
- (c) Terminal Testing: Select the TEST position before depressing the DATA button on the data set and then engage the reader to transmit. The receiver will monitor the sender terminals transmission under proper data set operation. It is necessary for the terminals to be in the MANUAL mode of operation.

5.91 Four-Wire Transmission:

- (a) Manual Operation: Select the TEST position before depressing the DATA button on the data set. It is necessary for the

terminals to be in the MANUAL mode of operation.

- (b) Unattended Operation: Select the TEST position before depressing the AUTO button on the data set. It is necessary for the terminals to be in the unattended (AUTO) mode of operation.

Test Procedures

5.92 To test the modification kit, it will be necessary for the data test center to call send-receive terminal and check the terminal operations in its various possible modes of operation.

Note: Remove R2001 resistor and strap A (yellow wire) when VS217 and VS219 sender terminals are equipped with a TP199551 protected-unattended transmitter modification kit (7024WD).

C. Local Control Cable Adaptor

General

5.93 The TP326713 local control cable adaptor is only for use with the TP199610 "Y" cable feature. The control cable allows transmission between sender and receiver (back-to-back operation), without placing an on-line call.

Detailed Circuit Description

5.94 With the LOCAL control switch in LOCAL, the AUTO-MANUAL switch in MANUAL, and the rotary switch in the SEND position, the send data lead is opened at the data set and tied to the receive data lead. The carrier detect and reverse channel receive leads are opened at the data set and a positive voltage is applied to both leads to simulate the reverse channel and carrier detect function.