

SPEED TEST CIRCUIT FOR TOUCH-TONE  
AUTOMATIC DIALERS  
SD-1C402-01

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| 1. <u>GENERAL</u>   | 1.3 <u>General Precautions</u>  |
| 1.1 <u>Description</u>  | <u>PRECAUTION 1: PRECAUTIONS DURING WIRING, SOLDERING AND TESTING ELECTRONIC EQUIPMENT ARE CONTAINED IN HANDBOOK 3 SECTION 71 AND MUST BE FOLLOWED AT ALL TIMES WHERE APPLICABLE TO THE OPERATIONS BEING PERFORMED.</u>   |
| 1.11 This section tests the Speed Test Circuit for Touch-Tone Automatic Dialers, SD-1C402-01. The test of the circuit consists of verifying and/or adjusting time intervals and validating the processing of tone signals.  | <u>PRECAUTION 2: WHEN CIRCUIT PACKS ARE REMOVED FOR ANY REASON EXTREME CARE MUST BE USED WHEN REPLACING THE C.P. TO ASSURE THAT THE CARD IS PROPERLY ALIGNED. THE CONNECTING TERMINALS AT THE REAR OF EACH CIRCUIT PACK ARE SOMEWHAT FRAGILE AND SHOULD NEVER BE FORCED INTO POSITION. IF THE CIRCUIT PACK IS PROPERLY ALIGNED IT WILL SLIDE SMOOTHLY INTO THE CONNECTOR WITH A PERCEPTIBLE TENSION AS THE CONNECTOR SPRINGS ARE ENGAGED.</u> |
| 1.12 The Speed Test circuit occupies 2 inches of vertical mounting space on a 23 inch frame. The circuit consists of three plug-in type circuit packs, which insert into connectors mounted on the mounting plate.  | <u>PRECAUTION 3: TO PREVENT THE DESTRUCTION OF CIRCUIT PACKS, POWER MUST BE REMOVED PRIOR TO ENGAGING OR DISENGAGING THE CIRCUIT PACKS WITH THEIR CONNECTORS.</u>   |
| 1.13 The Speed Test circuit is used to test the time interval of digits generated by automatic dialers and card dialers. The digit timer intervals of signal burst time, interdigit time and digit timer intervals of signal burst time, interdigit time and digit period are checked to the above specified minimum times. A closure to ground will be generated as an indication to the connecting circuit that the time interval of the digit under test has been validated. | <u>NOTE: The 21A TMS shall be allowed to warm up for at least 10 minutes before the oscillator is used and should be allowed to warm up for at least one hour before the OSC OUTPUT CAL control is adjusted.</u>  |
| 1.2 <u>Test of Associate Equipment</u>  | 2. <u>RECORDS AND REQUIREMENTS</u>  |
| 1.21 The circuits connecting to this circuit should be tested prior to performing the tests of this section. The connecting circuit which access the Speed Test circuit must be cabled to the Speed Test circuit and then made busy prior to making any tests or adjustments. The make busy procedures for the Touch-Tone Frequency Test Circuit (SD-94813-01) or the Station Ringer Test circuit (SD-1A157-01), as required, shall be followed.                                | 2.1 <u>Records:</u> Forms SD-97-1313 and SD-97-1315 are required for recording the results of these tests. For further information on records refer to Handbook 3, Section 6B.  |
|   | 2.2 <u>Requirements:</u> Tests of this section are based on SD information, CD information, manufacturing test requirements, X-78388, and BSP 201-819-501.  |

3. TEST EQUIPMENT

3.1 Test Sets

<u>Amt</u>	<u>ITE</u>	<u>Description</u>
1	5244	Counter
1	4442A	Volt-Ohmmeter
1	J94021A or 4089	21A TMS

3.2 Cords

<u>Amt</u>	<u>ITE</u>	<u>Cord Lgth</u>	<u>One End</u>	<u>Other End</u>
1	9133	1	1' Tip Plug	Tip Plug
1	9117	1	6' Tip Plug	Min. Allig. Clip
4	9416	1	6' Banana Plug	Banana Plug
1	9723	2	6' 241A Plug	(2) Banana Plugs
1	9430	1	4' KS-14530 Connector	Banana Plug
2	9140L3	1	3' Allig. Clip	Allig. Clip

3.3 Accessories

<u>Amt</u>	<u>Code</u>	<u>Description</u>
1	R-2739	Offset Screwdriver
3	ITE-8507	Alligator Clip
3	ITE-4160	Plug, Solderless

4. FUSING

- 4.1 Remove the screws securing the circuit packs, then Disengage the circuit packs (CP1, CP2 and CP3, from their connectors.
- 4.2 Using an ITE-4442A Volt-Ohmmeter with the "-" lead grounded, verify that all unfused posts on the fuse panel associated with the Test Circuit are free from foreign battery or ground.
- 4.3 Install the fuse associated with the Speed Test Circuit and verify:
- (a) That -48V is present at term 15 of the J2 connector located on the rear of the Speed Test Circuit;
  - (b) That terminals 5, 7, 9 and 11 of the J2 connector are free from -48V, -12V and ground and;
  - (c) That terminal 1 of the J2 connector is ground;

- (d) That -12V (min. -11.4V, max. -12.6V) is present on terminal 13, J2 connector.
- 4.4 Remove the -48V fuse associated with the Speed Test circuit and, using a volt-ohmmeter verify that no crosses exists between terminals 5, 7, 9 and 11 of the J2 connector.
- 4.5 Engage each circuit pack (CP1, CP2 and CP3) with its respective connector.
- NOTE: The Timer Circuit Pack can be distinguished from the Detector Circuit Pack by observing the pin jack designations.
- 4.6 Insert the -48V fuse associated with the Speed Test circuit. Using ITE-4442A verify that the voltages, between the points specified in Table A, are within the specified limits.

TABLE A

<u>-Meter Terminal Connected To</u>		<u>+Meter Terminal Connected To</u>		<u>Potential</u>	
<u>Pin</u>	<u>Connector</u>	<u>Pin</u>	<u>Connector</u>	<u>Min.</u>	<u>Max.</u>
9	J3		Ground	20.9	23.1
11	J3		Ground	17.1	18.9
13	J2	5	J3	5.7	6.7
13	J2	7	J3	4.3	4.7

5. TEST OPERATIONS

- 5.1 Test Setup - Timer
- 5.11 Set the controls of the ITE-5244 Electronic Counter as specified in Table B (if counter is Systron-Donner Model 6150) or Table C (if counter is Fairchild Model 8200).
- NOTE: See Fig. 1 for a diagram of the following connections:
- 5.12 Connect the Counter to the Speed Test circuit per the following:
- (a) Using an ITE-9133 cord, short test jack TS to test jack Y (located on Timer circuit pack).
  - (b) Using an ITE-9117 cord, connect test jack R (located on Detector circuit pack) to frame ground.
  - (c) Connect a Pamona connector to the primary counter input (input A if the Counter is a Fairchild or input B if the Counter is a Systron-Donner).

- (d) Using an ITE-9416 cord equipped with an ITE-4160 plug, connect the signal lead of the primary counter input to test jack TS of the Speed Test circuit. Using an ITE-9416 cord equipped with an Alligator Clip, connect the ground lead of the counter to frame ground.

NOTE: The time measurements made in the following tests will display a 5 digit number on the counter, e.g. a time measurement of 49.50 ms will be displayed as 49500. The display time of the count can be varied by rotating the Recycle Rate, Rotary Switch (Systron Donner), or the Time Base Multiplier, Red Rotary switch (Fairchild).

TABLE B

STEP	OPERATION (SYSTRON - DONNER)
1	Connect power cord to an A.C. outlet.
2	Operate the pushbutton switch, Power, to apply power to counter.
3	Operate the pushbutton switch, Resolution - Time 1 us.
4	Operate the rotary switch, Recycle Rate, to midrange position.
5	Operate the slide switch, Recycle Rate, to Fast position.
6	Operate the select switch, Function, to Time B-C position.
7	Operate the rotary Level switches for Inputs B and C to midrange position.
9	Operate the slide switches, Coupling, for Inputs B and C to AC position.
10	Operate the slide switch, Slope, for Input B to + position.
11	Operate the slide switch, Slope, for Input C to = position.
12	Operate the slide switch, Input Selection, to COM position.
13	At the rear panel of counter, operate the slide switches, Time Base and Std. Freq. Input, to the INT position, also operate the slide switch Storage to the OFF position.
14	Momentarily operate pushbutton switch, Reset.

TABLE C

STEP	OPERATION (FAIRCHILD)
1	At the rear panel, operate the Line Voltage slide switch to the 115 position and then connect the power cord.
2	At the front panel, operate the pushbutton switch, Power, to apply power to counter.
3	Operate the black rotary switch, Function, to Time position.
4	Operate the red rotary switch, Function, to A→B position.
5	Operate the black rotary switch, Time Base Multiplier, to 1 us position.
6	Operate the red rotary switch, Time Base Multiplier, fully counterclockwise then rotate it approximately 1/4 turn clockwise.
7	Operate the slide switch, Memory, to OFF position.
8	Operate the black rotary switches for Trigger Levels A and B to the A.C. X1 position.
9	Operate the red rotary switches for Trigger Levels A and B to midrange position.
10	Operate the slide switch, Slope, for Input A to + position.
11	Operate the slide switch, Slope, for Input B to - position.
12	Operate the rotary switch, Input Selection, to COM position.
13	At the rear panel of the counter, operate the 1 MHz Osc slide switch to the INT OUT position and operate the Fan slide switch to the ON position.
14	Momentarily operate the pushbutton switch, Reset.

5.2 Timer Circuit Pack

NOTE: The R16 potentiometer and the R5 potentiometer (which will be adjusted during succeeding paragraphs) are factory adjusted and normally will require only a minor adjustment. Therefore, if no display or an erroneous display is obtained consult the Trouble Locating Information.

5.21 Observe the counter, verify a time display between 49.48 and 49.52 ms. If this reading is not obtained, adjust the R16 potentiometer on the Timer circuit pack until the proper time display is obtained.

NOTE: Since two types of counters with different input designations can be used, the following notation is utilized to designate the slope settings. "Set the slope switches for "-" to "+"; indicates that the primary input channel shall have a negative (-) slope and the secondary input channel shall have a positive (+) slope. For the Systron-Donner counter input B's slope is "-" and input C's slope is "+". For the Fairchild counter input A's slope is "-" and input B's slope is "+".

5.22 Set the slope switches for "-" to "+". Observe the counter, a time display between 45.48 and 45.52 ms, inclusive, should be indicated. If this reading is not obtained, adjust the R5 potentiometer of the Timer circuit pack until the proper setting is obtained.

5.23 If potentiometers R5 or 16 have been adjusted while proceeding thru Paragraphs 5.21 and 5.22, repeat the operations per Paragraphs 5.21 and 5.22 until both requirements are met.

5.24 Set the slope switches for "-" to "-". Observe the counter, a time display between 94.96 and 95.04 ms, inclusively, should be indicated. If this reading is not obtained, adjust the R5 potentiometer of the Timer circuit pack until the proper setting is obtained.

5.25 Remove the tip plug from the TS test jack and reconnect it to the TBA test jack (located on the Timer circuit pack).

5.26 Set the slope switches for "-" to "+". Observe the counter, a time display between 10.45 and 10.55 ms, inclusively, should be indicated. If this reading is not obtained, adjust the R5 potentiometer of the Timer circuit pack until the proper setting is obtained.

5.27 If potentiometer has been adjusted while proceeding thru Paragraphs 5.24 to 5.26, repeat the operations per Paragraphs 5.21 thru 5.26.

NOTE: If the operations per Paragraphs 5.21 thru 5.26 must be repeated, remove the pin plug from test

jack TBA and reconnect it to test jack TS (located on the Detector Circuit pack).

5.28 Remove the tip plug from the TBA test jack and reconnect it to the OUT test jack (located on the Timer circuit pack). The slope switches are set for "-" to "+" from Paragraph 5.26. Observe the counter, a time display between 31.0 and 35.0 ms, inclusively, should be indicated. The time displayed by the counter should be noted for use in Paragraph 5.5.

5.3 Relay Test

5.31 Disconnect the cord shorting test jack Y to test jack TS.

5.32 Using a Volt-Ohmmeter check for the presence or absence of battery on term 4, J3 connector. If a battery potential is present record the potential for use in Paragraph 5.33. If a potential is not present set the Volt-Ohmmeter to R X1000 scale and record the reading to ground for use in Paragraph 5.33.

5.33 Using an ITE-9133 cord, short test jack TS to test jack Y (located on Timer circuit pack), verify a reading on the Volt-Ohmmeter approx. 2/3 of the reading recorded per Paragraph 5.32.

5.4 Test Setup - Detector

5.41 Set the controls of the 21A Transmission Measuring Set per the following Table.

STEP	OPERATION (21A TMS)
1	Connect the power cord to an A.C. outlet.
2	Operate the ON-OFF switch to the ON position.
3	Set the Frequency for 2000 Hz (FREQ MULT switch to X1000 position and adjust the FREQ control until the range scale indicates a 2).
4	Set the OSC OUTPUT for 0 db. (Rotate both OSC OUTPUT rotary switches to the white 0 positions).

NOTE: See Fig. 2 for a diagram of the following connections.

5.42 Verify that the following connections were not removed:

- (a) Test Jack TS is shorted to Test Jack Y.
- (b) Test Jack R is connected to frame ground.
- (c) The ground lead of the counter's primary input is connected to frame ground.

- 5.43 Using a Pamona connector, two ITE-9416 cords, an ITE-4160 plug and an alligator clip, connect the secondary input of the counter (input C if the Counter is a Systron-Donner; input B if the Counter is a Fairchild) to the Speed Test Circuit, ground lead to frame ground and signal lead to the DRP test jack (located on Detector circuit pack).
- 5.44 Remove the signal lead to the primary counter input from the OUT test jack and connect it to the RP test jack (located on the Detector circuit pack).
- 5.45 Using an ITE-9723 cord, equip the R banana plug with an alligator clip and connect the alligator clip to frame ground, equip the T lead with an ITE-9430 cord and an ITE-4160 plug and connect the tip plug to test jack T (located on the Detector circuit pack), connect the 241A plug to the 21A TMS OSC OUT 600 ohm jack.
- 5.46 Using an ITE-9140 cord, short pin 3, J1 connector to pin 3, J3 connector.

5.5 Detector Circuit Pack

- 5.501 Set the slope switches for "+" to "-". Observe the counter, verify a time display 0 to 3.5 ms longer than the indication recorded in Paragraph 5.28.
- 5.502 Operate the Input Selection switch of the counter to the SEP position.
- 5.503 Set the slope switches for "+" to "+". Observe the counter, verify a time display between 2.5 and 3.5 ms, the time displayed by the counter should be noted for use in Paragraph 5.504.
- 5.504 Set the slope switches for "-" to "-". Observe the counter, the time display should be within .1 ms of the time recorded in Paragraph 5.503.
- 5.505 Disconnect the secondary input of the Counter from the Speed Test Circuit. Remove the cord shorting test jack Y to test jack TS. Remove the short from pin 3, -J1 connector to pin 3, J3 connector.
- 5.506 Remove the pin plug (connected to primary input of the Counter) from the RP test jack and reconnect it to test jack TS (located on the Detector circuit pack).
- 5.507 Operate the Input Selection switch of the Counter of the SEP position.

- 5.508 At the rear of the Speed Test Circuit, ground terminal 6, J1 connector using an ITE-9140 cord.
- 5.509 Momentarily operate the Reset switch (located on the Counter) verify a counter display of 0.
- 5.510 Remove and reinsert the tip plug from test jack T, verify a counter display greater than 200 ms.
- 5.511 At the rear of the Speed Test Circuit remove ground from terminal 6, J1 connector.
- 5.512 Momentarily operate the Reset switch (located on the Counter), verify a counter display of 0.
- 5.513 Remove and reinsert the tip plug from test jack T, verify that no counter display is obtained (Counter display is 0).
- 5.514 Disconnect and secure all test equipment. Restore the connecting circuit, made busy per Paragraph 1.2 to normal.

6. TROUBLE LOCATING

6.1 General

- 6.11 Reference Potentials - The potentials utilized in this circuit with a brief description of their function are contained in Table D.

TABLE D

<u>POTENTIAL</u>	<u>FUNCTION</u>
-12V	Reference level for Operational amplifier and IC's (logic level 0).
-7.5V	Logic level 1 for IC's (+4.5V above reference).
-6V	+6V supply with respect to reference for OpAmps
-18V	-6V supply with respect to reference for OpAmps
-22V	-10V supply with respect to reference for OpAmps

- 6.12 Test Sets - If trouble is encountered when initially using either the counter or the oscillator the test set in question must be verified to insure proper functioning. To perform the verification refer to the TMO or the Instruction Manual for the test set.

6.2 Timer Circuit Pack

6.21 Test and adjustment of the Timer is accomplished by connecting the output of the tone burst, break, and digit checking circuitry to the input of the same circuitry thereby forming a square wave oscillator. The periods of the waveform are controlled by internal timing ramps of the Timer C.P. and are varied by potentiometers R16 and R5.

6.22 The following table lists trouble conditions and their possible causes that can be encountered during tests per Paragraph 5.2.

Trouble Condition	Probable Cause
No counter reading or erroneous counter reading is obtained when performing tests per Para. 5.21.	A) Test leads from the Speed Test Circuit to the counter are reversed. B) Counter switches incorrectly set. C) Test equipment misconnected to the Speed Test Circuit. D) Proper potentials not present on pins 1, 5, 7, 9, 11 and/or 13 of Timer Circuit Pack. E) Detector output is incorrect; remove the test lead from test jack TS to test jack Y, verify approx. -7.5V at test jack TS. F) Defective Timer Circuit Pack
No counter reading or erroneous counter reading when performing tests per Para. 5.22 thru 5.27.	A) Test equipment misconnected to the Speed Test Circuit. B) Defective Timer Circuit Pack.
No counter reading or erroneous counter reading when performing tests per Para. 5.28.	A) SC relay not properly wired. B) Foreign voltage or direct ground present on term. 14, J3 connector. C) Defective Timer Circuit Pack.

Lines presented in Script indicate new or changed information.

ATTACHMENTS

Figures 1 and 2 on Pages 7 and 8.

Reason for Reissue:

To remove reference to Terminal 1 and add reference to ground in 5.508 and 5.511.

6.3 Relay Test

6.31 The Relay Test is accomplished by periodically operating the SC relay from the controlled output pulses of the Timer Circuit Pack.

Trouble Condition	Probable Cause
No counter reading or erroneous reading is obtained when performing tests per Para. 5.33.	A) Lead SCG not grounded. B) Leads SC and SCG misconnected or not connected. C) Relay SC is not properly wired.

6.4 Detector Circuit Pack

6.41 Testing of the Detector Circuit Pack is accomplished by placing a tone (2000 Hz) on the Tip then periodically grounding the Tip, via the controlled operation of relay SC. Thus periodic spurts of tone are placed on the Tip enabling verification of the amplifiers and logic circuitry of the detector.

6.42 The following table lists trouble conditions and their possible causes that can be encountered during tests per Paragraph 5.5.

Trouble Condition	Probable Cause
No counter reading or erroneous reading is obtained when performing tests per Para. 5.51.	A) T lead is grounded. B) Test leads misconnected or controls of test sets incorrectly set. C) Relay SC is incorrectly wired. D) Defective Detector Circuit Pack.

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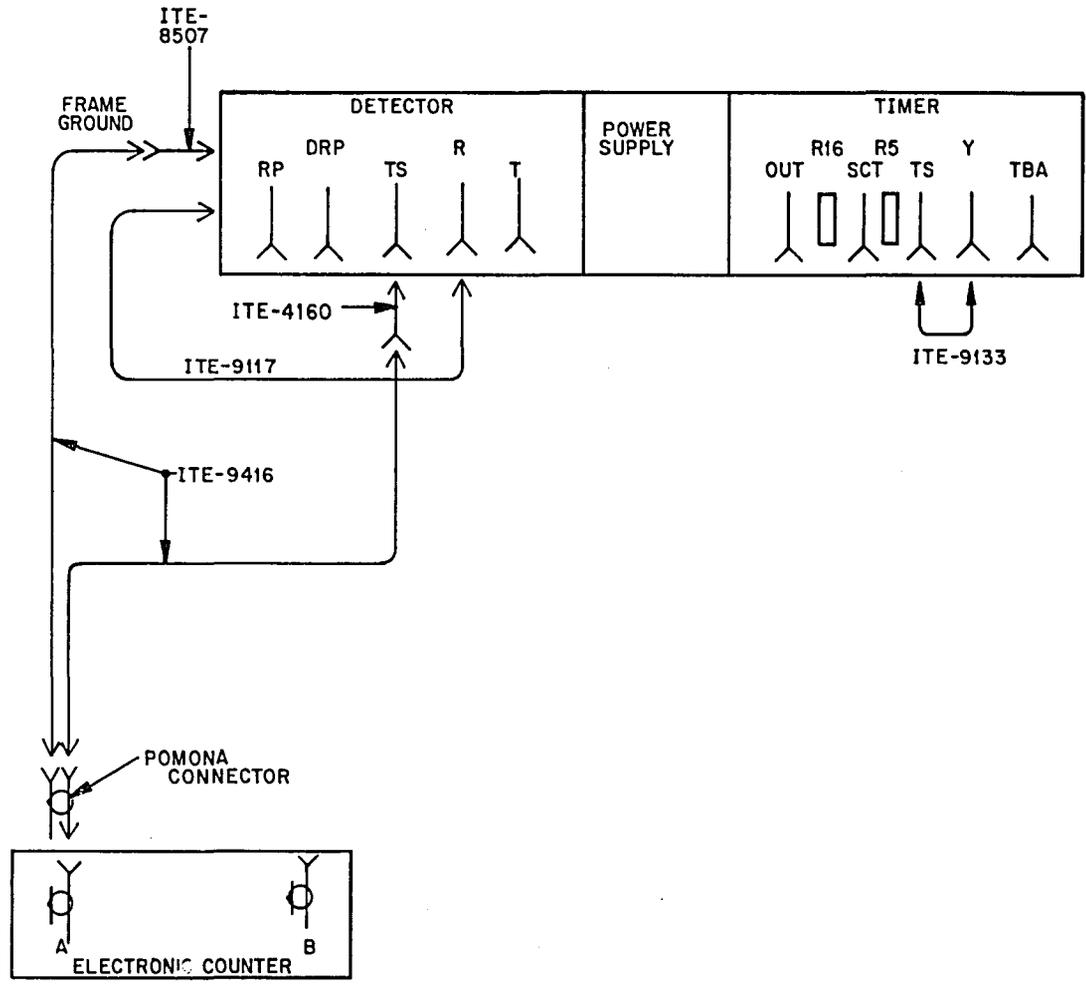


FIG. 1 - TEST CONNECTIONS, TIMER TEST

RP-0605-CB3

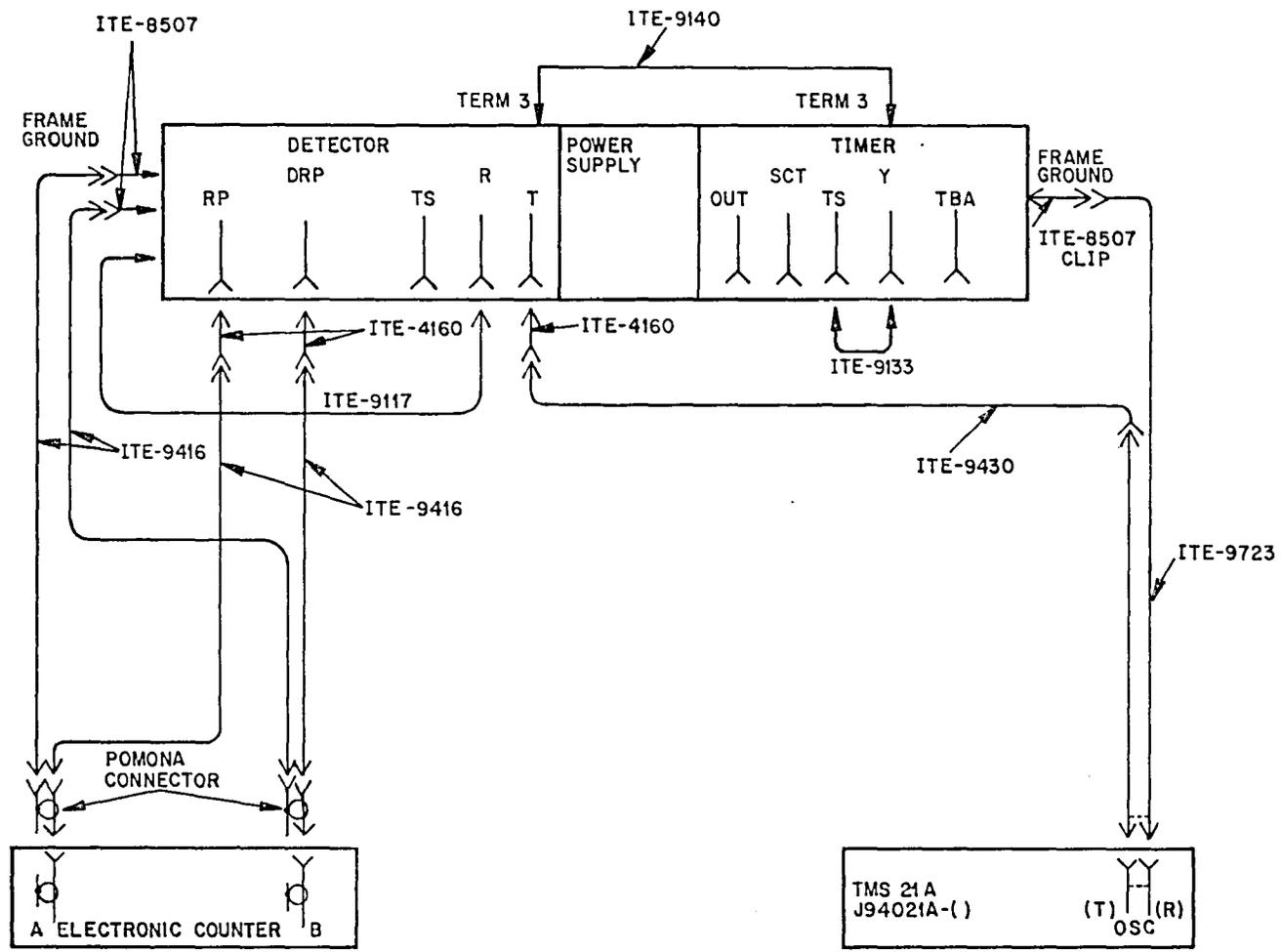


FIG. 2 - TEST CONNECTIONS, DETECTOR TEST

RP-0606-CB3