AMARS
No. 1A AUTOMATIC MESSAGE ACCOUNTING RECORDING SYSTEM
GENERAL INFORMATION

CONTENTS

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1. GENERAL INFORMATION

1.1 This section provides a glossary of terms and provides a list of the PDP11/70 Console switches and lamps with their associated definitions. It also provides a procedure for the removal and replacement of damaged Backplane pins.

2. TEST EQUIPMENT

2.1 Tool Sets

2.11 Tool Set 551 contains the following:

R-4828 Insertion tool for insertion of protruding terminals in Backplane. Ordering No. 134-82800 Comcode No. 402282032

DETAIL 1 Insertion head for protruding terminals inserted through spacer aligner on Backplane with .125 inch spacing. Comcode No. 402384523 Ordering No. 13482801

DETAIL 2 Insertion head for protruding terminals in Backplane with .125 inch spacing. Comcode No. 402384531 Ordering No. 13482802

DETAIL 3 Insertion head for protruding terminals in Backplane with .100 inch spacing. Comcode No. 402384549 Ordering No. 13482803

DETAIL 4 50 terminals type 1D1 without shoulders. Comcode No. 401987219 Ordering No. 134-82804

DETAIL 5 50 terminals type 1B4 with shoulders. Comcode No. 103-055984 Ordering No. 13482805

R-4761 Removal tool for removal of protruding terminals in Backplane. Ordering No. 13476100

3. GLOSSARY

3.1

Absolute (binary) - Machine executable code as magnetized on magnetic tape. For example, a source tape consisting of mnemonic characters (CLR, MOV, etc.) is assembled converting mnemonics into operational codes (absolute binary).

Active ON-LINE processor.

ACU Automatic Calling Unit

Address A binary code which designates the location of a unit of information in a data storage medium (i.e., core memory).

AIC Alarm Interface Circuit

APC AMARC Protocol Converter

baud Unit of signaling speed, usually equal to bit rate.

BCD Binary Coded Decimal; Coding of decimal digit (0-9) to a four position binary number. For example: a) decimal = 9, binary = 1001; b) decimal = 2, binary = 0010.

byte — A group of binary digits usually operated upon as a unit. In the PDP11, 8 bits are contained in one byte, and two bytes are contained in one word.

binary — Number system with string consisting of only Numbers 0 and 1.

bit — A unit of information content having two possible states - 0 or 1 (low or high). Smallest information unit in a register.

BDT — Billing Data Transmitter, replaces the paper tape perforator for AMA or CAMA application.

CAR — Data Set state - carrier signal on.

CDA — Call Data Accumulator; the additions and modifications of a Step-by-Step for the No. 1 AMARS.

CDT — Call Data Transmitter; the additions and modifications of a No. 5 X-BAR office for AMARS.

Channel — Signal path for communications between the remote central office and recording facility (No. 1A AMARC).

CPC — Earlier designation for circuit packs within a specific unit of the Data Set Control and Connection cabinet of the No. 1A AMARC (for corresponding JW number refer to particular schematic drawing).

CPUX-CUX — Central Processor Unit X (PDP 11/70) where X = 0 or 1.

CR — Signal between processor and TTY to perform a carriage return.

CTS — Data Set State - Clear to Send

data — A general term that denotes basic elements of information to be processed or produced by a computer. Usually refers to a group of binary bits representing a code, a character, or a word.

DEC — Digital Equipment Corporation.

DTR — Data Set state - Data terminal ready.

DUC — Dial-up Converter

E.I.A. — Standardized signal level for Data Sets and other terminals: +15 to +5 = HIGH; -15 to -5 = LOW.

ETS — Electronic Translation System

Generic — Software program controlling system operation of the No. 1A AMARC in working (call processing) state.

IOM — Input Output Manual describing TTY messages to and from the processor.

LAMA-C — System that provides Usage Sensitive Pricing in No. 5 Crossbar offices.

LED — Light Emitting Diode.

LF — Signal between processor and TTY to perform a line feed ( ).

MMU — MultiMessage Unit; option of No. 1A AMARC to provide calling and called party information for CDA calls.

MUX,MXPLR,MXPR — The Multiplexer

Octal — Number system where string consisting of Number 0 thru 7.

Off-line — Central processor state where the processor does not control the system (STANDBY).

On-line — Central processor state where the processor does control the system (ACTIVE).

OOS — Out of Service; State of processor where processor is removed from service (or potential service) due to maintenance requirements.

Non-Generic Parameters (NPD) — Specific central office specifications to be stored and used by the Generic program.

PDP11, PDP11/70 — Central processor (minicomputer manufactured by Digital Equip. Corp.)

PTP — Processor to Processor.

ROM — Read Only Memory; A memory device containing programmed (at factory) information. Information normally cannot be written.

RTS — Data Set state - request to send.

RUN — To activate processor and execute the program in memory. RUN lamp on the PDP 11/70 console indicates peripheral data responses have been received. Normally RUN lamp should be lit.

SMU — Single Message Unit; option of No. 1A AMARC providing mainly only calling party information of CDA calls.

STANDBY — Off-Line processor state.

SWR — Switch Register keys on PDP 11 minicomputer's console.

TTL — Transistor Transistor Logic; 0 volt = low, +5 = high.

USER — Modes of operation of the PDP 11/70 processor where certain areas of core memory are not writable (protected) and certain instructions are not executable. The opposite is the Kernel mode where all instructions and memory locations are usable.

VIRTUAL — Virtual address is where the data given is not the direct physical address of a memory word or device, but the 16 bit Virtual Address is used to construct a 22 bit physical address. When a Virtual address is displayed on the ADDRESS DISPLAY lamps, the Virtual lamp will be lit. With Management Option, the Virtual lamp should normally be lit.

VSS — Voice Storage System

WD — Watch Dog; Two bits in the Status Register (SR) of the 1DR11C-SA which when set (1) indicates that a particular processor has halted. Both bits set will trigger the major alarm.

4. CONSOLE SWITCHES AND LAMPS

A. Power Switch

1) OFF - Power to CPU is OFF
2) POWER - Power to CPU is ON and all console switches function normally.
3) LOCK - Power to CPU is ON, but the 7 control switches LOAD ADRS through START are disabled.

B. Address Register Display - These lights are used to show the address of the data being examined or just deposited. The address is a Virtual or Physical Address as determined by the Address Select Switch.

C. Data Register Display - These lights are used to show the 16-bit word just examined or deposited. The PARITY HIGH and PARITY LOW lights indicate the parity bit for the bytes on read operation; on write operations the bits are off. The data interpretation is determined by the DATA SELECT SWITCH.

D. Data Select Switch

1) DATA PATHS - Shows examined or deposited data
2) BUS REG - Internal CPU register for bus cycles
3) MADRS FPP/CPU - ROM address, FPP control microprogram and CPU contol microprogram.
4) DISPLAY REGISTER - Contents of the Display Register.

NOTE: This switch is normally set to the DATA PATHS position.

E. Address Select Switch

1) VIRTUAL - uses a 16-bit Virtual Address; 6 positions for USER, SUPERVISOR, and KERNAL.
2) CONS PHY - uses a 22 bit Physical Address to perform console operations.
3) PROG PHY - displays the 22-bit Physical Address that was generated by the Memory Management Unit.

NOTE: This switch is normally set to the CONS PHY position.

F. Switch Register - Switches used to manually load data or an address into the processor, as determined by the control switches and the Address Select Switch.

G. Control Switches

1) LOAD ADRS - When depressed, the contents of the Switch Register are loaded into the Address Display.
2) EXAM - When depressed the contents of the current location specified in the Address Display are displayed in the DATA Display Register when the Data Select Switch is in the DATA PATHS position.
3) DEP - Raising the switch causes the current contents of the Switch Register to be deposited into the address specified by the current contents of the Address Display.
4) CONT - Depressing the switch causes the CPU to resume execution.
5) ENABLE/HALT - a two position switch used to stop machine execution and to enable the system to run.
6) S/INST-S/BUS CYCLE - switch only affects the operation of the CONT switch. It controls whether the machine stops after instructions or bus cycles.
7) START - If ENABLE/HALT key is ENABLE the START key starts execution; in the HALT position, the START key clears the computer system.

H. Error Lights

1) PAR ERROR - indicates a parity error during a reference to memory.
2) ADRS ERROR - lights to indicate (a) reference of nonexistent memory; (b) access control violation; (c) reference of unassigned memory pages.

I. Processor State Lights

1) RUN - CPU is executing program instructions.
2) PAUSE - CPU is inactive because the current instruction execution has been completed as far as possible.
3) MASTER - CPU is in control of the UNIBUS.
4) USER - CPU is executing instructions in USER mode.
5) SUPER - CPU is executing instructions in SUPERVISOR mode.
6) KERNAL - CPU is executing instructions in KERNAL mode.
7) DATA - indicates whether last memory reference to D address space or I address space in current CPU mode.

J. Mapping Lights

1) 16 Bit - lights when CPU is using 16-bit mapping.
2) 18 Bit - lights when CPU is using 18-bit mapping.
3) 22 Bit - lights when CPU is using 22-bit mapping.

K. Lamp Test - When raised, all console indicator lights should go on.

5. BACKPLANE REPAIRS

NOTE: Before making any physical repairs to a Backplane, remove all power from that section of the Backplane and all wires from the damaged pin. Also, if a circuit pack is plugged onto that pin, remove it.

5.1 Tools and Terminals

5.11 One R-4828 Insertion tool and one R-4761 Removal tool are required for removing and adding terminals in a Backplane.

5.12 Two types of pressfit terminals are furnished. These are furnished (50 each) in Tool Set 551 or can be ordered separately using the Ordering No. 13482804 for 50 1D1 shoulderless terminals or Ordering No. 13482805 for 50 1B4 shouldered terminals.

5.13 The R-4760 Insertion tool with an insertion head screwed on is shown in Figure 1. This tool is used with three different Insertion heads Details 1, 2, and 3 (see Figure 1). Detail 1 head is used to insert pins through a spacer aligner on a Backplane with pin spacings of .125 inch. Detail 2 head is used to insert pins in Backplanes with pin spacings of .125 inch. Detail 3 head is used to insert pins in Backplanes with pin spacings of .100 inch.

NOTE: Shouldered pins must be inserted from the front of the Backplane, the side that the circuit packs plug into.

5.14 The R-4761 Removal tool is shown in Figure 2. This tool comes equipped with the removal head.

5.15 The two types of pressfit terminals can be identified by the presence or absence of a shoulder. The shoulder consists of a pair of wings on two sides of the pin next to the pin's pressure spring. The 1D1 does not have a shoulder (see Figure 3) and the 1B4 has a shoulder (see Figure 4).

5.2 Terminal Replacement Procedure

5.21 To remove a pin that is broken or too badly bent to straighten properly, insert the barrel of the R-4761 removal tool over the nonshouldered end of the pin as shown in Figure 5. There will be approximately 1/4 inch between the bottom of the barrel and the backplane.

5.22 Push the handle of the removal tool toward the backplane until the spring latch inside the tool releases the pressure spring. About two or three strokes with the tool is enough to remove the pin from the backplane.

5.23 To remove a shouldered pin that is broken on the nonshouldered end, use another pin to push the broken pin out from the nonshouldered end, or carefully pull the pin out with a pair of pliers. A broken nonshouldered pin can be pushed out using another pin.

5.24 To replace the pin, select the same type of pin that was removed from the backplane. Insert the pin in the center hole on the head of the insertion tool.

5.25 Turn the pin so that the slot in the pin faces the same direction as the cutout section on the head on the insertion tool as shown in Figures 6 and 7.

NOTE: Shouldered pins must be inserted from the front of the backplane only, the side that the circuit packs plug into.

5.26 Start the end of the new pin in the hole on the backplane. Align the existing pin on the left and on the right of the backplane into the two holes in the head of the insertion tool.

5.27 Push the new pin into the hole until it stops sliding freely.

5.28 Holding the insertion straight, carefully push the handle of the insertion tool toward the backplane until the spring latch inside the tool releases the pressure spring.

5.29 About two or three strokes with the tool should be enough to insert the pin properly. The end of the head of the insertion tool should rest against the back of the backplane (see Figure 8).

6. ELECTRO-STATIC DISCHARGE

6.1 Circuit Pack Handling

6.11 Experiments indicate that minimal static energy is transferred when the ground frame is touched (discharging oneself) prior to handling a circuit pack.

No changes are indicated due to extensive revision.

ATTACHMENTS
Figures 1 thru 8 on Pages 6 thru 7.

Manager, Product Engineering
Control Center

Reason for Reissue:
Addition of Backplane Pin replacement procedures.

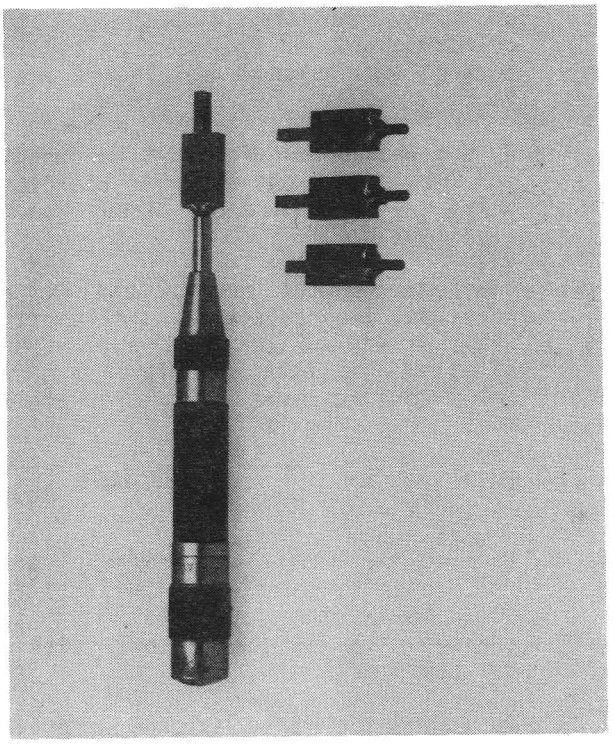


FIGURE 1

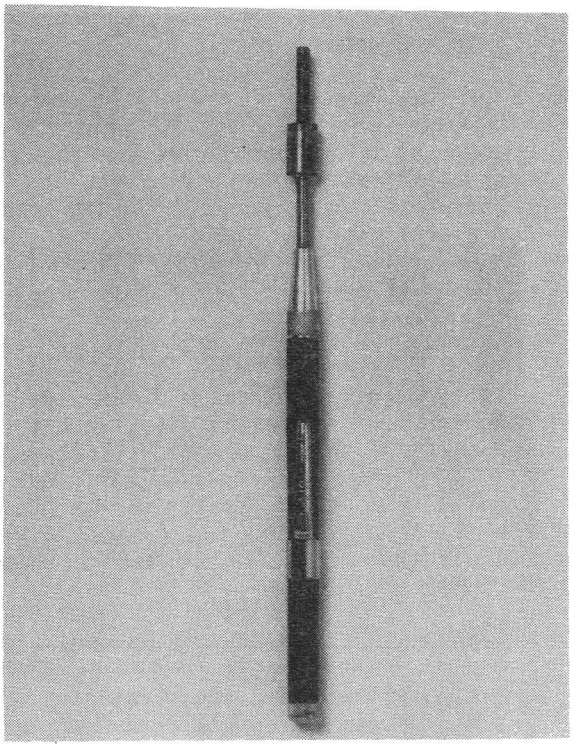
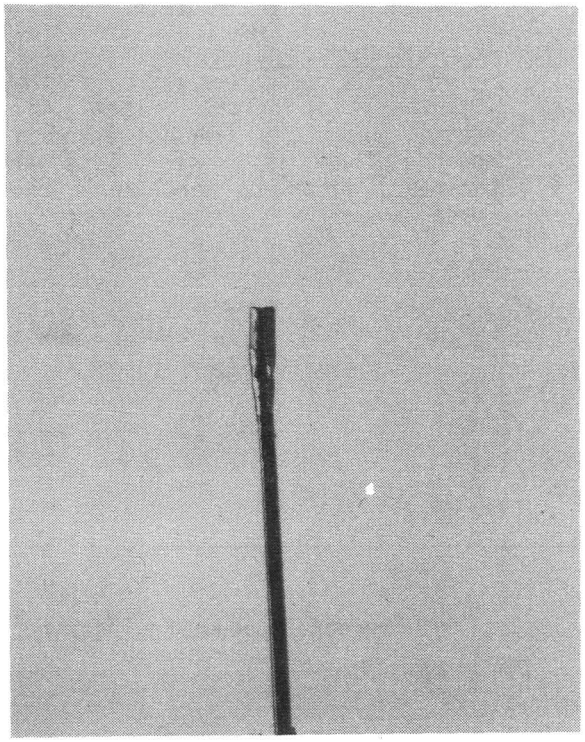


FIGURE 2



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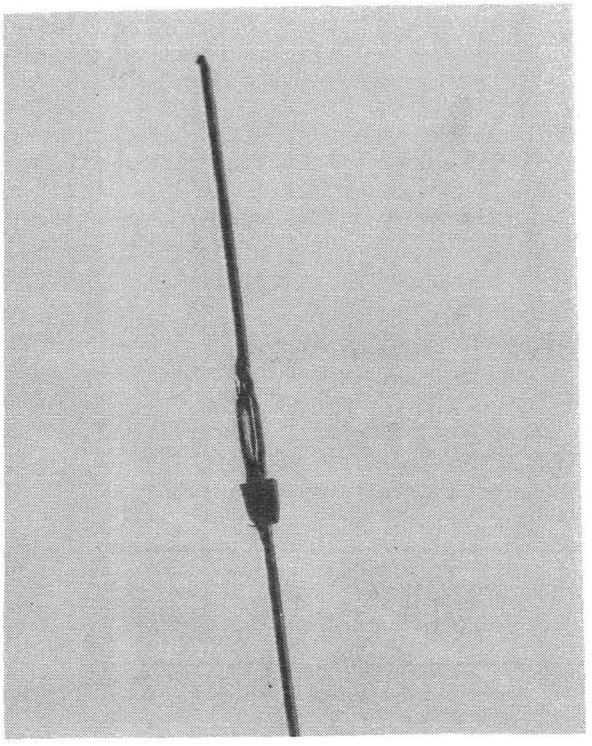

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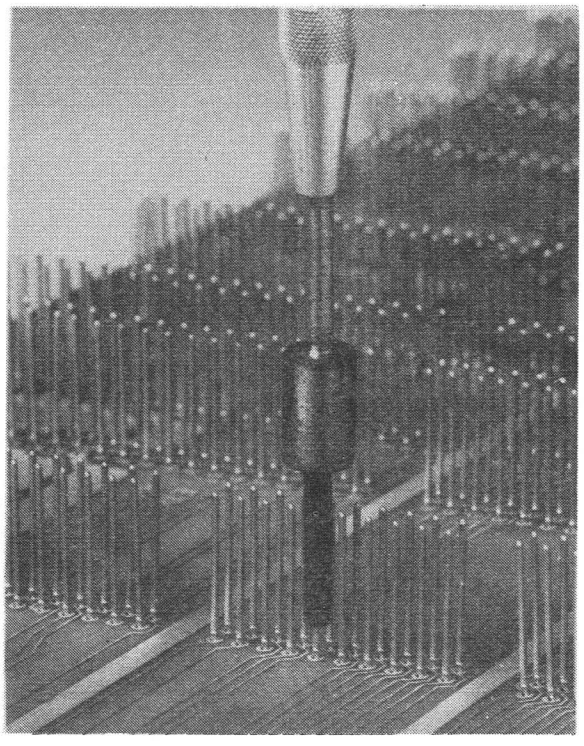

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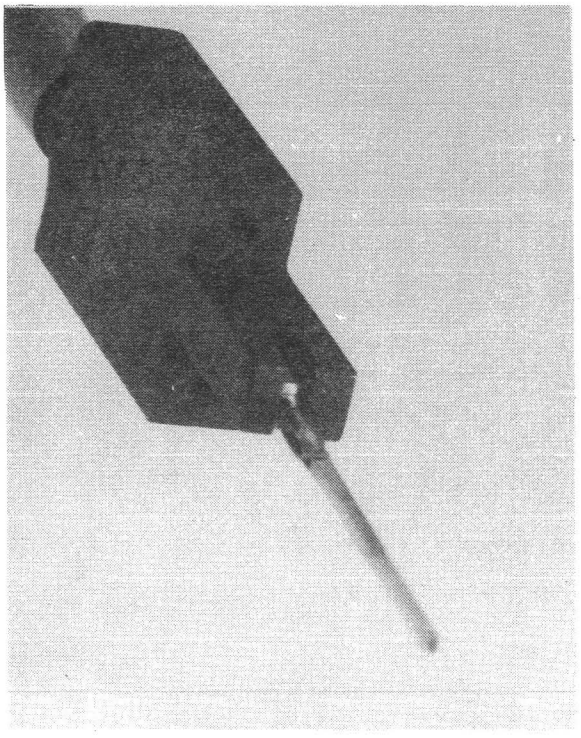
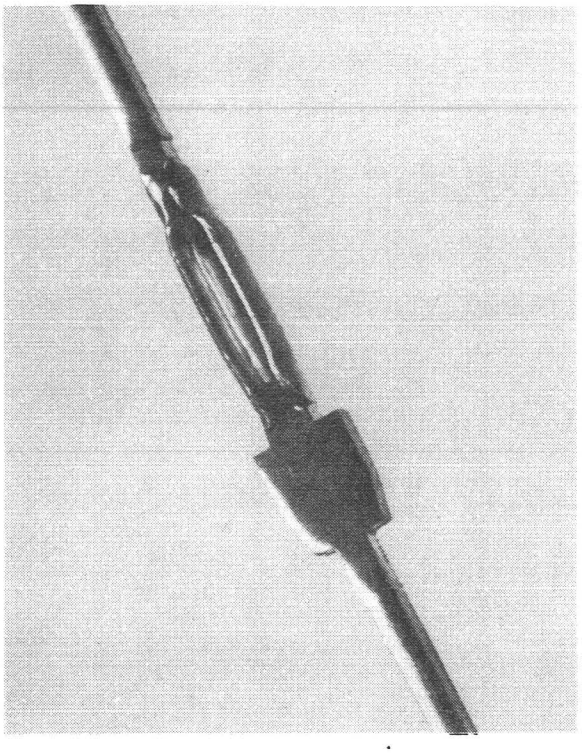


FIGURE 6



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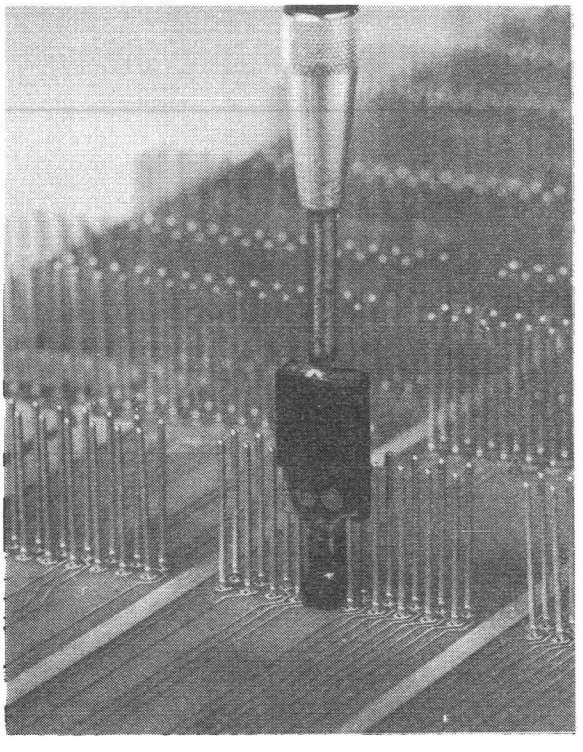

FIGURE 8