AMARS
NO. 1A AUTOMATIC MESSAGE ACCOUNTING RECORDING CENTER PROCESSOR INTERFACE CABINET INSTALLATION (J1P040D) (INITIAL NO. 1A AMARC INSTALLATIONS ONLY)

CONTENTS

1. GENERAL INFORMATION

1.1 The processor interface cabinet contains Alarm and Control Unit (ALM) (SD-5P013-01) (J1P040DF), Alarm and Control Unit (CONT) (SD-5P013-01) (J1P040DB), 0 ACU Interface Unit (0 ACU) (SD-5P015-01) (J1P040DD), Isolation Pulse Unit (PULSE) (SD-5P020-01) (J1P040DE), Power Transfer and Static Filter Unit (OPWR/FLT) (J1P040DG), and Power Supply.

1.2 Refer to ED5P285 for cable dress information.

1.3 Refer to SD-5P012-01 for connector to backplane pin number conversions.

1.4 The installation and tests of this cabinet should be completed before proceeding to Section 204E, 204F, and 204G.

1.5 Disregard the lighting of LEDs on circuit packs unless specified in this handbook section. Handbook 59, Section 204H will be used to verify proper illuminations of all untested LEDs.

1.6 The ends of all cables going to the DN11's should not be connected to the DN11's in the CPU's, at this time. Temporarily these cable ends will be run to the J1P040V-1, List 1 cabinet to enable ACU interface testing in a later handbook section. These cable ends will be connected to the DN11's in the CPU's in a later handbook section.

1.7 This Handbook section is not to be used for installing a J1P040D cabinet to an existing live billing No. 1A AMARC. The Generic 2 to Generic 3 Retrofit Procedure Handbook sections, contain the necessary information for installing a J1P040D cabinet to an existing live billing No. 1A AMARC.

2. RECORDS AND REQUIREMENTS

2.1 The Test Trouble Record forms (SD-97-1313 and SD-97-1315) should be used to record all troubles which are encountered when running the tests in this handbook section.

3. TEST EQUIPMENT

3.1 One ITE-5632 Digital Multimeter (or equivalent).

3.2 SPP-832 Spare Packs Package.

4. INSTALLATION OF THE CABINET

4.1 The Processor Interface Cabinet should be positioned in accordance with floor plan data requirements (FPD 824-100-105-1).

4.2 The uninterruptable power supplies (UPS) should have been installed and tested. Each UPS provides power to one complete side of the AMARC. Verify that the output voltage at each outlet for each phase in 120 VAC. Measure voltage between phase and neutral leads.

4.3 The data sets associated with the No. 1A AMARC are housed in their own separate cabinet. The 202T data sets are housed by 40B1 mountings. The 202S and 212A data sets and the 801C automatic dialing units are housed in a 40A2 mounting. The 829A data auxiliary data sets are housed by 46A1 data mountings. These are installed and maintained by the telephone company.

5. CABLING

NOTE: In connecting the ED-5P284-31 cables to the male connector on a DEC circuit board, the triangle on the cables (female) connector should be inserted to mate with the "A" designation on the circuit board. When connecting to the backplane, the triangle should always be on the bottom.

5.1 Remove power by turning the ON/OFF switch on both programmer's console to the OFF position.

5.2 Connect the following interframe cables from Table 1 (ED-5P284-31) between the Processor Interface Cabinet and Processor 0. (See cabling NOTE under Paragraph 5.)

5.3 Connect the following interframe cables from Table 2 (ED-5P284-31) between the Processor Interface Cabinet and Processor 1. (See cabling NOTE under Paragraph 5).

5.4 Restore power by turning the ON/OFF switch on both processor's console to the ON position.

6. FUSE AND POWER

6.1 Power Transfer Unit

6.101 Power for the Processor Interface Cabinet is supplied by the Power Transfer Unit. The Power Transfer Unit obtains power from a single-phase receptacle at the power distribution circuit. J0 and J1 receptacles on the unit receive plugs from the power strip within the cabinet. Do not connect power to the Power Transfer Unit until specified in the following paragraphs.

6.102 Remove all plugs from outlets on both sides of the Processor Interface Unit.

TABLE 1

DESIG.	GROUP	STAMPED	CONNECTED FROM LOC.	CONNECTED FROM UNIT	CONNECTED TO	STAMPED
** CB29-0	74	OPWR/FLT 02-090	(Note 1) 02-090	OPWR/FLT	SYSTEM CONSOLE 0	ALERTING TTY 0
CB40-0	51	OACU 06-017	06-017	OACU	NOTE 2	CPU0 00DN11
CB41-0	51	OACU 10-017	10-017	OACU	NOTE 2	CPU0 01DN11
CB42-0	51	OACU 06-049	06-049	OACU	NOTE 2	CPU0 02DN11
CB43-0	51	OACU 10-049	10-049	OACU	NOTE 2	CPU0 03DN11
CB44-0	52	OACU 06-085	06-085	OACU	NOTE 2	CPU0 04DN11
CB45-0	52	OACU 10-085	10-085	OACU	NOTE 2	CPU0 05DN11
CB46-0	52	OACU 06-117	06-117	OACU	NOTE 2	CPU0 06DN11
CB47-0	52	OACU 10-117	10-117	OACU	NOTE 2	CPU0 07DN11
* CB20-0	58	ALM 02-060	02-060	ALM	TRMT DMC11MA	CPU0 DMC11-TRMT
* CB21-0	58	ALM 02-044	02-044	ALM	RCV DMC11MA	CPU0 DMC11-RCV
-	-	NOTE 3	02-016	ALM	DL11WB	NOTE 3
CB30-0	52	ALM 10-027	10-027	ALM	DR11C-TTY CONN. 2	CPU0 DR11C-TTY CONN. 2
CB31-0	52	ALM 06-027	06-027	ALM	DR11C-TTY CONN. 1	CPU0 DR11C-TTY CONN. 1
CB35-0	52	CONT 24-021	24-021	CONT	0DR11C-SA CONN. 2	CPU0 0DR11C-SA CONN. 2
CB36-0	52	CONT 20-021	20-021	CONT	0DR11C-SA CONN. 1	CPU0 0DR11C-SA CONN. 1
CB37-0	52	CONT 24-027	24-027	CONT	1DR11C-SA CONN. 2	CPU0 1DR11C-SA CONN. 2
CB38-0	52	CONT 20-027	20-027	CONT	1DR11C-SA CONN. 1	CPU0 1DR11C-SA CONN. 1

* COAXIAL Cable
** M25A Cord

Note 1: Conn 'T' on CP(SH11)
Note 2: Do not connect this end of the cable to the DN11. Instead, temporarily run this cable to the J1P040V-1, List 1 cabinet and leave unconnected. Connection to be covered in a later handbook section.
Note 3: DEC Part No. BC05C-50 cable.

TABLE 2

DESIG.	GROUP	STAMPED	CONNECTED FROM LOC.	CONNECTED FROM UNIT	CONNECTED TO	STAMPED
** CB29-1	74	OPWR/FLT 02-098	(Note 1) 02-098	OPWR/FLT	SYSTEM CONSOLE 1	ANALYSIS TTY 1
CB40-1	53	OACU 06-033	06-033	OACU	NOTE 2	CPU1 00DN11
CB41-1	53	OACU 10-033	10-033	OACU	NOTE 2	CPU1 01DN11
CB42-1	53	OACU 06-065	06-065	OACU	NOTE 2	CPU1 02DN11
CB43-1	53	OACU 10-065	10-065	OACU	NOTE 2	CPU1 03DN11
CB44-1	53	OACU 06-101	06-101	OACU	NOTE 2	CPU1 04DN11
CB45-1	53	OACU 10-101	10-101	OACU	NOTE 2	CPU1 05DN11
CB46-1	53	OACU 06-133	06-133	OACU	NOTE 2	CPU1 06DN11
CB47-1	53	OACU 10-133	10-133	OACU	NOTE 2	CPU1 07DN11
* CB20-1	59	ALM 02-124	02-124	ALM	TRMT DMC11MA	CPU1 DMC11-TRMT
* CB21-1	59	ALM 02-108	02-108	ALM	RCV DMC11MA	CPU1 DMC11-RCV
-	-	NOTE 3	02-080	ALM	DL11WB	NOTE 3
CB30-1	52	ALM 10-095	10-095	ALM	DR11C-TTY CONN. 2	CPU1 DR11C-TTY CONN. 2
CB31-1	52	ALM 06-095	06-095	ALM	DR11C-TTY CONN. 1	CPU1 DR11C-TTY CONN. 1
CB35-1	53	CONT 24-089	24-089	CONT	0DR11C-SA CONN. 2	CPU1 0DR11C-SA CONN. 2
CB36-1	53	CONT 20-089	20-089	CONT	0DR11C-SA CONN. 1	CPU1 0DR11C-SA CONN. 1
CB37-1	53	CONT 24-095	24-095	CONT	1DR11C-SA CONN. 2	CPU1 1DR11C-SA
CB38-1	53	CONT 20-095	20-095	CONT	1DR11C-SA CONN. 1	CPU1 1DR11C-SA

* COAXIAL Cable
** M25A Cord

Note 1: Conn 'T' on CP (SH11)
Note 2: Do not connect this end of the cable to the DN11. Instead, temporarily run this cable to the J1P040V-1, List 1 cabinet and leave unconnected. Connection to be covered in a later handbook section.
Note 3: DEC Part No. BC05C-50 cable.

6.103 Disengage all circuit packs in the Control Unit (J1P040DB), Alarm Unit (J1P040DF), ACU Interface Unit (J1P040DD), Isolation Pulse Unit (J1P040DE) and the Power Transfer and Static Filter Unit (J1P040DG).

6.104 Verify that 'PWR Cord 0' is connected from the receptacle 1 on the side 0 power strip to the J0 outlet on the Power Transfer Unit.

6.105 Verify that 'PWR Cord 1' is connected from the receptacle 1 on the side 1 power strip to the J1 outlet on the Power Transfer Unit.

6.106 Connect the power cord P0 from the Power Transfer Unit to the receptacle for the Processor Interface Cabinet associated with CPU0. Verify that the pilot lamp at the top of both power strips is illuminated. If the pilot lamps are not illuminated, depress the circuit breaker button on top of the associated power strip. Verify that 120VAC is obtained at all outlets on both sides of the Processor Interface Cabinet.

6.107 Remove the AC0 fuse. Verify that 120 VAC has been removed from all outlets on side 0 of the Processor Interface Cabinet. Side 1 side should still retain power.

6.108 Remove power cord P0 from the receptacle.

6.109 Restore the AC0 fuse.

6.110 Connect power cord P1 to the receptacle for the Processor Interface Cabinet associated with CPU1. Verify that 120 VAC is obtained at all outlets on both sides of the Processor Interface Cabinet.

6.111 Remove the AC1 fuse. Verify that 120 VAC has been removed from all outlets on side 1 of the Processor Interface Cabinet. Side 0 should still retain power.

6.112 Restore the AC1 fuse.

6.113 Restore power cord P0 to the receptacle for the Processor Interface Cabinet associated with CPU0.

6.2 Fuse and DC Power

6.201 Remove fuses A0, B0, C0, D0, E0, F0, A1, B1, C1, D1, E1 and F1.

6.202 Verify that all fuses for the 0 PWR SUPP power supply at the top of the frame are in place.

6.203 Connect the plug from the 0 PWR SUPP power supply for side 0 to outlet 16 on side 0.

6.204 Connect the plug from the 0 PWR SUPP power supply for side 1 to outlet 16 on side 1.

6.205 Connect the plug from the +28v power supply PS0 located in the PULSE Unit to outlet 4 on side 0.

6.206 Connect the plug from the +28v power supply PS1 located in the PULSE unit to outlet 4 on side 1.

6.207 Operate both power switches on the 0 PWR SUPP power supply to the ON position.

6.208 Verify that no power on ground conditions exist on any of the +5v, +12v or -12v terminals of TB1 and TB3. Refer to SD-5P012-01, FS3 if necessary.

6.209 Insert an operated fuse, one at at time, into the fuse holder, listed in Table A, and observe that the associated LED indicator, listed in Table A, illuminates.

TABLE A

SIDE 0		SIDE 1	
FUSE HOLDER	LED	FUSE HOLDER	LED
A0	+5V0	A1	+5V1
C0	+12V0	C1	+12V1
D0	+12V0	D1	+12V1
E0	-12V0	E1	-12V1
F0	-12V0	F1	-12V1

6.210 Restore all fuses that were removed in Paragraph 6.201.

6.211 Use the Digital Voltmeter to adjust the +12v, -12v and +5v outputs of the 0 PWR SUPP power supply as accurately as possible. Verify these voltages at the terminals given in Table B. Refer to SD-5P012-01, FS3 if required.

TABLE B

VOLT	RANGE	SIDE	LOCATION	TERMINAL
+5	4.75v to 5.25v	0	TB2	1
+5	4.75v to 5.25v	1	TB4	1
-12	-11.4v to -12.6v	0	TB2	3
-12	-11.4v to -12.6v	1	TB4	3
+12	+11.4v to +12.6v	0	TB2	2
+12	+11.4v to +12.6v	1	TB4	2

NOTE: Output voltages must be adjusted as accurately as possible to +5v and +12v. There is an adjustment potentiometer on the 0 PWR SUPP supply that can be used for adjustments.

6.212 Verify +28v ±2v is obtained by measuring between the +28 V0 and +28 RT0 bugs on PULSE unit side 0 and between the +28 V1 and +28 RT1 bugs on PULSE unit side 1, located on the backplane of the PULSE unit. Refer to SD-5P020-01, FS3 if necessary.

6.213 Verify that power is supplied to both sides of all units within the Processor Isolation Cabinet. Refer to Table C for available voltages on specific units. Verify between the voltage bug and the GND bug.

Table 3

UNIT	VOLTAGE	LOCATION
CONT	+5v	+5v BUG
CONT	+12v	+12v BUG
CONT	NC	-12v BUG
ALM	+5v	+5v BUG
ALM	+12v	+12v BUG
ALM	-12v	-12v BUG
OACU	+12v	+12v BUG
OACU	-12v	-12v BUG
PULSE	+12v	+12V0 and +12V1
PULSE	NC	-12v BUG
PULSE	+5v	+5V0 and +5V1

6.214 Turn the two power switches on the 0 PWR SUPP power supply to the OFF position. Remove the plug for the +28v power supplies from outlet 4 on both sides. Insert all circuit packs in the Control Unit (J1P040DB), Alarm Unit (J1P040DF), ACU Interface Unit (J1P040DD), Isolation Pulse Unit (J1P040DE) and the Power Transfer and

Static Filter Unit (J1P040DG). Restore power using the two switches on the 0 PWR SUPP power supply and re-insert the +28v power supply plugs.

6.215 Control Console (J1P040E) for CPU0 should be powered from outlet 5 on side 0.

6.216 Control Console (J1P040E) for CPU1 should be powered from outlet 5 on side 1 only when a J1P040V-1 cabinet is not furnished.

6.217 Remove the F1 fuse located on the SN3 circuit pack in the PULSE unit one at a time and verify that the associated PWR ON LED extinguishes. Restore the F1 fuses.

7. POWER TRANSFER TEST

7.1 Remove power cord P0 from the receptacle for the Processor Interface Cabinet associated with CPU0.

7.2 Observe that the TRNSFR0 LED illuminate on the SH9 circuit pack located in the OPWR/FLT unit.

7.3 Restore power cord P0. The TRNSFR0 LED should extinquish.

7.4 Remove power cord P1 from the receptacle for the Processor Interface Cabinet associated with CPU1.

7.5 Observe that the TRNSFR1 LED illuminate on the SH9 circuit pack located in the OPWR/FLT unit.

7.6 Restore power cord P1. The TRNSFR1 LED should extinquish.

8. POWER SUPPLY FAILURE TEST

8.1 Verify that the ACFL0 and ACFL1 LEDs on the SH9 circuit pack in the OPWR/FLT unit are extinquished.

8.2 Operate the power switch on the 0 PWR SUPP associated with side 0 to the 'OFF' position.

8.3 Verify that the ACFL0 LED on the SH9 circuit pack in the OPWR/FLT unit illuminates.

8.4 Restore the power switch on the 0 PWR SUPP to the 'ON' position. The ACFL0 LED should extinquish.

8.5 Operate the power switch on the 0 PWR SUPP associated with side 1 to the 'OFF' position.

8.6 Verify that the ACFL1 LED on the SH9 circuit pack in the OPWR/FLT unit illuminates.

8.7 Restore the power switch on the 0 PWR SUPP to the 'ON' position. The ACFL1 LED should extinquish.

Manager, Product Engineering
Control Center

Reason for Reissue
To include UIS information.