AMARS
NO. 1A AUTOMATIC MESSAGE ACCOUNTING RECORDING CENTER
FUNCTIONAL ISOLATION CONTROL
GENERIC III
(INITIAL INSTALLATIONS ONLY)

CONTENTS

1. GENERAL INFORMATION

1.1 This section will functionally test the isolation capability of the J1P040D, J1P040V-1, List 1, and J1P040V-1, List 2, cabinets under the control of the Main Alarm Display Unit.

1.2 The installation and tests of Sections 204D, 204E, 204F, and 204G should be completed before proceeding with this section.

1.3 Both CPU's, the J1P040D-1, the J1P040V-1, List 1 (if provided), the J1P040V-1, List 2 (if provided), cabinets should all be powered up.

1.4 SD-5P006, SD-5P012 through SD-5P016 and SD-5P020 should be available for possible reference in this section.

1.5 The tests in this Handbook Section are only to be executed on new No. 1A AMARC installation.

2. RECORDS AND REQUIREMENTS

2.1 The Test Trouble Record forms (SD-97-1313 and SD-97-1315) should be used to record all troubles which are encountered when running the tests in this handbook section.

3. TEST EQUIPMENT

3.1 One ITE-5632 Digital Multimeter (or equivalent).

3.2 SPP-832 Spare Packs Package

4. INITIAL STATUS

4.1 With the HALT/ENABLE switch on both processor's consoles in the HALT position, depress the START switch on both processor's consoles.

4.2 Verify that the Main Display and Control Panel have the LEDs illuminated for "PROGRAM TIMEOUT" and 'NORMAL' for both processors and Critical alarm. The same indications should be present on the Auxiliary Alarm and Display Panel, if provided.

4.3 If audible alarms are sounding, depress the appropriate cutoff button on the Main Display and Control Panel. Retire alarms as necessary throughout the tests in this section.

4.4 Lamp Test

4.41 Depress the TEST LAMPS & AUDIBLE button on the Main Alarm Control and Display Panel. All lamps on the Main Alarm Control and Display Panel in addition to all "FAULT" lamps on all circuit packs with "FAULT" lamps should light; also, the audible alarm should sound. The original lamp display on the Auxiliary Alarm and Display Panel, if provided, should not change state.

4.42 Depress the TEST LAMPS & AUDIBLE button on the Auxiliary Alarm and Display Panel, if provided. All lamps on the Auxiliary Alarm and Display Panel in addition to all "FAULT" lamps on all circuit packs with "FAULT" lamps should light; also the audible alarm should sound. The original lamp display on the Main Alarm Control and Display Panel should not change state.

5. LOAD TEST PROGRAM

5.1 A small program must be entered into both CPUs. The following procedure should be used in entering the program into one of the CPUs. When one CPU has been loaded with the program, repeat the procedure in the other CPU.

5.11 At the processor console verify that the HALT/ENABLE key is in the HALT position.

5.12 On the switch register (SWR), toggle in an octal 1000, then depress LOAD ADDRESS. Address 1000 should be displayed in the address lamps on the CPU console.

5.13 Toggle in the first instruction code Table 1 into the SWR, then depress the DEPOSIT key. Note that the address displayed on the address lamps on the CPU console has automatically been incremented by 2.

5.14 Toggle in the next instruction code from Table 1 into the SWR, then depress the DEPOSIT key. Note that the address lamps on the CPU console have again incremented by 2.

5.15 Repeat Paragraph 5.14 until all instruction codes in Table 1 have been inserted into memory.

5.16 Toggle into the SWR an octal 1000, then depress the LOAD ADDRESS key. Depress the EXAMINE key and verify that the data displayed in the data lamps match with the instruction code and address listed in Table 1.

5.17 Depress the EXAMINE key and verify that the next instruction code from Table 1 is displayed in the DATA LAMPS.

5.18 Repeat Paragraph 5.17 until all addresses and instruction codes from Table 1 have been verified.

5.2 After the test program has been entered and verified in both CPUs, start the execution of the test program.

5.21 Load address 1000 into the SWR and depress the LOAD ADDRESS key on CPU0.

5.22 Restore all SWR keys to the zero position on CPU0.

5.23 Restore the ENABLE/HALT key on CPU0 to the ENABLE position.

5.24 Depress the START key on CPU0. The program should now be executing.

5.25 Repeat Paragraphs 5.21 through 5.24 on CPU1.

5.3 The red 'PROGRAM TIMEOUT' LED's for both CPU's should extinquish on the Main Alarm Control and Display Panel and also on the Auxiliary Alarm and Display Panel (if provided).

TABLE 1

ADDRESS	INSTRUCTION OCTAL CODE
1000	005037
1002	167730
1004	012700
1006	177777
1010	005300
1012	001376
1014	013737
1016	177570
1020	167732
1022	005237
1024	167730
1026	012700
1030	177777
1032	005300
1034	001376
1036	000137
1040	001000

6. ISOLATION AND ALARM TESTING

6.1 General

6.11 Table 2 contains the value which should be entered into the SWR for a particular step. Do not change the SWR setting until the next step. Table 3 contains the expected response in the J1P040D-1 cabinet. Table 4 contains the expected response in the J1P040V-1, List 1 Cabinet, if provided. Table 5 contains the expected response in the J1P040V-1, List 2 Cabinet, if provided.

6.12 The PROCESSOR, INTERFACE, ISOLATION OVERRIDE switches and the EXECUTE button are located on the Main Alarm Control and Display Panel. To put the system into a particular state, the appropriate switch is operated; then the EXECUTE button will be depressed; then the switch and EXECUTE button will be released.

6.13 When the system is put into the PROCESSOR, INTERFACE or ISOLATION OVERRIDE state, a red LED, above the associated toggle switch on the display panel, will illuminate to indicate the appropriate state. When the system is put into the RESTORE state, the red LED for the previous isolation state will extinquish.

6.2 Isolation tests using the Main Alarm Control and Display Panel. Also, check the associated indications on the Auxiliary Alarm Display Panel, if provided.

6.201 Insert the SWR value from Table 2 for Step 1 into the SWR. Observe the associated responses from tables 3 through 5. Also, verify that the green "NORMAL" LED's for both processors are illuminated on the Main Alarm Control Display Panel and Auxiliary Display Panel, if equipped.

6.202 Using the procedure indicated in Paragraph 6.12, attempt to ISOLATE the PROCESSOR and INTERFACE on both CPUs using the Main Alarm Control and Display Panel. No change in state should occur. Place both CPU's into the ISOLATION OVERRIDE ACTIVATE state. At the Main Alarm Control and Display Panel, verify, for both CPU's, that the NORMAL LED extinguishes and the LED above the override toggle switch illuminates. Place both CPU's into the ISOLATION OVERRIDE RELEASE state.

6.203 Insert the SWR value for Step 2. Observe the associated responses from tables 3 through 5. Also, verify that the green "NORMAL" LED's for both processors are illuminated on the Main Alarm Control Display Panel and Auxiliary Display Panel, if equipped.

6.204 Using the procedure indicated in Paragraph 6.12, attempt to ISOLATE the PROCESSOR and INTERFACE on both CPU's using the Main Alarm Control and Display Panel. No change in state should occur. Place both CPU's into the ISOLATION OVERRIDE ACTIVATE state. At the Main Alarm Control and Display Panel, verify, for both CPU's that the "NORMAL" LED extinguishes and the LED above the override toggle switch illuminates. Place both CPU's into the ISOLATION OVERRIDE RELEASE state.

6.205 Insert the SWR value for Step 3. Put CPU0 into the PROCESSOR ISOLATE state. Observe the associated responses from Tables 3 through 5.

6.206 Verify the SWR value for Step 4. Put CPU0 into the PROCESSOR RESTORE state. Observe the associated responses from Tables 3 through 5.

6.207 Verify the SWR value for Step 5. Put CPU0 into the INTERFACE ISOLATE mode. Observe the associated responses from Tables 3 through 5.

6.208 Verify the SWR value for Step 6. Put CPU0 into the INTERFACE RESTORE mode. Observe the associated responses from Tables 3 through 5.

6.209 Insert the SWR value for Step 7. Put CPU1 into the PROCESSOR ISOLATE state. Observe the associated responses from Tables 3 through 5.

6.210 Verify the SWR value for Step 8. Put CPU1 into the PROCESSOR RESTORE state. Observe the associated responses from Tables 3 through 5.

6.211 Verify the SWR value for Step 9. Put CPU1 into the INTERFACE ISOLATE state. Observe the associated responses from Tables 3 through 5.

6.212 Verify the SWR value for Step 10. Put CPU1 into the INTERFACE RESTORE state. Observe the associated responses from Tables 3 through 5.

6.3 Isolation Override

6.301 Insert the SWR value for Step 11. Put CPU0 first into the PROCESSOR ISOLATE state, then put CPU0 into the ISOLATION OVERRIDE ACTIVATE state. Observe the associated responses from Tables 3 through 5.

6.302 Verify the SWR value for Step 12. Put CPU0 into the ISOLATION OVERRIDE RESTORE state. The system should return to the PROCESSOR ISOLATE state on CPU0. Observe the associated responses from Tables 3 through 5.

6.303 Verify the SWR value for Step 13. Put CPU0 first into PROCESSOR ISOLATE RESTORE, then into INTERFACE ISOLATE and then into ISOLATION OVERRIDE ACTIVATE. Observe the associated responses from Tables 3 through 5.

6.304 Verify the SWR value for Step 14. Put CPU0 into the ISOLATION OVERRIDE RESTORE state. The system should return to the INTERFACE ISOLATE state on CPU0. Observe the associated responses from Tables 3 through 5.

6.305 Put CPU0 into the INTERFACE ISOLATE RESTORE state.

6.306 Insert the SWR value for Step 15. Put CPU1 first into PROCESSOR ISOLATE then into ISOLATION OVERRIDE ACTIVATE. Observe the associated responses from Tables 3 through 5.

6.307 Verify the SWR value for Step 16. Put CPU1 into the ISOLATION OVERRIDE RELEASE state. The system should return to the PROCESSOR ISOLATE state. Observe the associated responses from Tables 3 through 5.

6.308 Verify the SWR value for Step 17. Put CPU1 first into PROCESSOR ISOLATE RESTORE, then into INTERFACE ISOLATE and then into ISOLATION OVERRIDE ACTIVATE. Observe the associated responses from Tables 3 through 5.

6.309 Verify the SWR value for Step 18. Put CPU1 into the ISOLATION OVERRIDE RELEASE state. The system should return to the INTERFACE ISOLATE state on CPU1. Observe the associated responses from Tables 3 through 5.

6.310 Put CPU1 into the INTERFACE ISOLATE RESTORE state.

6.4 Improper Isolation Sequence Test

6.41 The D, V0 and V1 cabinets should be in the same state as Step 10, refer to Tables 3 through 5.

6.42 On CPU1 depress and hold the EXECUTE button, then operate the CPU1 PROCESSOR ISOLATION switch to the ACTIVATE position. Release the switch and button. No change in state should have occurred.

6.43 Set the processor SWR keys to the same value as Step 4. The D, V0 and V1 cabinets should be in the same state as Step 4; refer to Tables 3 through 5.

6.44 On CPU0 depress and hold the EXECUTE button, then operate the CPU0 PROCESSOR ISOLATION switch to the ACTIVATE position. Release the switch and button. No change in state should have occurred.

6.5 Alarm Release

6.51 Set the processor SWR keys to the same value as Step 19. Do not verify responses in Tables 3 through 5 at this time.

6.52 Halt CPU0 by placing the HALT/ENABLE key on CPU0 to the HALT position.

6.53 A major alarm should have sounded. Retire alarms by depressing the RETIRE ALARMS button on the Main Alarm Control and Display Panel.

6.54 Halt CPU1 by placing the HALT/ENABLE key on CPU1 to the HALT position.

6.55 A critical alarm should be sounded. Retire alarms by depressing the RETIRE ALARMS button on the Auxiliary Alarm and Display Panel, if provided. (If not provided, retire the alarm at the Main Alarm Control and Display Panel.)

6.56 The PROGRAM TIMEOUT LEDs for both processors should be illuminated. Also, verify that green "NORMAL" LED's for both processors are illuminated at the Main Alarm Control and Display Panel.

6.57 Verify the responses in Tables 3 through 5 for Step 19.

TABLE 2

STEP	SWR SETTINGS	
	CPU0	CPU1
1	20	40
2	40	20
3	100	20
4	100	20
5	100	20
6	100	20
7	20	100
8	20	100
9	20	100
10	20	100
11	100	20
12	100	20
13	100	20
14	100	20
15	20	100
16	20	100
17	20	100
18	20	100
19	40	20

NOTE 1: SWR = 20 indicates ACTIVE
SWR = 40 indicates STANDBY
SWR = 100 indicates OUT-OF-SERVICE

NOTE 2: The associated system status will be illuminated on the Display Panel(s).

ATTACHMENTS
TABLES 3-5

Reason for Reissue:
To include UIS changes.

Manager, Product Engineering
Control Center

TABLE 3
'D' CABINET

STEP	CONT UNIT, LOCATION 22-						ALM UNIT, LOC. 08-						OACU UNIT, LOC. 08-							
	032	038	044	100	106	112	032	038	056	100	106	124	022	038	054	070	090	106	122	138
1	NORM	NORM	X	NORM	NORM	X	G	G	G	G	G	A	G	A	G	A	G	A	G	A
2	NORM	NORM	X	NORM	NORM	X	G	G	A	G	G	G	A	G	A	G	A	G	A	G
3	PROC	PROC	ISLT	NORM	NORM	X	R	X	X	G	R	G	R	G	R	G	R	G	R	G
4	NORM	NORM	X	NORM	NORM	X	G	G	A	G	G	G	A	G	A	G	A	G	A	G
5	ISLT	NORM	ISLT	NORM	NORM	X	R	X	ISLT	G	R	G	R	G	R	G	R	G	R	G
6	NORM	NORM	X	NORM	NORM	X	G	G	A	G	G	G	A	G	A	G	A	G	A	G
7	NORM	NORM	X	PROC	PROC	ISLT	G	R	G	R	X	ISLT	G	R	G	R	G	R	G	R
8	NORM	NORM	X	NORM	NORM	X	G	G	G	G	G	A	G	A	G	A	G	A	G	A
9	NORM	NORM	X	ISLT	NORM	ISLT	G	R	G	R	X	ISLT	G	R	G	R	G	R	G	R
10	NORM	NORM	X	NORM	NORM	X	G	G	G	G	G	A	G	A	G	A	G	A	G	A
11	PROC	PROC	ISLT	NORM	NORM	X	R	X	**	G	R	G	G	G	G	G	G	G	G	G
12	PROC	PROC	ISLT	NORM	NORM	X	R	X	ISLT	G	R	G	R	G	R	G	R	G	R	G
13	ISLT	NORM	ISLT	NORM	NORM	X	R	X	**	G	R	G	G	G	G	G	G	G	G	G
14	ISLT	NORM	ISLT	NORM	NORM	X	R	X	ISLT	G	R	G	R	G	R	G	R	G	R	G
15	NORM	NORM	X	PROC	PROC	ISLT	G	R	G	R	X	**	G	G	G	G	G	G	G	G
16	NORM	NORM	X	PROC	PROC	ISLT	G	R	G	R	X	ISLT	G	R	G	R	G	R	G	R
17	NORM	NORM	X	ISLT	NORM	ISLT	G	R	G	R	X	**	G	G	G	G	G	G	G	G
18	NORM	NORM	X	ISLT	NORM	ISLT	G	R	G	R	X	ISLT	G	R	G	R	G	R	G	R
19	NORM	NORM	X	NORM	NORM	X	G	R,G	ISLT	G	R,G	ISLT	R	R	R	R	R	R	R	R

** = The MAN OVRD and NORMAL LED's should be illuminated.
R = Red LED
G = Green LED
A = Amber LED
X = All LED's off

TABLE 4
'V0' CABINET

STEP	TASYN UNIT, LOC. 08-								OASYN UNIT, LOC. 08-								TTY UNIT, LOC. 08-			
	022	038	054	070	090	106	122	138	022	038	054	070	090	106	122	138	022	038	054	070
1	G	A	G	A	G	A	G	A	G	A	G	A	G	A	G	A	G	G	G	G
2	A	G	A	G	A	G	A	G	A	G	A	G	A	G	A	G	G	G	G	G
3	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
4	A	G	A	G	A	G	A	G	A	G	A	G	A	G	A	G	G	G	G	G
5	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
6	A	G	A	G	A	G	A	G	A	G	A	G	A	G	A	G	G	G	G	G
7	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R
8	G	A	G	A	G	A	G	A	G	A	G	A	G	A	G	A	G	G	G	G
9	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R
10	G	A	G	A	G	A	G	A	G	A	G	A	G	A	G	A	G	G	G	G
11	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G
12	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
13	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G
14	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
15	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G
16	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R
17	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G
18	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R
19	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	G	G	G	G

R = Red LED
G = Green LED
A = Amber LED

TABLE 5
'V1' CABINET

STEP	2ASYN UNIT, LOC. 08-								TACU UNIT, LOC. 08-							
	022	038	054	070	090	106	122	138	022	038	054	070	090	106	122	138
1	G	A	G	A	G	A	G	A	G	A	G	A	G	A	G	A
2	A	G	A	G	A	G	A	G	A	G	A	G	A	G	A	G
3	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
4	A	G	A	G	A	G	A	G	A	G	A	G	A	G	A	G
5	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
6	A	G	A	G	A	G	A	G	A	G	A	G	A	G	A	G
7	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R
8	G	A	G	A	G	A	G	A	G	A	G	A	G	A	G	A
9	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R
10	G	A	G	A	G	A	G	A	G	A	G	A	G	A	G	A
11	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G
12	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
13	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G
14	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
15	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G
16	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R
17	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G
18	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R
19	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

R = Red LED
G = Green LED
A = Amber LED