Installation Engineering Handbook 59
Western Electric
Columbus Works

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AMARS
NO. 1A AUTOMATIC MESSAGE ACCOUNTING RECORDING CENTER
SECOND SUPPLEMENTARY PROCESSOR INTERFACE CABINET INSTALLATION
SYSTEM EXPANSION TO EXISTING SYSTEMS
(J1P040V-1, LIST 2)

CONTENTS

1. GENERAL INFORMATION

1.01 This handbook section procedure is used to install the Second Supplementary Processor Interface Cabinet to existing live billing No. 1A AMARC systems. If installing a new unit(s) in an existing J1P040V-1 cabinet on a live billing system, use HB59 Section 204K. If installing a new J1P040V-1, List 2 cabinet and a new unit in the J1P040V-1, List 1 cabinet on a live billing system, execute the steps in this handbook section, then, execute the steps in HB59 Sect. 204K.

1.02 This procedure should be done during low traffic periods since simplex operation of the system is required.

1.03 Should troubles be encountered on the active system while performing this procedure, immediately stop any further testing and proceed as follows: If the new J1P040V-1, List 2 cabinet contains a 2ASYN unit, return the system to TELCo for their normal system restoral procedures. If the new J1P040V-1, List 2 cabinet only contains a 1ACU unit, execute the steps in the paragraph entitled 'End of ACU Loop-Around Test' before returning the system to TELCo for their normal system restoral procedures.

1.04 The new DEC peripheral equipment associated with the J1P040V-1, List 2 cabinet must be installed and tested by DEC or maintenance personnel prior to the start of this handbook section.

1.05 The TELCO should arrange to have their craft personnel available for performing various system operations during this handbook section procedure.

1.06 The TELCO should arrange to have the DEC or maintenance personnel available for making cable connection in the DEC equipment or authorize Western Electric to perform the cable connections.

1.07 Do not route or connect any cables associated with the 1ACU unit and DN11 until instructed to later in this handbook section.

1.08 Cable dress information is located in ED5P285-12.

2. RECORDS AND REQUIREMENTS

2.1 The Test Trouble Record forms (SD-97-1313 and SD-97-1315) should be used to record all troubles which are encountered when running the tests in this handbook section.

3.   TEST EQUIPMENT

3.1   One ITE-5632 Digital Multimeter (or equivalent).

3.2   One ITE-8900 Data Set, Flexport and ACU interface loop-around cable kit.

3.3   SPP-832 Spare Pack Package.

3.4   W. E. Co. Diagnostics on disk (supplied by the TELCO).

4.   INSTALLATION OF THE CABINET

4.1   The Second Supplementary Processor Interface Cabinet should be positioned in accordance with floor plan data requirements (FPD 824-100-105-1).

4.2   The uninterruptable power supply receptacles for the J1PO40V-1, List 2 cabinet should have been installed and tested. Verify that the output voltage at each receptacle is 120 VAC. Measure between phase and neutral leads.

5.   FUSE AND POWER

5.1   Power Transfer Unit

5.101 Power for the Second Supplementary Processor Interface Cabinet is supplied by the Power Transfer Unit. The Power Transfer Unit obtains power from a single phase receptacle at the power distribution circuit. JO and J1 receptacles on the unit receive plugs from the power strips within the cabinet. Do not connect power to the Power Transfer Unit until specified in the following paragraphs.

5.102 Remove all plugs from outlets on both sides of the Second Supplementary Processor Interface Cabinet.

5.103 Disengage all circuit packs in the Asynchronous Interface Unit (2 ASYN) (J1PO400C), the ACU Interface Unit (1 ACU) (J1PO400D) and the Power Transfer and Static Filter Unit (2 PWR/FLT) (J1PO400G).

5.104 Verify the 'PWR CORD 0' is connected from the receptacle 1 on the side 0 power strip to the JO outlet on the Power Transfer Unit.

5.105 Verify that 'PWR CORD 1' is connected from the receptacle 1 on the side 1 power strip to the J1 outlet on the Power Transfer Unit.

5.106 Connect the power cord PO from the Power Transfer Unit to the receptacle for the Second Supplementary Processor Interface Cabinet associated with CPUO. Verify that the pilot lamp at the top of both power strips is illuminated. If the pilot lamps are not illuminated, depress the circuit breaker button on top of the associated power strip. Verify that 120 VAC is obtained at all outlets on both sides of the Second Supplementary Processor Interface Cabinet.

5.107 Remove the ACO fuse. Verify that 120 VAC has been removed from all outlets on side 0 of the Second Supplementary Processor Interface Cabinet. Side 1 should still retain power.

5.108 Remove power cord PO from the receptacle.

5.109 Restore the ACO fuse.

5.110 Connect power cord P1 to the receptacle for the Second Supplementary Processor Interface Cabinet associated with CPU1. Verify that 120 VAC is obtained at all outlets on both sides of the Second Supplementary Processor Interface Cabinet.

5.111 Remove the AC1 fuse. Verify that 120 VAC has been removed from all outlets on side 1 of the Second Supplementary Processor Interface Cabinet. Side 0 should still retain power.

5.112 Restore the AC1 fuse.

5.113 Restore power cord PO to the receptacle for the Second Supplementary Processor Interface Cabinet associated with CPUO.

5.2   Fuse and DC Power

5.201 Remove the DO, FO, D1, and F1 fuses.

5.202 Verify that all the fuses for the 2 PWR SUPP at the top of the frame are in place.

5.203 Connect the plug for the 2 PWR SUPP for side 0 to outlet 16 on side 0.

5.204 Connect the plug for the 2 PWR SUPP for side 1 to outlet 16 on side 1.

5.205 Operate both power switches on the 2
       PWR SUPP power supply to the ON posi-
       tion.

5.206 Verify that no power or ground condi-
       tions exist on any of the +12v or -12v
       terminals on TB1 or TB3. Refer to
       SD-5P016-01, FS3, if necessary.

5.207 Insert an operated fuse, one at a
       time, into the fuse holder, listed in
       Table A, and observe that the associ-
       ated LED indicator listed in Table A
       illuminates.

TABLE A

SIDE 0		SIDE 1	
FUSE HOLDER	LED	FUSE HOLDER	LED
D0	+12V0	D1	+12V1
F0	-12V0	F1	-12V1

5.208 Restore all fuses that were removed in
       Paragraph 5.201.

5.209 Verify the voltages at the terminals
       given in Table B. Refer to SD-5P012-
       01, FS3, if necessary.

TABLE B

VOLTAGE	RANGE	SIDE	LOC.	TERMINAL
+12V	+11.4v to +12.6v	0	TB1	7
+12V	+11.4v to +12.6v	1	TB3	7
-12V	-11.4v to -12.6v	0	TB1	10
-12V	-11.4v to -12.6v	1	TB3	10

       NOTE: The output voltage must be
       within the range indicated. There is
       an adjustment potentiometer on the 2
       PWR SUPP that can be used for adjust-
       ment.

5.210 Verify that power is supplied to both
       sides of all units within the Second
       Supplementary Processor Interface Cab-
       inet. Refer to Table C for available
       voltages on the specified units. Ver-
       ify between the voltage bug and the
       GND bug.

TABLE C

UNIT	VOLTAGE	LOCATION
2ASYN	+12v	+12v BUG
2ASYN	-12v	-12v BUG
1ACU	+12v	+12v BUG
1ACU	-12v	-12v BUG

5.211 Turn the two power switches on the 2
       PWR SUPP power supply to the OFF posi-
       tion. Insert all circuit packs in the
       Asynchronous Interface Units (2 ASYN)
       (J1P040DC), ACU Interface Unit (1ACU)

(J1P040DD) and the Power Transfer and
Static Filter Unit (2 PWR/FLT) (J1P040-
DG). Restore power using the two
switches on the 2 PWR SUPP power
supply.

6.   POWER TRANSFER TEST

6.1   Remove power cord P0 from the recept-
       acle for the Second Supplementary Pro-
       cessor Interface Cabinet associated
       with CPU0.

6.2   Observe that the TRNSFR0 LED illumi-
       nate on the SH9 circuit pack located
       in the 2 PWR/FLT unit.

6.3   Restore power cord P0. The TRNSFR0
       LED should extinguish.

6.4   Remove power cord P1 from the recept-
       acle for the Second Supplementary Pro-
       cessor Interface Cabinet associated
       with CPU1.

6.5   Observe that the TRNSFR1 LED illumi-
       nate on the SH9 circuit pack located
       in the 2 PWR/FLT unit.

6.6   Restore power cord P1. The TRNSFR1
       LED should extinguish.

7.   POWER SUPPLY FAILURE TEST

7.1   Verify that the ACFL0 and ACFL1 LEDs
       on the SH9 circuit pack in the 2 PWR/
       FLT unit are extinguished.

7.2   Operate the power switch on the 2 PWR
       SUPP associated with side 0 to the
       'OFF' position.

7.3   Verify that the ACFL0 LED on the SH9
       circuit pack in the 2 PWR/FLT unit
       illuminates.

7.4   Restore the power switch on the 2 PWR
       SUPP to the 'ON' position. The ACFL0
       LED should extinguish.

7.5   Operate the power switch on the 2 PWR
       SUPP associated with side 1 to the
       'OFF' position.

7.6   Verify that the ACFL1 LED on the SH9
       circuit pack in the 2 PWR/FLT unit
       illuminates.

7.7   Restore the power switch on the 2 PWR
       SUPP to the 'ON' position. The ACFL1
       LED should extinguish.

8.   CABLING

8.1   Turn the two power switches on the 2
      PWR SUPP power supply to the OFF posi-
      tion.

8.2   Request that the TELCO craft personnel
      remove the STANDBY processor to the
      out-of-service state, place into the
      PROCESSOR ISOLATE state, HALT the out-
      of-service processor; then, turn power
      off to the out-of-service processor by
      turning its ON/OFF switch on its pro-
      grammer's console to the 'OFF' posi-
      tion.

      NOTE: If only installing a 1ACU unit,
             there is no need to remove
             power from the prcessor.

8.3   Cable Connections on OOS CPU

      NOTE: In connecting the ED-5P284-31
      cables to the male connector on a DEC
      circuit board, the triangle on the
      cable connector (female) should be
      inserted to mate with the "A" designa-
      tion on the circuit board. When con-
      necting to the isolation backplane,
      the triangle must always be on the
      bottom.

8.31 Route and connect the following cables
      associated with the new unit(s). If
      CPUO is the out-of-service system,
      connect the cables as indicated in
      TABLE 1A and TABLE 1B. If CPU1 is the

TABLE 1A

DESIG.	GROUP	STAMPED	CONNECTED FROM LOC.	UNIT	CONNECTED TO	STAMPED
CB78-0	69	2ASYN 06-017	06-017	2ASYN	10DZ11B	CPUO 10DZ11B
CB79-0	69	2ASYN 06-049	06-049	2ASYN	11DZ11B	CPUO 11DZ11B
CB80-0	69	2ASYN 06-085	06-085	2ASYN	12DZ11B	CPUO 12DZ11B
CB81-0	69	2ASYN 06-117	06-117	2ASYN	13DZ11B	CPUO 13DZ11B
CB48-0	73	1ACU 06-017	06-017	1ACU	NOTE 1	CPUO 10DN11DA
CB49-0	73	1ACU 10-017	10-017	1ACU	NOTE 1	CPUO 11DN11DA
CB50-0	73	1ACU 06-049	06-049	1ACU	NOTE 1	CPUO 12DN11DA
CB51-0	73	1ACU 10-049	10-049	1ACU	NOTE 1	CPUO 13DN11DA
CB52-0	73	1ACU 06-085	06-085	1ACU	NOTE 1	CPUO 14DN11DA
CB53-0	73	1ACU 10-085	10-085	1ACU	NOTE 1	CPUO 15DN11DA
CB54-0	73	1ACU 06-117	06-117	1ACU	NOTE 1	CPUO 16DN11DA
CB55-0	73	1ACU 10-117	10-117	1ACU	NOTE 1	CPUO 17DN11DA

NOTE 1: Do not route this end of the cable to the DEC equipment at this time. IF a
2ASYN unit is equipped, leave these cable ends in the vicinity of the J1P040V-1, List 2
cabinet for testing purposes. If only a 1ACU units is equipped, temporarily route these
cable ends to the vacinity the J1P040V-1, List 1 cabinet for testing purposes.

TABLE 1B

DESIG.	GROUP	STAMPED	CONNECTED FROM LOC.	UNIT	CONNECTED TO LOC.	UNIT	STAMPED
*CB3-0	65	PULSE 04-058	TRMTCO2 RCVCO2 RERTNO2	PULSE PULSE PULSE	TRMTCO2 RCVCO2 RERTNO2	1 ACU 1 ACU 1 ACU	1 ACU
CB3	57	ALM-10-082-Q2	NOTE 1	NOTE 1	06-010-Q3	NOTE 2	To Bottom Most Equipped Unit 06-010-Q3

* The wire from the shield on this cable is connected in the J1P040D-1 Cabinet at GND
  BUS 0.

NOTE 1: Do not connect this end of cable CB3 at this time.

NOTE 2: CB3 connects from the ALM unit to the bottom most unit designated 2 ASYN or 1
ACU in the J1P040V-1, List 2 Cabinet.

TABLE 2A

DESIG.	GROUP	STAMPED	CONNECTED FROM LOC.	UNIT	CONNECTED TO	STAMPED
CB78-1	70	2ASYN 10-033	10-033	2ASYN	10DZ11B	CPU1 10DZ11B
CB79-1	70	2ASYN 10-065	10-065	2ASYN	11DZ11B	CPU1 11DZ11B
CB80-1	70	2ASYN 10-101	10-101	2ASYN	12DZ11B	CPU1 12DZ11B
CB81-1	70	2ASYN 10-133	10-133	2ASYN	13DZ11B	CPU1 13DZ11B
CB48-1	72	1ACU 06-033	06-033	1ACU	NOTE 1	CPU1 10DN11DA
CB49-1	72	1ACU 10-033	10-033	1ACU	NOTE 1	CPU1 11DN11DA
CB50-1	72	1ACU 06-065	06-065	1ACU	NOTE 1	CPU1 12DN11DA
CB51-1	72	1ACU 10-065	10-065	1ACU	NOTE 1	CPU1 13DN11DA
CB52-1	72	1ACU 06-101	06-101	1ACU	NOTE 1	CPU1 14DN11DA
CB53-1	72	1ACU 10-101	10-101	1ACU	NOTE 1	CPU1 15DN11DA
CB54-1	72	1ACU 06-133	06-133	1ACU	NOTE 1	CPU1 16DN11DA
CB55-1	72	1ACU 10-133	10-133	1ACU	NOTE 1	CPU1 17DN11DA

NOTE 1: Do not route this end of the cable to the DEC equipment at this time. If a 2ASYN unit is equipped, leave these cable ends in the vicinity of the J1P040V-1, List 2 cabinet for testing purposes. If only a 1ACU unit is equipped, temporarily route these cable ends to the vacinity of the J1P040V-1, List 1 cabinet for testing purposes.

TABLE 2B

DESIG.	GROUP	STAMPED	CONNECTED FROM LOC.	UNIT	CONNECTED TO LOC.	UNIT	STAMPED
**CB3-1	65	PULSE 04-093	TRMTC12 RCVC12 RERTN12	PULSE PULSE PULSE	TRMTC12 RCVC12 RERTN12	1 ACU 1 ACU 1 ACU	1 ACU
CB3	57	ALM-10-082-Q2	NOTE 1	NOTE 1	06-010-Q3	NOTE 2	To Bottom Most Equipped Unit 06-010-Q3

**The wire from the shield on this cable is connected in the J1P040D-1 Cabinet at GND BUS 1.

NOTE 1: Do not connect this end of cable CB3 at this time.

NOTE 2: CB3 connects from the ALM unit to the bottom most unit designated 2 ASYN or 1 ACU in the J1P040V-1, List 2 Cabinet.

out-of-service system, connect the cables as indicated in TABLE 2A and TABLE 2B.

NOTE 1: DEC or maintenance personnel should make all cable connections in the DEC equipment.

NOTE 2: Do not connect the cable end of CB3 to the J1P040D cabinet ALM unit at this time.

NOTE 3: Do not route cable ends to the DN11 equipment at this time. Refer to the note following the associated table.

8.4 Cable Connections on the other CPU

8.41 Preliminary

8.411 Turn the power switch associated with the present out-of-service CPU on the 2 PWR SUPP power supply to the 'ON' POSITION.

8.412 Request that the TELCO restore power to the out-of-service processor using the ON/OFF switch at the programmer's console if necessary, then with the HALT key still depressed, operate the START key once.

8.413 Pulse the circuit packs in the J1P040V-1, List 2 cabinet associated with the out-of-service processor by requesting that the TELCO again place the out-of-service processor into the PROCESSOR ISOLATE state without restoring from the PROCESSOR ISOLATE state first.

8.414 Verify that the "ISOLATED" red LED's on all TN102 circuit packs in the J1P040V-1, List 2 cabinet associated with the out-of-service processor are illuminated.

8.415 Request that the TELCO restore the out-of-service processor to the STAND-BY state using their normal procedures. Verify that all TN102 circuit packs in the J1P040V-1, List 2 cabinet associated with the STANDBY processor have their amber "STANDBY" LED's illuminated.

8.416 Request that the TELCO do a system switch. Verify that all TN102 circuit packs in the J1P040V-1, List 2 cabinet associated with the new ACTIVE processor have their green "NORMAL" LED's illuminated.

8.417 Request that the TELCO remove the new STANDBY processor to the out-of-service state, place into the PROCESSOR ISO-LATE state, HALT the out-of-service processor; then, turn the power off to the out-of-service processor by turning its ON/OFF switch on its programmer's console to the "OFF" position.

8.42 Route and connect the following cables associated with the new unit(s). If CPU0 is the out-of-service system, connect the cables as indicated in TABLE 1A and TABLE 1B (see notes below for exceptions). If CPU1 is the out-of-service system, connect the cables as indicated in TABLE 2A and TABLE 2B (see notes below for exceptions).

NOTE 1: DEC or maintenance personnel should make all cable connections in the DEC equipment.

NOTE 2: If a 1ACU unit and a 2ASYN unit are being equipped, do not connect the cable end of cable CB78-X (where X = OOS CPU number) at the J1P040V-1, List 2 cabinet at this time.

NOTE 3: Do not connect the cable end of CB3 to the J1P040D cabinet ALM unit at this time.

NOTE 4: Do not route cable ends to the DN11 equipment at this time. Refer to the note following the associated table.

9. DIAGNOSTICS

9.1 Preliminary Set-Up

9.11 Swap all TN102 circuit packs associated with the out-of-service CPU and the Active CPU in the J1P040V-1, List 2 cabinet.

9.12 Turn the power switch associated with the present OOS CPU on the 2 PWR SUPP power supply to the 'ON' position.

9.13 Pulse the circuit packs in the J1P040V-1, List 2 cabinet associated with the ACTIVE processor to the NOR-MAL state by requesting that the TELCO place the ACTIVE system first into the ISOLATION OVERRIDE ACTIVATE state then into the ISOLATION OVERRIDE RELEASE state.

9.14 Verify that all TN102 circuit packs in the J1P040V-1, List 2 cabinet have their green "NORMAL" LED's illuminated.

9.15 If no 1ACU unit is being equipped, proceed to paragraph 9.17.

9.16 Connect into the 50 pin connector labeled "DZ11" on the "ACU Loop-Around" box in the ITE-8900 kit the following cable.

9.161 If a 2ASYN unit is being equipped, use the cable end of CB78-X (where X-OOS CPU#) in the J1P040V-1, List 2 cabinet.

9.162 If only a 1ACU unit is being equipped perform the following:

a) Remove power in the J1P040V-1, List 1 cabinet associated with the OOS CPU.
b) Disconnect cable CB70-X (where X = OOS CPU #) and plug into the 50 pin connector on the ACU Loop-Around box.

NOTE: Refer to paragraph 1.03 for recovery procedures in case of trouble on the active side.

9.17 Request that the TELCO install the W.E. Co. diagnostic disk pack, boot the diagnostics and be ready to execute selected diagnostic programs when requested.

9.2   Execution of ACU Interface Loop-Around Test

9.21   IF no 1ACU unit is being equipped, proceed to paragraph 9.3.

9.22   Preliminary

9.221   The "async.dsif" diagnostic will be used to perform the ACU Interfaces Loop-Around tests. This diagnostic will be run in the 'q' mode of operation specifying only multiplexor 10 (or multiplexor 00 if only a 1ACU unit is being equipped).

9.222   The ACU Interface Loop-Around cables from the ITE-8900 package consists of the following three items:

a)   The first item has three connectors, one 50 pin connector and two 40 pin connectors. Cable CB78-X or CB70-X (where X = OOS CPU number) was plugged into the 50 pin connector in Paragraph 9.16 and remains in place until all ACU loop-around tests have been completed. The cables to be plugged into the 40 pin connectors are listed in TABLE 3 and are dependent on the test number and the CPU side of the J1P040V-1, List 2 cabinet under test.

b)   The other two items consist of EIA connectors wired internally to produce a loop-around. The designation on these connectors are "ACU (2N-2)" and "ACU (2N-1)." These connectors are plugged into the appropriate locations listed in Table 3, dependent on the test number.

9.23   Refer to TABLE 3. Connect the appropriate cables into the 40 pin connectors on the ACU interface loop-around for the test number to be executed associated with the CPU0 side of the J1P040V-1, List 2 cabinet. Connect the ACU (2N-2) and ACU (2N-1) connectors to the appropriate connectors for the test number to be executed.

NOTE: Start with test number 1.

9.24   Request the TELCO to execute, on the OOS CPU, the "async.dsif" diagnostic in the "q" mode for multiplexor 10 (if a 2ASYN unit is also being equipped), or multiplexor 00 (if only a 1ACU unit is being equipped). Also select the "d" and "p" options.

IMPORTANT NOTE: The TN102 circuit packs in the 1 ACU unit under test must be in the NORMAL green state. This was done in Paragraph 9.13. During the execution of the diagnostic test, a message will be printed indicating that the processor must be in the isolation state. Respond to this message by indicating that the processor is in the isolation state, even though the TN102 circuit packs are in the NORMAL state. DO NOT attempt to place the CPU into the isolation state during any portion of these loop-around tests.

9.25   The diagnostic program will now be executing. Examine the printout. If the diagnostic test failed, refer to the DZ11 manual for detailed trouble

TABLE 3

ACU INTERFACE LOOP-AROUND

TEST NO. (N) (OCTAL)	CABLE DESIG. TO BE PLUGGED INTO ITE ACU INTERFACE LOOP-AROUND (SEE NOTE 1)		ITE ACU INTERFACE LOOP-AROUND PLUG. PLUG INTO:				ACU CHANNELS UNDER TEST (OCTAL)	TN 102 UNDER TEST		
	CONN 1.	CONN. 2	ACU (2N-2)		ACU (2N-1)			UNIT	LOC. IF CPU0	LOC. IF CPU1
			UNIT	LOC.	UNIT	LOC.				
1	CB48-X	CB49-X	1ACU	02-016	1ACU	02-032	10 & 11	1ACU	08-022	08-038
2	CB50-X	CB51-X	1ACU	02-048	1ACU	02-064	12 & 13	1ACU	08-054	08-070
3	CB52-X	CB53-X	1ACU	02-080	1ACU	02-096	14 & 15	1ACU	08-010	08-106
4	CB54-X	CB55-X	1ACU	02-112	1ACU	02-128	16 & 17	1ACU	08-122	08-138

NOTE 1:   The X represents a '0' or '1' depending on which CPU side of the J1P040V-1, List 2 cabinet is under test.

analysis and re-execute the diagnostic test using the same cable arrangement.

9.26   If the diagnostic tests pass: Disconnect the cables from the 40 pin connectors on the ACU interface loop-around. Refer to TABLE 3. Connect the appropriate cables into the 40 pin connectors on the ACU Interface Loop-Around for the same test number as in Paragraph 9.23 but associated with the CPU1 side of the J1P040V-1, List 2 cabinet. (NOTE: no need to change connectors ACU (2N-2) and ACU (2N-1) until the next test number). Request the TELCO to re-execute the same diagnostic program (re-execute Paragraph 9.24 and 9.25).

9.27   If the diagnostic tests pass, repeat the procedure listed in Paragraphs 9.23 through 9.27 until all test numbers and both CPU sides of the J1P040V-1, List 2 Cabinet have been tested.

9.28   End of ACU Loop-Around Test

9.281   Remove the DN11 cables from the 40 pin connectors on the ACU Interface Loop-Around. Remove the ACU (2N-2) and ACU (2N-1) connectors. These cables and connectors were left in place from the last test.

9.282   If a 2ASYN unit is also being equipped remove cable CB78-X (where X = OOS CPU#) from the 50 pin connector on the ACU interface loop-around box and connect to its appropriate location as listed in TABLE 1A or TABLE 2A.

9.283   If only a 1ACU unit is being equipped, remove cable CB70-X (where X = OOS CPU#) from the 50 pin connector on the ACU interface loop-around box and restore to its appropriate location in the J1P040V-1, List 1 cabinet. Restore power to the OOS side of the J1P040V-1, List 1 cabinet. Request the TELCo to execute the "async.dsif" diagnostic on the OOS CPU for mulitplexor 00 using their normal (isolated) procedure.

NOTE: If the steps in this paragraph section were executed because of problems on the active billing side and emergency recovery steps are being performed, inform the TELCo that the diagnostic disk pack needs to be replaced with their AMA disk pack.

9.3   Data Set Loop-Around Tests

9.31   If only a 1ACU unit is being equipped, proceed to the paragraph entitled "Terminate Diagnostic Tests".

TABLE 4

DATA SET LOOP-AROUND
ITE-8900 CABLE CONNECTIONS

FOR MUX #	CONNECTOR END MARKED							
	CHL--0	CHL--1	CHL--2	CHL--3	CHL--4	CHL--5	CHL--6	CHL--7
	CONNECT IN V1 CABINET (2 ASYN) TO EQUIPMENT LOCATION							
10	02-016	14-016	02-024	14-024	02-032	14-032	02-040	14-040
11	02-048	14-048	02-056	14-056	02-064	14-064	02-072	14-072
12	02-080	14-080	02-088	14-088	02-096	14-096	02-104	14-104
13	02-112	14-112	02-120	14-120	02-128	14-128	02-136	14-136

9.32   GENERAL

9.321   The data set loop-around tests will utilize the data set loop-around cables contained in the ITE-8900 package.

NOTE: The LED in each connector should illuminate as the connector is inserted.

9.322   The "async.dsif" diagnostic program will be executed with all associated TN102 circuit packs, in the 2ASYN unit associated with the OOS CPU, in the NORMAL state. DO NOT attempt to place the CPU in the isolation state during any portion of the Data Set Loop-around tests.

9.323   One multiplexor will be tested at a time. Only the side of the 2ASYN unit associated with the OOS CPU will be tested.

9.33   Instructions

9.331   Install the data set loop-around cables contained in the ITE-8900 package as listed in Table 4 for the first multiplexor in the J1P040V-1, List 2 cabinet.

9.332   Request the TELCO to execute, on the OOS CPU, the "async.dsif" diagnostic in the "q" mode of for the multiplexor under test. Also select the "d" and "p" options.

IMPORTANT NOTE: The TN102 circuit packs in the 2ASYN unit associated with the OOS CPU must be in the NORMAL green state. This was done in Paragraph 9.13. During the execution of the diagnostic test, a message will be printed indicating that the processor must be in the isolation state. Respond to this message by indicating that the processor is in the isolation state, even though the TN102 circuit packs are in the NORMAL state. Do not attempt to place the CPU into the isolation state during any portion of the Data Set Loop-Around tests.

9.333   If the multiplexor tests fail, refer to the detailed printouts and the DZ11 manuals. Also refer to the SD for cable and circuit pack information.

9.334   After the multiplexor tests pass, remove the ITE-8900 cables.

9.335   Refer to TABLE 4. Reconnect the ITE-8900 cables for the next multiplexor to be tested.

9.336   Repeat the steps in Paragraphs 9.332 through Paragraph 9.335 until all multiplexors in the J1P040V-1, List 2 cabinet have been tested.

9.337   Remove the ITE-8900 cables from the last test. These cables will be used again later in this handbook section procedure.

9.4   Multiplexor Tests in the Isolation State

9.41   Request the TELCO to execute, on the OOS CPU, the "async.dsif" diagnostic in the "q" mode of operation for all equipped multiplexors in the J1P040V-1, List 2 cabinet.

IMPORTANT NOTE: This time, when the diagnostic requests that the system be placed in the isolation state, DO isolate the processor. When the processor is isolated, all TN102 circuit packs in the J1P040V-1, List 2 cabinet associated with the OOS side must have their red "ISOLATED" LED's illuminated.

9.42   Examine the printout for errors. Re-execute any failing diagnostic test. Refer to the DZ11 manual and SD's for detailed trouble shooting.

9.5   Terminate Diagnostic Tests

9.51   Request that the TELCo terminate the diagnostic program. The TELCo can now remove the diagnostic disk pack and replace it with the AMA disk pack.

NOTE: If a 2ASYN unit is equipped the diagnostic disk will be used on the other side of the system, later in this handbook section.

10.   INSTALL DN11 CABLES ON THE OOS CPU

NOTE: Perform the tests in this paragraph section only if a 1ACU unit is equipped.

10.1   Request the TELCO to perform the following steps on the OOS CPU: HALT, place in the PROCESSOR ISOLATE state and remove its power by turning its power switch to the 'OFF' position.

10.2 Turn the power switch associated with OOS CPU on the 2 PWR SUPP power supply to the 'OFF' position.

10.3 Route the DN11 cables associated with the OOS CPU to the associated DEC equipment cabinet. Refer to TABLE 1A or TABLE 2A depending on which processor is OOS.

10.4 Request that the DEC or maintenance personnel connect the DN11 cables to the approrpiate DN11 as indicated on the cable stamping in the OOS CPU only.

10.5 Turn the power switch associated with the OOS CPU on the 2 PWR SUPP power supply to the 'ON' position.

11.   DIAGNOSTIC SET-UP - OTHER CPU

11.1 Disengage the TN102 circuit packs in the 2ASYN unit, if equipped, associated with the present ACTIVE side.

11.2 Request the TELCO to restore the OOS CPU to the STANDBY state using their normal procedure. Verify that all TN102 circuit packs in the J1P040V-1, List 2 cabinet associated with the standby CPU have their amber 'STANDBY' LED's illuminated.

11.3 Request the TELCO to do a system switch. Verify that all TN102 circuit packs in the J1P040V-1, List 2 cabinet associated with the new ACTIVE side have their green 'NORMAL' LED's illuminated.

11.4 Request the TELCO to remove the new Standby CPU to the OOS state.

11.5 Connect DN11 cables in the new OOS CPU

NOTE: Perform the tests in this paragraph section only if a 1ACU unit is equipped.

11.51 Repeat the steps in paragraph 10 for the new OOS CPU.

12.   DIAGNOSTICS - OTHER CPU

12.1   General

12.11 The circuit packs for the 1ACU unit associated with this new OOS CPU where checked using the other CPU earlier in this handbook section.

12.12 If only a 1ACU unit is equipped, proceed to the paragraph entitled "Final Tests". Proceed with this paragraph section only if equipping a new 2ASYN unit.

12.13 This new OOS CPU only requires testing of its 2ASYN unit.

12.14 Circuit packs in the OOS side of the 2ASYN unit at present are disengaged. When engage, these TN102 boards must indicate a green 'NORMAL' state for the data set loop-around tests.

12.2 Proceed with this paragraph section only if equipping a new 2ASYN unit.

12.3 Request that the TELCo install the W.E. Co. diagnostic disk pack, boot the diagnostics and be ready to execute selected diagnostic programs when requested.

12.4 Engage all the TN102 circuit packs in the 2ASYN unit associated with the OOS CPU. Verify that each of these packs have their green 'NORMAL' LED illuminated.

NOTE: The 'NORMAL' state of these TN102 circuit packs is required for the data set loop-around tests that follow.

12.5 Perform the data set loop-around tests on the new OOS CPU by repeating the tests in Paragraph 9.33.

NOTE: General information on the test is given in Paragraph 9.32.

12.6 Perform the "Multiplexor Tests in the Isolated State" on the new OOS CPU by repeating the tests in Paragraph 9.4.

12.7 Request that the TECLo terminate the diagnostic program. The TELCo can now remove the diagnostic disk pack and replace it with the AMA disk pack.

13.   FINAL TESTS

13.1 Verify that all the TN102 circuit packs in the J1P040V-1, List 2 cabinet associated with the OOS CPU have their red "ISOLATED" LED's illuminated. Also, verify that all the TN102 circuit packs in the J1P040V-1, List 2 cabinet associated with the ACTIVE CPU have their green "NORMAL" LED's illuminated.

13.2   Inform the TELCO that the next step will register an alarm and produce an alarm output message on the ACTIVE system console. This alarm and message will not affect the billing operations of the ACTIVE system.

13.3   Carefully, connect the cable end of cable CB3, which was routed to the J1P040D cabinet earlier in this handbook section, labeled "ALM-10-082-Q2" to the ALM unit location 10-082-Q2.

        NOTE: The TELCO should retire the alarm generated by the above procedure.

13.4   Check that both "NORMAL" LED's on the Main Alarm Control and Display panel are illuminated. No red "FAULT" LED's in the J1P040D cabinet should be illuminated.

13.5   TN102 Functional Tests

13.51   General Procedure Instructions

13.511 Read all parts of the General Procedure Instructions before starting testing.

13.512 Disregard the alarms generated when disengaging and reengaging TN102 circuit packs for testing purposes. Billing should not be affected.

13.513 Without removing power, disengage the TN102 circuit pack at location 08-122 in the 2ASYN unit (if the 2ASYN unit is not equipped, use location 08-122 in the 1ACU unit). Verify that the green NORMAL LED associated with CPU0 on the Main Alarm Control and Display Panel extinguishes.

13.514 Without removing power, reengage the TN102 circuit pack. Verify that the green NORMAL LED associated with CPU0 on the Main Alarm Control and Display Panel illuminates.

13.515 Without removing power, disengage the TN102 circuit pack at location 08-138 in the 2ASYN unit (if the 2ASYN unit is not equipped, use location 08-138 in the 1ACU unit). Verify that the green NORMAL LED associated with CPU1 on the Main Alarm Control and Display Panel extinguishes.

13.516 Without removing power, reengage the TN102 circuit pack. Verify that the green NORMAL LED associated with CPU1 on the Main Alarm Control and Display Panel illuminates.

13.52   Procedure

13.521 With the system in its present configuration, perform the steps in the General Procedure Instructions.

13.522 Request the TELCo to perform the system functions. Perform the steps in the General procedure Instructions after entering each new system configuration.

   A)   Restore the OOS CPU to STANDBY
   B)   Perform a system switch
   C)   Remove the new STANDBY CPU to OOS

13.6   Conclusion

13.61   This marks the end of testing in this handbook section. The TELCo can now restore the OOS CPU to STANDBY, if desired.

Manager, Product Engineering
Control Center

Reason for Reissue:
   To add configuration hardware
   tests to check cables and paths
   through TN102 circuit packs.