AMARS
#1A AUTOMATIC MESSAGE ACCOUNTING AND RECORDING CENTER
(NO. 1A AMARC)
GENERIC 2 TO GENERIC 3 RETROFIT PROCEDURE
(GENERIC 3 CABINET INSTALLATION)

CONTENTS

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1. GENERAL INFORMATION

1.1 This procedure does not require any direct connection to any DEC equipment. Therefore, DEC personnel or maintenance personnel need NOT be present during the execution of this handbook section procedure.

1.2 The J1P040D, J1P040V-1 List 1 and J1P040V-1 List 2 (if provided) cabinets should be in position prior to the start of this handbook section.

1.3 Power should be provided per Note 109 in SD-5P006-01.

1.4 Incorrect responses on the TTY when installing "Y" cables can be examined by referring to the Input and Output (IM/OM) manuals for the appropriate generic program issue.

1.5 Cabling

1.51 The TELCo should arrange to have their data facilities personnel present to make modem cable connections to the Generic 3 equipment or authorize Western Electric to perform this operation.

1.52 This procedure requires that a "Y" cable connection be made at the data set cabinet for all active dedicated channels. These "Y" cables are contained in the transition kit (TH-405-000). The TELCo should arrange to have its data facilities personnel present to make these cable connections or authorize Western Electric to perform this operation. The TELCo should also arrange to have their AMARC craft personnel available to switch channels to dial-up facilities while the "Y" cables are being installed or authorize Western Electric to perform this operation.

1.53 When connecting cables to the backplane, the triangle on the connector should always be on the bottom.

2. RECORDS AND REQUIREMENTS

2.1 The Test Trouble Record forms (SD-97-1313 and SD-97-1315) should be used to record all troubles which may be encountered when executing the tests in this handbook section.

3. TEST EQUIPMENT

3.1 One ITE-5632 digital Multimeter (or equivalent).

3.2 AMARC Phase 2 to Phase 3 conversion kit, TH-405-000 (transition kit).

3.3 One ITE-5237B Oscilloscope (or equivalent).

3.4 SPP-832 Spare parts package.

3.5 Input and Output (IM/OM) manuals for the associated Generic 2 program issue.

4. INSTALL "Y" CABLES

4.1 General

4.11 A "Y" cable from the transition kit must be inserted at the data set cabinet for all active dedicated channels on the system.

4.12 The procedure will be to switch a channel to dial backup, install the "Y" cable at the data set cabinet then restore the channel to its dedicated link. If TELCo is to perform these functions, proceed to Paragraph 5 after TELCo has completed the procedure.

4.13 All M25A type cables associated with the No. 1A AMARC Phase II should be run up the left side of the Data Set Cabinet as viewed from the rear.

4.2 Procedure

4.21 Switch one channel to dial backup (starting with Channel 001).

Note 1: Channels 000, 020, 040, 060, 100 and 120 are dial backup channels and will not have a "Y" cable installed.

Note 2: A No. 3 ESS dedicated backup channel cannot be switched to a backup channel. As long as the No. 3 ESS is being polled on its dedicated channel, the "Y" cable can be installed on its dedicated backup with no special procedure.

4.211 To switch a non-No. 3 ESS channel to dial backup, input the following on the Active Processor's TTY:

Input: SW CHL XXX DLP!
Response: SW CHL XXX DLP ... OK
where: XXX = dedicated channel number

4.212 To switch a No. 3 ESS channel to its dedicated backup channel (next higher sequential channel no.), input the following on the Active Processor's TTY:

Input: SW CHL XXX BKP!
Response: SW CHL XXX BKP OK
where: XXX = dedicated channel number

4.3 Disconnect the M25A cable for the associated dedicated channel at the data set cabinet.

4.4 Install the male connector of the "Y" cable to the associated dedicated channel connector at the data set cabinet.

4.5 Install the end of the M25A cable, removed in Paragraph 4.3, to one of the female connectors on the "Y" cable.

4.6 Restore the channel from backup to its dedicated link by inputting the following on the active processor's TTY:

Input: RST CHL XXX!
Response: RST CHL XXX
where: XXX = dedicated channel number.
Note: There is no need to restore a No. 3 ESS backup channel.

4.7 Repeat Paragraphs 4.22 through 4.6 for the next higher sequential channel until all active dedicated channels are completed.

5. INSTALLATION OF ALARM DISPLAY PANEL(S)

5.1 Main Alarm Control and Display Panel

5.11 The Main Alarm Control and Display Panel is to be mounted in the Processor Cabinet for CPU0. Refer to SD-5P006-01, Note 202 for mounting information.

5.12 Connect the ED-5P284-31 group 60 cables listed in Table 1 from the Main Alarm Control and Display Panel to the J1P040DB (CONT) Unit located in the J1P040D-1 Cabinet.

Note: Refer to SD-5P006-01, Note 202 for cable routing and cable tie information.

5.2 Auxiliary Alarm and Display Panel (If Provided)

5.21 The TELCo will provide the location information for the Auxiliary Alarm and Display Panel.

5.22 Connect the TELCo provided M25A cables, or equivalent, listed in Table 2 from the Auxiliary Alarm and Display Panel to the J1P040DB (CONT) Unit located in the J1P040D-1 Cabinet.

6. PRELIMINARY CABLING

6.1 Interframe Western Cabinet Cabling

6.11 Connect the ED-5P284-31 cables listed in Table 3 from the specified unit in the J1P040D-1 cabinet to the specified unit in the J1P040V-1, List 1 cabinet (if provided).

6.12 Connect the ED-5P284-31 cables listed in Table 4 from the specified unit in the J1P040D-1 Cabinet to the specified unit in the J1P040V-1, List 2 Cabinet (if provided).

TABLE 1

		FROM MAIN DISPLAY UNIT	TO J1 P040DB(CONT)	
DESIG	LOC	STAMPED	LOC	STAMPED
CB13	J1	MDISP - J1	16 - 032	CONT 16 - 032
CB14	J2	MDISP - J2	16 - 040	CONT 16 - 040
CB15	J3	MDISP - J3	16 - 112	CONT 16 - 112
CB16	J4	MDISP - J4	16 - 104	CONT 16 - 104

TABLE 2

FROM AUXILARY DISPLAY UNIT		TO J1P040DB (CONT)	
LOC	STAMPED	LOC	STAMPED
J1	ADISP - J1	16-016	CONT 16 - 016
J2	ADISP - J2	16-024	CONT 16 - 024
J3	ADISP - J3	16-120	CONT 16 - 120

TABLE 3

DESIG	GROUP	STAMPED	CONNECTED FROM		CONNECTED TO		STAMPED
			LOC	UNIT	LOC	UNIT	
*CB2-0	65	PULSE 04-058	TRMTC01 RCVC01 RERTN01	PULSE PULSE PULSE	TRMTC01 RCVC01 RERTN01	OASYN OASYN OASYN	OASYN
**CB2-1	65	PULSE 04-093	TRMTC11 RCVC11 RERTN11	PULSE PULSE PULSE	TRMTC11 RCVC11 RERTN11	OASYN OASYN OASYN	OASYN
CB2	57	OACU-06-010-Q2	06-010-Q2	OACU	06-010-Q3	OASYN	OASYN-06-010-Q3
CB4	57	ALM-10-082-Q4	10-082-Q4	ALM	06-010-Q3	TTY	TTY-06-010-Q3
*CB4-0	65	PULSE 04-058	RCVC04 RCVC04 RERTN04	PULSE PULSE PULSE	TRMTC04 RCVC04 RERTN04	TTY TTY TTY	TTY(VO)
**CB4-1	65	PULSE 04-093	RCVC14 RCVC14 RERTN14	PULSE PULSE PULSE	TRMTC14 RCVC14 RERTN14	TTY TTY TTY	TTY(VO)
CB21	74(M25A cable)	OPWR/FLT 04-090	NOTE 1		02-016	TTY	TTY 02-016
CB22	74(M25A cable)	ALM 02-024	02-024	ALM	14-016	TTY	TTY 14-016

* The wire from the shield on this cable is connected in the J1P040D-1 Cabinet at GND BUS 0.
** The wire from the shield on this cable is connected in the J1P040D-1 Cabinet at GND BUS 1.

NOTE 1: Route this cable end to the area of the SH11 circuit pack at location 03-090 in the OPWR/FLT unit, with no connection made.

TABLE 4

DESIG	GROUP	STAMPED	CONNECTED FROM LOC	CONNECTED FROM UNIT	CONNECTED TO LOC	CONNECTED TO UNIT	STAMPED
*CB3-0	65	PULSE 04-058	TRMTC02 RCVC02 RERTN02	PULSE PULSE PULSE	TRMTC02 RCVC02 RERTN02	1 ACU 1 ACU 1 ACU	1 ACU
**CB3-1	65	PULSE 04-093	TRMTC12 RCVC12 RERTN12	PULSE PULSE PULSE	TRMTC12 RCVC12 RERTN12	1 ACU 1 ACU 1 ACU	1 ACU
CB3	57	ALM-10-082-Q2	10-082-Q2	ALM	06-010-Q3	SEE NOTE 1	To Bottom Most Equipped Unit 06-010-Q3

* The wire from the shield on this cable is connected in the J1P040D-1 Cabinet at GND BUS 0.
** The wire from the shield on this cable is connected in the J1P040D-1 Cabinet at GND BUS 1.

NOTE 1: CB3 connects from the ALM unit to the bottom most unit designated 2 ASYN or 1 ACU in the J1P040V-1, List 2 Cabinet.

6.2 Install DR11 Input Shorting Plugs

6.21 The DR11 input shorting plugs are contained within the TH-405-000 (transition kit).

6.22 Install the DR11 input shorting plugs on the Control Unit (CONT) positions 20-021, 20-027, 20-089 and 20-095.

7. FUSE AND POWER "D" CABINET

7.1 Power Transfer Unit

7.101 Power for the Processor Interface Cabinet is supplied by the Power Transfer Unit. The Power Transfer Unit obtains power from a single-phase receptacle at the power distribution circuit. J0 and J1 receptacles on the unit receive plugs from the power strip within the cabinet. Do not connect power to the Power Transfer Unit until specified in the following paragraphs.

7.102 Remove all plugs from outlets on both sides of the Processor Interface Unit.

7.103 Disengage all circuit packs in the Control Unit (J1P040DB), Alarm Unit (J1P040DF), ACU Interface Unit (J1P040DD), Isolation Pulse Unit (J1P040DE) and the Power Transfer and Static Filter Unit (J1P040DG).

7.104 Verify that 'PWR Cord 0' is connected from the receptacle 1 on the side 0 power strip to the J0 outlet on the Power Transfer Unit.

7.105 Verify that 'PWR Cord 1' is connected from the receptacle 1 on the side 1 power strip to the J1 outlet on the Power Transfer Unit.

7.106 Connect the power cord P0 from the Power Transfer Unit to the receptacle for the Processor Interface Cabinet associated with CPU0. Verify that the pilot lamp at the top of both power strips is illuminated. If the pilot lamps are not illuminated, depress the circuit breaker button on top of the associated power strip. Verify that 120 VAC is obtained at all outlets on both sides of the Processor Interface Cabinet.

7.107 Remove the AC0 fuse. Verify that 120 VAC has been removed from all outlets on side 0 of the Processor Interface Cabinet. Side 1 side should still retain power.

7.108 Remove power cord P0 from the receptacle.

7.109 Restore the AC0 fuse.

7.110 Connect power cord P1 to the receptacle for the Processor Interface Cabinet associated with CPU1. Verify that 120 VAC is obtained at all outlets on both sides of the Processor Interface Cabinet.

7.111 Remove the AC1 fuse. Verify that 120 VAC has been removed from all outlets on side 1 of the Processor Interface Cabinet. Side 0 should still retain power.

7.112 Restore the AC1 fuse.

7.113 Restore power cord P0 to the receptacle for the Processor Interface Cabinet associated with CPU0.

7.2 Fuse and DC Power

7.201 Remove fuses A0, B0, C0, D0, E0, F0, A1, B1, C1, D1, E1 and F1.

7.202 Verify that all fuses for the 0 PWR SUPP power supply at the top of the frame are in place.

7.203 Connect the plug from the 0 PWR SUPP power supply for side 0 to outlet 16 on side 0.

7.204 Connect the plug from the 0 PWR SUPP power supply for side 1 to outlet 16 on side 1.

7.205 Connect the plug from the +28v power supply PS0 located in the PULSE Unit to outlet 4 on side 0.

7.206 Connect the plug from the +28v power supply PS1 located in the PULSE unit to outlet 4 on side 1.

7.207 Operate both power switches on the 0 PWR SUPP power supply to the ON position.

7.208 Verify that no power on ground conditions exist on any of the +5v, +12v or -12v terminals of TB1 and TB3. Refer to SD-5P012-01, FS3 if necessary.

7.209 Insert an operated fuse, one at at time, into the fuse holder, listed in Table 7.209, and observe that the associated LED indicator, listed in Table 7.209, illuminates.

TABLE 7.209

SIDE 0		SIDE 1	
FUSE HOLDER	LED	FUSE HOLDER	LED
A0	+5V0	A1	+5V1
C0	+12V0	C1	+12V1
D0	+12V0	D1	+12V1
E0	-12V0	E1	-12V1
F0	-12V0	F1	-12V1

7.210 Restore all fuses that were removed in Paragraph 7.201.

7.211 Use the Digital Voltmeter to adjust the +12v, -12v and +5v outputs of the 0 PWR SUPP power supply as accurately as possible. Verify these voltages at the terminals given in Table 7.211. Refer to SD-5P012-01, FS3 if required.

TABLE 7.211

VOLT	RANGE	SIDE	LOCATION	TERMINAL
+5	4.75v to 5.25v	0	TB2	1
+5	4.75v to 5.25v	1	TB4	1
-12	-11.4v to -12.6v	0	TB2	3
-12	-11.4v to -12.6v	1	TB4	3
+12	+11.4v to +12.6v	0	TB2	2
+12	+11.4v to +12.6v	1	TB4	2

NOTE: Output voltages must be adjusted as accurately as possible to +5v and ±12v. There is an adjustment potentiometer on the 0 PWR SUPP supply that can be used for adjustments.

7.212 Verify +28v ±2v is obtained by measuring between the +28 V0 and +28 RT0 bugs on PULSE unit side 0 and between the +28 V1 and +28 RT1 bugs on PULSE unit side 1, located on the backplane of the PULSE unit. Refer to SD-5P020-01, FS3 if necessary.

7.213 Verify that power is supplied to both sides of all units within the Processor Isolation Cabinet. Refer to Table 7.213 for available voltages on specific units. Verify between the voltage bug and the GND bug.

Table 7.213

UNIT	VOLTAGE	LOCATION
CONT	+5v	+5v BUG
CONT	+12v	+12v BUG
ALM	+5v	+5v BUG
ALM	+12v	+12v BUG
ALM	-12v	-12v BUG
OACU	+12v	+12v BUG
OACU	-12v	-12v BUG
PULSE	+12v	+12V0 and +12V1
PULSE	+5v	+5V0 and +5V1

7.214 Turn the two power switches on the 0 PWR SUPP power supply to the OFF position. Remove the plug for the +28v power supplies from outlet 4 on both sides. Insert all circuit packs in the Control Unit (J1P040DB), Alarm Unit (J1P040DF), ACU Interface Unit (J1P040DD), Isolation Pulse Unit (J1P040DE) and the Power Transfer and Static Filter Unit (J1P040DG). Restore power using the two switches on the 0 PWR SUPP power supply and reinsert the +28v power supply plugs.

7.215 Remove the F1 fuse located on the SN3 circuit pack in the PULSE unit one at a time and verify that the associated PWR on LED extinguishes. Restore the F1 fuses.

7.3 Power Transfer Test

7.31 Remove power cord P0 from the receptacle for the Processor Interface Cabinet associated with CPU0.

7.32 Observe that the TRNSFR0 LED illuminate on the SH9 circuit pack located in the OPWR/FLT unit.

7.33 Restore power cord P0. The TRNSFR0 LED should extinquish.

7.34 Remove power cord P1 from the receptacle for the Processor Interface Cabinet associated with CPU1.

7.35 Observe that the TRNSFR1 LED illuminate on the SH9 circuit pack located in the OPWR/FLT unit.

7.36 Restore power cord P1. The TRNSFR1 LED should extinquish.

7.4 Power Supply Failure Test

7.41 Verify that the ACFL0 and ACFL1 LEDs on the SH9 circuit pack in the OPWR/FLT unit are extinquished.

7.42 Operate the power switch on the 0 PWR SUPP associated with side 0 to the 'OFF' position.

7.43 Verify that the ACFL0 LED on the SH9 circuit pack in the OPWR/FLT unit illuminates.

7.44 Restore the power switch on the 0 PWR SUPP to the 'ON' position. The ACFL0 LED should extinquish.

7.45 Operate the power switch on the 0 PWR SUPP associated with side 1 to the 'OFF' position.

7.46 Verify that the ACFL1 LED on the SH9 circuit pack in the OPWR/FLT unit illuminates.

7.47 Restore the power switch on the 0 PWR SUPP to the 'ON' position. The ACFL1 LED should extinquish.

8. FUSE AND POWER "V0" CABINET

8.1 Power Transfer Unit

8.101 Power for the First Supplementary Processor Interface Cabinet is supplied by the Power Transfer Unit. The Power Transfer Unit obtains power from a single phase receptacle at the power distribution circuit. J0 and J1 receptacles on the unit receive plugs from the power strip within the cabinet. Do not connect power to the Power Transfer Unit until specified in the following paragraphs.

8.102 Remove all plugs from outlets on both sides of the First Supplementary Processor Interface Cabinet.

8.103 Disengage all circuit packs in the Asynchronous Interface Unit (J1P040DC) (0 ASYN and 1 ASYN), Asynchronous Interface Unit (TTY) (J1P040DC), and Power Transfer and Static Filter Unit (J1P040DG).

8.104 Verify the 'PWR CORD 0' is connected from the receptacle 1 on the side 0 power strip to the J0 outlet on the Power Transfer Unit.

8.105 Verify that 'PWR CORD 1' is connected from the receptacle 1 on the side 1 power strip to the J1 outlet on the Power Transfer Unit.

8.106 Connect the power cord P0 from the Power Transfer Unit to the receptacle for the First Supplementary Processor Interface Cabinet associated with CPU0. Verify that the pilot lamp at the top of both power strips is illuminated. If the pilot lamps are not illuminated, depress the circuit breaker button on top of the associated power strip. Verify that 120VAC is obtained at all outlets on both sides of the First supplementary Processor Interface Cabinet.

8.107 Remove the AC0 fuse. Verify that 120VAC has been removed from all outlets on side 0 of the First Supplementary Processor Interface Cabinet. Side 1 should still retain power.

8.108 Remove power cord P0 from the receptacle.

8.109 Restore the AC0 fuse.

8.110 Connect power cord P1 to the receptacle for the First Supplementary Processor Interface Cabinet associated with

8.110 Cont'd

CPU1. Verify that 120VAC is obtained at all outlets on both sides of the First Supplementary Processor Interface Cabinet.

8.111 Remove the AC1 fuse. Verify that 120VAC has been removed from all outlets on side 1 of the First Supplementary Processor Interface Cabinet. Side 0 should still retain power.

8.112 Restore the AC1 fuse.

8.113 Restore power cord P0 to the receptacle for the First Supplementary Processor Interface Cabinet associated with CPU0.

8.2 Fuse and DC Power

8.201 Remove the D0, F0, D1 and F1 fuses.

8.202 Verify that all the fuses for the 1 PWR SUPP at the top of the frame are in place.

8.203 Connect the plug for the 1 PWR SUPP for side 0 to outlet 16 on side 0.

8.204 Connect the plug for the 1 PWR SUPP for side 1 to outlet 16 on side 1.

8.205 Operate both power switches on the 1 PWR SUPP power supply to the ON position.

8.206 Verify that no power or ground conditions exist on any of the +12v or -12v terminals on TB1 or TB3. Refer to SD-5P016-01, FS3, if necessary.

8.207 Insert an operated fuse, one at a time, into the fuse holder, listed in Table 8.207, and observe that the associated LED indicator listed in Table 8.207 illuminates.

TABLE 8.207

SIDE 0		SIDE 1	
FUSE HOLDER	LED	FUSE HOLDER	LED
D0	+12V0	D1	+12V1
F0	-12V0	F1	-12V1

8.208 Restore all fuses that were removed in Paragraph 8.201.

8.209 Verify the voltages at the terminals given in Table 8.209. Refer to SD-5P012-01, FS3, if necessary.

TABLE 8.209

VOLTAGE	RANGE	SIDE	LOC.	TERMINAL
+12v	+11.4v to +12.6v	0	TB1	7
+12v	+11.4v to +12.6v	1	TB3	7
-12v	-11.4v to -12.6v	0	TB1	10
-12v	-11.4v to -12.6v	1	TB3	10

NOTE: The output voltage must be within the range indicated. There is an adjustment potentiometer on the 1 PWR SUPP that can be used for adjustment.

8.210 Verify that power is supplied to both sides of all units within the First Supplementary Processor Interface Cabinet. Refer to Table 8.210 for available voltages on the specified units. Verify between the voltage bug and the GND bug.

TABLE 8.210

UNIT	VOLTAGE	LOCATION
0ASYN	+12v	+12v BUG
0ASYN	-12v	-12v BUG
1ASYN	+12v	+12v BUG
1ASYN	-12v	-12v BUG
TTY	+12v	+12v BUG
TTY	-12v	-12v BUG

8.211 Turn the two power switches on the 1 PWR SUPP power supply to the OFF position. Insert all circuit packs in the Asynchronous Interface Units (0 ASYN and 1 ASYN) (J1P040DC), Asynchronous Interface Unit (TTY) (J1P040DC) and the Power Transfer and Static Filter Unit (1 PWR/FLT) (J1P040DG). Restore power using the two switches on the 1 PWR SUPP power supply.

8.3 Power Transfer Test

8.31 Remove power cord P0 from the receptacle for the First Supplementary Processor Interface Cabinet associated with CPU0.

8.32 Observe that the TRNSFR0 LED illuminate on the SH9 circuit pack located in the 1 PWR/FLT unit.

8.33 Restore power cord P0. The TRNSFR0 LED should extinquish.

8.34 Remove power cord P1 from the receptacle for the First Supplementary Processor Interface Cabinet associated with CPU1.

8.35 Observe that the TRNSFR1 LED illuminate on the SH9 circuit pack located in the 1 PWR/FLT unit.

8.36 Restore power cord P1. The TRNSFR1 LED should extinquish.

8.4 Power Supply Failure Test

8.41 Verify that the ACFL0 and ACFL1 LEDs on the SH9 circuit pack in the 1 PWR/FLT unit are extinquished.

8.42 Operate the power switch on the 1 PWR SUPP associated with side 0 to the 'OFF' position.

8.43 Verify that the ACFL0 LED on the SH9 ciruit pack in the 1 PWR/FLT unit illuminates.

8.44 Restore the power switch on the 1 PWR SUPP to the 'ON' position. The ACFL0 LED should extinquish.

8.45 Operate the power switch on the 1 PWR SUPP associated with side 1 to the 'OFF' position.

8.46 Verify that the ACFL1 LED on the SH9 circuit pack in the 1 PWR/FLT unit illuminates.

8.47 Restore the power switch on the 1 PWR SUPP to the 'ON' position. The ACFL1 LED should extinquish.

9. FUSE AND POWER "V1" CABINET

9.1 Power Transfer Unit

9.101 Power for the Second Supplementary Processor Interface Cabinet is supplied by the Power Transfer Unit. The Power Transfer Unit obtains power from a single phase receptacle at the power distribution circuit. J0 and J1 receptacles on the unit receive plugs from the power strip within the cabinet. Do not connect power to the Power Transfer Unit until specified in the following paragraphs.

9.102 Remove all plugs from outlets on both sides of the Second Supplementary Processor Interface Cabinet.

9.103 Disengage all circuit packs in the Asynchronous Interface Unit (2 ASYN) (J1P040DC), the ACU Interface Unit (1 ACU) (J1P040DD) and the Power Transfer and Static Filter Unit (2 PWR/FLT) (J1P040DG).

9.104 Verify the 'PWR CORD 0' is connected from the receptacle 1 on the side 0 power strip to the J0 outlet on the Power Transfer Unit.

9.105 Verify that 'PWR CORD 1' is connected from the receptacle 1 on the side 1 power strip to the J1 outlet on the Power Transfer Unit.

9.106 Connect the power cord P0 from the Power Transfer Unit to the receptacle for the Second Supplementary Processor Interface Cabinet associated with CPU0. Verify that the pilot lamp at the top of both power strips is illuminated. If the pilot lamps are not illuminated, depress the circuit breaker button on top of the associated power strip. Verify that 120VAC is obtained at all outlets on both sides of the Second Supplementary Processor Interface Cabinet.

9.107 Remove the AC0 fuse. Verify that 120VAC has been removed from all outlets on side 0 of the Second Supplementary Processor Interface Cabinet. Side 1 should still retain power.

9.108 Remove power cord P0 from the receptacle.

9.109 Restore the AC0 fuse.

9.110 Connect power cord P1 to the receptacle for the Second Supplementary Processor Interface Cabinet associated with CPU1. Verify that 120VAC is obtained at all outlets on both sides of the Second Supplementary Processor Interface Cabinet.

9.111 Remove the AC1 fuse. Verify that 120VAC has been removed from all outlets on side 1 of the Second Supplementary Processor Interface Cabinet. Side 0 should still retain power.

9.112 Restore the AC1 fuse.

9.113 Restore power cord P0 to the receptacle for the Second Supplementary Processor Interface Cabinet associated with CPU0.

9.2 Fuse and DC Power

9.201 Remove the D0, F0, D1 and F1 fuses.

9.202 Verify that all the fuses for the 2 PWR SUPP at the top of the frame are in place.

9.203 Connect the plug for the 2 PWR SUPP for side 0 to outlet 16 on side 0.

9.204 Connect the plug for the 2 PWR SUPP for side 1 to outlet 16 on side 1.

9.205 Operate both power switches on the 2 PWR SUPP power supply to the ON position.

9.206 Verify that no power or ground conditions exist on any of the +12v or -12v terminals on TB1 or TB3. Refer to SD-5P016-01, FS3, if necessary.

9.207 Insert an operated fuse, one at a time, into the fuse holder, listed in Table 9.207, and observe that the associated LED indicator listed in Table 9.207 illuminates.

TABLE 9.207

SIDE 0		SIDE 1	
FUSE HOLDER	LED	FUSE HOLDER	LED
D0	+12V0	D1	+12V1
F0	-12V0	F1	-12V1

9.208 Restore all fuses that were removed in Paragraph 9.201.

9.209 Verify the voltages at the terminals given in Table 9.209. Refer to SD-5P012-01, FS3, if necessary.

TABLE 9.209

VOLTAGE	RANGE	SIDE	LOC.	TERMINAL
+12v	+11.4v to +12.6v	0	TB1	7
+12v	+11.4v to +12.6v	1	TB3	7
-12v	-11.4v to -12.6v	0	TB1	10
-12v	-11.4v to -12.6v	1	TB3	10

NOTE: The output voltage must be within the range indicated. There is an adjustment potentiometer on the 2 PWR SUPP that can be used for adjustment.

9.210 Verify that power is supplied to both sides of all units within the Second Supplementary Processor Interface Cabinet. Refer to Table 9.210 for available voltages on the specified units. Verify between the voltage bug and the GND bug.

TABLE 9.210

UNIT	VOLTAGE	LOCATION
2ASYN	+12v	+12v BUG
2ASYN	-12v	-12v BUG
1ACU	+12v	+12v BUG
1ACU	-12v	-12v BUG

9.211 Turn the two power switches on the 2 PWR SUPP power supply to the OFF position. Insert all circuit packs in the Asynchronous Interface Units (2 ASYN) (J1P040DC), ACU Interface Unit (1ACU) (J1P040DD) and the Power Transfer and Static Filter Unit (2PWR/FLT) (J1P040DG). Restore power using the two switches on the 2 PWR SUPP power supply.

9.3 Power Transfer Test

9.31 Remove power cord P0 from the receptacle for the Second Supplementary Processor Interface Cabinet associated with CPU0.

9.32 Observe that the TRNSFR0 LED illuminate on the SH9 circuit pack located in the 2 PWR/FLT unit.

9.33 Restore power cord P0. The TRNSFR0 LED should extinquish.

9.34 Remove power cord P1 from the receptacle for the Second Supplementary Processor Interface Cabinet associated with CPU1.

9.35 Observe that the TRNSFR1 LED illuminate on the SH9 circuit pack located in the 2 PWR/FLT unit.

9.36 Restore power cord P1. The TRNSFR1 LED should extinquish.

9.4 Power Supply Failure Test

9.41 Verify that the ACFL0 and ACFL1 LEDs on the SH9 circuit pack in the 2PWR/FLT unit are extinquished.

9.42 Operate the power switch on the 2 PWR SUPP associated with side 0 to the 'OFF' position.

9.43 Verify that the ACFL0 LED on the SH9 circuit pack in the 2 PWR/FLT unit illuminates.

9.44 Restore the power switch on the 2 PWR SUPP to the 'ON' position. The ACFL0 LED should extinquish.

9.45 Operate the power switch on the 2 PWR SUPP associated with side 1 to the 'OFF' position.

9.46 Verify that the ACFL1 LED on the SH9 circuit pack in the 2 PWR/FLT unit illuminates.

9.47 Restore the power switch on the 2 PWR SUPP to the 'ON' position. the ACFL1 LED should extinquish.

10. PRELIMINARY PANEL EXERCISE

10.1 General

10.11 The PROCESSOR, INTERFACE, ISOLATION OVERRIDE switches and the EXECUTE button for CPU0 and CPU1 are located on the Main Alarm Control and Display Panel. To put the system into a particular state, the appropriate switch is operated; then the EXECUTE button will be depressed; then the switch and the EXECUTE button will be released.

10.2 Isolation Override Restore Status

10.21 Using the panel, first place CPU0 and CPU1 into the ISOLATION OVERRIDE state, then, release CPU0 and CPU1 from the ISOLATION OVERRIDE state.

10.22 Depress the RETIRE ALARMS button.

10.23 Verify that the red CRITICAL, both red PROGRAM TIMEOUT and both green NORMAL LED's are illuminated on the panel.

NOTE: Disregard other LED's.

10.24 Verify the proper illumination of LED's in the Alarm and Control Units as listed in Step 1 of Table 5.

10.25 All TN102 circuit packs in all the ACU units and all the ASYN units should have their red LED's illuminated.

10.26 All TN102 circuit packs in the TTY unit should have their green LED's illuminated.

10.27 The green "PWR ON" LED's on the SN3 circuit packs in the PULSE unit should be illuminated.

10.3 Test Panel

10.31 Depress and hold the "TEST LAMPS and AUDIBLE" button on the panel.

10.32 All LED's on the panel should illuminate.

10.33 All red "FAULT" LED's on circuit packs in the Alarm and Control Unit should illuminate.

10.34 The red "FAULT" LED's on both SN3 circuit packs in the PULSE unit should illuminate.

10.35 Release the "TEST LAMPS AND AUDIBLE" button.

10.4 Alarm Cutoff

10.41 Verify that none of the amber LED's above the alarm cutoff buttons are illuminated. Depress the associated alarm cut-off button once to extinguish any LED's that are illuminated, if necessary.

10.42 Using the panel, place CPU0 into the INTERFACE ISOLATE state.

10.43 Depress each alarm cutoff button on the panel (CUTOFF AUDIBLE ALARM, CUTOFF BUILDING ALARM, CUTOFF REMOTE ALARMS). The amber LED above each alarm cutoff button should remain illuminated.

10.44 Depress each alarm cutoff button on the panel, again. The amber LED above each alarm cutoff button should extinguish.

10.45 Restore CPU0 from the INTERFACE ISOLATE state.

10.46 Using the panel, place CPU1 into the INTERFACE ISOLATE state.

10.47 Repeat Paragraphs 10.43 and 10.44.

10.48 Using the panel, restore CPU1 from the INTERFACE ISOLATE state.

10.49 Depress "RETIRE ALARMS" to silence the alarms, if necessary.

10.5 Processor Isolate

10.51 CPU0 side

10.511 Using the panel, place CPU0 into the PROCESSOR ISOLATE state.

10.512 Verify the proper illumination of LED's in the Alarm and Control Units as listed in Step 2 of Table 5.

10.513 All TN102 circuit packs in all the ACU units and all the ASYN units should have their red LED's illuminated.

10.514 All TN102 circuit packs associated with CPU0 in the TTY unit should have their red LED's illuminated.

10.515 All TN102 circuit packs associated with CPU1 in the TTY unit should have their green LED's illuminated.

10.516 Using the panel, release CPU0 from the PROCESSOR ISOLATE state.

10.52 CPU1 side

10.521 Using the panel, place CPU1 into the PROCESSOR ISOLATE state.

10.522 Verify the proper illumination of LED's in the Alarm and Control Units as listed in Step 3 of Table 5.

10.523 All TN102 circuit packs in all the ACU units and all the ASYN units should have their red LED's illuminated.

10.524 All TN102 circuit packs associated with CPU0 in the TTY unit should have their green LED's illuminated.

10.525 All TN102 circuit packs associated with CPU1 in the TTY unit should have their red LED's illuminated.

10.526 Using the panel, restore CPU1 from the PROCESSOR ISOLATE state.

10.6 Interface Isolate and Override

10.61 CPU0 side

10.611 Using the panel place CPU0 into the INTERFACE ISOLATE state.

10.612 Verify the proper illumination of LED's in the Alarm and Control Units as listed in Step 4 of Table 5.

10.613 TN102 circuit packs. All TN102 circuit packs in all the ACU units and all the ASYN units should have their red LED's illuminated. All TN102 circuit packs associated with CPU0 in the TTY unit should have their red LED's illuminated. All TN102 circuit packs associated with CPU1 in the TTY unit should have their green LED's illuminated.

10.614 Using the panel, place CPU0 into the ISOLATION OVERRIDE state while still in the INTERFACE ISOLATE state.
Note: The red LED's on the panel above the INTERFACE ISOLATE and ISOLATION OVERRIDE switches should be illuminated.

10.615 Verify the proper illumination of LED's in the Alarm and Control Units listed in Step 5 of Table 5.

10.616 TN102 circuit packs. All TN102 circuit packs associated with CPU0 in all ACU units and all ASYN units should have their green LED's illuminated. All TN102 circuit packs in the TTY unit should have their green LED's illuminated.

10.617 Using the panel, release CPU0 from the ISOLATION OVERRIDE state. The LED status should return to the same values as listed in Paragraphs 10.612 and 10.613.

10.618 Using the panel, release CPU0 from the INTERFACE ISOLATE state.

10.62 CPU1 side

10.621 Using the panel, place CPU1 into the INTERFACE ISOLATE state.

10.622 Verify the proper illumination of LED's in the Alarm and Control Units as listed in Step 6 of Table 5.

10.623 TN102 circuit packs. All TN102 circuit packs in all the ACU units and all the ASYN units should have their red LED's illuminated. All TN102 circuit packs associated with CPU0 in the TTY unit should have their green LED's illuminated. All TN102 circuit packs associated with CPU1 in the TTY unit should have their red LED's illuminated.

10.624 Using the panel, place CPU1 into the ISOLATION OVERRIDE state while still in the INTERFACE ISOLATE state.
Note: The red LED's on the panel above the INTERFACE ISOLATE and ISOLATION OVERRIDE switches should be illuminated.

10.625 Verify the proper illumination of LED's in the Alarm and Control Units listed in Step 7 of Table 5.

10.626 TN102 circuit packs. All TN102 circuit packs associated with CPU1 in all ACU units and all ASYN units should have their green LED's illuminated. All TN102 circuit packs in the TTY unit should have their green LED's illuminated.

10.627 Using the panel, release CPU1 from the ISOLATION OVERRIDE state. The LED status should return to the same values as listed in Paragraphs 10.622 and 10.623.

10.628 Using the panel, release CPU1 from the INTERFACE ISOLATE state.

TABLE 5

STEP	CONT UNIT, LOCATION 22-						ALM UNIT, LOC. 08-							
	032	038	044	100	106	112	032	038	056 (IF TN198)	056 (IF TN198B)	100	106	124 (IF TN198)	124 (IF TN198B)
1	NORM	NORM	OFF	NORM	NORM	OFF	G	R,G	OFF	ISLT	G	R,G	OFF	ISLT
2	PROC	PROC	ISLT	NORM	NORM	OFF	R	R	OFF	ISLT	G	R	OFF	ISLT
3	NORM	NORM	OFF	PROC	PROC	ISLT	G	R	OFF	ISLT	R	R	OFF	ISLT
4	ISLT	NORM	ISLT	NORM	NORM	OFF	R	R	OFF	ISLT	G	R	OFF	ISLT
5	ISLT	NORM	ISLT	NORM	NORM	OFF	R	R	OVRD	OVRD, NORM	G	R	OFF	ISLT
6	NORM	NORM	OFF	ISLT	NORM	ISLT	G	R	OFF	ISLT	R	R	OFF	ISLT
7	NORM	NORM	OFF	ISLT	NORM	ISLT	G	R	OFF	ISLT	R	R	OVRD	OVRD, NORM

R = Red LED
G = Green LED
A = Amber LED
OFF = All LED's off

10.7 DC Power/Panel Tests

10.71 V0 Cabinet DC Power Removal Side 0

10.711 At the V0 cabinet, 1 PWR SUPP, turn DC power off to the CPU0 side.

10.712 Verify that the red INTERFACE MAJOR LED is illuminated on the panel.

10.713 At the Alarm and Control unit circuit packs verify that the red "V" LED at location 08-050 and the red "FAULT" LED's at location 08-056 and 22-062 are illuminated.

10.714 Verify at the PULSE unit in the J1P040D cabinet that the circuit pack at location 04-54 has its red and green LED's illuminated.

10.715 Verify that the ACFL0 LED on the SH9 circuit pack in the 1 PWR/FLT unit illuminates.

10.716 Restore DC power to the V0 cabinet CPU0 side.

10.717 Depress RETIRE ALARMS at the panel. Verify that all LED's listed in Paragraphs 10.712 through 10.715 have extinguished.

10.72 V0 Cabinet DC Power Removal Side 1

10.721 At the V0 cabinet, 1 PWR SUPP, turn DC power off to the CPU1 side.

10.722 Verify that the red INTERFACE MAJOR LED is illuminated at the panel.

10.723 At the Alarm and Control unit circuit packs verify that the red "V" LED at location 08-118 and the red "FAULT" LED's at locations 08-124 and 22-130 are illuminated.

10.724 Verify at the Pulse unit in the J1P040D cabinet that the circuit pack at location 04-98 has its red and green LED's illuminated.

10.725 Verify that the ACFL1 LED on the SH9 circuit pack in the 1 PWR/FLT unit illuminates.

10.726 Restore DC power to the V0 cabinet CPU1 side.

10.727 Depress RETIRE ALARMS at the panel. Verify that all LED's listed in Paragraphs 10.722 through 10.725 have extinguished.

10.73 V1 Cabinet Power Removal

10.731 Repeat Paragraphs 10.71 through 10.72 using the V1 cabinet and its 2 PWR SUPP for DC power removal.
Note: The ACFL0 and ACFL1 LED's for the V1 cabinet are located on the SH9 circuit pack in the 2 PWR/FLT unit.

10.8 AC Power/Panel Tests

10.81 These tests will require the removal and restoral of the AC power plugs from the UPS for each cabinet. The procedure will be as follows:

A) The AC power plug for the 0 side of the cabinet under test should be unplugged.
B) Verify, at the panel, that the AUXILIARY MAJOR red LED illuminates.
C) Verify at the associated cabinet PWR TRANSFER unit that its amber TRANSFER LED illuminates.
D) Restore the power plug then depress RETIRE ALARMS at the panel. The status of the LED's tested in Steps B and C should extinguish.
E) Repeat the above procedure for the 1 side of the cabinet under test.

10.82 Procedure

10.821 Execute the procedure listed in Paragraph 10.81 first using the J1P040D cabinet; then the J1P040V-1, List 1 cabinet; and then the J1P040V-1, List 2 cabinet.

11. RUN DATA SET AND ACU MODEM CABLES

11.1 General

11.11 All connections and cables to the data set cabinet are the responsibility of the TELCo. The TELCo should arrange to have their data facilities personnel present to make the cable connections or authorize Western Electric to perform this operation. These cables are M25A type cables.

11.12 The modem cables associated with the Generic 3 are to be run under the false floor and up into the data set cabinets (These cords are a permanent installation). These cables should be run up the right side of the data set cabinet as viewed from the rear. The cables should be clearly labeled with the channel number and Generic number. Do NOT connect these cables in the data set cabinet at this time. The cables should be connected in the J1P040D, J1P040V-1 List 1 and J1P040V-1 List 2 cabinets.

11.2 Procedure

11.21 Take special note. Do NOT connect any modem cables associated with the Generic 3 equipment in the Data Set Cabinet(s).

11.22 If the TELCo is to connect and run the modem cables for the Generic 3 equipment, proceed to Paragraph 12.

11.23 The modem cables should be connected in the J1P040D, J1P040V-1 List 1 and J1P040V-1 List 2 cabinets. Refer to the dedicated channel table and the ACU channel table for connector location information. The dedicated channel numbers are interpreted as "channel XXY" (where XX = multiplexer no., Y = channel on the multiplexer).

DEDICATED CHANNEL TABLE

FOR MUX #	CONNECTOR END MARKED CHL--0	CHL--1	CHL--2	CHL--3	CHL--4	CHL--5	CHL--6	CHL--7
	CONNECT IN V0 CABINET (0 ASYN) TO EQUIPMENT LOCATION							
00	02-016	14-016	02-024	14-024	02-032	14-032	02-040	14-040
01	02-048	14-048	02-056	14-056	02-064	14-064	02-072	14-072
02	02-080	14-080	02-088	14-088	02-096	14-096	02-104	14-104
03	02-112	14-112	02-120	14-120	02-128	14-128	02-136	14-136
	CONNECT IN V0 CABINET (1 ASYN) TO EQUIPMENT LOCATION							
04	02-016	14-016	02-024	14-024	02-032	14-032	02-040	14-040
05	02-048	14-048	02-056	14-056	02-064	14-064	02-072	14-072
06	02-080	14-080	02-088	14-088	02-096	14-096	02-104	14-104
07	02-112	14-112	02-120	14-120	02-128	14-128	02-136	14-136
	CONNECT IN V1 CABINET (2 ASYN) TO EQUIPMENT LOCATION							
10	02-016	14-016	02-024	14-024	02-032	14-032	02-040	14-040
11	02-048	14-048	02-056	14-056	02-064	14-064	02-072	14-072
12	02-080	14-080	02-088	14-088	02-096	14-096	02-104	14-104
13	02-112	14-112	02-120	14-120	02-128	14-128	02-136	14-136

ACU CHANNEL TABLE

ACU NO.	CONNECT TO 0ACU UNIT LOC.	ACU NO.	CONNECT TO 1ACU UNIT LOC.
0	02-016	10	02-016
1	02-032	11	02-032
2	02-048	12	02-048
3	02-064	13	02-064
4	02-080	14	02-080
5	02-096	15	02-096
6	02-112	16	02-112
7	02-128	17	02-128

12. CABINET CABLING

12.1 General

12.11 The ribbon peripheral cables for the cabinet are to be run to the area of the switch panel in the associated DEC asynchronous channel cabinet or to the cabinet which contains the DEC peripherals to which these cables connect. Do NOT run or connect any ribbon cables associated with the DN11's or the 0ACU Unit (these cables will be used for testing and will be connected in a later handbook section).

12.12 Do NOT connect any ribbon cables to the DEC equipment or the switch panel. Only route to the proper area.

12.13 The coaxial cable for the DMC11 for Generic 3 will be routed under the floor to the associated processor cabinet. This cable end will be temporarily tied inside the processor cabinet.

12.2 Procedure

12.21 Table 6 shows the cables that are to be connected and routed for the CPU0 side.

NOTE: Refer to NOTES 3 and 4 in TABLE 6 associated with cables CB36-0 and CB38-0.

12.22 Table 7 shows the cables that are to be connected and routed for the CPU1 side.

NOTE: Refer to NOTES 3 and 4 in TABLE 7 associated with cables CB36-1 and CB38-1.

TABLE 6

DESIG.	GROUP	STAMPED	CONNECTED FROM LOC.	CONNECTED FROM UNIT	ROUTE TO AREA OF	STAMPED
* CB20-0	58	ALM 02-060	02-060	ALM	TRMT DMC11MA	CPU0 DMC11-TRMT
* CB21-0	58	ALM 02-044	02-044	ALM	RCV DMC11MA	CPU0 DMC11-RCV
CB30-0	52	ALM 10-027	10-027	ALM	DR11C-TTY CONN. 2	CPU0 DR11C-TTY CONN. 2
CB31-0	52	ALM 06-027	06-027	ALM	DR11C-TTY CONN. 1	CPU0 DR11C-TTY CONN. 1
CB35-0	52	CONT 24-021	24-021	CONT	0DR11C-SA CONN. 2	CPU0 0DR11C-SA CONN. 2
CB36-0	52	CONT 20-021		NOTE 3	0DR11C-SA CONN. 1	CPU0 0DR11C-SA CONN. 1
CB37-0	52	CONT 24-027	24-027	CONT	1DR11C-SA CONN. 2	CPU0 1DR11C-SA CONN. 2
CB38-0	52	CONT 20-027		NOTE 4	1DR11C-SA CONN. 1	CPU0 1DR11C-SA CONN. 1
CB60-0	68	TTY 06-017	06-017	TTY	0DZ11B-TTY	CPU0 0DZ11B-TTY
CB61-0	68	TTY 06-049	06-049	TTY	1DZ11B-TTY	CPU0 1DZ11B-TTY
CB70-0	68	0ASYN 06-017	06-017	0ASYN	NOTE 1	CPU0 00DZ11B
CB71-0	68	0ASYN 06-049	06-049	0ASYN	NOTE 1	CPU0 01DZ11B
CB72-0	68	0ASYN 06-085	06-085	0ASYN	NOTE 1	CPU0 02DZ11B
CB73-0	68	0ASYN 06-117	06-117	0ASYN	NOTE 1	CPU0 03DZ11B
CB74-0	69	1ASYN 06-017	06-017	1ASYN	NOTE 2	CPU0 04DZ11B
CB75-0	69	1ASYN 06-049	06-049	1ASYN	NOTE 2	CPU0 05DZ11B
CB76-0	69	1ASYN 06-085	06-085	1ASYN	NOTE 2	CPU0 06DZ11B
CB77-0	69	1ASYN 06-117	06-117	1ASYN	NOTE 2	CPU0 07DZ11B
CB78-0	69	2ASYN 06-017	06-017	2ASYN	NOTE 2	CPU0 10DZ11B
CB79-0	69	2ASYN 06-049	06-049	2ASYN	NOTE 2	CPU0 11DZ11B
CB80-0	69	2ASYN 06-085	06-085	2ASYN	NOTE 2	CPU0 12DZ11B
CB81-0	69	2ASYN 06-117	06-117	2ASYN	NOTE 2	CPU0 13DZ11B

* COAXIAL Cable

NOTE 1: Transition panel in the J1P040K Cabinet.
NOTE 2: Transition panel in the J1P040L Cabinet.
NOTE 3: Route this cable end to the vicinity of the CONT unit location 20-021.
NOTE 4: Route this cable end to the vicinity of the CONT unit location 20-027.

TABLE 7

DESIG.	GROUP	STAMPED	CONNECTED FROM LOC.	CONNECTED FROM UNIT	ROUTE TO AREA OF	STAMPED
* CB20-1	59	ALM 02-124	02-124	ALM	TRMT DMC11MA	CPU1 DMC11-TRMT
* CB21-1	59	ALM 02-108	02-108	ALM	RCV DMC11MA	CPU1 DMC11-RCV
CB30-1	52	ALM 10-095	10-095	ALM	DR11C-TTY CONN. 2	CPU1 DR11C-TTY CONN. 2
CB31-1	52	ALM 06-095	06-095	ALM	DR11C-TTY CONN. 1	CPU1 DR11C-TTY CONN. 1
CB35-1	53	CONT 24-089	24-089	CONT	ODR11C-SA CONN. 2	CPU1 ODR11C-SA CONN. 2
CB36-1	53	CONT 20-089		NOTE 3	ODR11C-SA CONN. 1	CPU1 ODR11C-SA CONN. 1
CB37-1	53	CONT 24-095	24-095	CONT	IDR11C-SA CONN. 2	CPU1 IDR11C-SA
CB38-1	53	CONT 20-095		NOTE 4	IDR11C-SA CONN. 1	CPU1 IDR11C-SA
CB60-1	70	TTY 10-033	10-033	TTY	ODZ11B-TTY	CPU1 ODZ11B-TTY
CB61-1	70	TTY 10-065	10-065	TTY	IDZ11B-TTY	CPU1 IDZ11B-TTY
CB70-1	70	0ASYN 10-033	10-033	0ASYN	NOTE 1	CPU1 00DZ11B
CB71-1	70	0ASYN 10-065	10-065	0ASYN	NOTE 1	CPU1 01DZ11B
CB72-1	70	0ASYN 10-101	10-101	0ASYN	NOTE 1	CPU1 02DZ11B
CB73-1	70	0ASYN 10-133	10-133	0ASYN	NOTE 1	CPU1 03DZ11B
CB74-1	71	1ASYN 10-033	10-033	1ASYN	NOTE 2	CPU1 04DZ11B
CB75-1	71	1ASYN 10-065	10-065	1ASYN	NOTE 2	CPU1 05DZ11B
CB76-1	71	1ASYN 10-101	10-101	1ASYN	NOTE 2	CPU1 06DZ11B
CB77-1	71	1ASYN 10-133	10-133	1ASYN	NOTE 2	CPU1 07DZ11B
CB78-1	70	2ASYN 10-033	10-033	2ASYN	NOTE 2	CPU1 10DZ11B
CB79-1	70	2ASYN 10-065	10-065	2ASYN	NOTE 2	CPU1 11DZ11B
CB80-1	70	2ASYN 10-101	10-101	2ASYN	NOTE 2	CPU1 12DZ11B
CB81-1	70	2ASYN 10-133	10-133	2ASYN	NOTE 2	CPU1 13DZ11B

* COAXIAL Cable

NOTE 1: Transition panel in the J1P040K Cabinet.
NOTE 2: Transition panel in the J1P040L Cabinet.
NOTE 3: Route this cable end to the vicinity of the CONT unit location 20-089.
NOTE 4: Route this cable end to the vicinity of the CONT unit location 20-095.

Manager, Product Engineering
Control Center

Reason for Reissue:
To include UIS information.