PBX AIOD-A1
TROUBLE SHOOTING GUIDE

CONTENTS

1. GENERAL INFORMATION

1.1 This sub-section provides procedures to follow when detailed trouble shooting is required on the AIOD-A1 system.

1.2 This sub-section is designed to supplement TLM-1C005. The trouble shooting procedures outlined in TLM-1C005 should be followed prior to following the procedures outlined in this sub-section.

1.3 Refer to Section 275 for coordinating information.

1.4 The trouble shooting information is arranged in this sub-section in the approximate order required when performing tests per Section 275B.

2. GENERAL TROUBLE SHOOTING INFORMATION

2.1 Error Codes

2.11 Refer to Table A for a list of the abbreviations of incoming errors, names of errors, source of error signal, trap registration, printing format, and the 2-digit error code printed.

2.12 If multiple error codes are printed, error codes other than those listed in Table A, all but 1 error code must be inhibited to be able to trouble shoot problems one at a time.

2.121 One of the most common sources of multiple error codes is mutilation of Word 1 or Word 2, therefore perform the operations of paragraph 6, Section 275B to verify that the parity check words are not mutilated.

2.122 If the above procedure fails to eliminate all but one error code, the nand gates must be inhibited of SD-1C005 FS5 to allow only 1 error code to be printed. Inhibit the nand gates by placing a "high" on the NC (not connected) input.

2.2 Test Points

2.21 Circuit pack test points given in this sub-section list the last three digits of the SD first, the circuit pack connector location second, and the connector terminal number third, e.g., 002 05C01-13 would be terminal 13 of the circuit pack located in position 05C01 of SD-1C002.

2.22 The following explanation describes how to determine the circuit pack connector location from the wiring side of the frame. Each tray, horizontal group of connectors, is numbered in each J unit from frame bottom to frame top (numbering sequence: 01, 05, 09, 13, 17, 21); the vertical rows are divided into alternating groups of light gray and dark gray connectors, the first group is A, proceeding from right to left, and the last group is D; and each connector within a group is numbered from right to left (numbering sequence: 01, 04, 07, 10, 13, 16, 19, 22). Therefore, location 05C04 would be the 2nd tray in the unit (05), third group of gray connectors from the right (C), and the second connector from the right in the C group (04).

2.23 The following list provides a cross reference between SD and J drawings for the circuit pack trays.

SD-1C001	J1C000 E-1
SD-1C002	J1C000 C-1
SD-1C002	J1C000 D-1
SD-1C003	J1C000 B-1
SD-1C004	J1C000 F-1
SD-1C005	J1C000 L-1
SD-1C005	J1C000 M-1

2.3 Circuit Pack Replacement Procedure

The procedure to be followed is replacement of one circuit pack at a time. After each replacement a check should be made to see if the replacement cleared the trouble. If the trouble is not cleared, remove the replacement circuit pack, replace the original circuit pack, and proceed to the next replacement. When the trouble is cleared, leave the replacement circuit pack in the circuit and tag the original circuit pack.

2.4 Typical Error Codes

The following is a list of error codes frequently encountered, their probable cause and a suggested remedy.

Error Code	Probable Cause	Suggested Remedy
22,23	Problems in the connect process	Refer to paragraph 10.
24,25	Failure to connect correctly or no indentification data.	Refer to paragraph 10.
63,64 65,66	Mutilated Trunk Number or Station Number.	Refer to paragraph 9.
68	P2 bit in error	Unless otherwise specified per test, operate the P2 switch to its complimentary position and repeat the test.
83	Mutilated Word 1 or Word 2.	Perform tests per paragraph 6 Section 275B.
84	Failure to find Station Number	Refer to paragraph 11.
**	Multiple error codes	Refer to paragraph 2.1.

** Any two digits or symbols other than those listed in Table A.

TABLE A

ERRORS

Error Abbreviation	Name	Source of Error Signal	Trap	TSD	Seq	Code	Category Under 0 Option
PSF-RCVR0	Patch Selection Failure Receiver 0		X		1	22	MJ
PSF-RCVR1	Patch Selection Failure Receiver 1		X		1	23	MJ
RMT0	Receiver Message Time-Out 0 or 1		X		1	24	MJ
RMT1			X		1	25	MJ
RCTAL-RCVR0	Receiver Connect Time-Out Alarm - Receiver 0		X		1	26	MJ
RCTAL-RCVR1	Receiver Connect Time-Out Alarm - Receiver 1	Digit Register Connector (SD-1C004-01)	X		1	27	MJ
YDAL	Y Driver Alarm			X	2	28	MJ
XDAL	X Driver Alarm			X	2	29	MJ
DTAL-RDS0	Disconnect Time-Out Alarm Receiver 0				1	32	MN
CDAL	Core Driver Alarm			X	2	33	MJ
FDAL	Ferrod Detector Alarm				2	34	MN
DTAL-RDS1	Disconnect Time-Out Alarm Receiver 1				1	35	MN
TPF	Translator Parity Failure			X	1	62	MJ
F25TKA	Failure 2/5 Check Trunk No. Receiver A		X		2	63	MJ
F25STA	Failure 2/5 Check Station No. Receiver A				1	64	MN
F25TKB	Failure 2/5 Check Trunk No. Receiver B		X		1	65	MJ
F25STB	Failure 2/5 Check Station No. Receiver B				1	66	MN
OSCA	Oscillator A Failure				2	72	MN
OSCB	Oscillator B Failure				2	73	MN
EPHBA	Error - Phase Generator B				2	74	MN
EPHBB							
EPHAA	Error - Phase Generator A				2	75	MN
EPHAB							
TRARF	Translator Address Register Failure				1	76	MN
RATF	Office Index Relay Translator Failure	SIS Control			2	77	MN
CKPA	Check Parity Assembly	(SD-1C002-01)	X		1	82	MJ

TABLE A (Cont.d)

ERRORS

Error Abbreviation	Name	Source of Error Signal	Trap	TSD	Seq	Code	Category Under O Option
CKPC	Check Parity - Self Check				1	83	MN
CKPO	Check Parity - Central Office Request				1	84	MN
DRAST	Digit Register A Station Gating Failure				1	85	MN
DRATK	Digit Register A Trunk Gating Failure		X		1	86	MJ
DRBST	Digit Register B Station Gating Failure					87	MN
DRBTK	Digit Register B Trunk Gating Failure		X		1	88	MJ
DRARF	Data Register Address Register Failure		X		1	89	MJ
PWF	Power Failure	F, A&M (SD-1C006-01)			2	39	MJ
	Major Alarm Path Failure						MJ
TCPC	Test Circuit Parity Check	SI Test			2	68	MN
	Low Tape	(SD-1C005-01)					
STST	Test Circuit Self Test				1	69	MN
MUL	Multiple				2	70	MJ or MN

NOTE: With the NT switch in the TEST position all printouts will be sequence 2.

3. DIGIT REGISTER CONNECTOR INITIALIZATION

3.1 If -15V is not present on the terminals listed in paragraph 3.2 Section 275B, verify that all LV- and HG- relays are released.

3.2 The following list provides other voltages and their probable cause that may be encountered when performing paragraph 3.2 Section 275B.

VOLTAGE	PROBABLE CAUSE
0V	LV- or HG- relays locked operated
0V	COTA- and COTB- switch crosspoints latched operated.
24V	COTA- and COTB- switch crosspoints non-operated.

3.3 If the COTA- and the COTB- switches have not been forced into an idle state, COTA- switch crosspoints latched operated and COTB- switch crosspoints non-operated, a 34 error code (FDAL) will be printed when the printer is placed in service.

4. NORMAL STATUS

If any relay(s) per paragraph 4 Section 275B, normally released, are locked operated one of the following operations will normally release the relay(s).

4.1 Momentarily disengage CP75 at location 005 21D16.

4.2 Momentarily disengage CP96 at location 004 05D19.

4.3 Momentarily operate relay DIS0 or DIS1.

5. CENTRAL REGISTER CONTROL

Paragraph 5 Section 275B checks that each flip flop of the Central Register (FS6 SD-1C005) can be set and cleared via the Control Panel. Each CR- TSR (Toggle Shift Register) is set by its associated Control Panel switch via the SW- lead. For a detailed description refer to CD-1C005 paragraph 2.15.

6. PARITY CHECK WORDS

Refer to paragraph 8 of this section for trouble shooting information. A detailed description of the use of Word 1 and Word 2 is provided in CD-1C002 paragraph 3.01 and paragraph 5.

7. ERROR MONITORING (STST)

7.1 Trouble Shooting Setup

7.11 To verify that information can be shifted through the Central Register, rotate the fastener (located below the Printer) 1/4 turn clockwise and slide the Printed forward. Load a bit in the P2 position, NT switch NORMAL, and momentarily operate switch STST. The bit is shifted through the Central Register one stage at a time.

7.12 To verify or check for the control pulses the oscilloscope should be used in a Triggered Delay Sweep Mode. Refer to the Instruction Manual provided with the oscilloscope for steps required to use the Triggered Delay Sweep.

7.2 Description

7.21 Block Diagram 1 (BD1) provides a simplied version of the Error Monitoring functions.

7.22 For detailed information refer to CD-1C005 paragraph 4.23 and BD2 in SD-1C005. The timing sequence is provided in SD-1C005 SC1, SC2 and SC5.

8. INPUT/OUTPUT

8.1 Trouble Shooting Setup

8.11 The following setup performs repeated WO cycles to enable easier trouble shooting.

a) Load the desired Trunk Number, Station Number, Switch, Level and the appropriate parity bits into the Central Register using the Control Panel.
b) Insert the ITE-5182 extender board into location 005 01D13 and open pin 11.
c) Connect a 737A Tool from 005 09D04-18 to 005 09D04-3.

8.12 The following setup performs reforms repeated RO cycles. After the first RO cycle the location being addressed will contain all "0's".

a) Load the desired Trunk Number into the Central Register using the Control Panel.
b) Insert the ITE-5182 extender board into location 005 09D07 and open pin 23.
c) Connect a 737A Tool from 005 09D04-25 to 005 09D04-27.

8.13 The following setup performs repeated RW cycles. To load information into a specific address perform a WO cycle first.

a) Load the desired Trunk Number into the Central Register using the Control Panel.
b) Insert the ITE-5182 extender board into location 005 09D07 and open pin 11.
c) Connect a 737A Tool from 005 09D04-20 to 005 09D04-27.

8.2 Description

8.21 Block Diagram 2 (BD2) provides a simplified version of the handling of the Trunk Number and Station Number during a WO cycle. Refer to the following CD's for a detailed description of a WO cycle:

CD	Paragraph
1C005	2
1C003	1., 2., 3., 4., 5., 6., and 7.

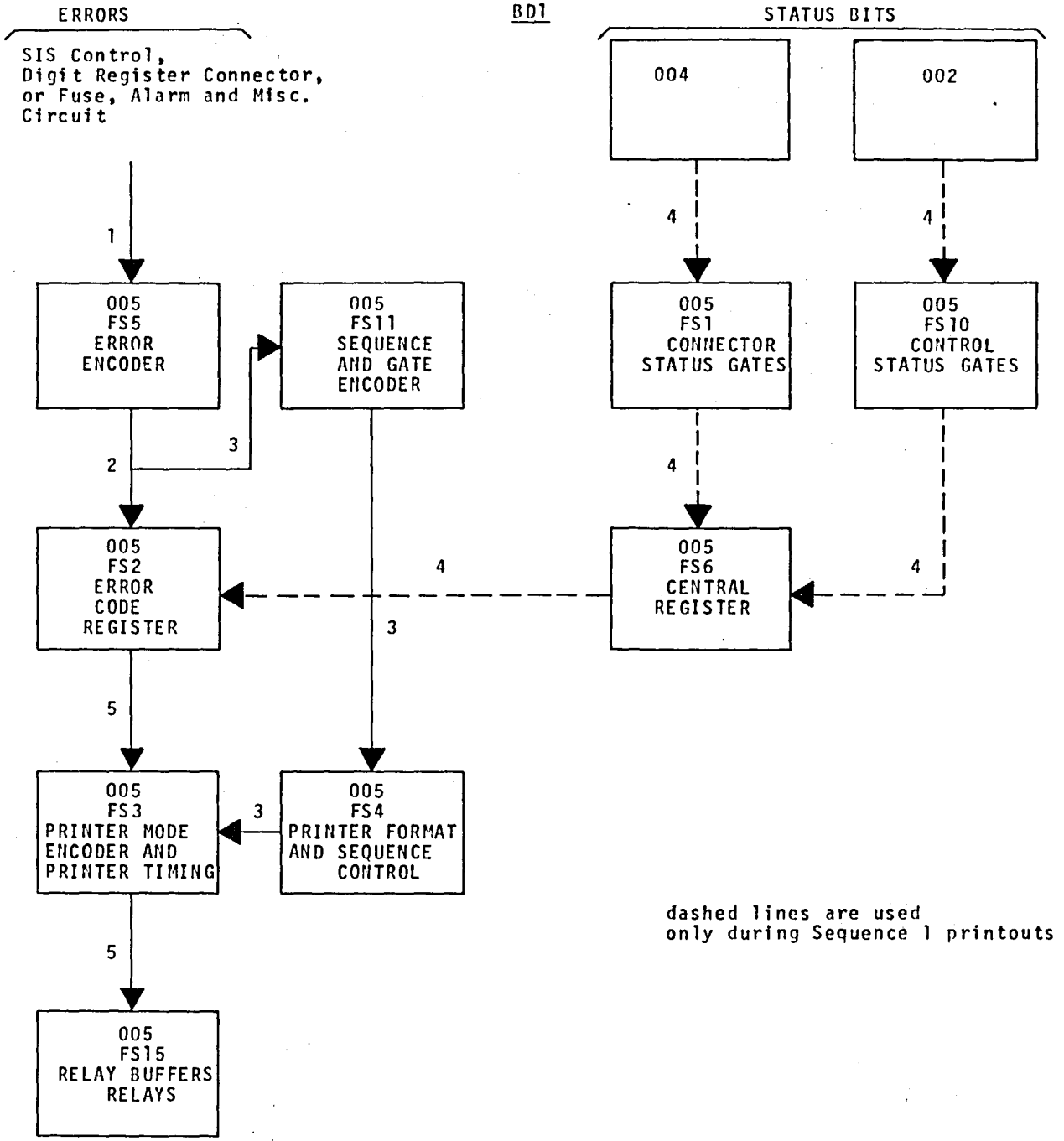
8.22 Block Diagram 3 (BD3) provides a simplified version of the handling of the Trunk Number and Station Number during a RO cycle. Refer to the following CD's for a detailed description of a RO cycle:

CD	Paragraph
1C005	2.
1C003	1., 2., 3., 4., 5., 6., and 8.

8.23 Because of the similarity between a RO cycle and a RW cycle both cycles are shown on one block diagram (BD3). Refer to the following CD's for a detailed description of a RW cycle.

CD	Paragraph
1C005	2.
1C003	1., 2., 3., 4., 5., 6., 7. and 8.

BD1

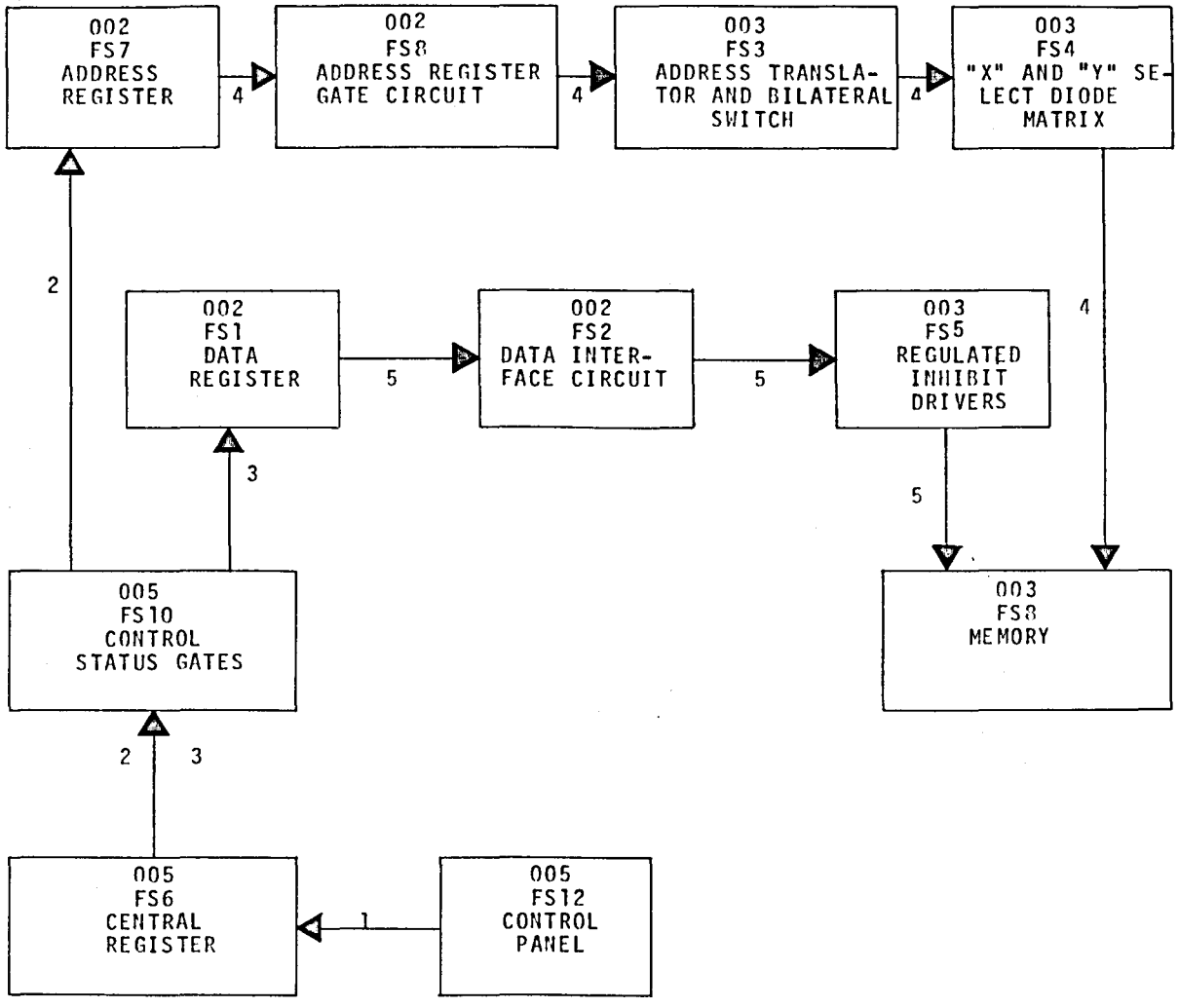


ERROR MONITORING - SIMPLIFIED

Brief Description:

1) Error signal received from 002, 004, or 006 circuit.
2) The error code is stored as a two digit binary number.
3) Appropriate Sequence is determined, Sequence 1 or Sequence 2.
4) On a Sequence 1 printout the Status Bits are loaded into the Central Register and the Central Register is connected to the Error Code Register.
5) The contents of the Error Code Register (and Central Register) are used to control the printout.

BD2

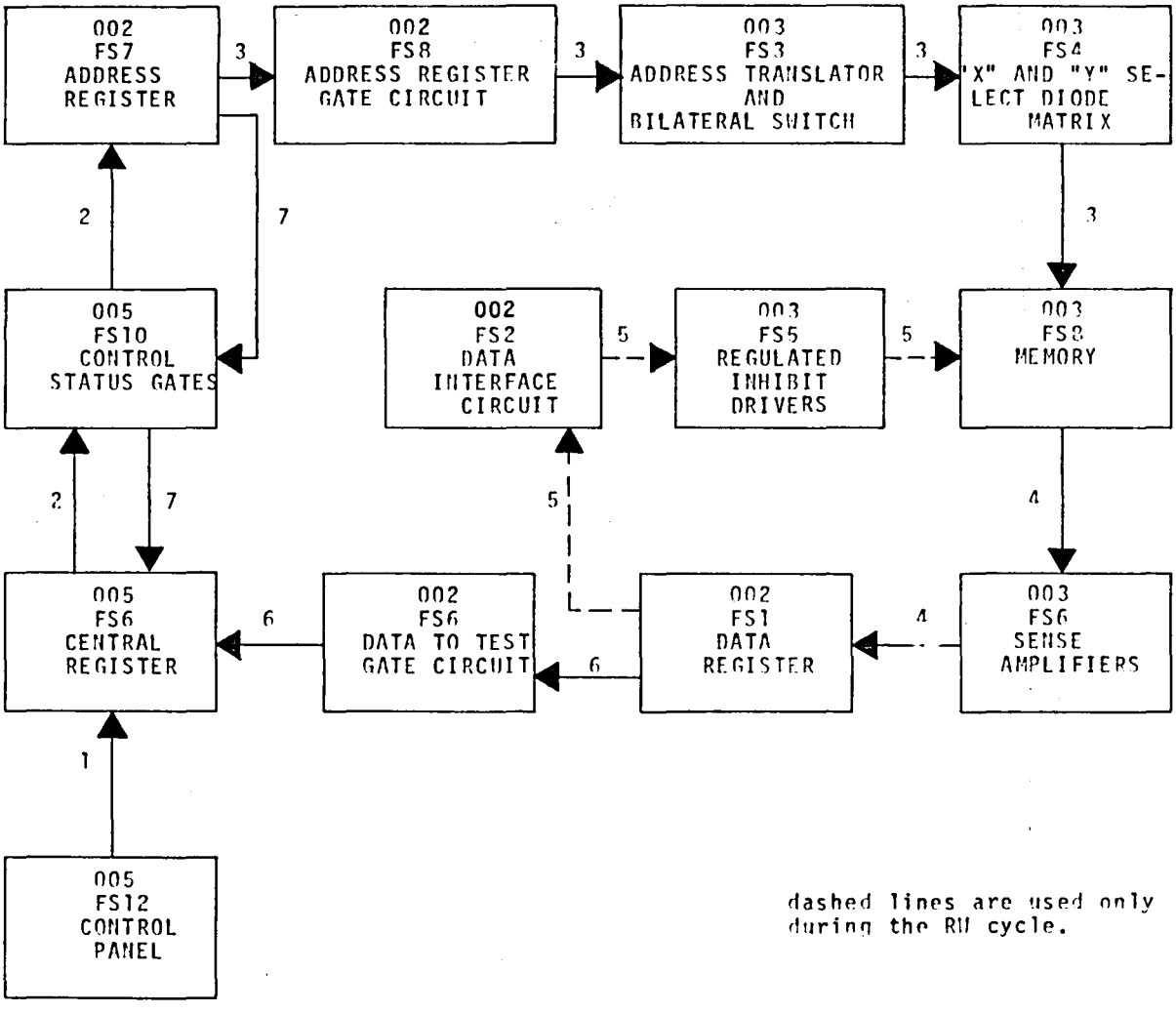


WO CYCLE - SIMPLIFIED

Brief Description

1) The Control Panel is used to load information into the Central Register.
2) The Trunk Number is transferred from the Central Register to the Address Register.
3) The Station Number is transferred from the Central Register to the Data Register.
4) The Trunk Number is used to select the desired Memory location.
5) The Station Number is written into the Memory location previously selected.

BD3



RO CYCLE AND RW CYCLE - SIMPLIFIED

Brief Description

1) The Control is used to load the Trunk Number into the Central Register.
2) The Trunk Number is transferred from the Central Register to the Address Register.
3) The Trunk Number is used to select the desired Memory location.
4) The contents of the Memory location addressed are read out and transferred to the Data Register.
5) On a RW cycle only the contents of the Data Register is written into Memory.
6) The contents of the Data Register is transferred to the Central Register.
7) The contents of the Address Register is transferred to the Central Register.

8.3 Waveforms

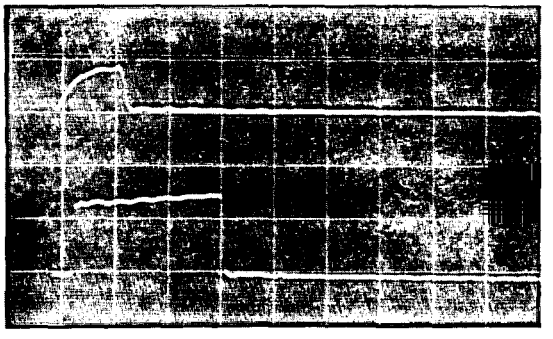
The following waveforms are examples encountered during Normal frame operation. Trunk Number 0177 and Station Number 1111 were employed. The test points given reflect this Trunk Number and Station Number. If a different Trunk Number and Station Number are employed some of the test points will change.

COMMAND PULSE

The waveform shown was obtained performing a RW cycle per paragraph 8.13. For RO cycle use 003 05C01-11 as SYC and for the A chan. For WO cycle use 003 05C04-5 as SYC, the B chan waveform is not obtainable using the WO cycle.

SYC: 003 05C01-7
A chan: 003 05C01-7(RW)
B chan: 003 05D13-13(RXD)

5V/cm
1usec/cm



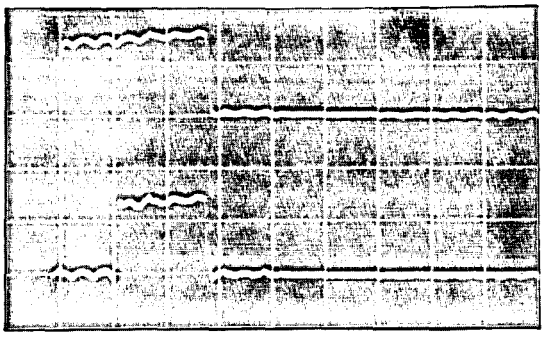
WF1

READ PULSES

The Read pulses are obtainable only for RW and RO cycles. Change SYC for RO cycle to 003 05C01-11.

SYC: 003 05C01-7(RW)
A chan: 003 05D13(RXD)
B chan: 003 01D10-13(RYD)

5V/cm
1usec/cm



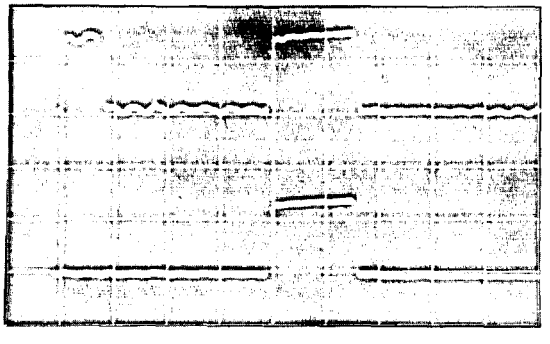
WF2

WRITE PULSES

The Write pulses are obtainable only for RW and WO cycles. When using WO as SYC, the waveforms will be that shown on the right half of the graticule.

SYC: 003 05C01-7(RW)
A chan: 003 01D16-13(WYD)
B chan: 003 05D19-13(WXD)

5V/cm
1usec/cm



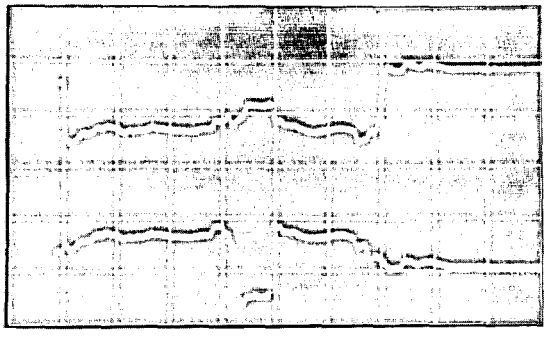
WF3

ADDRESS TRANSLATOR AND BILATERAL SWITCH (Switch Activated)

One AX, one BX, one AY and one BY Translator switch are activated to address one specific store location.

SYC: 003 05C01-7(RW)
A chan: 003 01D04-22(1RAX)
B chan: 003 01D04-24(1WAX)

20V/cm
1usec/cm



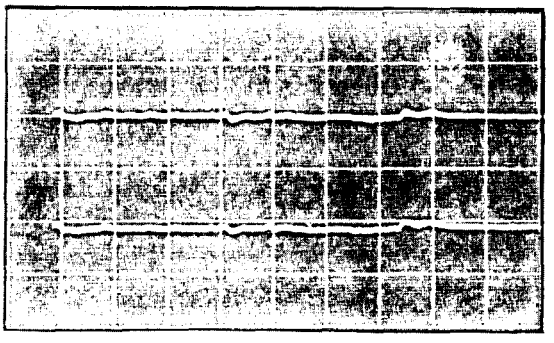
WF4

ADDRESS TRANSLATOR AND BILATERAL SWITCH (Switch Idle)

Output of all Translator switches not in use will be as shown.

SYC: 003 05C01-7(RW)
A chan: 003 01D04-6(ORAX)
B chan: 003 01D04-8(OWAX)

20V/cm
1usec/cm



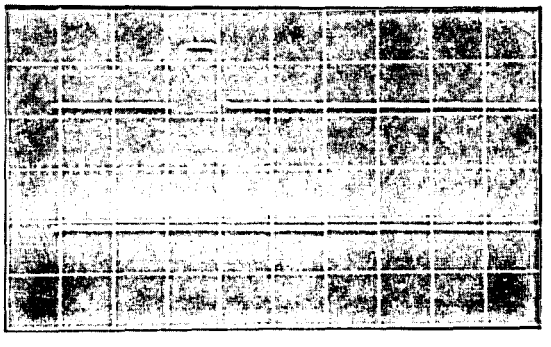
WF5

SENSE AMPLIFIER

Channel A shows a "1" being read out of Memory. Channel B shows an "0" being read out of Memory.

SYC: 003 05C01-7(RW)
A chan: 003 13A10-21
B chan: 003 13A07-21

10V/cm
1usec/cm



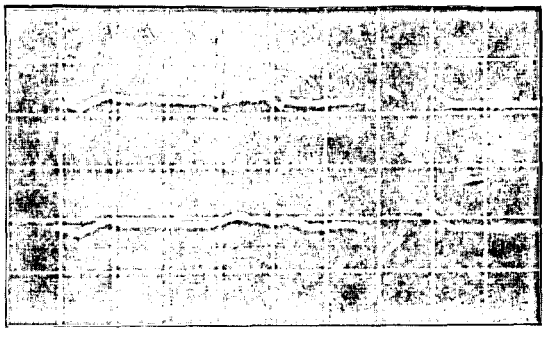
WF6

REGULATED INHIBIT DRIVERS (1 Written)

Chan A and Chan B show the output of the Inhibit Driver when a "1" is written into Memory.

SYC: 003 05C01-7(RW)
A chan: 003 09C05-19
B chan: 003 09C05-23

10V/cm
1usec/cm



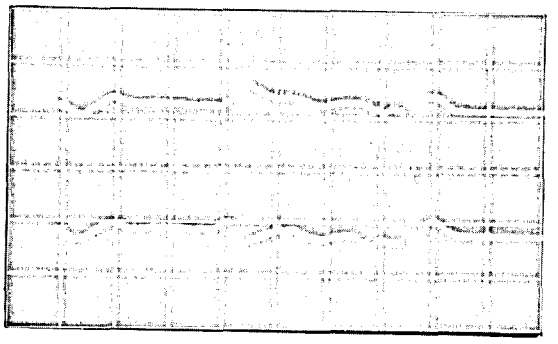
WF7

REGULATED INHIBIT DRIVERS (0 Written)

Chan A and Chan B show the output of the Inhibit Driver when an "0" is written into Memory.

SYC: 003 05C01-7(RW)
A chan: 003 09C05-21
B chan: 003 09C05-25

10V/cm
1usec/cm



WF8

9. ASSEMBLY

9.1 Trouble Shooting Setup

9.11 When trouble is encountered during Assembly, the Control Panel should be setup to perform a TDR Request. This procedure bypasses the Digit Register Connector, thus avoiding any troubles in the DRC. This procedure also increases the repetition rate of PBX Requests thus providing a steady scope display.

9.12 The oscilloscope must be operated utilizing the Triggered Delay Sweep Mode to verify the presence of all Control pulses. Refer to the Instruction Manual provided with the scope for steps required to use Triggered Delay Sweep.

9.13 When using the 545B oscilloscope in the Triggered Delay Sweep mode, set the A Time Base to 5usec/cm and the B Time Base to 10msec/cm. Connect the A channel to the ODD f-f and use the B channel to check for Control pulses.

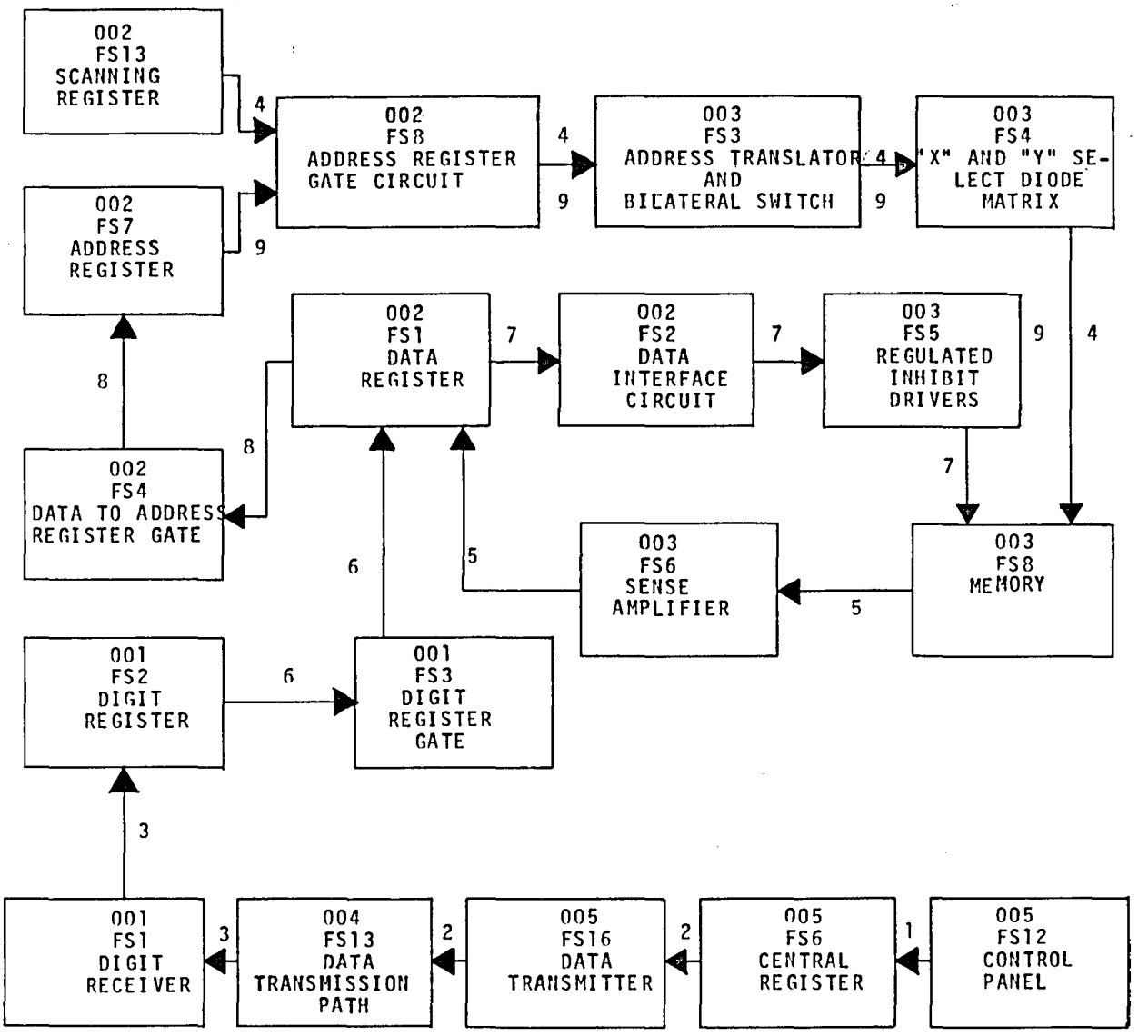
9.2 Description

9.21 Block Diagram 4(BD4) provides a simplified version of the steps performed during Assembly. The process described is using a TDR Request.

9.22 For a detailed description of Assembly refer to the following CD's:

CD	Paragraph
1C001	All
1C002	4.03 thru 4.08 & 11.
1C005	3.

BD4



ASSEMBLY - SIMPLIFIED

Brief Description - ASSEMBLY

1) The Control Panel is used to load data into the Central Register.

2) The data is shifted out of the Central Register and converted to Frequency Shift Keying signals.

3) The Frequency Shift keying signals are converted back to their logical pulses and stored 1 digit at a time in the Digit Register.

4) A Temporary store location is interrogated.

5) Contents of the temporary location written into the Data Register.

6) 1 digit at a time the data is transferred from the Digit Register to the Data Register.

7) Contents of the Data Register written into Temporary store location.

NOTE: Steps 4, 5, 6 and 7 are repeated for each digit, omit step 7 on last digit.

8) Trunk Number is transferred from the Data Register to the Address Register.

9) Trunk Number is used to select the desired Memory location.

10) Contents of Data Register are written into Memory.

9.3 Waveforms

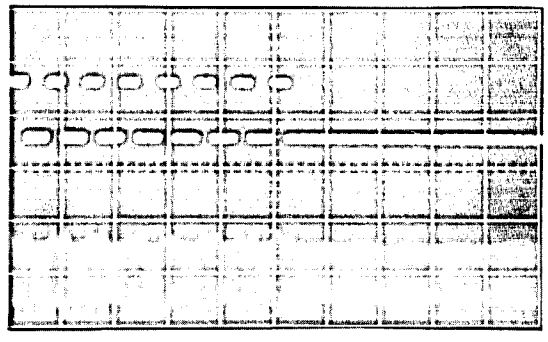
The following waveforms are examples encountered during a TDR Request. These waveforms and the procedure described depict normal operation of the AIOD-A1 frame.

2 OUT OF 5 CODED DATA

WF9
depicts Trunk Number 1111 and Station Number 1111 as it is transmitted by the Test Circuit. The B chan trace depicts the 1150 HZ and 1850 HZ signal. As can be seen it is difficult to discern an error.

SYC: 005 17D16-14
A chan: 005 17D16-14
B chan: 001 01C16-7

A chan: 5v/cm, 10ms/cm
B chan:.2v/cm, 10ms/cm



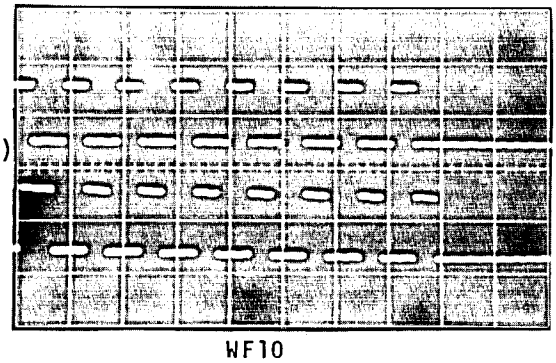
WF9

2 OUT OF 5 CODED DATA

Each digit in WF10 occupies one centimeter, total 8 digits. The time difference between the A chan trace and the B chan trace is the time between transmission and reception of the 2/5 coded Data.

SYC: 005 17D16-14
A chan: 005 17D16-14
B chan: 001 01C13-2

5v/cm
5msec/cm (uncalibrated)



WF10

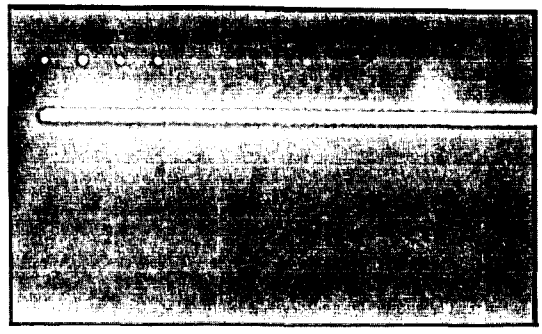
ODD Flip-Flop

Setup Scope for Triggered Delay Sweep. During the Assembly the ODD f-f sets once for each digit of the Trunk Number and Station Number. As the Delay-Time Multiple is varied the brightened segment will jump from one pulse to the next. The second pulse is the brightened segment in WF11.

SYC: 002 17B13-9
A chan: 002 17B13-9

5v/cm
10msec/cm

HORIZONTAL DISPLAY:
"B" INTENSIFIED BY "A"



WF11

ODD Flip-Flop (TN)

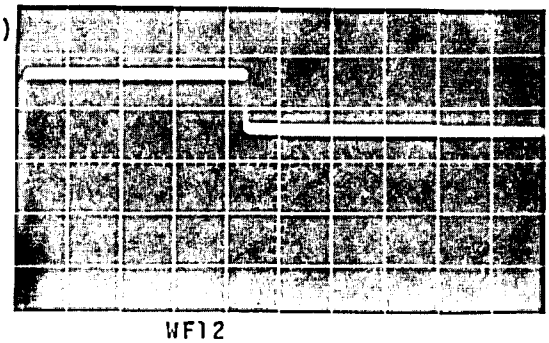
Scope Setup for Triggered Delay Sweep

WF12 shows the ODD f-f output during reception of a Trunk Number digit. The first four pulses of WF11 are Trunk Number pulses and will appear as that shown when they are expanded.

SYC: 002 17B13-9
A chan: 002 17B13-9

HORIZONTAL DISPLAY:
"A" DLY'D BY "B"

5v/cm 5usec/cm



WF12

ODD Flip-Flop (SN)

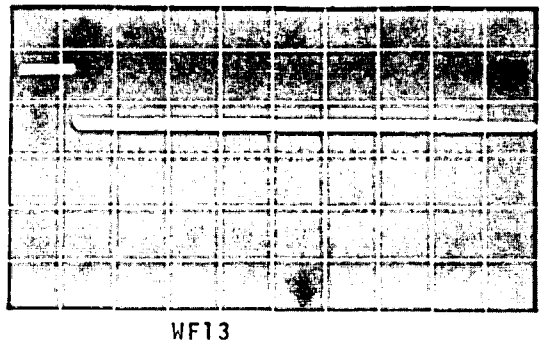
Scope Setup for Triggered Delay Sweep

WF13 shows the ODD f-f output for Assembly of the Station Number digits The last four pulses of WF11 are Station Number pulses and will appear as that shown when expanded.

SYC: 002 17B13-9
A chan: 002 17B13-9

HORIZONTAL DISPLAY:
"A" DLY'D BY "B"

5v/cm 5usec/cm



WF13

The following waveforms are examples of the control pulses used during Assembly, refer to Table B for a list of Test Points for all the control pulses per SC's of SD-1C002. All of the following waveforms were obtained using the Triggered Delay Sweep. If the Triggered Delay Sweep is not used the SYC point will always be the first Trunk Number pulse.

Reset ODD Flip-Flop

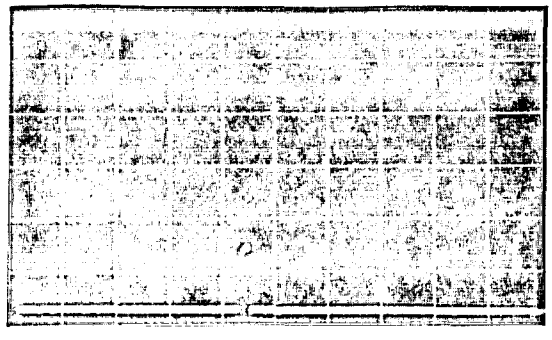
WF14 depicts the time and duration of the pulse used to reset the ODD flip-flop during reception of a Trunk Number digit.

SYC: 002 17B13-9
A chan: 002 17B13-9

B chan: 002 17B04-11

HORIZONTAL DISPLAY:
"A" DLY'D BY "B"

5v/cm 5usec/cm



WF14

OERIN

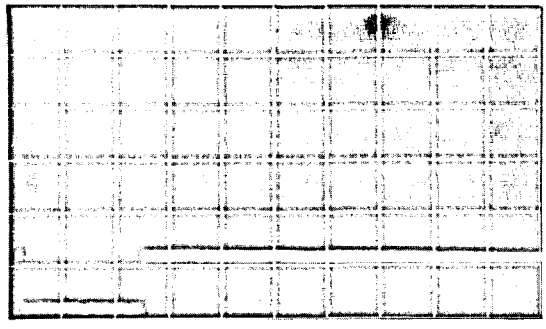
WF 15 depicts the time and duration of the OERIN pulse during reception of a Trunk Number digit.

SYC: 002 17B13-9

B chan: 002 13B16-9

HORIZONTAL DISPLAY: "A" DLY'D BY "B"

5v/cm 5usec/cm



WF 15

RO

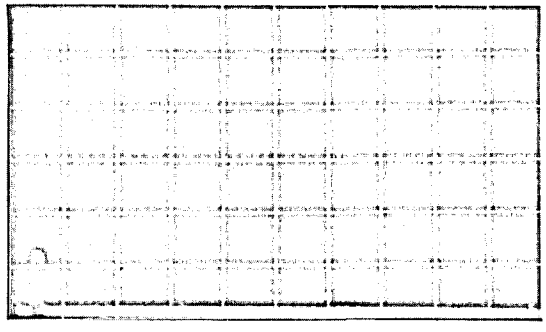
WF 16 depicts the time and duration of the RO pulse during reception of a Trunk Number digit.

SYC: 002 17B13-9

B chan: 002 13B16-9

HORIZONTAL DISPLAY: "A" DLY'D BY "B"

5v/cm 5usec/cm



WF 16

Reset TR Flip-Flop

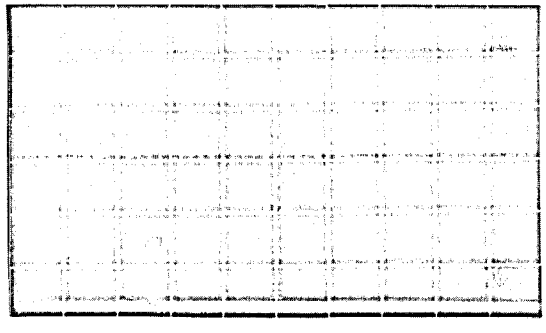
WF 17 depicts the time and duration of the pulse used to reset the TR flip-flop during reception of the 4th Station Number digit.

SYC: 002 17B13-9

B chan: 002 13A07-25

HORIZONTAL DISPLAY: "A" DLY'D BY "B"

5v/cm 5usec/cm



WF 17

TKCF

A pulse will appear as shown in WF 18 if there is an error in the Trunk Number digit.

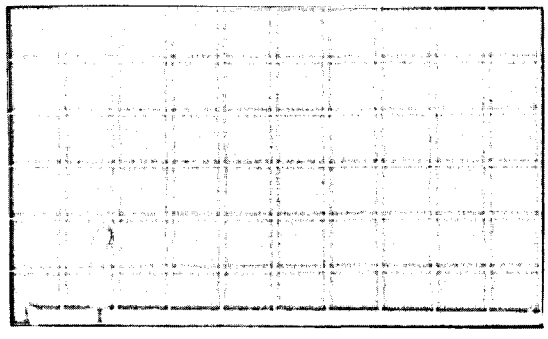
NOTE: A error in one Trunk Number digit will cause an output on succeeding Trunk Number digits. Therefore, when trouble shooting SYC on the first digit that has an output at the given test point.

SYC: 002 17B13-9

B chan: 002 17C13-11

HORIZONTAL DISPLAY "A" DLY'D BY "B"

5v/cm 5usec/cm



WF 18

9.4 Test Points

The following Table provides the test points for the pulse designations given in the SC 15 of SD-1C002

TABLE B

Lead Desig	Test Point
Check 2/5 (Error)	17C07-20 (A Reg) 17C07-22 (B Reg)
CKPA CKPO CO EVEN FF Gata Data T.N.	17B22-25 13A13-05 13C16-25 17B10-19
GCHK GTDA ODD FF OERIN Reset Data Reg	13A19-19 13B22-28 17B13-09 13B16-09 13A04-09
Reset ODD FF RO RSFF RSGN RSPA	17B04-11 13D04-17 17B10-09 17B10-10 13A07-07
RSTAR SCA1, 3N SCA2,4	13A04-04 (1) 17A04-09(A Reg) (3) 17A04-04(B Reg) (2) 17A04-28(A Reg) (4) 17A04-17(B Reg)
SHFDA TRF TR FF UDPA UDPB	13C07-16 17C04-14 13A04-28 13A16-19 13A16-23
UDPMB UPPMA WO W1C W2C FF	01C13-26 17C22-14 13D04-28 13B16-4 17B13-19
W2 CON W2RN	13B16-28 13B19-28

10. DIGIT REGISTER CONNECTOR

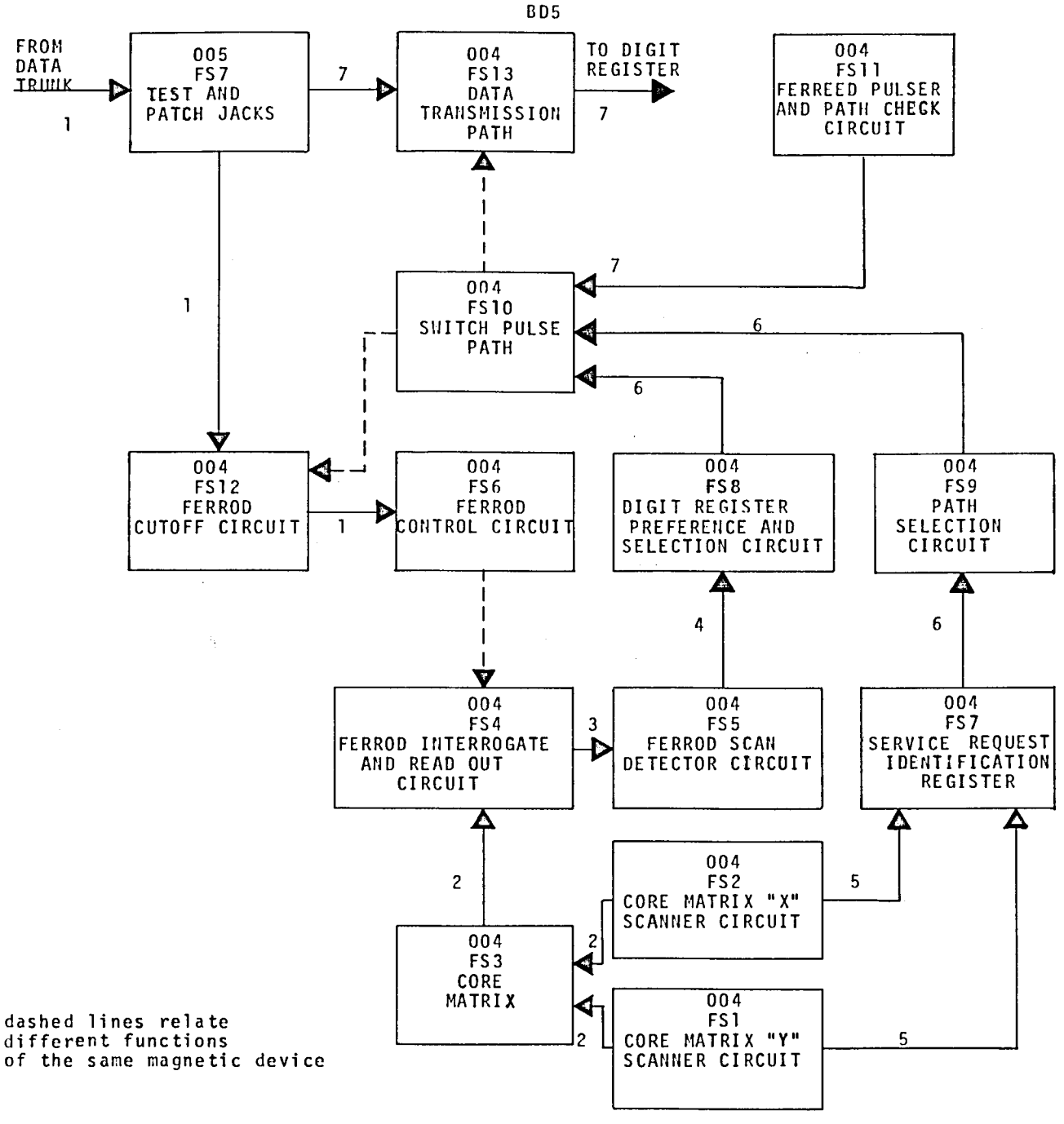
10.1 Trouble Shooting Setup

To be able to limit the errors generated to the Digit Register Connector it is essential that a TDR Request can be completed successfully utilizing both Digit Registers. This procedures verifies that all other circuits used for a PBX Request function correctly and are not generating errors. To trouble shoot the Digit Register Connector perform a TRAC Request, use any valid 2/5 coded Trunk Number and any valid 2/5 coded Station Number.

10.2 Description

10.21 Block Diagram 5 (BD5) provides a simplified version of the functions necessary to establish a connection form a Data Trunk to a Digit Register. For a detailed description refer to CD-1C004 paragraphs 1. and 2..

10.22 Block Diagram 6 (BD6) provides a simplified version of the functions necessary to disconnect a Data Trunk from a Digit Register. For a detailed description refer to CD-1C004 paragraph 3.

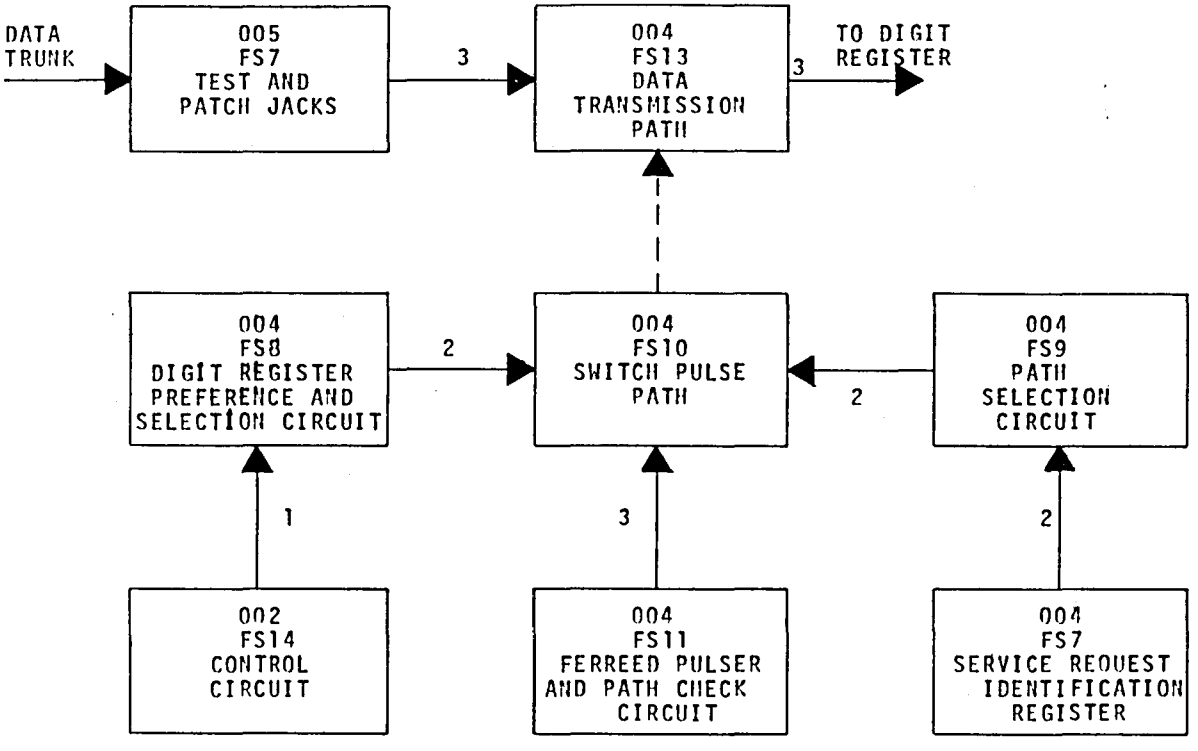


ESTABLISHING CONNECTION - SIMPLIFIED (Paragraph 10.2)

Brief Description

1) Service Request, the -48V simplexed battery is changed to simplex grd, thus de-energizing the ferrod control winding.
2) A pulse is produced on the ferrod read-out winding.
3) The pulse is detected as a Service Request.
4) An idle Digit Register is selected.
5) Identity of the Data Trunk is stored.
6) A unique path is selected via contacts of relays LV-, HG- and RC-.
7) A pulse is applied closing the ferrod switch crosspoints, this connects the Data Trunk to a Digit Register.

BD6



dashed lines relate different functions of the same magnetic device.

DISCONNECT - SIMPLIFIED

Brief Description

1) Signal that Assembly has been completed.

2) A unique path is selected via contacts of relays LV-, HG-, and DIS-.

3) A pulse is applied severing the connection between the Data Trunk and the Digit Register.

10.3 Waveforms and Other Info

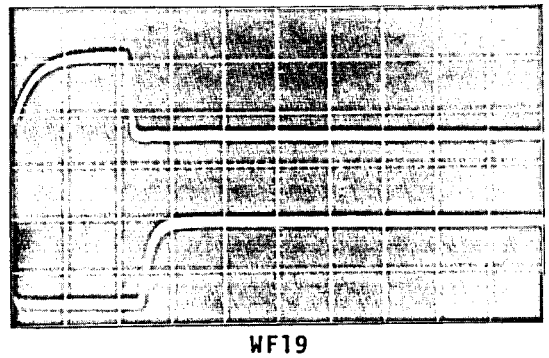
The following waveforms provide points which can be checked to verify proper operations. Because of the design of the 004 Circuit portions of the circuit are somewhat susceptable to noise and relay problems. The tension on all relays is extremely important with the RR-relay tension being most trouble some.

Ground pin 01B13-28 004 to observe waveforms;WF19,WF20 and WF21.
The associated waveform shows pulses generated when a Service Request is detected.

Service Request

SYC 004 05D22-16
A chan: 004 05D22-16
B chan: 004 05D22-28

5v/cm
1usec/cm



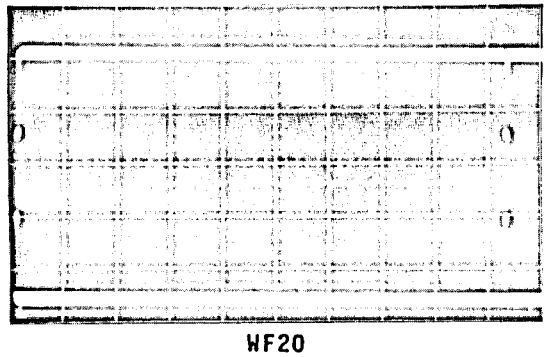
WF19

Service Request

The associated waveform shows the spacing between pulses when a Service Request is detected.

SYC 004 05D22-16
A chan: 004 05D22-16
B chan: 004 05D22-28

5v/cm
.1msec/cm



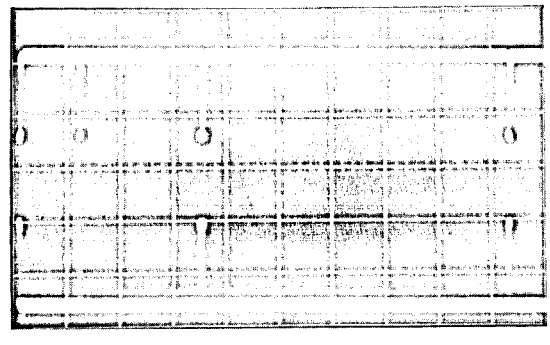
WF20

False Service Requests

The associated waveform shows false Service Requests. These false Service Requests may be steady or may be intermittant and will generate 24 or 25 error codes. The cause may be a weak R20 board or the C.P. listed in TLM-1C005, low -48V supply voltage or misadjusted relay.

SYC 004 25D22-16
A chan: 004 25D22-16
B chan: 004 25D22-28

5v/cm
.1msec/cm



WF21

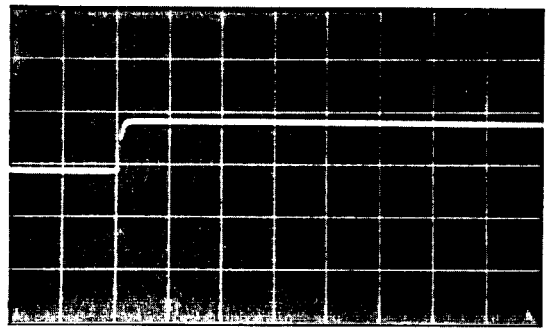
Pulser

The pulser is used to open and close the ferrod cross-points. The associated waveform can be used to verify pulser operation.

A defective pulser will cause relays such as LV-, HG-, RC-, RR- and DIS- to lock operated and an error code to be printed.

SYC 004 09D04-2
A chan 004 09D04-2

5v/cm
20usec/cm



WF22

10.4 Digit Register Connector Relays

10.41 The spring tension and the associated relay circuitry in the Digit Register connector is critical for proper operation. Improper relay operation can cause various error codes and may cause other relays to lock operated.

10.42 The following procedure can be used to check relay tension and associated circuitry.

A) Insert a dummy plug in one RMB- jack.
B) Perform a TRAC Request.
C) With the relays pulsing check to determine if an increase or decrease in relay tension causes a decrease in the error codes printed. The RR- relays should be checked first. If a decrease is observed check the associated relay circuitry and relay tension.

11. LOOP TESTS AND SYSTEM TEST

11.1 Short Loop Test

Failures when performing Short Loop Tests are generally caused by crosses in the switchboard cabling between the AIOD frame and the AIOD Translator and between the AIOD Translator and the Central Office equipment. For a description refer to CD-1C002 paragraph 12.47.

11.2 Long Loop Tests

11.21 Block Diagram 7 (BD7) provides a simplified version of the handling of information by the AIOD-A1 frame during a C.O. Request (or Long Loop Test). For a detailed description refer to CD-1C002 paragraphs 11.13 and 12.48.

11.22 The following are the problems most commonly encountered when performing a Long Loop Test.

A) An 84 error code will be printed if a PBX Request or WO cycle was not performed prior to initiating the Long Loop Test or if the AIOD-A1 cross connections are wrong (Refer to paragraph 3.23, Section 275A).

B) No error code will be printed if the AIOD frame is in the TRAP or TSD state or for most Translator failures, but the test will fail.

11.3 System Test

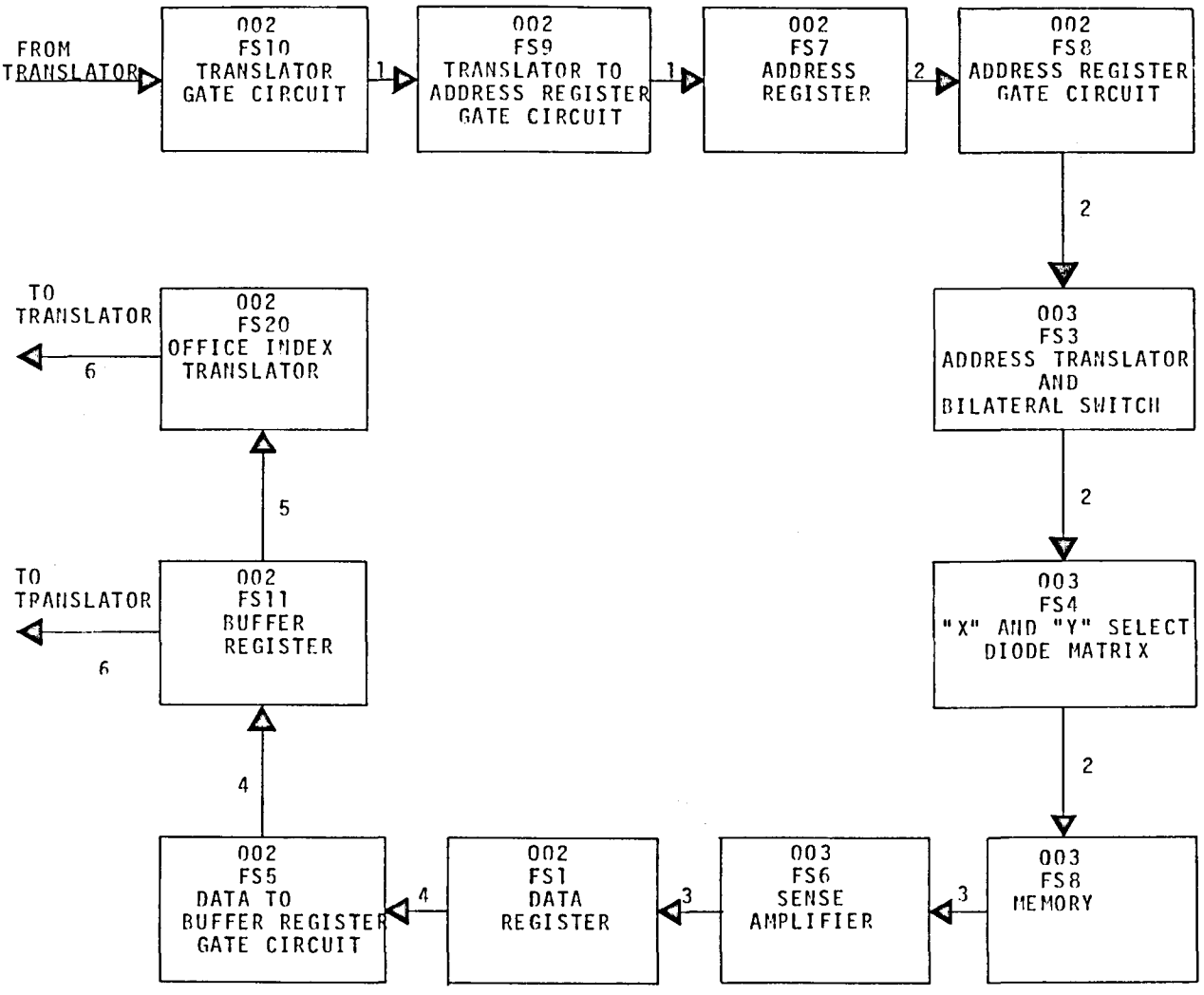
11.31 System test refers to the initiation of a call from the PBX-ANI and allowing the Central Office billing equipment to request the billing information from the AIOD frame.

NOTE: This test is to be performed only at the Request of the local operating company,

11.32 An intermediate step between Long Loop Tests and System Test is to initiate a request from the PBX-ANI and, using the Trunk Number supplied by the PBX-ANI Test Set, then perform a RO or RW cycle and verify that the Station Number and Switch and Level have been stored correctly.

11.33 Even though Long Loop Tests and the tests of paragraph 11.32 can be performed, an 84 error code will be printed when system testing if the Trunk Number assignments at the PBX-ANI and at the C.O. differ.

BD7



CENTRAL OFFICE REQUEST - SIMPLIFIED

Brief Description

1) The Trunk Number is sent from the AIOD Translator and loaded into the Address Register.

2) The Trunk Number is used to address the desired Memory location.

3) The contents of the Memory location addressed are written into the Data Register.

4) The Station Number, Switch and Level are transfered from the Data Register to the Buffer Register.

5) The Switch and Level is converted to a 1 out of 30 Office Index Code.

6) The Station Number and Office Index are sent to the AIOD Translator.

11.34 With the AIOD-A1 frame in the TRAP or TSD state most System Tests will fail. Refer to Section 275A paragraphs 6.2 and 6.3 for an explanation of TRAP and TSD.

11.35 On a System Test, provided that Section 275B can be performed successfully, error codes whose source of error signal is SD-1C004 or 63, 64, 65 and 66 error codes are generally caused by PBX-ANI failure.

Manager, Engineering, Switching Equipment, Reproduction and Step-by-Step P.E.C.C.