

33-TYPE DATA UNIT DESCRIPTION

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1. GENERAL

1.01 This section contains a description of the 33A1 Data Unit (DU) and information pertinent to its operation. Information concerning equipment associated with the data unit is not included but is described in Sections 593-801-100, -200, and -500.

1.02 The 33A1 Data Unit serves as the basic transceiver component of Data Set 306A-type. When used in the data set, the data unit interfaces with a customer's business machine and provides full-duplex synchronous data transmission. The customer's digital data signal of 1.344 megabits per second (Mbps) is converted to the standard bipolar signal of 1.544 Mbps, thus making it compatible with present 4-wire T1 facilities. The high-speed data circuitry of the transceiver is designed to operate with bipolar signals on the line side for direct connection to a T1 line terminating unit (LTU). The data unit is intended for limited distance private line service and possesses features consistent with some switched service applications.

1.03 The data unit utilizes two types of customer interface signals. One type is the high-speed clock and data signals which are balanced dc-coupled and meet the international standard CCITT Recommendation V35 Appendix 4. The other type is the unbalanced voltage-type control signals which meet EIA Standard RS-232-C format. The control signals indicate the status of the station and of the customer's equipment.

1.04 The data unit is designed to be operational with or without the customer controls interface circuit pack AR504. The polarity of the control signals is such that the removal of circuit pack (CP) AR504 allows the data unit to be operational. Physical removal of the circuit pack may aid in determining if the correct option(s) are installed and/or if correct control signals are being received from the business machine. For example, assume the data unit is inoperative. After removal of CP AR504, the data unit is operational. First, verify that options are properly installed, and if

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they are, then the control signals are incorrect and may be caused by the business machine or the customer-provided cable between the business machine and data unit.

1.05 If incomplete information or data is contained in this BSP, initiate BSP Comment Form E-3973.

2. PHYSICAL DESCRIPTION

2.01 Figure 1 shows the front view of the 33A1 Data Unit which is of modular construction and contains nine AR-type circuit packs.

2.02 The unit is designed to mount with four self-tapping screws onto a 6-inch mounting plate, or equivalent, with appropriate cutout. When completely wired and assembled, the data unit weighs approximately 10 pounds and 10 ounces.

2.03 Figure 2 shows the rear view of the 33A1 Data Unit. Assembled at the rear of the apparatus unit are a customer interface connector, a 944A equalizer, and two terminal boards (TB). Customer connector J10 is a 34-pin female connector.

The equalizer compensates for the cabling to the T1 line terminating unit. TB1 has a field of 45 screw terminals which are used for interconnections with other apparatus and for option strapping. Options wired in the data unit should be recorded on a label and then placed on the coverplate or in the wideband data station cabinet. TB2 has a field of 34 terminals which provide test points corresponding to the interface leads. Not shown is a coverplate used to protect wiring and prevent accidental short circuits.

2.04 The 33A1 Data Unit power requirements are given in Table A and the working limits are given in Table B.

3. FUNCTIONAL DESCRIPTION

GENERAL

3.01 Figure 3 shows a simplified block diagram of the 33A1 Data Unit with timing signals. The 1.544-MHz reference waveform is shown to indicate the pulse duration (width) as compared to the other waveforms. The balanced data signals, waveform 1, show only 14 bits of the data stream

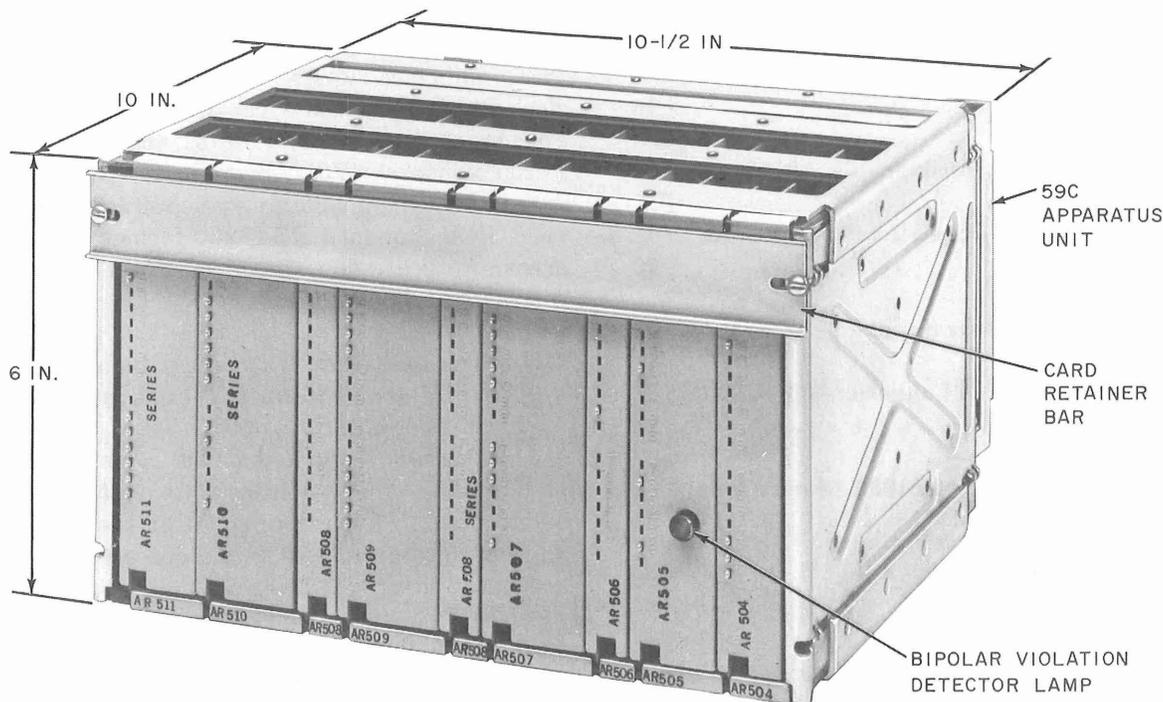


Fig. 1—33A1 Data Unit—Front View

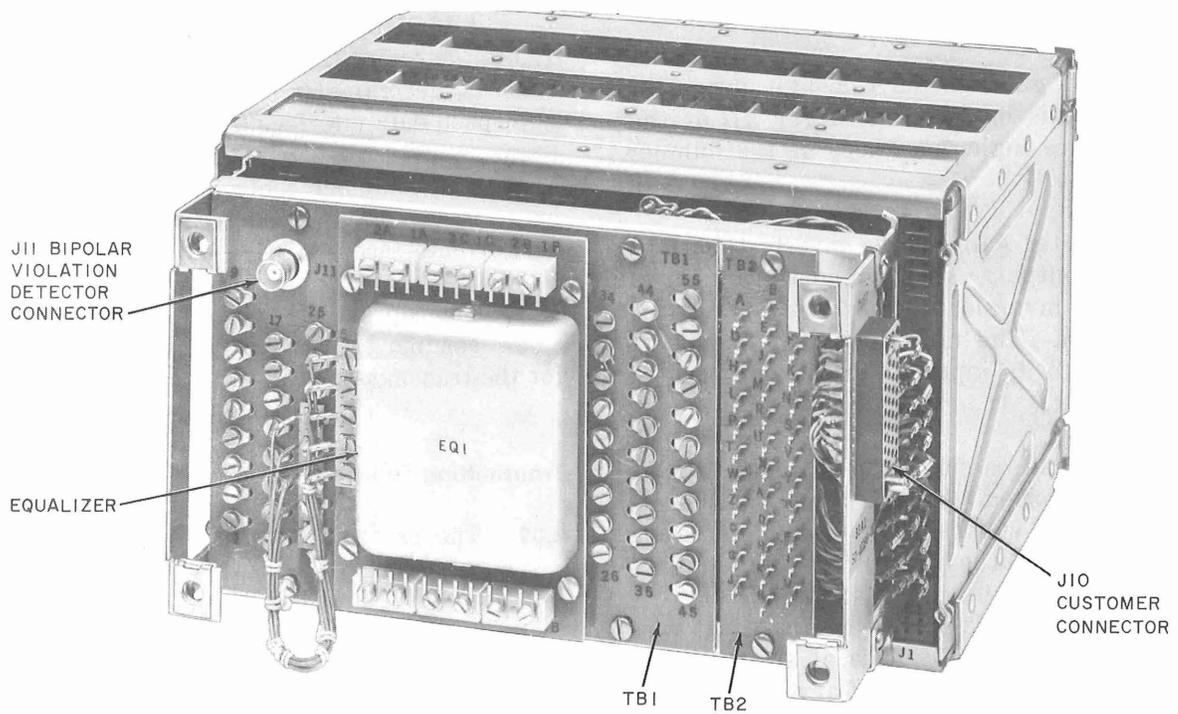


Fig. 2—33A1 Data Unit—Rear View

TABLE A
POWER REQUIREMENTS

VOLTAGE		CURRENT
NOMINALLY	MAY VARY	
+18V	+17 to +20V	400 mA
-18V	-17 to -20V	400 mA
+4.5V	+4.2 to 4.7	2.5 A

TABLE B
WORKING LIMITS

TEMP. RANGE	RELATIVE HUMIDITY
40 to 120° F	Up to 95%

being received and sent to the customer business machine. Waveform 2 shows the unbalanced 1.344-Mbps data signal. Waveform 3 shows the unbalanced data signal after being scrambled. Waveform 4 shows the digital data signal with the insertion of the framing and stuffing bits with

a data speed of 1.544 Mbps. Waveform 5 shows the bipolar line signal corresponding to the 1.544-Mbps digital signal. Notice that the positive ones or mark bits become alternate positive and negative pulses and the zero or space bits become the absence of pulses. This signal is compatible with the T1 line requirements. Waveform 6 shows the conversion from the received bipolar signal to a 1.544-Mbps digital signal. Waveform 7 is the scrambled data signal at 1.344-Mbps. After the data signal is descrambled, it is sent to the customer business machine.

3.02 Digital logic symbols used in this section are shown and explained in Fig. 4. A brief description of the logic gates is given below to aid in understanding the symbols in Fig. 4. Only two states or conditions exist in binary logic circuitry. An ON signal will represent a logic 1, high, or positive voltage and an OFF signal will represent a logic 0, low, or negative voltage unless otherwise stated. The digital logic circuit symbols used in Fig. 5 and 8 are explained in Fig. 4.

- An OR gate will have a high output, or the gate is enabled whenever *any* of the

inputs are high regardless of the number of inputs.

- An AND gate will have a high output, or the gate is enabled whenever *all* of the inputs are high regardless of the number of inputs.
- An inverter gate simply inverts the input for its output. Two symbols are used to indicate inversions: the inverter and the negation. The negation symbol may be applied to an input or to the output of a gate.
- A NOR gate is simply an OR gate with its output inverted. Thus, if any input is high, the output will be low. If all inputs are low, the output is high.
- A NAND gate is simply an AND gate with its output inverted. Thus, if all inputs are high, the output is low. If any of the inputs are low, the output is high.
- A flip-flop (F/F) is a device that has the ability to maintain an output when the inputs are removed. A set-clear flip-flop has two inputs, a set (S) and a clear (C), and two outputs, a high (1) and a low (0). The flip-flop truth table in Fig. 4 defines the outputs as functions of the S and C. Only a momentary high is needed on the S or C input to define the output state which will remain in that state until another input is applied except when both inputs are low.

3.03 Figure 5 shows a simplified functional block diagram of the 33A1 Data Unit. The heavy solid lines indicate the normal path of the send and receive data. The heavy dashed lines indicate alternate data paths when the scrambler and descrambler circuit packs are removed.

3.04 For descriptive purposes, the data unit is divided into three functions: namely transmitting, receiving, and the customer control function.

3.05 The transmitting function consists of the customer high-speed data interface (AR509), scrambler (AR508), transmitting bit rate converter (AR510), and transmitting 1.544-Mbps bipolar line interface (AR511) circuit packs and the equalizer.

3.06 The receiving function consists of the receiving 1.544-Mbps bipolar line interface (AR505), framing detector (AR506), receiving bit rate converter (AR507), descrambler (AR508), and the customer high-speed data interface (AR509) circuit packs.

3.07 The customer controls function is explained under circuit pack description for the customer controls interface (AR504).

3.08 To help simplify the functional description, assume all control signals are conditioned for the transmission and reception of data.

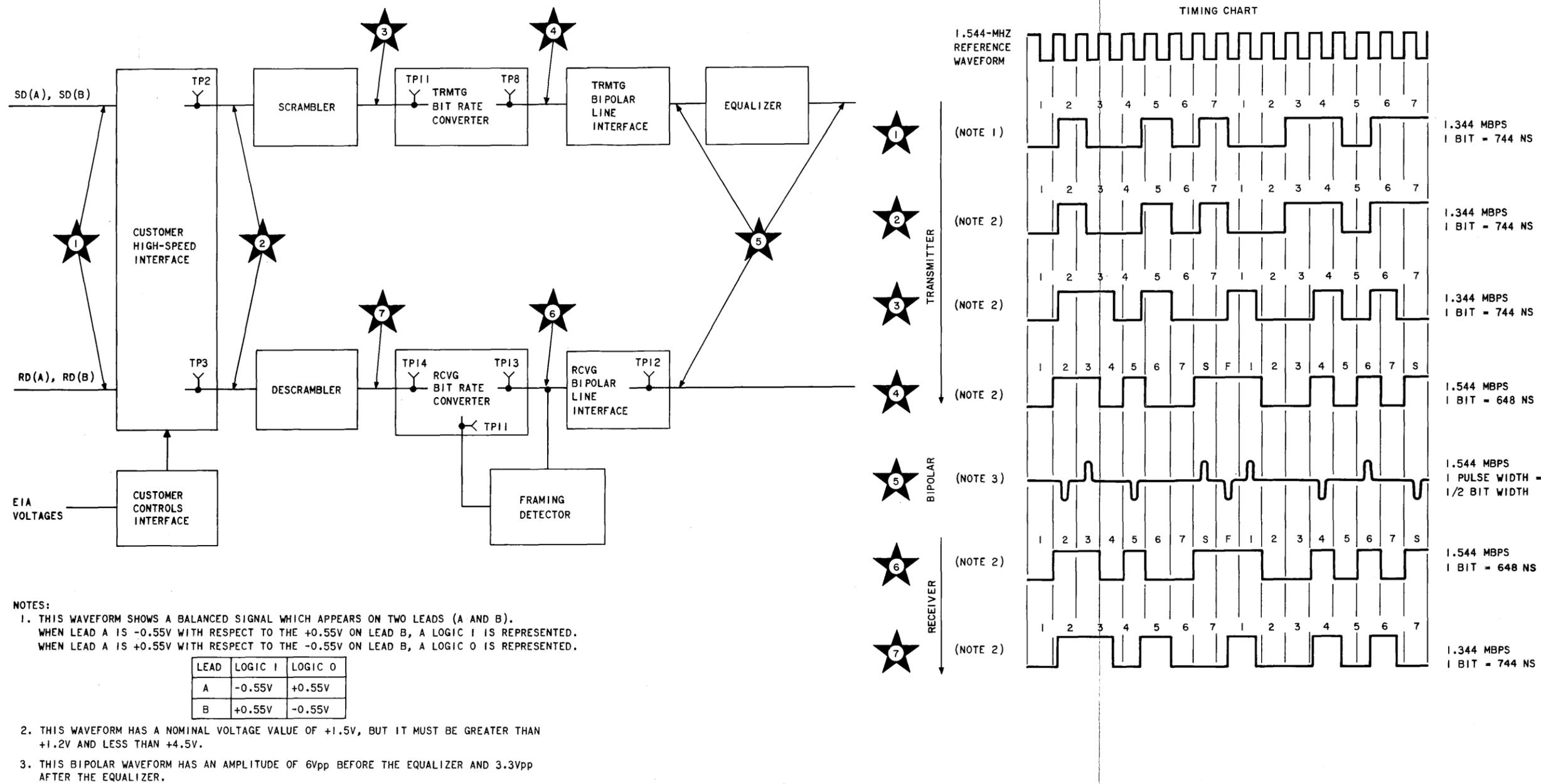
Transmitting Function

3.09 The procedure for transmitting data starts with the sync recovery in the transmitting bit rate converter CP AR510. The sync recovery locks to the master 1.544-MHz oscillator which determines the line bit rate. Its output is a 1.344-MHz square wave which is passed to the customer via the TSO lead, through a balanced cable driver on the customer high-speed data interface CP AR509, and onto the Serial Clock Transmit (SCT) leads.

3.10 The SCT clock signal is returned to the data set over the Serial Clock Transmit External (SCTE) leads. The SCTE signal is used by the business machine to clock the Send Data (SD) signal on the SD leads. Balanced cable terminators on CP AR509 convert the SCTE and SD signals to resistor-transistor logic (RTL) levels. The Transmit Gate 1 (XG1) signal controls the transmission of the SD signal. If XG1 is a one, it inhibits (blocks) the SD signal by preventing it from being retimed. If XG1 is zero, the SD signal is allowed to pass and be retimed. The SCTE signal is passed to the scrambler, CP AR508, via SCTS and its inverse to CP AR510 via SCTI.

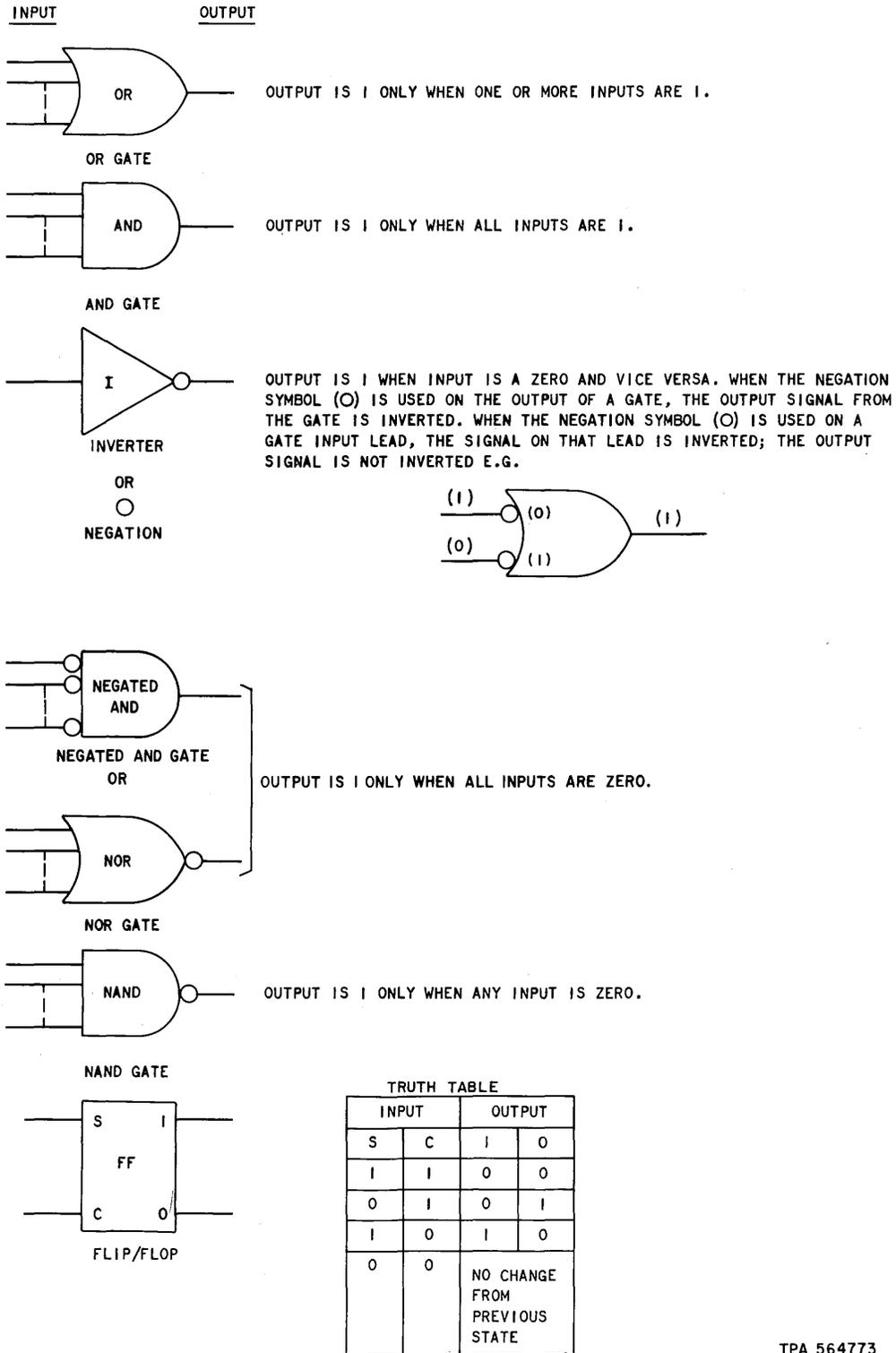
3.11 The SD signal is applied to CP AR510 via SDB, and to CP AR508 via SDA. When CP AR508 is plugged in, SP has a positive voltage applied to it and the signal on SDB is inhibited by the gate on CP AR509. Therefore, in normal use only the SDA signal is used.

3.12 The scrambler randomizes the SD signal and sends it via SDS lead if the Transmit Gate 2 (XG2) lead is held at a steady 0.



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Fig. 3—Simplified Block Diagram of 33A1 Data Unit With Timing Signals



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Fig. 4—Logic Symbol Description

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3.13 The scrambled SD signal enters the transmitting bit rate converter, CP AR510, on lead SDS. The signal is written into the elastic store under control of the steady 1.344-MHz clock on SCTI.

3.14 The framing and stuffing bits are added in the elastic store and the composite data signal is read out at 1.544 Mbps via HSD. The framing/stuffing generator is driven by the master 1.544-MHz clock via HTC which can come from either the internal 1.544-MHz oscillator or some external source on the THFC leads. Framing bits are generated every 193 bits and are alternately ones and zeros unless there is a one on the XG2 lead. When XG1 is a one, then all framing bits are ones. Stuffing bits, which are all ones, are generated every 8 bits within the 193-bit frame. The arrangement of the framing, stuffing, and data bits is shown in Fig. 6.

3.15 The sync recovery output is produced by comparing the SCTI signal and staggered 1.344-MHz signal. The staggered 1.344-MHz signal is produced from the recovered 1.544-Mbps signal by eliminating transitions during the framing and stuffing bit. This completes a clock signal loop between the data unit and the business machine to provide synchronous operation and is known as phase-lock loop.

3.16 The 1.544-MHz output of the elastic store on HSD goes to the transmitting 1.544-Mbps bipolar line interface, CP AR511. The signal is first retimed and then converted to a balanced bipolar signal in which ones becomes half-bit pulses of alternating polarity and zeros become the absences of pulses.

3.17 The bipolar line signal is then equalized to compensate for the length of cable to the T1 line terminating unit (LTU).

Receiving Function

3.18 The bipolar signal from the T1 LTU is transformer-coupled into the bipolar-to-binary converter. The signal is monitored by the bipolar violation detector which has an output whenever two successive ones have the same polarity. After conversion, the 1.544-Mbps binary signal on HRD goes to the elastic store in the receiving bit rate converter CP AR507 and the framing detector CP AR506.

3.19 The exact bit rate of the received signal is derived by the 1.544-MHz clock extraction circuit which produces a clock signal on the HRC lead which is used to drive the framing and stuffing generator and the framing detector.

3.20 To synchronize the framing and stuffing generator with the received signal, framing pulses on lead FRR are sent to the framing detector. The detector examines the received signal only during the framing pulses and shifts the framing pulses on lead FRR until the received signal during the framing pulses is alternately 1s and 0s which means that frame sync is established.

3.21 When frame sync is achieved, the RDF lead is made a one. Thus, a one on the RDF lead means that the data set is receiving a valid framing signal. In the absence of a signal, the RDF lead is forced to zero by the clock monitor circuit.

3.22 The received signal is written into the elastic store by the "staggered 1.344" which is the recovered 1.544-MHz clock with transitions missing during the framing and stuffing bits. Thus, only the data bits are written into the elastic store. The data is read out of the elastic store by the steady 1.344-MHz clock from the sync recovery which locks onto the staggered 1.344-Mbps signal.

3.23 The 1.344-Mbps output on RDB is sent to the descrambler CP AR508 and to the RD selector on the customer high-speed data interface CP AR509. When the descrambler is used, a positive voltage on lead DP blocks the RDB input to the interface circuit. The descrambler changes the scrambled data back to its original form without need for a synchronizing signal from the scrambler.

3.24 The descrambled data passes through the RD selector and is retimed by the steady 1.344-MHz clock signal. The received data may be inhibited (blocked) by a one on the RG lead.

3.25 The received data and the recovered, steady 1.344-MHz clock are sent to balanced cable drivers and are delivered to the business machine on leads RD and SCR, respectively.

CIRCUIT PACK DESCRIPTION

3.26 Each circuit pack has a faceplate with numbered test points and an AR code number

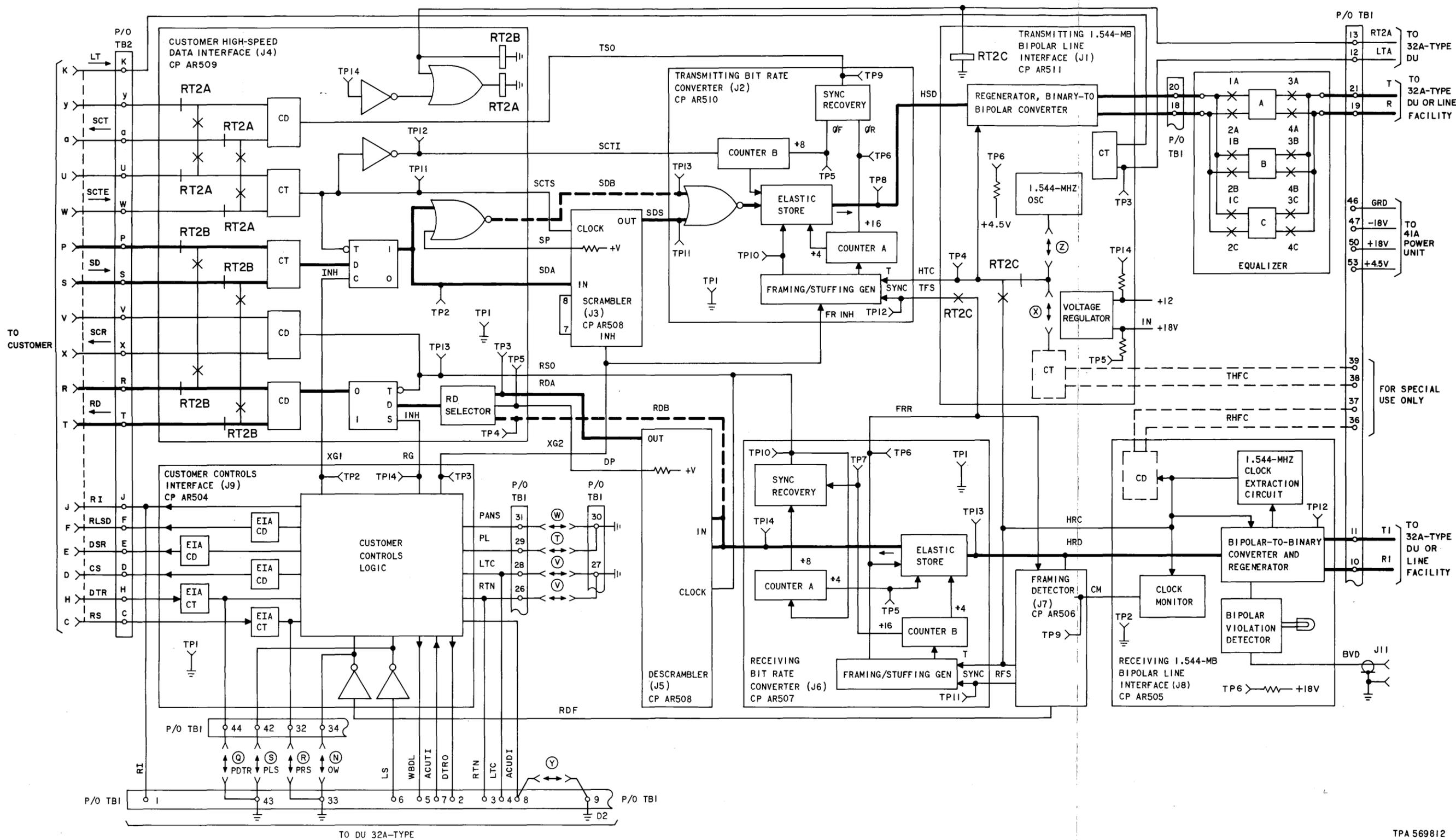


Fig. 5—Simplified Functional Block Diagram of 33A1 Data Unit

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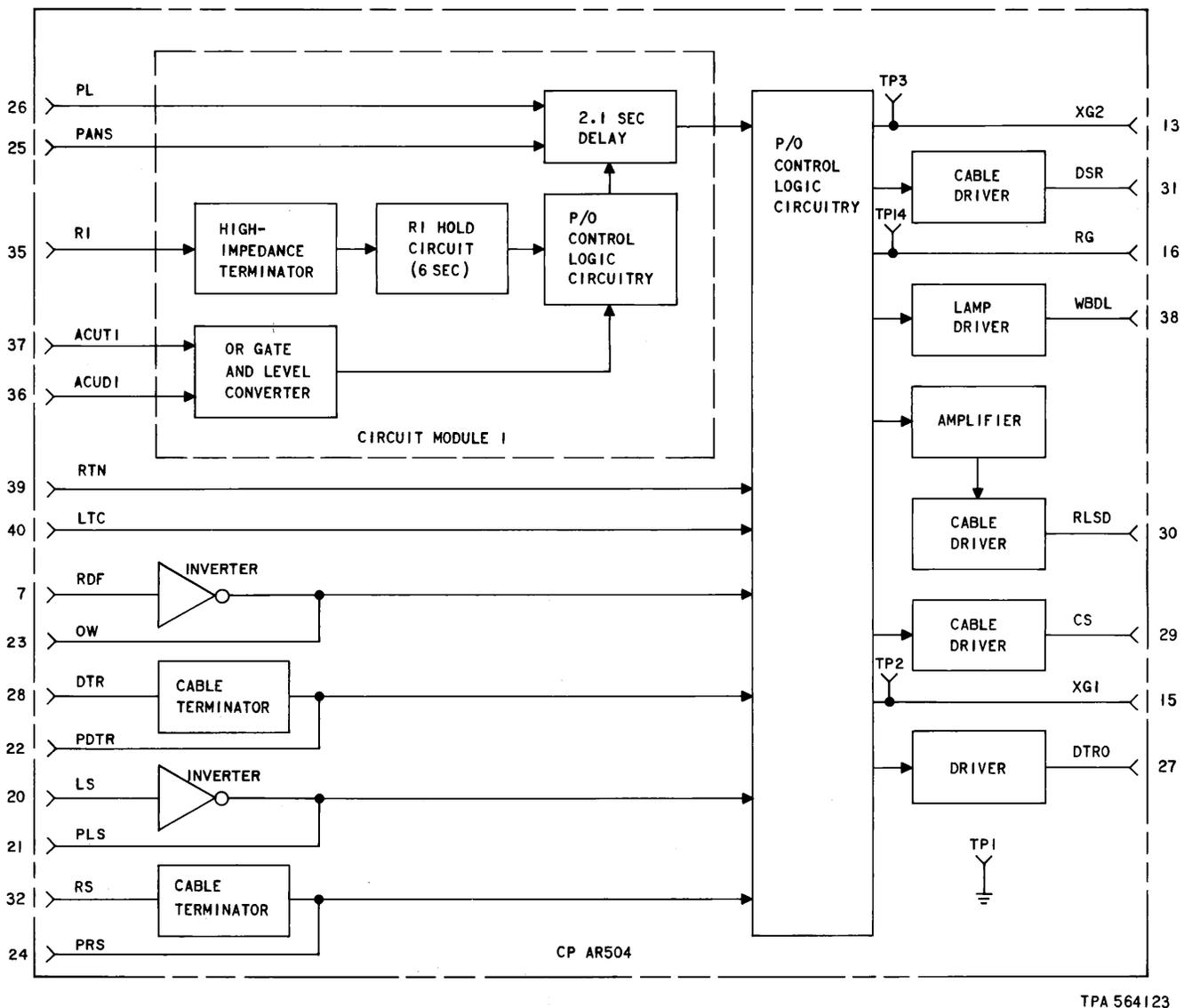


Fig. 7—Customer Controls Interface—Functional Block Diagram CP AR504

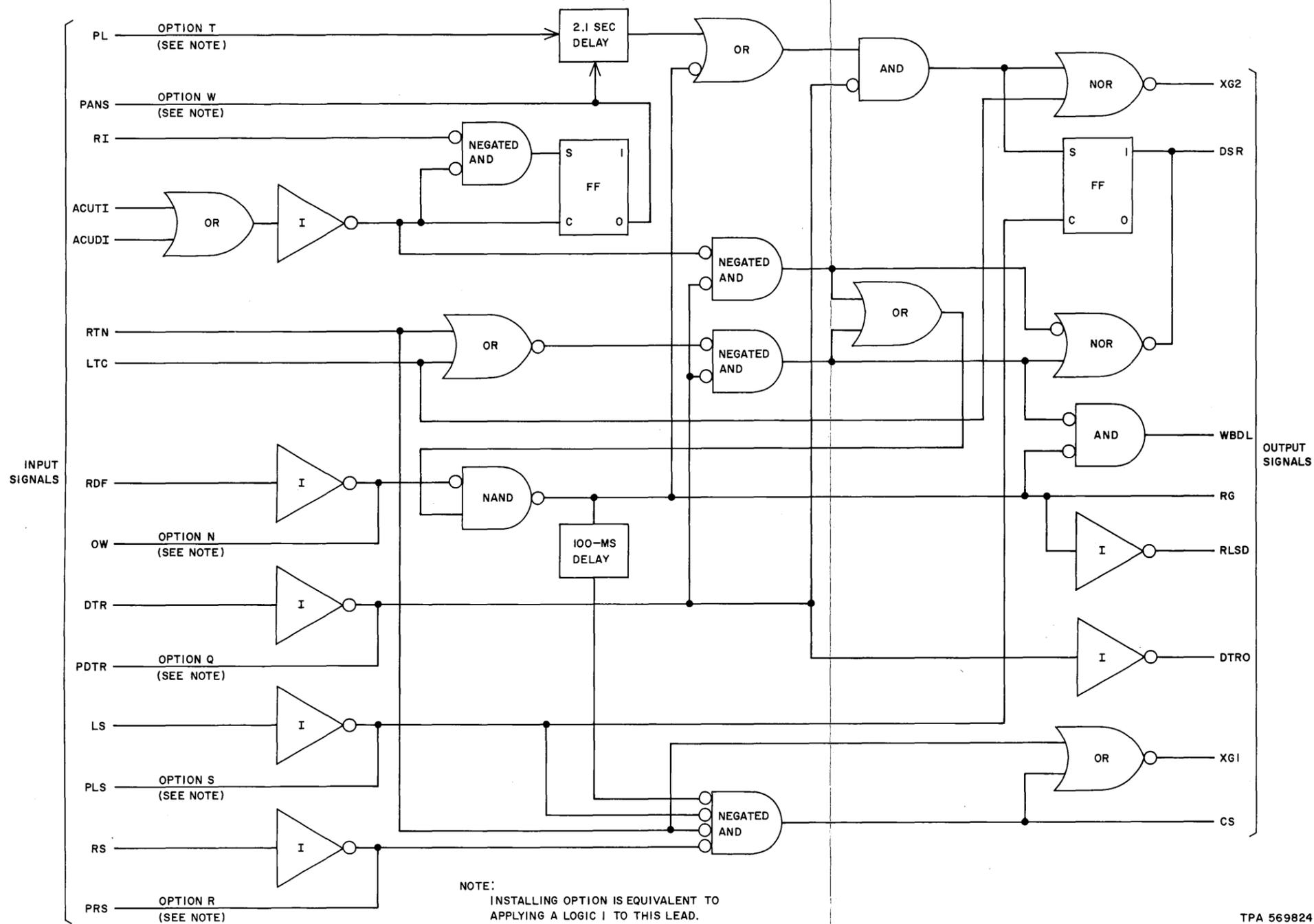
3.35 The Private Line (PL) and Permanent Answer (PANS) leads will be described under options T and W, respectively.

3.36 Ring Indicator (RI) is used in conjunction with the Automatic Calling Unit Talk Indicator (ACUTI) and Automatic Calling Unit Data Indicator (ACUDI) to distinguish the answering data set from the originating data set. The presence of ringing will cause the RI hold circuit on circuit module 1 to be held at ground between rings. Six seconds after the last ring, the RI hold circuit output will

go high allowing another call to be answered. See 3.39.

3.37 Automatic Calling Unit Talk Indicator (ACUTI) signal is used in conjunction with the ACUDI signal to determine an "off-hook" condition. A ground is placed on this lead whenever an associated Data Auxiliary Set (DAS) 804 is "off-hook" in the talk mode.

3.38 Automatic Calling Unit Data Indicator (ACUDI) signal is used in conjunction with the ACUTI signal to determine the "off-hook" or on-line



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Fig. 8—Simplified Control Logic Circuitry of Customer Controls Interface CP AR504

condition. A ground is placed on this lead whenever an associated DAS 804 is "off-hook" in the data mode or "on-hook" in the data mode with Data Terminal Ready (DTR) ON.

3.39 The RI, ACUTI, and ACUDI signals provide one method to establish an ON signal on the XG2 and Data Set Ready (DSR) leads.

3.40 Remote Test Normal (RTN) is an indicator lead for the remote test mode. The ground is removed from this lead whenever the data set is placed in either the remote test 1 or remote test 2 mode. This will cause an OFF condition on the Clear-to-Send (CS), Wideband Data Lamp (WBDL), XG1, and DSR leads.

3.41 Local Test Control (LTC) is an indicator lead for the local test mode. The ground is removed whenever the data set is placed in the local test mode. This will cause an OFF condition on the Receive Gate (RG), DSR, Receive Line Signal Detector (RLSD), and WBDL leads.

3.42 Receive Data Framing (RDF) indicates when the data set is in frame sync by supplying an ON signal originating from the framing detector CP AR506. This signal is also referred to as Receive Data Monitor (RDM). A permanent RDF ON signal may be installed by strapping option N. When the data set is out of frame sync (RDF is 0), an OFF condition is on the XG2, WBDL, RLSD, RG, and CS leads.

3.43 Data Terminal Ready (DTR) is used to control the holding and dropping of a wideband call. A DTR ON signal is required for transmission of framing signals and to enable the data set to answer a call automatically when automatic answering is used. An OFF signal will terminate the call and cause an OFF condition either directly or indirectly on all the outputs (XG2, DSR, RG, WBDL, RLSD, CS, XG1, and DTRO). For private line applications, a permanent DTR ON signal may be established by strapping option Q. Other methods are also available to supply a DTR ON signal, such as from the customer equipment or from the associated equipment. The method of supplying the DTR signal is dependent upon how the system is to be operated. Refer to 593-801-100 for more information on system arrangements.

3.44 Line Status (LS) is used in special applications where coordinated voiceband data is required.

Refer to 593-801-100. Normally used is a permanent ON signal supplied by strapping option S. An LS OFF signal will cause an OFF condition on the CS, XG1, and DSR leads.

3.45 Request-to-Send (RS) signal must be in an ON condition to send wideband data. It may be wired permanently ON in the business machine or in the data unit by strapping option R. An OFF signal will cause an OFF condition on the CS and XG1 leads, but the data unit will continue to transmit a framing sync signal to maintain bit synchronization.

3.46 The output signals of the customer controls interface consist of XG2, DSR, RG, WBDL, RLSD, CS, XG1, and DTRO and are described in 3.47 through 3.54.

3.47 Transmit Gate 2 (XG2) is used to control framing signals being transmitted from the data set. An ON signal is represented by a logic 0, thus allowing framing and scrambler idle code transmission. The XG2 signal is affected by the LTC, DTR, RDF, PANS, ACUTI, ACUDI, RI, and RTN signals.

3.48 Data Set Ready (DSR) indicates that the data unit is not in a test mode and may transmit wideband data provided CS is ON and may receive wideband data provided RLSD is ON. DSR is affected by LS, DTR, PANS, RI, ACUTI, ACUDI, RDF, RTN, and LTC signals.

3.49 Receive Gate (RG) is used to either pass or block the Receive Data (RD) signal. When RG is at a logic 0, it allows the receive data to be transmitted to the customer, otherwise the customer RD lead is held in the steady mark condition. RG is affected by the RDF, LTC, RTN, DTR, ACUDI, and ACUTI signals.

3.50 Wideband Data Lamp (WBDL) signal is used to light a lamp in an associated DAS 804A-type when the data unit is in a condition where wideband data may be received. WBDL is affected by the RG, DTR, RTN, and LTC signals.

3.51 Receive Line Signal Detector (RLSD) signal is one indication that signals on the RD lead are reliable. An ON condition is an indication that the data unit is in frame sync and is receiving good framing information over the T1 line from the distant data set. When RLSD is OFF, the

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RD lead will be held in the "mark hold" state and the CS lead will be held OFF. RLSD is affected by the RDF, DTR, LTC, RTN, ACUTI, and ACUDI signals.

3.52 Clear to Send (CS) indicates that the wideband data unit is in a condition to permit either the transmission or reception of data or test signals in a local test condition. A time delay is built into the logic circuitry for the CS circuit to insure that the wideband data sets at both ends are in bit synchronization before CS is turned ON. The time delay, approximately 100 milliseconds, is measured from the time RLSD goes ON. Once the time delay has elapsed, the CS signal will follow the RS signal. CS is affected by the LS, RS, RTN, and RG signals.

3.53 Transmit Gate 1 (XG1) is used to enable or inhibit the send data signal from the input of the scrambler, otherwise the scrambler input is held in the steady mark condition. XG1 is affected by the RTN, LS, RS, and RG signals.

3.54 Data Terminal Ready Out (DTRO) signal is the inverted form of the DTR signal and affected only by DTR.

B. Receiving 1.544-Mbps Bipolar Line Interface—CP AR505

3.55 Figure 9 shows a simplified functional block diagram of circuits which convert the incoming 1.544-Mbps bipolar signal into a 1.544-Mbps digital data signal and also provide a bipolar violation detector. The bipolar-to-binary circuitry is contained on the main board and the bipolar violation detector is incorporated in an attached circuit module (CM1).

3.56 The incoming bipolar signal is transformer-coupled from the T1 and R1 leads. The impedance-matching pad serves to drop the signal to a workable level and improves the return loss. The low-pass filter removes the high-frequency noise components from the input signal. The signal is applied to the differential comparator circuits and to the automatic threshold circuit. The automatic threshold circuit peak-rectifies the signal to produce negative and positive reference voltages equal to one-half the peak signal amplitude for the differential comparator circuits. Here is where the bipolar-to-binary conversion occurs with the bipolar positive and negative pulses becoming binary ones. This output signal is sent to the logic circuits while being

monitored by the bipolar violation detector (BVD). The detector checks the incoming data and lights a lamp every time two one pulses occur without alternating. The violations are accessible on the BVD lead by connecting an electronic counter to J11. Normally, +1 volt is applied when terminated into 50 ohms resistance. When a violation occurs, it produces a 324-nanosecond pulse or short to ground, thus registering one violation.

3.57 The 1.544-MHz clock recovery or extraction circuit produces a clock signal from the data signal. The clock signal on lead HRC is used to retime the data signal. Also on the circuit module is a balanced cable driver which allows external use of the recovered 1.544-MHz clock signal for special applications. The output is on leads Receive High Frequency Clock (RHFC) A and B. The clock signal is sent to the clock monitor where it is rectified to produce a positive voltage on CM whenever clock is present on HRC and is at ground otherwise.

C. Framing Detector—CP AR506

3.58 A simplified functional block diagram of the framing detector is shown in Fig. 10. The framing detector samples the receive data signal on lead HRD every 193 bits under control of FRR from the framing generator on AR507. If the sampled bits consistently alternate between 1 and 0, the framing generator is assumed to be in frame synchronization with the received data, and RDF is made a logic 1. If the sampled bits do not consistently alternate between 1 and 0, the framing generator is assumed to be out of frame synchronization and RDF is set to 0. Then a pulse is produced on RFS one bit later than the framing pulse on FRR to shift the framing generator by one bit. If CM is zero, indicating no received data signal, RDF is forced to a logic 0. The recovered clock, HRC, is used to provide certain timing functions.

D. Receiving Bit Rate Converter—CP AR507

3.59 A simplified functional block diagram is shown in Fig. 11. This CP converts the 1.544-Mbps data signal on HRD into a 1.344-Mbps data signal on RBD by removing the framing and stuffing bits. The converter has two circuit modules mounted to the main board. The main board also contains two counters (dividers) and the elastic store.

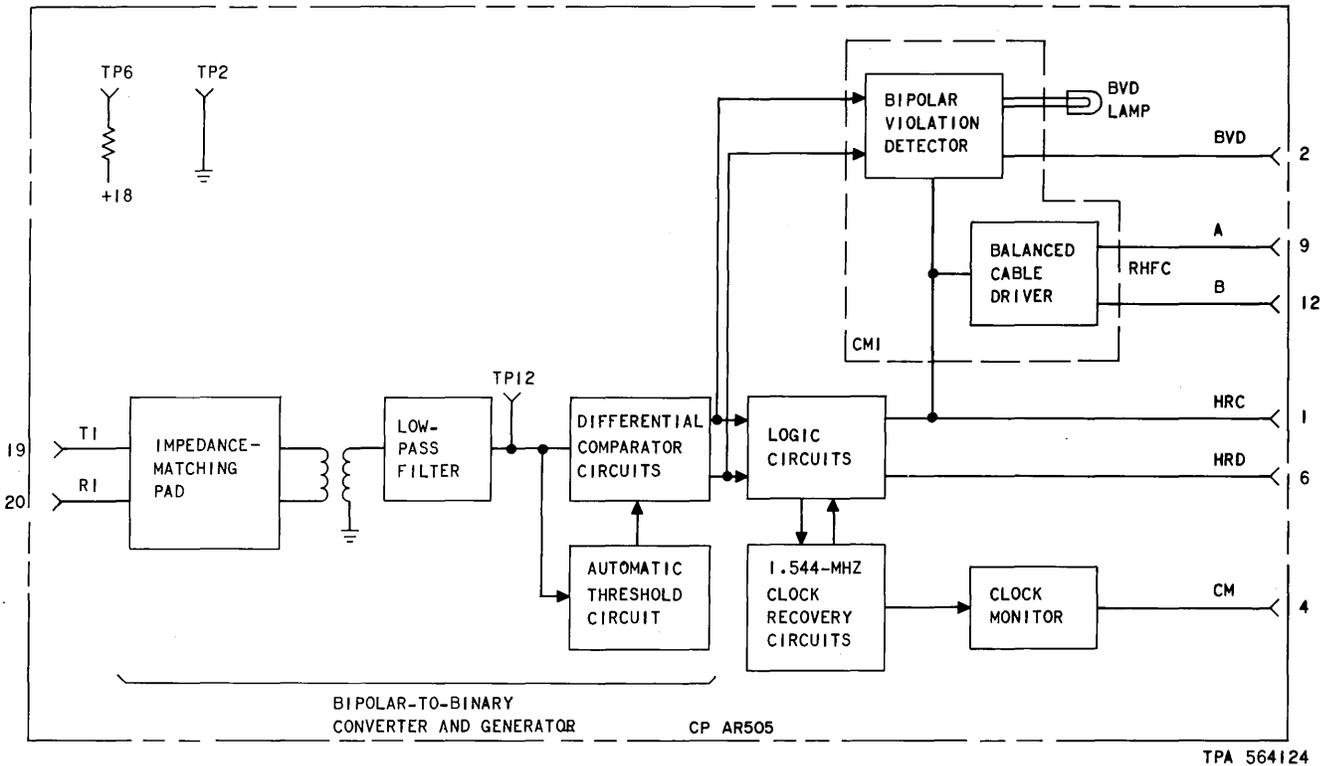


Fig. 9—Receiving 1.544-MBPS Bipolar Line Interface—Functional Block Diagram CP AR505

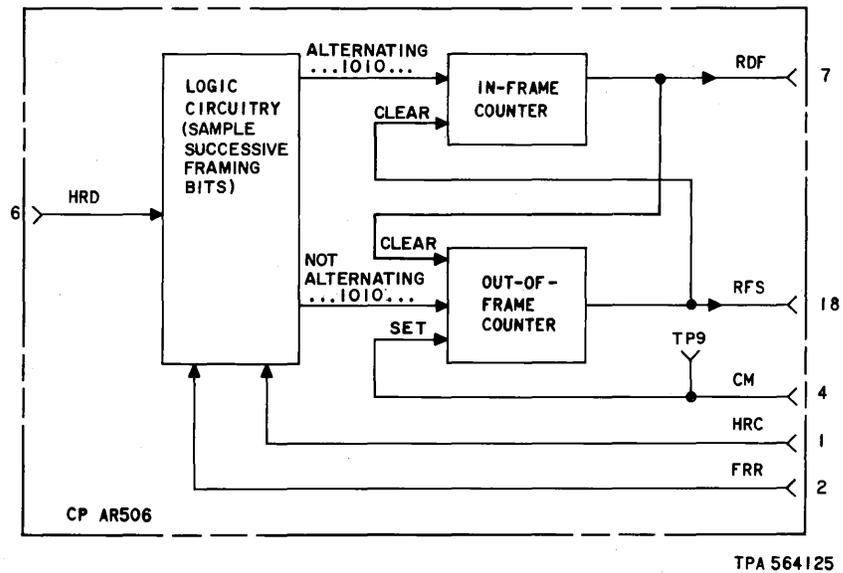


Fig. 10—Framing Detector—Functional Block Diagram CP AR506

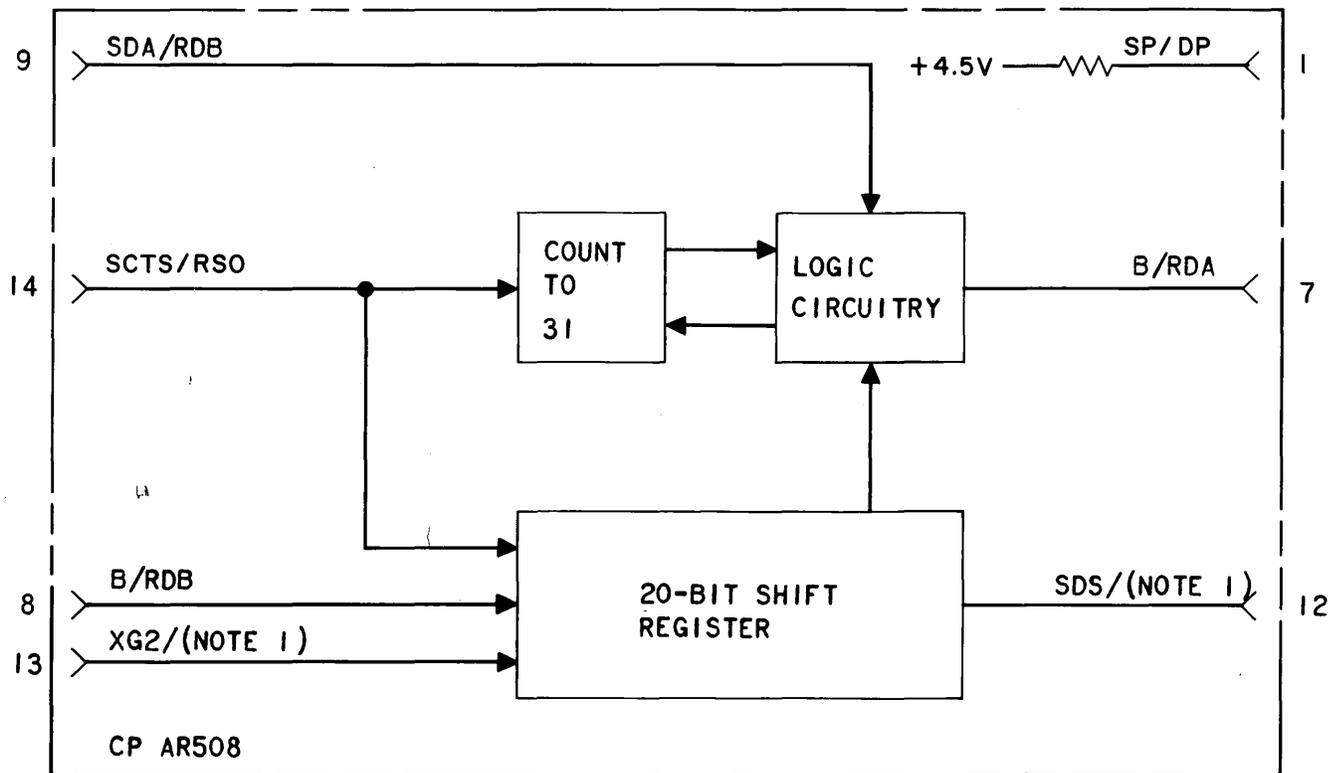
3.64 Figure 5 shows the data paths with and without the scrambler and the descrambler which are controlled by the SP/DP lead. When these CPs are utilized, the data is sent and received on the SDA and the RDA leads (heavy solid lines), respectively. When both CPs are removed, the data is sent and received over the SDB and the RDB leads (heavy dashed lines), respectively.

3.65 A simplified functional block diagram is shown in Fig. 12 for both the scrambler and the descrambler which use the same circuit pack circuitry. The lead designation before the slash applies to the scrambler and after the slash to the descrambler.

3.66 The scrambler is used on the transmit side to randomize the 1.344-Mbps data signal. The SD signal enters on the SDA lead to the logic

circuitry where it is combined with a signal from the counter (count to 31) and a signal consisting of the 3rd and 20th stages of the shift register. The resulting signal is random data that is the input to the shift register since terminal 7 is connected to 8. A 1.344-MHz clock signal on SCTS is sent to the count to 31 and shift register and shifts the data bits on each negative-going transition. The count to 31 along with the monitor circuits of the logic circuitry prevents short words or all ones (1) or all zeros (0) from becoming repetitive. The scrambler output on SDS may be held in the 0 state if the control logic circuit pack (AR504) applies an inhibit signal on XG2.

3.67 The descrambler is used on the receive side to de-randomize the 1.344-Mbps data signal received on RDB with two inputs at terminals 8 (shift register) and 9 (logic circuitry). Operation



NOTES:

1. THIS LEAD IS NOT USED IN THE DESCRAMBLER.
2. THE LEAD DESIGNATION BEFORE THE SLASH APPLIES TO THE SCRAMBLER, AFTER THE SLASH TO THE DESCRAMBLER.

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Fig. 12—Scrambler/Descrambler—Functional Block Diagram CP AR508

of the shift register and the counter is identical to that in the scrambler, but the inputs and outputs are changed somewhat to reverse the process. The 1.344-Mbps clock signal on RSO allows the data bits to be timed onto lead RDA. Terminals 12 and 13 are not used.

F. Customer High-Speed Data Interface—CP AR509

3.68 A simplified functional block diagram is shown in Fig. 13. This CP provides for the interchange of balanced signals consisting of clocks and data with the customer. The CP contains balanced cable drivers and terminators, logic circuitry, and relays that provide the remote test 2 mode. The high-speed balanced cable drivers accept binary signals and convert them to a balanced signal output at 100 ohms impedance with approximately 1.1 volts peak-to-peak differential. The high-speed balanced cable terminators accept balanced line signals and convert them into binary signals compatible with resistor-transistor logic for integrated circuits. The input impedance is 100 ohms. The data unit is placed in the remote test 2 mode whenever relays RT2A (K1) and RT2B (K2) are operated under control of the RT2A lead.

3.69 Balanced signals are used for Serial Clock Transmit (SCT), Serial Clock Transmit External (SCTE), Send Data (SD), Receive Data (RD), and Serial Clock Receive (SCR). These balanced signals cannot be measured with a vacuum tube voltmeter. Although an indication is present, it is not useful. An oscilloscope must be used to determine the quality of the balanced interface signal. The balanced voltage signal is sent over two leads which are referenced to ground. One lead is labeled A and the other B. Whenever a negative .55V appears on lead A and a positive .55V appears on lead B, this condition represents a binary 1. Whenever the A lead is a positive .55V and the B lead is a negative .55V, this condition represents a binary 0. Therefore, the measurement of balanced signals must be accomplished by a dual trace oscilloscope (Tektronix model 422 or equivalent) with one probe on the A lead and the other probe on the B lead. The procedures for obtaining the waveforms for the balanced signals are given in 3.81.

3.70 Serial Clock Transmit is a 1.344-MHz balanced clock signal transmitted to the customer over the SCT (A), terminal Y on TB2, and SCT (B) terminal a on TB2 leads. The clock signal has

an accuracy of ± 0.003 percent which is equal to that of the 1.544-MHz oscillator on CP AR511 and received on the TSO lead. The symmetry of the SCT signal should be as shown in Fig. 14. Notice the signal is positioned half above and below a center line or a zero crossing line. Also, one cycle covers five divisions which represents one period. The negative-going transition must pass within the limits of .45 and .55 of the clock period. To determine where the limits are located on the zero crossing, multiply the 5 divisions (1 period) by .45 which equals 2.25 divisions for the left limit. Now multiply the 5 divisions by .55 which equals 2.75 divisions which is the right limit. In this example, the negative-going transition must pass between the limits.

3.71 Serial Clock Transmit External is a 1.344-MHz balanced transmit clock signal received from the customer over the SCTE (A), terminal U on TB2, and SCTE (B) terminal W on TB2. The SCTE signal is generated from the SCT signal supplied from the data unit and is used to clock the send data signal. The SCTE signal must be present prior to the transmission of data per interface specifications. After the SCTE signal is terminated, it appears on the Serial Clock Transmit Scrambler (SCTS) lead and its inverted form appears on the Serial Clock Transmit Inverted (SCTI) lead. The signal on SCTS has the same transitions as the SCTE clock signal and is used as a synchronizing pulse for the scrambler. The SCTI signal is a source for a smooth 1.344-MHz clock used in the transmitting bit rate converter. The SCTS signal is also sent to a regenerator where it is used to retime the SD signal.

3.72 The symmetry of the SCTE signal should be as shown in Fig. 15. The transitions should occur between .4 and .6 of a clock period. The same procedure is used to find the zero crossing limits as described in 3.70, but .4 and .6 are used instead of .45 and .55. Notice the limits are wider for the SCTE signal and the waveform shows a negative-going transition. The transitions crossing the zero line (zero crossing) may be measured at the data set connector with the leads terminated in the data set or in an external 100-ohm resistor.

3.73 The SP signal is sent to the SD control where the signal determines the lead over which the SD signal will be sent. The SP signal is held at a logic 1 when the scrambler board is plugged into the data set. This causes the SDB

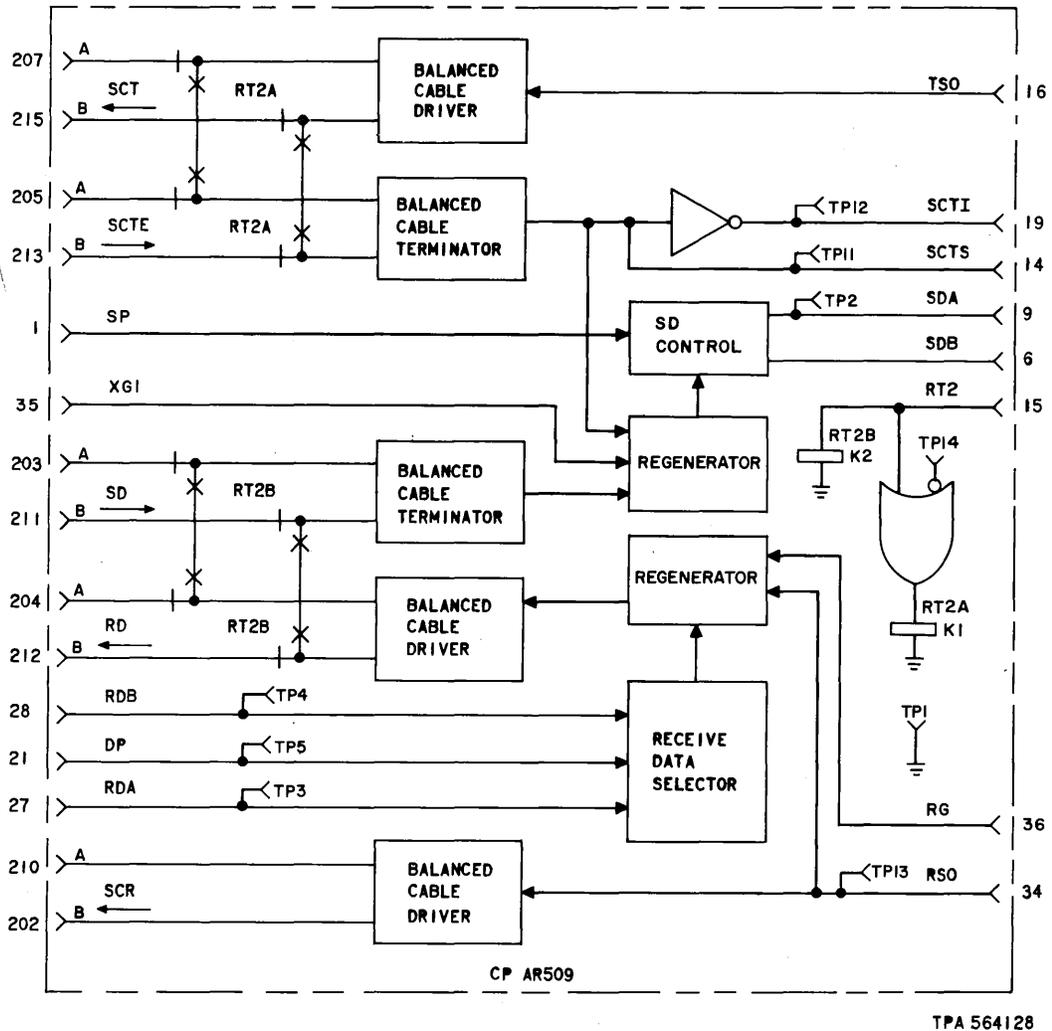


Fig. 13—Customer High-Speed Data Interface—Functional Block Diagram CP AR509

lead to be clamped to a logic 0 and the SD signal is sent over the SDA lead. If the scrambler is removed, the clamp on SDB is removed and the SD signal is transmitted over the SDB lead.

3.74 The Transmit Gate 1 signal at terminal 35 is applied to a send data regenerator as shown in Fig. 13. Normally, XG1 is a logic 0 (ON) which allows the SD signal to pass on either lead SDA or SDB. When XG1 is a logic 1 (OFF), the regenerator output is held at a logic 0 causing a steady mark to be sent on both the SDA and SDB leads.

3.75 Send Data is a balanced 1.344-Mbps serial binary data signal from the business machine.

The SD signal is sent over the SD (A), terminal P on TB2, and SD (B) terminal S on TB2, and must be properly aligned with the SCTE signal. After the SD signal is terminated, it is passed to the regenerator or inhibitor where it is joined by the XG1 and SCTE signals. After being retimed and allowed to pass, the SD signal is sent to the SD control where it is sent over either the SDA or SDB lead. The symmetry of the SD signal should be as shown in Fig. 16 which shows two bits of data expanded over 10 divisions instead of one cycle expanded over 5 divisions like the other balanced signals. However, the two bits per ten divisions is the same time scale as one clock cycle per five divisions. The SD signal is clocked on the positive-going transition of the SCTE (A)—SCTE

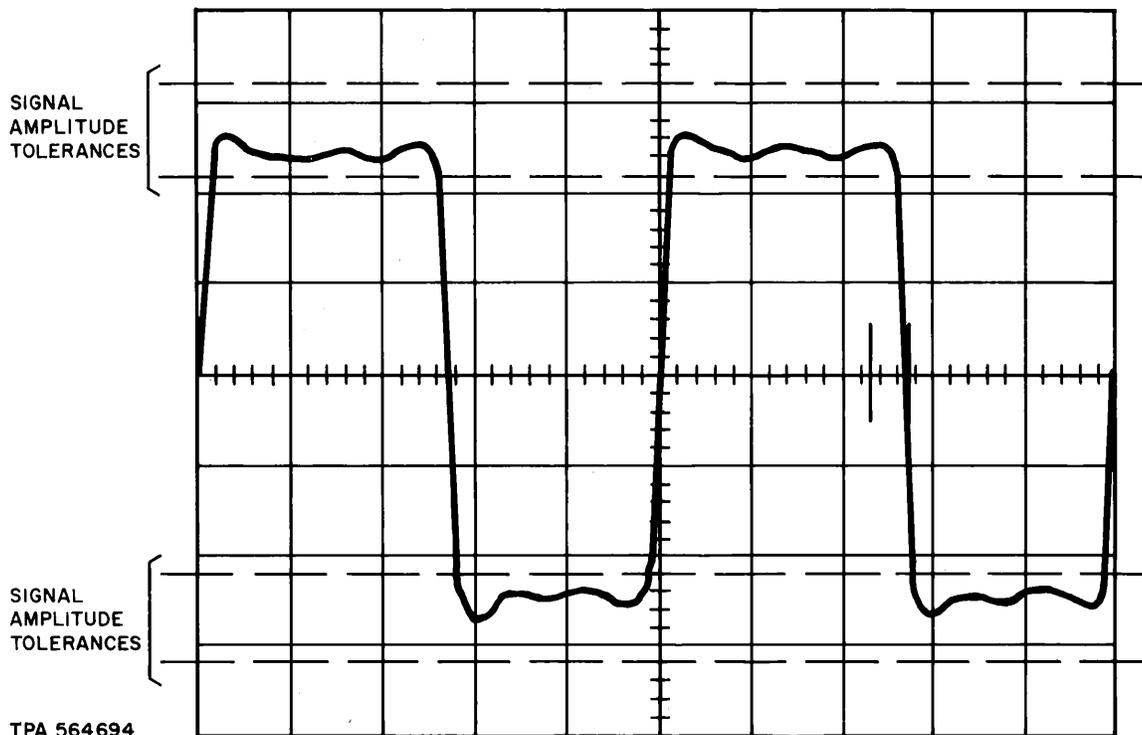


Fig. 14—Serial Clock Transmit Signal [SCT(A)—SCT(B)]

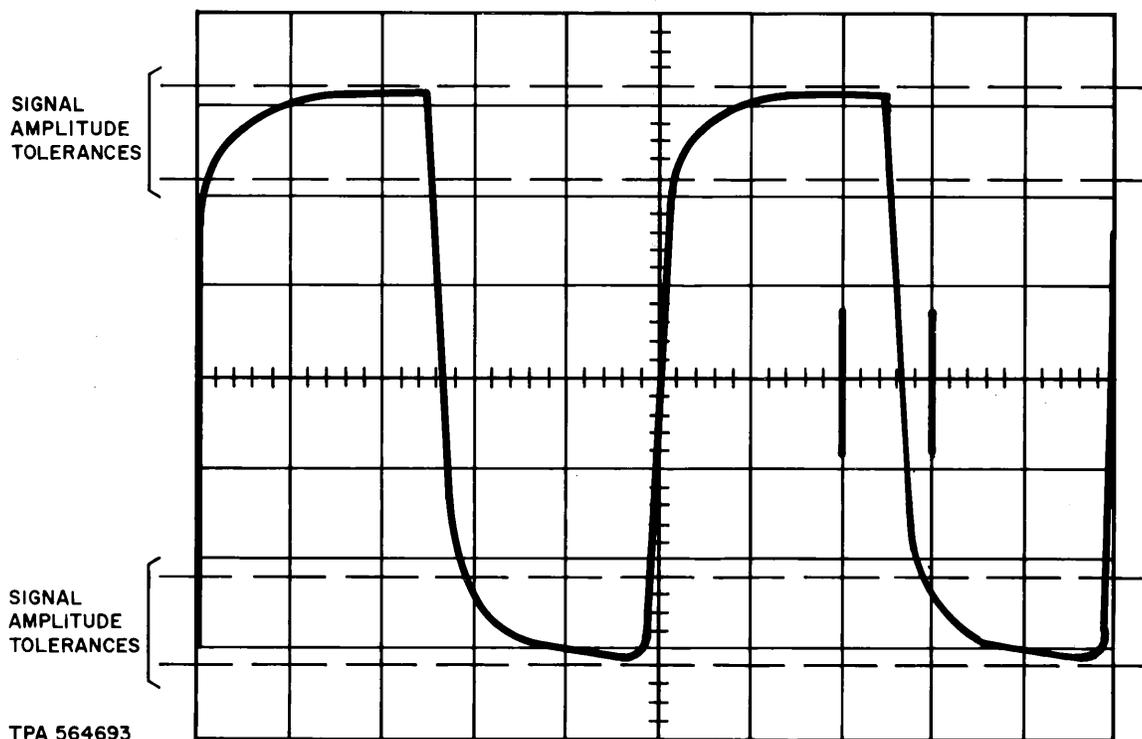


Fig. 15—Serial Clock Transmit External Signal [SCTE(A)—SCTE(B)]

(B) signal. The SD transitions cannot lead or lag the SCTE transitions by more than 10 percent of the SCTE clock period. Therefore, the SD signal should be sent simultaneously with the SCTE signal. The above requirements may be measured at the data unit connector as described under Oscilloscope Waveforms. Further information may be obtained in Section 593-801-100.

3.76 Receive Data is a balanced 1.344-Mbps serial binary data signal which is sent to the customer over the RD (A), terminal R on TB2,

and RD (B) terminal T on TB2 leads. The receive data input is present on both the RDA and RDB leads to the receive data selector. However, only one RD signal is allowed to pass to the RD regenerator which depends on the signal on the DP lead. If this lead is positive, thus indicating the descrambler is plugged in the data unit, then the signal on the RDA lead is selected. If the DP lead is zero, thus indicating the descrambler is not plugged in, then the signal on the RDB lead is selected. After selecting the RD signal, it is sent to a regenerator where it is retimed by the RSO

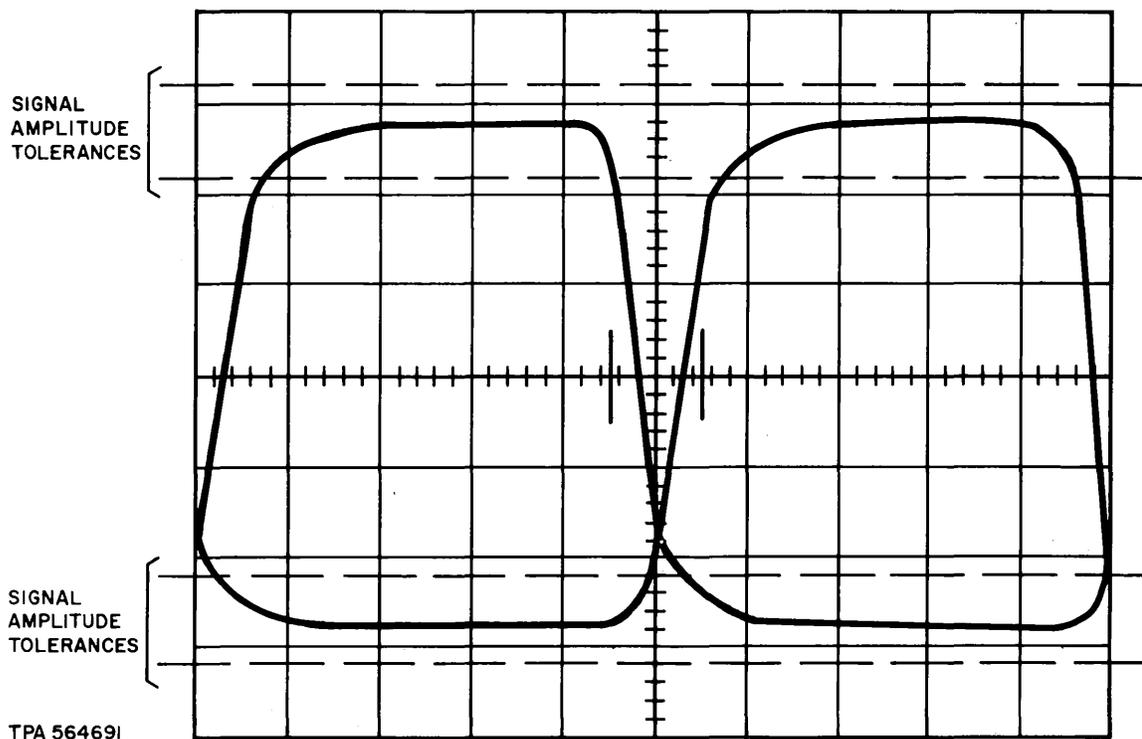


Fig. 16—Send Data Signal

clock signal. Then the RD signal is sent to the RD balanced cable driver. The RD and SCR signals have the same timing relationship as the SD and SCTE signals. The symmetry of the RD signal should be as shown in Fig. 17 and the transitions should occur between .45 and .55 of the SCR clock period.

3.77 The RD regenerator will be held in the mark-hold condition whenever the RG signal is a logic 1. During the mark-hold condition, the RD (A) lead is negative with respect to the RD (B) lead and this represents the equivalent of receiving a binary ONE. Normally, RG is a logic 0 (ON) which unclamps the RD signal and allows the receive data signal to pass to the customer.

3.78 Serial Clock Receive is a balanced 1.344-MHz clock signal sent to the customer over the SCR (A), terminal V on TB2, and SCR (B) terminal X on TB2 leads. The symmetry of the SCR signal is the same as the SCT signal as shown in Fig. 14. The transitions should occur between .45 and .55 of the clock period. Variations in the SCR clock periods between adjacent cycles are expected to be less than 0.1 percent of a clock period. The

SCR may suffer jitter and since the RD signal is timed by the SCR, they will jitter simultaneously.

3.79 The TSO signal is a 1.344-MHz clock signal originating from the sync recovery in CP AR510. It is the input clock for the SCT clock signal.

3.80 The Remote Test 2 (RT2) signal operates the RT2A and RT2B relays by supplying an ON (voltage) signal. This loops the SCT to the SCTE and the RD to the SD leads allowing the data set to retransmit the received data. Grounding TP14 causes RT2A, but not RT2B, to operate and loops SCT to SCTE.

Oscilloscope Waveforms

3.81 The oscilloscope waveform of the balanced signals of the customer high-speed interface may be obtained by using a Tektronix 422 or equivalent with two times ten (X10) attenuator probes. Carefully adjust the compensation and gain of both channels for identical response. Check the compensation and gain by connecting both probes to the same signal and set both VOLTS/DIV

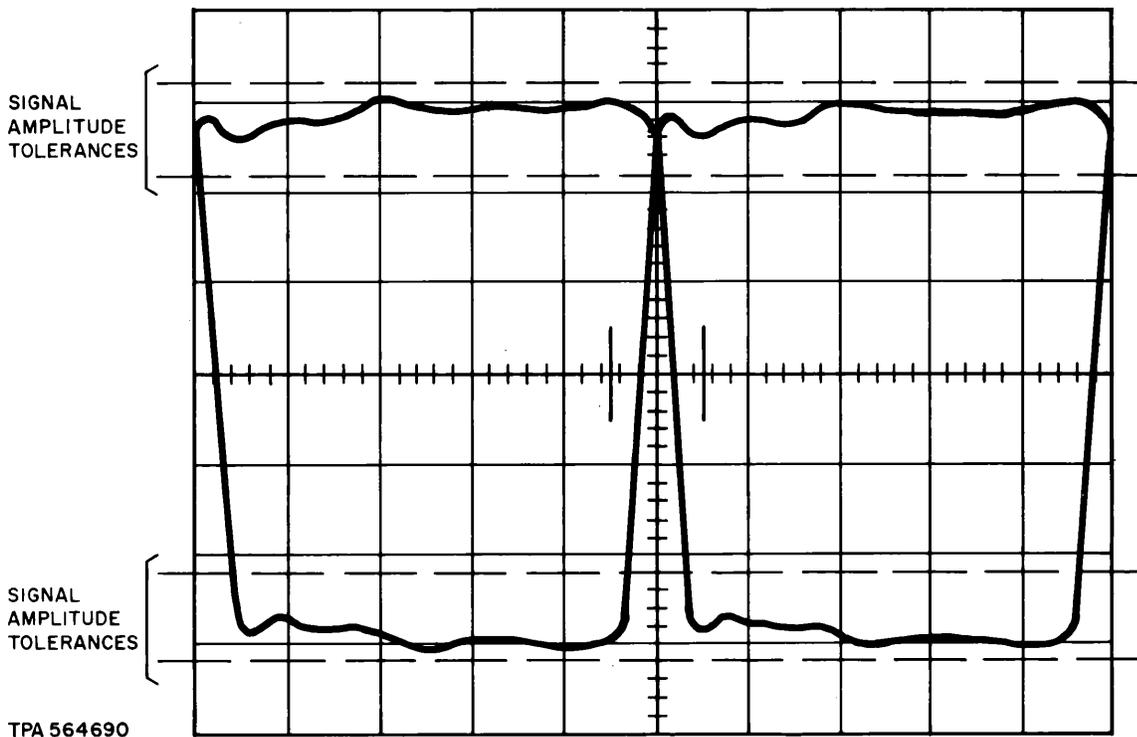


Fig. 17—Receive Data Signal

switches on the scope to .01. Add the two signals algebraically with channel 2 inverted. Adjust the gain and compensation of one channel as required to approach a straight line trace. Perform the following steps to obtain the balanced interface signal:

(a) Set the controls on the scope as follows:

- (1) Mode switch to ALG ADD.
- (2) Pull the INVERT switch.
- (3) VOLTS/DIV switch to .02.
- (4) TRIGGERING source switch to EXT.
- (5) TRIGGERING coupling switch to AC.
- (6) TRIGGERING LEVEL switch to AUTO.
- (7) TIME/DIV switch to 1 μ SEC.
- (8) Pull the X10 MAG switch.

(b) Connect both probes to the same signal (leads A and B) and adjust the GAIN controls to get a straight line.

Note: Whenever the scope probes are connected to a signal, connect the probe ground leads to a common ground, such as the metal chassis.

- (c) Place both AC-GND-DC switches to GND and set trace on scope on the center line.
- (d) Place both AC-GND-DC switches to DC and connect a lead between the TRIG IN jack on the scope to TP9 on CP AR510 in the data unit.
- (e) To obtain the **SCT signal** (Fig. 14), connect INPUT 1 probe to test point Y on TB2 (located on the rear of the 33A1 DU) and connect INPUT 2 probe to test point **a** on TB2.
- (f) Adjust the VARIABLE control on the TIME/DIV switch to get one cycle of the SCT signal in five vertical divisions (graticule lines).
- (g) Adjust the horizontal POSITION control until the positive-going transition of the SCT

signal passes through zero, where the center vertical graticule line intersects the center horizontal graticule line. The amplitude of the signal should be within the limits shown in Fig. 14, and the zero crossing (where the signal crosses the center horizontal graticule line) of the negative-going transition of the signal should be within the limits given.

(h) To obtain the **SCTE signal**, set up the scope according to steps (a) through (d) and connect INPUT 1 probe to test point U on TB2 and connect INPUT 2 probe to test point W on TB2.

(i) Adjust the VARIABLE control on the TIME/DIV switch to get one cycle of the signal in five vertical graticule lines.

(j) Adjust the horizontal POSITION control until the positive-going transition of the signal passes through zero (Fig. 15). The amplitude of the signal should be within the limits given and the zero crossing of the negative-going transition of the signal should be within limits as shown.

(k) To obtain the **SD signal**, set up the scope according to steps (i) through (j) and connect INPUT 1 probe to test point P and connect INPUT 2 probe to test point S on TB2.

(l) The waveform should look like Fig. 16 with the signal amplitude and zero crossings within the indicated limits.

(m) To obtain the **SCR signal**, set up the scope according to steps (a) through (c) and place both AC-GND-DC switches to DC. Connect a lead from the TRIG IN jack on the scope to TP13 on CP AR509 in the data set.

(n) Connect the INPUT 1 probe to test point V on TB2 and connect the INPUT 2 probe to test point X on TB2.

(o) Adjust the VARIABLE control on the TIME/DIV switch to get one cycle of the signal in five vertical graticule lines.

(p) Adjust the horizontal POSITION control until the positive-going transition of the signal passes through zero. This signal should be the same as in Fig. 14.

- (q) The amplitude and the zero crossing of the negative-going transition of the signal should be within the limits given in Fig. 14.
- (r) To obtain the *RD signal*, set up the scope according to steps (m) through (o).
- (s) Connect the INPUT 1 probe to test point R on TB2 and connect the INPUT 2 probe to test point T on TB2.
- (t) The waveform should look like Fig. 17 with the signal amplitude and zero crossings within the indicated limits.

G. Transmit Bit Rate Converter—CP AR510

3.82 A simplified functional block diagram is shown in Fig. 18 and this CP converts the 1.344-Mbps customer data signal to a 1.544-Mbps data signal by adding framing and stuffing bits. The framing bit (every 193rd bit) provides the standard framing signal of a D1 channel bank and is also used in the startup of the system synchronization. The stuffing bit is a logic 1 every eighth bit within a frame to assure a signal that will keep the T1 repeaters in synchronization. This CP consists of a main board and two circuit modules (CM). The main board consists of counters A and B, an elastic store, and logic circuitry. CM1 contains a 1.344-MHz voltage-controlled crystal oscillator, phase comparator, and low-pass filter. CM1 locks onto a "staggered" 1.344-MHz signal from the generator to produce a smooth 1.344-MHz signal on TSO which is returned via customer SCTE leads. CM2 consists of the framing/stuffing generator and logic circuits. The framing generator produces framing and stuffing bits and a "staggered" 1.344-MHz signal which is equivalent to the 1.544-MHz signal less the transitions during the framing and stuffing bits.

3.83 The SCTI clock signal is the inverted form of the SCTE signal. This smooth 1.344-MHz clock is divided by four and is used to write the data bits into the elastic store. SCTI is also divided by eight and provides one input to the phase comparator.

3.84 The HSD lead is the output of the elastic store at 1.544 Mbps. The output signal is read out of the elastic store by a staggered 1.344-Mbps signal which is equivalent to a 1.544-Mbps signal with the framing and stuffing pulses inserted.

3.85 The SDB and SDS leads carry the input data signal, but the SDB lead is blocked or clamped when the scrambler is used, thus the input signal is sent over the SDS lead.

3.86 The HTC, TFS, and XG2 signals are used by the generator to produce a framing bit every 193 cycles of the input clock on HTC. The framing bit itself alternates between a logic 1 and 0 which facilitates finding the framing bit in the composite bit stream. In addition, the generator produces a stuffing bit every eight cycles of the input clock on HTC. The TFS lead will provide the 1.544-MHz clock signal when the data unit is in remote test 2. The XG2 signal controls the framing bit signal by allowing framing to be sent whenever XG2 is logic 0 (ON). Framing will stop being transmitted whenever the signal is at a logic 1 (OFF).

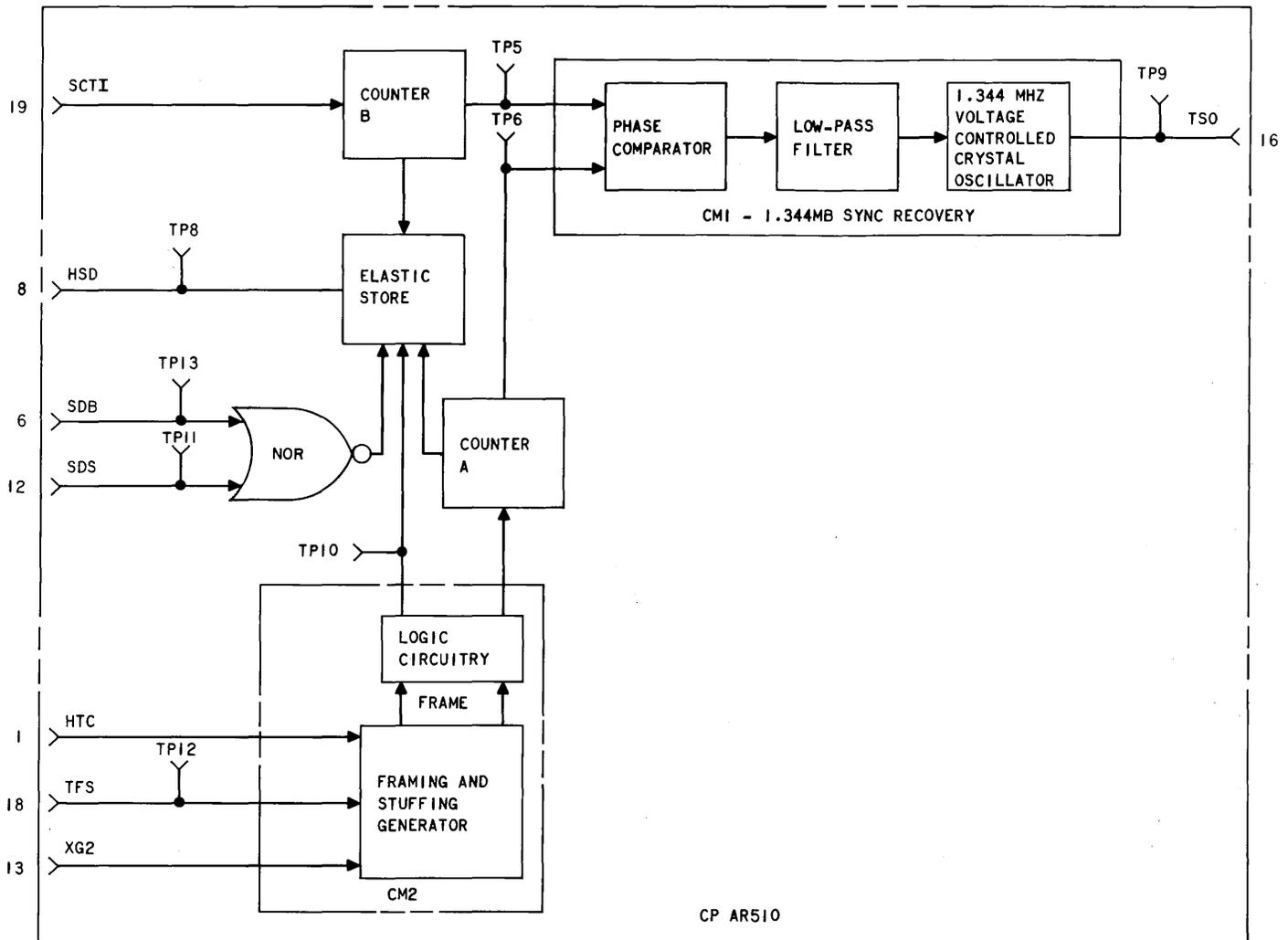
3.87 Counter A also receives the staggered 1.344-Mbps signal and sends one of its outputs to the elastic store and the other output to the phase comparator. The two input signals (a staggered 1.344-MHz and a smooth 1.344-MHz) to the phase comparator are compared to reduce the phase jitter and then used to either speed up or slow down the VCXO after passing through the low-pass filter. The smooth 1.344-MHz oscillator output is sent over the TSO lead to the SCT balanced cable driver which is returned via customer leads SCTE and appears on lead SCTI.

H. Transmitting 1.544-Mbps Bipolar Line Interface—CP AR511

3.88 A simplified functional block diagram is shown in Fig. 19. This CP converts the incoming 1.544-Mbps digital data signal into a 1.544-Mbps bipolar data signal. The CP includes terminators, 1.544-MHz crystal oscillator, regenerator and binary-to-bipolar converter circuitry, relay RT2C, and a voltage regulator.

3.89 The EIA cable terminator receives an ON or an OFF signal on lead LT and sends the respective indication out on lead LTA to indicate if the data set is in local test or not.

3.90 The balanced cable terminator is used when an external 1.544-MHz clock signal is used instead of the local 1.544-MHz clock signal. The input signal is received on the Transmit High



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Fig. 18—Transmit Bit Rate Converter—Functional Block Diagram CP AR510

Frequency Clock (THFC) leads A and B. Option X must be installed and option Z must be removed.

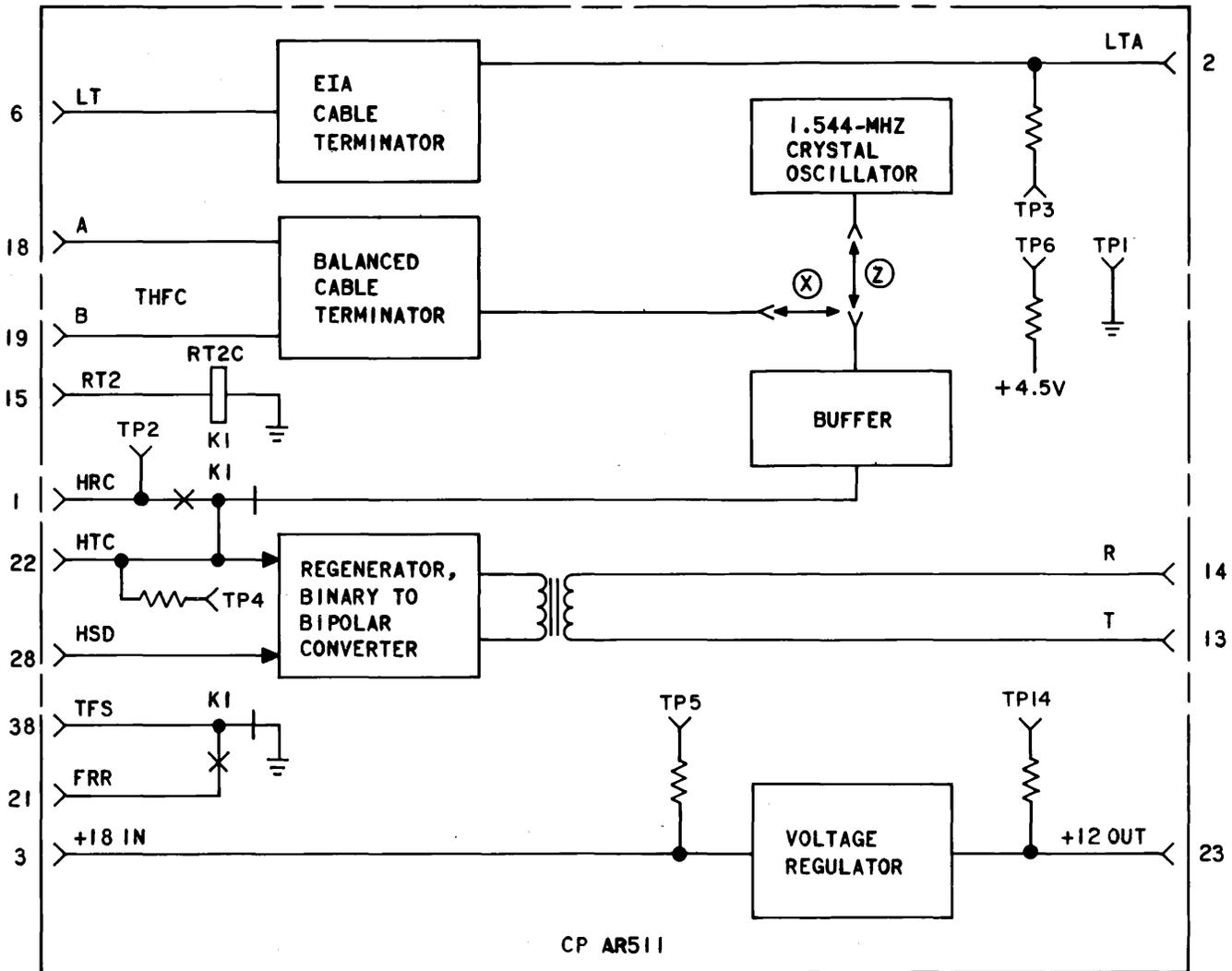
3.91 To put the data unit into remote test 2, an ON signal is supplied on lead RT2 which operates relay RT2C, as well as the RT2A and RT2B relays on CP AR509. When the relay is energized, the recovered 1.544-MHz clock signal on lead HRC is used instead of an external clock signal or the normally used clock signal from the 1.544-MHz crystal oscillator. Also, the ground signal is removed on lead TFS and the framing pulse signal on FRR is sent out on TFS. When the relay is not energized, the normally used clock signal is sent to the regenerator and out on lead HTC. The clock signal is used in the regenerator to retime

the data signal on HSD, so that the pulses are only half the width of the original data pulses. Then the data signal is converted into a bipolar signal (see waveform 5 on Fig. 3) which is transformer-coupled to leads R and T.

3.92 The voltage regulator is a 12V series feedback regulator which has an output between 10.8 and 13.2 volts. Several circuit packs require this value of voltage for proper operation.

EQUALIZER—EQ1

3.93 The 944A equalizer is required to compensate for different cable lengths between the data unit and a T1 line terminating unit. Table C



NOTE:

OPTION X IS FOR EXTERNAL CLOCK.
 OPTION Z IS FOR INTERNAL CLOCK.

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Fig. 19—Transmitting 1.544-MBPS Bipolar Line Interface—Functional Block Diagram CP AR511

shows which section to use for different lengths. EQ1 consists of three sections with four screws each. If a screw is down, a connection is made; however, only one section is used at a time.

4. OPTIONS

4.01 Certain options are required depending on the type of service and station arrangement. Other options are determined by the customer's preference.

TABLE C

944A EQUALIZER

CABLE LENGTH IN FEET	SECTION	TIGHTEN SCREW TERMINALS ON EQ1
0 - 150	C	1C, 2C, 3C, 4C
150 - 450	B	1B, 2B, 3B, 4B
450 - 750	A	1A, 2A, 3A, 4A

4.02 The options shown in Fig. 5 provide a permanent ON condition on the appropriate option lead by supplying ground. Options available for the 33A1 Data Unit are described as follows:

Note: The terminal board connection for a particular option immediately follows the option designation.

- **Option F**—Power for test set (TB1: 54-55)—This option supplies approximately +18 volts on customer connector to power a test set should this ever be necessary. Not factory furnished.
- **Option G**—Circuit ground connected to frame ground under spade lug screw at lower right-hand corner on rear of data unit—This option is normally used unless ground noise problems force a floating circuit ground for satisfactory operation. Factory furnished.
- **Option N**—One way, transmit only (TB1: 33-34)—This option is used to permit transmit-only operation without requiring reception of framing signal (RDF ON signal). Not factory furnished.
- **Option Q**—Permanent data terminal ready (TB1: 43-44)—This option is used to supply a permanent data terminal ready indication to the data unit in lieu of a customer-supplied data terminal ready signal. Not factory furnished.
- **Option R**—Permanent request to send (TB1: 32-33)—This option is used to supply a permanent request-to-send indication to the data unit in lieu of a customer-supplied request-to-send signal. Not factory furnished.
- **Option S**—Permanent line status (TB1: 42-43)—This option is normally used unless voiceband DATA-PHONE type operation is desired, in which case the option is omitted and the LS lead from a Data Auxiliary-Set 804-type is used to turn on the data set; therefore, simultaneous wideband data and voice operation is not possible. Factory furnished.

- **Option T**—2-Second Billing Delay (TB1: 29-30)—This option is a 2-second billing delay to prevent transmission or reception of data until after billing has been initiated. Not factory furnished.
- **Option V**—No 32A Data Unit (TB1: 26-27, 27-28)—This option is required when a 32A-type Data Unit is not provided. Not factory furnished.
- **Option W**—No DAS 804 control, simulated answer (TB1: 30-31)—This option is required for operation when the DAS 804-type is not used. Factory furnished.
- **Option X**—External clock (on CP AR511)—This option allows an externally provided 1.544-MHz signal on the THFC leads to be used as the master clock in special applications. Not factory furnished.
- **Option Y**—No DAS 804 control, permanent off-hook (TB1: 8-9)—This option is required to permanently provide the equivalent of the ACUTI off-hook indication when the DAS 804-type is not used. Factory furnished.
- **Option Z**—Internal clock (on CP AR511)—This option is normally used to supply the locally generated clock signal from the 1.544-MHz oscillator on CP AR511. Factory furnished.

5. REFERENCES

5.01 The circuit descriptions (CDs) and the schematic drawings (SDs) for the 33A1 Data Unit and associated apparatus are as follows:

- CD- and SD-1D187-01—Data Set 306-Type
- CD- and SD-1D196-01—33-Type Data Unit
- CD- and SD-1D218-01—32A-Type Data Unit
- CD- and SD-1D237-01—Wideband Data Station Using Data Set 306-Type, Application Schematic.

SECTION 590-100-123

5.02 Bell System Practices used as information are as follows:

SECTION	TITLE
590-100-122	32A-Type Data Unit, Description and Operation
593-801-100	Wideband Data Station Using Data Set 306, Point-to-Point,

SECTION

TITLE

	Limited Distance, Description and Operation
598-030-100	Data Auxiliary Set 804A-Type, Description and Operation.