

**DATA SET 205C-TYPE
TRANSMITTER-RECEIVER
THEORY OF OPERATION
AND
SUPPLEMENTARY INFORMATION**

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1. GENERAL

1.01 This section contains theory of operation together with tests that require the use of complex test equipment (oscilloscopes, electronic counters, etc). The tests are designed to assist in localizing a malfunction which may not have been determined in testing with the more common test sets. Testing of individual circuit packs is included in the appendix. The complete detailed circuit descriptions and schematic drawings are provided in CD- and SD-1D087-01. Circuit sketches of the individual circuit packs are provided by SD-1D060 (sheets J1 through J12).

1.02 This section is being reissued to provide circuit pack identification by apparatus coding (two digits prefixed by "AR"). Previous

documentation for the data set identified circuit packs by the last three digits of the equipment code (six digits prefixed by "A").

1.03 The coding used in this practice when circuit packs are referenced contains the present "AR" coding, the last three digits of equipment coding in parentheses for early manufactured data set reference, and the circuit pack location which is separated by a slant line. The reference AR75(181)/019 should be interpreted the circuit pack with apparatus code AR75, equipment coded A835181, and in data set slot location 019.

1.04 A separate code is used to establish the data set mnemonic symbols to the EIA Standard RS-232-B symbols and is separated by a slant line. The send data interface lead is mnemonically abbreviated SD and will meet the RS-232-B requirements of circuit BA. The coding SD/BA symbolizes both abbreviations.

1.05 The Data Set 205C-type replaces Data Set 205A which is rated Manufacture Discontinued. A 205C can replace a 205A directly if CUSTOMER B interface pin 11 is connected to either a negative voltage or ground.

1.06 Data Set 205C-type uses synchronous 4-phase modulation techniques for transmitting serial binary data at either 2400 or 1200 bits per second (bps). Transmission is over 2-wire or 4-wire voice-frequency circuits using an 1800-Hz suppressed carrier. The line signal spectrum is essentially confined to a band extending from 600 to 3000 Hz.

1.07 Data set clock signals being supplied to the customer business machine are synchronous with transmit and receive data. These

clocks are selected by the customer and, through an external connection, are at the data rate or twice the data rate.

1.08 Two Data Set 205C-type units can be interconnected to become a 4-wire regenerative repeater. Timing and data signals are exchanged between the two sets through their respective CUSTOMER B connector.

1.09 Data Set 205C2 can be made compatible with Data Set 207-type through interconnection with Data Auxiliary Set (DAS) 811D1. The DAS 811D1 provides separate interface connections for (1) customer-furnished crypto ancillary equipment, and (2) BLACK telephone and control equipment. This compatibility can exist only when Data Set 205C2 is in a terminal configuration and data transmission and reception is at 2400 bps. Remote testing of Data Set 205C2 requires bypassing DAS 811D1. Further information regarding DAS 811D1 is provided in Sections 598-063-ZZZ.

1.10 The data set is designed to operate in an ambient room temperature range of +50 to +120°F with relative humidity up to 95 per-

cent. The ac input requirements are 117 volts (± 10 percent) at 60 (± 0.8) Hz.

1.11 The data set can be mounted in a 23-inch relay rack. Its overall dimensions are 22.93 inches wide by 17.97 inches high by 8.32 inches deep.

2. SYSTEM CONFIGURATION AND OPERATION

2.01 Data Set 205C-type can be used on either 2-wire or 4-wire point-to-point telephone line configurations as shown in Fig. 1. More elaborate system configurations can be developed from these basic types.

A. Operation on 2-Wire Facilities

2.02 For 2-wire operation, the cord from the 4A1 Data Unit is connected to the 2-WIRE receptacle on the data set. The 2-wire telephone facility is terminated at the TEL LINE connector on the 4A1 Data Unit.

2.03 When operating in the 2-wire mode, local copy is provided on the receive data circuit whenever the data set is transmitting. Neither

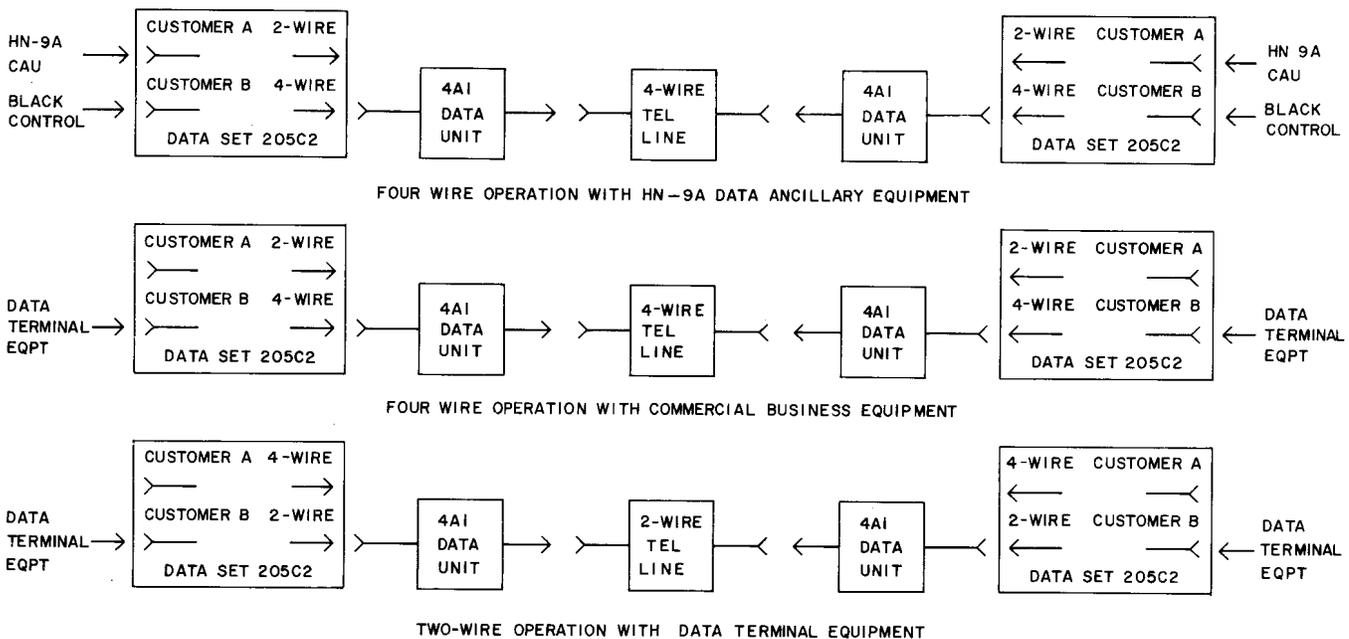


Fig. 1 — System Configurations

the remote test nor continuous-carrier functions can be provided. Any strap between terminals 1 and 2 on the transmit-receive switch circuit pack AR95(181)/019 must be removed. The interface lead confirm (CON, pin 18) must be grounded or connected to a negative voltage potential to provide an OFF condition. When the above requirements are provided, the data set carrier is controlled by the request-to-send circuitry.

B. Operation on 4-Wire Facilities

2.04 For 4-wire operation, the cord from the 4A1 Data Unit is connected to the 4-WIRE receptacle on the data set. The 4-wire telephone facility is terminated at the TEL LINE connector on the 4A1 Data Unit.

2.05 When operating in the 4-wire mode, the data set can provide simultaneous transmission and reception. Other features provided through this type facility include remote testing from a 904E Data Test Center, selection of either continuous carrier or carrier controlled by the request-to-send function, and control of the request-to-send/clear-to-send time interval by using the confirm circuit.

3. SUMMARY OF CONNECTORS AND OPTION STRAPPING

3.01 The following summary describes both external and internal connections required for data set operation. Various installation strapping is included for reference convenience. Detailed requirements are included in later descriptions.

Interface Connections of Data Set 205C-Type

Note: Lightning protection is *not* provided on any interface circuit. Cables carrying these circuits may not be used out-of-doors.

3.02 *CUSTOMER A Jack (J62)*: This receptacle is a 15-pin KS-19087-L1 connector. When used, the customer must supply the connecting cable terminated with a mating connector, Cinch (or Cannon) DA-19603-403, and locking hood, Cinch (or Cannon) DA-51225-1, for interconnection.

3.03 The CUSTOMER A connector provides an interchange for data and clock circuits, serial clock rate (SCX2) circuit, the data set ready (DSR/CC and DSRX2) circuit, frame ground (FG/AA), and signal ground (SG/AB). The DSR/CC and DSRX2 circuits are strapped on the mating customer-supplied connector.

3.04 CUSTOMER A connector is provided specifically for use with government-furnished HN-9A Data Ancillary equipment. The data and clock circuits are capable of operation over twisted-pair cables several thousand feet long provided that resistance and ground potential requirements are met.

3.05 *CUSTOMER B Jack (J61)*: This receptacle is a 25-pin KS-19087-L2 connector. The customer must supply a connecting cable terminated with a mating connector, Cinch (or Cannon) DB-19604-432, and locking hood, Cinch (or Cannon) DB-51226-1, for interconnection.

3.06 The CUSTOMER B connector provides interchange with the customer business machine and data set control circuits, data and clock circuits, the clock rate selection circuit, frame ground, and signal ground. The signals interfaced through this connector can be used with cable lengths up to 50 feet. The CUSTOMER B connector is also used for testing purposes.

3.07 *2-WIRE Plug (P1)*: This receptacle mates with the connector terminating the 4A1 Data Unit cable. The 2-WIRE plug provides interface for the single transmit and/or receive pair used in 2-wire operation.

3.08 *4-WIRE Plug (P2)*: This receptacle mates with the connector that terminates the 4A1 Data Unit cable. The 4-WIRE plug provides interface for the transmit and receive pairs used in 4-wire operation.

3.09 *TEL LINE Connector*: The TEL LINE connector interfaces the 2-wire or 4-wire telephone facility with the 4A1 Data Unit. This connector is a 25-pin KS-19088-L2 and requires a 25-pin KS-19087-L2 mating connector and KS-19196-L2 locking hood which is supplied by the installer.

3.10 *AC INPUT Jack (J1)*: The AC INPUT connector receives the miniature 3-wire twist-lock female plug of a KS-14532-L16 ac

power cord. The opposite end of the power cord is terminated with a conventional parallel blade with ground lug male plug. The power cord carries the required 117 volts (± 10 percent) 60 (± 0.8) Hz from the power source to the AC INPUT.

3.11 DC OUTPUT Jack (J2): The DC OUTPUT jack mates with a 6-pin KS-8585-L16 connector and a 4-conductor power cord to provide the data set with +18.0 (± 1.0) Vdc (pin 3), -18.0 (± 1.0) Vdc (pin 5), a common ground (pin 4), and frame ground (pin 6). The remaining pins are unused. The opposite end of the power cord should be provided with a 6-pin KS-8586-L50 connector to mate with the data set.

Data Set Internal Connections and Strapping

3.12 Ground Straps E1 and E2: A strap is provided between terminals E1 and E2 to connect signal ground to frame ground. This strap should remain intact for all data set testing and normal operation. In some applications, the customer may require a common grounding point in the equipment. For these applications, the strap between E1 and E2 should be cut and proper grounding provided for the data set through leads available on the CUSTOMER B and/or CUSTOMER A interface connectors.

3.13 Transmitter Timing: Internal transmitter timing may be used by providing a strap between terminals 3 and 4 on the transmit-receive switch circuit pack AR95(181)/019. This strap grounds the external clock input to prevent false timing corrections due to noise. External timing can be provided by removing the strap from terminals 3 and 4. The customer can provide a timing source through the CUSTOMER B interface lead SCTE/DA on pin 24. This strap must be removed for regenerative repeater operation.

3.14 2-Wire Operation: When operating over 2-wire facilities, the carrier must be controlled by request-to-send (RS/CA) being ON for at least 640 milliseconds before data transmission. This requires that the strap between terminals 1 and 2 on AR95(181)/019 be removed. In this mode, the customer business machine must provide a minimum number of data crossings per second on the send data (SD/BA) interface lead to achieve far-end receiver synchronization when clear-to-send (CS/CB) is ON.

3.15 Transmitter Output Power: The transmitter output power is set by a strap connection on the transmitter output circuit pack AR90(182)/044. The output power corresponds to that measured with a random data signal and with the transmitting line pair terminated in 600 ohms for 4-wire operation or 900 ohms for 2-wire operation. The transmitter output power is adjustable by strapping as listed in Table A.

TABLE A

TRANSMITTER OUTPUT POWER STRAPPING

OUTPUT LEVEL	CONNECT TERMINALS
0 dBm	1 and 4
-3 dBm	1 and 3
-6 dBm	1 and 2
-9 dBm	None

3.16 Receiver Input Sensitivity: The input to the receiver is an automatic gain control (AGC) circuit with a 30 dB dynamic range and an input sensitivity of -39 (± 1.0) dBm. If the received signal is sufficiently greater than the basic receiver sensitivity, loss pads of 5, 10, and 15 dB may be connected into the signal path to reduce the sensitivity of the receiver to noise or speech interference. The loss pads are set by external strapping of terminals on automatic gain control 1 circuit pack AR88(178)/017. The resulting characteristics are listed in Table B.

TABLE B

RECEIVER LOSS PAD STRAPPING

PAD LOSS (dB)	STRAP TERMINALS	AGC SENSITIVITY (dBm)	NOMINAL RECEIVED POWER (dBm)
0	1 and 5	-38 to -10	-30 to -38
5	2 and 5	-33 to -5	-25 to -30
10	3 and 5	-28 to 0	-20 to -25
15	4 and 5	-23 to +5	+5 to -20

4. DATA SET TRANSMITTER

4.01 Incoming serial data bits are delivered to the transmitter through the send data (SD/BA) interface lead. The data transitions are synchronous with the positive-going transitions of the transmitter clock (SCT/DB). These are examined in pairs (dibits) and are used to control the 4-phase modulation of the carrier.

CARRIER CONTROL**A. Four-Wire Operation*****Continuous Carrier***

4.02 In 4-wire operation, carrier may be placed continuously ON by strapping terminals 1 and 2 on circuit pack AR75(181)/019. When operating in the continuous carrier mode, interface lead confirm (CON) is placed OFF by the customer. A continuous clear-to-send (CS/CB) ON signal is put on the line by the data set and no idle code is generated.

4.03 The continuous carrier mode provides for customer operation without waiting for the CS/CB ON signal before each transmission. For this service, the customer business machine must provide a minimum number of crossings per second of send data (SD/BA) for far-end receiver synchronization whether transmitting data or not. Required data crossing rates are provided in Part 8.

B. Two-Wire Operation***Carrier Controlled by Request-to-Send (RS/CA)***

4.04 The carrier may be turned on and off with the request-to-send (RS/CA) interface signal. In this mode, the strap between terminals 1 and 2 on circuit pack AR95(181)/019 must be removed.

4.05 A 1000 quad-bit synchronizing (idle) code is now transmitted for a time not less than 638.33 msec whenever RS/CA is placed ON. The idle code time interval may be controlled by the confirm (CON) circuit. After the idle code transmission, a clear-to-send (CS/CB) ON signal is provided to the customer business machine. This signal indicates that the far-end receiver has had sufficient time to synchronize and data may now be transmitted.

4.06 The customer business machine must provide a minimum number of data crossings per second on the send data (SD/BA) lead, for receiver synchronization, while CS/CB is ON. The line spectrum for the transmission of repeated dibits is shown in Fig. 2.

TRANSMITTER TIMING

Note: When the data set clock signals have been selected to be at the data rate, transmitter timing may be derived from the internal crystal oscillator, a customer-supplied external source (2400-Hz square wave or send data [SD/BA]), or by a clock signal from another data set. External timing is not provided when using double-speed clock signals. When two data sets are used as a regenerator, clock signals are exchanged between the two data sets.

A. Data Set-Supplied

4.07 Internal timing may be used with both normal- and double-speed clocks. When internal timing is used, a strap must be connected between terminals 3 and 4 on circuit pack AR95(181)/019. This strap grounds the external clock (SCTE/DA) input to prevent false timing corrections due to noise.

B. Customer-Supplied

4.08 External timing may be used only with normal-speed clocks. This mode requires that terminals 3 and 4 on circuit pack AR95(181)/019 be open. A strap between these terminals must be removed. A square-wave clock or send data (SD/BA) is applied to the external timing (SCTE/DA) input and is used to generate discrete phase corrections of the transmitter clock.

C. Regenerator Timing

4.09 Two data sets are required to make a regenerative repeater arrangement. During this mode of operation, each data set transmitter receives external timing from the receiver of the opposite data set. A square-wave clock signal from the serial clock receive (SCR/DD) output of each receiver is applied to the serial clock transmit external (SCTE/DA) lead of the opposite transmitter. This configuration requires the removal of any strap between terminals 3 and 4 on circuit pack AR95(181)/019.

5. DATA SET RECEIVER

5.01 The data set receiver demodulates the received line signal to deliver serial received data (RD/BB) and a synchronous clock, serial

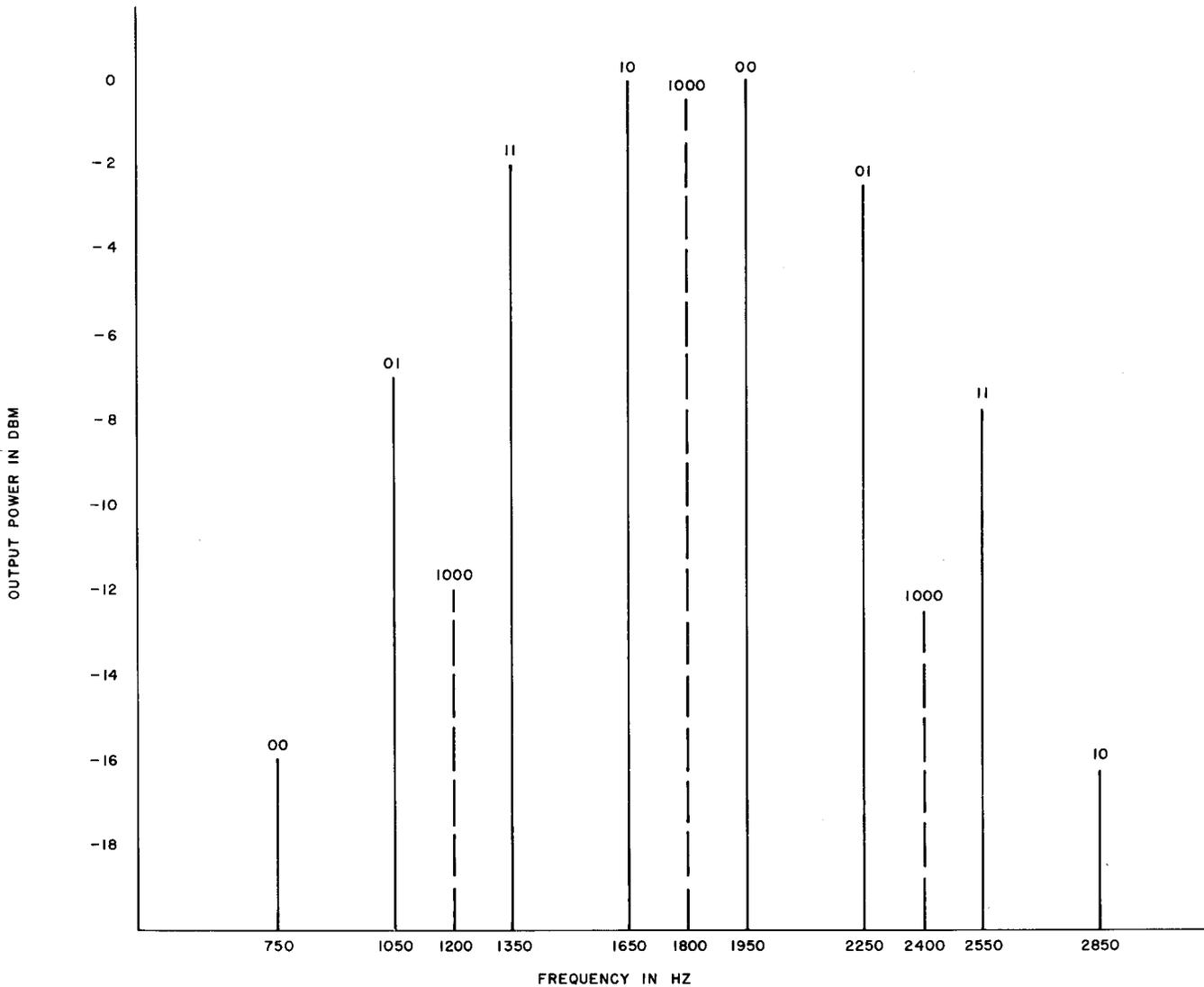


Fig. 2 — Output Spectrum for Repeated Dibit Codes at 2400 bps

clock receive (SCR/DD), to the customer business machine or another data set for regeneration.

5.02 The receiver input is an AGC circuit with a 30-dB dynamic range and a sensitivity of $-39 (\pm 1.0)$ dBm. If the received signal is sufficiently greater than the basic receiver sensitivity, loss pads of 5, 10, or 15 dB may be strapped into the circuit to reduce the receiver sensitivity to noise or speech interference.

6. DATA, CLOCK, AND CONTROL INTERFACE SIGNALS

6.01 The data set interface consists of three groupings of leads: (1) those that interface with the customer business machine(s),

(2) the telephone facility and transfer arrangement, and (3) the data set ac power. The ac power connection is covered in 3.10 and will not be described in this part. The interchange with the customer business machine(s) include the data, clock, and control signals.

6.02 Electrical connections between the data set and the customer business machine(s) (except for ac power and frame ground) are made through the CUSTOMER B and CUSTOMER A interface connectors. The pin assignments for all data set interface leads are given in Table C and illustrated in Fig. 3.

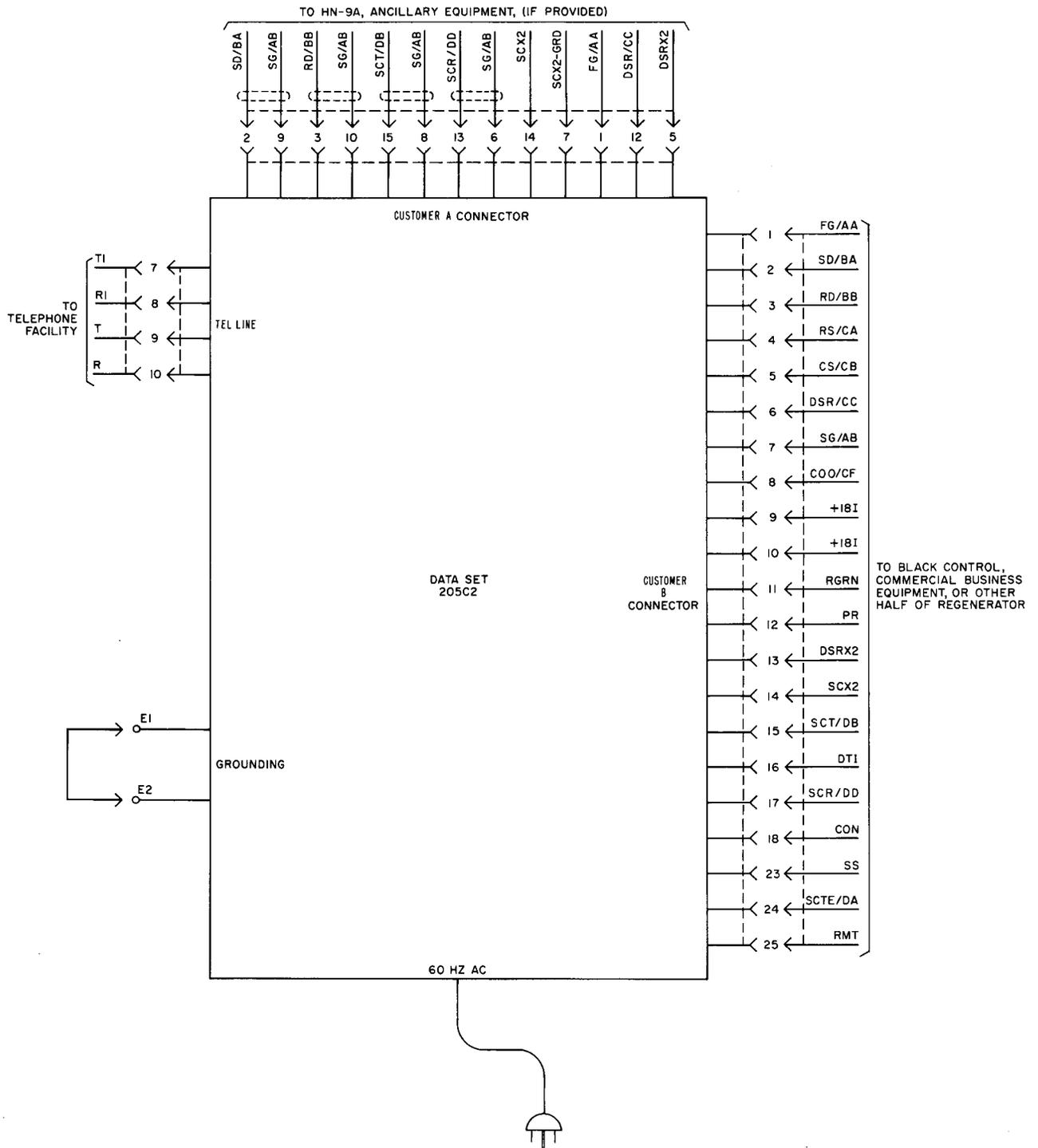


Fig. 3 — Interface Connections

TABLE C
INTERFACE CONNECTOR PIN ASSIGNMENT

CUSTOMER B (J61)				
PIN NO.	CIRCUIT FUNCTION	MNEMONIC SYMBOL	EIA SYMBOL	SIGNAL
1	Frame Ground	FG	AA	
2	Send Data	SD	BA	
3	Receive Data	RD	BB	
4	Request-to-Send	RS	CA	
5	Clear-to-Send	CS	CB	
6	Data Set Ready	DSR	CC	
7	Signal Ground	SG	AB	
8	Carrier On-Off	COO	CF	
9	+18 Volts dc	+18 I		
10	-18 Volts dc	-18 I		
11	Regeneration	RGRN		
12	Prepare Receiver	PR		
13	Data Set Ready — Double Speed	DSRX2		
14	Serial Clock — Double Speed	SCX2		
15	Serial Clock Transmit	SCT	DB	
16	Dibit Clock Transmit	DT1		
17	Serial Clock Receive	SCR	DD	
18	Confirm	CON		
23	Speed Select	SS		
24	Serial Clock Transmit External	SCTE	DA	
25	Remote Test	RMT		
CUSTOMER A (J62)				
1	Frame Ground	FG	AA	
2	Send Data	SD	BA	
3	Receive Data	RD	BB	
5	Data Set Ready — Double Speed	DSRX2		
6	Signal Ground	SG	AB	Shield Ground for SCR
7	Serial Clock — Double Speed — Ground	SCX2-GRD		
8	Signal Ground	SG	AB	Shield Ground for SCT
9	Signal Ground	SG	AB	Shield Ground for SD
10	Signal Ground	SG	AB	Shield Ground for RD
12	Data Set Ready	DSR	CC	
13	Serial Clock Receive	SCR	DD	
14	Serial Clock — Double Speed	SCX2		
15	Serial Clock Transmit	SCT	DB	

Note: Unnumbered pins are not used.

6.03 The following interface signal definitions are as specified in EIA Standard RS-232-B:

Voltage Level	Positive	Negative
Binary Sense	1	0
Data Sense	MARK	SPACE
Signal Sense	Present	Absent
Control Sense	ON	OFF

6.04 *Electrical Characteristics of Drivers and Terminators:* With one exception, the electrical characteristics of the interface circuits available on the CUSTOMER B connector meet the EIA RS-232-B specifications. Interface circuits SD/BA, RD/BB, SCT/DB, and SCR/DD also meet the intent of Military Standard (MIL. STD) 188B which is more stringent regarding signal rise time. The one exception is the data carrier detector (COO/CF) circuit which is a line energy detector that operates on received power, regardless of its nature, and not on data carrier exclusively.

A. Military Standard 188B Terminator

6.05 This terminator is used for the send data (SD/BA) circuit. The terminator can assume one of two states. A voltage greater than +0.5V will cause it to assume one state and a voltage of less than -0.5V will cause it to assume the other. The two levels are balanced (with respect to 0 volts) to within 10 percent of each other. The terminator has an input resistance in excess of 5000 ohms and a shunt capacitance of less than 1000 pf.

B. Military Standard 188B Driver

6.06 This driver is used for the following circuits:

- Receive data (RD/BB)
- Serial clock transmit (SCT/DB)
- Serial clock receive (SCR/DD)

The driver delivers an open-circuit output voltage of 6.1 volts (± 5 percent), positive and negative, through less than 100 ohms source impedance. The rise and fall times of the output wave shape is approximately 11 microseconds, that is, 5.5 percent of the half-period of a 2400-Hz square wave.

C. EIA RS-232-B Terminator

6.07 This terminator is used for the following circuits:

- Request-to-send (RS/CA)
- Regenerate (RGRN)
- Confirm (CON)
- Speed select (SS)
- Remote test (RMT)
- Serial clock transmit external (SCTE/DA)

The EIA terminators recognize a minimum of +3.0 volts to a maximum of +25 Vdc as an ON signal and a minimum of -3.0 volts to a maximum of -25 Vdc as an OFF signal without regard to rise or fall time of transitions. Shunt capacitance to signal ground of the customer equipment and cabling, measured at the interface, shall not exceed 2500 pf. Input resistance to the terminators is approximately 3000 ohms, except for SCTE/DA which is 30,000 ohms. The reasons for this are:

- (a) A high input resistance on SCTE/DA allows up to ten externally timed data sets to be driven from the SCT/DB output of one internally timed data set.
- (b) When using send data (SD/BA) as the external timing source, a high SCTE/DA input resistance prevents loading of the Mil. Std 188B terminator used for SD/BA.

D. EIA RS-232-B Driver

6.08 This driver is used for the following circuits:

- Clear-to-send (CS/CB)
- Data set ready (DSR/CC)
- Carrier on-off (COO)
- Prepare receiver (PR)
- Serial clock — double speed (SCX2)
- Data set ready — double speed (DSRX2)

The driver will deliver a +6.8 (± 1.2) volt ON signal or a -6.8 (± 1.2) volt OFF signal to a 3000-ohm or greater resistive load.

DESCRIPTION OF INTERFACE SIGNALS

6.09 The descriptions contained in the remainder of this part will characterize the general operating conditions of the data set interface signals.

A. Request-to-Send (RS/CA) — Terminator**Continuous-Carrier Operation (4-Wire Mode Only)**

6.10 When the data set has been internally strapped for continuous carrier, the RS/CA circuit is disabled.

Carrier Controlled by RS/CA (4-Wire or 2-Wire Mode)

6.11 When the data set is not internally strapped for continuous carrier, the data set carrier is switched ON and OFF with RS/CA.

(a) **Four-Wire Operation:** In this mode, an RS/CA ON signal enables the data set carrier and initiates the RS/CA-CS/CB time period during which the synchronizing idle code is transmitted. At the end of this time period, the data set provides a CS/CB ON signal to the business machine indicating that data may be transmitted. The RS/CA interface lead must be held ON for the full duration of the message and for the entire interval of the last bit to be transmitted.

(b) **Two-Wire Operation:** In this mode, placing RS/CA ON will connect the transmitter to the telephone line, enable the data set carrier, and initiate the RS/CA-CS/CB time period during which the synchronizing idle code is transmitted. At the same time, the data set receiver is connected to provide local copy through the receive data (RD/BB) circuit. The RS/CA interface lead must be held ON for the full duration of the message and for the entire interval of the last bit to be transmitted. When RS/CA changes to OFF, the data set carrier is inhibited, the transmitter is disconnected from the line, and the receiver circuits are connected to the telephone line.

B. Clear-to-Send (CS/CB) — Driver

6.12 An ON indication at the CS/CB interface lead provides an indication to the business machine that the transmission of the synchronizing pattern has ended and the data set will accept and transmit data. The CS/CB lead is switched OFF with the RS/CA lead changing to OFF.

6.13 The RS/CA-CS/CB time period depends on the state of the confirm (CON) circuit described as follows:

(a) **Confirm OFF:** In this condition, an RS/CA ON signal will initiate a 640 $\begin{pmatrix} +0.00 \\ -1.67 \end{pmatrix}$

msec timing period that ends with enabling CS/CB to provide an ON signal. This interval is adequate for a far-end receiver to acquire synchronization.

(b) **Confirm ON:** In this condition, the RS/CA circuit is prevented from initiating the 640

$\begin{pmatrix} +0.00 \\ -1.67 \end{pmatrix}$ msec timing period until the receiver has detected a synchronizing pattern from the far-end data set. This assures that a far-end receiver is connected to the telephone line.

C. Confirm (CON) — Terminator

6.14 The function of the confirm circuit has been described in 6.13. The confirm circuit is for use in the 4-wire mode only. When operating over 2-wire facilities, confirm must be placed OFF by the customer.

D. Data Carrier Detector (COO/CF) — Driver

6.15 When COO/CF is ON, an indication is provided to the business machine that the data set receiver is detecting telephone line power. Excessive line noise or speech, as well as carrier, can operate this circuit. When the COO/CF is OFF, the receive data (RD/BB) interface lead is held at the negative voltage level. The sensitivity of the COO/CF circuit is $-39 (\pm 1.0)$ dBm with random signal input.

E. Data Speed Select (SS) — Terminator

6.16 The bit-per-second rate of the data set is controlled by the SS lead. When SS is ON, the data set operates at 2400 bits per second. When SS is OFF, the data set operates at 1200 bits per second. The latter speed reduces the bandwidth of the line signal and gives greater probability of successful transmission over other facilities than those normally used.

6.17 When the regenerate (RGRN) interface is OFF, the SS controls the transmit and receive clocks (SCT/DB and SCR/DD) supplied to the connecting data equipment in accordance with the bit rate. These clocks can be either at the data rate or twice the data rate.

6.18 It is necessary that both the local and far-end data sets be conditioned for the same bit rate.

F. Data Set Ready (DSR/CC)— Driver

6.19 An ON condition of the DSR/CC lead indicates to the business machine that the data set is *not* in a test mode and operating voltages are provided. The DSR/CC is placed OFF when the data set is in a test mode or when operating power is removed.

6.20 The DSR/CC circuit is used only when data and clock signals are interfaced through the CUSTOMER B connector. When the CUSTOMER A connector is used for data and clock signals, the DSRX2 lead will be used in place of DSR/CC.

G. Data Set Ready X2 (DSRX2)— Driver

6.21 The DSRX2 circuit description is identical to that for DSR/CC, except DSR/CC passes through a strap provided by the customer in the plug connected to CUSTOMER A receptacle before appearing in CUSTOMER B connector as DSRX2. Therefore, if the plug to CUSTOMER A connector is removed, the DSR/CC signal cannot be delivered.

6.22 The DSRX2 interface lead is for use only when data and clock signals are being provided through the CUSTOMER A connector.

H. Remote Test (RMT)— Terminator

6.23 The RMT circuit permits a data set to be tested from a 904E Data Test Center when the data set is in the 4-wire mode. The data set is conditioned for remote testing by the customer upon request from the test center. When RMT is ON, the data set will:

- Disconnect all data and timing interface circuits.
- Disconnect all control interface circuits except RMT, DSR/CC (DSRX2), signal ground (SG), and dibit clock transmit (DTI).
- Provide a DSR/CC (DSRX2) OFF indication to the control interface.
- Condition the local data set for remote testing.

6.24 With the data set in the remote test mode, the data test center may check the following:

- The function of the CON interface lead
- The RS/CA-CS/CB time interval
- Data performance at 2400 and 1200 bps
- Local oscillator accuracy
- Effectiveness of the receiver synchronization recovery circuits.

6.25 When the customer restores the RMT lead to OFF, the data set is released from the remote test mode and all circuits are restored.

6.26 When operating the data set in a 2-wire mode, the remote test feature is not provided and the RMT interface lead will not accept any signal.

I. Serial Clock Timing External (SCTE/DA)— Terminator

Note: External timing may not be used when the data set clocks, SCT/DB and SCR/DD, are at twice the bit rate. If external timing is *not* used, an internal strap connection must be made between terminals 3 and 4 on circuit pack AR95(181)/019. When external timing *is* used, the strap must be removed.

6.27 The data set may be synchronized with an external source by using the SCTE/DA circuit. The input may be either a square wave at the bit rate or send data (SD/BA) itself. (To use SD/BA as an input to SCTE/DA, the customer must supply a strap between pins 2 and 24 on the CUSTOMER B connector.) In either case, the required minimum frequency accuracy of the external source is ± 0.01 percent.

6.28 The transmitter is initially synchronized with SCTE/DA by application of the square-wave source or a send data dotting code (alternate 0-1) for at least 40 msec before RS/CA switches ON. Once the 40-msec time period has elapsed and RS/CA is ON, it is necessary to ensure at least 13 positive transitions of SCTE/DA per second to keep the transmitter in synchronization.

6.29 The maximum synchronization holdover time depends upon the transmitter and receiver clock frequency tolerances. However, since the receiver clock frequency tolerance is fixed at ± 0.0005 percent, the holdover time will vary primarily with the transmitter clock frequency tolerance. The holdover time of 6.0 seconds for a transmitter timing tolerance of ± 0.0005 percent decreases linearly to 0.57 second for a tolerance of ± 0.01 percent.

J. Regeneration (RGRN) — Terminator

Note: The RGRN interface lead on pin 11 of the CUSTOMER B connector must be connected to a negative voltage (-3 to -25 volts) unless the data set is to be used as a regenerative repeater. If the data set is used as a regenerator, then both SS and RGRN interface leads must be connected to a positive voltage ($+3$ to $+25$ volts).

6.30 The RGRN circuit permits the data set to be operated as a half-regenerator. Two data sets are required for each 4-wire regenerative repeater. Interconnections between the two data sets are established through the CUSTOMER B connectors. Figure 4 illustrates the typical regenerative repeater interconnections. Both the RGRN and SS interface leads must be ON when the data set is used as a regenerator. The frequency of the receiver clock signal appearing at SCR/DD is 1200 Hz (receiver dibit clock). Receive data (RD/BB) is connected to the send data (SD/BA) input of the transmitter. Serial clock receive (SCR/DD) is connected to the external timing input (SCTE/DA) of a transmitter to keep the transmitter dibit clock "in phase" with the receiver dibit clock. This maintains the identity of the A and B data bits and guarantees that the repeated line signal is identical to the received line signal at a regenerative repeater.

6.31 When RGRN is OFF, (for normal clocks) the frequency of the receiver clock (SCR/DD) is the bit rate frequency, either 2400 Hz or 1200 Hz as determined by the condition of the SS interface lead.

6.32 Table D summarizes the clock rates appearing on SCT/DB and SCR/DD leads as a function of the control leads RGRN, SS, and SCX2.

K. Prepare Receiver (PR) — Driver

Note: The PR circuit is provided by circuit packs located at positions 049 and 050.

6.33 The PR circuit is used to provide an indication to control equipment after the synchronizing code has been detected and completed, and the received data is positive for at least 85 milliseconds. The customer business machine must supply the positive send data at the transmitter. The PR circuit is switched OFF when either a negative voltage occurs in the receive data or the COO/CF circuit is in the OFF condition. The PR circuit will remain OFF until COO/CF is switched ON or the receive data is continuously positive for at least 85 milliseconds.

L. Serial Clock Transmit (SCT/DB) — Driver

6.34 The SCT/DB signal is a square-wave clock provided by the data set at the data rate or twice the data rate. The SCT/DB signal is used by the customer business machine to synchronize send data with the transmitter timing.

6.35 When external transmitter timing (SCTE/DA) is used, jitter will be present in the SCT/DB signal due to discrete phase corrections made in the transmitter timing circuit.

6.36 Each correction advances or delays a positive transition of SCT/DB by approximately $8.7 \mu\text{sec}$ ($1/48$ of a 2400-Hz period). Once initial phase synchronization has been obtained, the correction rate is determined by the difference in frequencies of the internal oscillator and the external timing source.

6.37 The maximum correction rates for maintenance of synchronization (exclusive of noise-induced corrections) to be expected after initial phase synchronization has been obtained are given below. These rates are given as a function of the external timing accuracy and presume:

- (a) An internal clock of 2400 (± 0.0005) Hz
- (b) An external clock at 2400 Hz and
- (c) A positive transition rate of SCTE/DA that is at least equal to the maximum correction rate given.

EXTERNAL CLOCK ACCURACY	MAXIMUM CORRECTIONS PER SECOND
PERCENT	
± 0.01	12.2
± 0.001	1.7
± 0.0005	1.2

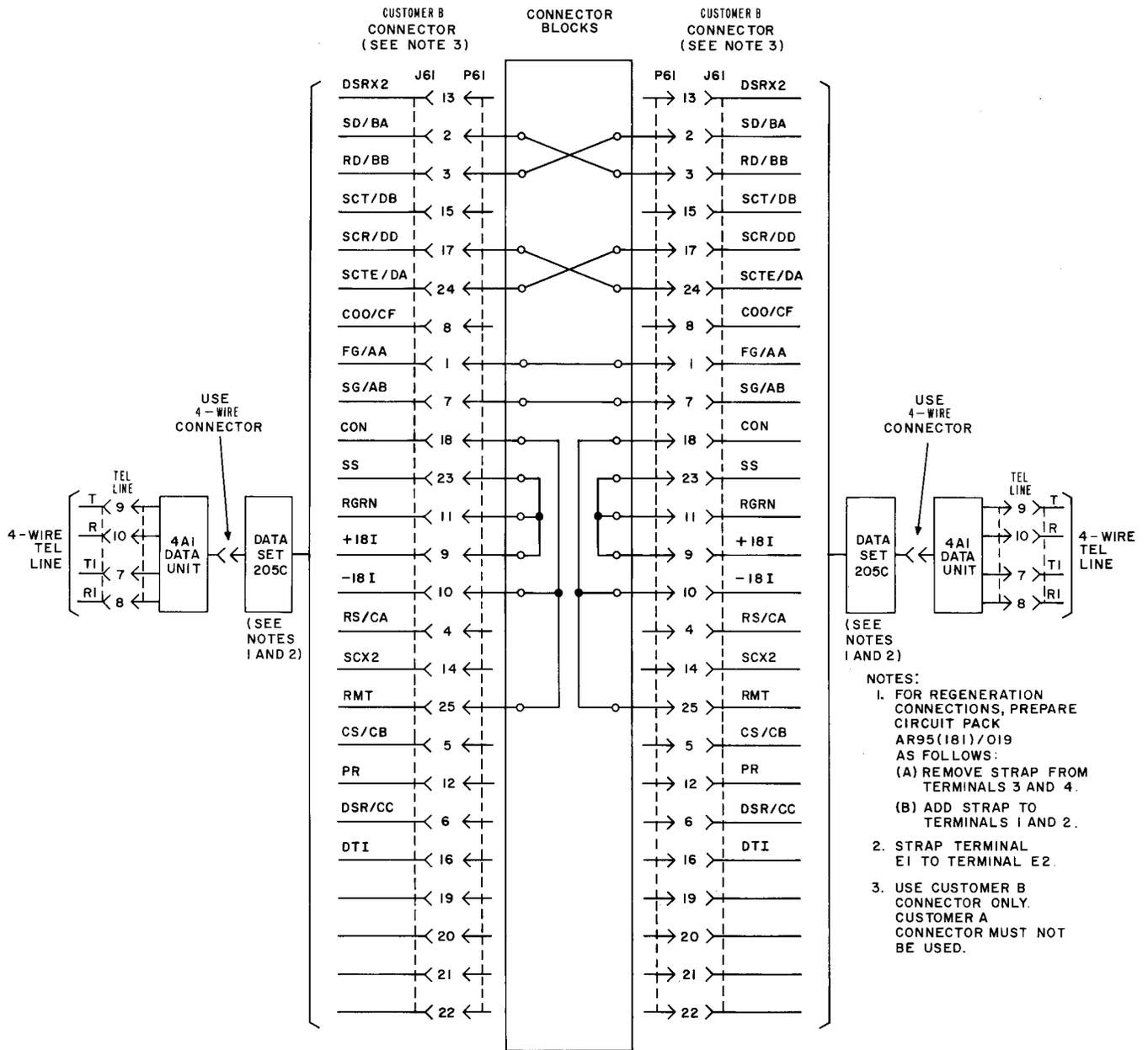


Fig. 4 — Regenerative Repeater Interconnections

TABLE D
CLOCK RATES

SS	RGRN	SCX2 STRAPPED TO TERM. 7	CLOCK FREQ. (Hz)	
			SCT	SCR
ON	OFF	NO	2400	2400
ON	OFF	YES	4800	4800
OFF	OFF	NO	1200	1200
OFF	OFF	YES	2400	2400
ON	ON	NO	2400	1200

M. Serial Clock Receive (SCR/DD) — Driver

6.38 The SCR/DD signal is a square-wave clock provided by the data set at the data rate or twice the data rate. Positive transitions of SCR/DD are coincident with the transitions of receive data. The frequency of SCR/DD is 1200 Hz when both RGRN and SS are ON.

6.39 Jitter will be present in the SCR/DD signal due to discrete phase corrections made in the receiver timing circuit. Corrections never occur more often than once every 11.7 msec (every 28 cycles of a 2400-Hz clock period). After initial phase synchronization is obtained, additional corrections will be necessary only when the SCR/DD signal drifts out of phase due to local oscillator drift, corrections generated by noise, or a change in the line delay. Consequently, corrections of SCR/DD should occur considerably less often than once every 11.7 msec during normal operation. For example, corrections due to oscillator drift will occur at a rate of approximately six per second if the transmitter clock variation is ± 0.01 percent.

N. Send Data (SD/BA) — Terminator

6.40 Serial data to be transmitted is applied to the data set on the SD/BA circuit in synchronism with SCT/DB. With SCT/DB at twice the data rate, transitions of SD/BA must occur within ± 80 μ sec of every other positive transition of SCT/DB. When SCT/DB is at the data rate, transitions of the SD/BA must occur within ± 160 μ sec of each positive transition of SCT/DB (all measurements taken at the CUSTOMER B connector) when used for transmitter timing.

6.41 The rise and fall times of the SD/BA input should be no greater than 11 μ sec.

O. Receive Data (RD/BB) — Driver

6.42 The serial data obtained from demodulating the received line signal is delivered to the interface by the RD/BB circuit. Transitions of RD/BB are coincident with positive transitions of SCR/DD. The RD/BB circuit is clamped OFF whenever the received input power is below the padded receiver sensitivity.

7. TRANSMISSION REQUIREMENTS

7.01 Error Performance: The Data Set 205C2 is designed to operate on a long-term error rate of less than one error in 10^5 bits when transmitting random data at 2400 bps on private line facilities with C2 conditioning.

7.02 Transmitter Circuits: The transmitter output power can be padded by -9 , -6 , -3 , or 0 dBm. The transmitter output impedance is 600 ohms for 4-wire facilities and 900 ohms for 2-wire facilities.

7.03 Receiver Circuits: The receiver input impedance is 600 ohms on 4-wire facilities or 900 ohms on 2-wire facilities. The input power can be padded as shown in Table E.

TABLE E

PAD LOSS (dB)	MINIMUM INPUT POWER (dBm)	MAXIMUM INPUT POWER (dBm)
0	-38	-10
5	-33	-5
10	-28	0
15	-23	$+5$

7.04 The automatic gain control range is 30 dB.

7.05 The derived clock lock-in-time is 0.6 second maximum following RS/CA switching ON and when using the transmitter internally generated idle code.

7.06 Receiver Clock Recovery: The data set uses a zero-crossing clock recovery system that requires the number of crossings per second

to be greater than some minimum value in order to keep the receiver in synchronization in the presence of clock variation and noise and to restore the receiver clock after a dropout. The definition of a crossing depends on the bit rate of the data set.

(a) For a 2400-bps rate, a crossing is defined as a change in a bit state with respect to the state of the second previous bit. A dot pattern (-101010-) contains no data crossings and may not be used. Quad-bit codes, such as 1000, 1100, 1011, etc, are necessary to provide crossings.

(b) For a 1200-bps rate, a crossing is defined as a change in the bit state with respect to the previous bit. Using this definition, only the steady 0000 or 1111 codes are prohibited.

7.07 Data Crossing Rates: Due to the transmitter clock variation and noise, a minimum number of crossings per second must be provided to hold the receiver clock. After a dropout, a higher crossing rate should be used.

(a) **Minimum Crossing Rate:** The minimum crossing rate per second (Table F) necessary to hold the receiver clock in synchronization depends primarily on the accuracy of the transmitter timing source. (The receiver clock accuracy is fixed at ± 0.0005 percent by the internal crystal oscillator.)

TABLE F

TRANSMITTED TIMING ACCURACY	MINIMUM CROSSING RATE PER SECOND
PERCENT	
± 0.0005	10
± 0.0010	14
± 0.0050	46
± 0.0100	90

(b) **Crossing Rate Versus Restoral Time:** After a dropout period, the receiver clock restoral time will depend primarily on the crossing rate of the received data. To ensure restoring the far-end receiver clock after dropout, the local business machine shall provide a send data (SD/BA) crossing rate that exceeds

the minimum values given in (a). The figures presented in Table G assume a worstcase transmitter clock variation, ie, ± 0.01 percent.

TABLE G

CROSSINGS PER SECOND	MINIMUM RESTORAL TIME
	SECONDS
150	1.75
300	0.53
600	0.22

8. DATA SET GROUNDING

8.01 The data set frame ground (FG/AA) and the ac power third-wire ground are connected in the data set. However, the data set signal ground (SG/AB) is connected to FG/AA and the ac power ground through a wire strap between terminals E1 and E2 on the connector mounting plate. Some applications may require that this grounding be established in the customer's equipment. To satisfy this condition, the strap between E1 and E2 is removed, and FG/AA and SG/AB, respectively, are connected in the customer's equipment through leads in the CUSTOMER A connector. When grounding is provided in this manner, the resistance of the SG/AB to FG/AB must be low enough that a short to SG/AB from the ac supply will cause the fuse in the ac supply to open.

8.02 When the E1 to E2 strap is present, ac power supply and grounding arrangements for the customer's data equipment and the data set must be such that the difference in ground potential between the separate equipment does not exceed ± 2.0 volts peak when measured on an oscilloscope with a bandwidth of at least one megacycle.

9. DATA SET TESTING

9.01 The following test procedures do not cover all trouble possibilities. The tests are designed to indicate which circuit pack (or packs) should be replaced as a logical choice to repair a trouble condition using an oscilloscope.

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9.02 It is recommended that the tests be performed in numerical sequence if the type of trouble is unknown. If a trouble or an abnormal condition still exists after replacement of the suggested circuit packs, the preceding test must be made and each preceding test until the circuit pack causing the trouble is replaced.

9.03 *The following test equipment is required to perform the tests:*

- 1 — 901B-2 Data Test Set
- 1 — 902B Data Test Set
- 2 — 903B Data Test Sets
- 1 — KS-14510 volt-ohm-milliammeter
- 1 — 1011-type handset
- 1 — Oscilloscope, Tektronix 533 with CA plug-in unit (or their equivalent)
- 1 — KS-19087-L2 connector
- 12 — Test probes — double end — WECO 735A (to mate with test points on data set circuit pack assemblies)
- 6 — Test probes — scope probe end adapter — WECO 729A or use Mueller "Micro-Gater" clips (34C), or equivalent, to make up test probes
- 1 — 600-ohm resistor, ± 1 percent, 0.25 watt.

A. Data Set Preparation and Arrangement of External Test Equipment

9.04 Prepare the Data Set 205C2 as follows:

- (a) In the following order, disconnect the ac power cord, the TEL LINE, the customer cord(s), and the 4A1 Data Unit cord from their respective connectors on the data set.
- (b) Check that terminals E1 to E2 on the data set are strapped.
- (c) Carefully remove and check the AR95-(181)/019 circuit pack. Strap terminals 3 to 4 and remove any strap between terminals 1 and 2. Carefully reinsert the circuit pack in the proper position.
- (d) Connect the 4A1 Data Unit cord to the 4-WIRE connector.

- (e) Operate the LINE-TEST key to TEST position.

9.05 *Connect and prepare the 901B-2 Data Test Set as follows:*

- (a) Position both A TEST and B TEST switches to OFF and ATT-UNATT switch to UNATT. This will permit the data set to operate at full speed.

- (b) Connect the 901B-2 test set cord to the interface adapter (part of the 901B-2 test set cover). Connect the interface adapter to the data set CUSTOMER B connector by using the W25A cord provided. Set SELECTOR switch to 3.

- (c) Position B TEST switch to 1.

- (d) Condition the KS-14510 to measure on the 60 Vdc scale. Connect the negative lead to terminal A and the positive lead to terminal C, both on the 901B-2 test set.

- (e) Apply ac power to the data set. Observe an indication of 18 (± 2.2) Vdc (negative power supply) on the test meter.

- (f) Disconnect the meter probes from the 901B-2 test set.

- (g) Position B TEST switch to 2.

- (h) Connect the negative test meter lead to terminal C and the positive lead to terminal A, both on the 901B-2 test set. Observe an indication of 18 (± 2.2) Vdc (positive power supply) on the test meter.

- (i) If both the measured indications are within the specified limits, remove the ac power from the data set and disconnect the test meter leads from the 901B-2 test set terminals.

- (j) Make the following arrangements on the interface adapter:

- Open shorting clips 11, 12, 14, 18, 23, 24, and 25.
- Strap 9 to EQ 18, 9 to 19, 20 to EQ 23, TST 14 to EQ 25, 10 to EQ 11, and TST 18 to EQ 12.

- (k) Connect the ac power cord to the data set.

9.06 Measure the interface voltages. The dc measurements are made between terminals A and C. Terminal C is always at ground potential. The ac measurements are made between terminals B and C.

9.07 Measure the data set ready (DSR/CC) interface voltage. Set the 901B-2 A TEST switch to position 1 and B TEST switch to OFF. Proceed as follows:

(a) With the equipment prepared as above, the DSR voltage measured between 901B-2 test set terminals A and C (ground) should be $-6.5 (\pm 1.3)$ Vdc. Remove the test meter probes. If the reading is out of limits, test as described in TEST 12.

(b) Operate the LINE-TEST key to LINE position.

(c) The DSR/CC voltage measured between terminals A and C should be $+7.0 (\pm 1.3)$ Vdc. If the reading is out of limits, test as described in TEST 12.

(d) Operate the LINE-TEST key to TEST position.

9.08 Measure for the dc and ac interface voltage requirements listed in Table H. If any measurement exceeds the listed tolerance, refer to the appropriate test section using Table I for the same A TEST and B TEST switch positions. It is recommended that all dc voltage measurements be obtained first, then repeat the procedures to obtain ac voltage indications.

TABLE H
INTERFACE REQUIREMENTS

LEAD TESTED	A TEST POSITION	B TEST POSITION	RS LEAD CONDITION	SD LEAD CODE*	TEST METER INDICATION	
					DC MEASUREMENTS	AC MEASUREMENTS
SCT	23	8	OFF	01	0.0 (± 0.7)	6.8 (± 1.6)
DTI	22	8	OFF	01	0.0 ($+1.5$ -0.7)	7.5 (± 2.1)
CS	21	8	OFF	01	$-6.5 (\pm 1.3)$	0.0
RD	20	8	OFF	01	$-6.1 (\pm 0.7)$	0.0
SCR	19	8	OFF	01	0.0 (± 0.7)	6.8 (± 1.6)
PR	18	8	OFF	01	$-6.5 (\pm 1.3)$	0.0
COO	17	8	OFF	01	$-6.5 (\pm 1.3)$	0.0
CS	21	5	ON	01	$+7.0 (\pm 1.3)$	0.0
RD	20	5	ON	01	0.0 (± 0.7)	6.8 (± 1.6)
PR	18	5	ON	01	$-6.5 (\pm 1.3)$	0.0
COO	17	5	ON	01	$+7.0 (\pm 1.3)$	0.0
RD	20	4	ON	00	$+6.1 (\pm 0.7)$	0.0
PR	18	4	ON	00	$+7.0 (\pm 1.3)$	0.0
RD	20	3	ON	11	$-6.1 (\pm 0.7)$	0.0

* With 900-type test equipment, the 01 code which appears on the DTI lead is connected to the SD lead for the test indicated.

TABLE I
OSCILLOSCOPE TESTS

B TEST POSITION	A TEST POSITION						
	23	22	21	20	19	18	17
8	4	2	3, 10	5, 9	4	14	6
5			3, 10	5, 9		14	6
4				5, 9		14	
3				5, 9		14	
6	11		11	11	11		11

9.09 Operate the ATT-UNATT switch on the 901B-2 test set to ATT position. (In the ATT position, the data set is operated at half speed.) Repeat all measurements specified in Table H. Results should be the same for all steps except when B TEST switch is in position 5 and A TEST switch is in either position 20 or 18. Measurements for these steps are:

A TEST (position 20)

+6.1 (± 0.7) Vdc; 0 Vac

A TEST (position 18)

+7.0 (± 1.3) Vdc; 0 Vac.

Note: Remove test meter leads and observe polarity before each measurement.

9.10 The numbers in Table I indicate a specific group of oscilloscope tests to be used for many combinations of A TEST and B TEST positions. The table can be used to rapidly trouble shoot a voltage requirement failure resulting from Table H tests. Make the lowest numbered test first if more than one test number is given.

9.11 Perform preliminary data set tests using the following sequence:

(a) Position A TEST switch to 23 and B TEST switch to 5.

(b) Position ATT-UNATT switch to UNATT.

(c) Place 1011-type handset across terminals B and C on 901B test set and a 2400-Hz tone will be heard (full-speed transmit clock).

If tone is not heard, test as described in TEST 4.

(d) Position ATT-UNATT switch to ATT and a 1200-Hz tone will be heard (half-speed transmit clock).

(e) Position ATT-UNATT switch to UNATT. A 2400-Hz tone will be heard (full-speed transmit clock).

(f) Momentarily place a strap from EQ 14 to TST 7. A 4800-Hz tone will be heard (double-speed transmit clock).

(g) Position A TEST switch to 19, repeat (b) through (f) (receive clock), and obtain the same requirements.

(h) Position A TEST switch to 19 and ATT-UNATT switch to UNATT.

(i) Remove the strap between 10 and EQ 11 and momentarily place a strap between 9 and EQ 11 on the interface adapter. A 1200-Hz tone will be heard (half-speed receive clock).

(j) Remove the strap between 9 and EQ 11 and place a strap between 10 and 11 EQ on the interface adapter.

(k) Remove the strap between terminals 3 and 4 on circuit pack AR95(180)/019.

(l) Position the LINE-TEST key in LINE position.

(m) Position A TEST switch and B TEST switch to OFF.

(n) Connect a strap between terminals EQ 24 and 17 on the interface adapter.

(o) Condition the KS-14510 test meter to measure on the 3-volt ac scale. Measure between the TRANSMIT CLOCK terminal and the RECEIVE CLOCK terminal on the 901B test set. The test meter shall indicate less than 0.5 Vac. If the meter indication exceeds 0.5 Vac, test as described in TEST 13.

Note: Use the special 0-3VAC scale (red) provided on the test meter.

- (p) Remove the strap between terminals EQ 24 and 17 on the interface adapter.
- (q) Replace the strap between terminals 3 and 4 on circuit pack AR95(181)/019.
- (r) Remove ac power from the data set.
- (s) Remove the strap between terminals 9 and 18 and strap terminals 10 and 18 on the interface adapter.
- (t) Place a 600-ohm resistor between terminals 7 and 8 on the KS-19087-L2 connector and connect it to the TEL LINE connector on the 4A1 Data Unit. Condition the KS-14510 test meter to measure on the 3-volt ac scale and place probes across the 600-ohm resistor.
- (u) Check that the LINE-TEST key is in LINE position.
- (v) Position both A TEST and B TEST switches to OFF.
- (w) Connect ac power to the data set.
- (x) Position B TEST switch to 5. Line readings should be:

VOLTS	TRANSMIT OUTPUT LEVEL	STRAPPING ON AR90(182)/044
0.70	0	1-4
0.50	-3	1-3
0.35	-6	1-2
0.25	-9	None

Note: All readings ± 0.15 volt. If reading is out of limit, test as described in TEST 6.

- (y) Position B TEST switch to 8. A 0 reading should be obtained for all transmit output levels.
- (z) Remove the KS-19087-L2 connector from the TEL LINE connector.
 - (aa) Operate the LINE-TEST key to TEST position.
 - (ab) Disconnect ac power from the data set.

- (ac) Proceed with maintenance tests.
- (ad) Table J lists the dc voltages that appear at test points on the circuit packs. If the voltage indication is not obtained, the circuit pack shall be replaced.

TABLE J
DC VOLTAGE READING ON DATA SET

DC VOLTAGE	TEST POINT	CIRCUIT PACK LOCATION
+6.2 (± 0.6)	TP8	001, 002, 003, 005, 006, 007, 008, 009, 037, 038, 039, 040, 041, 042, 043, 049, 050, 053, 054, 055, 056, 057, 058
	TP14	010, 017
	TP6	012, 014
	TP2	021
+6.8 (± 1.0)	TP7	019
	TP8	059
+8.2 (± 0.9)	TP1	044
+12.0 (± 1.5)	TP11	017
	TP6	019
-6.2 (± 0.6)	TP6	060
-6.8 (± 1.0)	TP12	059
-8.2 (± 1.1)	TP3	012, 014
-12.0 (± 1.5)	TP10	016

B. Data Set Test Setup

9.12 Prepare the data set for testing as follows:

- (a) In the following order, disconnect the ac power cord, the telephone line, the customer cord(s), and the 4A1 Data Unit cord from their respective connectors on the data set.
- (b) Check that terminals E1 to E2 on the data set are strapped.

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(c) Carefully remove and check circuit pack AR95(181)/019. Strap terminals 3 and 4 and remove the strap between terminals 1 and 2 if the board is not already strapped in this manner. Carefully reinsert the circuit pack in the proper position.

(d) Connect the 4A1 Data Unit cord to the 4-WIRE connector.

(e) Operate the LINE-TEST key to TEST position.

9.13 *Connect and prepare the 901B-2 Data Test Set as follows:*

(a) Position both A TEST and B TEST switches to OFF and ATT-UNATT switch to UNATT.

(b) Connect the 901B-2 test set cord to the interface adapter (part of the 901B-2 test set cover). Connect the interface adapter to the data set CUSTOMER B connector by using the W25A cord provided. Set SELECTOR switch to 3.

(c) Make the following arrangements on the interface adapter:

- Open shorting clips 11, 14, 23, 24, and 25.
- Strap 9 to 19, 10 to EQ 11, 10 to 18, 20 to EQ 23, and EQ 25 to TST 14.

(d) Set the 903B test set switches as follows:

- BIT RATE to EXT CLOCK
- RANDOM-DOT to RANDOM
- TRIGGER to + (plus).

Note: In the following connections, strap red to red and black to black. Connect the EXT CLOCK terminals of the 903B test set to the TRANSMIT CLOCK terminals of the 901B-2 test set.

(e) Connect the ac power cord of the 903B test set and the ac power cord of the data set to an ac voltage source.

9.14 *Information Note:* The 901B-2 test set performs the functions listed below:

(a) SELECTOR switch in position 3 prepares the A TEST and B TEST switches to control the data set.

(b) A TEST switch connects various interface leads to test terminals on the 901B-2 test set. See Table K.

(c) B TEST switch is used in conjunction with A TEST switch and in a similar manner. See Table L.

(d) The ATT-UNATT switch is used as one of two control inputs for speed selection.

9.15 *Signal grounds are available at the following circuit pack locations:*

(a) TP12 on 008

(b) TP1 on 012

(c) TP1 on 014

(d) TP5 on 017

(e) TP4 on 021

(f) TP3 on 044

(g) TP4 on 059.

9.16 *At the conclusion of the maintenance tests, perform the following steps:*

(a) Disconnect ac power from both the 903B test set and the data set.

(b) Remove all test equipment connections.

(c) Remove the strap between terminals E1 and E2 if required to do so by service order.

(d) Verify that original options are replaced in the data set.

(e) Operate and lock the LINE-TEST key in LINE position.

(f) Connect the 4A1 Data Unit cord to either the 2-WIRE or 4-WIRE connector in accordance with the original option.

(g) Connect ac power to the data set.

(h) If 4-wire operation is used, call the data test center for a final check before releasing the data set to customer service.

**TABLE K
A TEST SWITCH**

A TEST POSITION	CONNECTS			
	INTERFACE LEAD		RMT	901B A TERM. TO
	RS TO	SD TO	TO	
1				DSR
2				RD
3				SCT
4				CS
5				COO
6	+18I	-18I	GRD	RD
7	+18I	+18I	GRD	RD
8	+18I	DTI	GRD	RD
9	+18I		GRD	SCR
10	+18I			CS
11	+18I			COO
12	+18I			
13	+18I			
14	+18I			SCR
15	+18I			
16	+18I			
17				COO
18				PR
19				SCR
20				RD
21				CS
22				DTI
23				SCT
OFF				

Note: Blank spaces indicate no connections.

**TABLE L
B TEST SWITCH**

A TEST POSITION	CONNECTS			
	INTERFACE LEAD		RMT	901B A TERM. TO
	RS TO	SD TO	TO	
1				-18I
2				+18I
3	+18I	-18I	GRD	
4	+18I	+18I	GRD	
5	+18I	DTI	GRD	
6	GRD	DTI	+18I	
7	GRD	DTI	+18I	
8	GRD	DTI	GRD	
9	GRD	DTI	GRD	
10	+18I	+18I	GRD	
11	GRD	+18I	+18I	
OFF				

Note: Blank spaces indicate no connections.

TEST 1 — CLOCK CIRCUIT

9.17 The clock circuit consists of a 65A oscillator and associated countdown circuits. The clock circuit components generate square-wave signals at frequencies required by both transmitter and receiver sections of the data set. The waveform shown in Fig. 5 represents normal operation of the clock circuit and is keyed to the respective test point on the functional schematic shown in Fig. 6. Replace the suggested circuit packs if the proper result for the test is not obtained.

Note: All VOLTS/CM readings in the following tests allow for oscilloscope probe attenuation of X10.

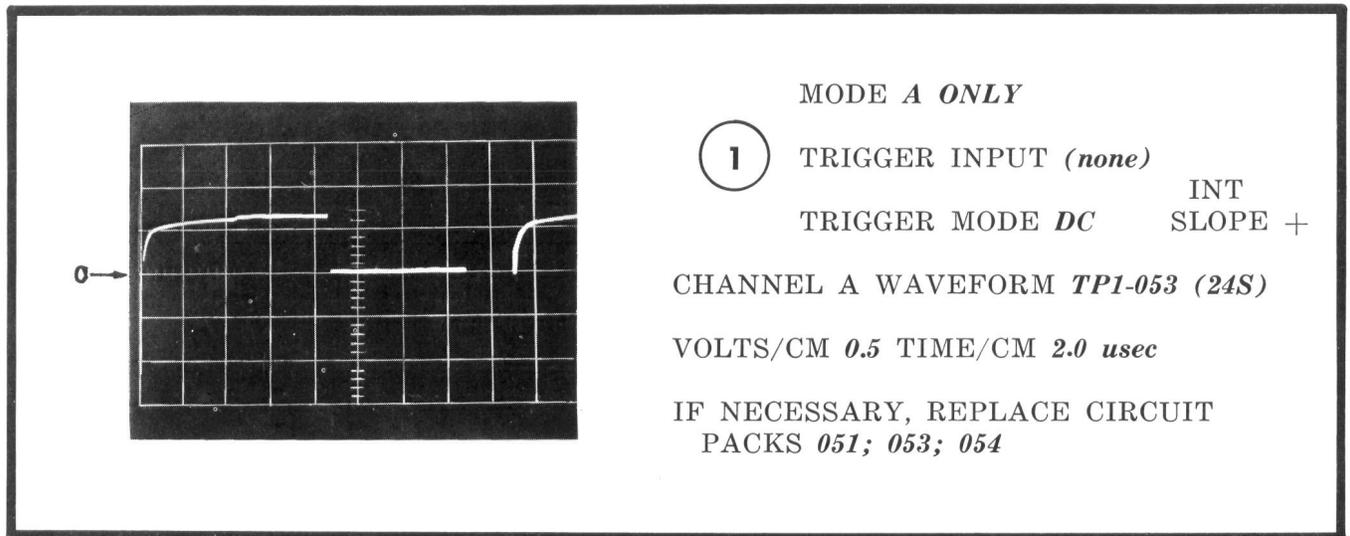


Fig. 5 — Clock Circuit Test

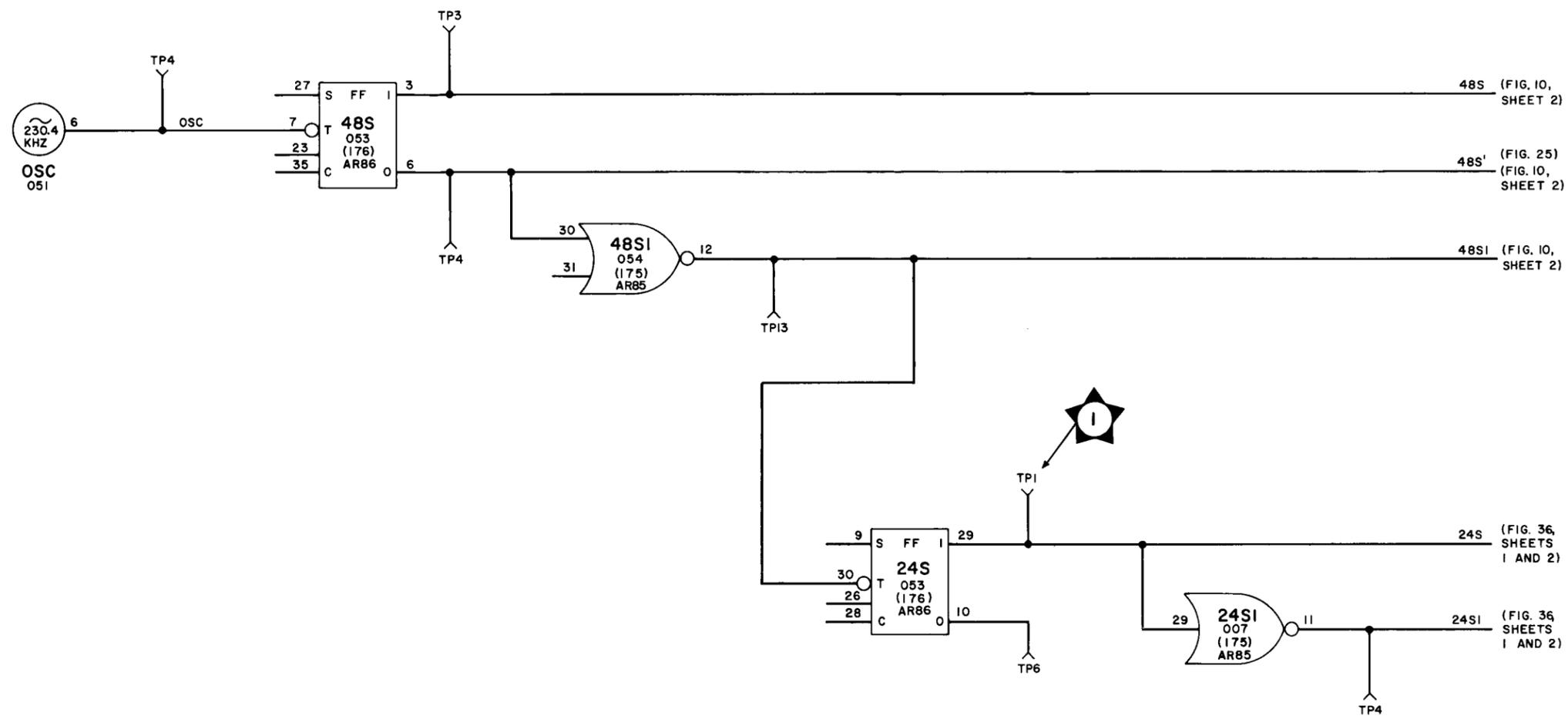


Fig. 6 — Clock Circuits, Functional Schematic

TEST 2 — TRANSMITTER TIMING

9.18 The transmitter timing circuits generate the timing signals required by the data transmitter circuits. Input signals from the clock circuits are divided by complimentary flip-flop chains to provide the required pulse train frequencies for the various operational modes of the data transmitter and associated circuits. When an external timing source is used, add-delete count correction circuits adjust the transmitter operation to allow the transmitter timing to phase-lock with the external signal source.

9.19 Waveforms shown in Fig. 7 through Fig. 9 are keyed to the functional schematic shown in Fig. 10 (2 sheets). The waveforms illustrate normal operation of the flip-flop circuits when the data set is in TEST condition.

Observe a dc level
of +6.5 (± 0.9) Vdc.

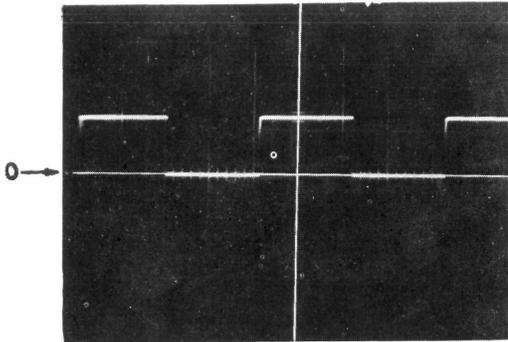
MODE A *ONLY*

② TRIGGER INPUT (*none*) INT
TRIGGER MODE *DC* SLOPE +

CHANNEL A WAVEFORM *TP4-009 (SXG)*

VOLTS/CM *0.5* TIME/CM *2.0 usec*

IF NECESSARY, REPLACE CIRCUIT
PACKS *008; 009; 059*



MODE A *ONLY*

③ TRIGGER INPUT (*none*) INT
TRIGGER MODE *DC* SLOPE +

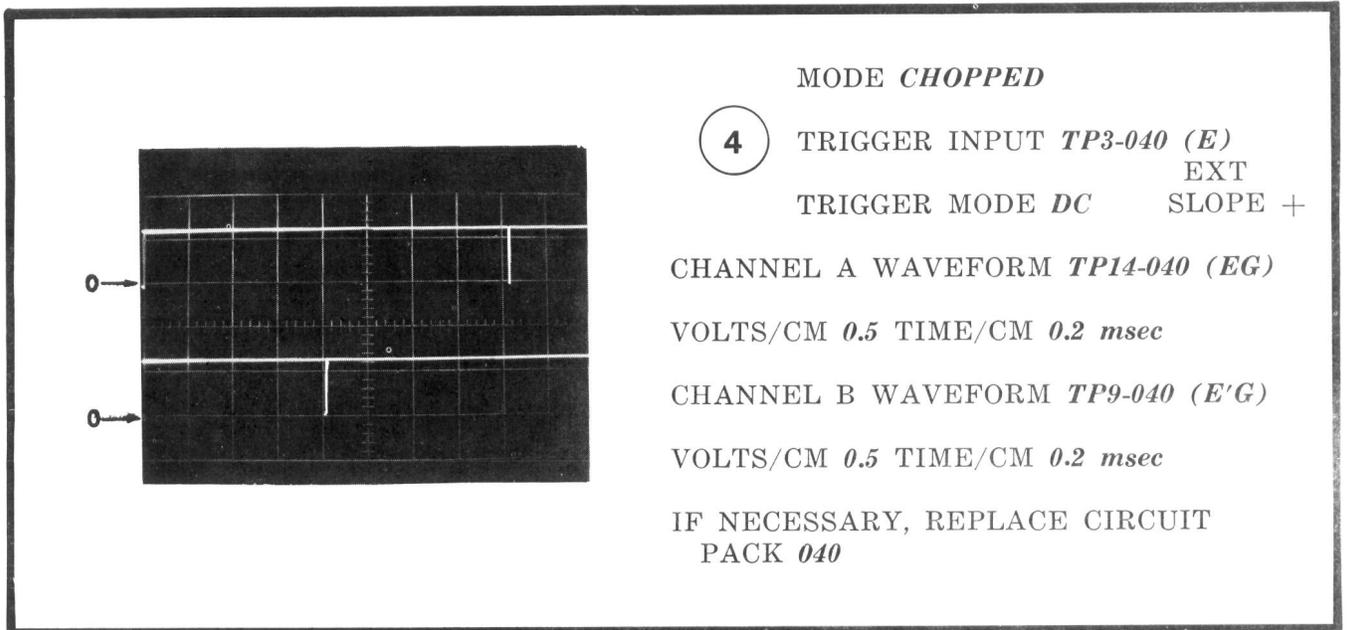
CHANNEL A WAVEFORM *TP14-041 (2ST')*

VOLTS/CM *0.5* TIME/CM *50 usec*

IF NECESSARY, REPLACE CIRCUIT
PACKS *041; 042; 043*

Fig. 7 — Transmitter Timing Test

CONDITIONS: Adjust oscilloscope to trigger on the rise (positive transition) of E.



CONDITIONS: Same as 4

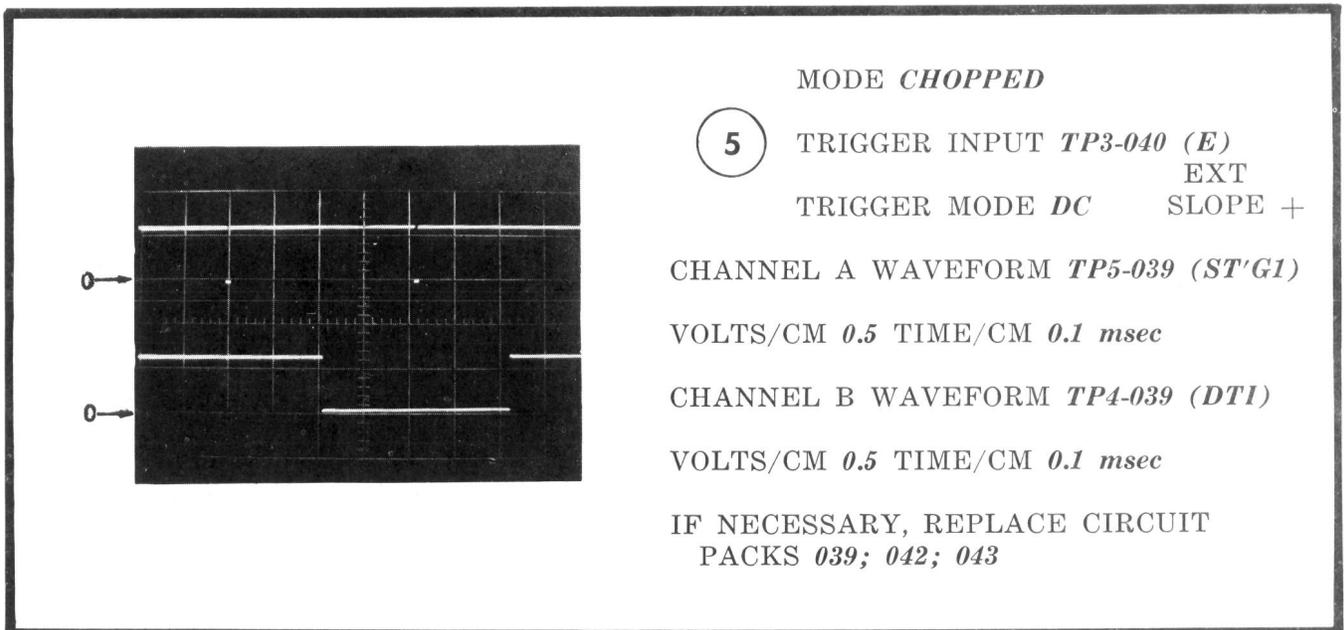
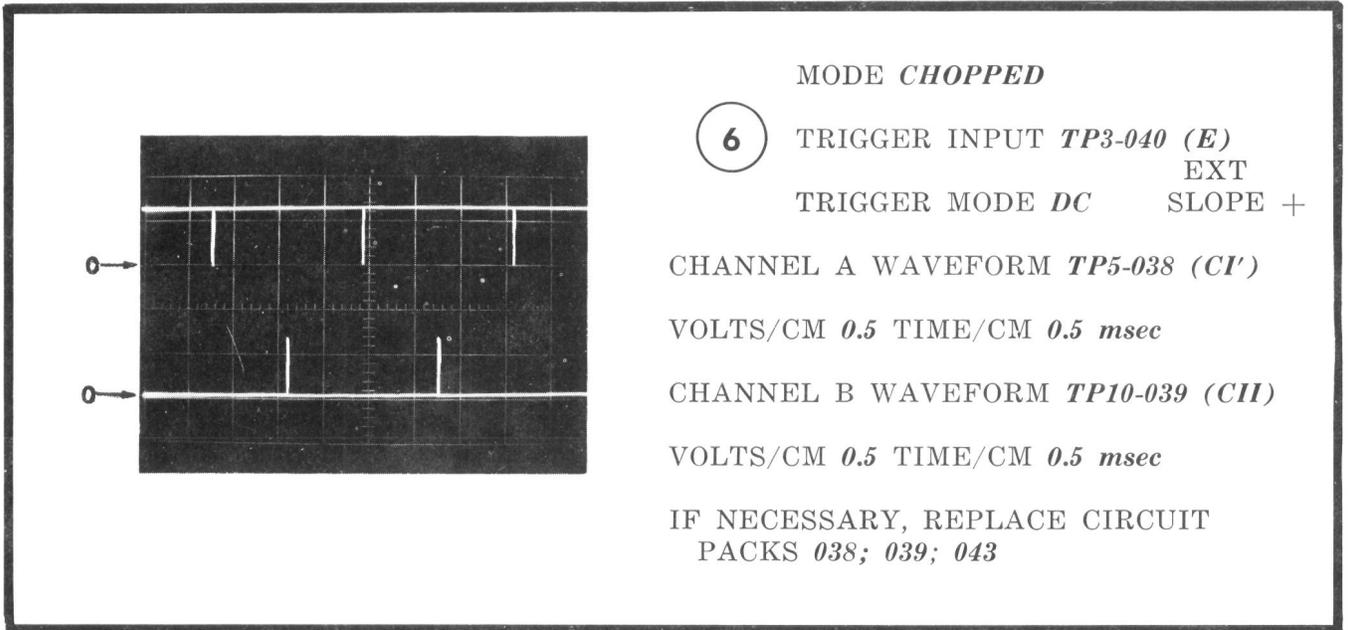


Fig. 8 — Transmitter Timing Test

CONDITIONS: Same as 4



CONDITIONS: Same as 4

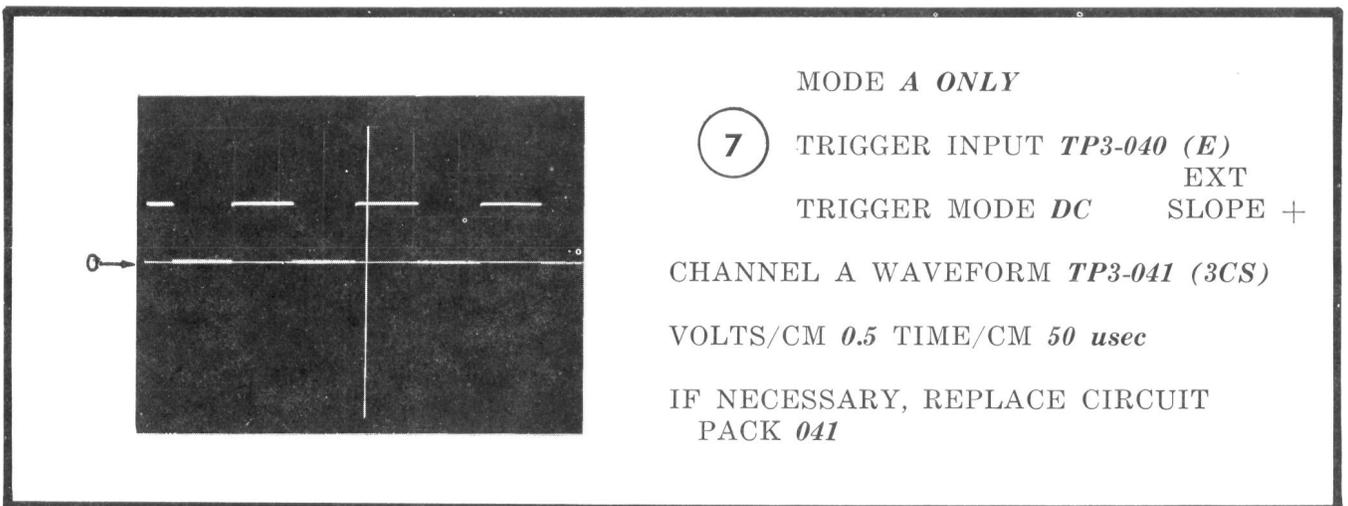


Fig. 9 — Transmitter Timing Test

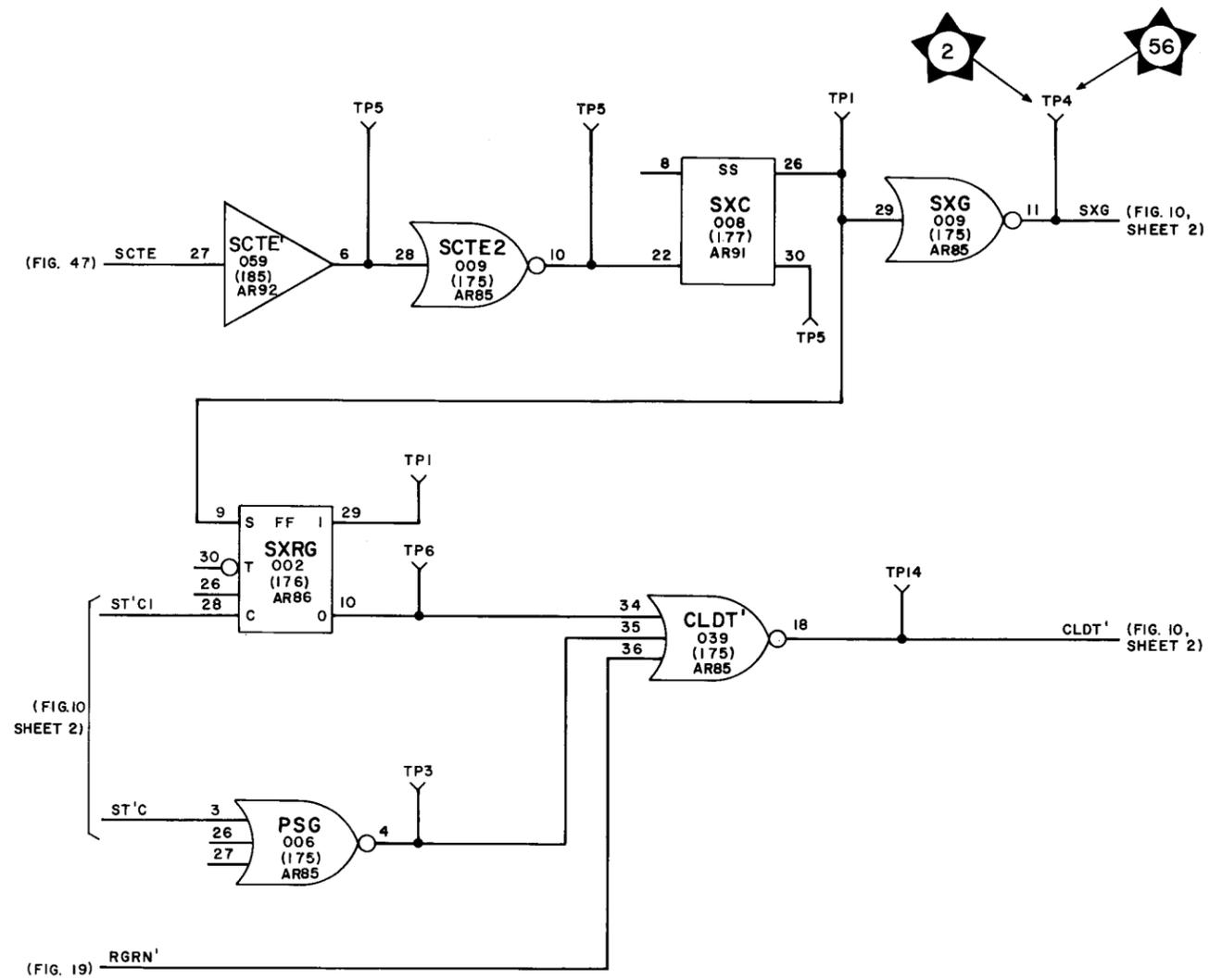


Fig. 10—Transmitter Timing Circuits, Functional Schematic (Sheet 1 of 2)

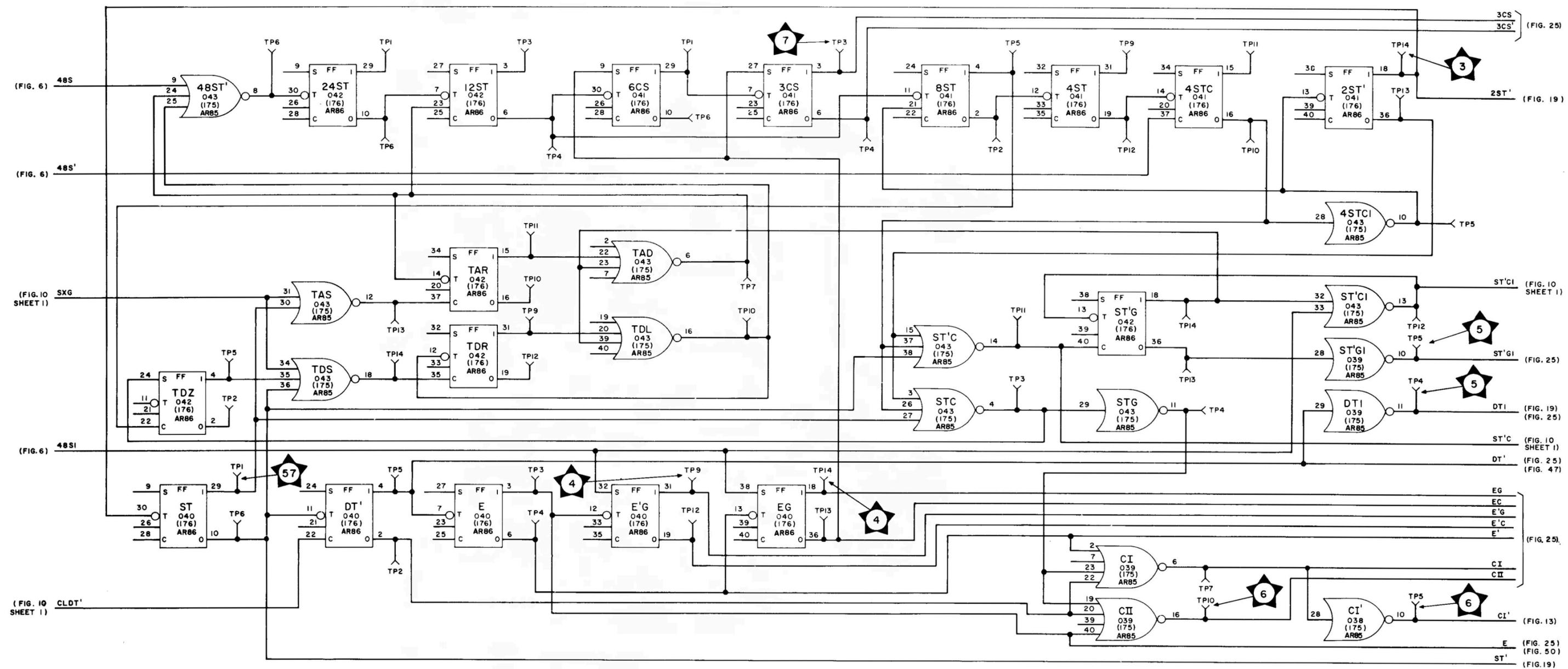


Fig. 10—Transmitter Timing Circuits, Functional Schematic (Sheet 2 of 2)

TEST 3 — TRANSMITTER CONTROL TIMING

9.20 The transmitter control timing circuits provide transmitter timing functions when keyed by request-to-send (RS/CA) signal through the customer connector. The timing circuits generate a clear-to-send (CS/CB) signal to notify customer equipment that the send-data (SD/BA) lead is available and the data set will accept and process customer equipment signals.

9.21 Voltage and waveform requirements shown in Fig. 11 and Fig. 12 are keyed to the functional schematic shown in Fig. 13.

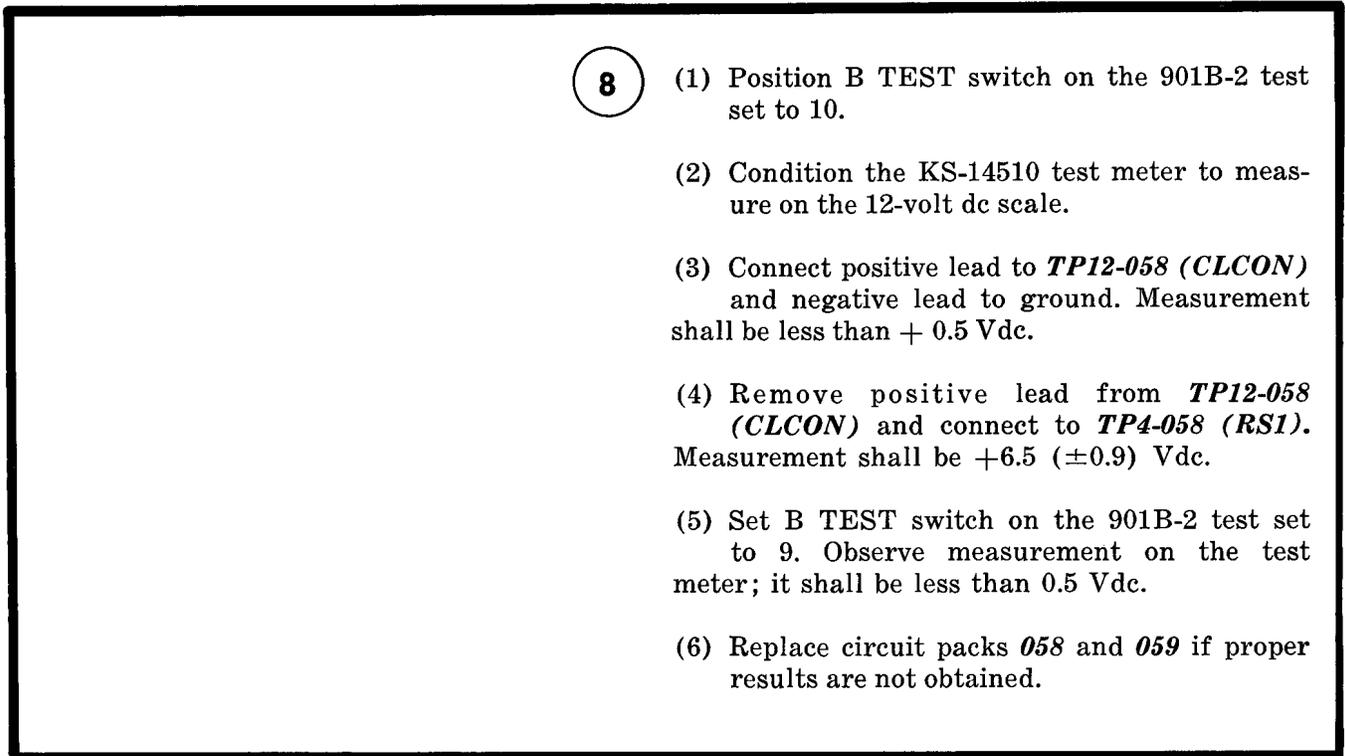
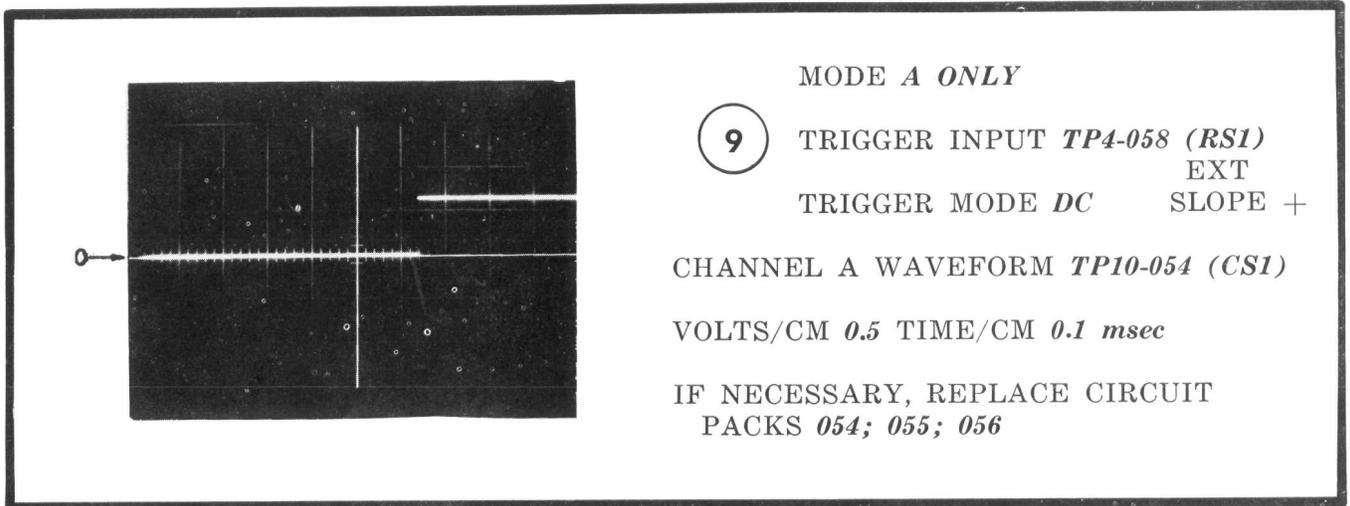
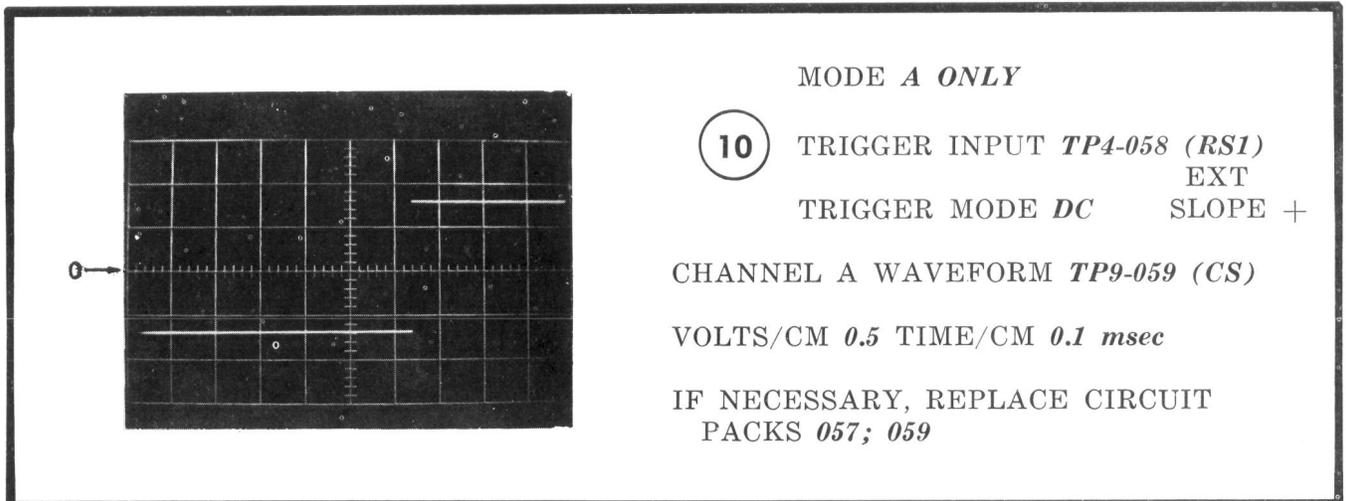


Fig. 11 — Transmitter Control Timing Test

CONDITIONS: Adjust oscilloscope to trigger on the rise of RS1. Operate B TEST switch between positions 9 and 10. Observe waveform as shown each time the B TEST switch is operated between positions 9 and 10.



CONDITIONS: Same as 9.



After completing Step 10 (end of Test 3), position B TEST switch to OFF.

Fig. 12 — Transmitter Control Timing Test

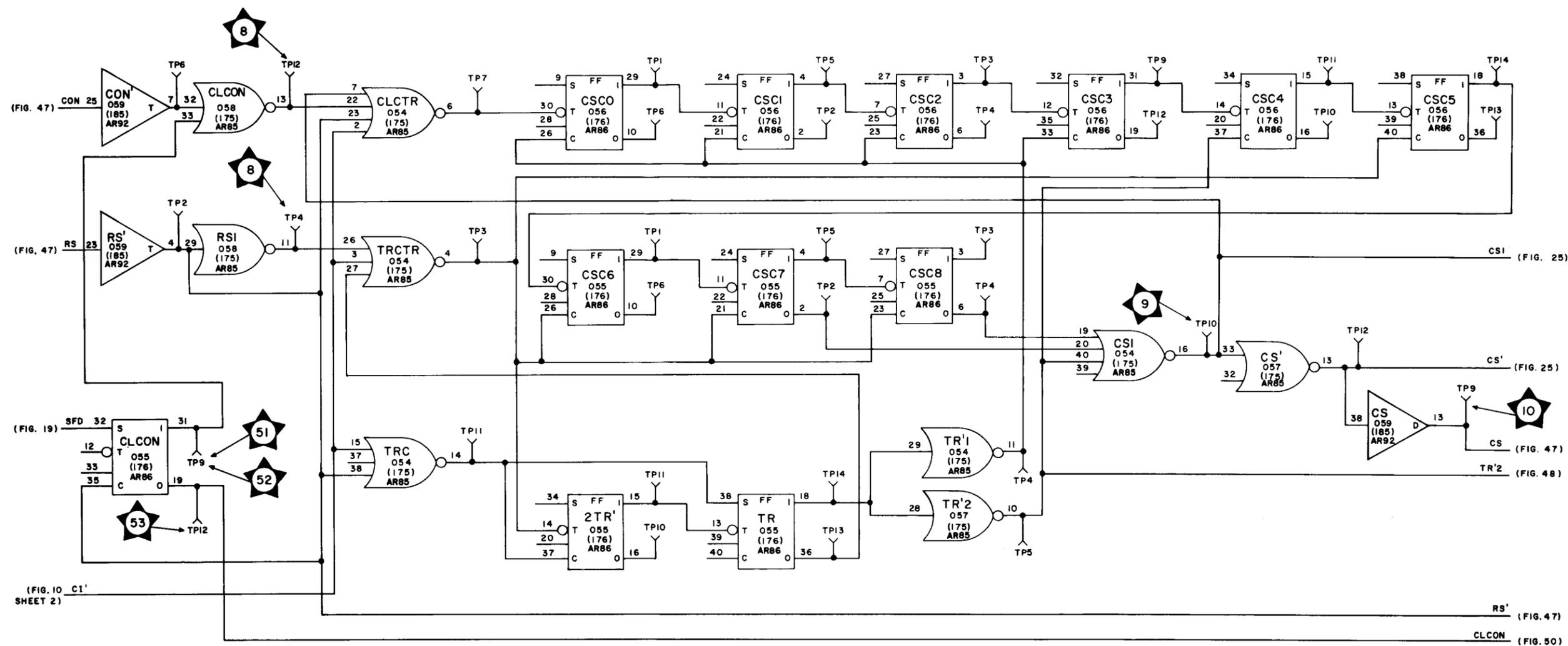


Fig. 13— Transmitter Control Timing Circuits, Functional Schematic

TEST 4 — CLOCK SPEED SELECT CIRCUITS

9.22 The clock speed select circuits provide control signals required by the data set transmitter and receiver for various modes of operation. Voltage and waveform requirements shown in Fig. 14 through Fig. 18 are keyed to the functional schematic diagram shown in Fig. 19.

Note: Speed selection requirements noted by waveform "CONDITIONS" must be accomplished by using the ATT-UNATT switch on the 901B-2 test set together with proper connections on the interface adapter.

CONDITIONS: Adjust oscilloscope to trigger on the rise of DTI. Position the ATT-UNATT switch on the 901B-2 test set to UNATT.

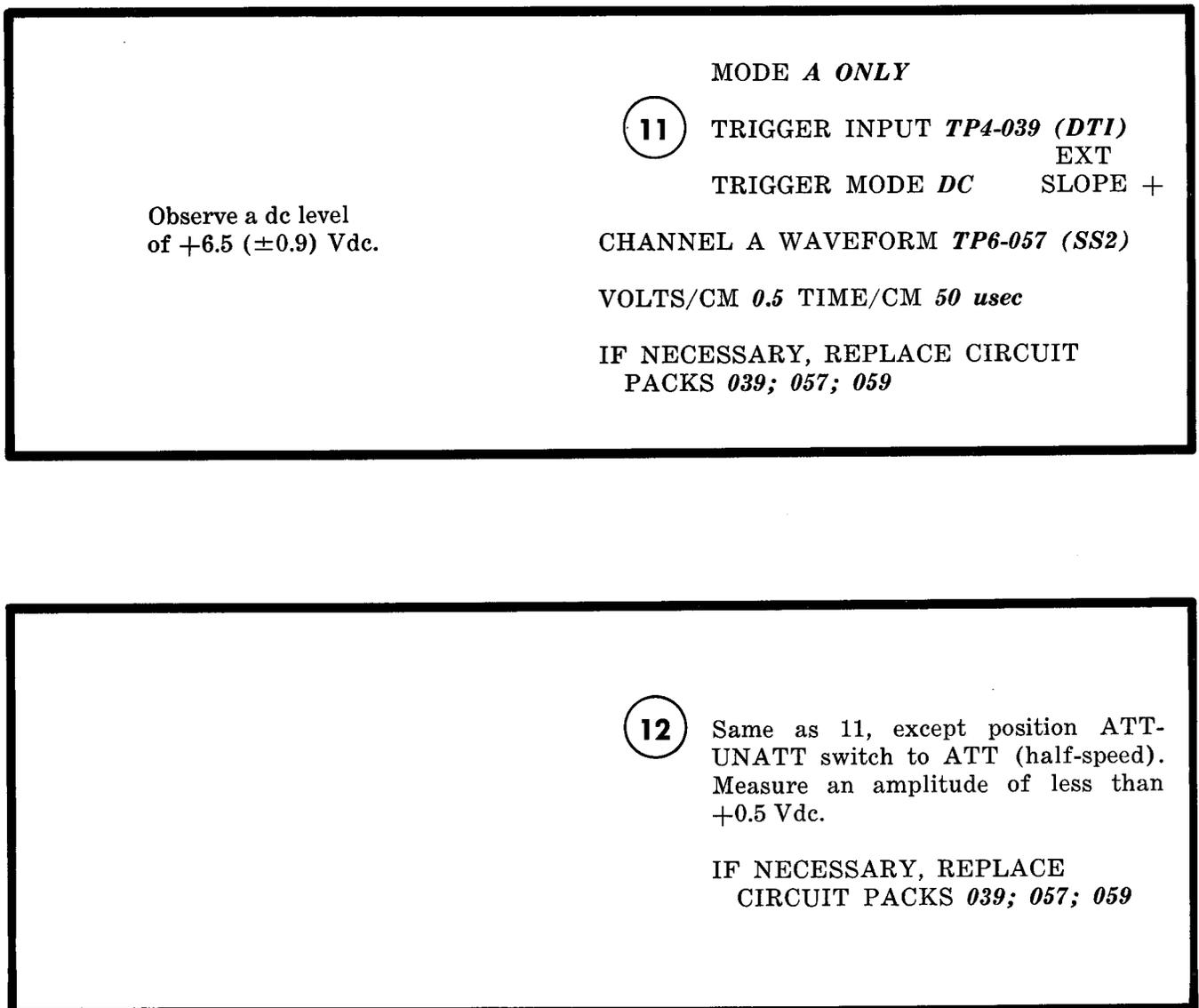
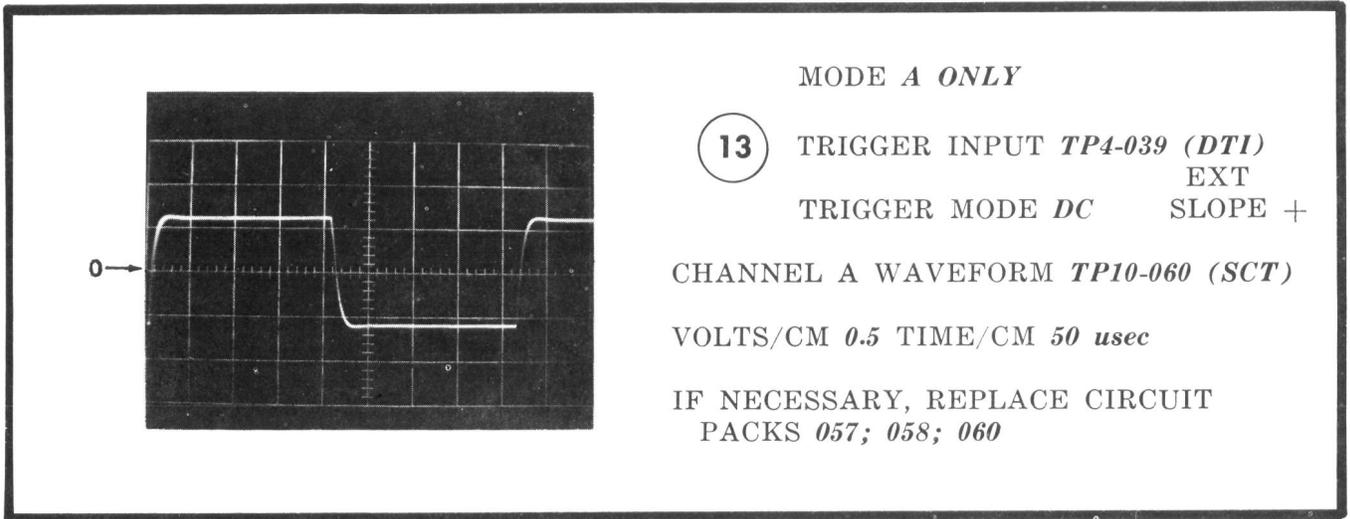


Fig. 14 — Clock Speed Select Circuit Test

CONDITIONS: Adjust oscilloscope to trigger on the rise of DTI. Position ATT-UNATT switch on the 901B-2 test set to UNATT.



CONDITIONS: Same as 13, except position ATT-UNATT switch on the 901B-2 to ATT.

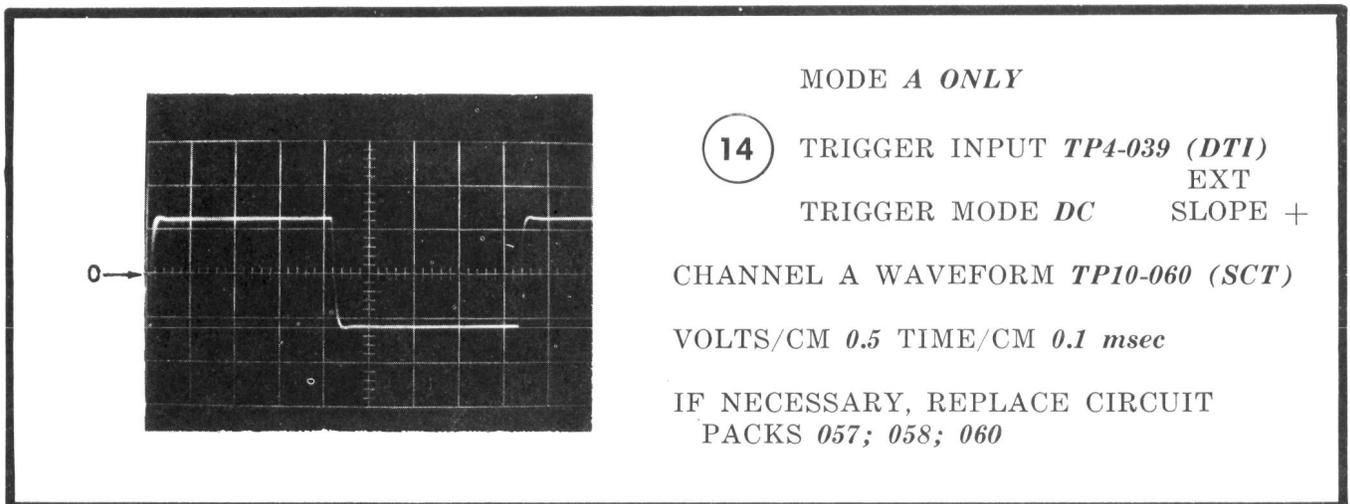
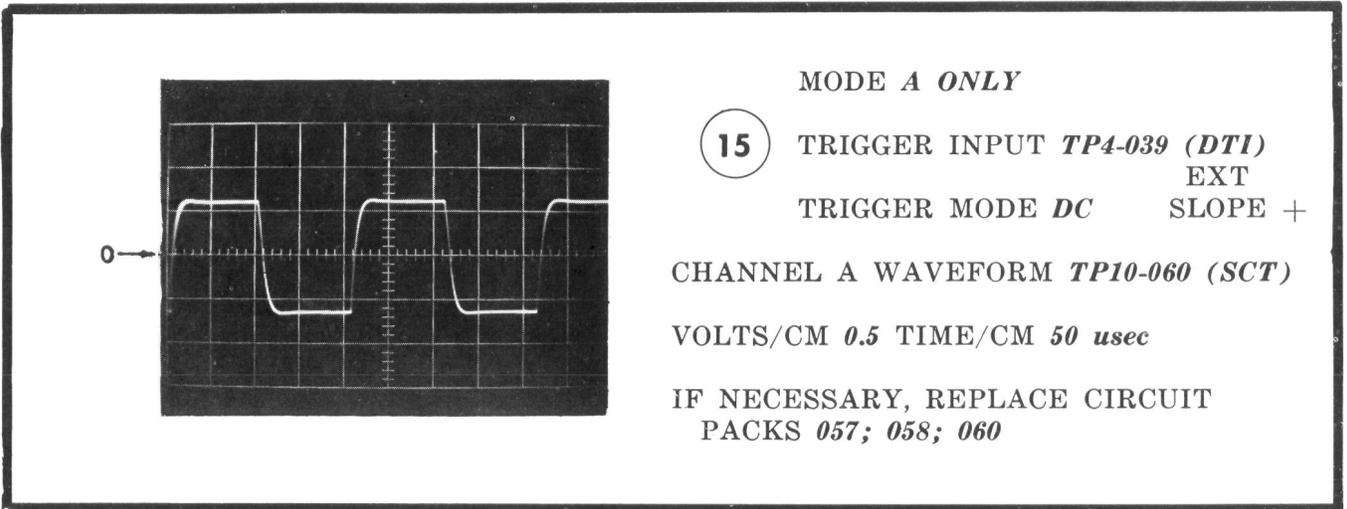


Fig. 15 — Clock Speed Select Circuit Test

CONDITIONS: Same as 14, except strap between terminals 7 and EQ 14 on the interface adapter. Same waveform as in 13, with TIME/CM 50 μ sec. After waveform is obtained, position ATT-UNATT switch on the 901B-2 to UNATT and observe waveform shown below.



CONDITIONS: Adjust oscilloscope to trigger on the rise of DR. Terminals 7 and EQ 14 on the interface adapter strapped. ATT-UNATT switch on the 901B-2 test set to UNATT.

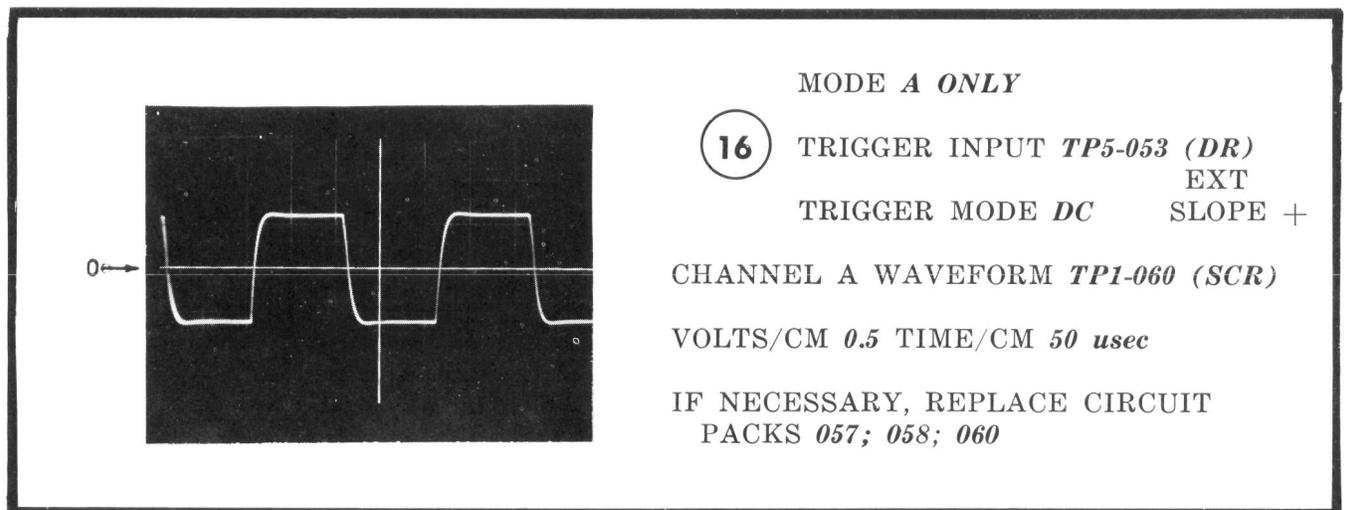
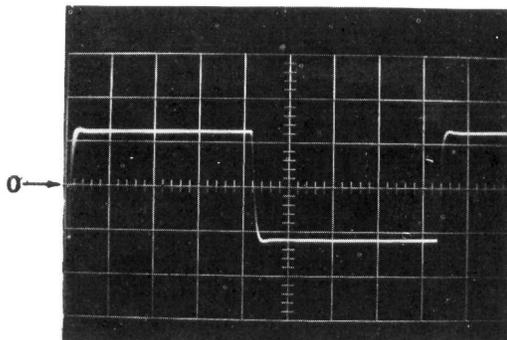


Fig. 16 — Clock Speed Select Circuit Test

- 17 Same as 16, except position ATT-UNATT switch to ATT (half-speed). Waveform should be similar to Test 13.

IF NECESSARY, REPLACE
CIRCUIT PACKS 057; 058; 060

CONDITIONS: Adjust oscilloscope to trigger on the rise of DR. Remove the strap on terminals 7 and EQ 14 on the interface adapter.



MODE A ONLY

- 18 TRIGGER INPUT TP5-053 (DR)
EXT
TRIGGER MODE DC SLOPE +

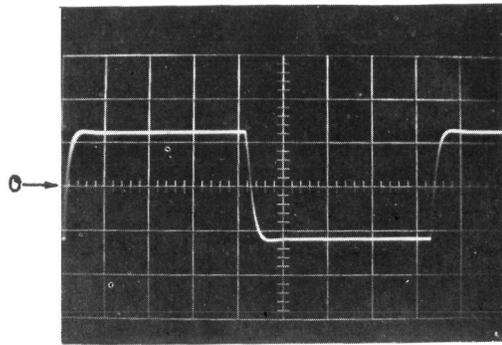
CHANNEL A WAVEFORM TP1-060 (SCR)

VOLTS/CM 0.5 TIME/CM 0.1 msec

IF NECESSARY, REPLACE CIRCUIT
PACKS 057; 058; 060

Fig. 17 — Clock Speed Select Circuit Test

CONDITIONS: Adjust oscilloscope to trigger on the rise of DR. Position ATT-UNATT switch on the 901B-2 to UNATT.



MODE *A ONLY*

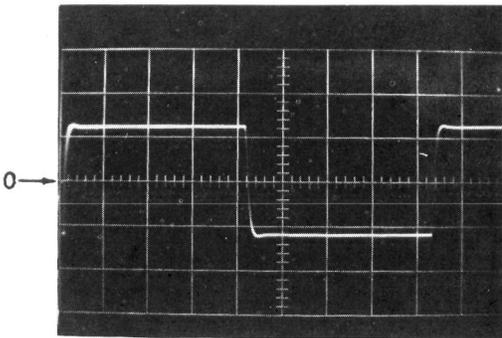
19 TRIGGER INPUT *TP5-053 (DR)*
EXT
TRIGGER MODE *DC* SLOPE +

CHANNEL A WAVEFORM *TP1-060 (SCR)*

VOLTS/CM *0.5* TIME/CM *50 usec*

IF NECESSARY, REPLACE CIRCUIT
PACKS *057; 058; 060*

CONDITIONS: Adjust oscilloscope to trigger on the rise of DR. On the interface adapter, remove the strap between 10 and EQ 11 and strap terminals 9 and EQ 11.



MODE *A ONLY*

20 TRIGGER INPUT *TP5-053 (DR)*
EXT
TRIGGER MODE *DC* SLOPE +

CHANNEL A WAVEFORM *TP1-060 (SCR)*

VOLTS/CM *0.5* TIME/CM *0.1 msec*

IF NECESSARY, REPLACE CIRCUIT
PACKS *009; 057; 058; 060*

After the tests are complete, remove the strap between terminals 9 and EQ 11 on the interface adapter and strap terminals 10 and EQ 11.

Note: If SCR/DD trouble cannot be corrected by replacing circuit packs, proceed to TEST 8 — RECEIVER TIMING.

Fig. 18 — Clock Speed Select Circuit Test

TEST 5 — DATA TRANSMITTER

9.23 The data transmitter encodes serial binary data as a band-limited signal suitable for transmission over telephone lines.

9.24 Waveform requirements shown in Fig. 20 through Fig. 24 are keyed to the functional schematic shown in Fig. 25. The waveforms are examples of normal operation for various modes in which the transmitter may be used.

CONDITIONS: Adjust oscilloscope to trigger on the rise of DTI. Set B TEST switch on the 901B-2 test set to position 3. Set ATT-UNATT switch to ATT.

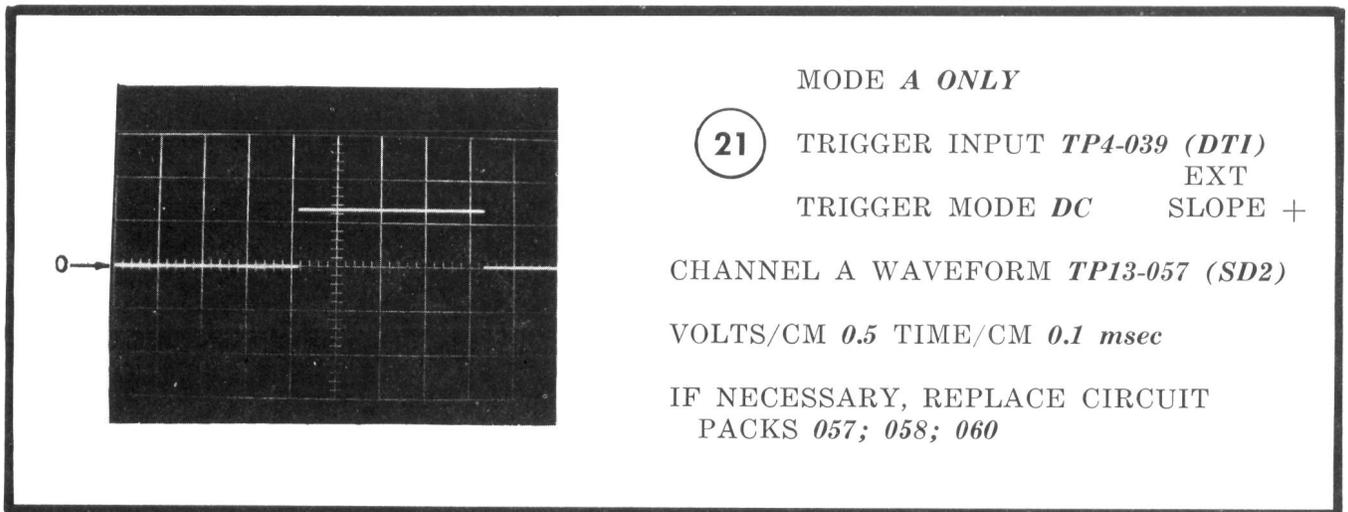
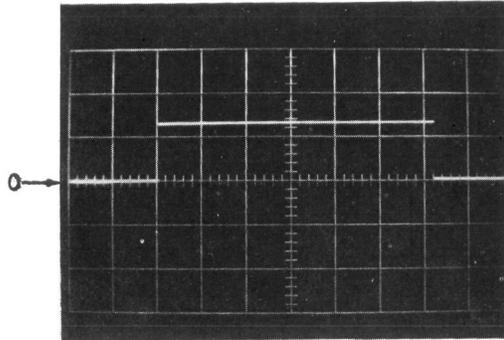


Fig. 20 — Data Transmitter Test

CONDITIONS: Adjust oscilloscope to trigger on the rise of E. Position ATT-UNATT switch to UNATT. Position B TEST switch to OFF.



MODE A ONLY

22 TRIGGER INPUT *TP3-040 (E)*
EXT
TRIGGER MODE *DC* SLOPE +

CHANNEL A WAVEFORM *TP13-057 (SD2)*

VOLTS/CM *0.5* TIME/CM *0.2 msec*

IF NECESSARY, REPLACE CIRCUIT
PACKS *057; 058*

CONDITIONS: Set B TEST switch on the 901B-2 test set to position 4. Adjust oscilloscope to trigger on the rise of E.

MODE A ONLY

23 TRIGGER INPUT *TP3-040 (E)*
EXT
TRIGGER MODE *DC* SLOPE +

Observe a dc level
of $+6.5 (\pm 0.9)$ Vdc.

CHANNEL A WAVEFORM *TP13-057 (SD2)*

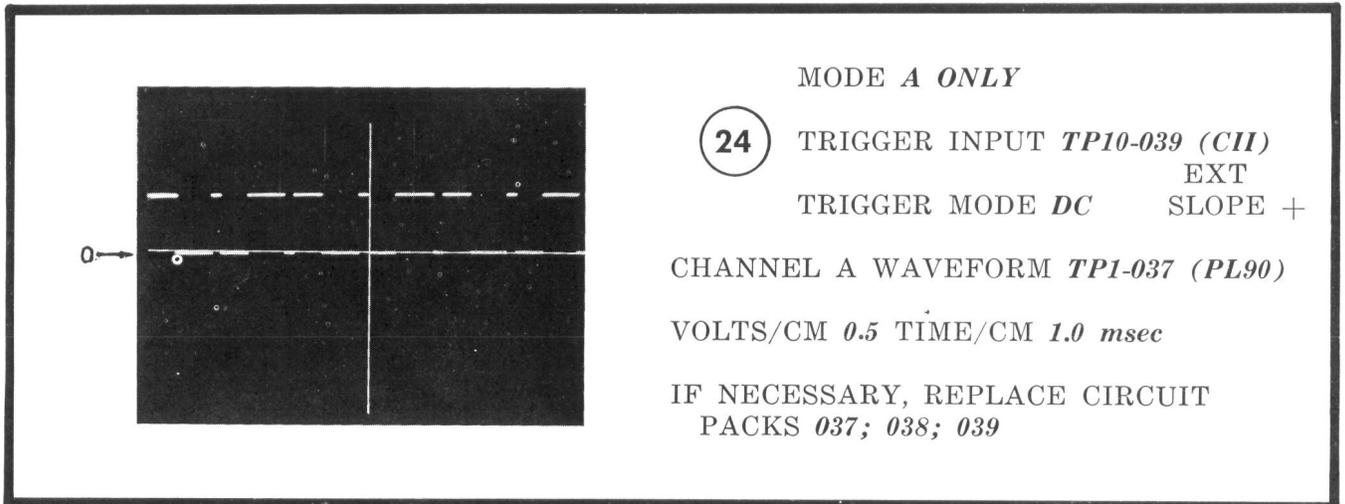
VOLTS/CM *0.5* TIME/CM *0.2 msec*

IF NECESSARY, REPLACE CIRCUIT
PACKS *057; 058; 060*

Fig. 21 — Data Transmitter Test

Note: Waveforms shown for Tests 24 and 25 are interchangeable. For both tests, either waveform is correct.

CONDITIONS: Adjust the oscilloscope to trigger on the rise of CII.



CONDITIONS: Same as 24, except set B TEST switch on the 901B-2 to position 3.

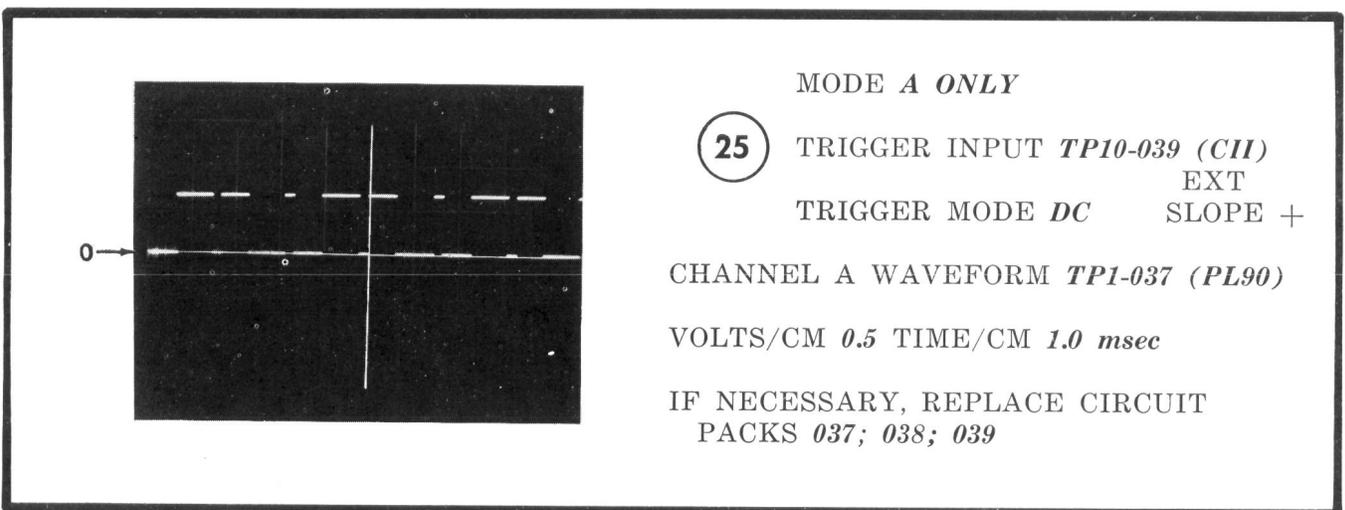
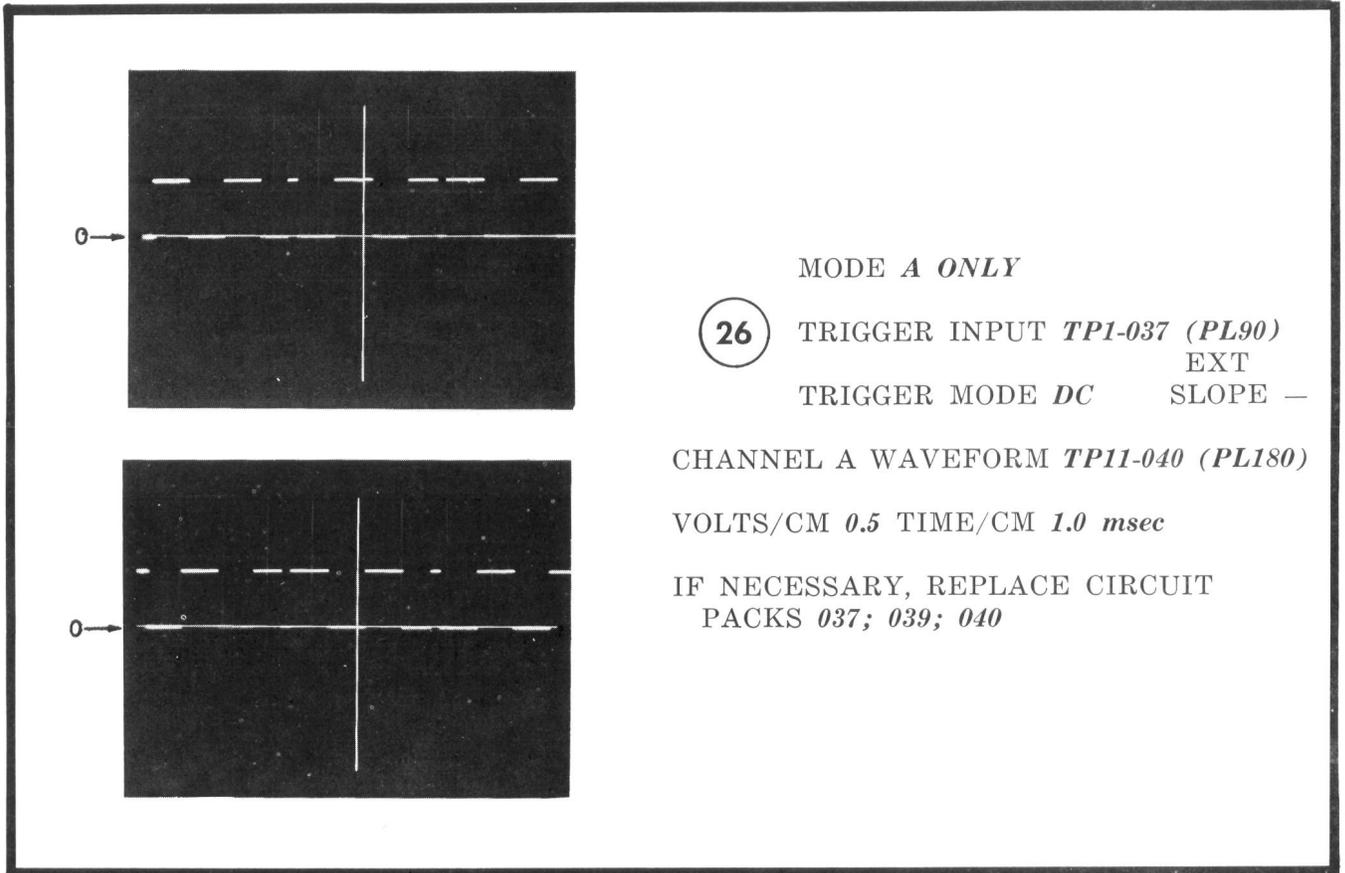


Fig. 22 — Data Transmitter Test

CONDITIONS: Set B TEST switch on the 901B-2 test set to position 5. Adjust oscilloscope to trigger on the fall of PL90. Either waveform is correct.



CONDITIONS: Position the B TEST switch on the 901B-2 test set to OFF. Ground both TP11-040 (PL180) and TP1-037 (PL90). Adjust oscilloscope to trigger on the rise of E.

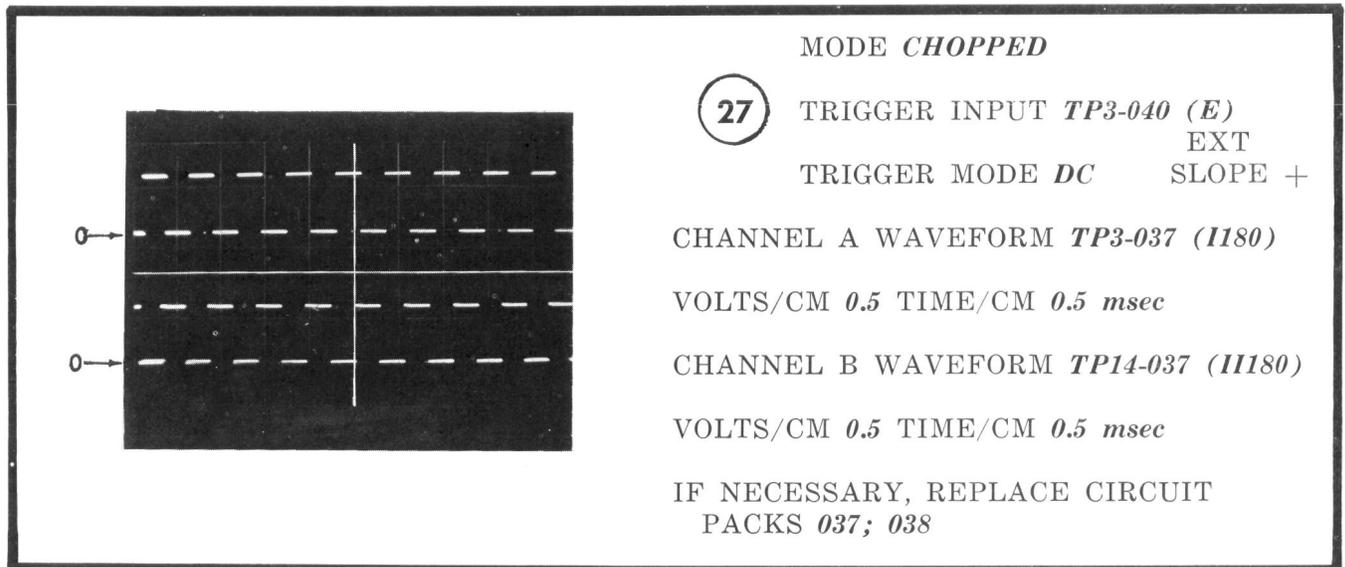
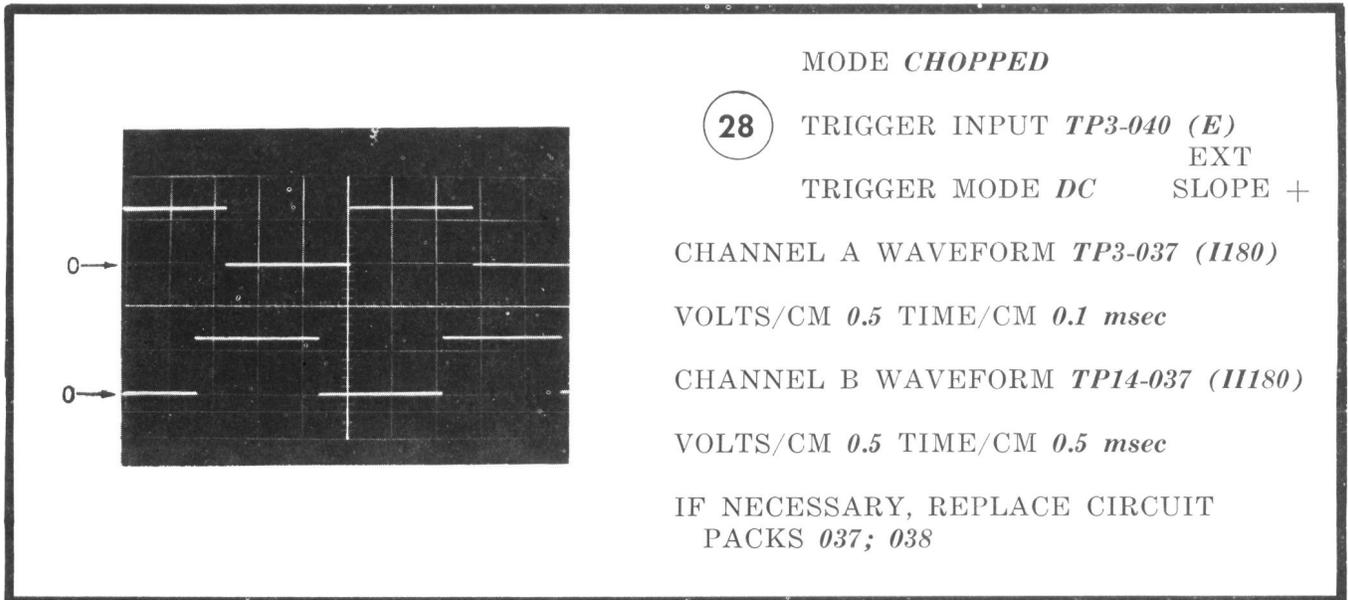


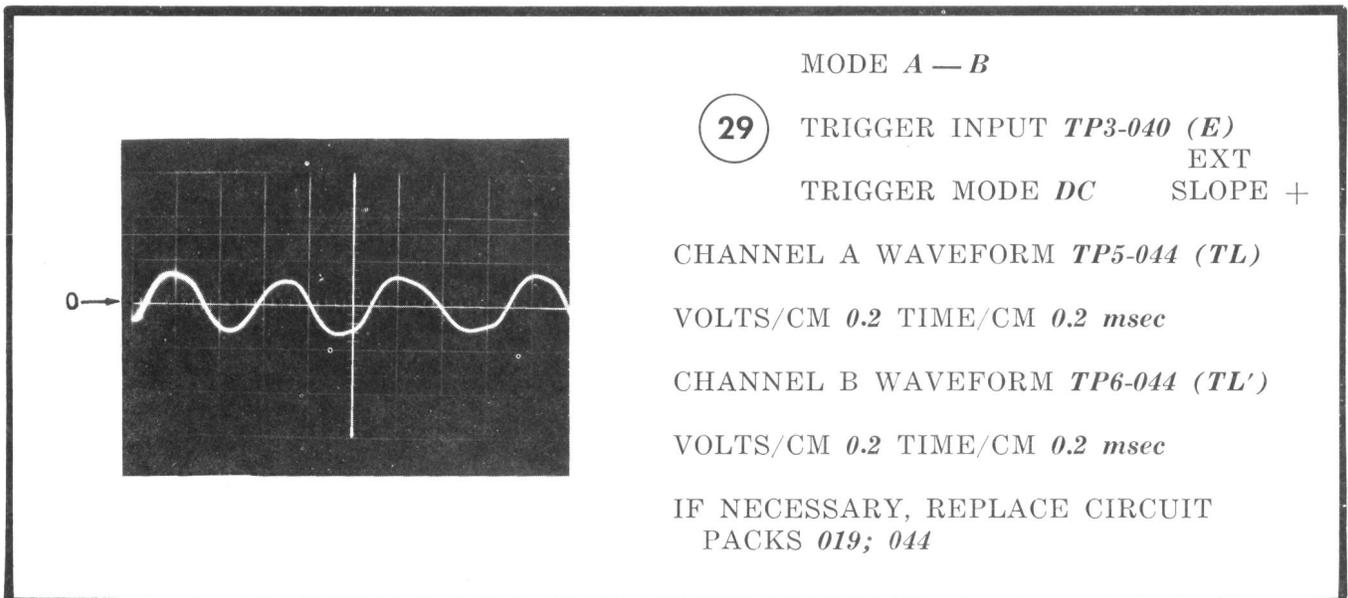
Fig. 23 — Data Transmitter Test

CONDITIONS: Same as 27, except remove grounds from both TP11-040 (PL180) and TP1-037 (PL90). Then ground TP10-040 (PL180') and TP6-037 (PL90').



CONDITIONS: Adjust oscilloscope to trigger on the rise of E.

Note: The waveform below is for strapping between terminals 1 and 4 on circuit pack in slot location 044. Other strapping will result in less amplitude.



After testing, remove ground from both TP10-040 (PL180') and TP6-037 (PL90') and position MODE switch to A ONLY.

Fig. 24 — Data Transmitter Test

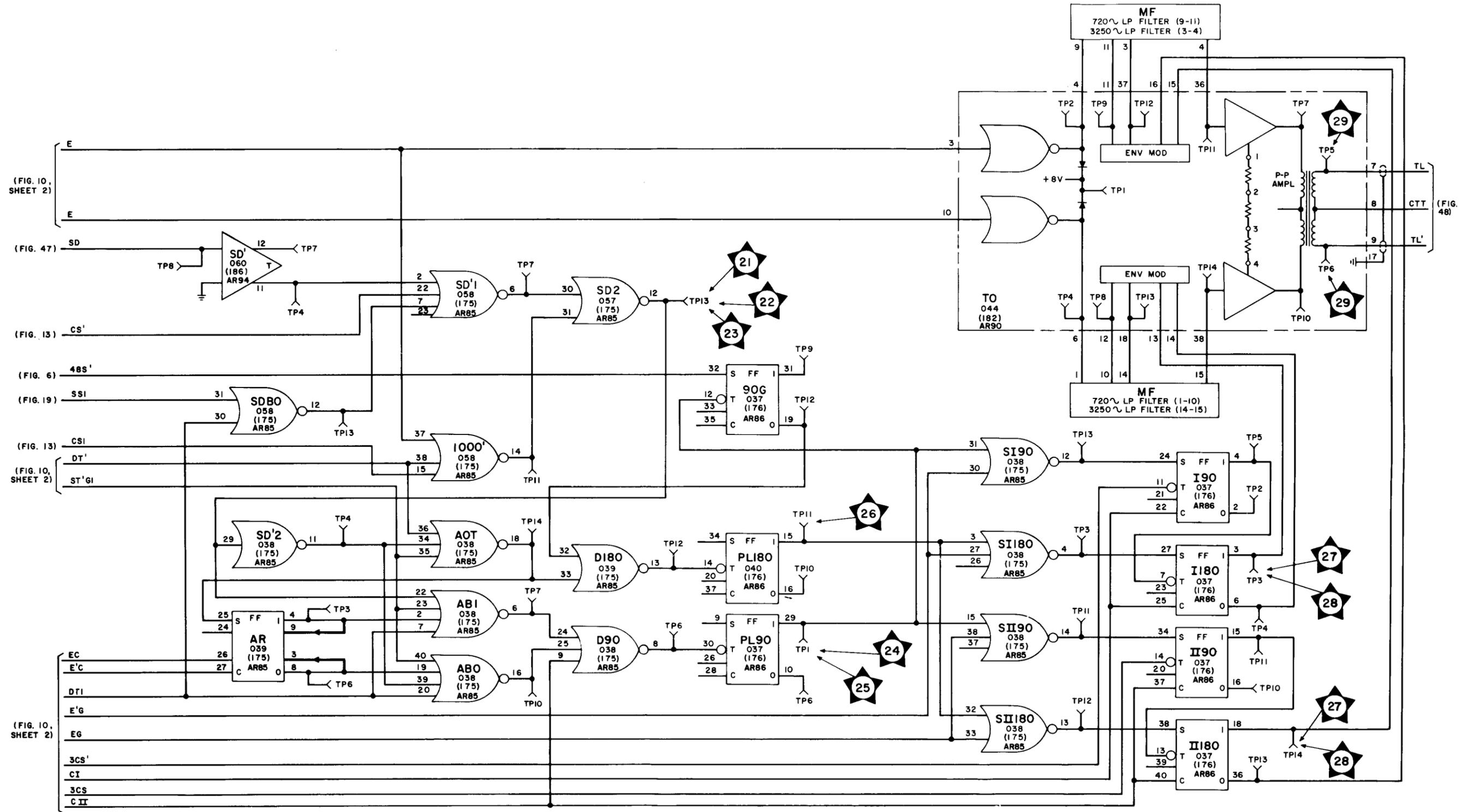


Fig. 25 — Data Transmitter Circuits, Functional Schematic

TEST 6 — TRANSMIT RECEIVE SWITCH (TR-SW)

9.25 The transmit-receive switch controls the application of transmit line signals through an electronic switch when the carrier is controlled by request-to-send (RS/CA). The data set receiver is always connected to the receive line pair through the transmit-receive switch circuit components.

9.26 The waveform requirements shown in Fig. 26, Step 30 displays bandpass filter output under test conditions.

Note: The waveform shown is for 1 to 4 strapping on circuit pack in slot location 044. Other strapping will result in less amplitude.

CONDITIONS: Set B TEST switch on the 901B-2 test set to position 5.

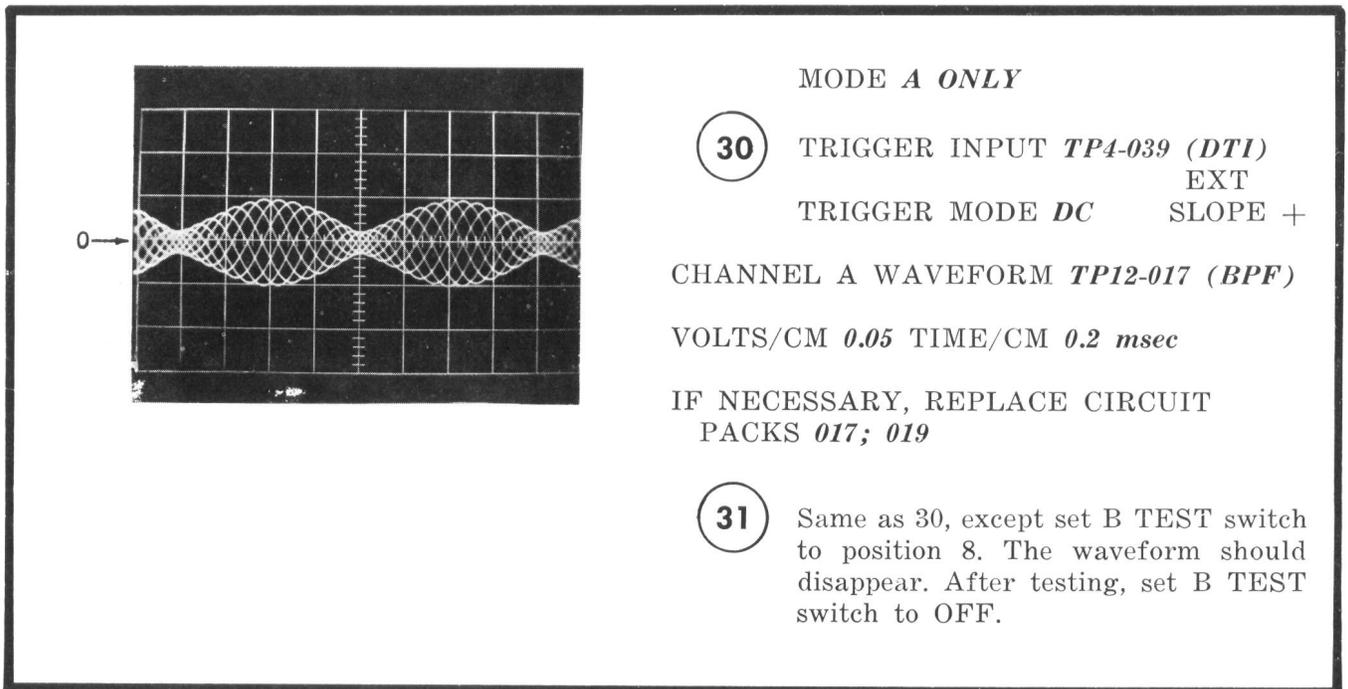


Fig. 26 — Transmit-Receive Switch Test

TEST 7 — ANALOG RECEIVER

9.27 The analog receiver circuits both amplify the band-limited line signal to a fixed amplitude and convert the received signal into two parallel signals which constitute the A and B bits of received serial binary data.

9.28 Voltage and waveform requirements shown in Fig. 27 through Fig. 29 are keyed to the functional schematic shown in Fig. 30. The waveforms are examples of normal operation for various code combinations the receiver will convert.

CONDITIONS: Set B TEST switch on the 901B-2 to position 5. Adjust oscilloscope to trigger on the rise of DTI.

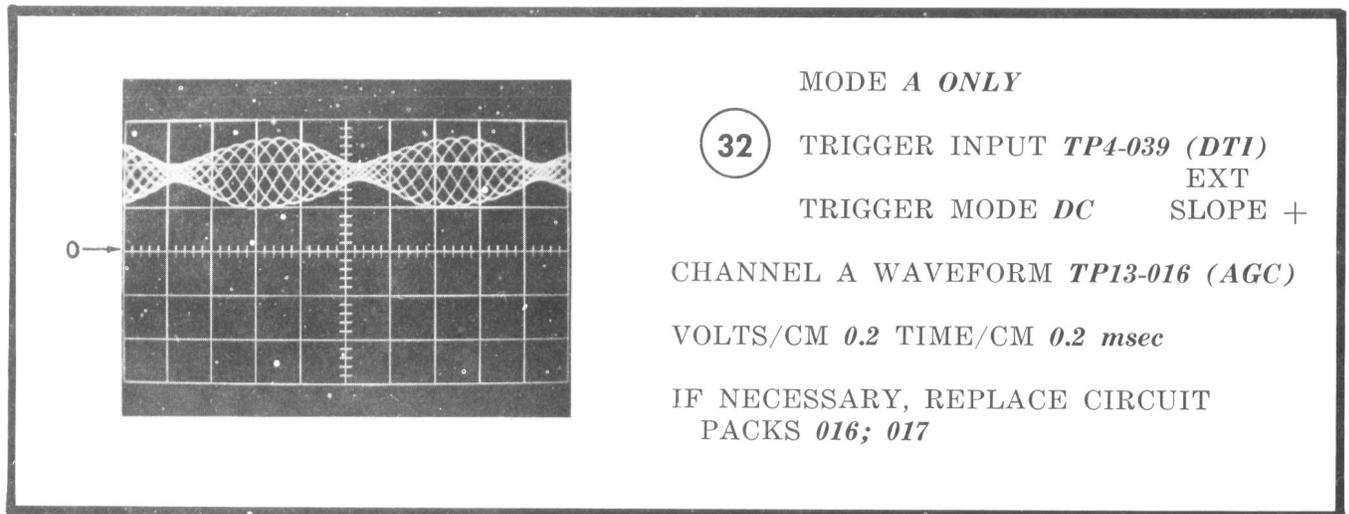


Fig. 27 — Analog Receiver Test

33

- (1) Condition the KS-14510 test meter to measure on the 12-volt dc scale.
- (2) Connect positive lead to *TP10-059 (COO)* and negative lead to ground. Reading shall be $+7.0 (\pm 1.3)$ Vdc.
- (3) Remove test leads. Proceed to Test 34.

34

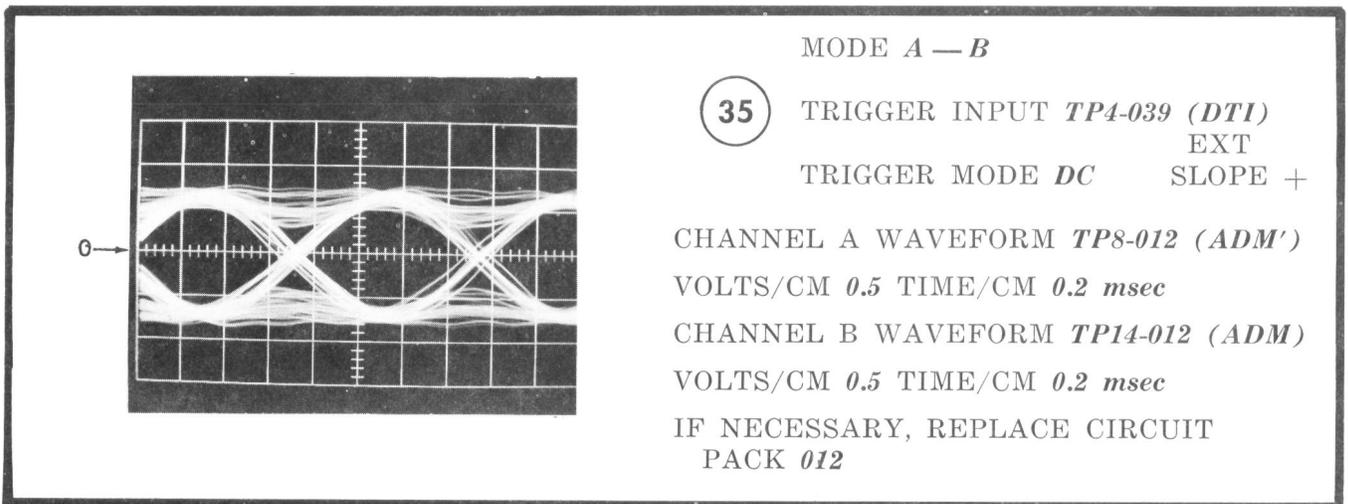
- (1) Operate LINE-TEST key to LINE position.
- (2) Connect the negative lead to *TP10-059 (COO)* and the positive lead to ground. Reading shall be $-6.5 (\pm 1.3)$ Vdc.
- (3) Replace circuit packs 007, 008, 009, 016, 017, 059 if proper results are not obtained.
- (4) Remove test meter leads and position B TEST switch to OFF.
- (5) Operate LINE-TEST key to TEST position.

Fig. 28 — Analog Receiver Test

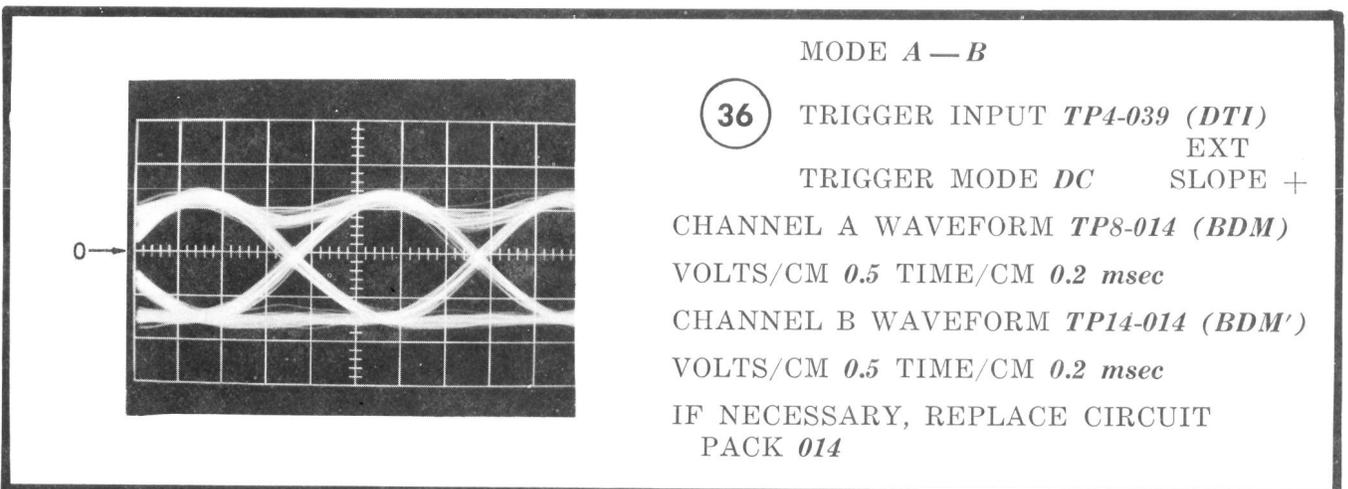
CONDITIONS: Adjust the oscilloscope to trigger on the rise of DTI. Condition external test equipment as follows:

Note: In the following connections, strap red to red and black to black.

- (1) Connect EXT CLOCK terminals on the 903B test set to TRANSMIT CLOCK terminals on the 901B-2 test set.
- (2) Connect SIGNAL OUT terminals on the 903B test set to TRANSMIT DATA terminals on the 901B-2 test set.
- (3) Position A TEST switch on the 901B-2 test set to 9.
- (4) Momentarily press START switch on the 903B test set to ensure start of the word generator.



DO NOT READJUST OSCILLOSCOPE



After completing the above tests, set the A TEST switch to OFF and remove all connections between the 901B-2 test set and the 903B test set.

Note: Failure to observe the step above will cause false indications in the following tests.

Fig. 29 — Analog Receiver Test

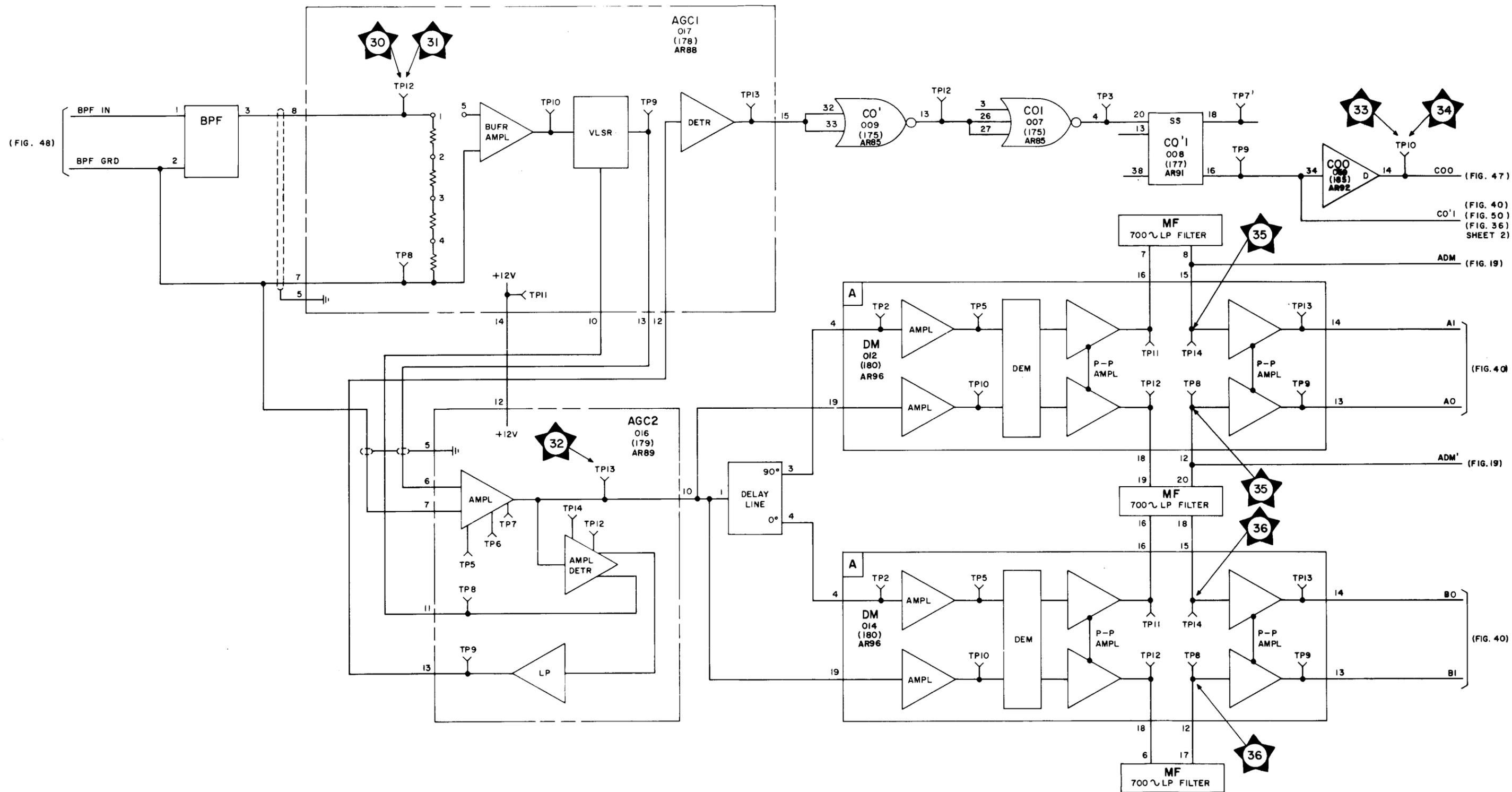
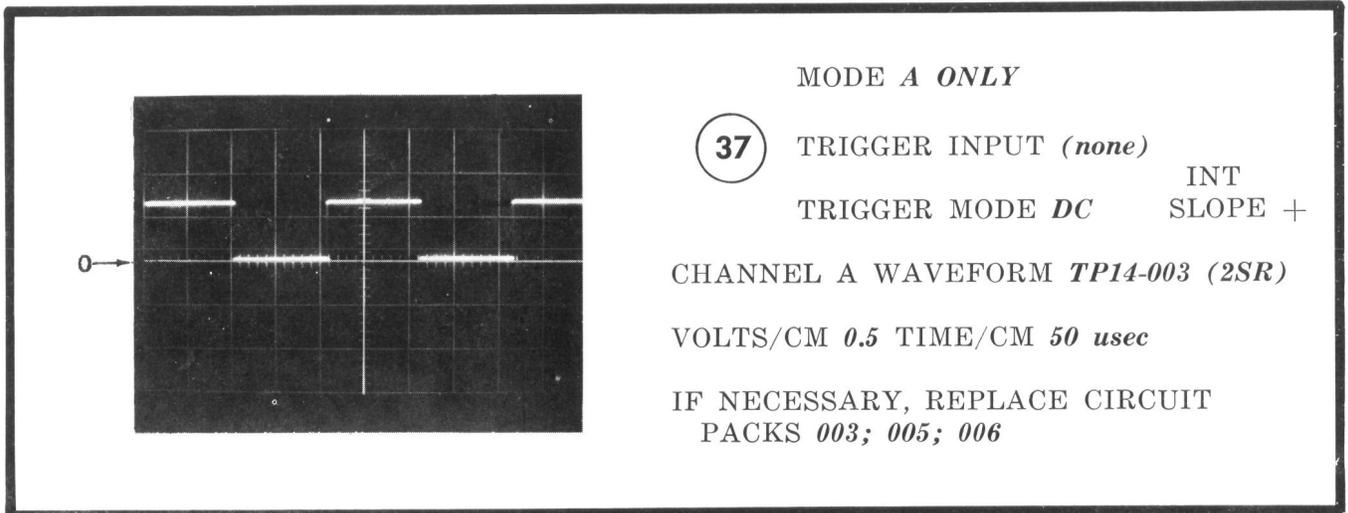


Fig. 30—Analog Receiver Circuits, Functional Schematic

TEST 8—RECEIVER TIMING

9.29 The receiver timing circuits recover synchronization timing signals required for both sampling and parallel-to-serial conversion of the received data. Waveforms shown in Fig. 31 through Fig. 35 are keyed to the functional schematic shown in Fig. 36, except Test 39 which is keyed to Fig. 40.

CONDITIONS: Ground both TP7-006 (RAD) and TP10-006 (RDL).



CONDITIONS: Same as 37, except connect and adjust oscilloscope to trigger on the rise of DR.

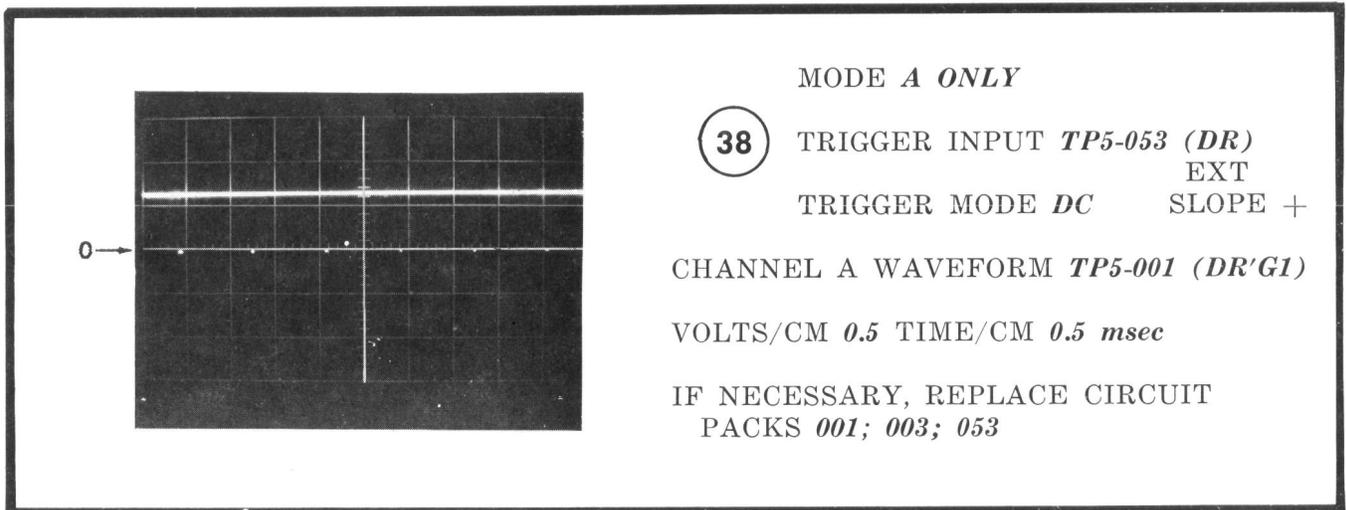
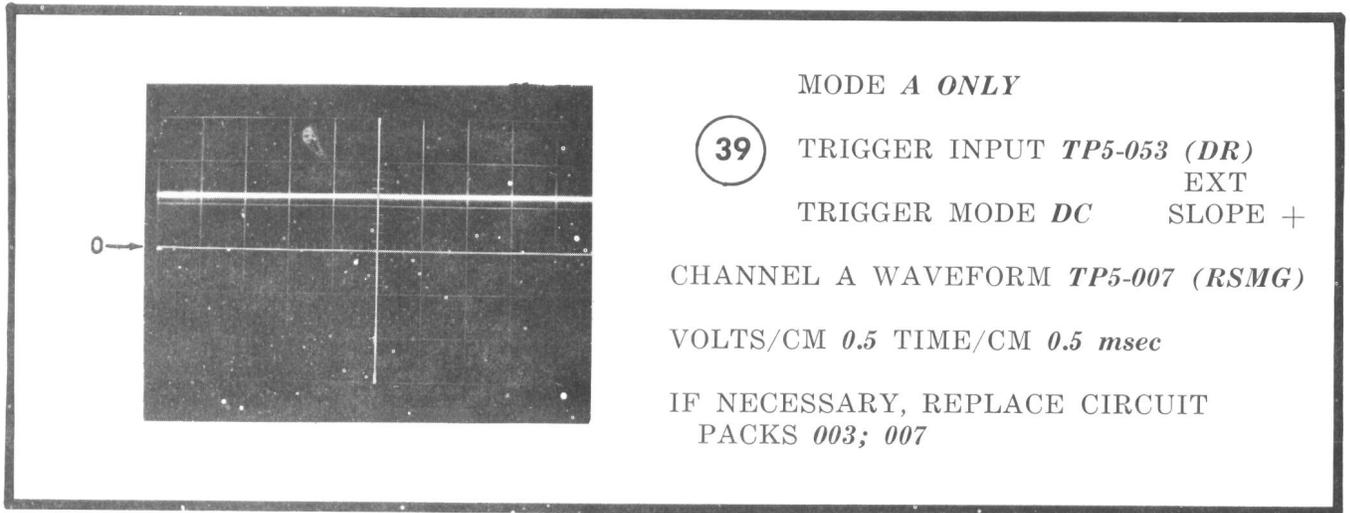


Fig. 31 — Receiver Timing Test

CONDITIONS: Same as 38.



CONDITIONS: Same as 38.

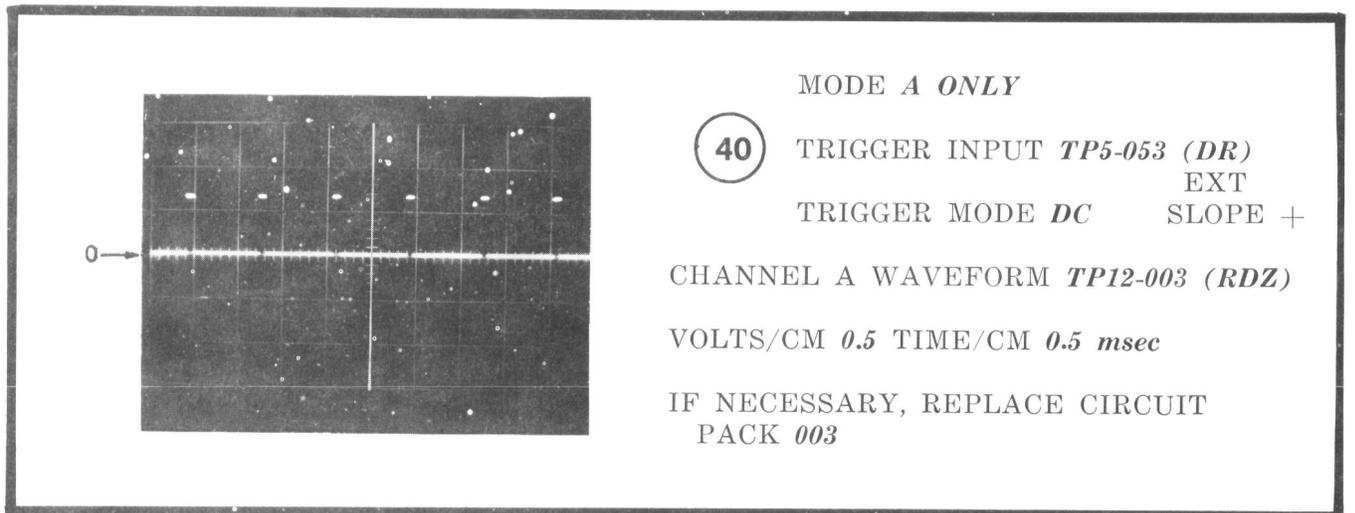
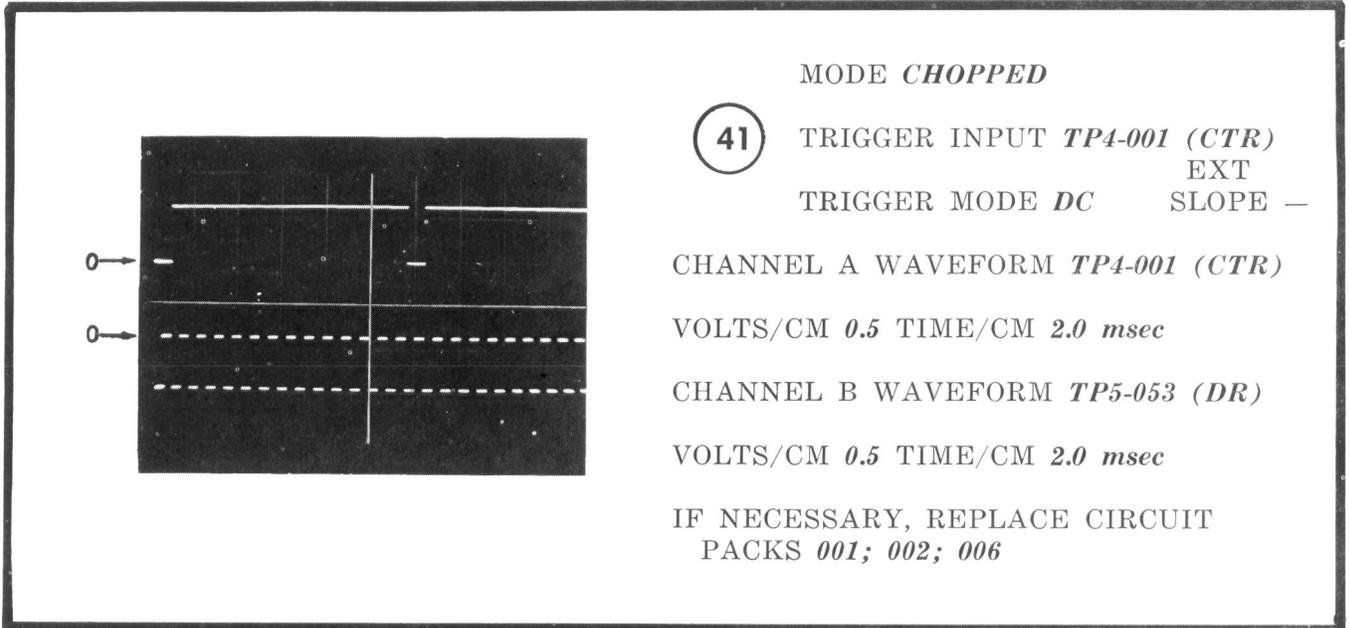


Fig. 32 — Receiver Timing Test

CONDITIONS: Same as 38, except ground both TP7-001 (RAS) and TP10-007 (RXG). Adjust oscilloscope to trigger on the fall of CTR. Set A TEST switch on the 901B-2 test set to position 9. Observe 14 cycles of DR for one cycle of CTR.



REMOVE ALL GROUND CONNECTIONS FROM CIRCUIT PACKS 001; 006; AND 007.

CONDITIONS: Ground both TP4-001 (CTR) and TP10-007 (RXG). Adjust oscilloscope to trigger on the fall of DR.

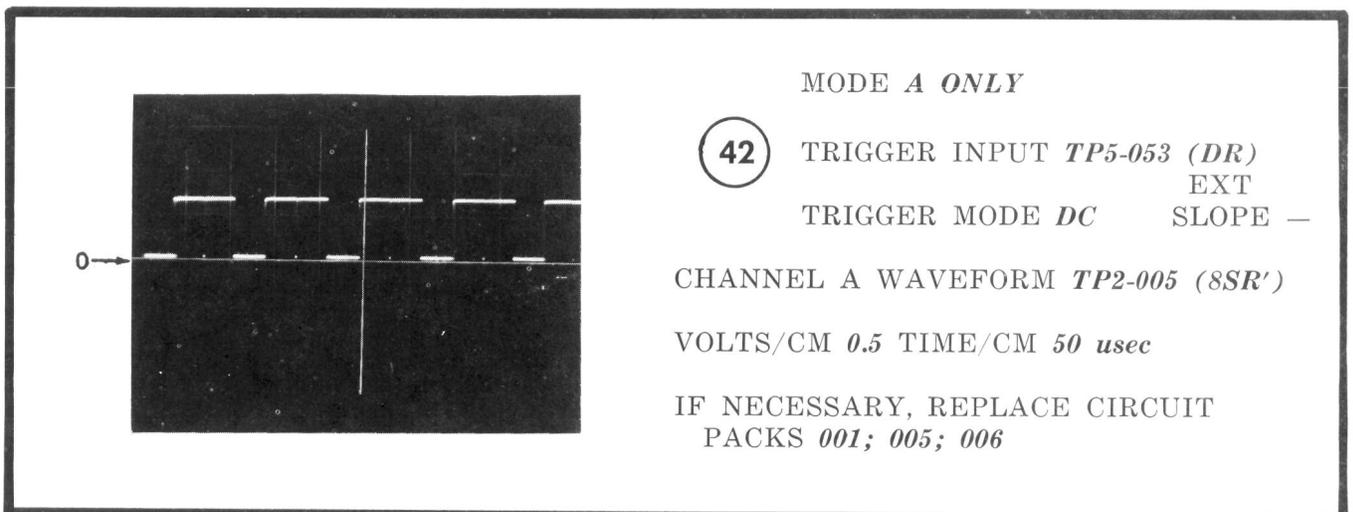
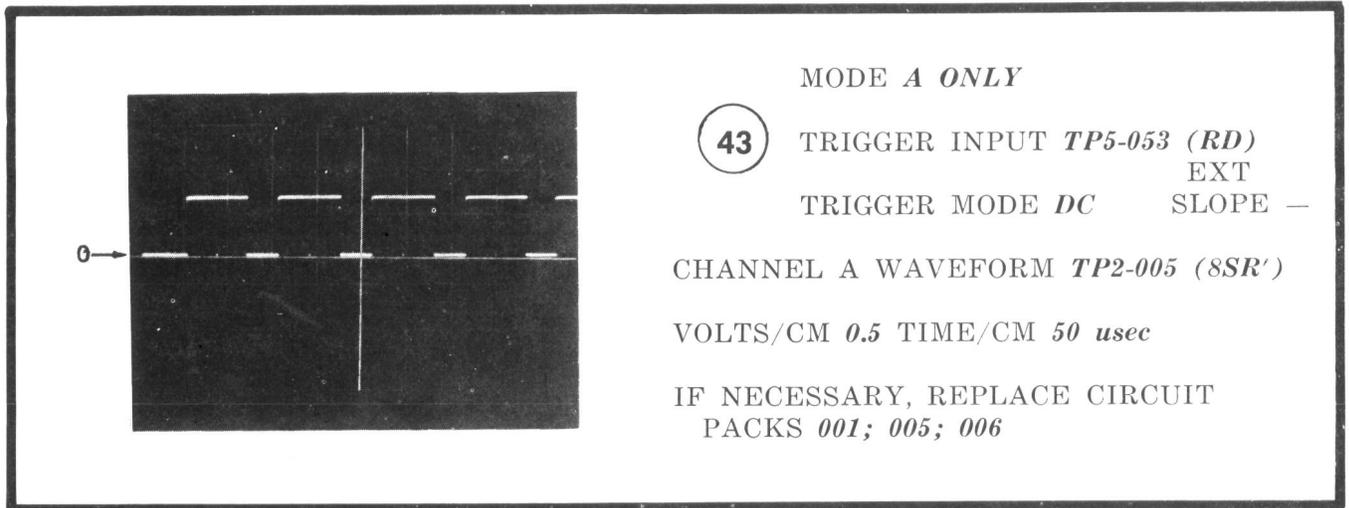


Fig. 33 — Receiver Timing Test

CONDITIONS: Same as 42, except also momentarily ground TP7-001 (RAS) while observing this waveform.



CONDITIONS: Same as 42, except also momentarily ground TP10-001 (RDS) while observing this waveform.

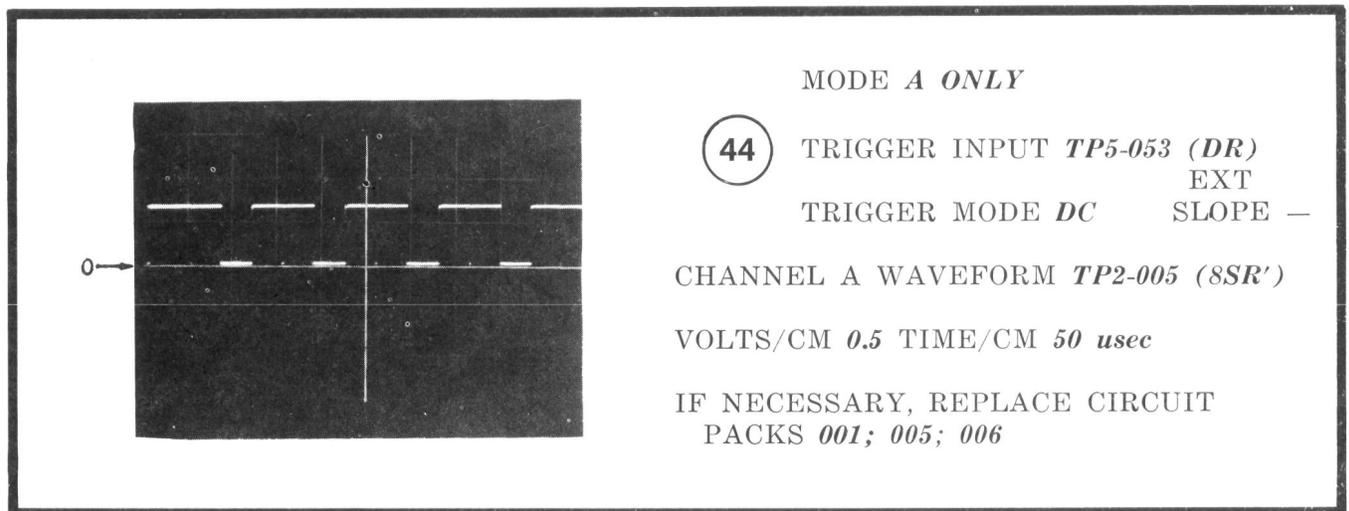
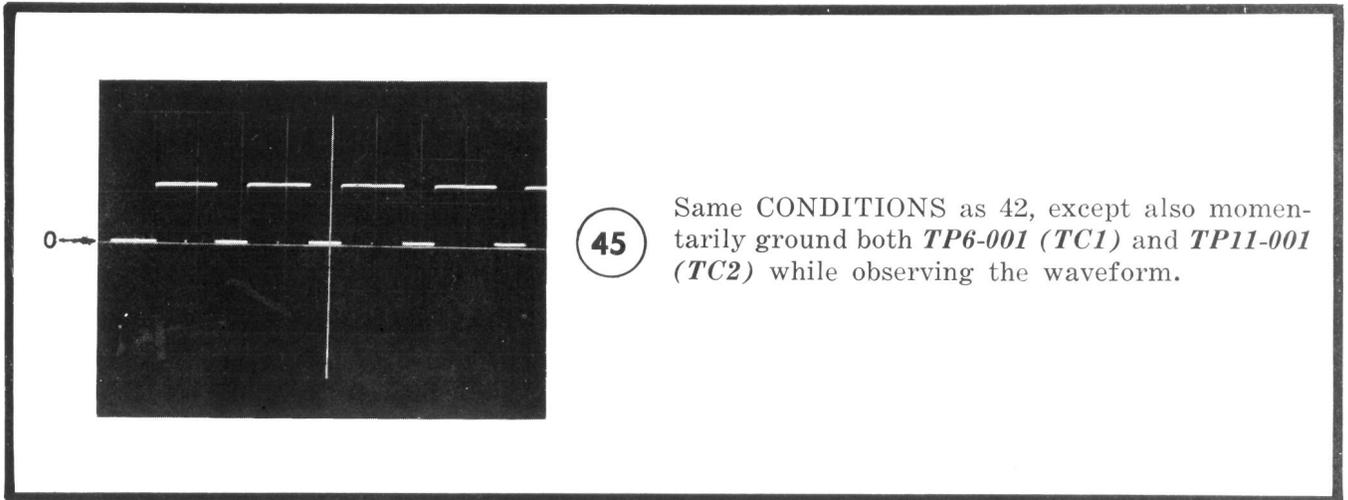


Fig. 34 — Receiver Timing Test



After testing, remove all external ground connections to circuits packs 001 and 007 and position A TEST switch on the 901B-2 test set to OFF.

Fig. 35 — Receiver Timing Test

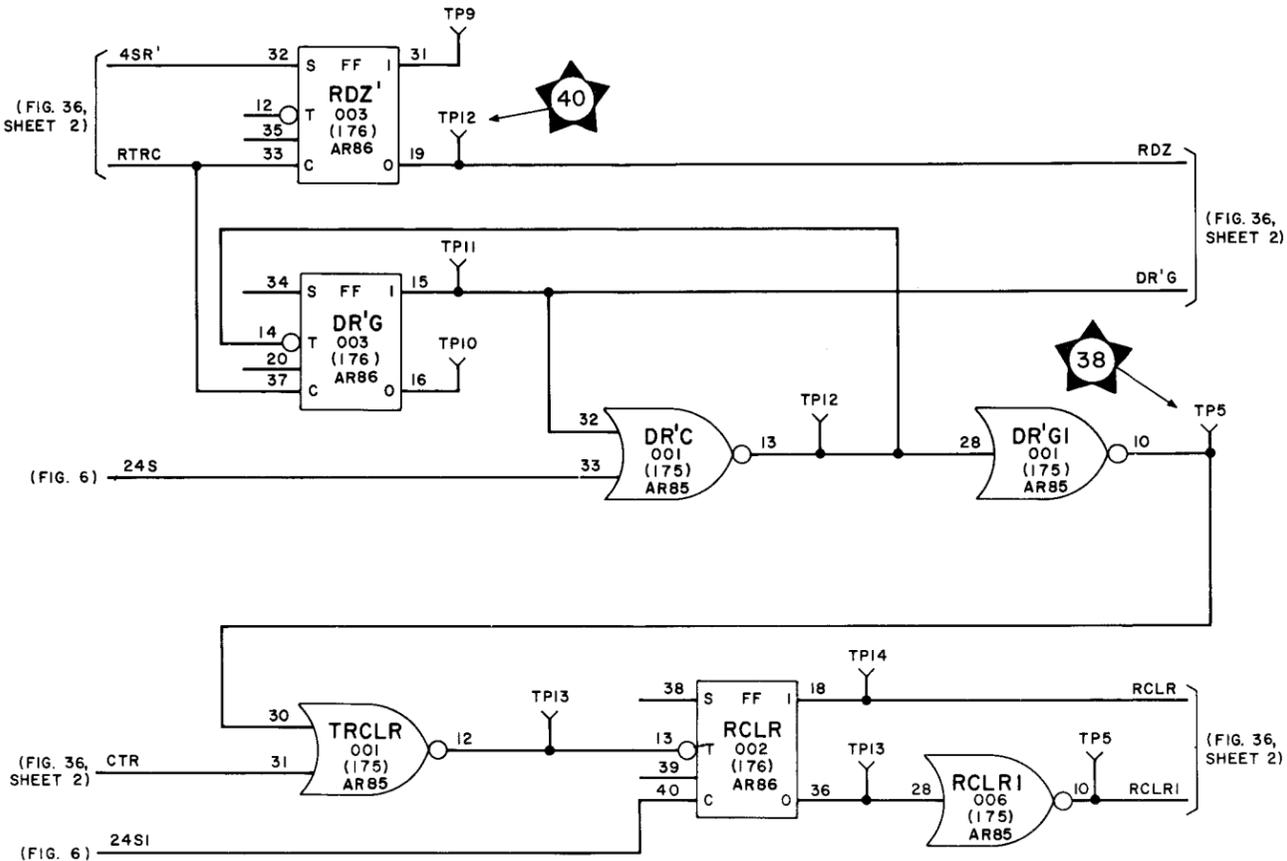
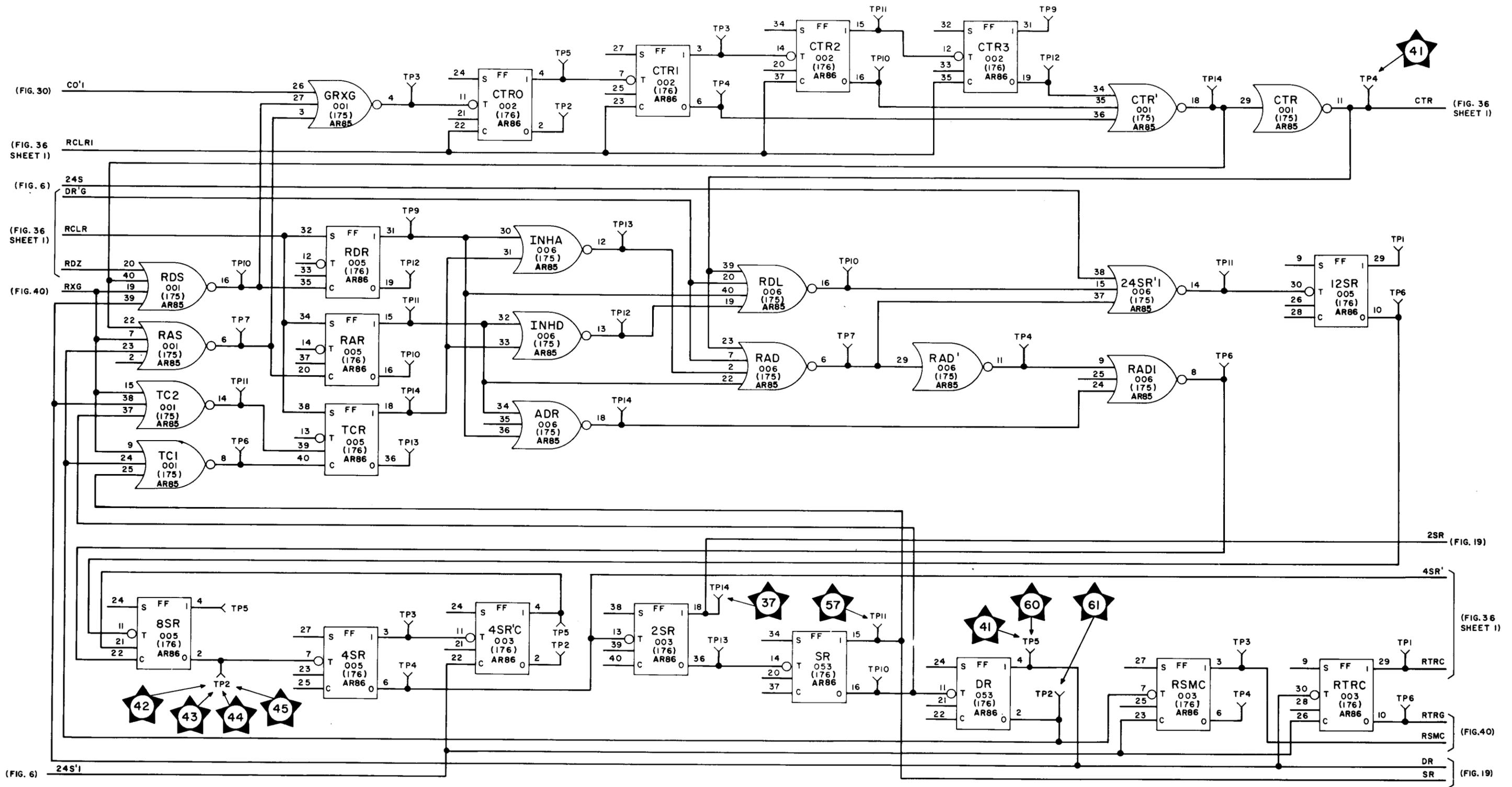


Fig. 36—Receiver Timing Circuits, Functional Schematic (Sheet 1 of 2)



TEST 9—DIGITAL DATA RECEIVER TEST

9.30 The digital data receiver converts the demodulated data waveforms into standard logic signals. These signals are generated as a serial binary data waveform acceptable to customer equipment. The digital data receiver also generates axis-crossing pulses for timing the recovery circuit operation. Waveforms shown in Fig. 37 through Fig. 39 are keyed to the functional schematic shown in Fig. 40.

9.31 Condition the data set and external test sets as follows:

Note: In the following connections, strap red to red and black to black.

- (a) Connect EXT CLOCK terminals on the 903B test set to TRANSMIT CLOCK terminals on the 901B-2 test set.
- (b) Connect SIGNAL OUT terminals on the 903B test set to TRANSMIT DATA terminals on the 901B-2 test set.
- (c) Set A TEST switch on the 901B-2 test set to position 9.
- (d) Momentarily press START switch on the 903B test set to ensure start of the word generator.

CONDITIONS: Adjust oscilloscope to trigger on the rise of DTI.

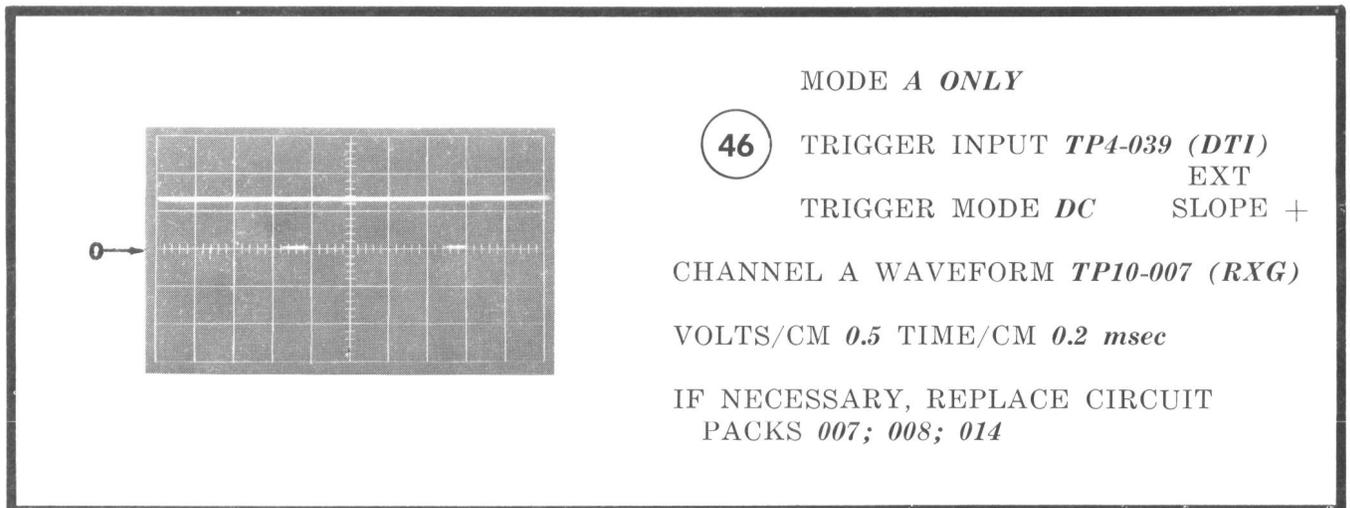


Fig. 37 — Digital Data Receiver Test

47 Same as 46, except connect Channel A oscilloscope probe to the following test points:

TP2-008 (A0P)

TP14-008 (A1P)

TP13-008 (B1P)

TP3-008 (B0P)

Observe similar but inverted waveform as in 46 at each test point.

After testing, position the A TEST switch to OFF and remove all connections between the 903B test set and the 901B-2 test set.

CONDITIONS: Set A TEST switch to position 8 and ground TP10-054 (CS) while observing waveform.

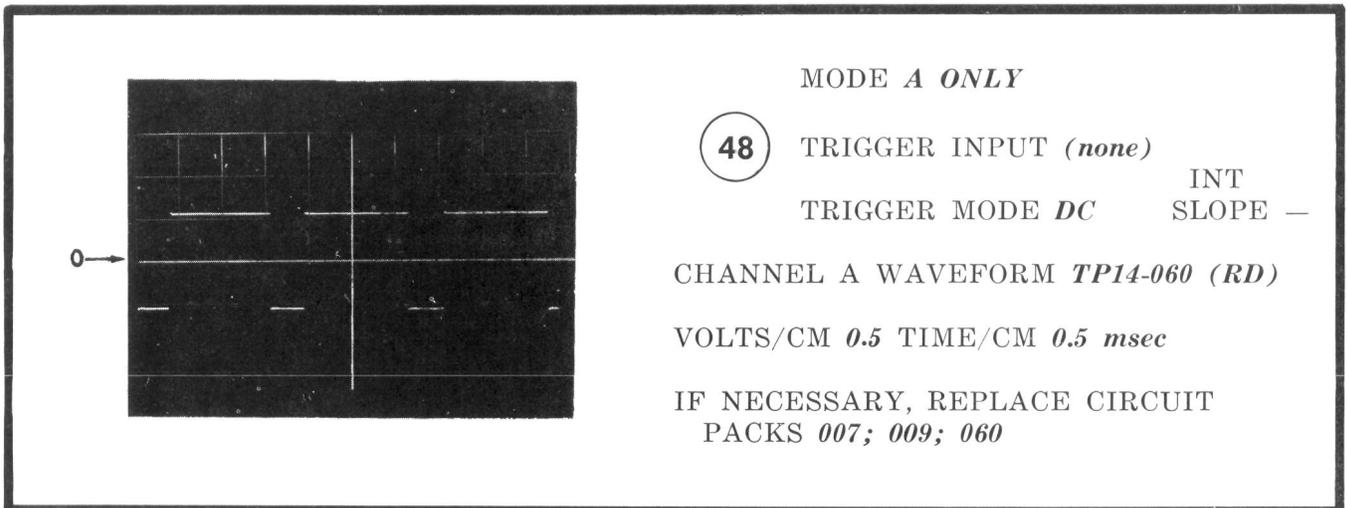
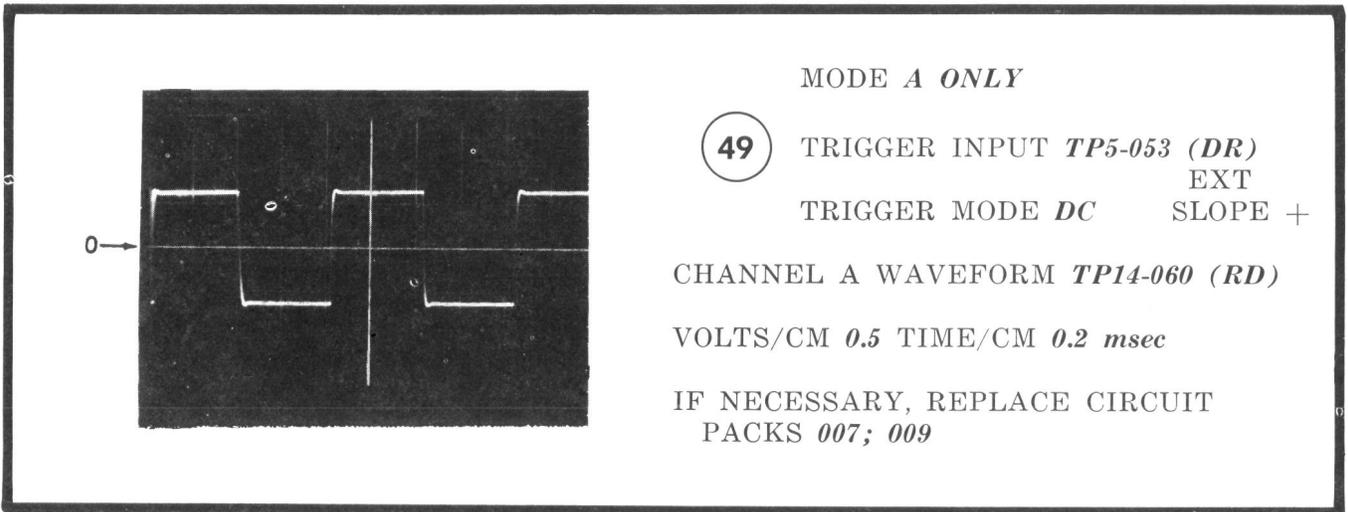


Fig. 38 — Digital Data Receiver Test

CONDITIONS: With A TEST switch set to position 8, adjust the oscilloscope to trigger on the rise of DR.



Observe a dc level
of $+6.1 (\pm 0.7)$ Vdc.

50

Same as 49 except operate the ATT-UNATT switch on the 901B-2 test set to ATT position.

After testing, position the A TEST switch to OFF and the ATT-UNATT switch to UNATT.

Fig. 39 — Digital Data Receiver Test

TEST 10 — SINGLE-FREQUENCY DETECTOR

9.32 The single-frequency detector circuits respond to the repeated 1000 synchronizing code. The detector output provides the control timing circuits with the signal required to enable and initiate clear-to-send (CS/CB) timing under the control of the confirm (CON) interface signal.

9.33 Checking the single-frequency detector operation consists of measuring the voltages required in the following tests shown in Fig. 41 and Fig.42 and which are keyed to Fig. 13.

51

- (1) Set B TEST switch on the 901B-2 to position 10.
- (2) Ground both *TP10-054 (CS/CB)* and the negative test lead of the KS-14510 test meter.
- (3) Connect the positive test meter lead to *TP9-055 (CLCON')*.
- (4) The measured indication shall be 6.5 (± 0.9) Vdc.
- (5) Replace circuit packs 009, 010, and 055 if proper results are not obtained.

52

- (1) Same connections as in 51, except set B TEST switch to position 9.
- (2) The measured voltage shall be less than +0.5 Vdc.

Fig. 41 — Single-Frequency Detector Test

53

- (1) Same as 52, except that on the interface adapter:
 - (a) Remove the strap between terminals 10 and EQ 18.
 - (b) Place a strap between terminals 9 and EQ 18.
- (2) Connect the positive test meter lead to *TP12-055 (CLCON)*.
- (3) The measured indication shall be 6.5 (± 0.9) Vdc.
- (4) Replace circuit packs 058 and 059 if proper results are not obtained.

After testing, remove both test meter leads and the ground from TP10-054 (CS/CB). Position B TEST switch to OFF. Remove the strap from between 9 and EQ 18, and place a strap between 10 and EQ 18 on the interface adapter.

Fig. 42 — Single-Frequency Detector Test

TEST 11 — REMOTE TEST

9.34 The data set may be tested remotely by a 904-type Data Test Center. Data set functions can be transferred from LINE condition to REMOTE TEST by a customer-originated signal on the RMT interface lead. During REMOTE TEST operation, circuits within the data set generate the required control signals for the various operational modes for both transmitter and receiver sections.

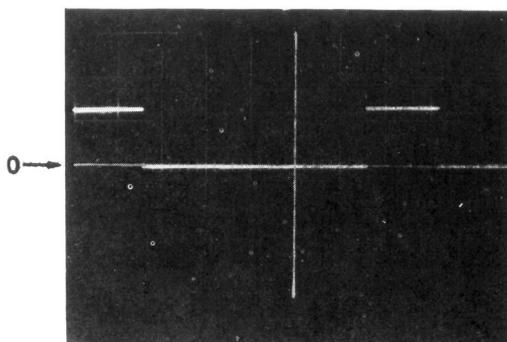
9.35 Waveforms and voltage requirements for REMOTE TEST operation, shown in Tests 54 and 55, are keyed to the functional schematic shown in Fig. 47.

Note: Test 56 is keyed to Fig. 10 (sheet 1) and Test 57 is keyed to Fig. 10 (sheet 2). Fig. 41 shows the strapping provided by the 4A1 Data Unit connection cord which permits either 2-WIRE 4-WIRE operation.

54

- (1) Position B TEST switch to 10. Observe that the K2 wire-spring relay in bottom right section of the data set is released.
- (2) Position B TEST switch to 11. Observe that the K2 relay operates.
- (3) Replace circuit pack 021 if proper result is not obtained.

CONDITIONS: Operate LINE-TEST key to LINE position. Strap TP3-040 (E) to TP12-009 (CO'). Strap TP4-040 (E') to TP12-057 (CS').



MODE A ONLY

55

TRIGGER INPUT (*none*)

TRIGGER MODE DC INT SLOPE +

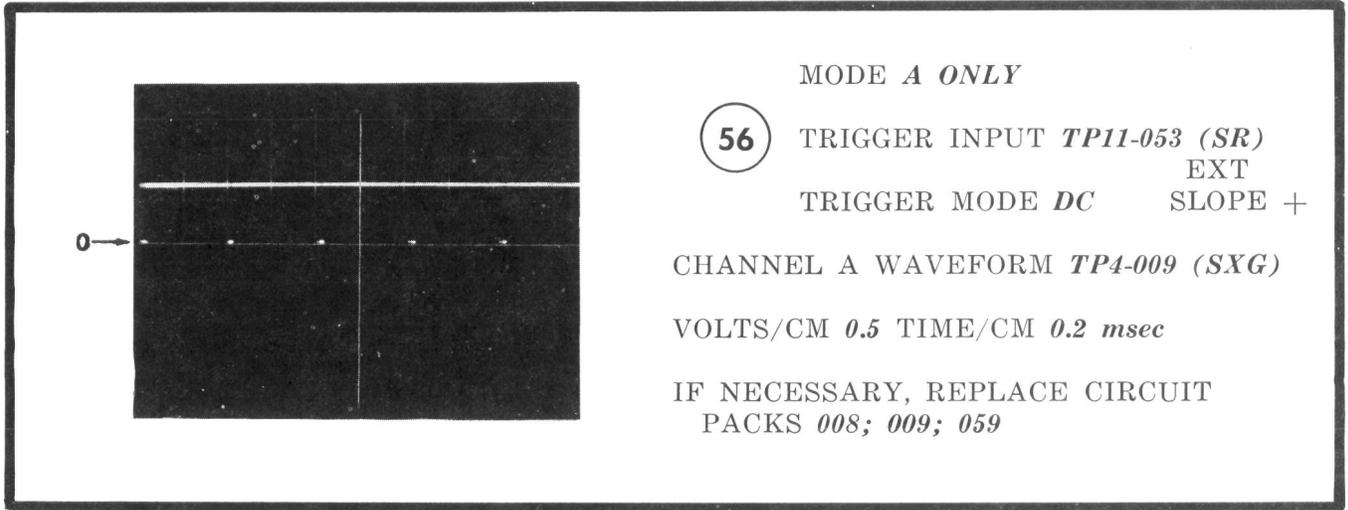
CHANNEL A WAVEFORM TP6-054 (RTSS)

VOLTS/CM 0.5 TIME/CM 0.5 msec

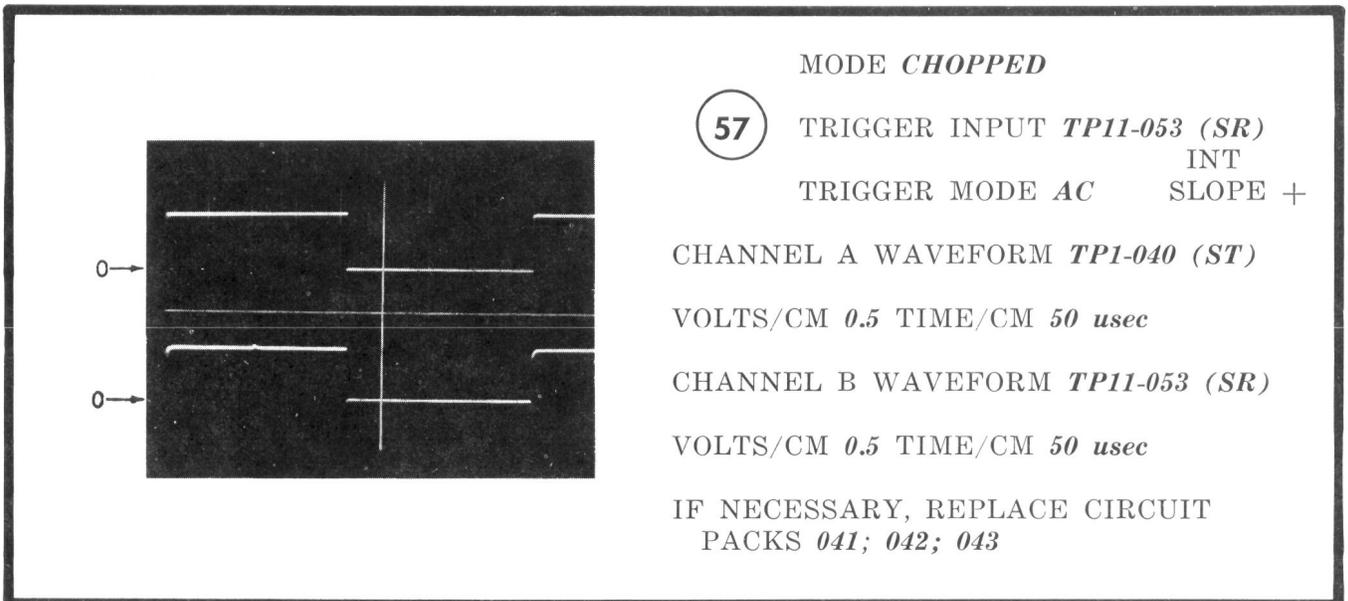
IF NECESSARY, REPLACE CIRCUIT PACKS 021; 053; 054

Fig. 43 — Remote Test

CONDITIONS: Remove all straps used in 55. Ground both TP12-053 (RTCON') and TP13-053 (RTRS'). Adjust the oscilloscope to trigger on the rise of SR.



CONDITIONS: Same as 56, except position MODE switch to CHOPPED. The positive transitions of ST shall be within ± 0 and $-35 \mu\text{sec}$ of the positive transitions of SR.



After testing, remove the straps from circuit pack 053, position B TEST switch to OFF, and operate the LINE-TEST key to TEST position.

Fig. 44 — Remote Test

TEST 12 — DSR/CC LEAD CHECK

58

- (1) Condition the KS-14510 test meter to measure on the 12-volt scale.
- (2) Connect the negative test meter lead to **TP13-059 (DSR/CC)** and the positive lead to ground. The test meter should indicate $-6.5 (\pm 1.3)$ Vdc.
- (3) Remove the test meter leads.

59

- (1) Operate the LINE-TEST key to LINE position.
- (2) Connect the positive test meter lead to **TP13-059 (DSR/CC)** and the negative lead to ground. The test meter should indicate $+7.0 (\pm 1.3)$ Vdc.
- (3) If necessary, replace circuit packs **054; 057; 059**.

Fig. 45 — DSR/CC Lead Check Test

TEST 13—REGENERATION CIRCUIT TESTS
 (See Fig. 36, sheet 2)

60

- (1) Check that the LINE-TEST key is in LINE position.
- (2) Carefully remove the circuit pack from location 019. Remove the strap between terminals 3 and 4. Carefully replace the circuit pack in the original location.
- (3) Remove the strap between 10 and EQ 11 and connect a strap between 9 and EQ 11 on the interface adapter.
- (4) On the interface adapter: (a) open the circuit between TST 15 and EQ 15 by sliding the shorting clip, and (b) close the circuit between TST 24 and EQ 24 by using the shorting clip provided.
- (5) Position ATT-UNATT switch to UNATT.
- (6) Position B TEST switch to OFF and A TEST switch to 22.
- (7) Connect **TP5-053 (DR)** to TRANSMIT CLOCK terminal on the 901B-2 test set.
- (8) Connect the oscilloscope TRIGGER to terminal A on the 901B-2 test set. Position the MODE switch to DC and TRIGGER SLOPE to + (plus).
- (9) Position VOLTS/CM switch to 0.5 and TIME/CM switch to 0.2 msec.
- (10) Connect CHAN A probe to TRANSMIT CLOCK terminals on the 901B-2 test set. Observe waveform as shown in Test 3.

61

- (1) Remove the connection between **TP5-053 (DR)** and TRANSMIT CLOCK and connect TRANSMIT CLOCK to **TP2-053**. Observe waveform as shown in Test 3.
- (2) If necessary, replace circuit packs **057** and **059**.
- (3) Remove the connection between **TP2-053** and TRANSMIT CLOCK on the 901B-2 test set.
- (4) On the interface adapter: (a) open the circuit between TST 24 and EQ 24 by sliding the shorting clip, and (b) close the circuit between TST 15 and EQ 15 by using the shorting clip provided, and (c) remove the strap between terminals 9 and EQ 11, and place a strap between terminals 10 and EQ 11.
- (5) Carefully remove the circuit pack from location 019 and replace the strap between terminals 3 and 4. Replace the circuit pack in the original location.
- (6) Position A TEST switch to OFF.

Fig. 46 — Regeneration Circuit Tests

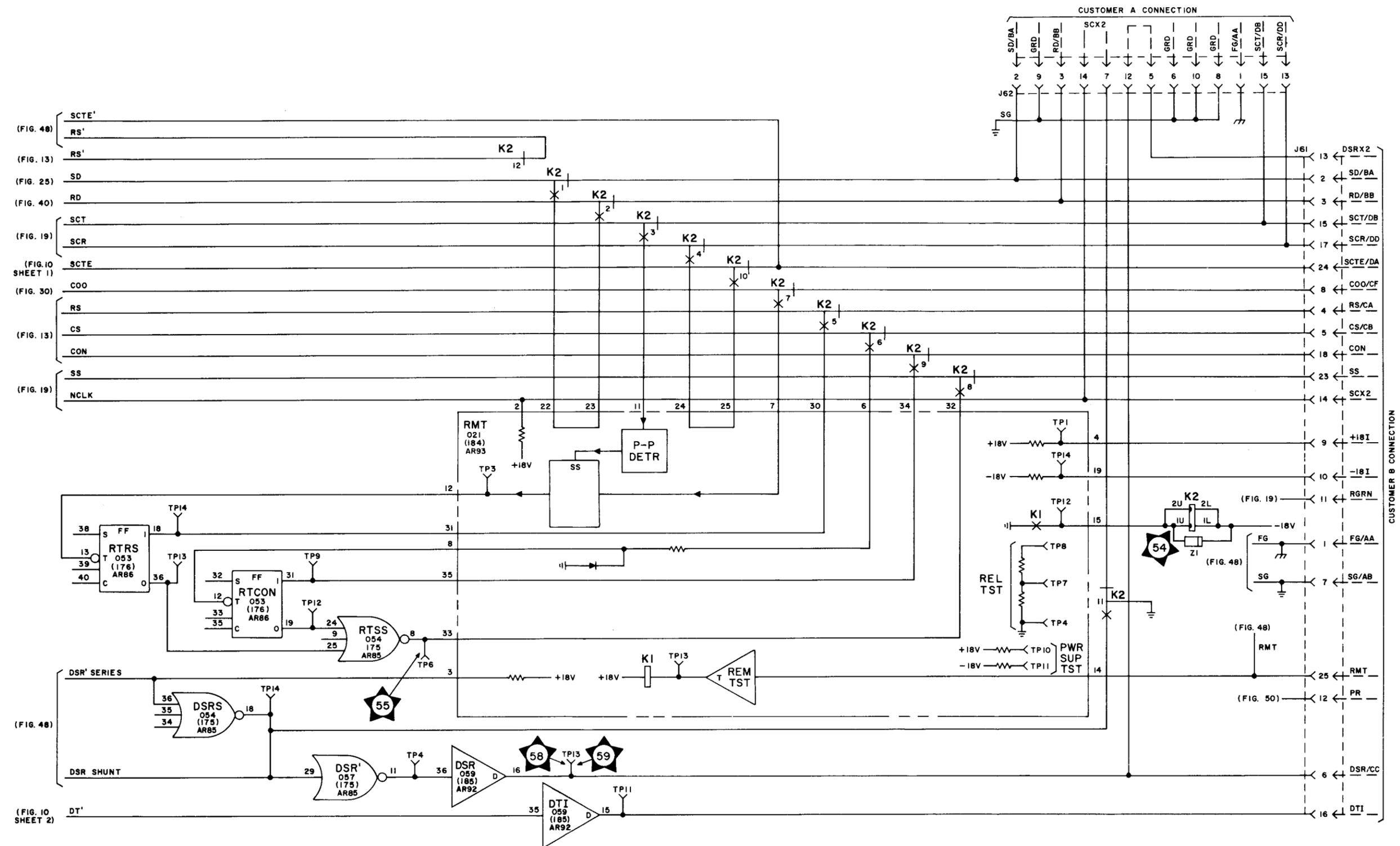


Fig. 47 — Interface Connections, Functional Schematic

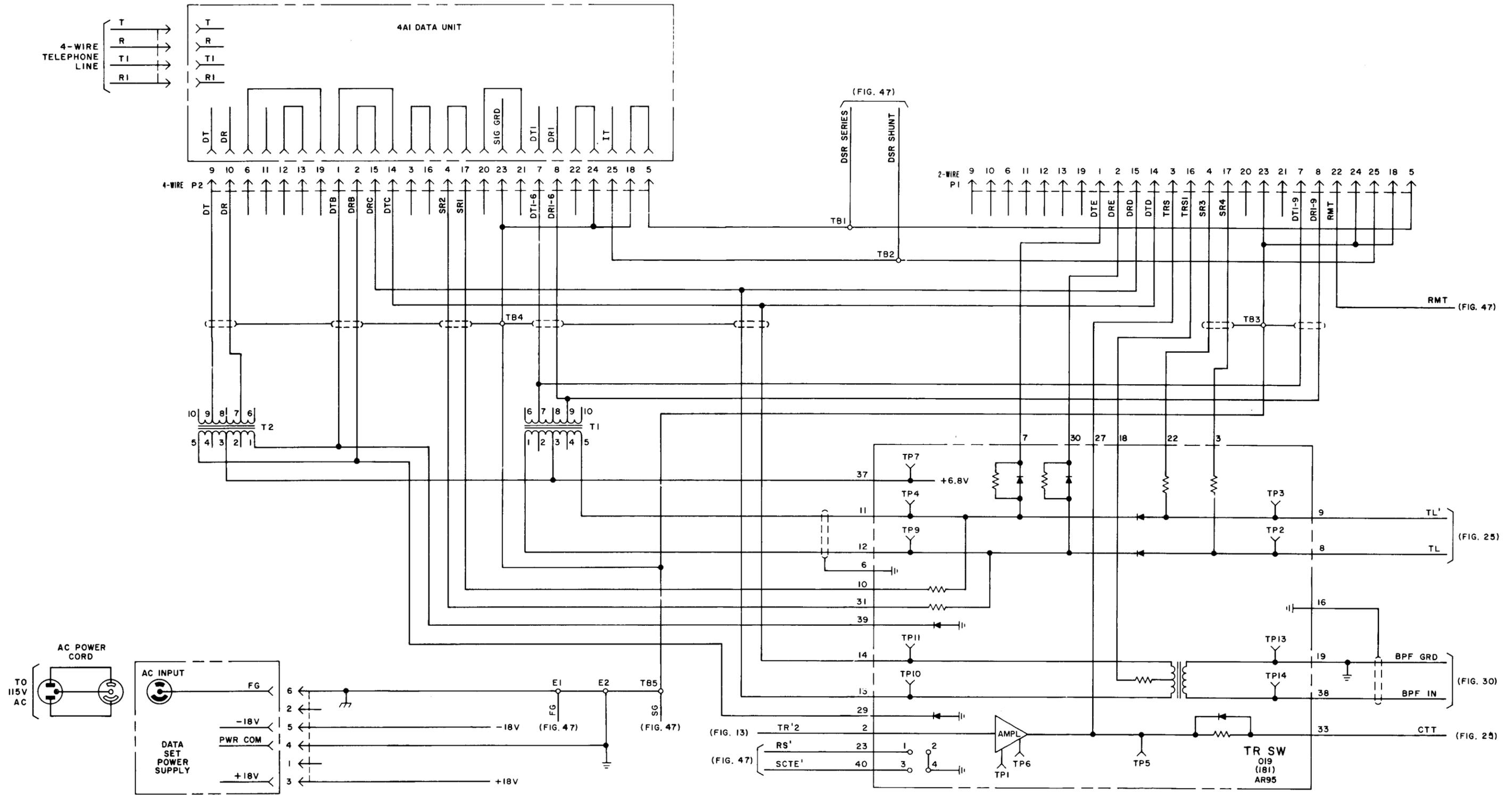


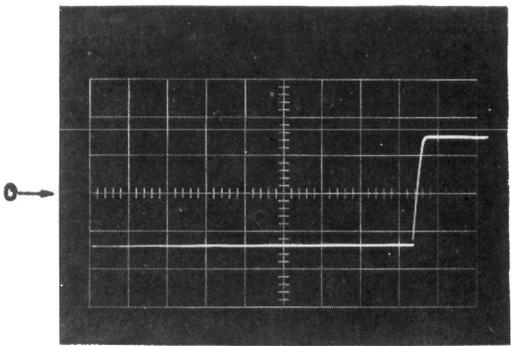
Fig. 48 — Transmit-Receive Switch and Telephone Line Connections, Functional Schematic

TEST 14 — PREPARE RECEIVER TIMING

9.36 Test the prepare receiver timing circuits with a KS-14510 test meter through Step 65 before replacing the suggested boards. Observe polarity of the test meter leads when obtaining the measurements. The data set LINE-TEST key should be in TEST position. Tests shown in Fig. 49 are keyed to the functional schematic shown in Fig. 50.

<p>62 (1) Position the ATT-UNATT switch on the 901B-2 to UNATT.</p> <p>(2) Position A TEST switch to OFF and B TEST switch to 6.</p> <p>(3) Connect the test meter between <i>TP14-059 (PR)</i> and ground.</p> <p>(4) Indication: $-6.5 (\pm 1.3)$ Vdc.</p>	<p>64 Same as 62, except B TEST switch to position 4. Indication: $+7.0 (\pm 1.3)$ Vdc.</p> <p>65 Same as 64, except operate LINE-TEST key to LINE position. Indication: $-6.5 (\pm 1.3)$ Vdc.</p> <p>IF NECESSARY, REPLACE CIRCUIT PACKS <i>049; 050; 059</i>.</p>
<p>63 Same as 62, except B TEST switch to position 3. Indication: $-6.5 (\pm 1.3)$ Vdc.</p>	

CONDITIONS: Observe waveform each time LINE-TEST key is operated from LINE to TEST position.

	<p>MODE <i>A ONLY</i></p> <p>66 TRIGGER INPUT <i>TP3-050 (CPR')</i> EXT TRIGGER MODE <i>DC</i> SLOPE <i>+</i></p> <p>CHANNEL A WAVEFORM <i>TP14-059 (PR)</i></p> <p>VOLTS/CM <i>0.5</i> TIME/CM <i>10 msec</i></p> <p>IF NECESSARY, REPLACE CIRCUIT PACKS <i>049; 050; 059</i></p>
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Position the B TEST switch to OFF on the 901B-2 test set.
END OF MAINTENANCE TESTS (See 9.16)

Fig. 49 — Prepare Receiver Timing Test

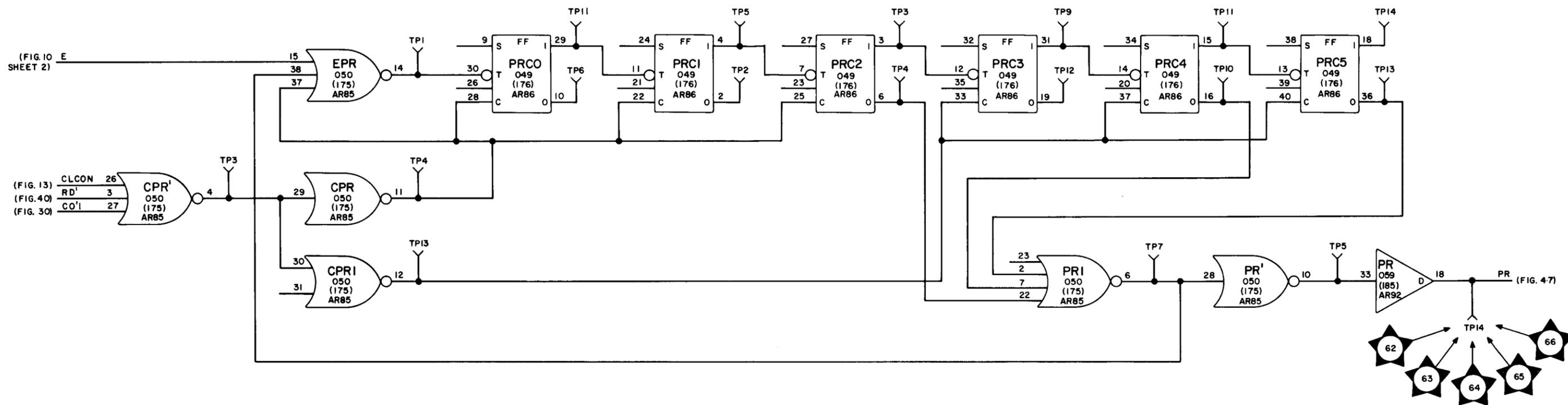


Fig. 50—Prepare Receiver Circuits, Functional Schematic