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1A. GENERAL

1.01A The information contained in the following descriptions, tests, sketches, and drawings is given to assist in understanding the function of the data set circuit packs.

1.02A A glossary of mnemonic symbols is included as the final pages of the Appendix. The glossary contains a brief definition of each mnemonic symbol used in the functional schematics keyed for oscilloscope tests. For a detailed definition of each symbolic function and an analysis of how and why the functions are interconnected, refer to CD-1D085-01.

2A. NOR GATE CIRCUIT PACK ASSEMBLY AR85 (A835175)

2.01A *Circuit Description:* The AR85 circuit pack contains eight NOR gates and two inverter stages. Transistors Q4 and Q5 and associated components are the inverter stages. The remaining transistors and components are the NOR gates.

2.02A Operation of a NOR gate and an inverter is similar except an inverter has a "fan-in" of one input as compared to a NOR gate having a "fan-in" of either two, three, or four inputs. The following description is illustrated by a circuit sketch that follows the test procedures.

2.03A The following circuit pack AR85 operational description is typical of both gates and inverters. Using transistor Q1 and associated components as an example: When a +6.2 Vdc (a logical "1") signal is applied to one or more input terminals (2, 7, 22, and/or 23), transistor Q1 will conduct. During the ON time, the collector of Q1 (and output terminal 6) is held to less than +0.5 Vdc (a logical "0") through the conducting transistor to ground. Transistor Q1 is turned OFF when all input terminals are simultaneously receiving less than +0.5 Vdc. When Q1 is OFF, the output terminal is held at approximately +6.2 Vdc through operation of clamping diode CR1.

NOR Gate Circuit Pack Test:

A. Test Equipment

1 — NOR gate test set such as shown in Fig. 1A

1 — Oscilloscope, Tektronix 533 with type CA plug-in unit (or equivalent)

2 — Probes, Tektronix P6006 (10X) (or equivalent)

1 — Square-wave generator, Hewlett-Packard 211A (or equivalent)

1 — Mercury relay, WECo 291A (or equivalent)

1 — DC voltmeter, 20,000 ohm/volt, ±3 percent

1 — DC milliammeter, ±5 percent

3 — Switches:

1 — DPDT

1 — 5-wafer, 10-position, rotary

1 — 4-wafer, 5-position, rotary

5 — Resistors:

1 — 100 ohms (±1 percent), 1 watt, WECo 144E (or equivalent)

1 — 316 ohms (±1 percent), 0.5 watt, WECo 145A (or equivalent)

1 — 121 ohms (±1 percent), 1 watt, WECo 144E (or equivalent)

1 — 2150 ohms (±1 percent), 1/2 watt, WECo 145A (or equivalent)

1 — 3160 ohms (±1 percent), 1/2 watt, WECo 145A (or equivalent).

B. Power Requirements

+18.0 (±0.5) Vdc — 200 mA

+2.5 (±0.1) Vdc — 40 mA

+6.0 (±0.3) Vdc — 20 mA

C. Test Procedures

2.04A *Diode Short Test:*

(1) This test is to be made before the circuit pack to be tested is inserted into the test set.

(2) Ground pin 1 and apply +6.0 (±0.3) Vdc to test point 8 on the circuit pack; current drain should be less than 3.0 mA dc.

2.05A *Zener Voltage Test:*

(1) Insert the circuit pack into the test set and connect +18.0 (±0.5) Vdc to J10.

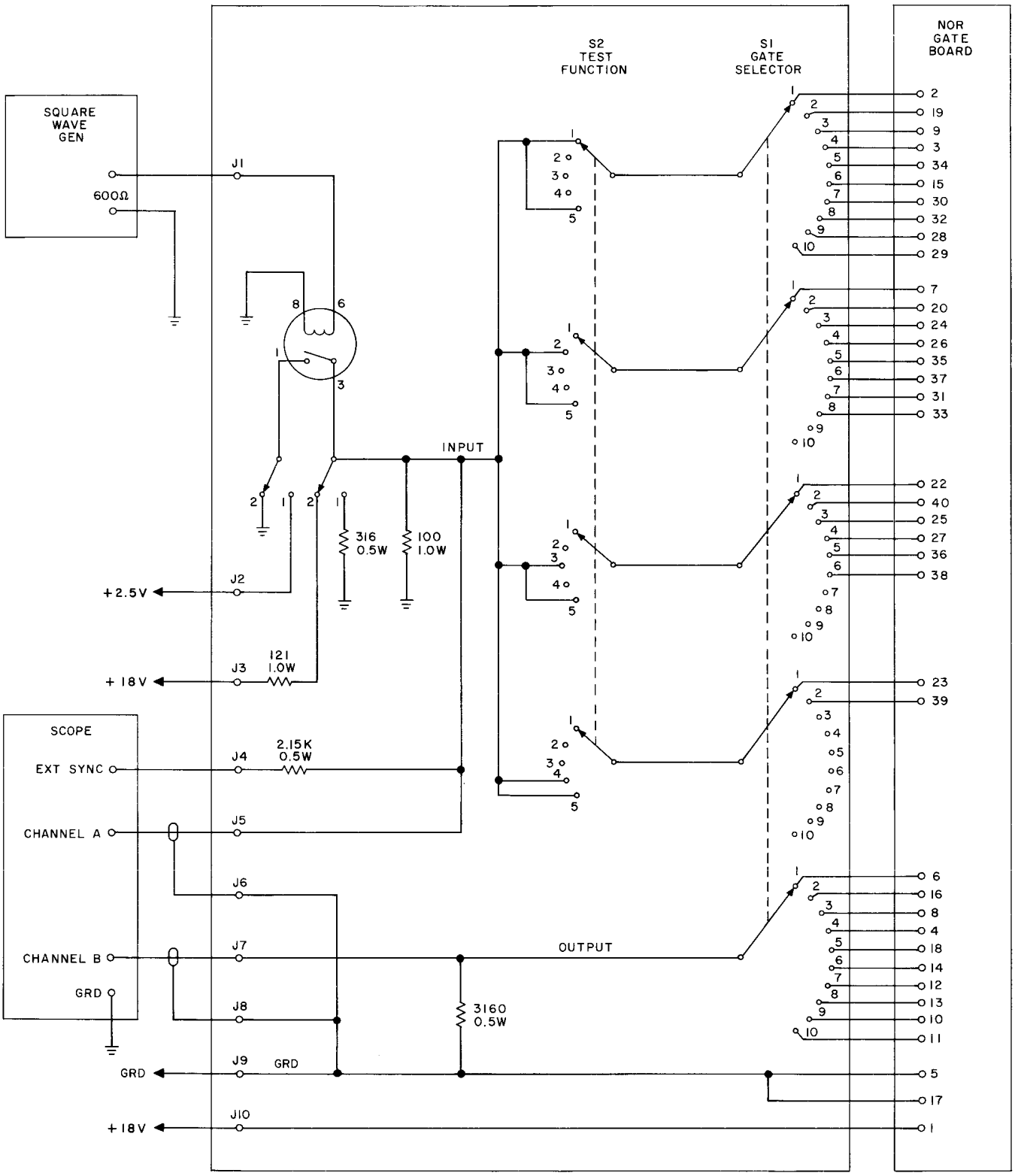


Fig. 1A — NOR Gate Test Set

(2) The voltage between test point 7 and ground, when measured with the voltmeter, should be +6.2 (±0.6) Vdc.

2.06A ***Turn-On Time:***

(1) Connect the test circuit as shown in Fig. 1A.

Note: Consult Table A to determine which gate and corresponding input resistance are under test.

(2) Set the frequency of the square-wave generator between 40 and 50 Hz.

(3) Set the DPDT switch to position 1.

(4) Set the GATE and TEST FUNCTION selector to position 1.

(5) Set the EXT SYNC TRIGGER to the (+) positive position.

(6) Rotate the GATE selector through positions 1 to 10. At each position, the input and output step shall be as specified in Fig. 2A.

(7) Set the TEST FUNCTION selector to position 2. Rotate the GATE selector through positions 1 to 8. Observe output as in (6). Time base measurements need not be made.

(8) Set the TEST FUNCTION selector to position 3. Rotate the GATE selector through positions 1 to 6. Observe output as in (6). Time base measurements need not be made.

(9) Set the TEST FUNCTION selector to position 4. Rotate the GATE selector through position 1 to 2. Observe output as in (6).

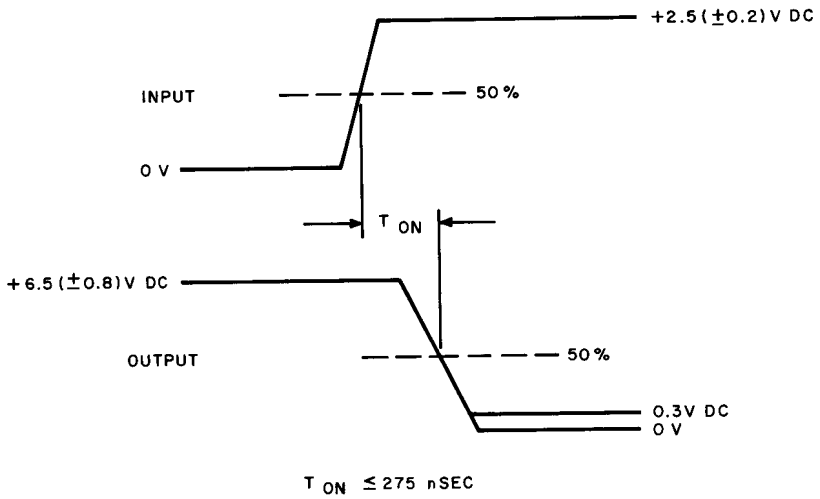


Fig. 2A — NOR GATE Test

TABLE A

KEY TO COMPONENTS UNDER TEST AT EACH POSITION OF TEST SET SWITCHES

TEST FUNCTION POSITION	GATE SELECTOR POSITION	INPUT TERMINAL	INPUT RESISTOR	TRANSISTOR	OUTPUT TERMINAL
1	1	2	R1	Q1	6
	2	19	R23	Q10	16
	3	9	R5	Q2	8
	4	3	R8	Q3	4
	5	34	R17	Q8	18
	6	15	R20	Q9	14
	7	30	R13	Q6	12
	8	32	R15	Q7	13
	9	28	R11	Q4	10
	10	29	R12	Q5	11
2	1	7	R2	Q1	6
	2	20	R24	Q10	16
	3	24	R6	Q2	8
	4	26	R9	Q3	4
	5	35	R18	Q8	18
	6	37	R21	Q9	14
	7	31	R14	Q6	12
	8	33	R16	Q7	13
3	1	22	R3	Q1	6
	2	40	R25	Q10	16
	3	25	R7	Q2	8
	4	27	R10	Q3	4
	5	36	R19	Q8	18
	6	38	R22	Q9	14
4	1	23	R4	Q1	6
	2	39	R26	Q10	16
5	1	2, 7, 22, 23	R1, R2, R3, R4	Q1	6
	2	19, 20, 40, 39	R23, R24, R25, R26	Q10	16
	3	9, 24, 25	R5, R6, R7	Q2	8
	4	3, 26, 27	R8, R9, R10	Q3	4
	5	34, 35, 36	R17, R18, R19	Q8	18
	6	15, 37, 38	R20, R21, R22	Q9	14
	7	30, 31	R13, R14	Q6	12
	8	32, 33	R15, R16	Q7	13
	9	28	R11	Q4	10
	10	29	R12	Q5	11

2.07A *Gate Turn-Off Time:*

(1) Set the DPDT switch to position 2 and the TEST FUNCTION selector to position 1.

(2) Set the EXT SYNC TRIGGER to (—) negative.

(3) Rotate the GATE selector through positions 1 to 10. The input and output steps shall be as specified in Fig. 3A at each position.

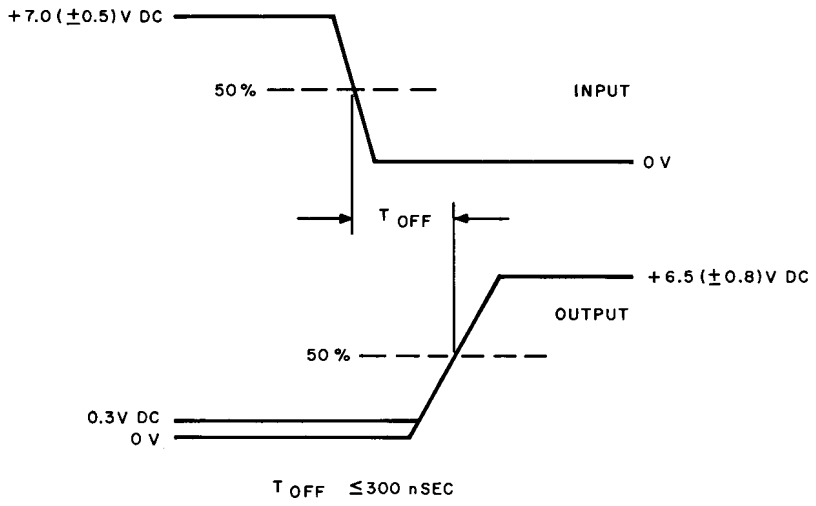
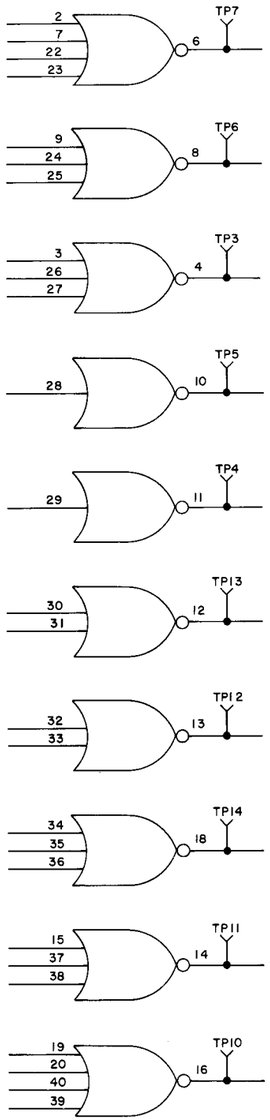


Fig. 3A. — NOR Gate Test



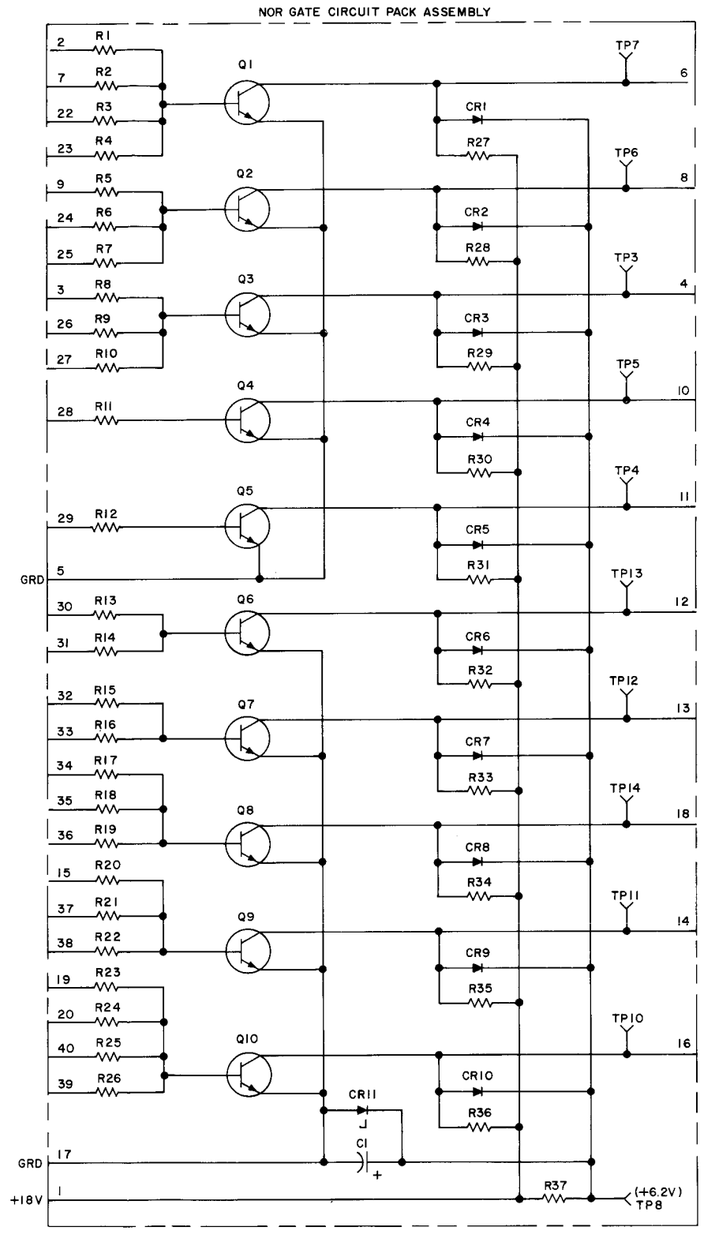


Fig. 4A — NOR Gate, Circuit Pack Assembly AR85 (A835175), Circuit Sketch

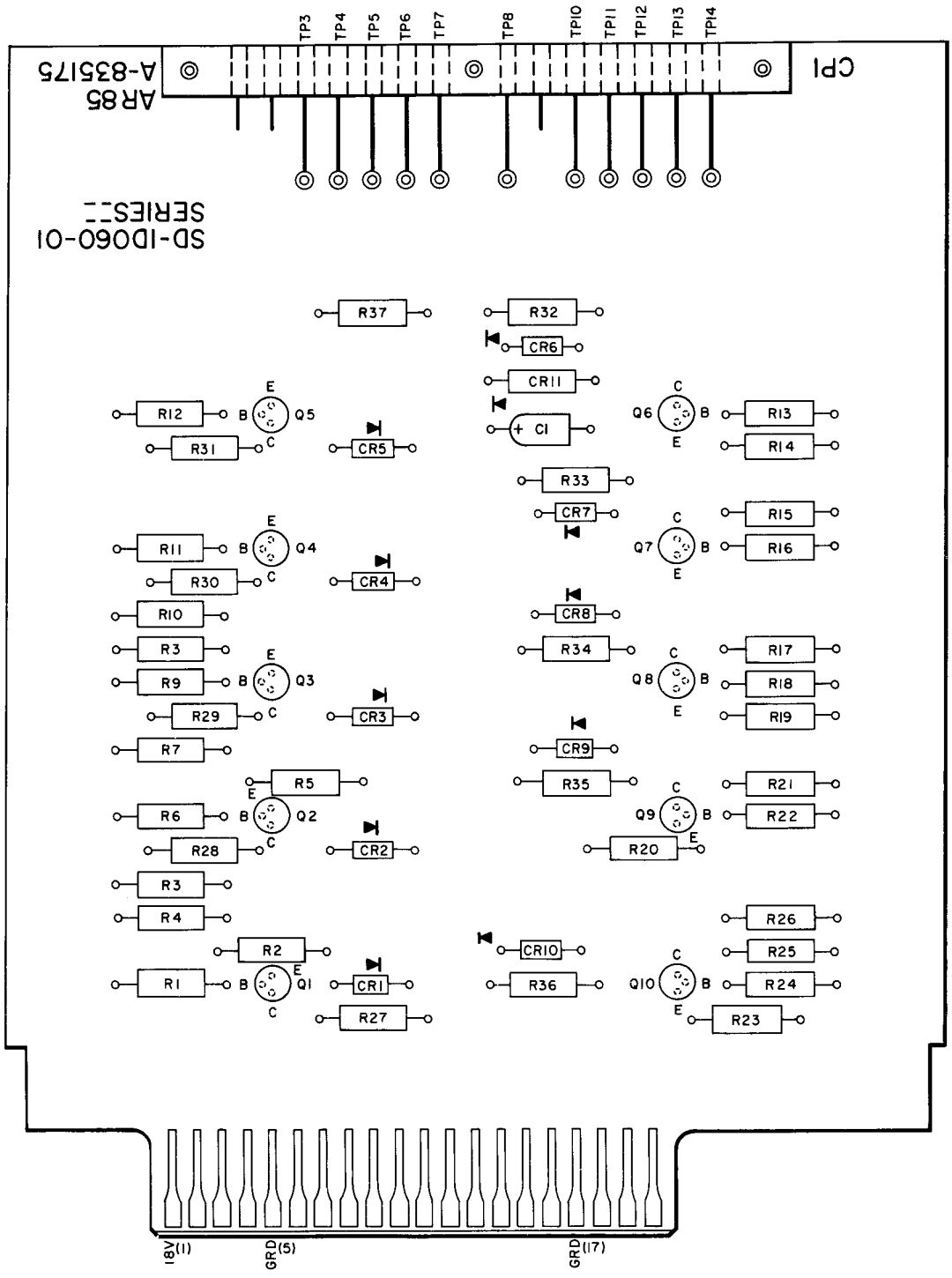


Fig. 5A — NOR Gate, Circuit Pack Assembly AR85 (A835175), Component Location

3A. COMPLEMENTARY FLIP-FLOP CIRCUIT PACK ASSEMBLY AR86 (A835176)

3.01A *Circuit Description:* The AR86 circuit pack contains six identical complementary flip-flop circuits. Two transistors and associated components are used for each circuit. Operation of all circuits is identical so only the "point zero" components will be described. The following descriptions are illustrated by a circuit sketch that follows the test procedures.

3.02A This circuit will provide either a "set" or a "clear" output state. A "set" state is provided when transistor Q1.0 is conducting and Q2.0 is cut off. A "clear" state is provided when transistors Q1.0 is cut off and Q2.0 is conducting. Input signals of less than +0.5 Vdc (a logical "0") on either "set" (terminal 9) or "clear" (terminals 26 and 28) will not change the operating state. If the circuit is operating at "set" state and a voltage of +6.2 Vdc (a logical "1") is applied to either "clear" input terminal, transistor Q2.0 starts conducting and cuts off transistor Q1.0 causing the circuit to be operated into the "clear" state. During the "clear" state, the voltage of output terminal 29 is less than +0.5 Vdc and output terminal 10 is clamped to approximately +6.2 Vdc.

3.03A When +6.2 Vdc is applied to the "set" input terminal (9), the circuit will switch to the "set" state. During the "set" state, output terminal 29 is clamped to approximately +6.2 Vdc and terminal 10 is less than +0.5 Vdc.

3.04A Signals on the toggle terminal (30) are applied to a steering circuit composed of components C1.0, C2.0, CR3.0, CR4.0, R5.0, and R6.0. The steering circuit applies the negative signal transitions to the base of the conducting transistor. During the "set" state (with transistors Q1.0 conducting and Q2.0 cut off), the positive voltage on the collector of Q2.0 also reverse-biases CR4.0 through R5.0. The collector of Q1.0 is near ground potential and CR3.0 is near conduction. A negative transition on the toggle terminal is differentiated by C1.0 and applied through CR3.0 to the base of Q1.0. The applied negative signal cuts off Q1.0 and Q2.0 starts conducting, thereby switching the circuit to the opposite state. The next negative transition on the toggle terminal is differentiated through CR4.0 to the base of Q2.0 and the circuit is switched again.

Complementary Flip-Flop Circuit Pack Test:

A. Test Equipment

1 — Complementary flip-flop test set such as shown in Fig. 6A.

1 — Oscilloscope, Tektronix 533 with type CA plug-in unit (or equivalent)

2 — Probes, Tektronix P6006 (10X) (or equivalent)

1 — DC voltmeter, 20,000 ohm/volt, ±3 percent

1 — 0 to 50 microammeter, ±3 percent

2 — Resistors:

1 — 0.121 meg (±5 percent), 1/2 watt, WECo 145A (or equivalent)

1 — 2150 ohms (±1 percent), 1/2 watt, WECo 145A (or equivalent).

B. Power Requirements

+18.0 (±0.5) Vdc — 200 mA

+6.0 (±0.3) Vdc — 0.1 mA

C. Preliminary Procedure

3.05A Set up the test circuit as shown in Fig. 7A. The scope EXT SYNC TRIGGER selector should be set to the (+) positive position.

NOTES:
1. ALL RESISTOR VALUES IN OHMS, 1/2 WATT, 1% TOL, UNLESS SPECIFIED.
2. ALL CAPACITORS IN UUF, 5% TOL, UNLESS SPECIFIED.

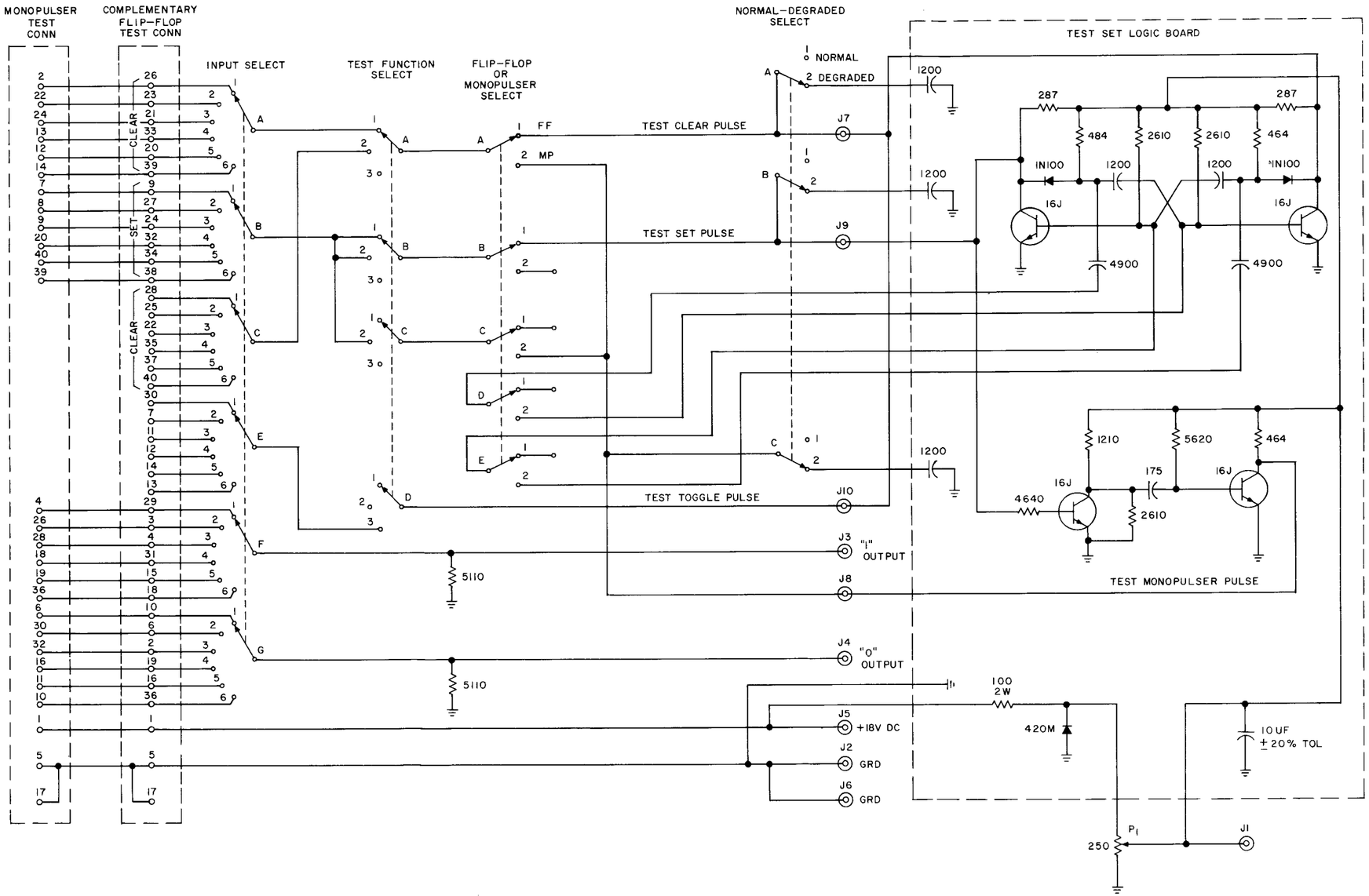


Fig. 6A — Complementary Flip-Flop Test Set

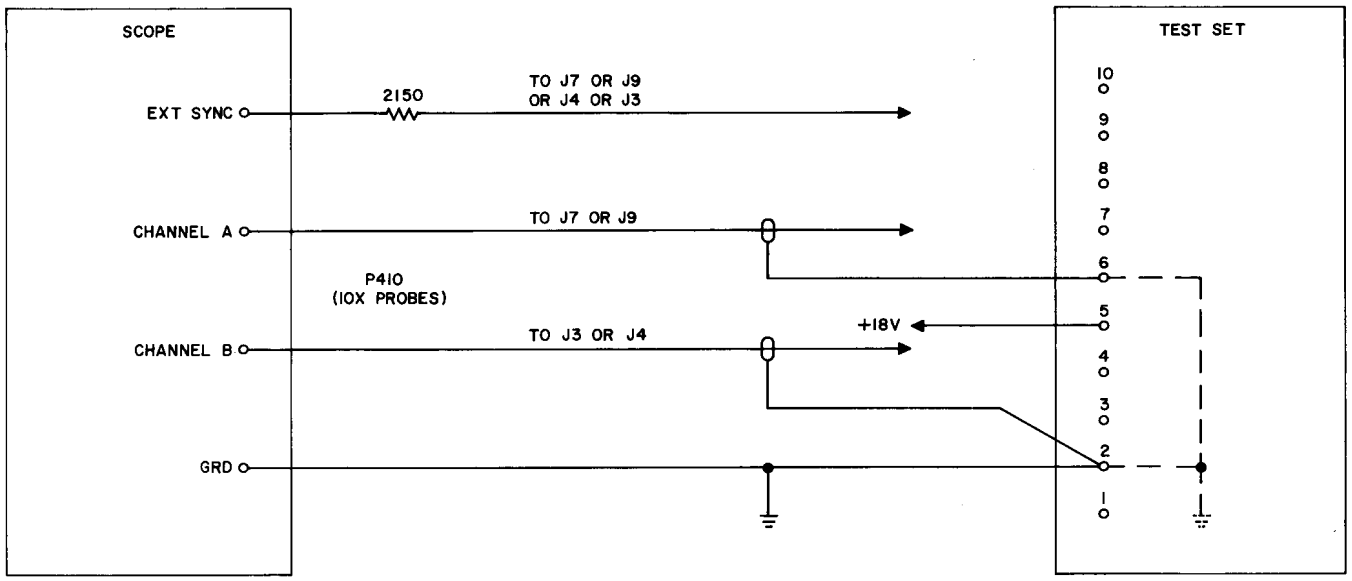


Fig. 7A — Complementary Flip-Flop Test Circuit

3.06A Make the following settings on the test set:

(1) INPUT selector to position 1.

(2) TEST FUNCTION selector to position 1.

(3) FLIP-FLOP — MONOPULSER selector to FLIP-FLOP.

(4) NORMAL — DEGRADED selector to NORMAL.

(5) Adjust the potentiometer until the voltage between J1 and ground of the test set is 6.0 (±0.2) Vdc.

D. Test Procedures

3.07A ***Diode Leakage Test:***

(1) This test is to be made before the circuit pack is inserted into the test set.

(2) Ground pin 1 and apply +6.0 (±0.3) Vdc in series with a 0.121-meg resistor to test point 8 of the circuit pack to be tested.

(3) The total current drawn shall be less than 35 uA dc.

(4) Remove connections made in (2).

3.08A ***Zener Voltage Test:***

(1) Insert the circuit pack to be tested into the test set flip-flop test connector.

(2) The voltage between test point 8 and ground when measured with the voltmeter shall be +6.2 (±0.6) Vdc.

3.09A ***Pulse Test — Normal Input:***

Consult Table B to determine which flip-flop circuit and corresponding input resistor or capacitor is under test.

3.10A ***Clear Test:***

(1) Connect the EXT SYNC lead to J7 on the test set.

(2) Connect the CHAN A probe to J7 on the test set.

(3) Connect the CHAN B probe to J4 on the test set.

(4) The input test pulse on J7 shall be as specified in Fig. 8A.

(5) Rotate the INPUT selector through positions 1 to 6.

(6) The output pulse on J4 of the test set shall be as specified in Fig. 9A at each position.

(7) Rotate the TEST FUNCTION selector to position 2.

(8) Repeat as in (5) and (6).

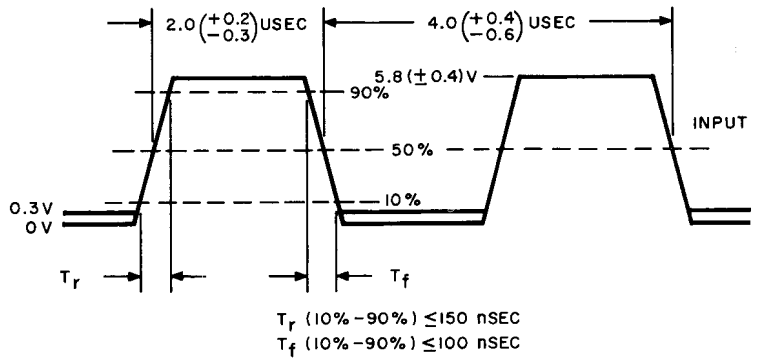


Fig. 8A — Complementary Flip-Flop Test

TABLE B

KEY TO COMPONENTS UNDER TEST AT EACH POSITION OF TEST SET SWITCHES

TEST FUNCTION POSITION	INPUT SELECTOR POSITION	INPUT TERMINAL	INPUT RESISTOR CAPACITOR	TRANSISTOR	OUTPUT TERMINAL
1	1	26, 9	R9.0, R7.0	Q1.0, Q2.0	29, 10
	2	23, 27	R9.1, R7.1	Q1.1, Q2.1	3, 6
	3	21, 24	R9.2, R7.2	Q1.2, Q2.2	4, 2
	4	33, 32	R8.3, R7.3	Q1.3, Q2.3	31, 19
	5	20, 34	R8.4, R7.4	Q1.4, Q2.4	15, 16
	6	39, 38	R9.5, R7.5	Q1.5, Q2.5	18, 36
2	1	28, 9	R8.0, R7.0	Q1.0, Q2.0	29, 10
	2	25, 27	R8.1, R7.1	Q1.1, Q2.1	3, 6
	3	22, 24	R8.2, R7.2	Q1.2, Q2.2	4, 2
	4	35, 32	R9.3, R7.3	Q1.3, Q2.3	31, 19
	5	37, 34	R9.4, R7.4	Q1.4, Q2.4	15, 16
	6	40, 38	R8.5, R7.5	Q1.5, Q2.5	18, 36
3	1	30	C1.0, C2.0	Q1.0, Q2.0	29, 10
	2	7	C1.1, C2.1	Q1.1, Q2.1	3, 6
	3	11	C1.2, C2.2	Q1.2, Q2.2	4, 2
	4	12	C1.3, C2.3	Q1.3, Q2.3	31, 19
	5	14	C1.4, C2.4	Q1.4, Q2.4	15, 16
	6	13	C1.5, C2.5	Q1.5, Q2.5	18, 36

3.11A ***Set Test:***

(1) Connect the EXT SYNC lead to J9 of the test set.

(2) Connect the CHAN A probe to J9 of the test set.

(3) Connect the CHAN B probe to J3 of the test set.

(4) Rotate the TEST FUNCTION selector to position 2.

(5) Rotate the input selector through positions 1 to 6.

(6) The output pulse on J3 shall be as specified in Fig. 9A.

3.12A ***Toggle Test:***

(1) Rotate the EXT SYNC TRIGGER selector to the (—) negative position.

(2) Rotate the TEST FUNCTION selector to position 3.

(3) Connect the EXT SYNC lead to J4 on the test set.

(4) Connect the CHAN A probe to J7 on the test set.

(5) Connect the CHAN B probe to J3 on the test set.

(6) Rotate the INPUT selector through positions 1 to 6.

(7) The output pulse on J3 of the test set shall be as specified in Fig. 10A.

(8) Connect the EXT SYNC lead to J3 on the test set.

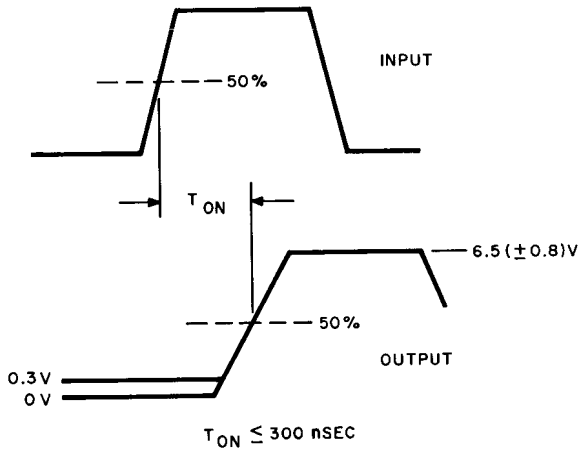


Fig. 9A — Complementary Flip-Flop Test

(9) Connect the CHAN B probe to J4 on the test set.

(10) Repeat (6). The output pulse on J4 shall be as shown in Fig. 10A.

3.13A ***Pulse Test — Degraded Input:***

(1) Set the NORMAL — DEGRADED selector to DEGRADED. Adjust the potentiometer P1 until the amplitude of the input test pulse on J7 and J9 is 3.0 (±0.2) volts.

(2) With the input pulse as shown in Fig. 11A, repeat 3.10A, 3.11A, and 3.12A; however, time base measurements need not be made. Output waveforms shall appear as in Fig. 9A and 10A.

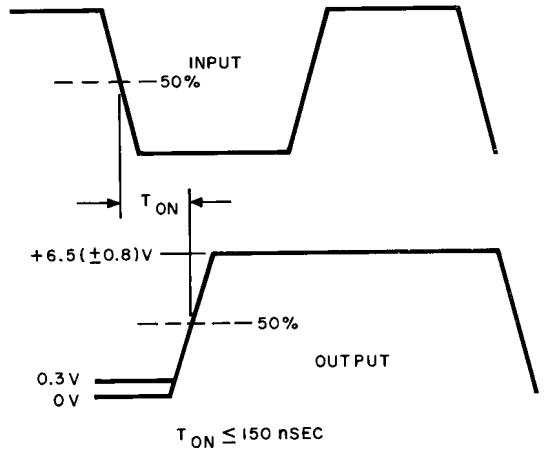


Fig. 10A — Complementary Flip-Flop Test

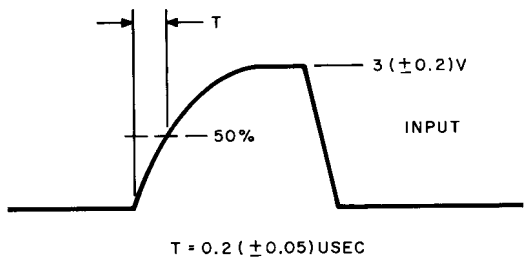
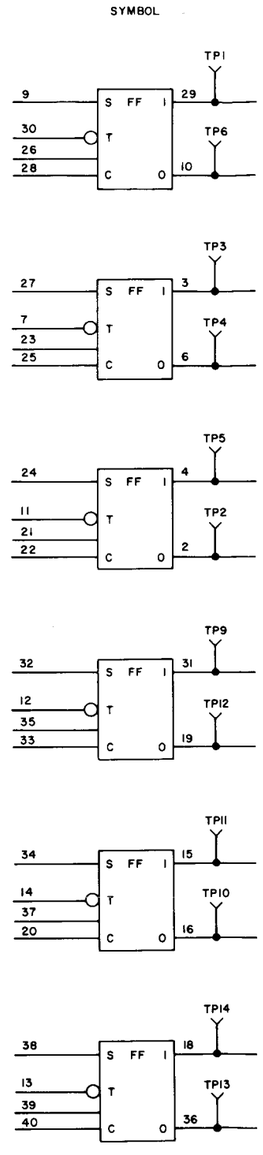


Fig. 11A — Complementary Flip-Flop Test



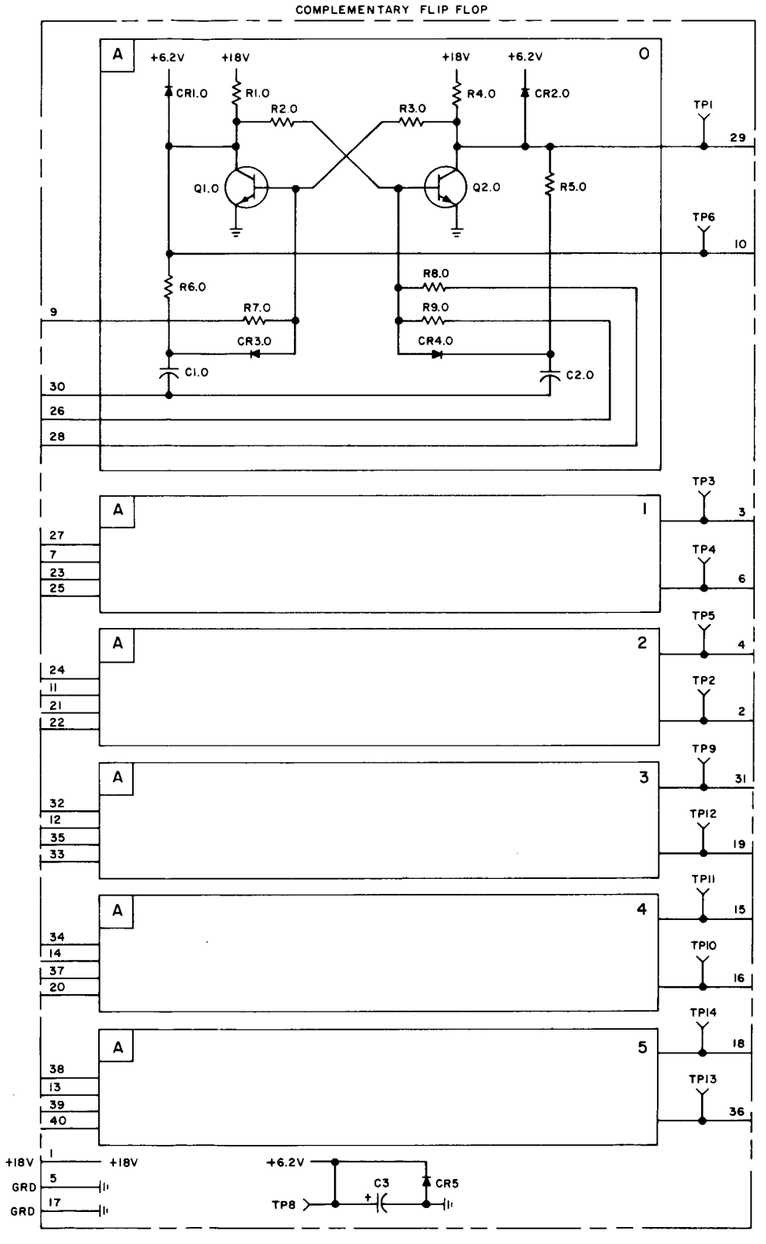


Fig. 12A — Complementary Flip-Flop, Circuit Pack Assembly AR86 (A835176), Circuit Sketch

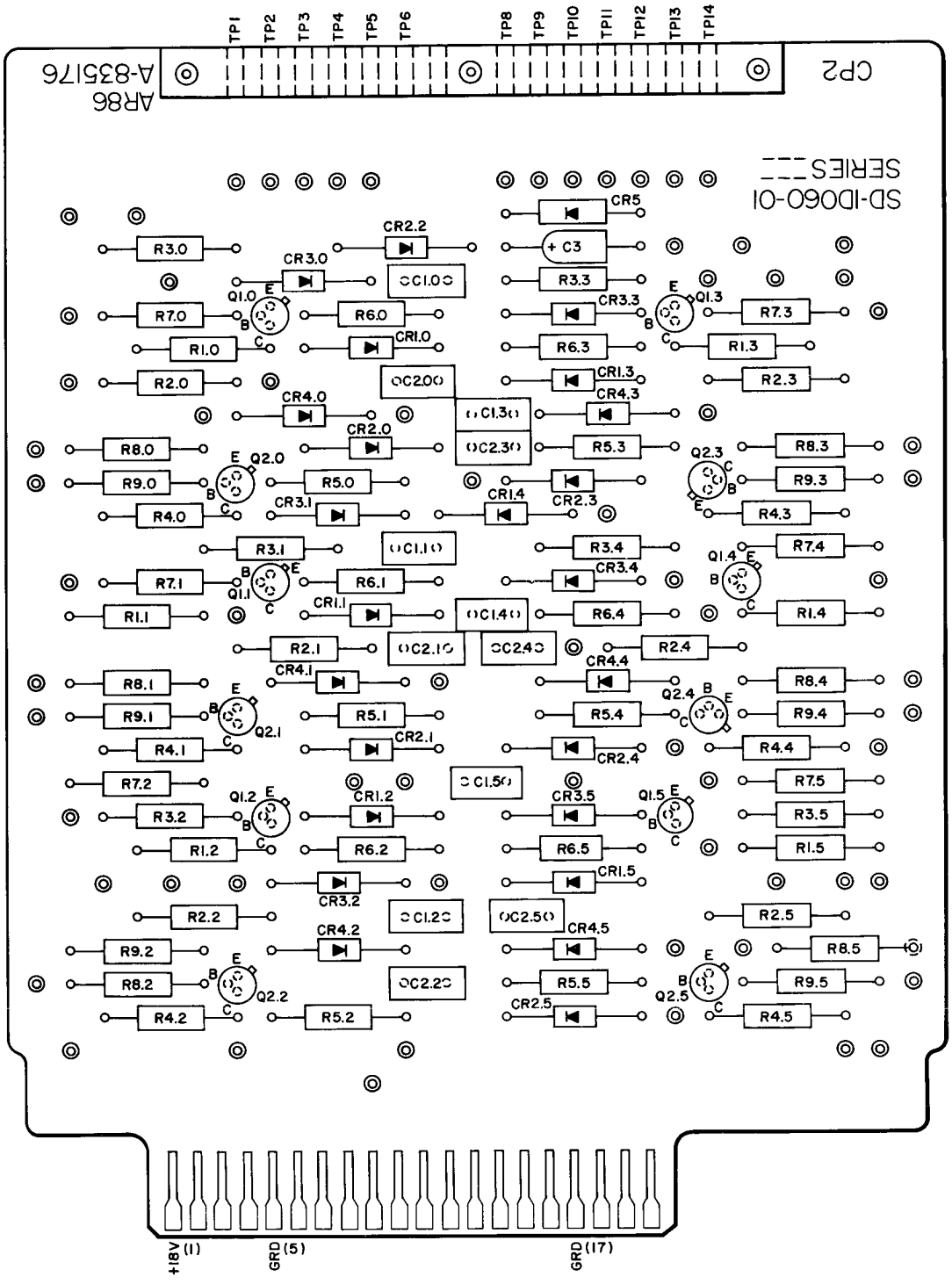


Fig. 13A — Complementary Flip-Flop Circuit Pack Assembly AR86 (A835176), Component Location

4A. SINGLE-FREQUENCY DETECTOR CIRCUIT PACK AR87 (A835183)

4.01A *Circuit Description:* The AR87 circuit pack contains (1) a peak-to-peak amplifier and an emitter-follower; (2) a voltage-doubling rectifier circuit and amplifier; and (3) a fast-operate slow-release circuit and slicer. The following description is illustrated by a circuit sketch that follows the test procedures. Required external connections are illustrated in Fig. 14A and 17A.

4.02A The single-frequency detector monitors the receive data circuits. Ac signals on input terminals 3 and 4 are applied to the primary winding of transformer T1 through emitter followers Q1 and Q2. The signal on the transformer secondary is the difference of the two input signals which is applied to terminal 7 through emitter follower Q3. An externally tuned circuit connected between terminals 7 and 9 passes a narrow band of frequencies to the grounded base amplifier Q4. The amplified signals are applied through C9 to the voltage-doubling circuit consisting of T2, CR1, CR2, R20, C11, and C12.

4.03A If no ac signals are applied to input terminals 3 and 4, there will be no ac signal from the tuned filter at terminal 9. In the absence of ac signals, Q5 and Q6 are turned on by current from the temperature-compensating bias network. This network consists of RT1, R18, R21, and R31. When Q6 is on, Q7 is off and output terminal 14 is clamped to +6.2 Vdc by clamping diode CR4.

4.04A When ac signals from the tuned filter are applied at terminal 9, a negative voltage is developed at the base of Q5 which turns off both Q5 and Q6. When Q6 is off, its collector becomes positive which permits Q7 to turn on, and the voltage on output terminal 14 becomes less than +0.5 Vdc.

4.05A Terminal 12 is the input for the fast-operate slow-release circuit. When +6.2 Vdc (a logical "1") is applied to terminal 12, both Q8 and Q9 are turned on. This permits C15 to discharge through Q8 and R29 to ground, causing output terminal 15 to be approximately zero Vdc. If the signal on terminal 12 is less than +0.5 Vdc (a logical "0"), both Q8 and Q9 turn off and C15 charges positively through R28 and R29. Approximately 25 milliseconds after the +0.5 Vdc input signal is applied, output terminal 15 is clamped to +6.2 Vdc by clamping diode CR5 and the collector of Q8, and TP10 is held at approximately +14.4 Vdc by CR9.

4.06A If a +6.2 Vdc signal is applied to terminal 12, either during or after the 25-millisecond time stated in 4.05A, both Q8 and Q9 are turned on and output terminal 15 (and the collector of Q8) simultaneously go to approximately zero Vdc.

SINGLE-FREQUENCY DETECTOR TEST

A. Testing Equipment

1 — Oscilloscope, Tektronix 533 with type CA plug-in unit (or equivalent)

2 — Probes, Tektronix P6006 (10X) (or equivalent)

1 — Sine-wave generator, Hewlett-Packard model 200CD (or equivalent)

1 — Square-wave generator, Hewlett-Packard model 211A (or equivalent)

1 — DC voltmeter; 20,000 ohms/volt, ±3 percent

1 — AC voltmeter, Hewlett-Packard model 400L (or equivalent)

1 — Mercury relay, WECo 291A (or equivalent)

3 — Resistors:

- 1 — 75 ohms (±1 percent), 1/2 watt, WECo 145A (or equivalent)
- 2 — 316 ohms (±1 percent), 1/2 watt, WECo 145A (or equivalent)

2 — Capacitors:

- 1 — 100 uf (±20 percent), WECo 602B (or equivalent)
- 1 — 40 uf (±20 percent), WECo 602A (or equivalent)

1 — Transformer, WECo Rep 120C (or equivalent)

1 — Switching diode, KS-16986-L2 (or equivalent).

B. Power Requirements

+18.0 (±0.5) Vdc — 100 mA

−18.0 (±0.5) Vdc — 75 mA

C. Test Procedure

4.07A ***Zener Voltage Test:***

(1) Connect +18.0 (±0.5) Vdc to terminal 1 and ground to terminals 5 and 17.

(2) The voltage between test point 14 and ground shall be +6.2 (±0.6) Vdc.

4.08A ***Threshold Test:***

(1) Connect the circuit pack to the suggested test circuit shown in Fig. 14A. Connect +18.0 (±0.5) Vdc to terminal 1, −18.0 (±0.5) Vdc to terminal 20, and ground to terminals 5 and 17. For this section of the test, place a short between pins 1 and 3 of the mercury relay.

(2) Set the frequency of the sine-wave generator to 600 Hz (±5 percent).

(3) Set the amplitude of the input sine wave at the primary of the transformer to 1.2 (±0.1) volts rms.

(4) The voltage between terminal 14 and ground shall be +6.5 (±0.8) Vdc.

(5) Increase the amplitude of the input sine wave to 2.0 (±0.1) volts rms.

(6) The voltage between terminal 14 and ground shall be less than or equal to +0.3 Vdc.

(7) Reduce the amplitude of the input sine wave until the output on terminal 14 switches to +6.5 (±0.8) Vdc. The amplitude of the input sine wave at the point of switching shall be 1.6 (±0.2) volts rms.

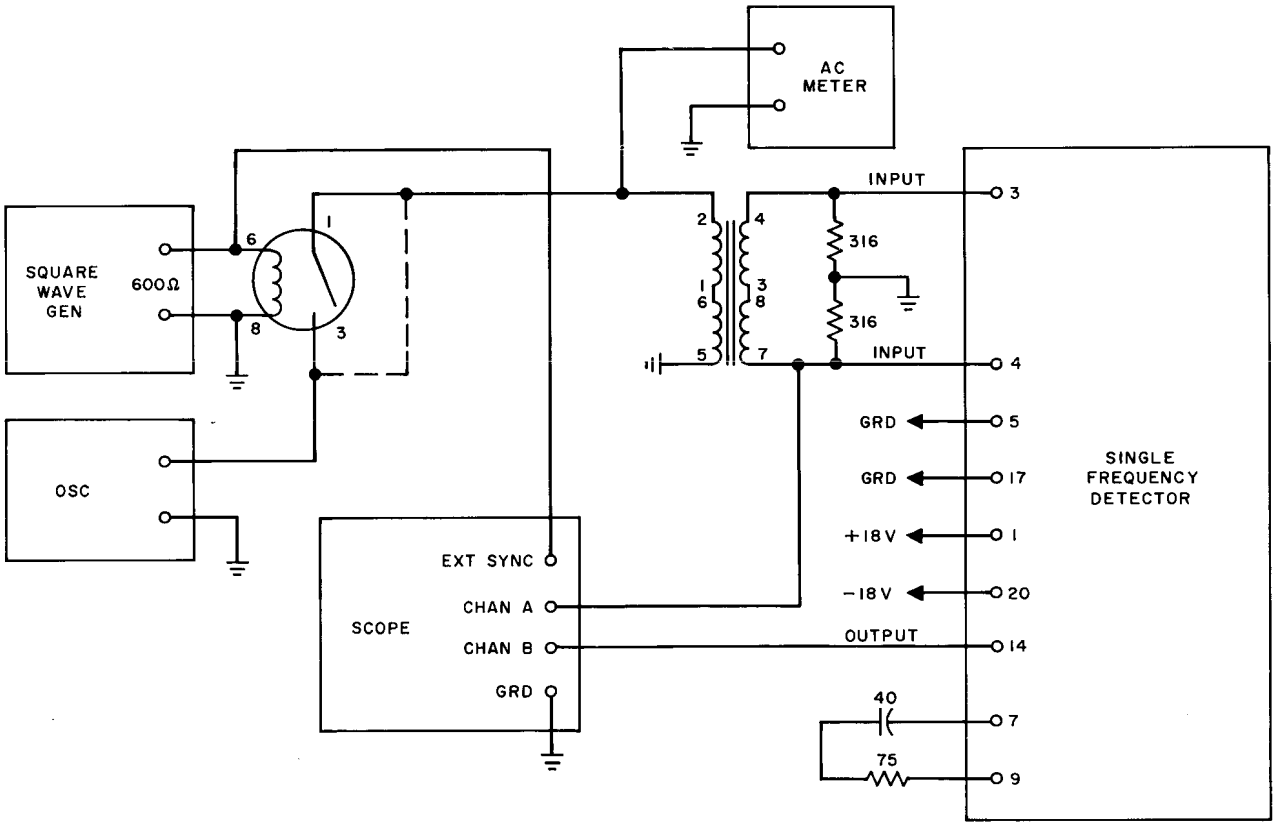


Fig. 14A — Single-Frequency Detector Test Circuit

4.09A ***Transient Test:***

(1) Connect the circuit pack to the suggested test circuit shown in Fig. 14A.

(2) Set the frequency of the sine-wave generator to 600 Hz (±5 percent).

(3) Temporarily short pin 1 to pin 3 of the mercury relay. Set the amplitude of the input sine wave at the primary of the transformer to 3.5 (±0.05) volts rms. Remove the short between pins 1 and 3 of the relay.

(4) Set the frequency of the square-wave generator to 2.0 Hz. Set the amplitude of the square-wave generator high enough to operate the mercury relay.

(5) Set the scope EXT SYNC TRIGGER to the (—) negative position. The output waveform at terminal 14 shall be as specified in Fig. 15A.

(6) Set the scope EXT SYNC TRIGGER to the (+) positive position. The output waveform at terminal 14 shall be as specified in Fig. 16A.

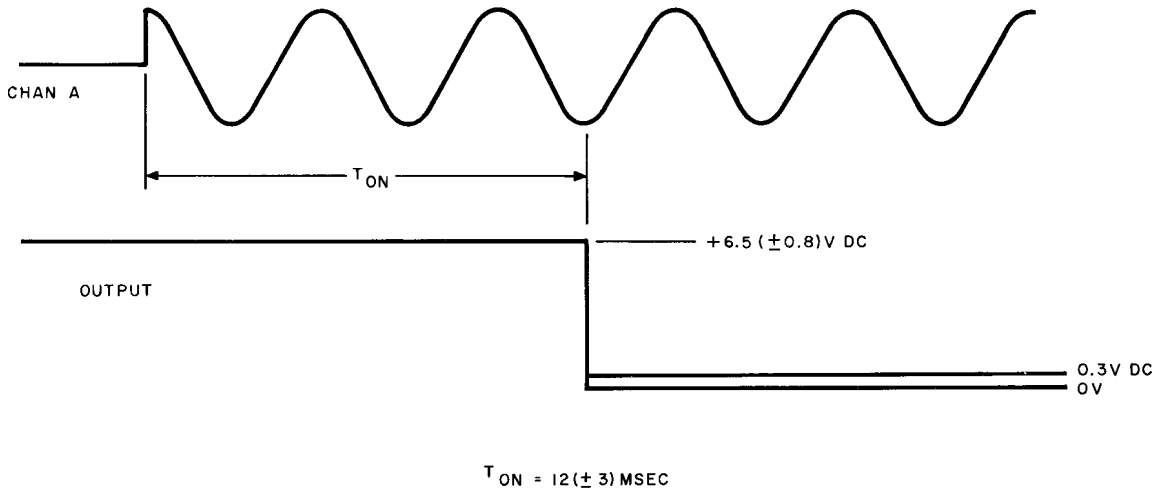


Fig. 15A — Single-Frequency Detector Test

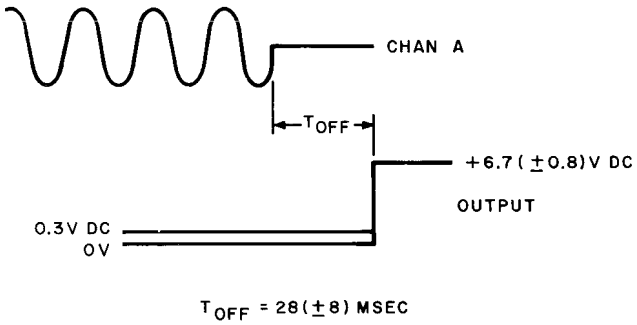


Fig. 16A — Single-Frequency Detector Test

4.10A ***Integrator-Slicer Test:***

(1) Connect the circuit pack to the suggested test circuit shown in Fig. 17A. Connect +18.0 (±0.5) Vdc to terminal 1, −18.0 (±0.5) Vdc to terminal 20, and ground to terminals 5 and 17.

(2) Set the frequency of the square-wave generator to 5 (±0.5) Hz.

(3) The input waveform shall be as specified in Fig. 18A.

(4) Set the scope EXT SYNC TRIGGER to the (−) negative position. The output waveform shall be as specified in Fig. 18A.

(5) Set the scope EXT SYNC TRIGGER to the (+) positive position. T_3 shall be as specified in Fig. 18A.

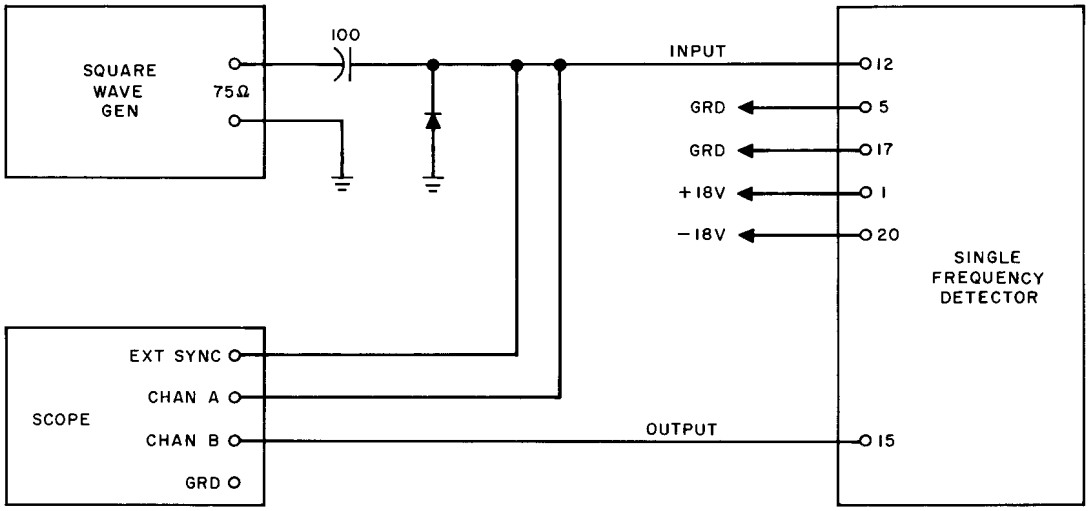


Fig. 17A — Single-Frequency Detector Test Circuit

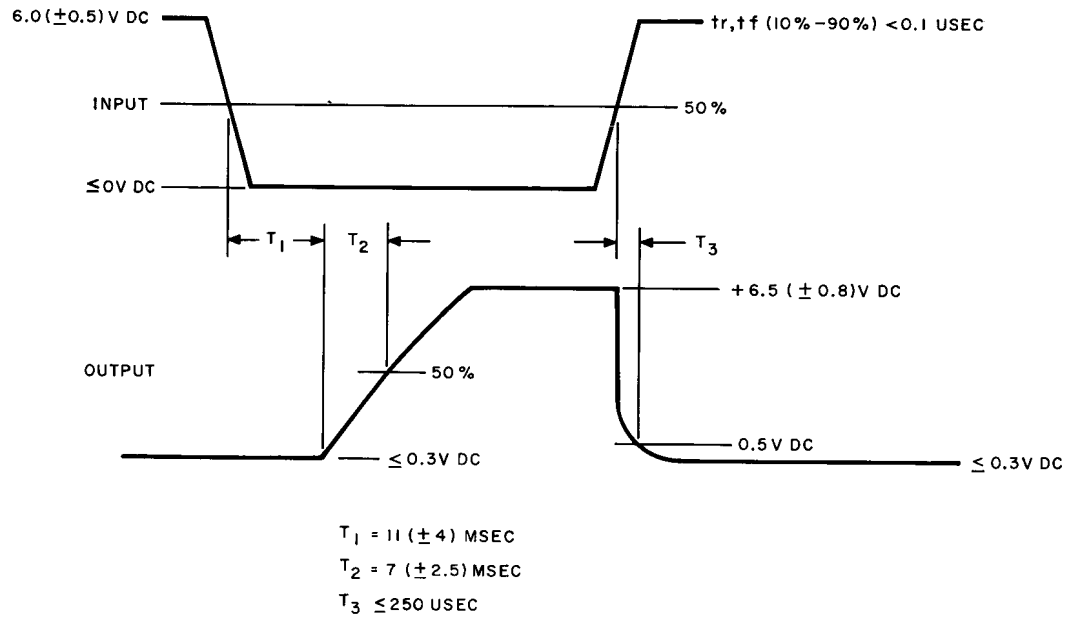
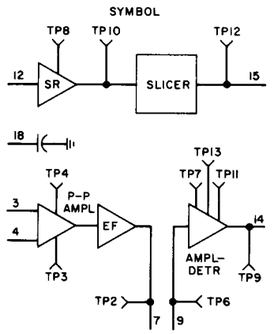


Fig. 18A — Single-Frequency Detector Test



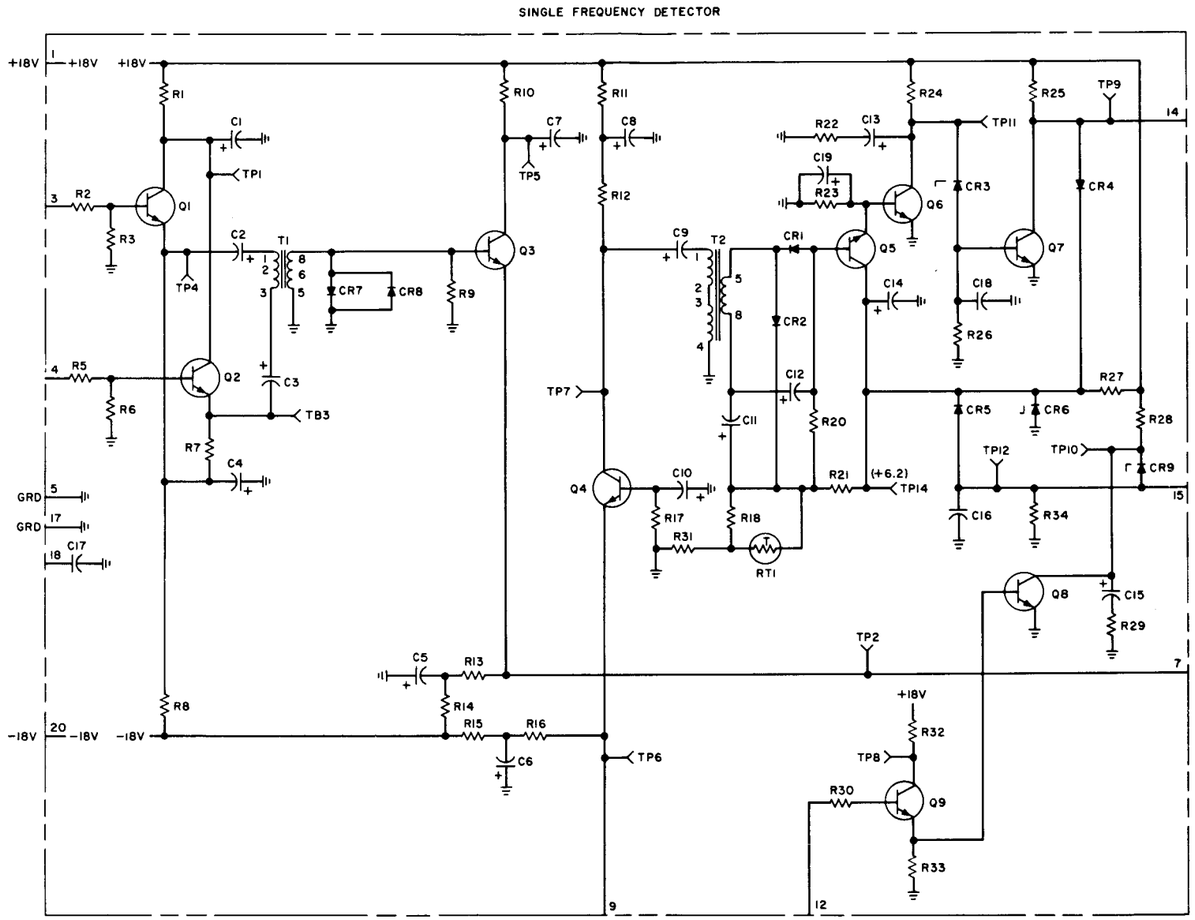


Fig. 19A — Single-Frequency Detector, Circuit Pack Assembly AR87 (A835183), Circuit Sketch

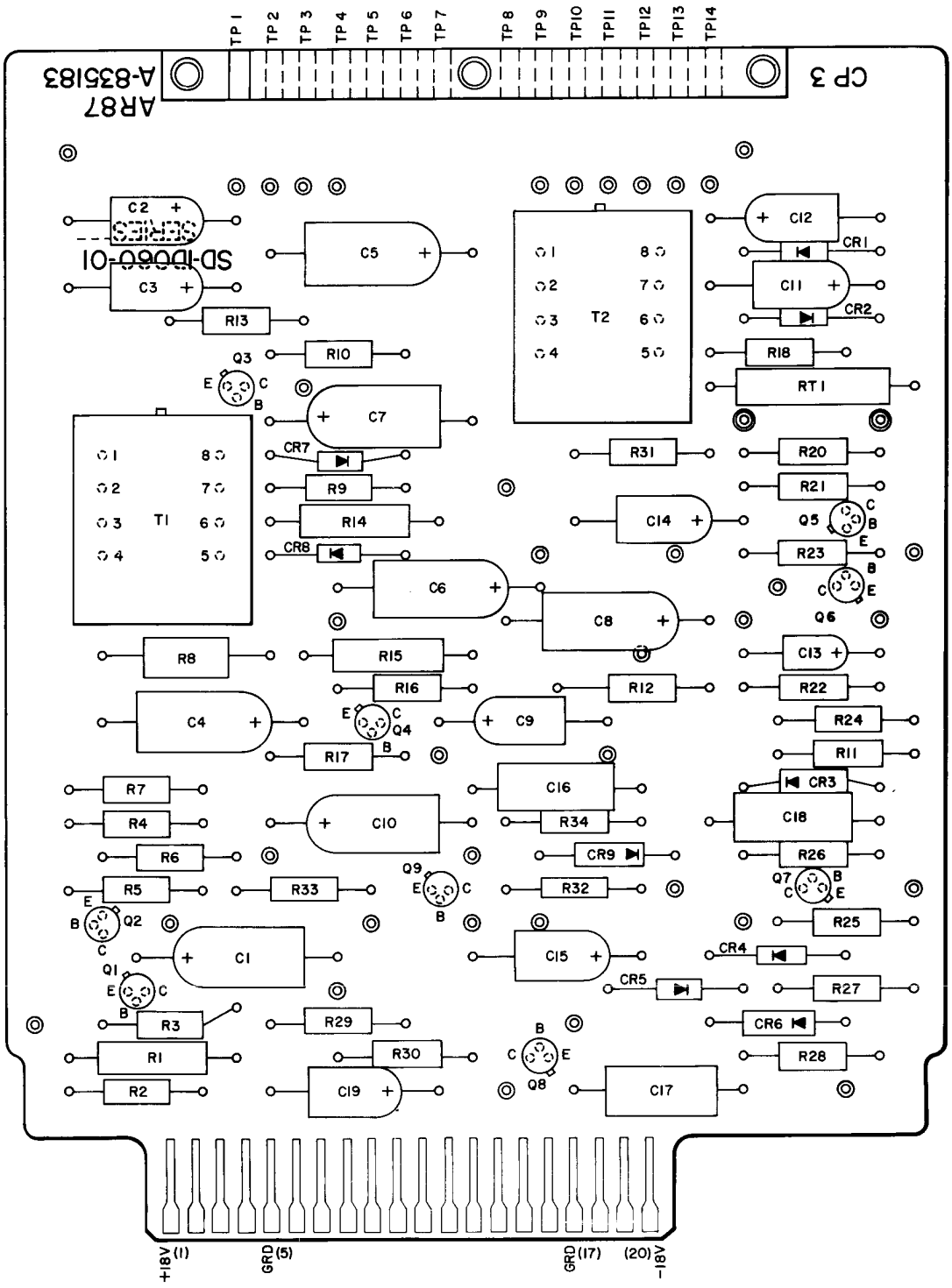


Fig. 20A — Single-Frequency Detector, Circuit Pack Assembly AR87 (A835183), Component Location

5A. AUTOMATIC GAIN CONTROL AMPLIFIERS (AGC1 AND AGC2) CIRCUIT PACK ASSEMBLIES AR88 AND AR89 (A835178 AND A835179)

5.01A *Circuit Description:* Each AGC circuit is dependent on the operation of the other AGC circuit. Either circuit is tested using the other circuit (known to be good) as signal reference. The following descriptions for each circuit pack are illustrated by circuit sketches which follow the test procedures.

5.02A *AGC1 (AR88):* This circuit pack contains two amplifier circuits and a variable-loss diode bridge. The received line signal is applied through terminals 8 and 7 to buffer amplifier Q1. Input signal level is adjusted by a flat-loss pad consisting of resistors R2, R3, R4, and R5. Output signals from the amplifier are applied to the diode bridge consisting of T1, T2, CR2A, CR2B, and R13 through R16. The ac impedance of the diodes is inversely proportional to the current being passed. The transmission loss of the bridge is determined by the potential difference between terminals 10 and 14 which varies directly with the line signal on terminal 8. The potential difference is controlled by AGC2 (AR89) circuits.

5.03A When receiving very weak signals, the potential difference between terminal 14 (positive) and terminal 10 (negative) is approximately zero and the transmission loss between the collector of Q1 and output terminal 13 is small. As the received signal level increases, the potential difference increases which also increases the bridge loss. Through this feedback action, an essentially constant bridge output is maintained at terminal 13.

5.04A The remaining amplifier on AR88 provides a "CARRIER ON" indication. When the AGC2 (AR89) circuits provide a carrier indication to the input terminal (12), the amplifier output terminal (15) is held at approximately +6.2 Vdc as the "CARRIER ON" indication. Without the AGC2 carrier indication, the input terminal receives approximately +6.0 Vdc which permits the amplifier to saturate. When the amplifier is saturated, the output terminal will be held to less than +0.5 Vdc.

5.05A The +12 Vdc on terminal 14 is also applied to the AGC2 circuits as a reference source.

5.06A *AGC2 (AR89):* This circuit pack contains the AGC amplifier, a rectifier, and the carrier detector circuit. Output signals from the AGC1 circuit pack diode bridge are applied to buffer amplifier Q1 through input terminal 6. Transistors Q2, Q3, Q4, and associated components make a feedback amplifier with an approximate gain of 90. The amplifier output is applied to both output terminal 10 and buffer amplifier Q5.

5.07A The output of amplifier Q5 is applied to the rectifier circuit CR2, CR3, R30, R32, RT1, and Q6. If line signals are not received, diodes CR2 and CR3 provide approximately −1.4 Vdc to the base of transistor Q6. This potential will prevent both Q6 and Q7 from conducting. When line signals are received, the negative half-cycles hold Q6 cut off and positive half-cycles, with amplitudes greater than +1.4 Vdc, permit Q6 and Q7 to conduct. Signals at the collector of Q6 are applied through R38 and terminal 11 to the diode bridge on AGC1 circuit pack AR88. The signals are filtered by R38 (on the AGC2 circuit pack) and C8 (on the AGC1 circuit pack).

5.08A Transistor Q7 provides a "CARRIER ON" indication when line signals are received and output terminal 13 is terminated by R8 on the AGC1 circuit pack. A "CARRIER ON" indication is approximately zero Vdc and a "CARRIER OFF" indication is approximately +6.2 Vdc.

Automatic Gain Control 1 Test

5.09A *The AGC1 Circuit Pack:* SD-1D060-01 sheet J4, must be tested in conjunction with an AGC2 circuit pack SD-1D060-01 sheet J5, or its equivalent. Therefore, an AGC2 circuit pack shall be contained in the test facility for the AGC1 circuit pack.

A. Test Equipment

1 — AGC2 circuit pack, SD-1D060-01 sheet J5 (or equivalent)

1 — Oscilloscope, Tektronix 533 with type CA plug-in unit (or equivalent)

2 — Probes, Tektronix P6006 (10X) (or equivalent)

1 — DC volt-ohmmeter, Hewlett-Packard 412A (or equivalent), DC accuracy ±1 percent, ohmmeter ±5 percent

1 — AC vacuum tube voltmeter, Hewlett-Packard 400L (or equivalent)

1 — Square-wave generator, Hewlett-Packard 211A (or equivalent)

1 — Sine-wave generator, harmonic distortion less than 0.5 percent, Hewlett-Packard 200CD (or equivalent)

1 — Mercury relay, WECo 291A (or equivalent)

1 — Wave analyzer, Hewlett-Packard 302A (or equivalent)

2 — Capacitors:

1 — 2.0 uf (±10 percent), WECo 579A (or equivalent)

1 — 5.0 uf (±20 percent), WECo 600B (or equivalent)

3 — Resistors:

1 — 562 ohms (±1 percent), 1/2 watt, WECo 145A (or equivalent)

1 — 31.6 ohms (±1 percent, 1/2 watt, WECo 145A (or equivalent)

1 — 1000 ohms (±1 percent), 1/2 watt, WECo 145A (or equivalent).

B. Power Requirements

+18.0 (±0.5) Vdc — 100 mA

−18.0 (±0.5) Vdc — 50 mA

C. Test Procedures

5.10A ***Resistance Test:***

(1) Five slotted machine screw terminals are located on the AGC1 circuit pack. The resistance between the screw terminals shall be as follows:

BETWEEN SCREW TERMINALS	RESISTANCE VALUE OHMS
1 and 2	866 (±5%)
2 and 3	487 (±5%)
3 and 4	287 (±5%)
4 and test point 8	365 (±5%)

(2) Insert a strap between screw terminals 1 and 5.

5.11A ***Zener Voltage Test (AGC1 Circuit Pack):***

(1) Apply ground to terminals 5 and 17, +18.0 (±0.5) Vdc to terminal 1, and −18.0 (±0.5) Vdc to terminal 20.

(2) The voltage between terminal 14 and ground shall be +12 (±1.5) Vdc.

(3) The voltage between test point 14 and ground shall be +6.2 (±0.45) Vdc.

5.12A ***Gain Control Test:***

(1) The gain control test of the AGC1 circuit pack is made in conjunction with the AGC2 circuit pack. Connect the circuit packs as in the suggested test circuit shown in Fig. 21A with the scope connected to terminal 10 of the AGC2 circuit packs. Connect power to both circuit packs as specified in 5.11A (1).

(2) Connect the sine-wave generator in series with a 2.0 uf capacitor to terminal 8 of the AGC1 circuit pack. Set the frequency of the generator to 1800 Hz (±5 percent). Set the output level of the generator to 0.

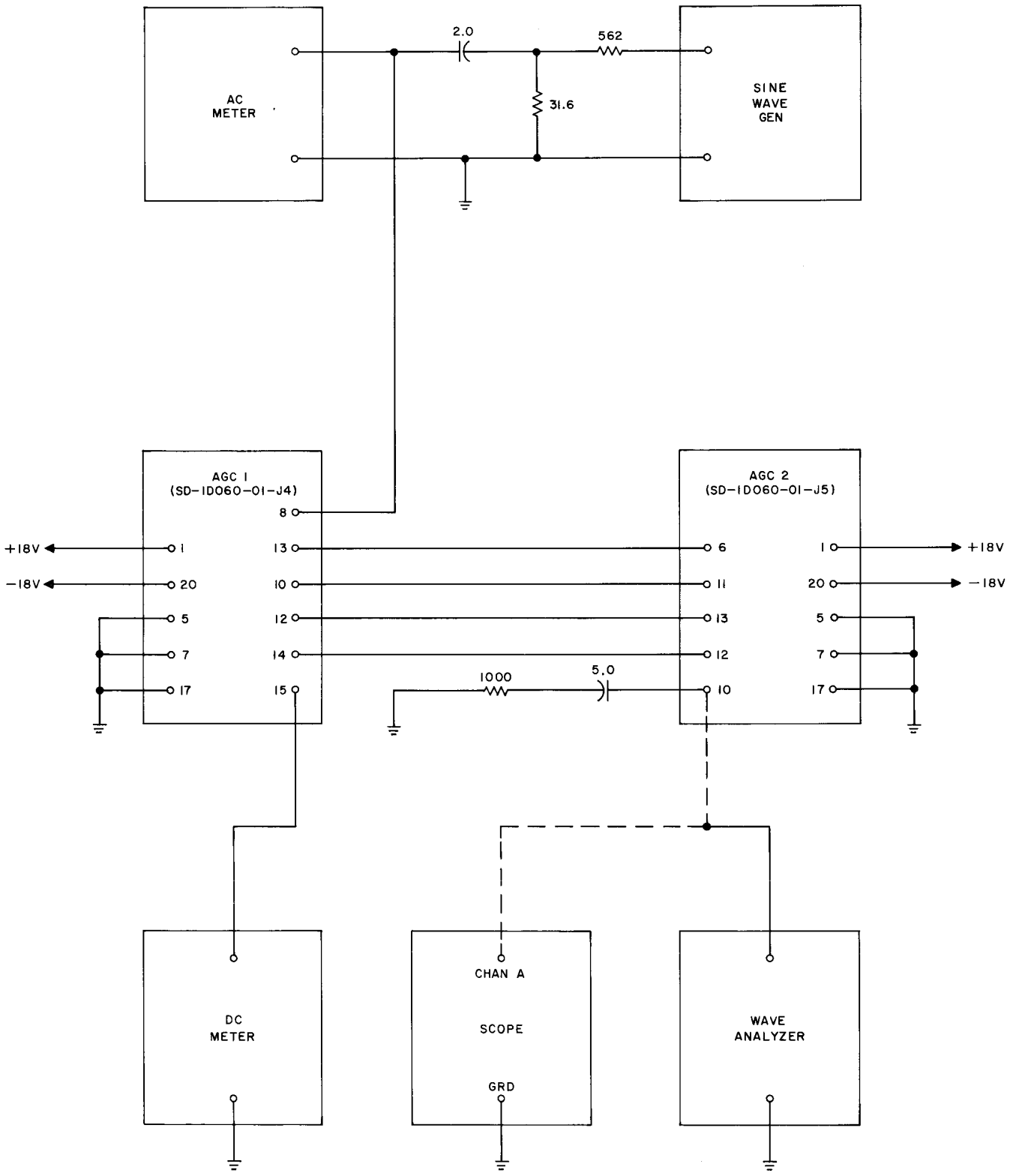


Fig. 21A — Automatic Gain Control 1 Test Circuit

(3) Slowly increase the output level of the generator until the carrier detector voltage on terminal 15 of the AGC1 circuit pack switches to +6.5 (±0.8) Vdc. The input voltage between terminal 8 and ground of the AGC1 circuit pack shall be 13.5 $\begin{pmatrix}-0.8\\+0.9\end{pmatrix}$ mV rms. Record the input level.

(4) The output waveform on terminal 10 of the AGC2 circuit pack shall be a sine-wave amplitude of 2.5 (±0.3) Vac peak-to-peak.

(5) Increase the input signal level between terminal 8 and ground of the AGC1 circuit pack to 78 (±1) mV rms. The output level on terminal 10 of the AGC2 circuit pack shall be a sine wave of amplitude 2.5 $\begin{pmatrix}+0.35\\-0.30\end{pmatrix}$ Vac peak-to-peak. The voltage on terminal 15 of the AGC1 circuit pack shall be +6.5 (±0.8) Vdc.

(6) Increase the input signal level between terminal 8 and ground of the AGC1 circuit pack to 450 (±5) mV rms. The output level on terminal 10 of the AGC2 circuit pack shall be a sine wave with an amplitude of 2.5 $\begin{pmatrix}+0.45\\-0.30\end{pmatrix}$ volts peak-to-peak. The voltage on terminal 15 of the AGC1 circuit pack shall be +6.0 (±0.8 Vdc.

5.13A ***Distortion Measurement:***

(1) The distortion measurement of the AGC1 circuit pack is made in conjunction with the AGC2 circuit pack. Connect the circuit packs to the suggested test circuit shown in Fig. 21A, with the wave analyzer connected to terminal 10 of the AGC2 circuit pack. Apply power to both circuit packs as in 5.11A (1).

(2) With the wave analyzer connected to terminal 10 of the AGC2 circuit pack, apply a 78 (±1) mV rms signal at 600 Hz (±5 percent) to input terminal 8 of the AGC1 circuit pack. Tune the wave analyzer to obtain a peak reading on the meter at the fundamental frequency of 600 Hz. Set the meter indication to 0 dB by adjusting the wave analyzer reference adjustment.

(3) Tune the wave analyzer for a peak meter reading in the vicinity of the second harmonic frequency of 1200 Hz. The meter should indicate 30 dB or lower at the second harmonic frequency.

5.14A ***Carrier Detector Response Time:***

(1) The carrier detector response test of the AGC1 circuit pack is made in conjunction with the AGC2 circuit pack. Connect the circuit packs to the suggested test circuit shown in Fig. 22A. Apply power to both circuit packs as in 5.11A (1).

(2) Set the frequency of the square-wave generator to approximately 1 Hz. Set the symmetry control to its center position and the 600-ohm output amplitude control to 0.

(3) Set the frequency of the sine-wave generator to 1800 Hz (±5 percent). Adjust the generator amplitude control until the input level at terminal 8 of the AGC1 circuit pack is 2 dB higher than the level recorded in 5.12A (3). Set the 600-ohm output amplitude control of the square-wave generator to its center position.

(4) Set the scope EXT SYNC TRIGGER selector to the (+) positive position. The input waveform on terminal 8 of the AGC1 circuit pack and the output waveform on terminal 15 of the AGC1 circuit pack shall be as specified in Fig. 23A.

(5) Set the scope EXT SYNC TRIGGER selector to the (−) negative position. The input and output waveforms shall be as specified in Fig. 24A.

Automatic Gain Control 2 Test:

5.15A ***The AGC2 Circuit Pack:*** SD-1D060-01, sheet J5, must be tested in conjunction with and AGC1 circuit pack, SD-1D060-01, sheet J4, or its equivalent. Therefore, an AGC1 circuit pack shall be contained in the test facility for the AGC2 circuit pack.

A. Test Equipment

1 — AGC1 circuit pack, SD-1D060-01 sheet J4 (or equivalent). (This circuit pack or its equivalent must have met requirements specified in previous test.)

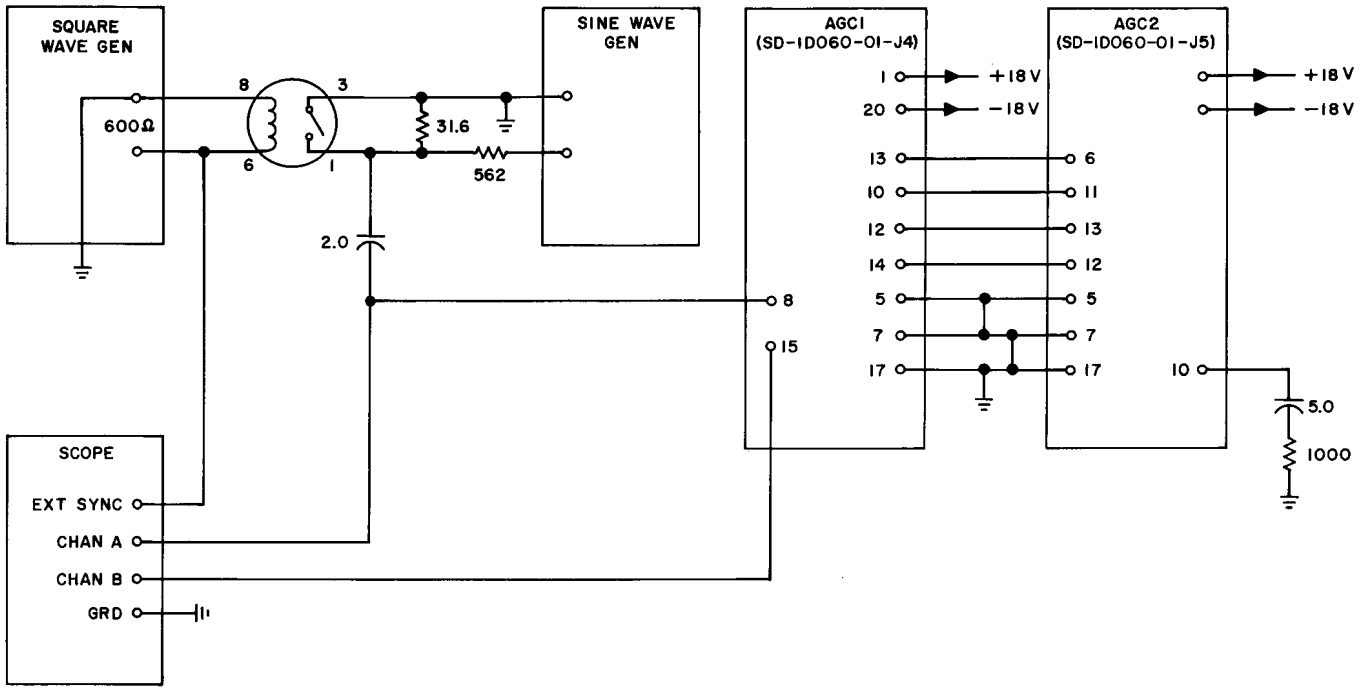


Fig. 22A — Automatic Gain Control 1 Test Circuit

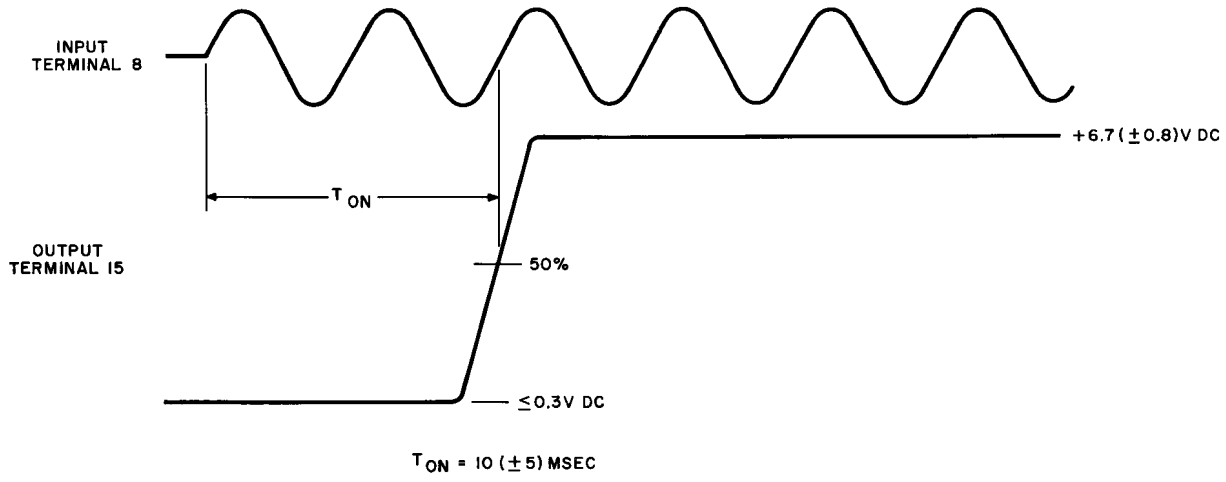


Fig. 23A — Automatic Gain Control 1 Test

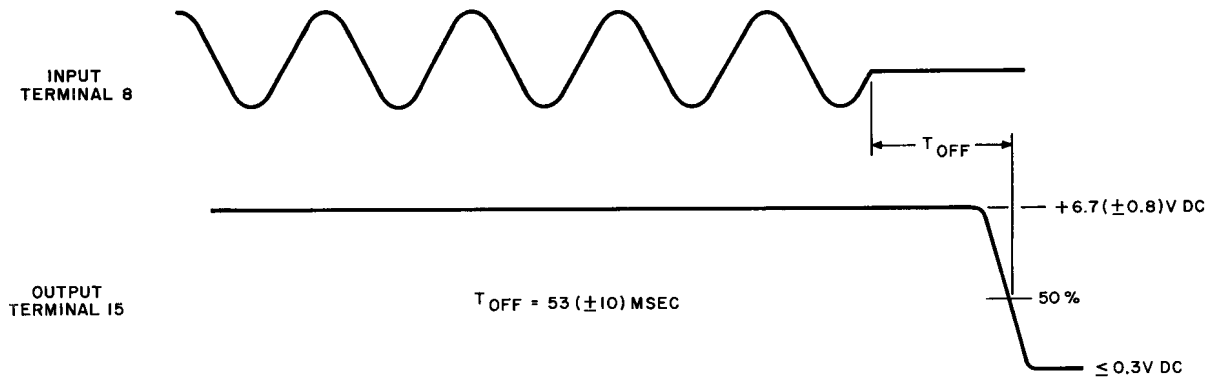


Fig. 24A — Automatic Gain Control 1 Test

1 — Oscilloscope, Tektronix 535A with type CA plug-in unit (or equivalent)

2 — Probes, Tektronix P6006 (10X) (or equivalent)

1 — DC volt-ohmmeter, Hewlett-Packard 412A (or equivalent). DC accuracy ±1 percent; ohmmeter ±5 percent

1 — AC voltmeter, Hewlett-Packard 400L (or equivalent)

1 — Square-wave generator, Hewlett-Packard 211A (or equivalent)

1 — Sine-wave generator, harmonic distortion less than 0.5 percent. Hewlett-Packard 200CD (or equivalent)

1 — Mercury relay, WECo 291A (or equivalent)

1 — Wave analyzer, Hewlett-Packard 302A (or equivalent)

2 — Capacitors:

2.0 uf (±10 percent), WECo 579A (or equivalent)

5.0 uf (±20 percent), WECo 600B (or equivalent)

3 — Resistors:

1 — 1000 ohms (±1 percent), 1/2 watt, WECo 145A (or equivalent)

1 — 562 ohms (±1 percent), 1/2 watt, WECo 145A (or equivalent)

1 — 31.6 ohms (±1 percent), 1/2 watt, WECo 145A (or equivalent)

1 — Test set such as shown in Fig. 26A.

B. Power Requirements

+18.0 (±0.5) Vdc — 100 mA

−18.0 (±0.5) Vdc — 50 mA

C. Test Procedures

5.16A ***Zener Voltage Test:*** Apply ground to terminals 5 and 17, +18.0 (±0.5) Vdc to terminal 1, and +18.0 (±0.5) Vdc to terminal 20. The voltage between test point 10 and ground shall be −12.0 (±1.5) Vdc.

5.17A ***Gain Adjustment:***

(1) The gain adjustment of the AGC2 circuit pack is made in conjunction with the AGC1 circuit pack. Connect the circuit packs to the suggested test circuit shown in Fig. 25A. Connect power to both circuit packs as specified in 5.18A.

(2) Five numbered strapping pins are located on the AGC2 circuit pack. This section of the test will determine which pins, if any, are to be strapped. Connect the test set shown in Fig. 26A to the five strapping pins located on the AGC2 circuit pack. Set both switches to position 1.

(3) Connect the sine-wave generator in series with a 2.0 uf capacitor to terminal 8 of the AGC1 circuit pack as shown in Fig. 25A. Set the frequency of the generator to 1800 Hz (±5 percent) and adjust the amplitude to obtain a 13.1 (±0.05) mV rms signal between terminal 8 and ground of the AGC1 circuit pack. The voltage between terminal 15 and ground shall be +6.5 (±0.8) Vdc.

(4) Rotate switches A and B on the test set, beginning with both switches at position 1, according to the sequence given in Table C, until the voltage between terminal 15 and ground on the AGC1 circuit pack switches to less than +0.3 Vdc. Note the position of the test set switches.

(5) Using the test set switch positions obtained in (4) consult Table C to determine which pins should be strapped.

(6) Remove the circuit pack from the test circuit and strap the appropriate pins according to the instructions given in A-A of AGC2 circuit pack assembly drawing A-835179.

Note: Subsequent strap changes may be required only if components are replaced.

5.18A ***Gain Control Test:***

(1) The gain control test of the AGC2 circuit pack is made in conjunction with the AGC1 circuit pack. Connect the circuit packs to the suggested test circuit shown in Fig. 27A with the scope connected to terminal 10 of the AGC2 circuit pack. Apply power to both circuit packs as specified in 5.16A.

(2) Set the frequency of the sine-wave generator to 1800 Hz (±5 percent). Set the output level of the generator to 0.

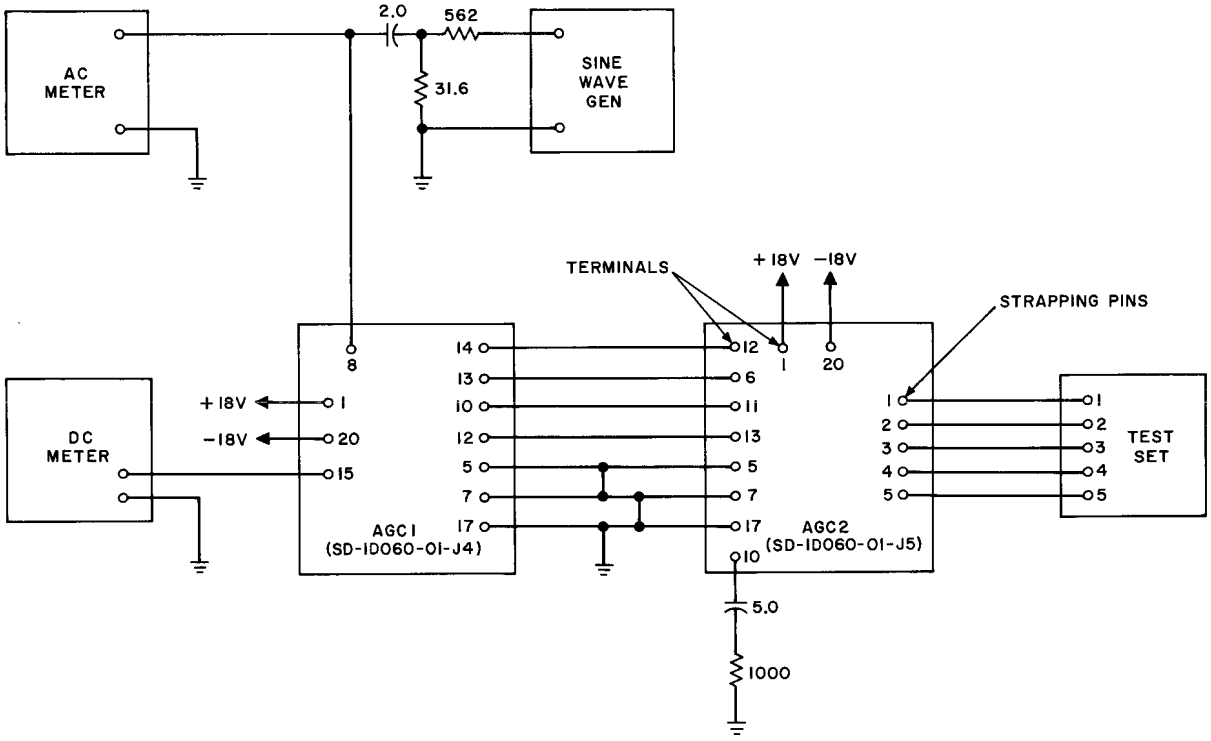


Fig. 25A — Automatic Gain Control 2 Test Circuit

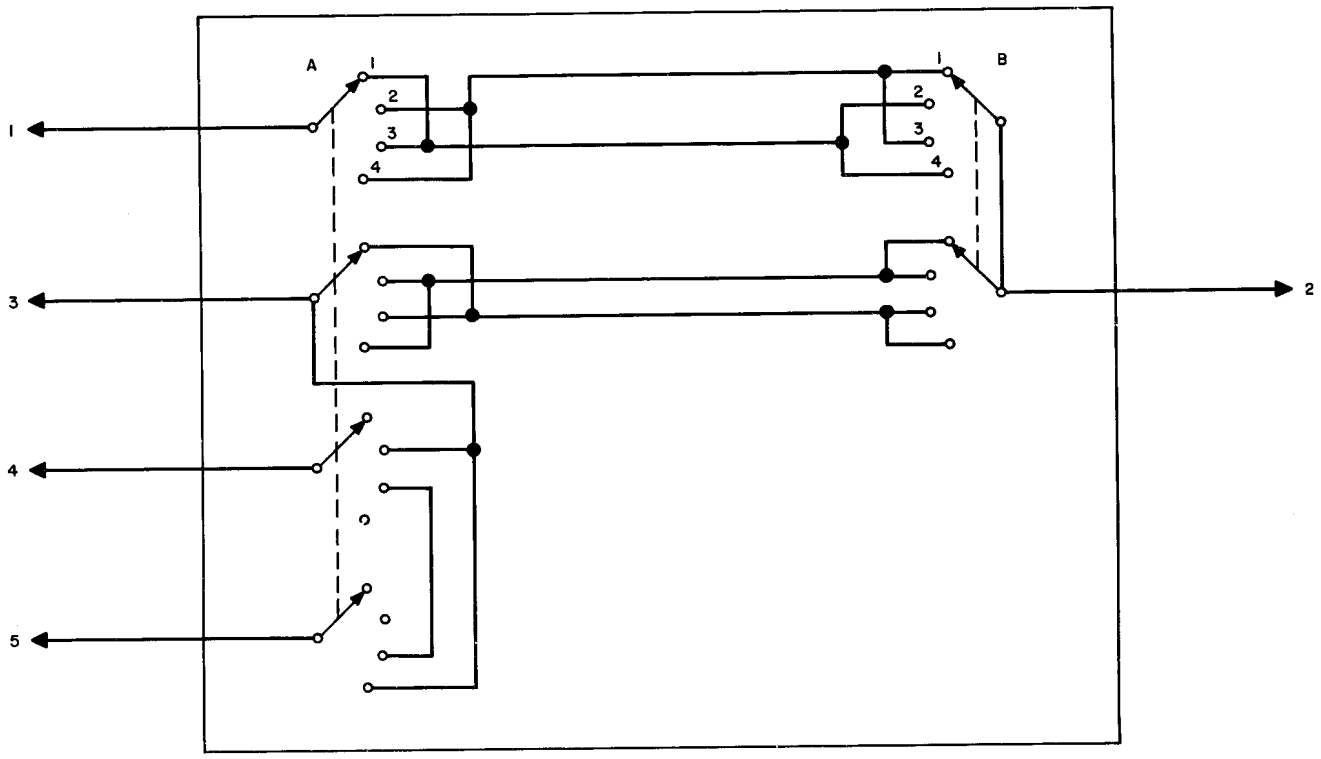


Fig. 26A — Automatic Gain Control 2 Test Set

TABLE C

STRAPPING FOR PIN POSITION

TEST SET (STEP 4) SWITCH POSITIONS		CHECK INDICATES PINS TO BE STRAPPED				TOTAL RESISTANCE BETWEEN PINS 1 AND 5
SWITCH A	SWITCH B	1 TO 2	2 TO 3	3 TO 4	4 TO 5	OHMS
1	1					2307
1	2	√				2145
1	3		√			1991
1	4	√	√			1829
2	4			√		1688
2	3	√		√		1526
2	2		√	√		1372
2	1	√	√	√		1210
3	1				√	1079
3	2	√			√	935
3	3		√		√	781
3	4	√	√		√	619
4	4			√	√	478
4	3	√		√	√	316
4	2		√	√	√	162
4	1	√	√	√	√	Less than 1

(3) Slowly increase the output level of the generator until the carrier detector voltage on terminal 15 of the AGC1 circuit pack switches to +6.5 (±0.8) Vdc. The input level between terminal 8 and ground of the AGC1 circuit pack shall be 13.5 (±0.4) mV rms. Record the input level.

Note: After the initial gain adjustment and upon subsequent testing of the AGC2 circuit pack, the input level requirements when the carrier detector voltage switches to +6.5 (±0.8) Vdc shall be 13.5 $\begin{pmatrix}+0.9\\-0.8\end{pmatrix}$ mV rms.

(4) The output waveform on terminal 10 of the AGC2 circuit pack shall be a sine-wave amplitude of 2.5 (±0.3) Vac peak-to-peak.

(5) Increase the input signal level between terminal 8 and ground of the AGC1 circuit pack to 78 (±1) mV rms. The output level on terminal 10 of the AGC2 circuit pack shall be a sine wave of amplitude 2.5 $\begin{pmatrix}+0.35\\-0.30\end{pmatrix}$ Vac. The voltage on terminal 15 of the AGC1 circuit pack shall be +6.5 (±0.8) Vdc.

(6) Increase the input signal level between terminal 8 and ground of the AGC1 circuit pack to 450 (±5) mV rms. The output level on terminal 10 of the AGC2 circuit pack shall be a sine-wave amplitude of 2.8 $\begin{pmatrix}+0.45\\-0.30\end{pmatrix}$ volts peak-to-peak. The voltage on terminal 15 of the AGC1 circuit pack shall be +6.5 (±0.8) Vdc.

5.19A ***Distortion Measurement:***

(1) The distortion measurement of the AGC2 circuit pack is made in conjunction with the AGC1 circuit pack. Connect the circuit packs to the suggested test circuit shown in Fig. 27A, with the wave analyzer connected to terminal 10

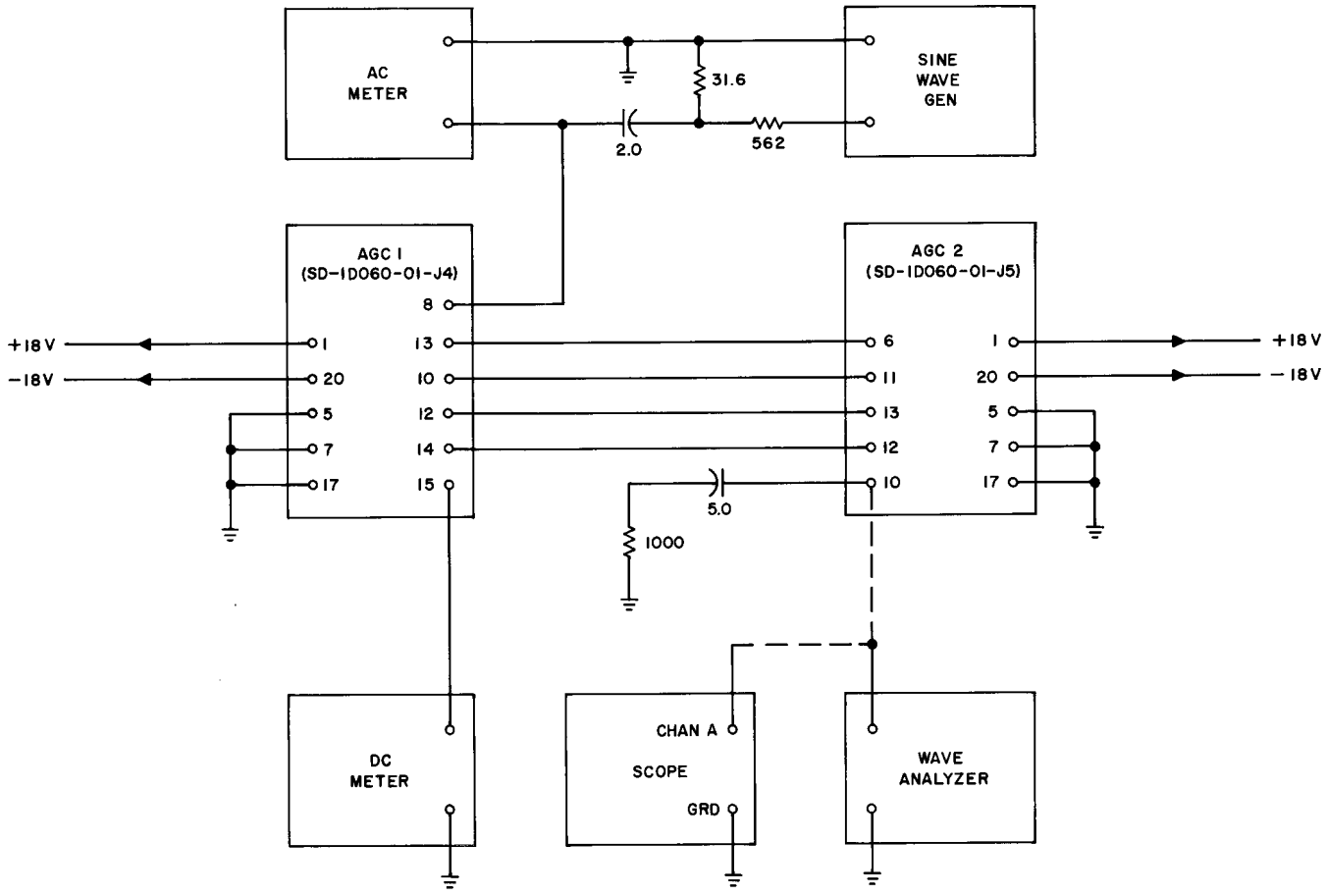


Fig. 27A — Automatic Gain Control 2 Test Circuit

of the AGC2 circuit pack. Apply power to both circuit packs as in 5.16A.

(2) With the wave analyzer connected to terminal 10 of the AGC2 circuit pack, apply a 78 (±1) mV rms signal at 600 Hz (±5 percent) to input terminal 8 of the AGC1 circuit pack. Tune the wave analyzer to obtain a peak reading on the meter at the fundamental frequency of 600 Hz. Set the meter indication to 0 dB by adjusting the wave analyzer reference adjustment.

(3) Tune the wave analyzer for a peak meter reading in the vicinity of the second harmonic frequency of 1200 Hz. The meter should indicate —30 dB or lower at the second harmonic frequency.

5.20A ***Carrier Detector Response Time:***

(1) The carrier detector response test of the AGC2 circuit pack is made in conjunction with the AGC1 circuit pack. Connect the circuit packs to the suggested test circuit shown in Fig. 28A. Apply power to both circuit packs as in 5.16A.

(2) Set the frequency of the square-wave generator to 1 Hz. Set the symmetry control to its center position and the 600-ohm output control to 0.

(3) Set the frequency of the sine-wave generator to 1800 Hz (±5 percent). Adjust the generator amplitude control until the input level at terminal 8 of the AGC1 circuit pack is 2 dB higher than the level recorded in 5.18A (3). Set the 600-ohm output amplitude control of the square-wave generator to its center position.

(4) Set the scope EXT SYNC TRIGGER selector to the (+) positive position. The input waveform on terminal 8 of the AGC1 circuit pack and the output waveform on terminal 15 of the AGC1 circuit pack shall be as specified in Fig. 29A.

(5) Set the scope EXT SYNC TRIGGER selector to the (—) negative position. The input and output waveforms shall be as specified in Fig. 30A.

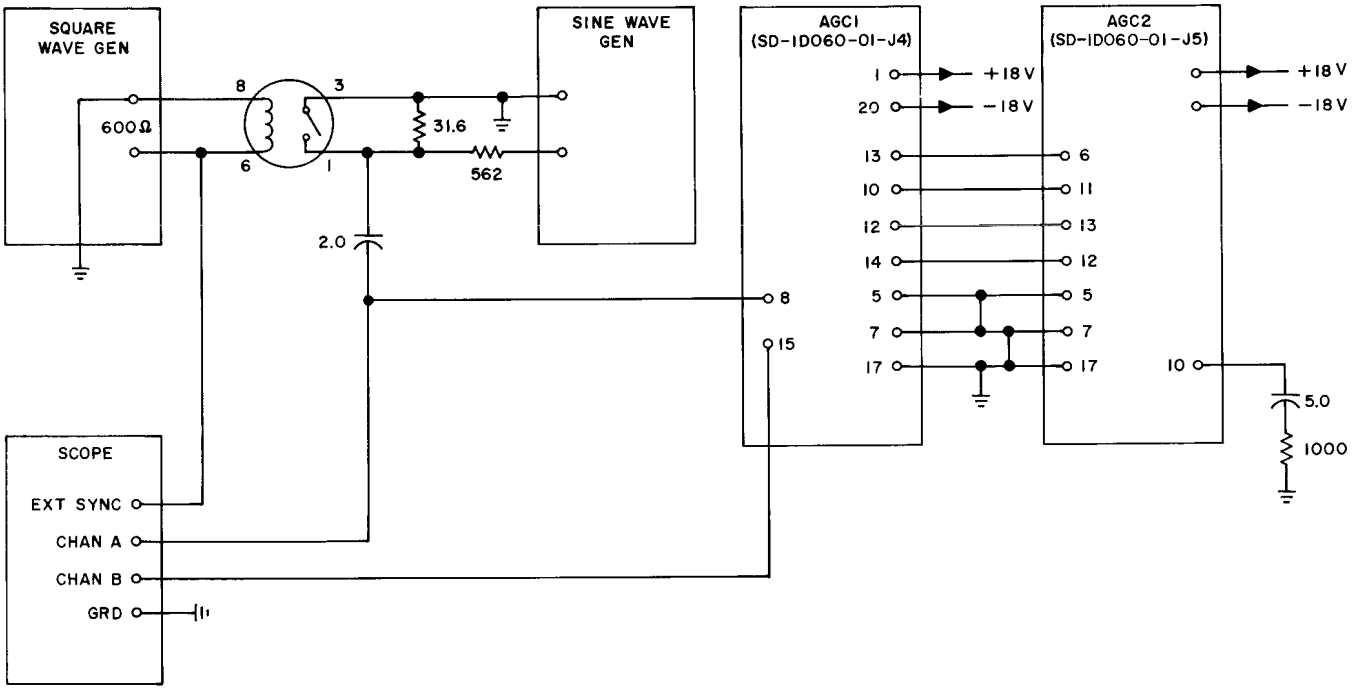


Fig. 28A — Automatic Gain Control 2 Test Circuit

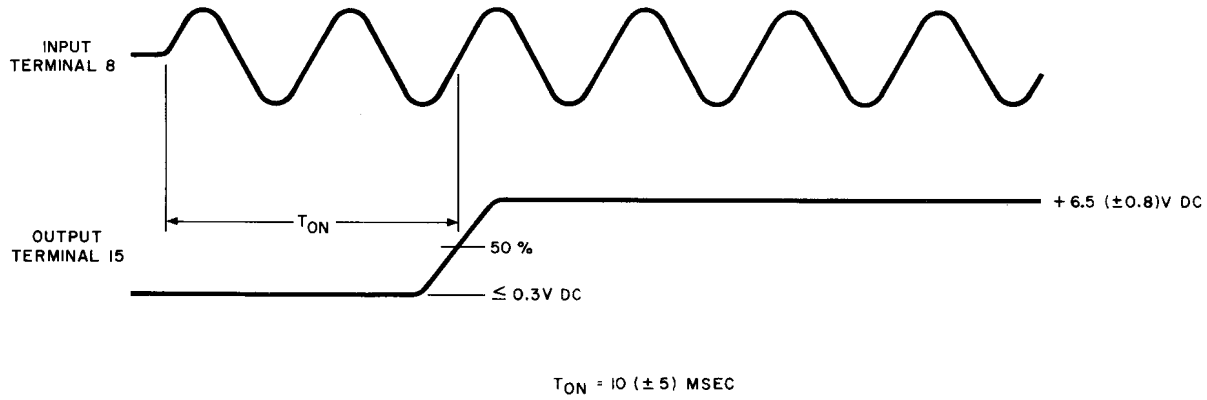


Fig. 29A — Automatic Gain Control 2 Test

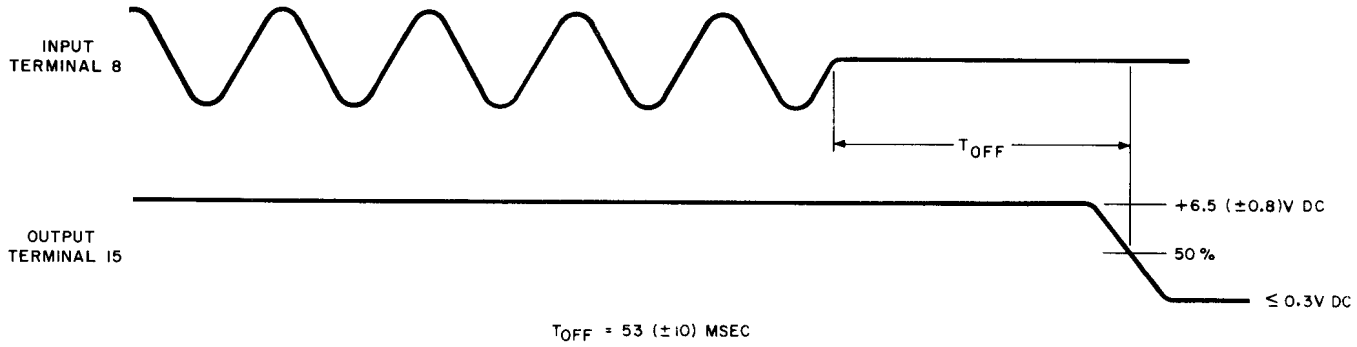


Fig. 30A — Automatic Gain Control 2 Test

SYMBOL

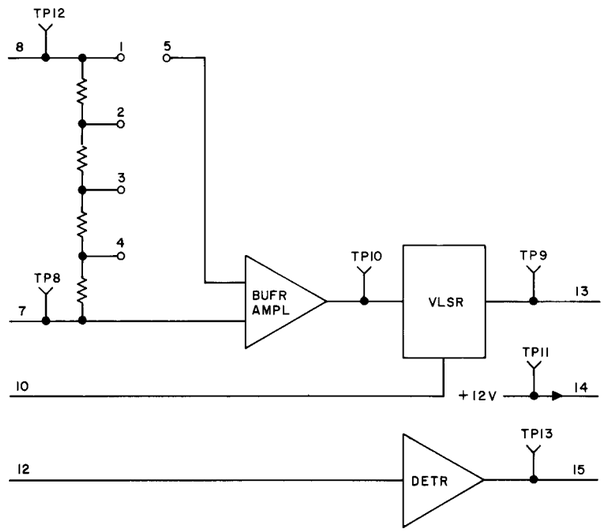


TABLE A

PAD LOSS	STRAP TERMINALS
0	1-5
5	2-5
10	3-5
15	4-5

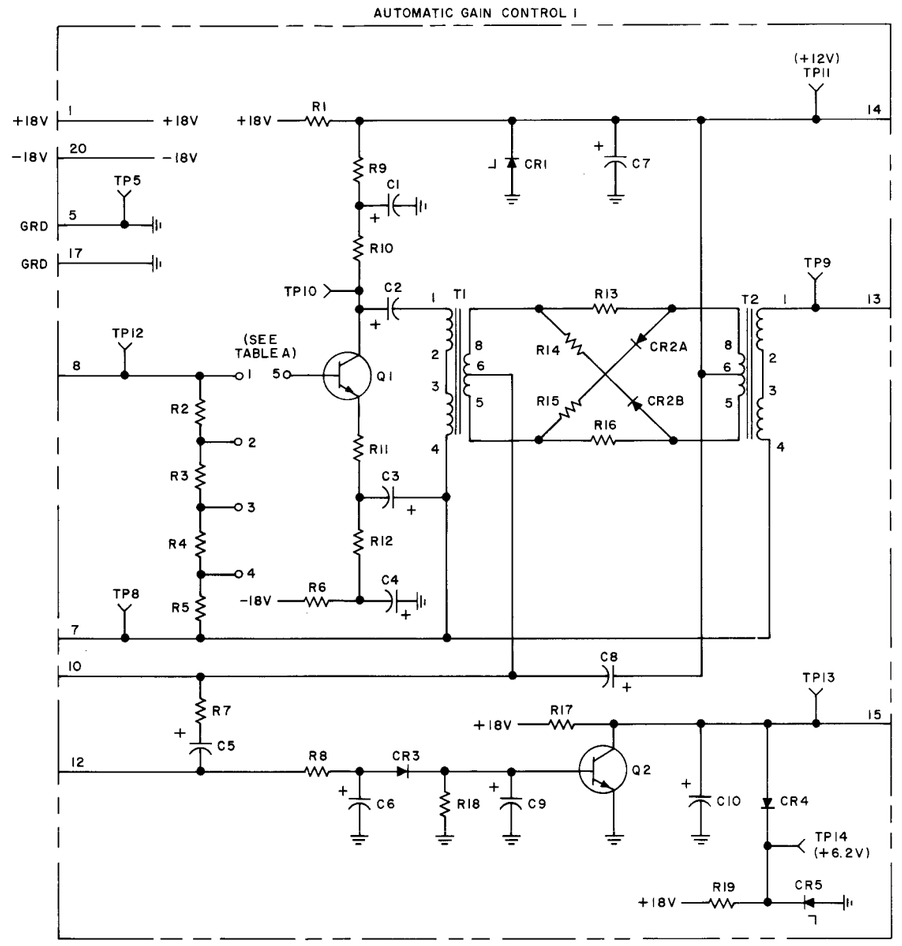


Fig. 31A — Automatic Gain Control 1, Circuit Pack Assembly AR88 (A835178), Circuit Sketch

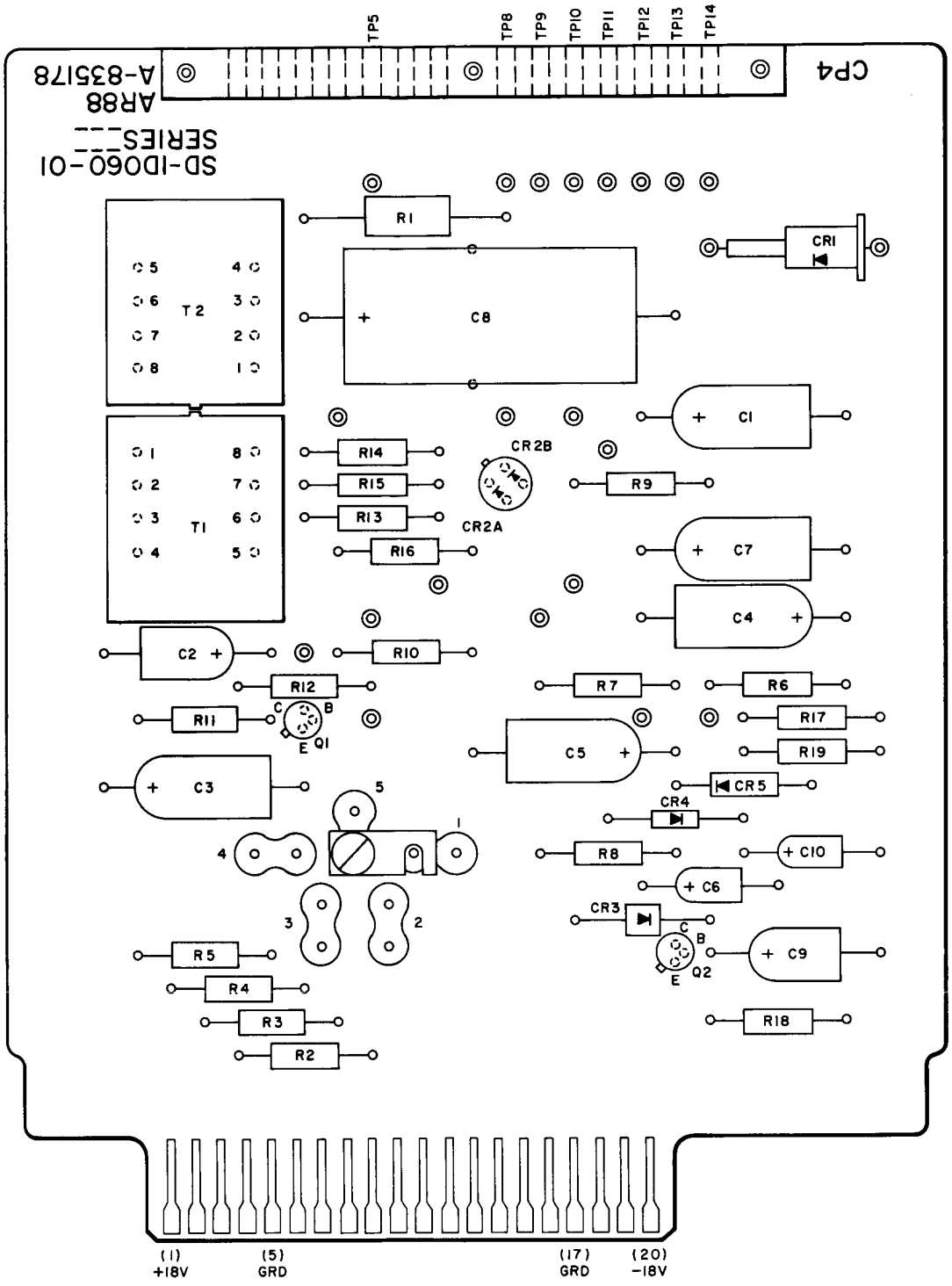
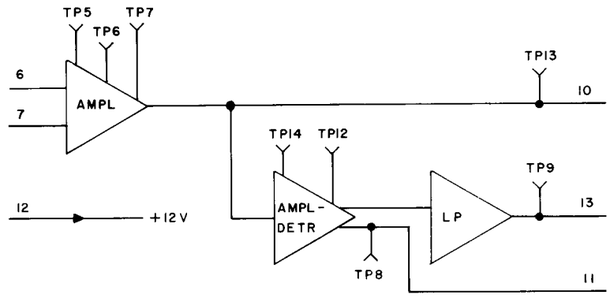


Fig. 32A — Automatic Gain Control 1, Circuit Pack Assembly AR88 (A835178), Component Location

SYMBOL



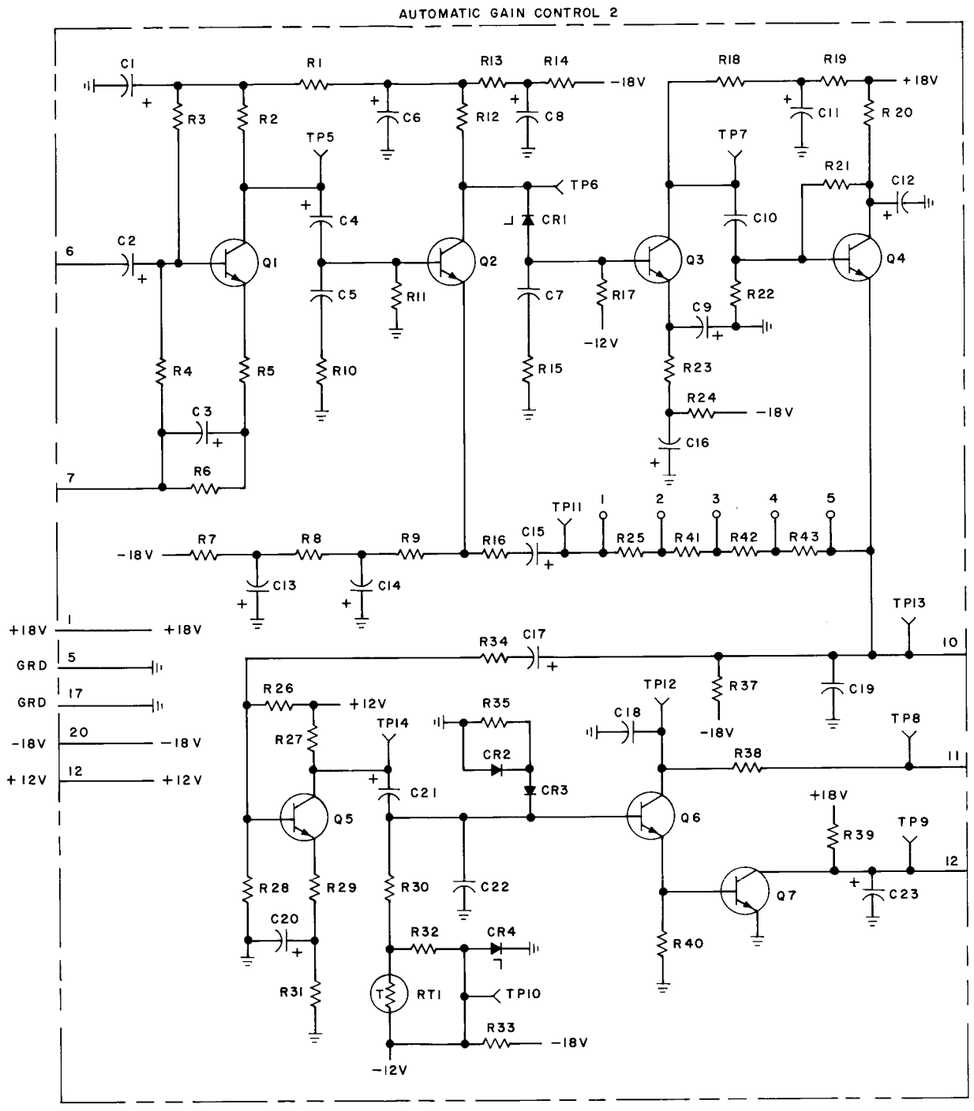


Fig. 33A — Automatic Gain Control 2, Circuit Pack Assembly AR89 (A835179), Circuit Sketch

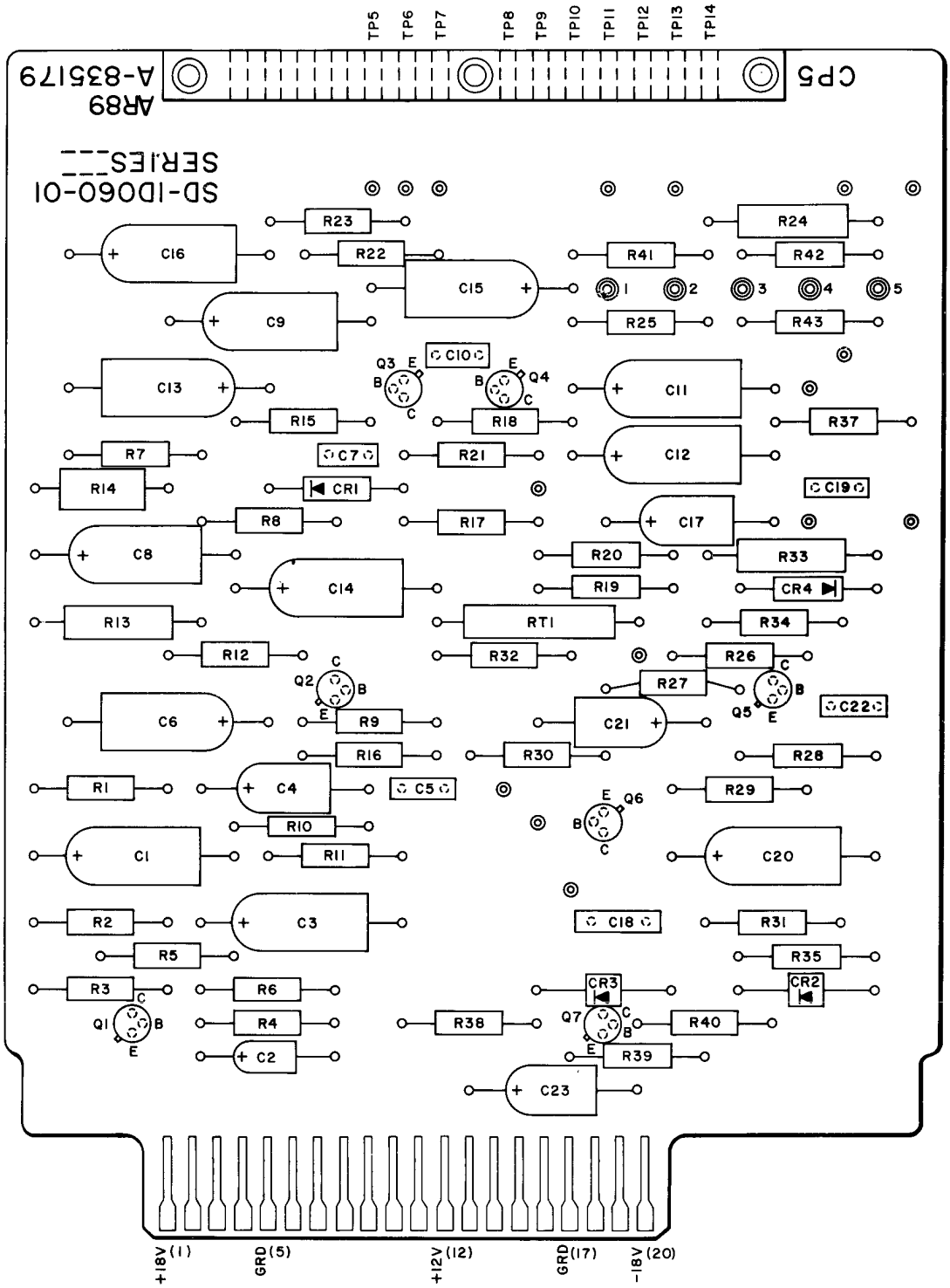


Fig. 34A — Automatic Gain Control 2, Circuit Pack Assembly AR89 (A835179), Component Location

6A. TRANSMITTER OUTPUT CIRCUIT PACK AR90 (A835182)

6.01A *Circuit Description:* The AR90 circuit pack contains two identical modulators and a differential line amplifier. The following description is illustrated by a circuit sketch that follows the test procedures.

6.02A Applied input square-wave signals on terminals 3 and 10 are amplified by Q1 and Q2, respectively. Output signals at terminals 4 and 6 are applied to separate external low-pass filters. The dc biased sine-wave signals from the filters are applied through terminals 11 and 12 to the envelope modulators.

6.03A Components CR1, CR2, R1, R2, R3, and T1 are used for one modulator circuit; and CR6, CR7, R9, R10, R11, and T2 compose the remaining modulator circuit. Input signals on terminals 15 and 16 are a phase-modulated square wave and its inverse, which will be amplitude-modulated by the sine wave applied on terminal 11. As the applied square wave on terminal 16 switches from +6.2 Vdc to less than +0.5 Vdc, CR2 conducts and shorts terminal 5 of T1 to ground. At the same time, CR1 is cut off and the signal on terminal 11 is applied through R1 and the transformer winding.

6.04A During the next half-cycle of the phase-modulated square-wave signal, CR1 conducts and the signal on terminal 11 is applied through R3 and the transformer winding in the opposite direction. The signal on the transformer secondary winding is an ac waveform with an envelope determined by the signal applied through terminal 11 with a carrier frequency determined by the phase-modulated square-wave signals applied through terminals 15 and 16. Similar operation, except for component nomenclature, applies to the remaining modulator circuit.

6.05A The two ac waveforms generated by the two modulators are applied through separate external low-pass filters to amplifier input terminals 36 and 38, respectively. The input signals are summed and amplified by differential amplifier Q3 and Q4. The amplifier gain is adjusted by strapping R16 through R23 to achieve nominal line levels of 0, —3, —6, and —9 dBm.

Transmitter Output Test:

A. Test Equipment

1 — Oscilloscope, Tektronix 533 with type CA plug-in unit (or equivalent)

2 — Probes, Tektronix P6006 (10X) (or equivalent)

1 — Oscillator, Hewlett-Packard 200CD (or equivalent)

1 — 0- to 10-volt dc voltmeter, 20,000 ohm/volt, calibrated to 0.5 percent full scale accuracy

1 — Square-wave generator, Hewlett-Packard 211A (or equivalent)

1 — Ohmmeter, Hewlett-Packard 412A (or equivalent) ±5 percent accuracy

1 — 0- to 10-uA dc meter, ±3 percent, Hewlett-Packard 412A (or equivalent)

1 — Transformer, WECo Rep 120C (or equivalent)

1 — AC voltmeter, Hewlett-Packard 400L (or equivalent)

2 — DPDT switches

1 — Inductor, 0.115h (±2 percent), WECo 1592A (or equivalent)

3 — Capacitors:

1 — 40 uf (±20 percent), WECo 602A (or equivalent)

2 — 0.0392 uf (±2 percent), WECo 570K (or equivalent)

1 — Switching diode, KS-16986-L2 (or equivalent)

7 — Resistors:

2 — 316 ohms (±1 percent), 1/2 watt, WECo 145A (or equivalent)

2 — 5260 ohms (±1 percent), 1/2 watt, WECo 145A (or equivalent)

1 — 5110 ohms (±1 percent), 1/2 watt, WECo 221A (or equivalent)

1 — 1.78 meg (±1 percent), 1/2 watt, WECo 221A (or equivalent)

1 — 600 ohms (±1 percent), 1/2 watt, WECo 221A (or equivalent).

B. Power Requirements

+18.0 (±0.5) Vdc — 50 mA

−18.0 (±0.5) Vdc — 25 mA

C. Test Procedures

6.06A ***Resistance Measurement:***

(1) Located on the circuit pack are four numbered slotted machine screw strapping terminals. The resistance between the terminals shall be as follows:

BETWEEN SCREW TERMINALS	RESISTANCE VALUE OHMS
1 and 2	220 (±5%)
2 and 3	150 (±5%)
3 and 4	100 (±5%)

(2) The resistance between screw terminal 4 and the circuit pack plug terminal 20 shall be 2940 ohms (±5 percent).

(3) Insert a strap between terminals 1 and 4.

6.07A ***Diode Leakage Test:*** Connect ground to terminals 5 and 17. Connect +18.0 (±0.5) Vdc in series with 1.78-meg resistor to terminals 15, 16, 13, and 14 as shown in Fig. 35A. The current drawn from the +18 volt supply shall be less than 0.2 uA dc.

6.08A ***Zener Voltage Test:*** Connect ground to terminals 4, 5, 6, and 17, and +18.0 (±0.5) Vdc to terminal 1. The voltage between test point 1 and ground shall be +8.2 (±0.45) Vdc when measured with a voltmeter calibrated to 0.5 percent accuracy.

6.09A ***Square-Wave Driver Test:***

(1) Connect ground to terminals 5 and 17 and +18.0 (±0.5) Vdc to terminal 1.

(2) Connect the circuit pack to the suggested test circuit shown in Fig. 36A using the output of the square-wave generator. Set the symmetry control to the center position.

(3) The input waveforms on terminals 3 and 10 and the output waveforms on terminals 4 and 6 shall be as specified in Fig. 37A.

6.10A ***Line Amplifier Test:***

(1) Connect the circuit pack to the suggested test circuit shown in Fig. 38A. Frequency of oscillator shall be 1800 Hz (±5 percent).

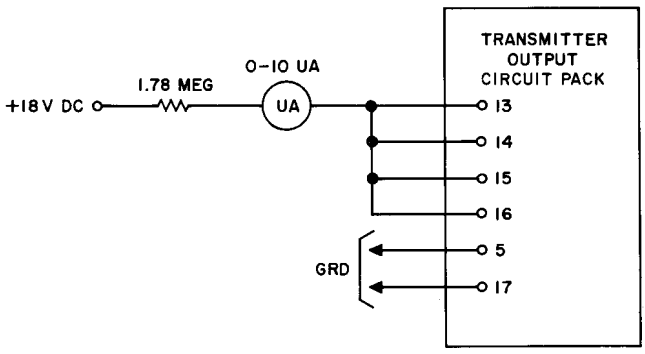


Fig. 35A — Transmitter Output Test

(2) With both switches set to position 1, adjust the oscillator to produce a 1.0 (±0.05) Vac rms signal between input terminal 13 and ground and between input terminal 14 and ground. The output voltage between terminals 7 and 9 shall be 1.7 (±0.25) Vac rms.

(3) With both switches set to position 2, adjust the oscillator to produce a 1.0 (±0.05) Vac rms signal between the input terminal 15 and ground and between input terminal 16 and ground. The output voltage between terminals 7 and 9 shall be 1.7 (±0.25) Vac rms.

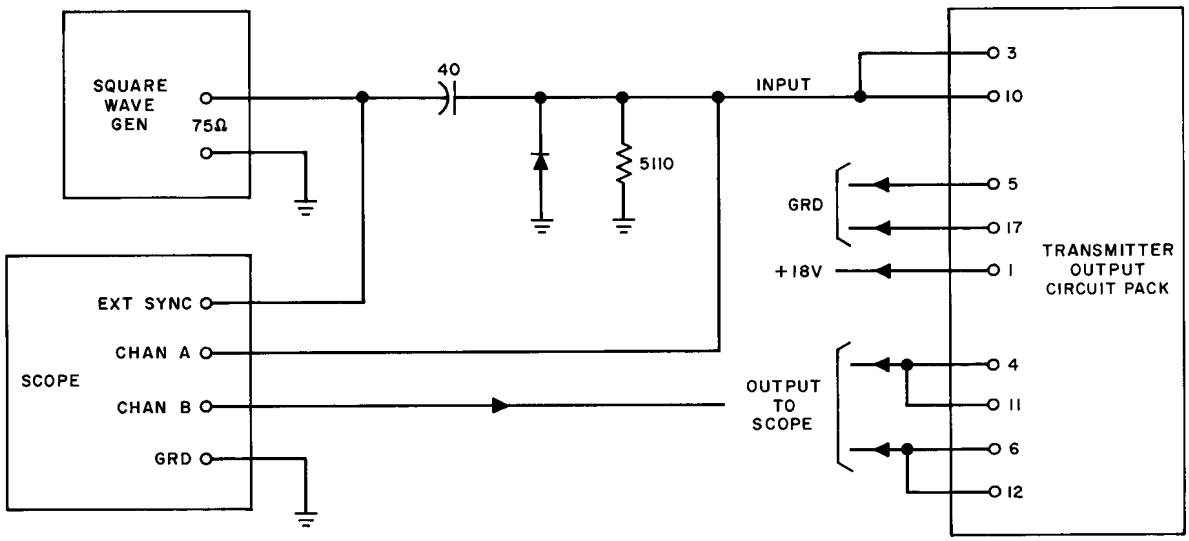


Fig. 36A — Transmitter Output Test Circuit

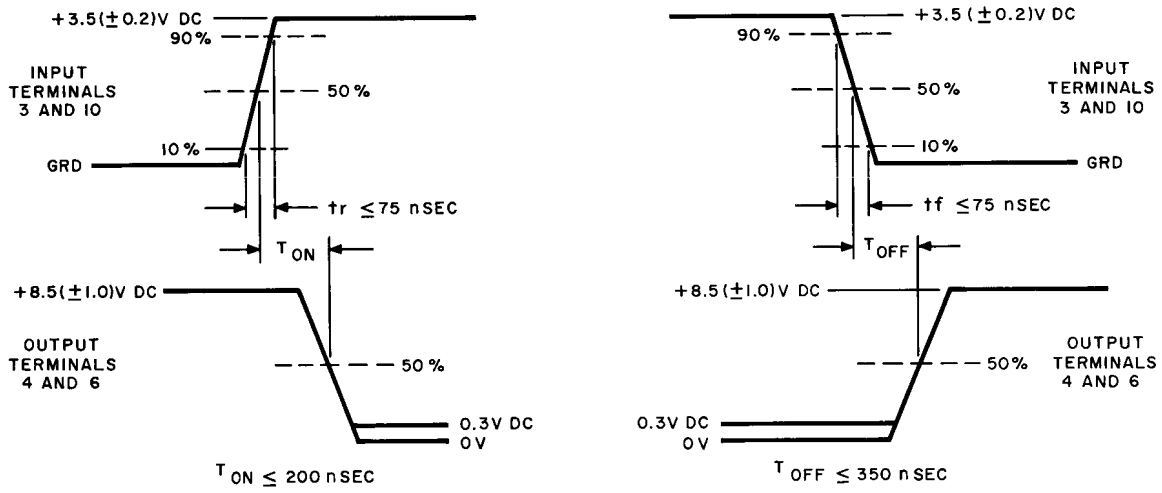


Fig. 37A — Transmitter Output Test

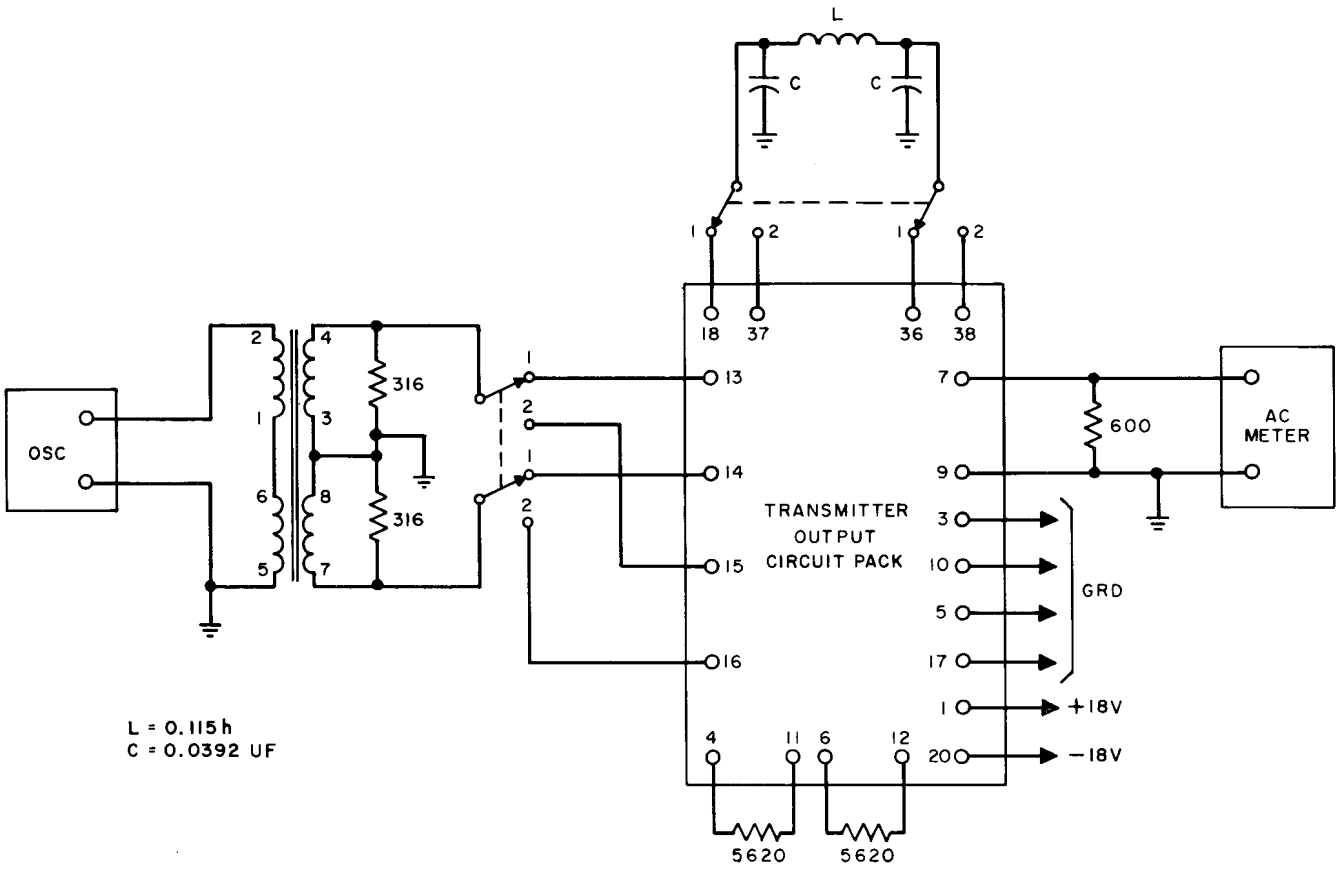


Fig. 38A — Transmitter Output Test Circuit

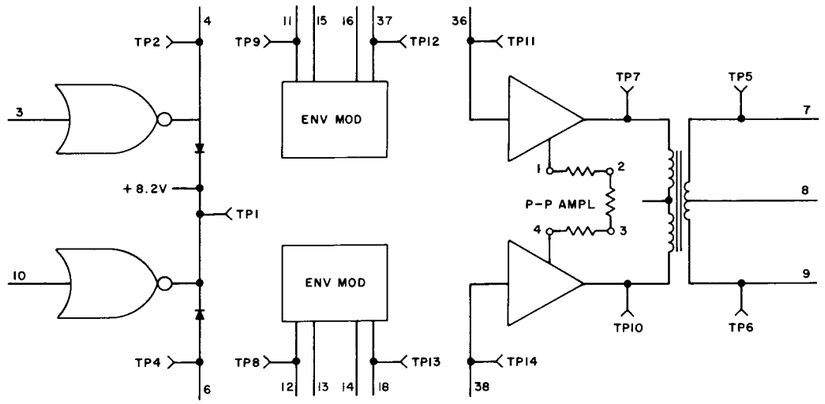


TABLE A

OUTPUT LEVEL	CONNECT TERMINALS
0 DBM	1 AND 4
-3 DBM	1 AND 3
-6 DBM	1 AND 2
-9 DBM	NONE

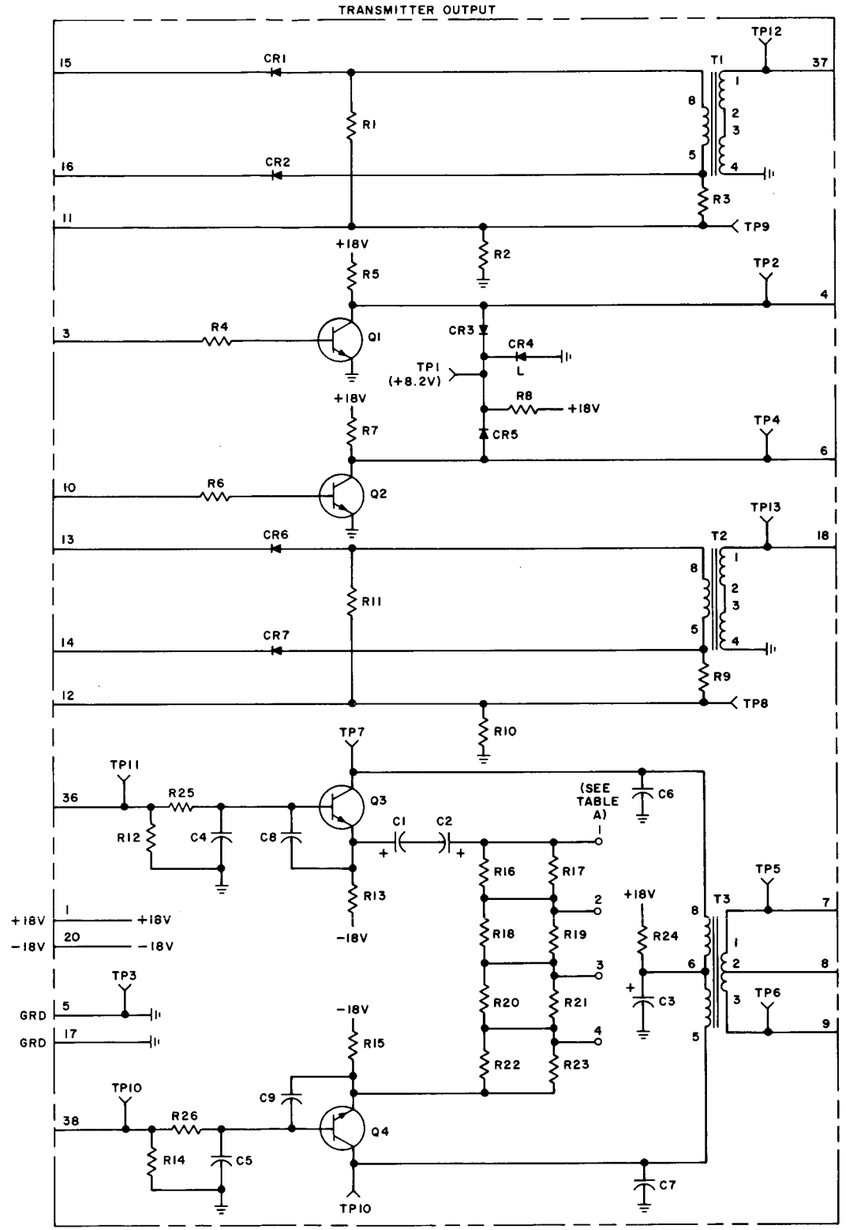


Fig. 39A — Transmitter Output, Circuit Pack Assembly AR90 (A835182), Circuit Sketch

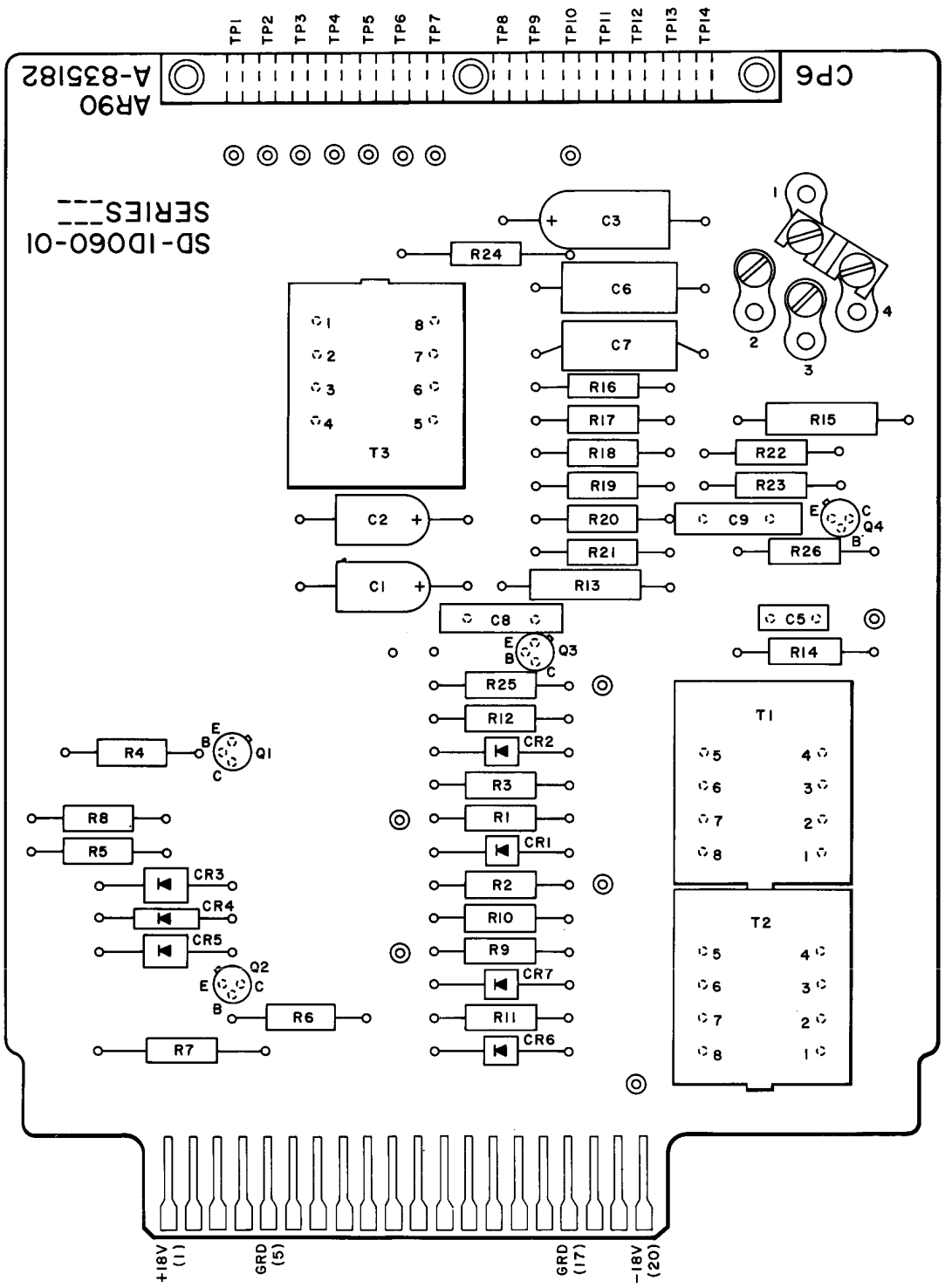


Fig. 40A — Transmitter Output, Circuit Pack Assembly AR90 (A835182), Component Location

7A. MONOPULSER CIRCUIT PACK ASSEMBLY AR91 (A835177)

7.01A *Circuit Description:* The AR91 circuit pack contains six similar monopulser circuits. Because of the similarity, only the "point zero" circuit will be described. The following description is illustrated by a circuit sketch that follows the test procedures. During quiescent conditions when less than +0.5 Vdc (a logical "0") is applied to input terminals 2 and 7, Q1.0 is cut off and Q2.0 is saturated. The collector of Q1.0 is connected to output terminal 6 and is clamped to +6.2 Vdc (a logical "1") by CR2.0. The collector of Q2.0 is connected to output terminal 4 and the voltage is less than +0.5 Vdc.

7.02A If either input terminal receives a +6.2 Vdc signal, Q1.0 will conduct into saturation and drop the voltage on output terminal 6 to less than +0.5 Vdc. At the same time that Q1.0 conducts, the charge stored on C1.0 places a negative voltage at the base of Q2.0 and the stage is cut off. Transistor Q2.0 remains cut off until the time constant of C1.0 and R4.0 allows the base voltage to become positive and Q2.0 to conduct into saturation.

7.03A For each +6.2 Vdc signal applied at either input terminal 2 or 7, a +6.2 Vdc signal appears at output terminal 4 for approximately 10 microseconds. A +0.5 Vdc signal is generated at output terminal 6 whenever the voltage at terminals 2 or 7 is greater than +6.2 Vdc. The circuit may not be retriggered until both inputs are less than +0.5 Vdc and sufficient time has elapsed for C1 to recharge to its quiescent value.

Monopulser Circuit Pack Test

A. Test Equipment

1 — Monopulser test set such as shown in Fig. 6A

1 — Oscilloscope, Tektronix 533 with type CA plug-in unit (or equivalent)

2 — Probes, P6006 (10X) (or equivalent)

1 — DC voltmeter, 20,000 ohm/volt, ±3 percent

1 — DC milliammeter, ±5 percent.

B. Power Requirements

+18.0 (±0.5) Vdc — 200 mA

+6.0 (±0.3) Vdc — 20 mA

C. Preliminary Procedure

(1) Set up the test circuit as shown in Fig. 41A. The scope EXT SYNC TRIGGER selector should be set to the (+) positive position.

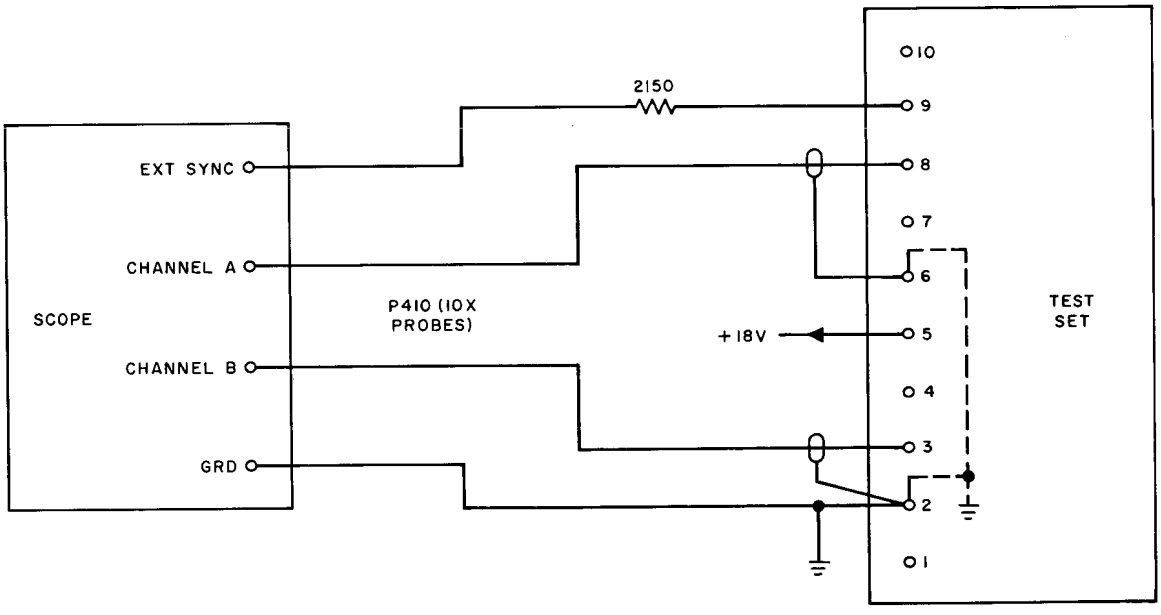


Fig. 41A — Monopulser Test Circuit

(2) Make the following settings on the test set:

(a) INPUT selector to position 1

(b) TEST FUNCTION selector to position 2

(c) FLIP-FLOP-MONOPULSER selector to MONOPULSER.

D. Test Procedures

7.04A ***Diode Short Test:***

(1) This test is to be made before the circuit pack is inserted into the test set.

(2) Ground pin 1 and apply +6.0 (±0.3) Vdc to test point 8 of the circuit pack to be tested.

(3) The total current drawn shall be less than 3.0 mA dc.

7.05A ***Zener Voltage Test:***

(1) Insert the circuit pack to be tested into the test set monopulser test connector.

(2) The voltage between test point 8 and ground when measured with the voltmeter should be +6.2 (±0.6) Vdc.

7.06A ***Pulse Test — Normal Input:***

(1) Consult Table D to determine which monopulser and corresponding input resistor are under test.

(2) Set the NORMAL-DEGRADED selector to NORMAL.

(3) Adjust potentiometer P1 until the voltage between J1 and ground measures +6.0 (±0.2) Vdc with the voltmeter.

(4) The input test pulse on J8 should be as specified in Fig. 42A.

(5) Rotate the INPUT selector through positions 1 to 6. The output pulse on J3 should be as specified in Fig. 42A at each position.

(6) With the TEST FUNCTION selector in position 2, repeat as in (5).

7.07A ***Pulse Test — Degraded:***

(1) Set the NORMAL-DEGRADED selector to DEGRADED.

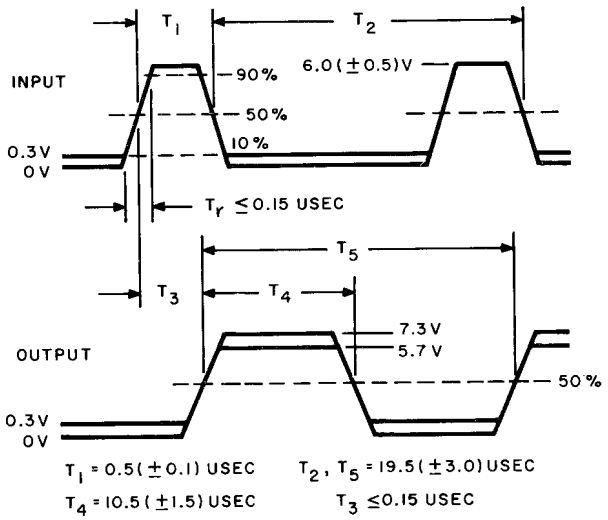


Fig. 42A — Monopulser Test

(2) Adjust potentiometer P1 until the amplitude of the input test pulse on J8 is 3.0 (±0.2) volts on the oscilloscope. The input test pulse should appear as in Fig. 43A.

(3) Rotate the INPUT selector through positions 1 to 6. The output pulse on J3 should appear as in Fig. 43A. Time base measurements need not be made on the output waveform.

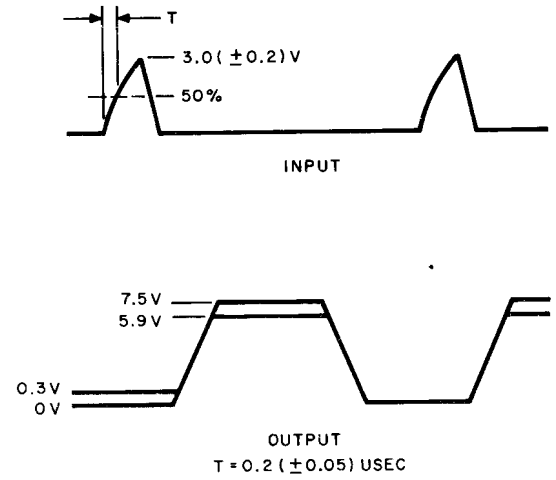
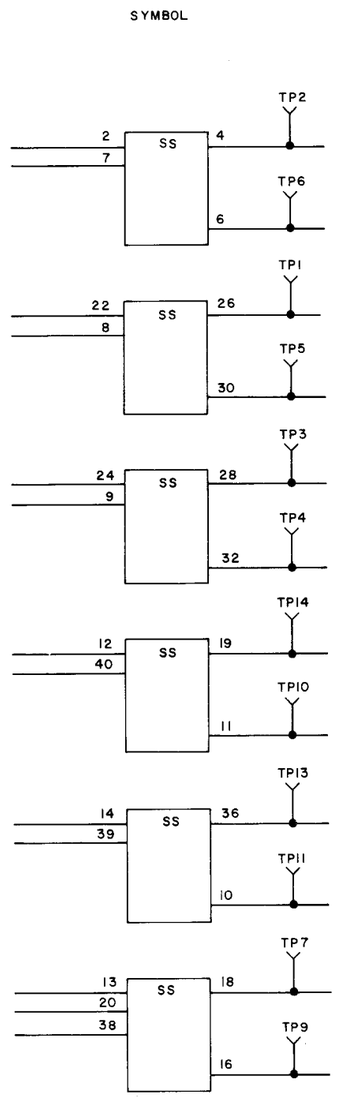


Fig. 43A — Monopulser Test

TABLE D

KEY TO COMPONENTS UNDER TEST AT EACH POSITION OF TEST SET SWITCHES

TEST FUNCTION POSITION	INPUT SELECTOR POSITION	INPUT TERMINAL	INPUT RESISTOR	TRANSISTOR	OUTPUT TERMINAL
1	1	2	R1	Q1, Q2	6, 4
	2	22	R7	Q3, Q4	30, 36
	3	24	R13	Q5, Q6	32, 23
	4	13	R19	Q7, Q8	16, 18
	5	12	R25	Q9, Q10	11, 19
	6	14	R31	Q11, Q12	10, 36
2	1	7	R2	Q1, Q2	6, 4
	2	8	R8	Q3, Q4	30, 36
	3	9	R14	Q5, Q6	32, 28
	4	20	R20	Q7, Q8	16, 18
	5	40	R26	Q9, Q10	11, 19
	6	39	R32	Q11, Q12	10, 36



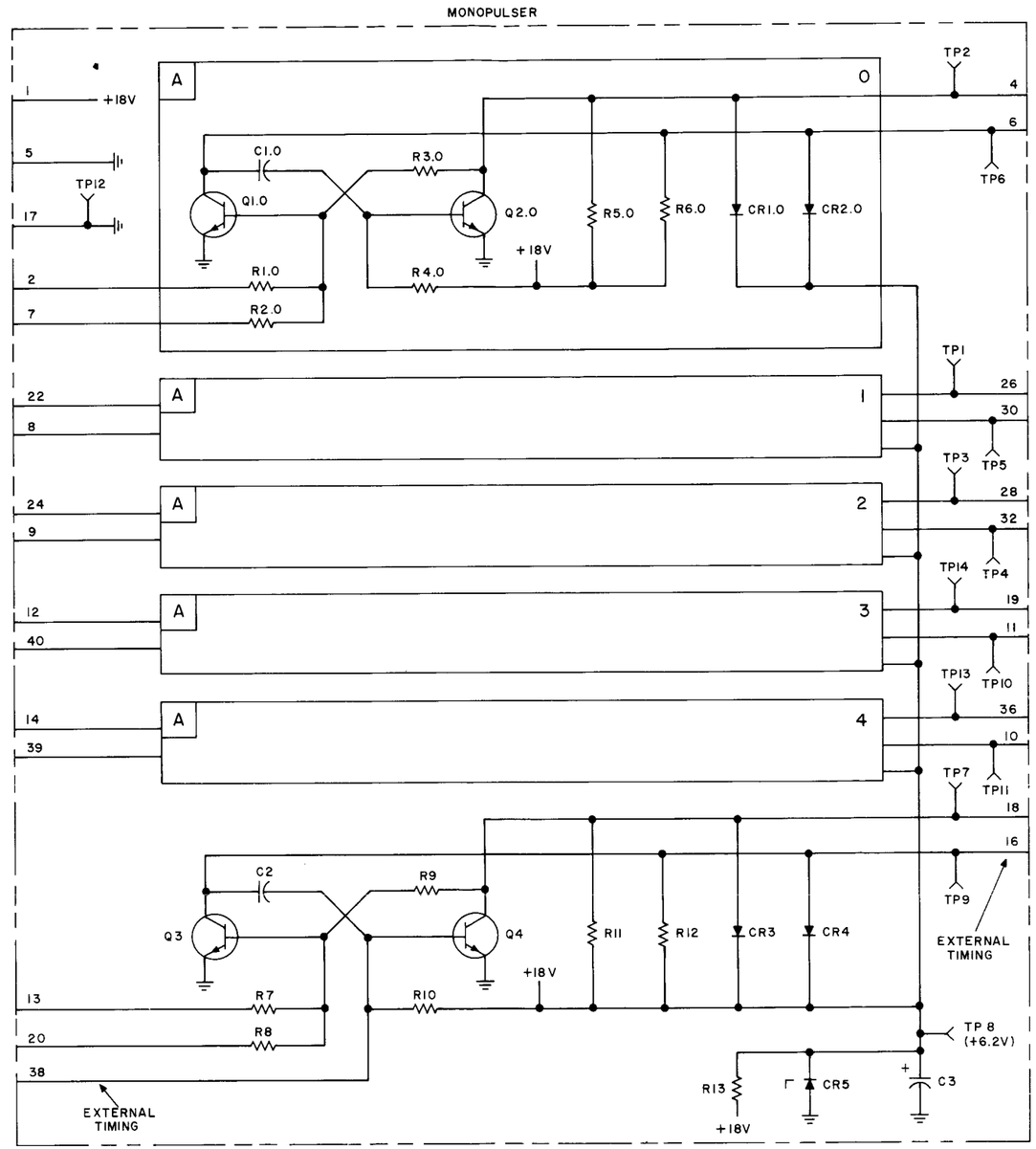


Fig. 44A — Monopulser, Circuit Pack Assembly AR91 (A835177), Circuit Sketch

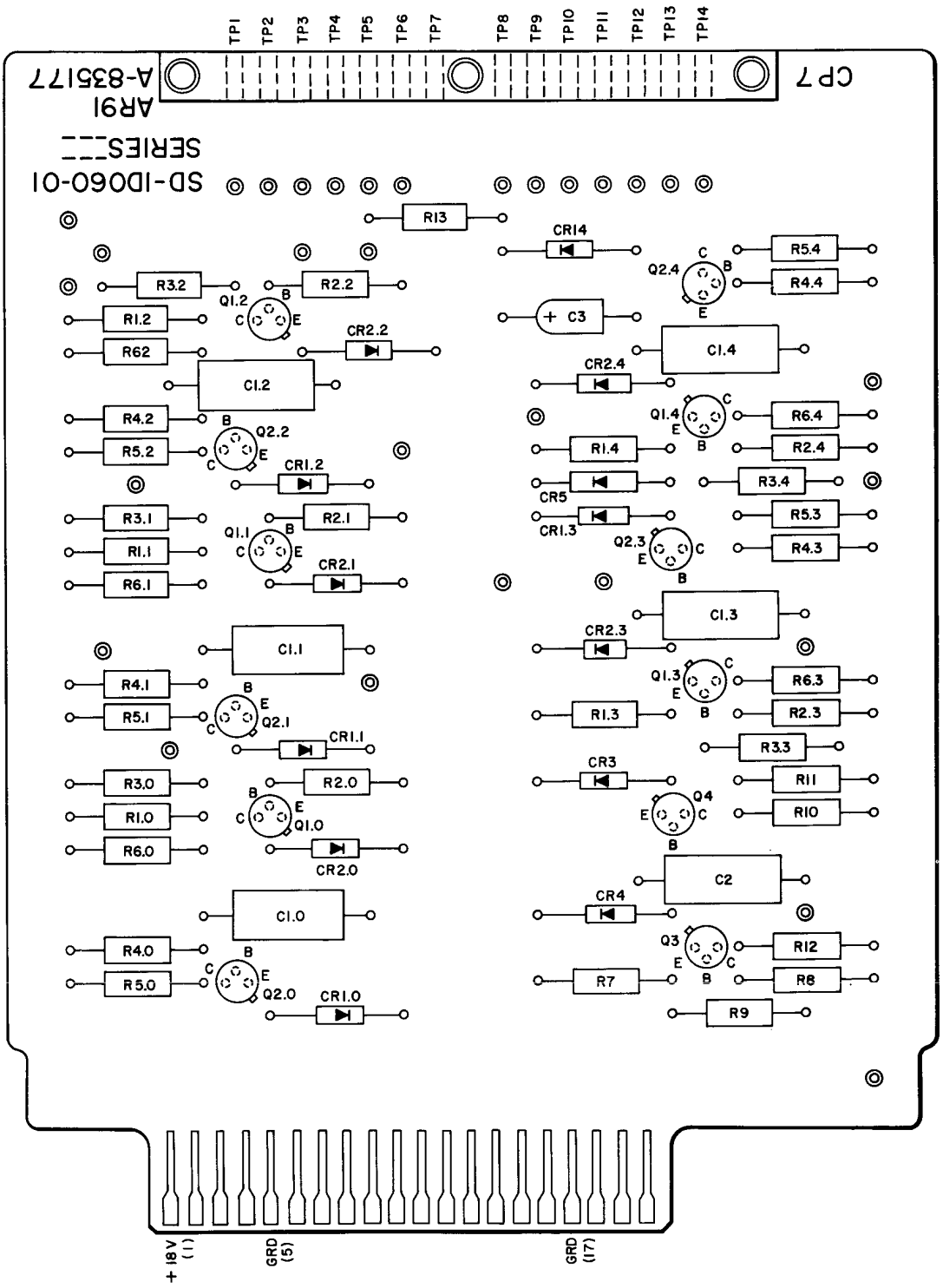


Fig. 45A — Monopulser, Circuit Pack Assembly AR91 (A835177), Component Location

8A. EIA INTERFACE CIRCUIT PACK ASSEMBLY AR92 (A835185)

8.01A ***Circuit Description:*** The AR92 circuit pack contains five driving interface circuits and five terminating interface circuits. One terminating circuit has a high input impedance. The following descriptions are illustrated by a circuit sketch that follows the test procedures.

8.02A The driver interface circuits are identical and only the "point zero" circuit will be described. When the applied signal on input terminal 38 is approximately +6.2 Vdc (a logical "1"), CR1.0 is reverse-biased and Q1.0 conducts to saturation through R1.0, CR2.0, and CR3.0. During this time, the output terminal 13 will be held to approximately −6.8 Vdc. If the applied input signal is less than +0.5 Vdc, CR1.0 conducts and reverse-biases CR2.0 into the high impedance region of operation. When CR2.0 is a high impedance, Q1.0 cuts off and the output terminal is clamped to approximately +6.8 Vdc through CR4.0.

8.03A Four of the five terminators are identical and operation of only the "point five" circuit is described. If the input signal on terminal 23 is greater than +3.0 volts, Q2.5 conducts and the output terminal 4 is held to less than +0.5 Vdc. If the input signal is more negative than −3.0 Vdc, Q2.5 is cut off and the output terminal is clamped to +6.8 Vdc through CR6.5.

8.04A The high-impedance terminator has a similar operation as previously described for other terminators. The major difference is that Q3 is an emitter-follower that drives Q4. An input signal on terminal 27 greater than +3.0 Vdc causes output terminal to be less than +0.5 Vdc and an input more negative than −3.0 Vdc clamps the output terminal to approximately +6.8 Vdc.

EIA Interface Test

A. Test Equipment

1 — Oscilloscope, Tektronix 533 with type CA plug-in unit (or equivalent)

2 — Probes, Tektronix P6006 (10X) (or equivalent)

1 — DC meter, 0 to 20 volts, 20,000 ohm/volt, ±3 percent)

1 — DC meter, 0 to 10 mA, ±3 percent

4 — Resistors:

1 — 75 ohms (±1 percent), 1 watt, WECo 144E (or equivalent)

1 — 147 ohms (±1 percent), 2 watts, WECo 147D (or equivalent)

1 — 600 ohms (±1 percent), 1/2 watt, WECo 145A (or equivalent)

1 — 2150 ohms (±1 percent), 1/2 watt, WECo 145A (or equivalent)

1 — Mercury relay, WECo 291A (or equivalent)

1 — Square-wave generator, Hewlett-Packard model 211A (or equivalent)

1 — 2-section, 10-position rotary wafer switch.

B. Power Requirements

+18.0 (±0.5) Vdc — 200 mA

−18.0 (±0.5) Vdc — 100 mA

+6.0 (±3) Vdc — 10 mA

C. Test Procedures

8.05A ***+6.8 Vdc Regulator Diode Test:*** Connect ground to terminals 5 and 17 and apply +18 (±0.5) Vdc to terminal 1. The voltage between test point 8 and ground should be +6.8 (±0.9) Vdc.

8.06A ***−6.8 Vdc Regulator Diode Test:*** With terminals 5 and 17 connected to ground, apply −18.0 (±0.5) Vdc to terminal 20. The voltage between test point 12 and ground shall be −6.8 (±0.9) Vdc.

8.07A ***Output Clipping Diode Short Test:*** With the circuit pack connected to the suggested test circuit shown in Fig. 46A, connect +6.0 (±0.3) Vdc to test point 8 on the circuit pack. Measure the current drawn at each output terminal by rotating the switch through positions 1 to 10. At each position of the switch, the current drawn should be less than 1.5 mA dc.

8.08A ***Input Regulator Diode Test:*** With the circuit pack connected to the suggested test circuit shown in Fig. 47A, connect ground to terminals 5 and 17, +18.0 (±0.5) Vdc to terminal 1, and −18 (±0.5) Vdc to terminal 20. Measure the voltage between the input and test point 12 of each of the five driver inverters by rotating the switch through positions 1 to 5. This voltage should be +9.3 (±1.0) Vdc.

8.09A ***Pulse Tests:*** With the circuit pack connected to the suggested test circuit shown in Fig. 48A, connect ground to terminals 5 and 17, +18.0 (±0.5) Vdc to terminal 1, and −18.0 (±0.5) Vdc to terminal 20. Temporarily short terminal 1 to terminal 3 of the mercury relay. The voltage between point A and ground should measure +6.0 (±0.3) Vdc with the voltmeter. Remove the short on the mercury relay and set the frequency of the square-wave generator between 40 and 50 Hz. Set the EXT SYNC TRIGGER selector to (+) positive.

8.10A ***Turn-On Time:***

(1) Rotate the switch through positions 1 to 5. The input-output waveforms shall be as specified in Fig. 49A.

(2) Rotate the switch through positions 6 to 9. The input-output waveforms shall be as specified in Fig. 50A.

(3) Rotate the switch to position 10. The input-output waveforms shall be as specified in Fig. 51A.

8.11A ***Turn-Off Time:***

(1) Set the EXT SYNC TRIGGER to (−) negative.

(2) Repeat 8.10A (1), (2), and (3). Input-output waveforms shall be as specified in Fig. 52A, 53A, and 54A, respectively.

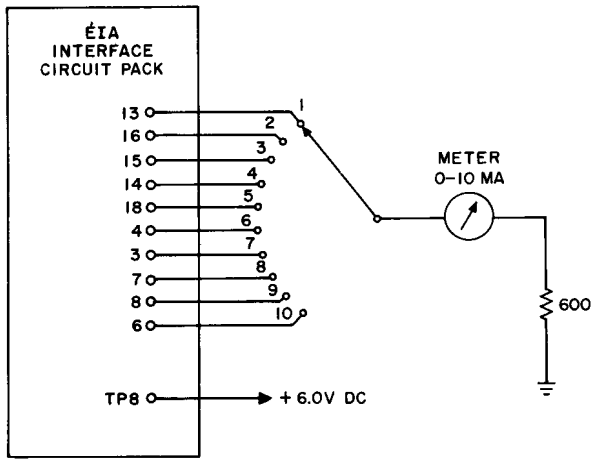


Fig. 46A — EIA Interface Test Circuit

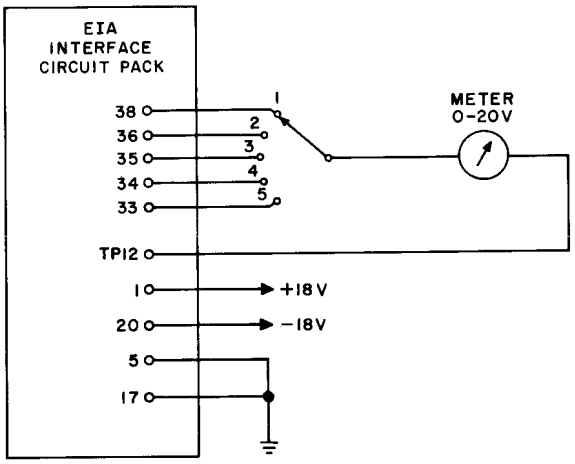


Fig. 47A — EIA Interface Test Circuit

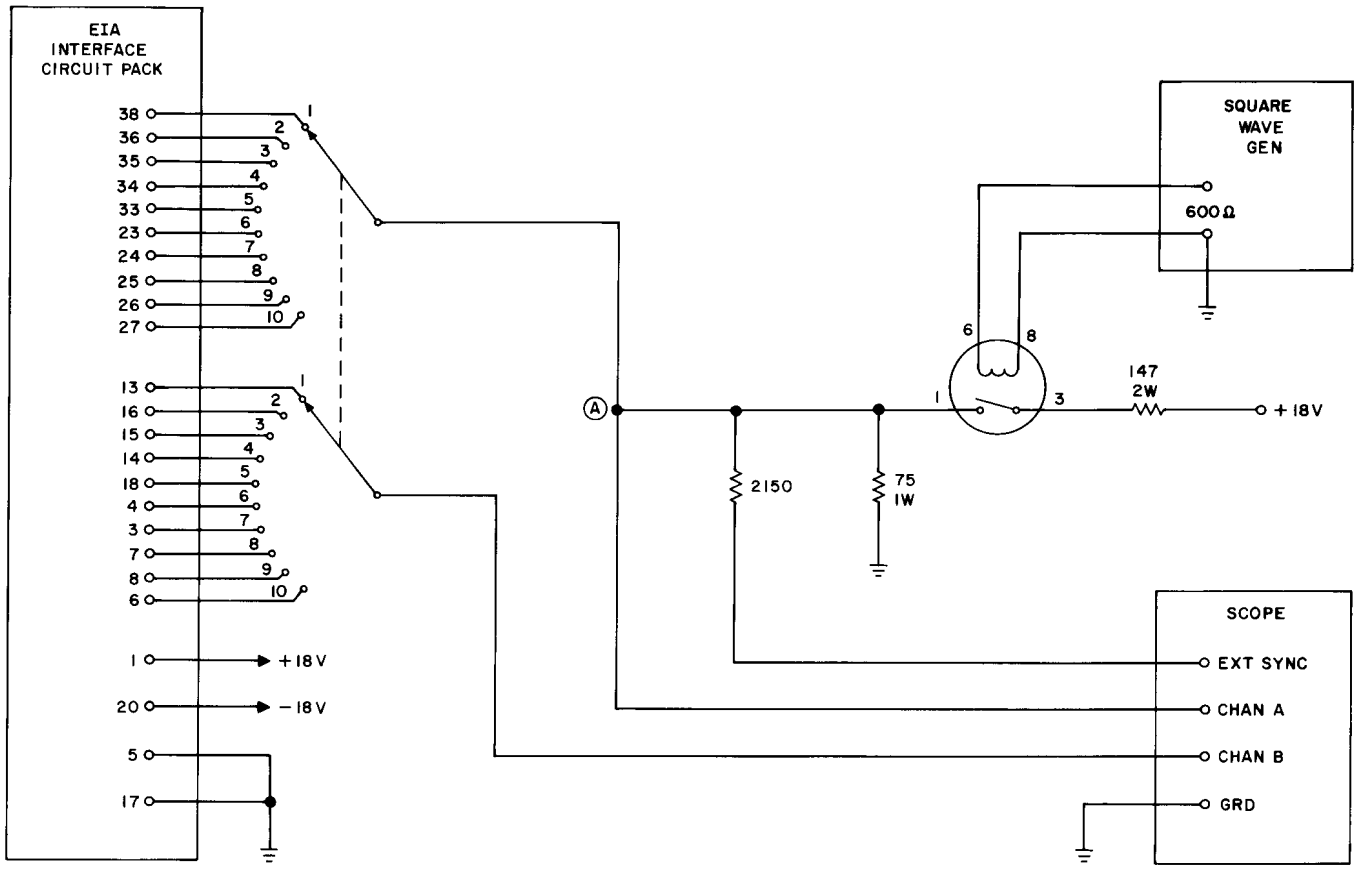


Fig. 48A — EIA Interface Test Circuit

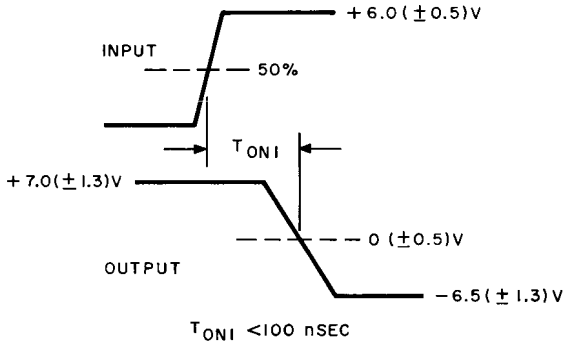


Fig. 49A — EIA Interface Test

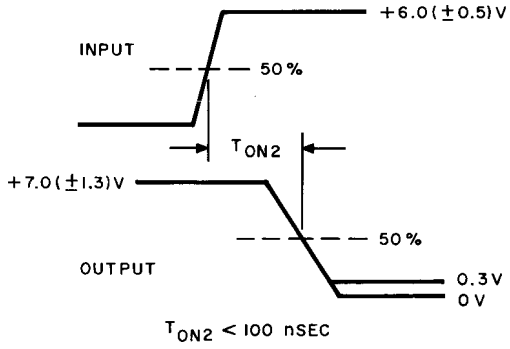


Fig. 50A — EIA Interface Test

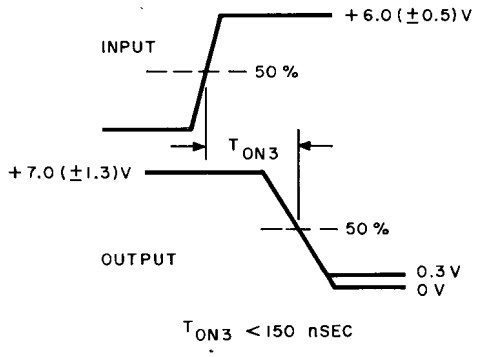


Fig. 51A — EIA Interface Test

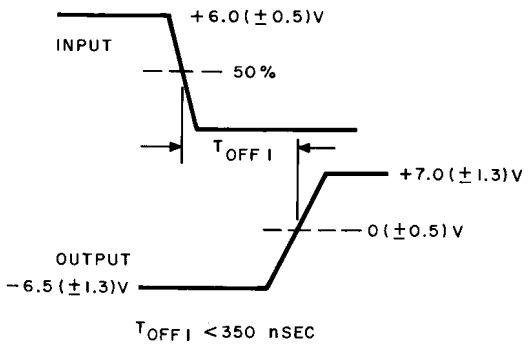


Fig. 53A — EIA Interface Test

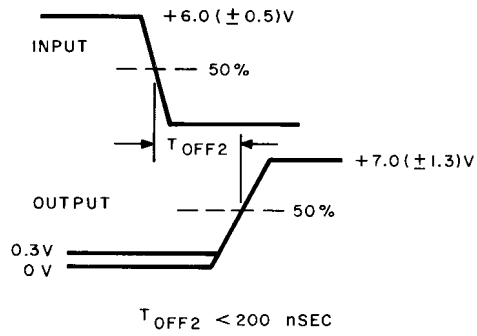


Fig. 52A — EIA Interface Test

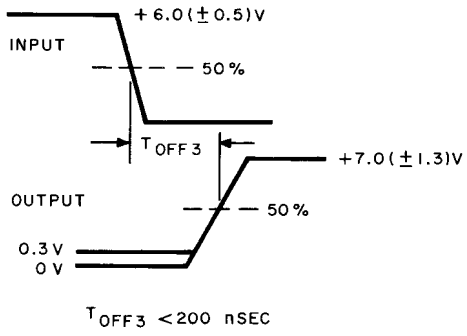
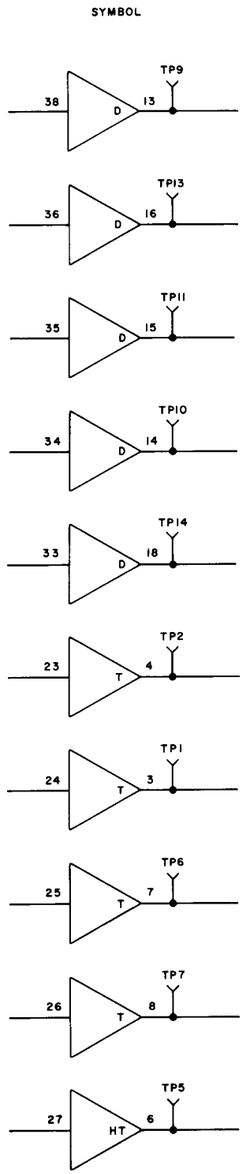


Fig. 54A — EIA Interface Test



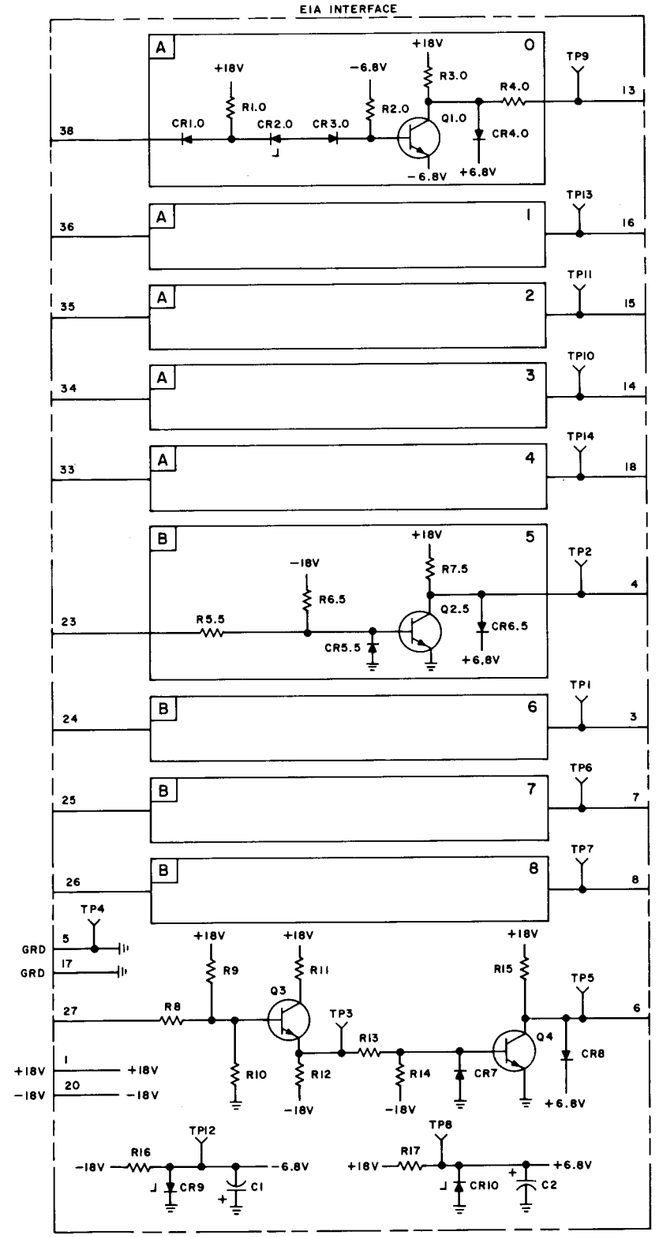


Fig. 55A — EIA Interface, Circuit Pack Assembly AR92 (A835185), Circuit Sketch

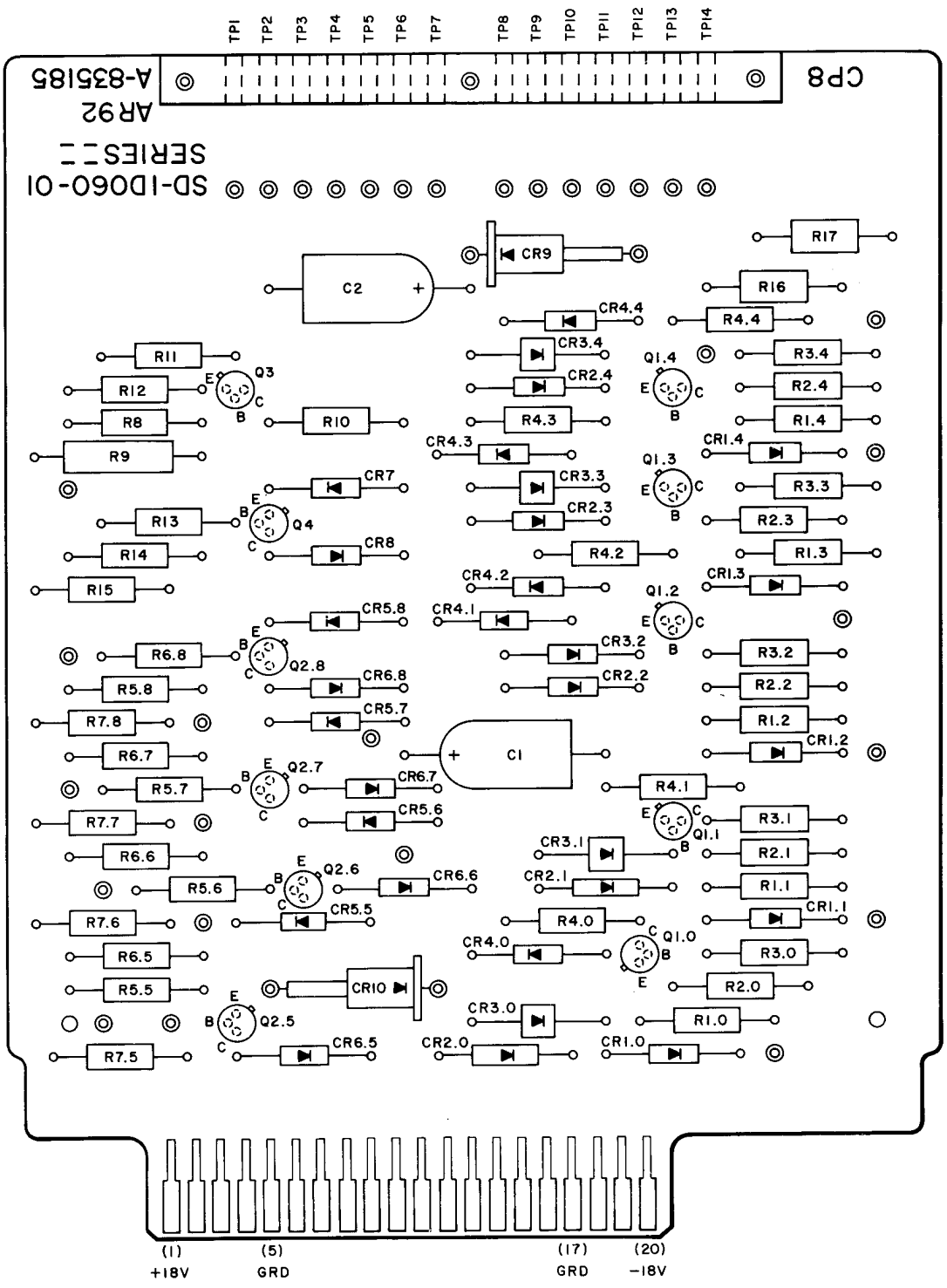


Fig. 56A — EIA Interface, Circuit Pack Assembly AR92 (A835185), Component Location

9A. REMOTE TEST CIRCUIT PACK ASSEMBLY AR93 (A835184)

9.01A *Circuit Description:* The AR93 circuit pack contains a gated pulse-forming circuit and a driver to control relay K1. The circuit pack also contains miscellaneous components and terminal straps. The following descriptions are illustrated by a circuit sketch that follows the test procedures.

9.02A Received ac signals are applied through terminal 11 to a peak-to-peak detector circuit. Each positive half-cycle of the applied ac input signal is passed by R2, C1, CR2, and peak detected by CR3 and C3. A positive dc voltage stored by C3 is applied through R8 to the base of Q2. Components R3 and C2 make a differentiating circuit for applying either positive or negative pulses to the base of Q2. With no input signals on terminal 11, Q2 will be normally cut off and the collector (and output terminal 13) clamped to +6.2 Vdc (a logical "1") through CR8. Only positive signal transitions on terminal 7 will permit Q2 to conduct for approximately 30 microseconds to supply a negative pulse of the same time duration on terminal 12. When the 12 Vac (peak-to-peak) signal is applied to terminal 11, Q2 is normally conducting and the output terminal is held to less than +0.5 Vdc. With this condition, only negative transitions on terminal 7 will cause Q2 to cut off for 15 microseconds which provides a positive pulse on terminal 12 for the same time duration.

9.03A Transistor Q1 operates as a control switch for relay K1. A positive voltage on input terminal 14 allows Q1 to conduct and operate the relay. A negative voltage on terminal 14 causes Q1 to cut off and the relay is released.

9.04A Power supply voltages can be measured between TP10 (+18 Vdc) and TP4 (ground), or between TP11 (−18 Vdc) and TP4. Resistors R17 and R18, in series with the test points, are current limiters.

9.05A The customer is provided access to the −18 Vdc and +18 Vdc power supplies through R5, R11, and terminals 19 and 4, respectively.

9.06A Components R15, R16, and test points TP7 and TP8 provide a test circuit for relay K1. When TP8 is connected to TP13 and TP7 is connected to TP4, relay K1 should operate. Relay K1 should release when the TP7 to TP4 connection is removed.

Remote Test Circuit Test

A. Test Equipment

1 — Oscilloscope, Tektronix 533 with type CA plug-in unit (or equivalent)

2 — Probes, Tektronix P6006 (10X) (or equivalent)

2 — Square-wave generators, Hewlett-Packard model 211A (or equivalent)

1 — DC voltmeter, 20,000 ohm/volt, ±3 percent

1 — Ohmmeter, ±5 percent

1 — Capacitor, 40 uf (±20 percent), WECo 602A (or equivalent)

5 — Resistors:

- 1 — 5110 ohms (±1 percent), 1/2 watt, WECo 221A (or equivalent)
- 1 — 2150 ohms (±1 percent), 1/2 watt, WECo 145A (or equivalent)
- 1 — 19.6k ohms (±1 percent), 1/2 watt, WECo 221A (or equivalent)
- 1 — 215 ohms (±1 percent), 1/2 watt, WECo 145A (or equivalent)
- 1 — 1.78 meg (±1 percent), 1/2 watt, WECo 221A (or equivalent)

1 — Switching diode, KS-16986-L2 (or equivalent).

B. Power Requirements

+18.0 (±0.5) Vdc — 50 mA

−18.0 (±0.5) Vdc — 5 mA

C. Test Procedures

9.07A *Resistance Test:*

(1) The resistance between terminals 6 and 8 shall be 3160 ohms (±5 percent).

(2) The resistance between terminals 1 and 2, terminal 1 and test point 10, and between terminal 20 and test point 11 shall be 1960 ohms (±5 percent).

(3) The resistance between terminals 19 and 20 shall be 681 ohms (±5 percent).

(4) The resistance between terminals 1 and 4 shall be 681 ohms (±5 percent).

(5) The resistance between terminals 1 and 3 shall be 11,000 ohms (±5 percent).

9.08A ***Diode Leakage Test:***

(1) Connect terminals 5 and 17 to ground. Connect +18.0 (±0.5) Vdc in series with a 1.78 meg (±1 percent) resistor to terminal 6. The current drawn from the +18.0 Vdc supply shall be less than 7.0 uA.

(2) Repeat (1) for terminal 7.

9.09A ***Strap Test:*** Using the ohmmeter, the resistance measured between the following terminals shall be less than 1 ohm.

FROM	TO
Terminal 22	Terminal 23
Terminal 24	Terminal 25
Terminal 26	Terminal 27
Terminal 28	Terminal 29
Terminal 30	Terminal 31
Terminal 32	Terminal 33
Terminal 34	Terminal 35
Terminal 36	Terminal 37
Terminal 38	Terminal 39

9.10A ***Zener Voltage Test:***

(1) With ground connected to terminals 5 and 17, apply +18.0 (±0.6) Vdc to terminal 1.

(2) The voltage between test point 2 and ground shall be +6.2 (±0.5) Vdc.

9.11A ***Pulse-Forming Network Dynamic Test:***

(1) With ground connected to terminals 5 and 17 and +18.0 (±0.5) Vdc connected to terminal 1, connect the circuit pack to the suggested test circuit shown in Fig. 57A. Set the frequency of the square-wave generator to 2.5 kHz (±10 percent).

(2) Set the scope EXT SYNC TRIGGER selector to the (+) positive position.

(3) The input waveform at terminal 7 shall be as specified in Fig. 58A.

(4) The output waveform at terminal 12 shall be as specified in Fig. 58A.

(5) Connect the circuit pack to the suggested test circuit shown in Fig. 59A.

(6) The input waveforms at terminals 7 and 11 shall be as specified in Fig. 60A. The relative phase of the input waveforms is immaterial.

(7) The voltage at test point 5, when measured with the voltmeter, should be +10.0 (±1.5) Vdc.

(8) Set the scope EXT SYNC TRIGGER selector to the (—) negative position.

(9) The output waveform shall be as specified in Fig. 60A.

9.12A ***Relay and Relay Driver Test:***

(1) Connect ground to terminals 5 and 17, +18.0 (±0.5) Vdc to terminal 1, and —18.0 (±0.5) Vdc to terminal 20.

(2) With test point 8 connected to test point 13, and test point 7 connected to ground, measure the resistance between terminal 15 and ground. The resistance shall be less than 1 ohm.

Caution: Do not use 1X range on ohmmeter.

(3) Remove the connection between test point 7 and ground. The ohmmeter should indicate an open circuit between terminal 15 and ground. Remove the connection between test point 13 and test point 8.

(4) Connect the circuit pack to the suggested test circuit shown in Fig. 61A. Set the frequency of the square-wave generator to 10 Hz (±10 percent).

(5) The input waveform at terminal 14 and the output waveform at terminal 15 shall be as specified in Fig. 62A. No time base measurements need to be made.

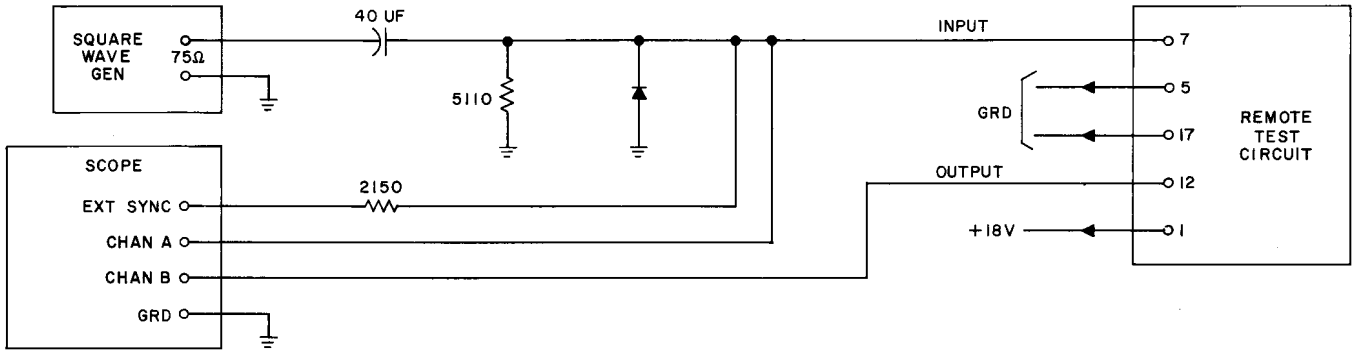


Fig. 57A — Remote Test Circuit Pack Test Circuit

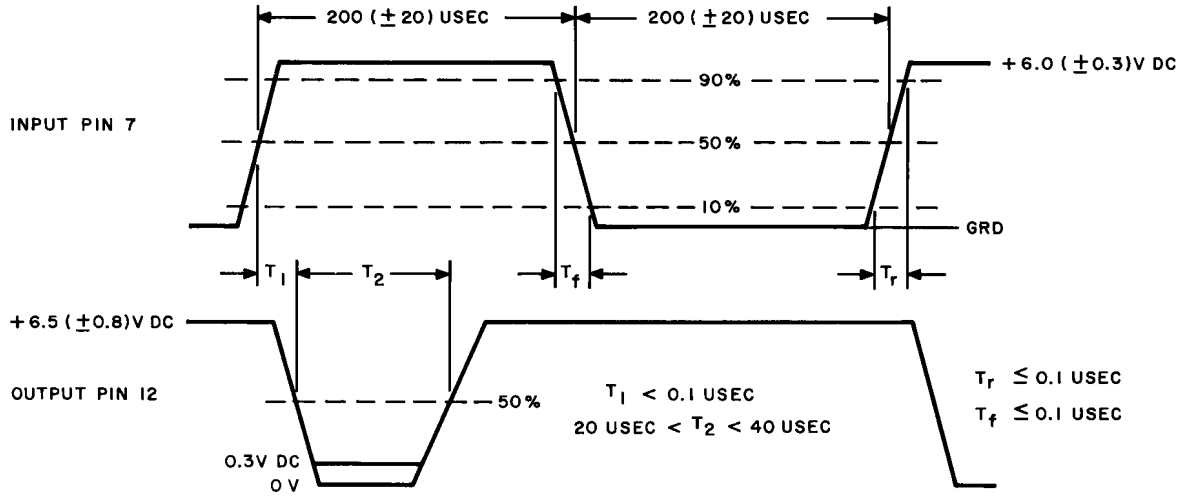


Fig. 58A — Remote Test Circuit Pack Test

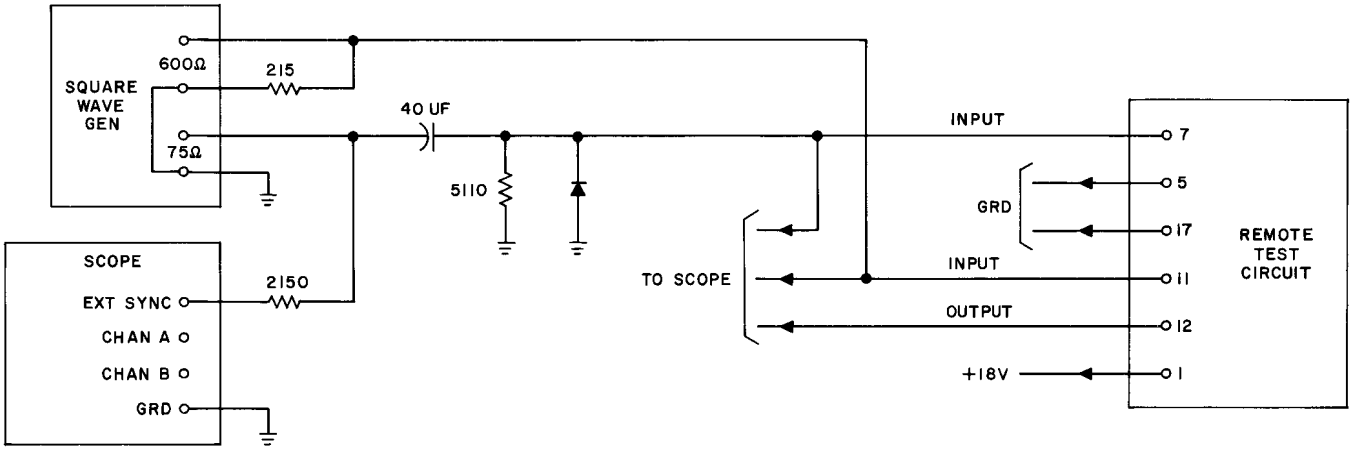


Fig. 59A — Remote Test Circuit Pack Test Circuit

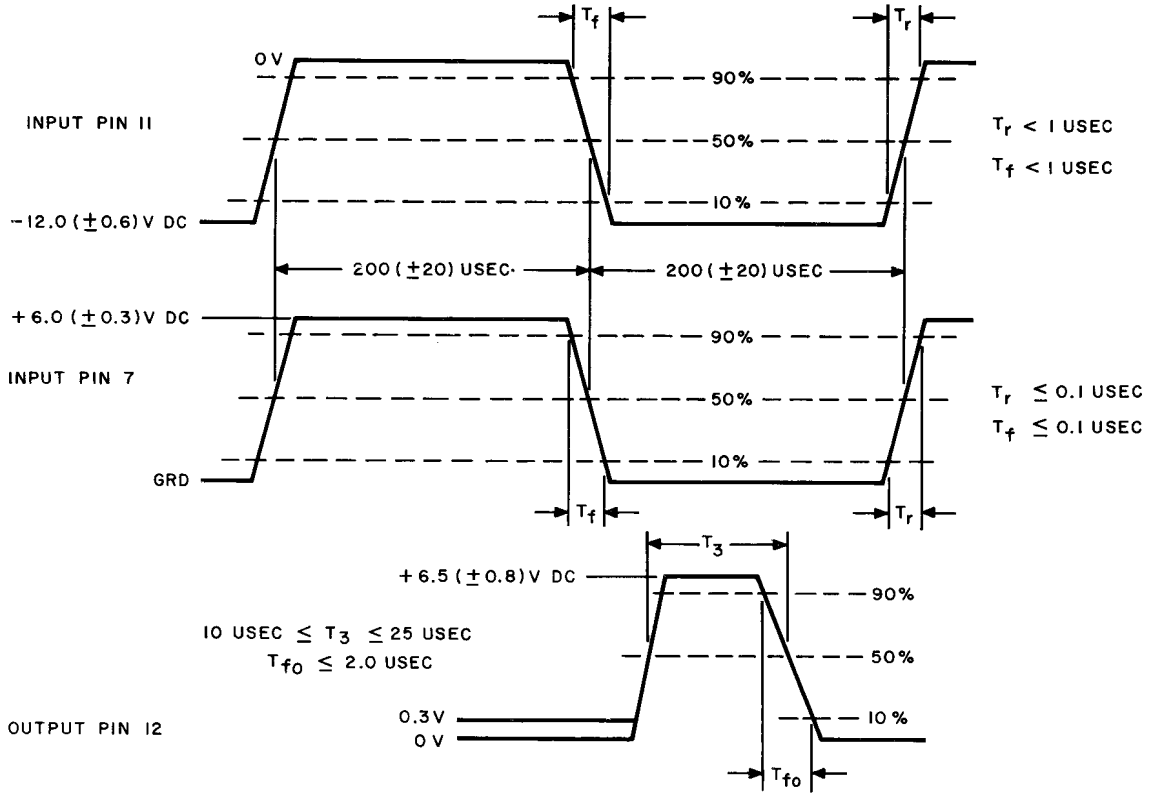


Fig. 60A — Remote Test Circuit Pack Test

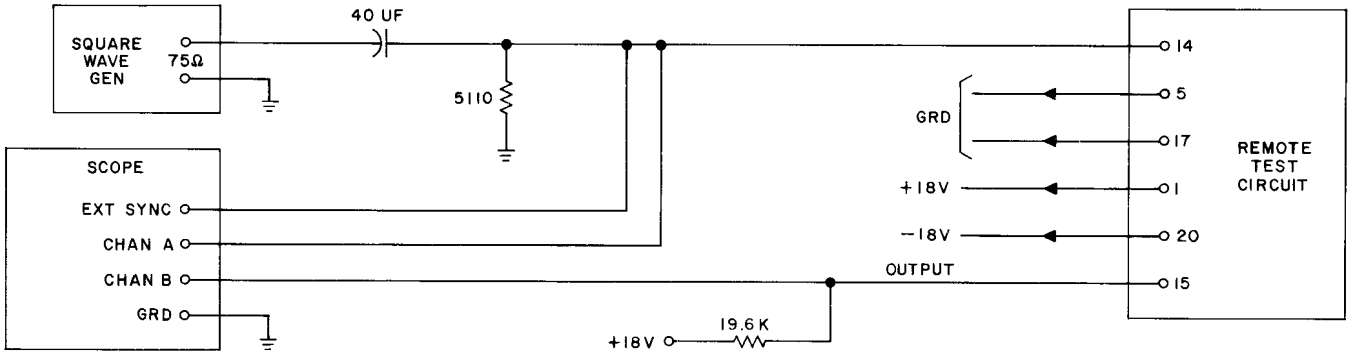


Fig. 61A — Remote Test Circuit Pack Test Circuit

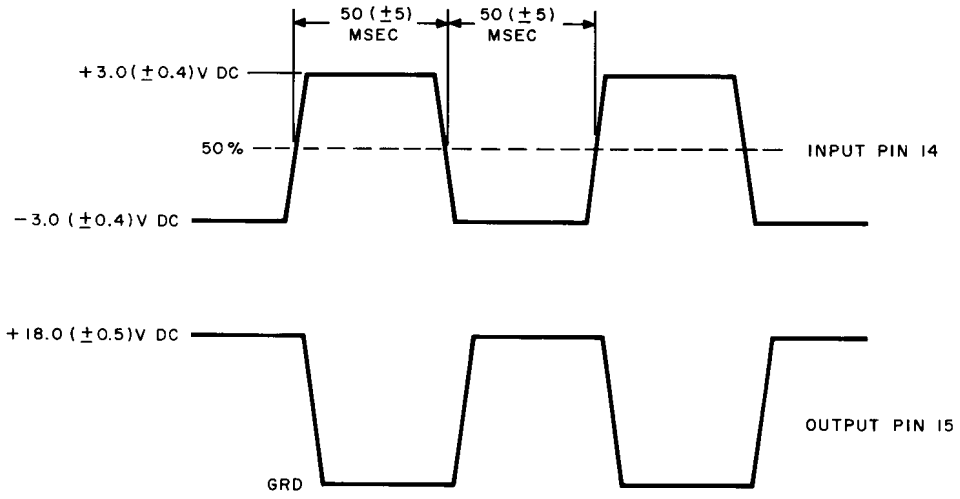
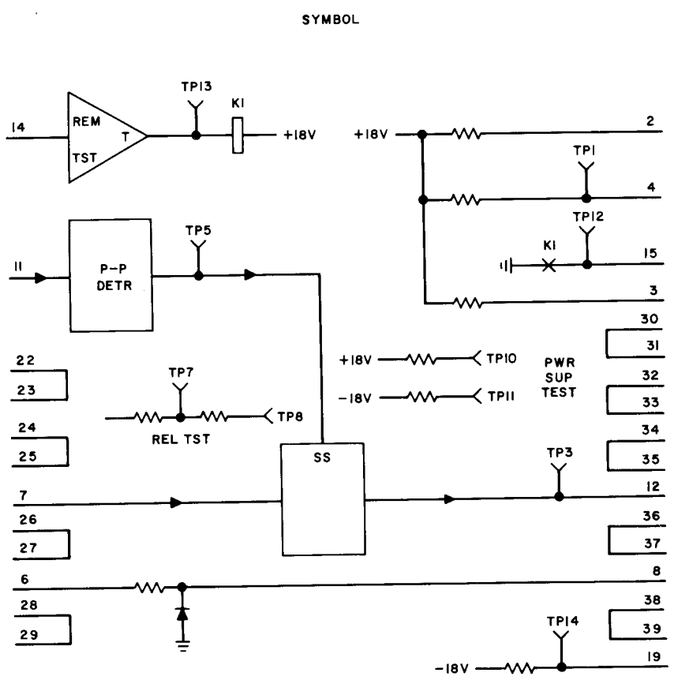


Fig. 62A — Remote Test Circuit Pack Test



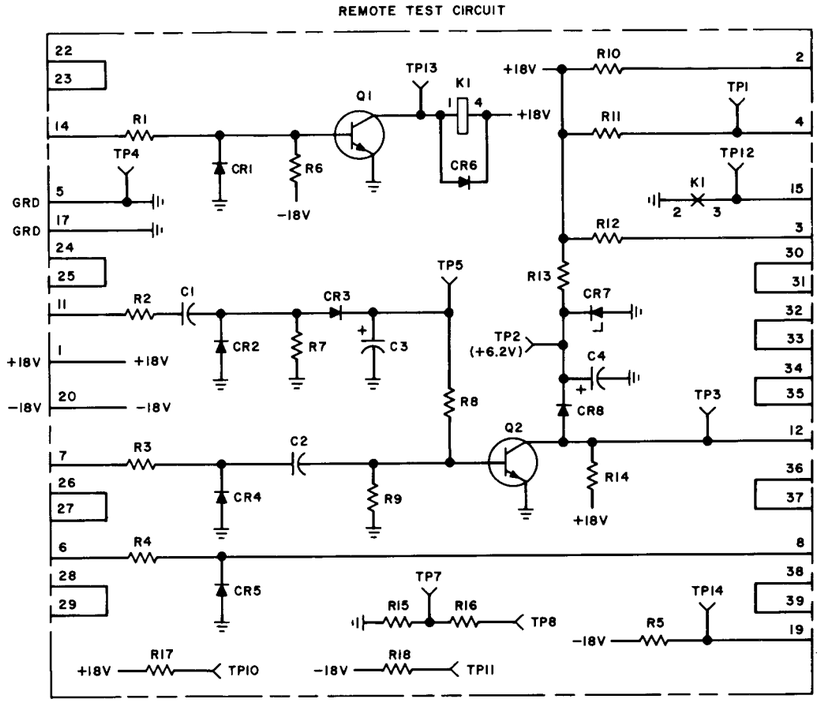


Fig. 63A — Remote Test, Circuit Pack Assembly AR93 (A835184), Circuit Sketch

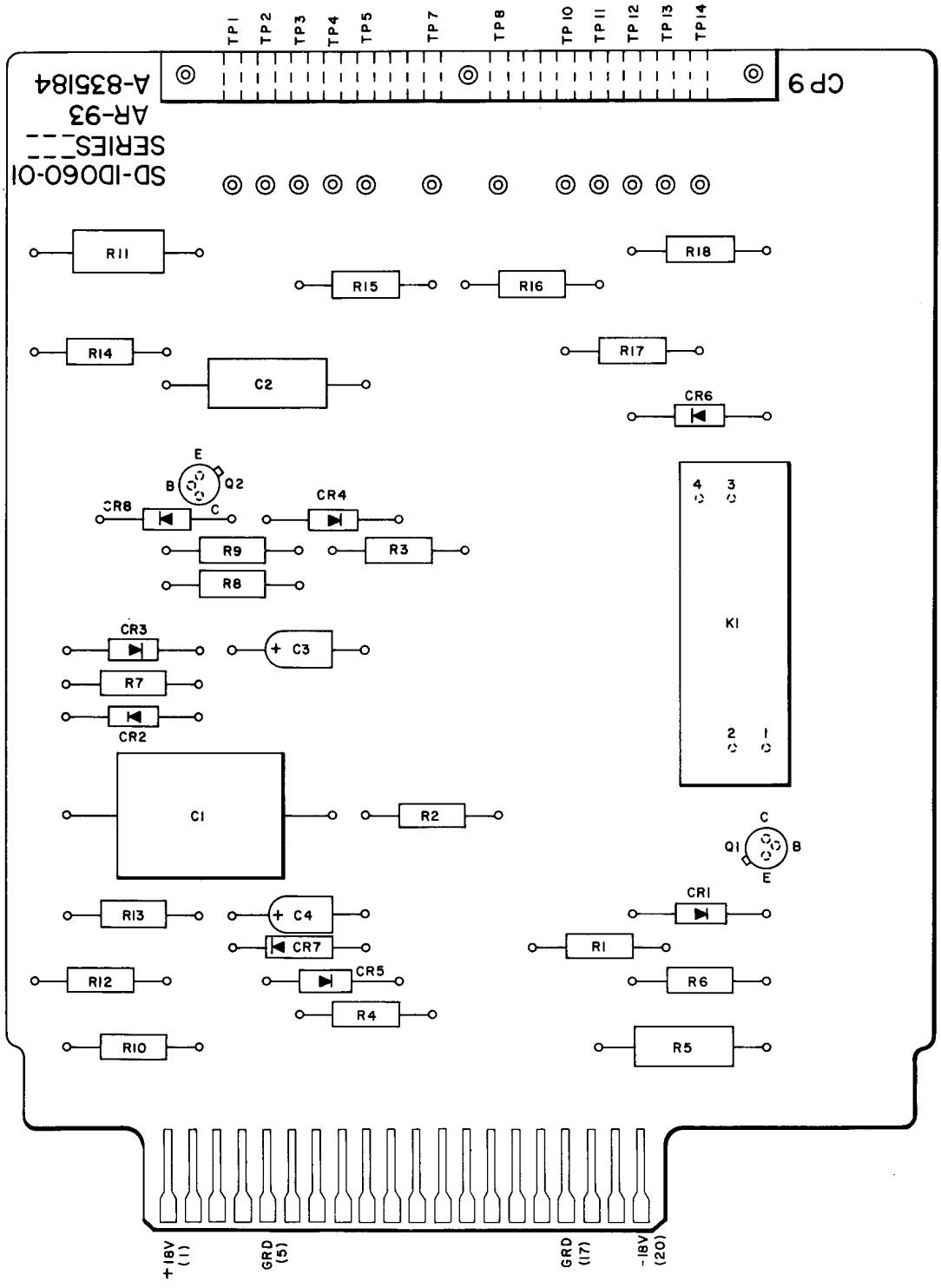


Fig. 64A — Remote Test, Circuit Pack Assembly AR93 (A835184), Component Location

10A. MILITARY STANDARD 188B INTERFACE CIRCUIT PACK ASSEMBLY AR94 (A835186)

10.01A *Circuit Description:* The AR94 circuit pack contains three identical interface driver circuits and one interface terminating circuit. The following descriptions are illustrated by a circuit sketch that follows the test procedures.

10.02A The driver circuits are identical and only the "point zero" components are described. When the input signal on terminal 9 is +6.2 Vdc (a logical "1"), Q1.0 conducts and the cathode of shifting diode CR1.0 is held to less than +0.5 Vdc. The anode voltage of CR1.0 is approximately −8.2 Vdc due to the voltage drop across the diode. With this voltage condition, Q2.0 conducts to saturation and Q3.0 is cut off resulting in an output of +6.2 Vdc on terminal 10.

10.03A When the input signal on terminal 9 is less than +0.5 Vdc, Q1.0 is cut off and the cathode of CR1.0 becomes approximately +8.2 Vdc. The anode voltage of CR1.0 is approximately zero volt due to the voltage drop across the diode. This voltage condition results in Q2.0 being cut off and Q3.0 conducts to saturation. An output voltage of −6.2 Vdc is applied through terminal 10.

10.04A A low-pass filter using L1.0, C2.0, and R8.0 increases the rise and fall time of the driver output to approximately 11 microseconds (under no-load condition).

10.05A The interface terminator circuit is an emitter-coupled flip-flop circuit with two stable states. Input terminals 7 and 13 accept either balanced or unbalanced bipolar signals. The balance control R10 biases Q4 and Q5 to operate on equal but opposite polarity signals applied to terminal 7.

10.06A When Q5 is cut off, output terminal 12 is clamped to +6.2 Vdc, and Q6 conducts with a base potential provided through R17 and emitter-follower Q7. A positive input signal on input terminal 7 will cause Q5 to conduct through emitter-follower Q4, and the voltage at output terminal 12 will drop to approximately +0.5 Vdc. When Q5 conducts, Q6 is operated into cutoff. Transistor Q5 continues to be saturated, by the potential supplied through R12 and Q4, until the input signal on terminal 7 becomes negative. With a negative input signal, Q5 is cut off and Q6 conducts again.

10.07A Output terminal 11 always is the inverse of that signal on terminal 12.

MIL. STD 188B Interface Test

A. Test Equipment

1 — Oscilloscope, Tektronix 535A with type 53/54C plug-in unit (or equivalent)

2 — Probes, Tektronix P6006 (10X) (or equivalent)

1 — DC voltmeter, 0 to 10 volts dc, 20,000 ohm/volt calibrated to 0.5 percent full scale accuracy

1 — Square-wave generator, Hewlett-Packard 211A (or equivalent)

1 — Sine-wave generator, Hewlett-Packard 200CD (or equivalent)

1 — AC voltmeter, Hewlett-Packard 400L (or equivalent)

1 — Transformer, WECo Rep 120C (or equivalent)

1 — Capacitor, 40 uf (±20 percent), WECo 602A (or equivalent)

4 — Resistors:

1 — 5110 ohms (±1 percent), 1/2 watt, WECo 221A (or equivalent)

1 — 2150 ohms (±1 percent), 1/2 watt, WECo 145A (or equivalent)

1 — 511 ohms (±1 percent), 1/2 watt, WECo 221A (or equivalent)

1 — 100 ohms (±1 percent), 1/2 watt, WECo 221A (or equivalent).

B. Power Requirements

+18.0 (±0.5) Vdc — 50 mA

−18.0 (±0.5) Vdc — 50 mA

C. Test Procedures

10.08A ***Zener Voltage Test:***

(1) With ground connected to terminals 5 and 17 and +18.0 (±0.5) Vdc applied to terminal 1, measure the voltage between test point 3 and ground with the calibrated voltmeter. The voltage should be between +5.8 and +6.6 Vdc.

(2) Apply −18.0 (±0.5) Vdc to terminal 20. Measure the voltage between test point 6 and ground with the calibrated voltmeter. The voltage should be between −5.8 and −6.6 Vdc.

10.09A ***Driver Pulse Test:***

(1) With the circuit pack connected to the suggested test circuit shown in Fig. 65A, connect +18.0 (±0.5) Vdc to terminal 1, −18.0 (±0.5) Vdc to terminal 20, and ground to terminals 5 and 17.

(2) Set the frequency of the square-wave generator to about 5000 Hz with a duty cycle of 50 percent.

(3) Set the scope EXT SYNC TRIGGER selector to the (+) positive position.

(4) The input waveform should be as specified in Fig. 66A.

(5) Observe the output of each of the three interface drivers by rotating the switch through positions 1 to 3. At each position, the output shall be as specified in Fig. 66A.

(6) Set the scope EXT SYNC TRIGGER selector to the (−) negative position. Rotate the switch through positions 1 to 3. The output waveform at each position shall be as specified in Fig. 66A.

10.10A ***Terminator Balance Adjustment:***

(1) With the circuit pack connected to the suggested test circuit shown in Fig. 67A, connect +18.0 (±0.5) Vdc to terminal 1, −18.0 (±0.5) Vdc to terminal 20, and ground to terminals 5, 13, and 17.

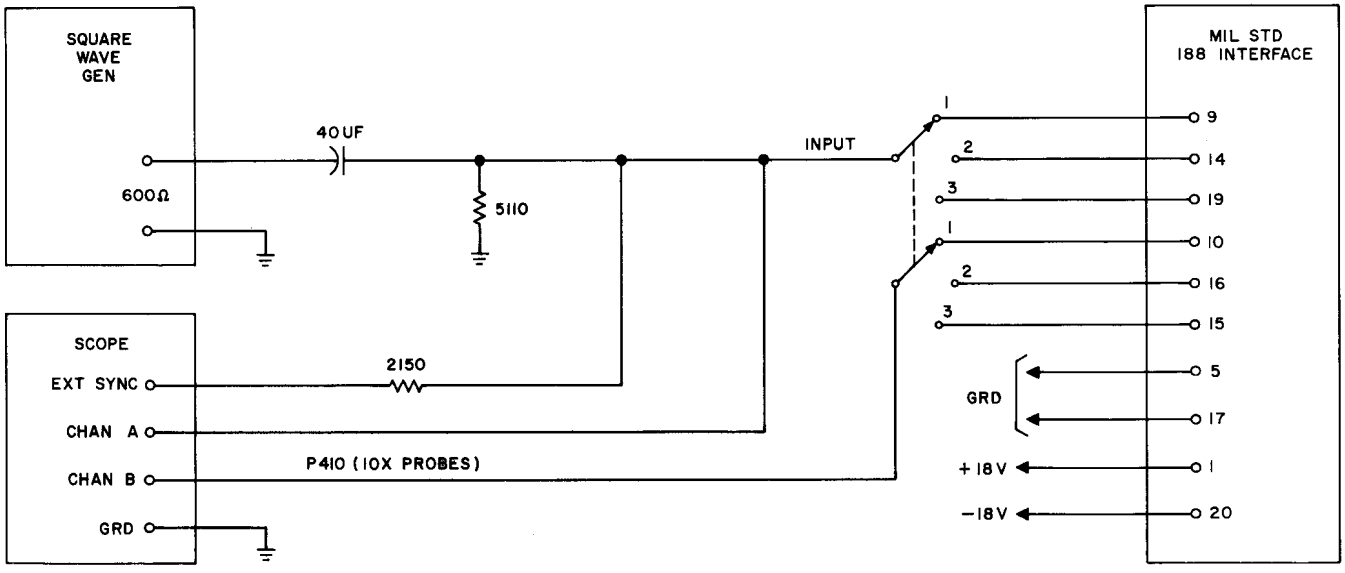


Fig. 65A — MIL. STD 188B Interface Test Circuit

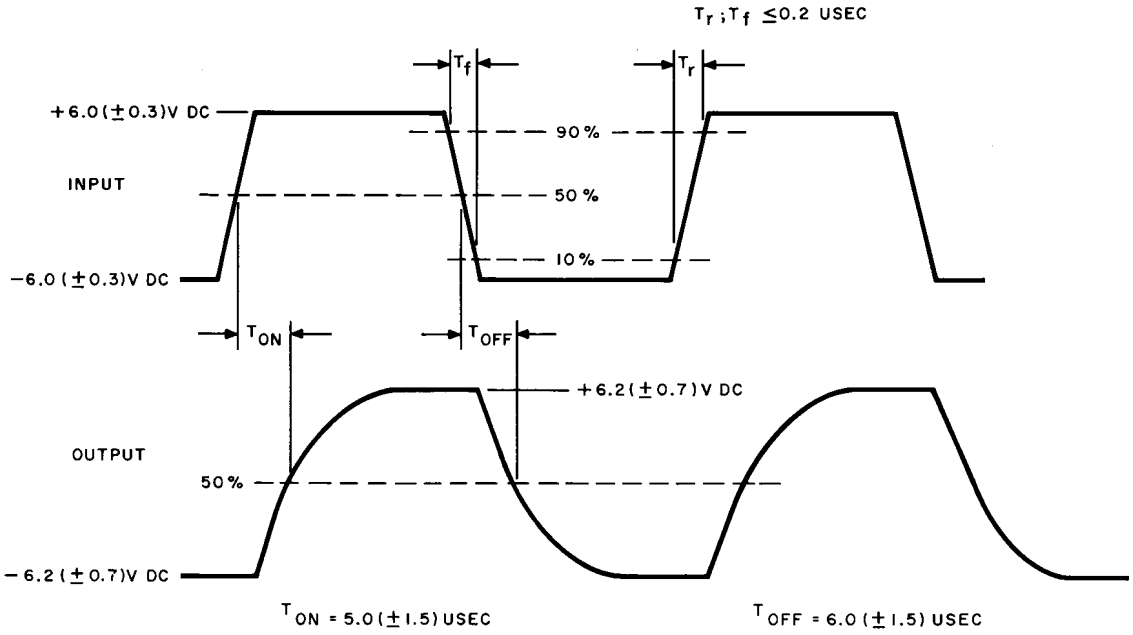


Fig. 66A — MIL. STD 188B Interface Test

(2) Set the controls on the oscillator so that the input sine wave to terminal 7 is about 1.5 volts rms with a period of 200 (±10.0) μsec (5000 Hz).

(3) Make the following settings and connections on the scope:

(a) Connect the vertical signal output to the TIME BASE B TRIGGER input.

(b) Rotate the TIME BASE A TRIGGER stability control fully clockwise.

(c) Set the MODE selector on the dual trace amplifier to ALTERNATE.

(d) On the dual trace amplifier, set the CHAN A polarity switch to the (+) positive position and the CHAN B polarity switch to the (—) negative position.

(e) Set the TIME BASE B TRIGGER mode to the dc position and the trigger slope to the (+) EXT position.

(f) Set the TIME BASE B TIME/CM selector to 20 μsec.

(g) Set HORIZONTAL DISPLAY to B.

(4) Adjust the TIME BASE B STABILITY and TRIGGERING LEVEL controls to obtain a display of the waveform on test point 4. Overlay the CHAN A and CHAN B waveforms as shown in Fig. 68A by adjusting the AMPLIFIER VERTICAL POSITION controls. The TRIGGERING LEVEL control should be set in a region where a slight counterclockwise or clockwise movement does not cause T_D to vary.

(5) Adjust potentiometer R10 until the negative transition of the A sweep precedes the negative transition of the B sweep by approximately 20 μsec.

(6) Reduce the amplitude of input sine wave to 0.35 (±0.01) volt rms.

(7) Rotate potentiometer R10 clockwise until the negative transition of the A sweep precedes the negative transition of the B sweep by approximately 4 μsec (ie, T_D is approximately 4 μsec as shown in Fig. 68A).

(8) Set the HORIZONTAL DISPLAY selector to the B-INTENSIFIED-BY-A position. Set the TIME BASE A TIME/CM selector to 1 μsec.

(9) Adjust the delay time multiplier until the intensified portion of the sweep overlays the negative transitions of the displayed waveforms.

(10) Rotate the HORIZONTAL DISPLAY selector to the A-DELAYED-BY-B position.

(11) Rotate R10 clockwise until T_D is less than 0.5 μsec. Because of backlash, it is important that the final setting be made in the clockwise direction. If T_D is made greater than 0.5 μsec by excessive clockwise rotation of R10, back off in the counterclockwise direction until T_D is approximately equal to 10 μsec, then reduce T_D to less 0.5 μsec by rotating R10 in the clockwise direction.

(12) Set the HORIZONTAL DISPLAY selector to the B position. Set the AMPLIFIER MODE switch to the A ONLY position. reduce T_D to less 0.5 μsec by rotating R10 in terminal 7 to 0.1 ($\pm$0.005) volt rms. A square wave, with arbitrary duty cycle, should be observed at test point 4. No time base measurements need be taken.

(13) After initial adjustment of R10 and upon subsequent tests of the MIL. STD 188B interface circuit pack, it shall not be required to adjust R10 if T_D is less than 4 μsec.

10.11A ***Terminator Pulse Test:***

(1) Connect the circuit pack to the suggested test circuit shown in Fig. 69A.

(2) Set the frequency of the square-wave generator to 5000 Hz ($\pm$5 percent) with a duty cycle of 50 percent. Set the amplitude of the input pulse on terminal 7 (test point 8) to 2.0 ($\pm$0.6) Vdc.

(3) The input pulse on test point 8 should be as specified in Fig. 70A.

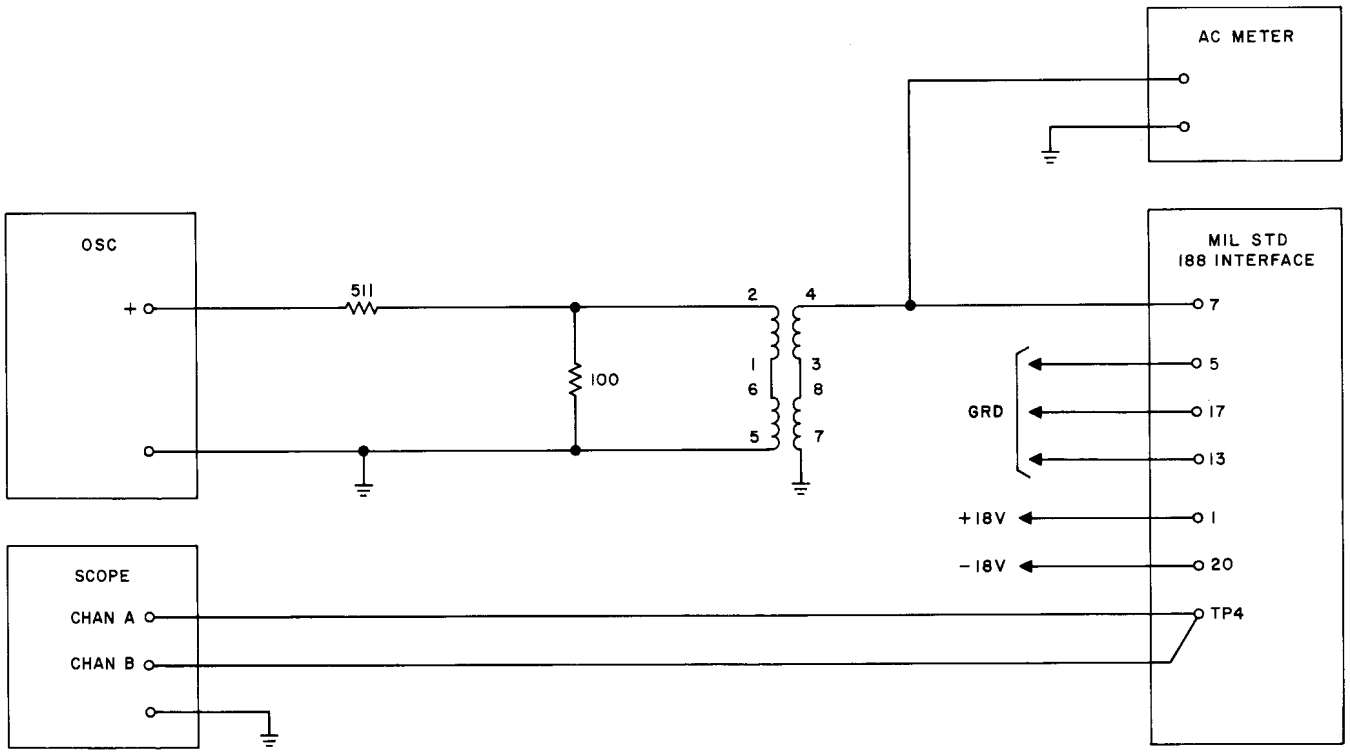


Fig. 67A — MIL. STD 188B Interface Test Circuit

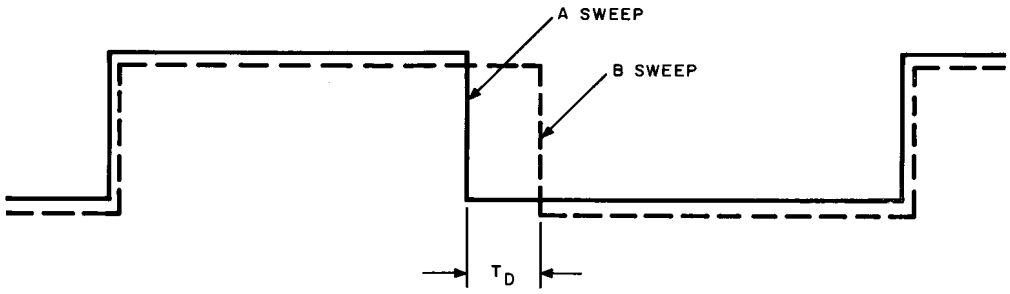


Fig. 68A — MIL. STD 188B Interface Test

(4) Set the scope EXT SYNC TRIGGER selector to the (+) positive position. The output pulse on terminal 12 should be as specified in Fig. 70A (1). Measure T17. Set the EXT SYNC TRIGGER SLOPE to the (—) negative position and measure T27.

(5) The output pulse on terminal 11 should be as specified in Fig. 70A (2). With the EXT SYNC TRIGGER selector set at the (+) positive position, measure T14. Set the trigger slope to the (—) negative position and measure T24.

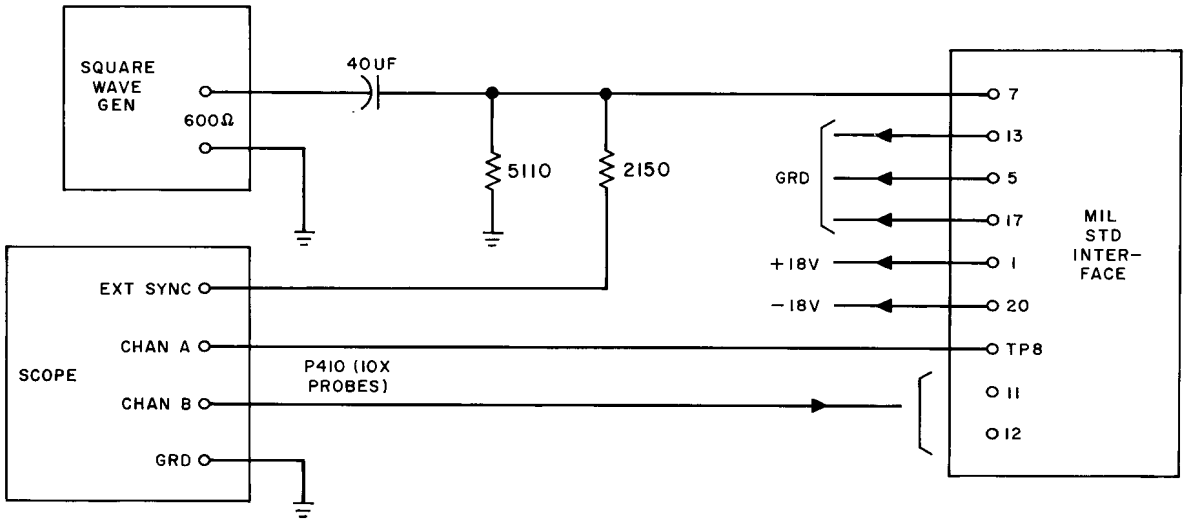


Fig. 69A — MIL. STD 188B Interface Test Circuit

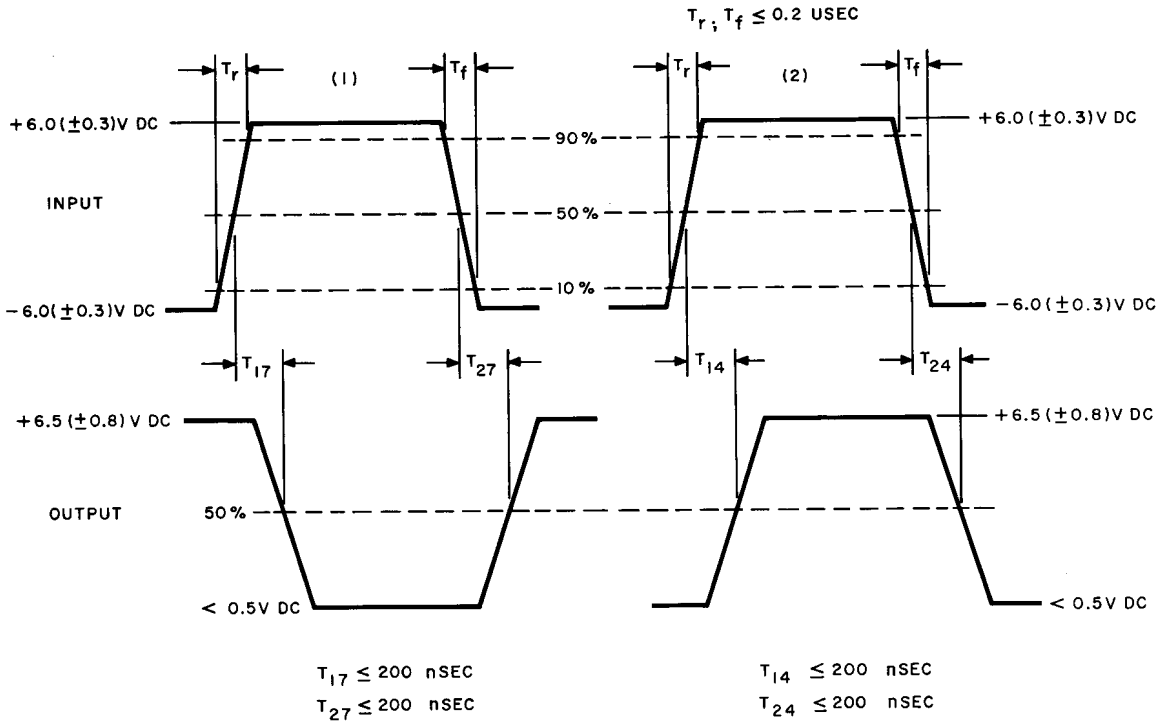
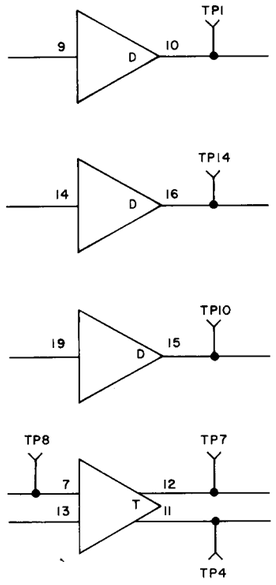
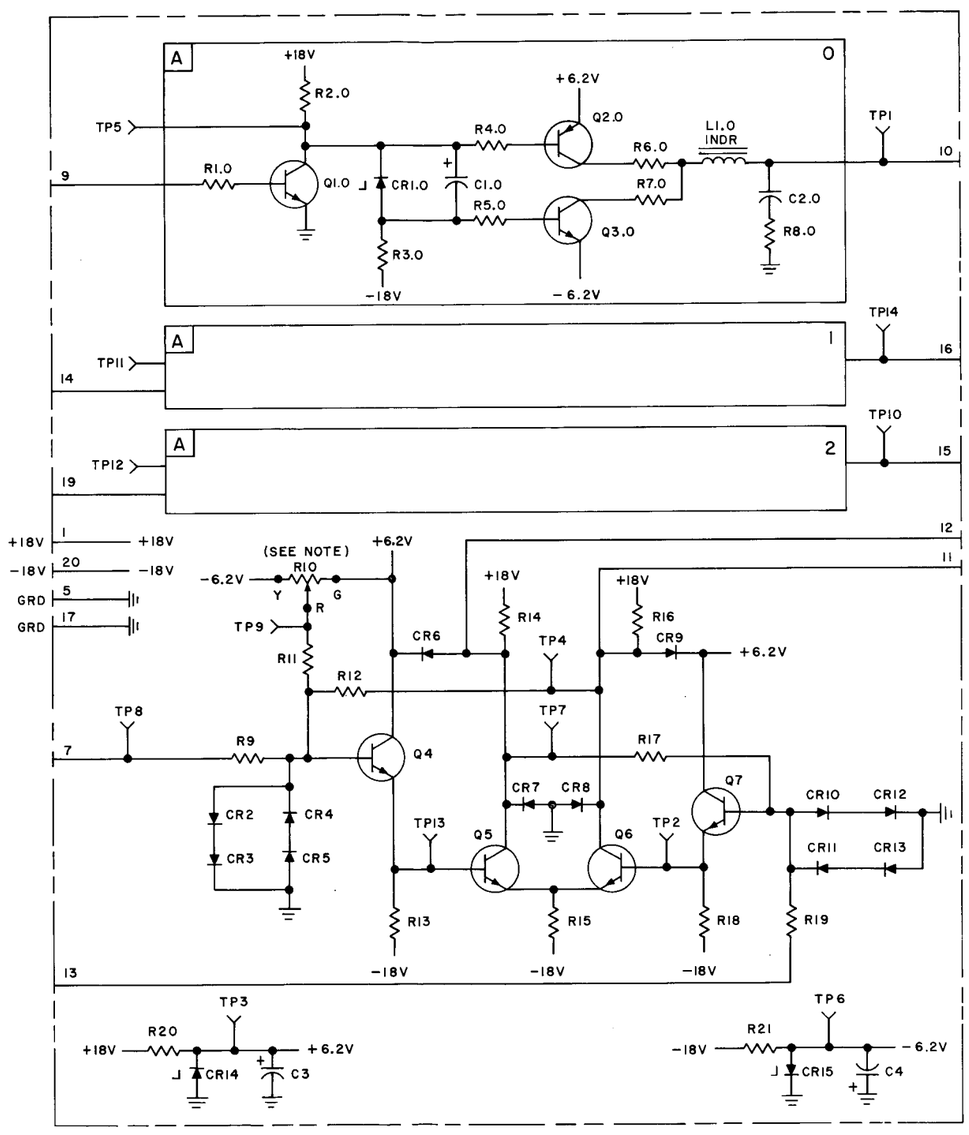


Fig. 70A — MIL. STD 188B Interface Test

SYMBOL



MIL STD 188 INTERFACE



NOTE:

AT THE TIME THE PRINTED WIRING BOARD IS MANUFACTURED, POTENTIOMETER R10 IS ADJUSTED WITH TERMINAL 13 GROUNDED SO THAT THE TERMINATOR SWITCHES WITHIN LESS THAN ±0.3 VOLTS, AND AT MAGNITUDES DIFFERING BY LESS THAN 50 MILLIVOLTS, APPLIED TO TERMINAL 7. NO CHANGE IN ADJUSTMENT IS EVER REQUIRED UNLESS COMPONENTS ARE REPLACED.

Fig. 71A — MIL. STD 188B Interface, Circuit Pack Assembly AR94 (A835186), Circuit Sketch

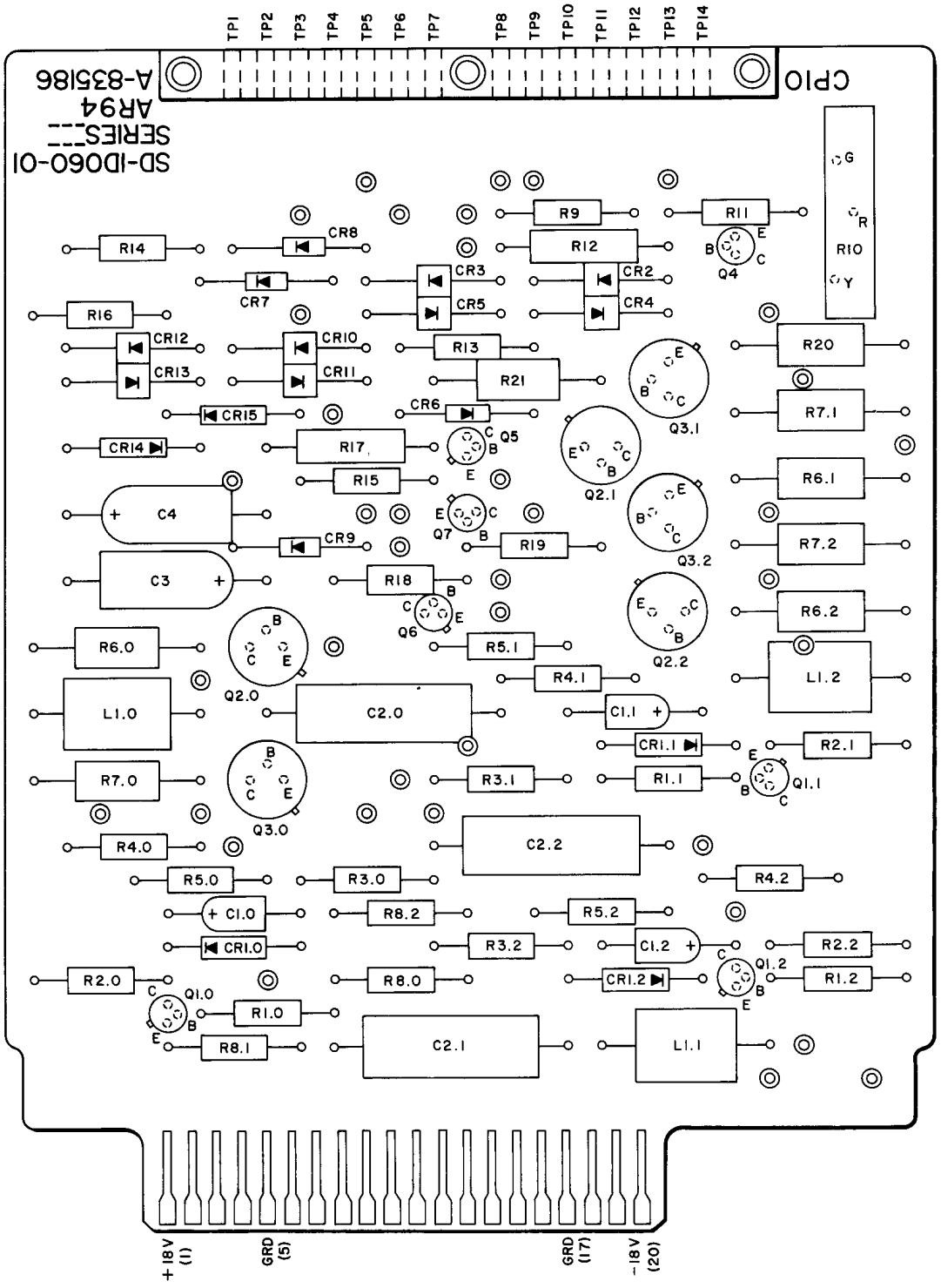


Fig. 72A — MIL. STD 188B Interface, Circuit Pack Assembly AR94 (A835186), Component Location

11A. TRANSMIT-RECEIVE SWITCH CIRCUIT PACK ASSEMBLY AR95 (A835181)

11.01A *Circuit Description:* The AR95 circuit pack contains the transmit-receive driver and the transmit-receive switch control components. The following descriptions are illustrated by a circuit sketch that follows the test procedures.

11.02A When the driver input signal on terminal 2 is less than +0.5 Vdc (a logical "0"), Q1 is cut off and Q2 conducts. The base of Q2 and the output signal is held at +12 Vdc through clamping diode CR13. When the input signal on terminal 2 is +6.2 Vdc (a logical "1"), Q1 conducts and Q2 is cut off by the voltage across CR12. The output signal is now held to less than +1.0 Vdc. The driver output signal through terminal 33 and +6.8 Vdc at terminal 37 are connected to the transmit-receive switch control circuits by straps external to the circuit pack.

11.03A Transmitted line signals are controlled by the following components; CR1, CR2, CR3, CR15, R1 through R5, and R18.

11.04A Receiver inputs (terminals 13 and 14) connect directly to the receive line transformer. Terminal 10 is externally strapped to terminal 31 to provide 600-ohm termination for the transmit line.

11.05A CR4 and CR5 provide surge protection for the transmit circuits. CR10 and CR11 provide surge protection for the receive circuits.

Transmit-Receive Switch Test

Note: Located on the circuit pack are four slotted machine screw terminals numbered 1 to 4. A strap should be inserted between screws 3 and 4. There should not be a strap between screws 1 and 2.

A. Test Equipment

1 — DC vacuum tube volt-ohmmeter, Hewlett-Packard 412A (or equivalent). DC accuracy ±1 percent; ohmmeter ±5 percent

3 — Resistors:

1 — 1000 ohms (±1 percent), 1/2 watt, WECo 145A (or equivalent)

1 — 1.78 meg (±1 percent), 1/2 watt, WECo 221A (or equivalent)

1 — 2370 ohms (±5 percent), 1/2 watt, WECo 221A (or equivalent).

B. Power Requirements

+18.0 (±0.5) Vdc — 75 mA

+30 (±1.5) Vdc — 50 mA

C. Test Procedures

11.06A *Resistance Test:*

(1) The following resistance tests are to be made before voltage is applied to the circuit pack. Connect ground to terminals 5 and 17. A strap should be inserted between screws 3 and 4. There should not be a strap between screws 1 and 2.

(2) The resistance between the following terminals shall be as indicated.

TERMINALS	RESISTANCE VALUE OHMS
13 to 14	20 (±20%)
13 to 18	521 (±10%)
19 to 38	68 (±20%)
3 to 8	348 (±5%)
9 to 22	348 (±5%)
11 to 10	316 (±5%)
12 to 31	316 (±5%)
4 to GRD	Less than 1
6 to GRD	Less than 1
15 to GRD	Less than 1
16 to GRD	Less than 1
40 to GRD	Less than 1
Screw No. 1 to 23	Less than 1
Screw No. 2 to GRD	Less than 1
Screw No. 3 to GRD	Less than 1
Screw No. 4 to 40	Less than 1

(3) The following resistance tests result in values that depend on the direction of current flow from the test instrument. In Table E, the resistance values indicated correspond to current flow from terminal A to terminal B as listed. In the Hewlett-Packard model 412A, test current flows from the MA/OHM probe when the TEST FUNCTION selector is in the OHMS position; therefore, the MA/OHM probe should be applied to the terminal listed as FROM and to the common probe to the terminal listed as TO.

TABLE E

CURRENT FLOW RESISTANCE VALUES

TERMINALS		REMARKS	RISISTANCE
FROM	TO		OHMS
27	33		196 (±5%)
33	27	RANGE Selector on 100X	Less than 100
11	7	RANGE Selector on 100X	Less than 100
7	11		1210 (±5%)
12	30	RANGE Selector on 100X	Less than 100
30	12		1210 (±5%)

11.07A ***Diode Leakage Test:*** Remove ground from terminals 5 and 17.

(1) Connect +18.0 (±0.5) Vdc in series with a 1.78 meg (±1 percent) resistor to terminal 11. Apply ground to terminal 9. The current drawn from the +18.0 Vdc supply shall be less than 7.0 uA dc.

(2) Repeat (1) for terminal 12 with ground connected to terminal 8.

(3) Repeat (1) for terminal 9 with ground connected to terminal 8.

(4) Repeat (1) for terminal 8 with ground connected to terminal 9.

11.08A ***Zener Voltage Test:***

(1) With ground connected to terminals 5 and 17, connect +18.0 (±0.5) Vdc to terminal 1.

(2) The voltage between terminal 37 and ground shall be +6.8 (±0.8) Vdc.

(3) The voltage between test point 6 and ground shall be +12.0 (±1.5) Vdc.

(4) Apply +30.0 (±1.5) Vdc in series with a 1000-ohm (±1 percent) resistor to terminal 29. The voltage between terminal 29 and ground shall be +18.0 (±2.3) Vdc.

(5) Repeat (4) for terminals 39, 11, and 12.

11.09A ***Bias Voltage Test:*** With ground connected to terminals 5 and 17 and +18.0 (±0.5) Vdc connected to terminal 1, the voltage between terminal 8 and ground, between terminal 9 and ground, between terminal 11 and ground, and between terminal 12 and ground shall be 3.0 (±0.3) Vdc.

11.10A ***T-R Switch Driver Test:***

(1) Make the following connections on the circuit pack under test:

(a) Connect ground to terminals 5 and 17.

(b) Connect +18.0 (±0.5) Vdc to terminal 1.

(c) Connect terminal 11 to terminal 37.

(d) Connect a 2370-ohm (±1 percent) resistor between terminals 37 and 2.

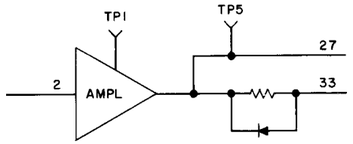
(e) Connect terminal 9 to terminal 33.

(2) The voltage between terminal 27 and ground shall be less than 1 volt dc.

(3) Remove the connection between terminals 37 and 2. Connect ground to terminal 2.

(4) The voltage between terminal 27 and ground shall be +11.8 (±1.6) Vdc.

SYMBOL



TRANSMIT – RECEIVE SWITCH

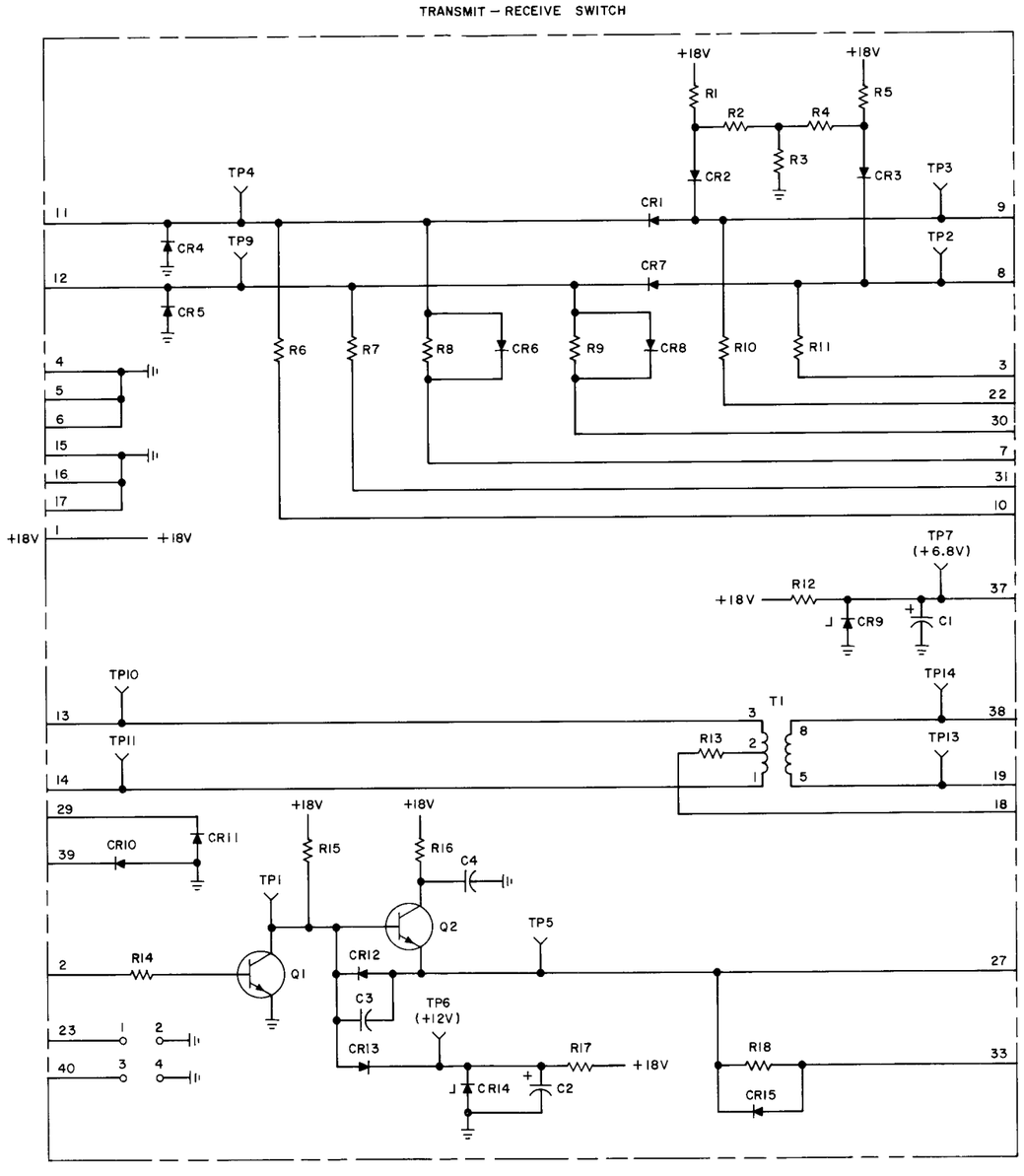


Fig. 73A — Transmit-Receive Switch, Circuit Pack Assembly AR95 (A835181), Circuit Sketch

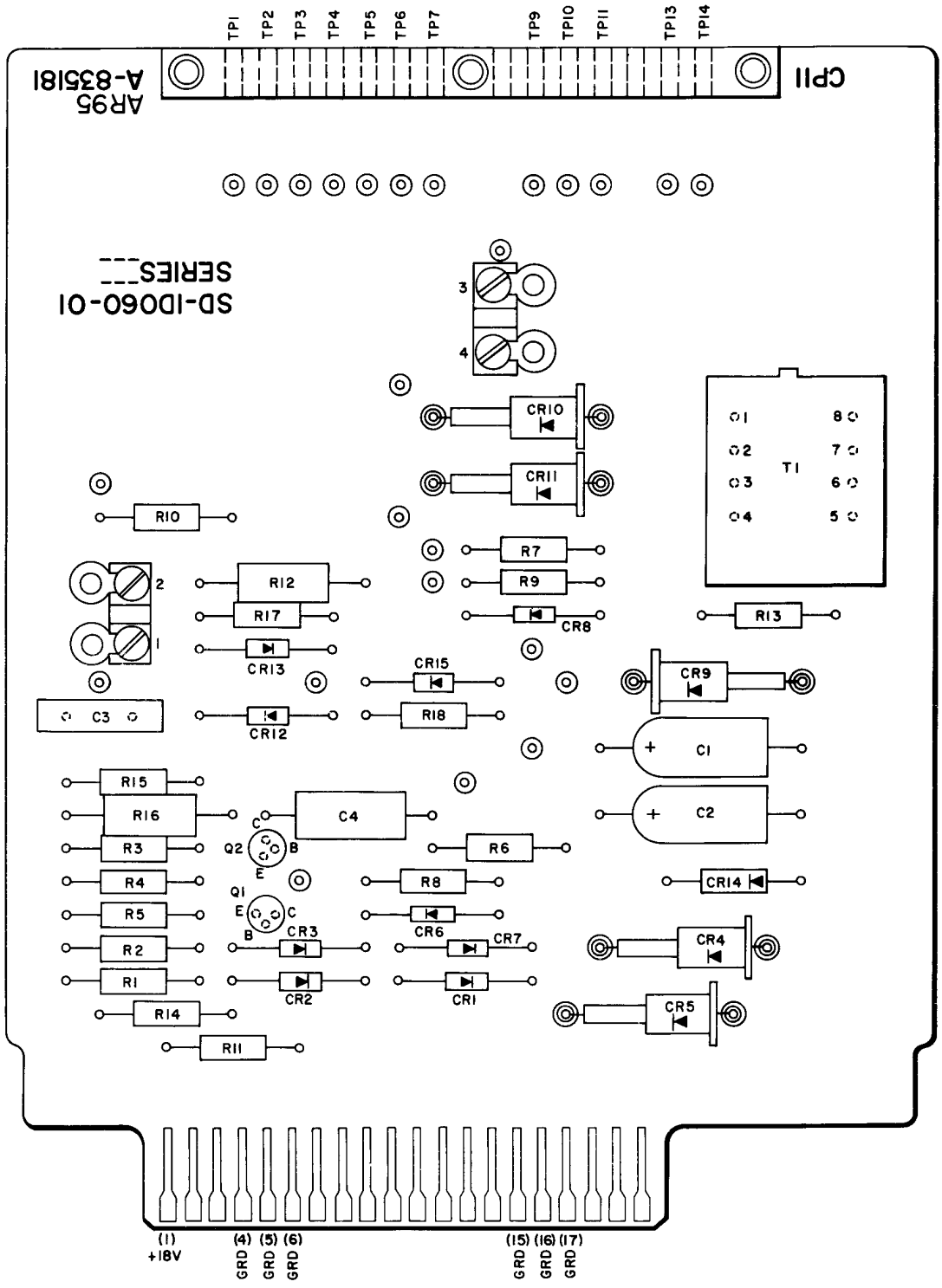


Fig. 74A — Transmit-Receive Switch, Circuit Pack Assembly AR95 (A835181), Component Location

12A. DEMODULATOR CIRCUIT PACK ASSEMBLY AR96 (A835180)

12.01A *Circuit Description:* The AR96 circuit pack contains two input amplifiers, an intermediate amplifier, an output amplifier and two cross-coupled diode networks which provide signal phase comparison for both direct and delayed line signals. The following descriptions are illustrated by a circuit sketch that follows the test procedures. Required external connections are illustrated in Fig. 75A.

12.02A One input amplifier, using Q1 and Q2, buffers and amplifies delayed line signals for application across T1. The remaining input amplifier, using Q3, buffers and amplifies signals for application across T2.

12.03A Signals on the transformer secondary windings are applied to the cross-coupled diode networks which consist of the following components: CR2 through CR5, CR7 through CR12, CR14, CR15, and R10 through R17. Without an input line signal, current through R10, R11, R16, and R17 will forward bias CR2 through CR5 and CR7 through CR10, and will flow to the center-tap of T1 and T2. Consequently, CR11, CR12, CR14, and CR15 are cut off or near cut off and the differential amplifier (using Q4 and Q6) is cut off.

12.04A When a line signal is applied to the input amplifiers and the signals at the amplifier outputs are approximately in phase (ie, the signals differ by ±45°), the following circuit reaction occurs. During the positive half-cycle of the two signals, bias current through CR3 and CR7 is reduced because of almost simultaneous positive signal voltages at terminal 8 of both T1 and T2. CR11 and Q4 will conduct as the voltage at R10 and CR11 becomes positive with respect to the —18 volt supply.

12.05A During the negative half-cycle of the two signals, bias current through CR4 and CR10 is reduced because of almost simultaneous positive signal voltages at terminal 5 of both T1 and T2. CR12 and Q4 will conduct at the voltage at R11 and CR12 become positive with respect to the —18 volt supply.

12.06A If the applied line signals across T1 and T2 are out-of-phase, (ie, the signals differ by ±135°), CR2 and CR9 are near cut off by the positive voltages at both terminal 8 of T1 and terminal 5 of T2 during one half-cycle. This condition permits CR15 and Q6 to conduct. The next half-cycle conditions CR5 and CR8 near cut off to permit CR14 and Q6 to conduct.

12.07A Signals on the collectors of Q4 and Q6 are negative pulses produced by the AND/OR analog logic circuits. These signals represent the nearly in-phase or out-of-phase character of both the applied direct and delayed phase-modulated line signal. The signals are applied to external low-pass filters through terminals 16 and 18. The low-pass filters remove harmonics of the demodulated line signal. Signals from the filters are applied to the differential output amplifier through terminals 15 and 12.

12.08A The differential output amplifier, Q5 and Q7, amplifies the demodulated data waveform and provides output signals through terminals 14 and 13 which are suitable for operating the digital data receiver gates.

Demodulator Circuit Pack Test

A. Test Equipment

1 — Oscilloscope, Tektronix 533 with type CA plug-in unit (or equivalent)

2 — Oscillators, Hewlett-Packard 200CD (or equivalent)

1 — DC voltmeter, 20,000 ohm/volt, ±1 percent, Hewlett-Packard 412A (or equivalent)

1 — AC voltmeter, ±3 percent, Hewlett-Packard 400L (or equivalent)

2 — Capacitors, 2.0 uf, (±5 percent), WECo 542F (or equivalent).

B. Power Requirements

+18.0 (±0.5) Vdc — 25 mA

—18.0 (±0.5) Vdc — 100 mA

C. Test Procedures

(1) Connect ground to terminals 5 and 17, +18.0 (±0.5) Vdc to terminal 1, and −18.0 (±0.5) Vdc to terminal 20.

(2) The voltage between test point 3 and ground shall be −8.2 (±1.0) Vdc.

(3) The voltage between test point 6 and ground shall be +6.2 (±0.4) Vdc.

(4) The voltage between test point 4 and terminal 20 shall be +12 (±1.5) Vdc.

12.09A ***Demodulator Test:***

(1) Connect the circuit pack to the suggested test circuit shown in Fig. 75A.

(2) With the amplitude control of oscillator No. 2 set to 0, temporarily connect ground to input terminal 19.

(3) Set the controls of oscillator No. 1 to produce a 0.2 (±0.005) volt rms signal at 1800 Hz between input terminal 4 and ground. The waveform between test point 5 and ground shall be a sine wave of 0.68 (±0.15) Vac peak-to-peak.

(4) Remove the ground connection from input terminal 19. With the amplitude control of oscillator No. 1 set to 0, temporarily connect ground to terminal 4.

(5) Set the controls of oscillator No. 2 to produce a 0.5 (±0.005) volt rms signal at 1800 Hz between input terminal 19 and ground. The waveform between test point 10 and ground shall be a sine wave of 0.68 (±0.15) Vac peak-to-peak. Remove the ground connection from terminal 4.

(6) Set the controls of oscillator No. 1 to produce a 0.32 (±0.005) Vac rms signal at 1800 Hz between input terminal 4 and ground.

(7) Set the controls of oscillator No. 2 to produce a 0.80 (±0.005) Vac rms signal at 1800 Hz between input terminal 19 and ground.

(8) Connect the scope, using the differential mode of operation, to terminals 16 and 18. Satisfactory synchronization may be obtained by connecting EXT SYNC to VERTICAL SIGNAL OUT on the scope. The output waveform shall be a sine wave. Track the frequency of oscillator No. 2 in the vicinity of 1800 Hz until the frequency of the output sine wave is approximately 2 Hz. The output sine wave will have an amplitude of 12.5 (±2.5) Vac peak-to-peak.

(9) With the controls of the oscillators set as in (8), connect the scope, using the differential mode, to terminals 13 and 14. The output waveform shall be a square wave of approximately 2 Hz with amplitude 12.4 (±1.2) Vac peak-to-peak.

(10) Increase the frequency of oscillator No. 2 to approximately 2700 Hz. With the EXT SYNC TRIGGER selector set to the (+) positive position, expand the TIME/CM selector until an overlay of positive transitions is displayed on the scope as shown in Fig. 76A. The rise time of the first transition shall be as specified in Fig. 76A.

(11) Momentarily turn off oscillator No. 1. The differential voltage between terminals 13 and 14 shall be less than 150 mV peak-to-peak. Turn on oscillator No. 1. Momentarily turn off oscillator No. 2. The differential voltage between terminals 13 and 14 shall be less than 150 mV peak-to-peak.

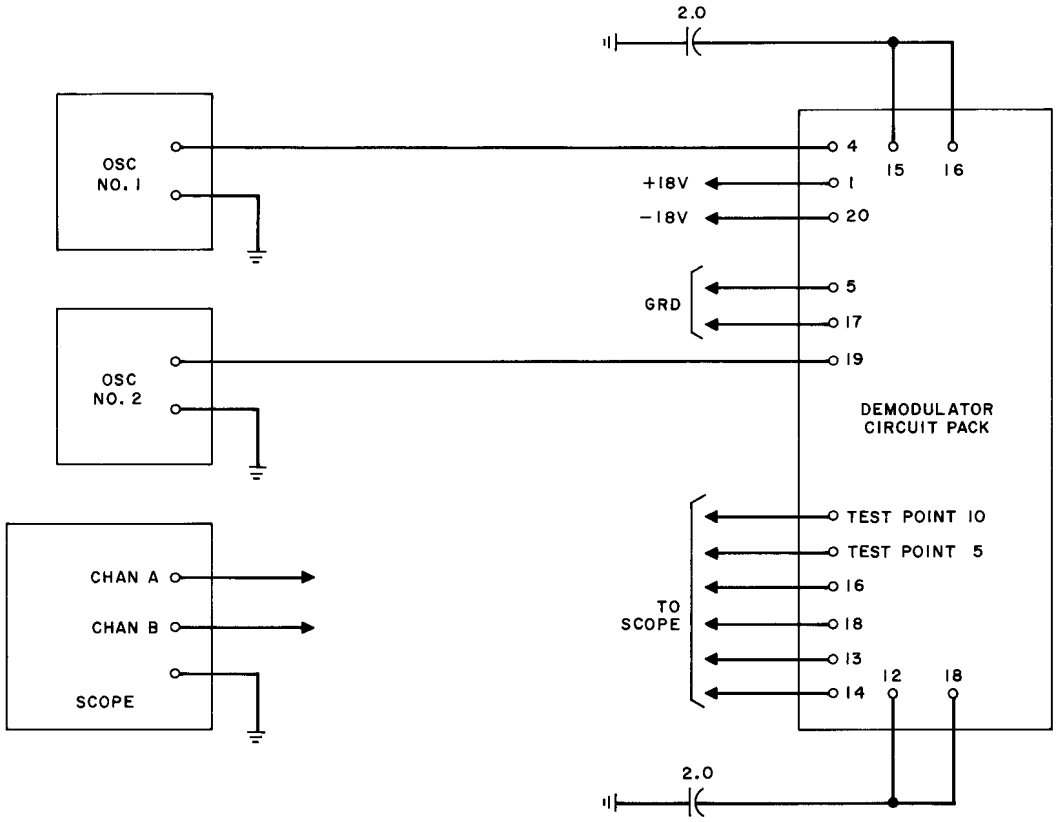


Fig. 75A — Demodulator Circuit Pack Test Circuit

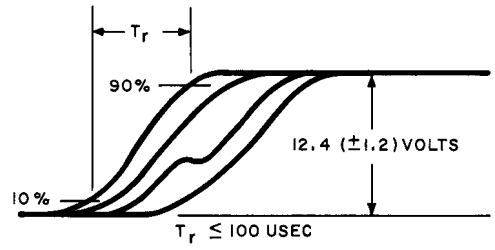
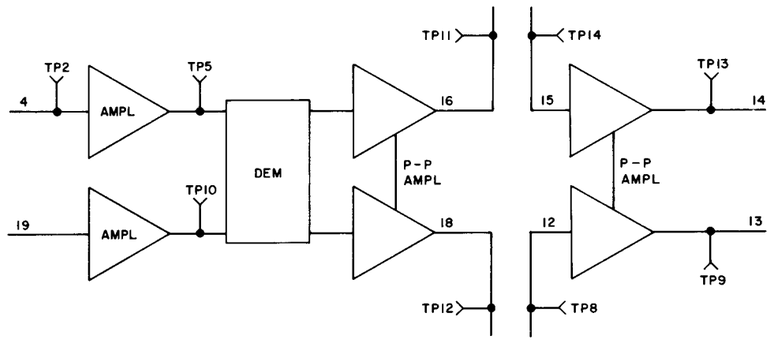


Fig. 76A — Demodulator Circuit Pack Test

SYMBOL



DEMODULATOR

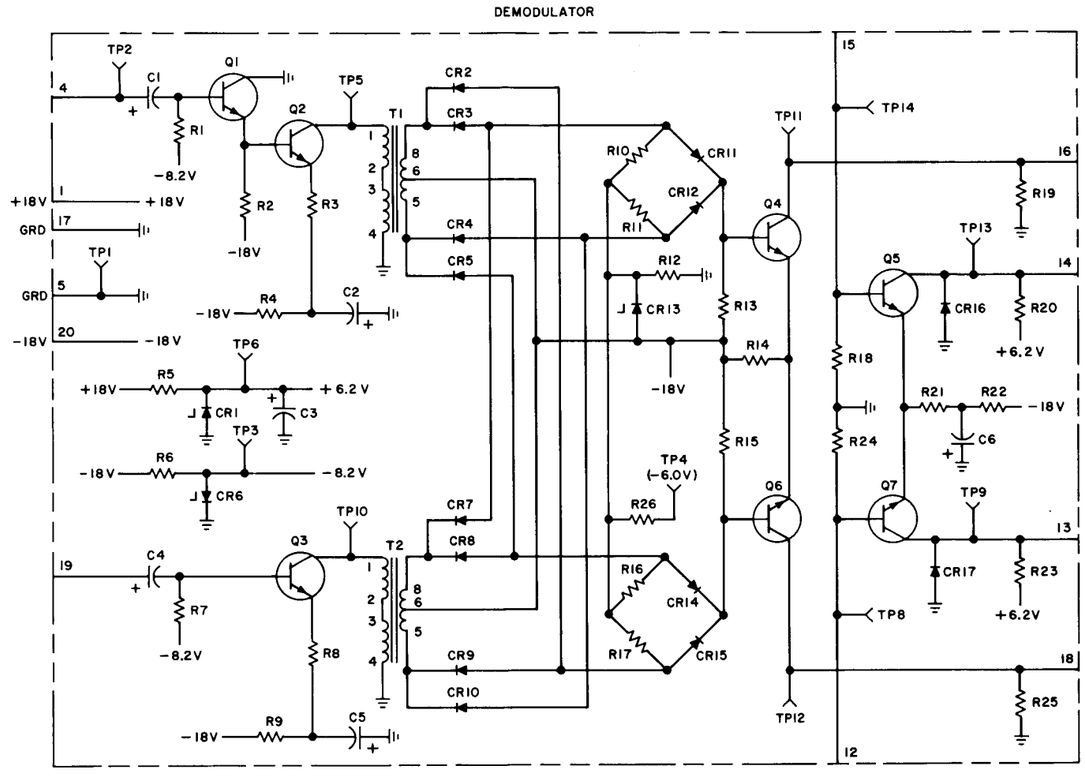


Fig. 77A — Demodulator, Circuit Pack Assembly AR96 (A835180), Circuit Sketch

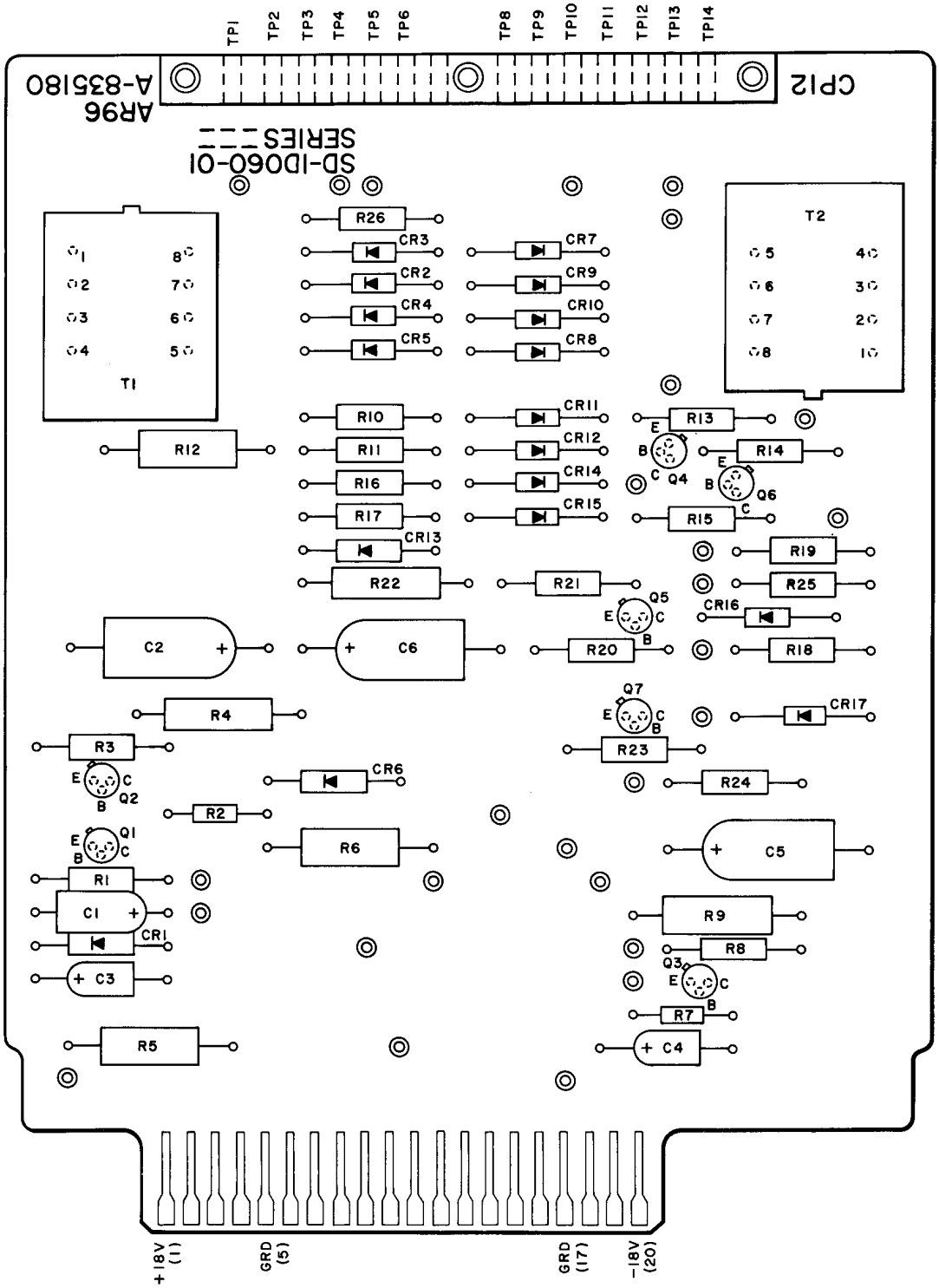


Fig. 78A — Demodulator, Circuit Pack Assembly AR96 (A835180), Component Location

13A. 65A OSCILLATOR CIRCUIT PACK ASSEMBLY

13.01A *Circuit Description:* The 65A oscillator is a stable time base generator. Timing signals are generated by a crystal oscillator, buffer-amplified and shaped in three circuit stages. A circuit sketch is illustrated in Fig. 79A.

13.02A The crystal oscillator circuit is a modified Pierce-type which uses a crystal unit at 230.4 kHz and acts as a positive reactance in series with varactor diode CR3. Temperature compensation is achieved by applying a bias voltage to CR3 which is derived from a temperature compensation network using thermistors RT1 and RT2, together with R14 and R15. Frequency adjustment is made through variable resistor R29 which sets the bias level for CR3. Transistors Q1 and Q3 amplify the crystal signal which is applied through a low-pass filter using L1 and C6. Proper signal phase shift to maintain oscillation is provided by C10. Diode limiting by CR1 and CR2 together with voltage divider R18 and R22 insures a crystal drive level below 10 microamperes. Zener voltage regulation is provided by CR4 and CR5.

13.03A The oscillator signal is coupled through C11 to Q5. The signal is buffer-amplified to drive the output stage.

13.04A The output stage is a Schmitt-Trigger using Q2, Q4, and associated components. Transistors Q2 and Q4 are biased to provide a 6-volt square-wave output with a 60 percent duty cycle. The output signal has a rise and fall time of less than 0.1 microsecond.

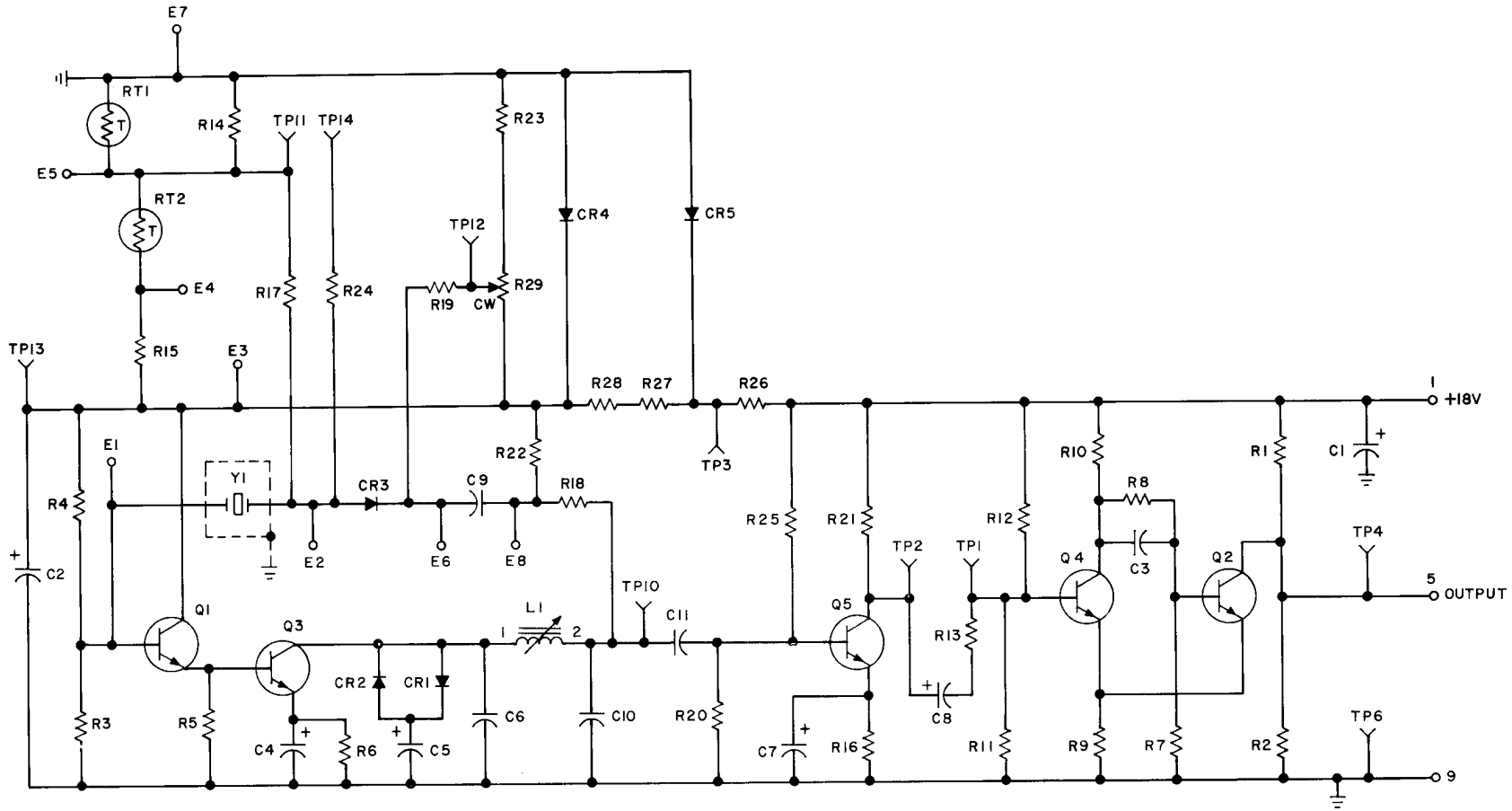


Fig. 79A — 65A Oscillator, Circuit Pack Assembly, Circuit Sketch

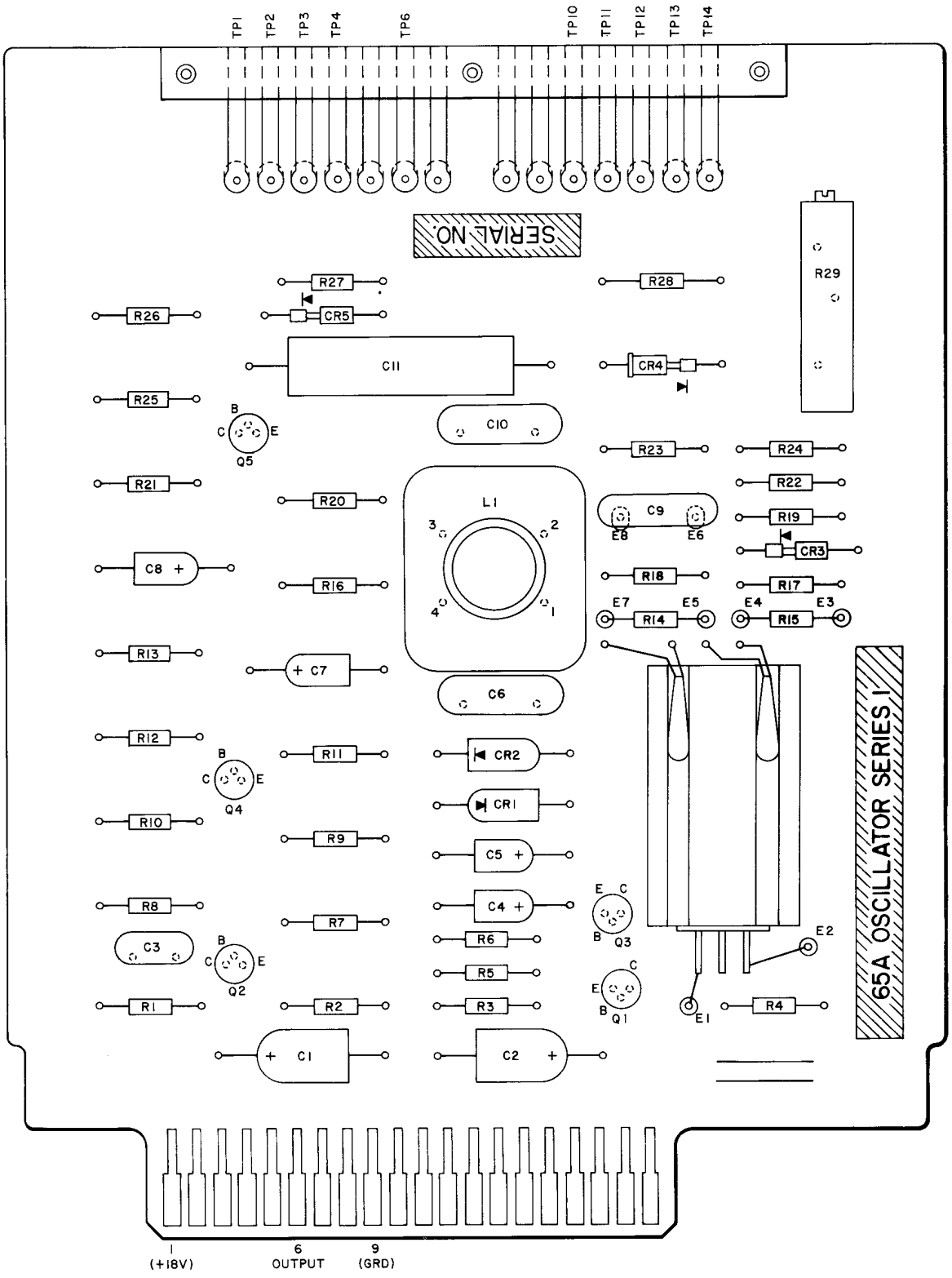


Fig. 80A — 65A Oscillator, Circuit Pack Assembly, Component Location

14A. GLOSSARY OF MNEMONIC SYMBOLS

14.01A The mnemonic symbols used to identify the function of schematic components are briefly defined in the following list. The circuit pack location number is included for reference.

ABBREVIATION	CIRCUIT PACK	DEFINITION
AB0	038	A equals B equals 0
AB1	038	A equals B equals 1
ADR	006	Add and delete registers operated
AGC1	017	Automatic gain control 1
AGC2	016	Automatic gain control 2
A0C	007	A bit — 0 — clear
A0P	008	Pulse on A bit transition from 0
A0T	038	A equals 0 — transmit
AR	039	A register
A1C	007	A bit — 1 — clear
A1P	008	Pulse on A bit transition from 1
B0C	007	B bit — 0 — clear
B0P	008	Pulse on B bit transition from 0
BPF		Band pass filter
BRG	009	B register
BRG-01	009	B register — 0 output inverted
BTRN1	009	B bit transfer — 1
BTRN2	009	B bit transfer — 2
B1C	007	B bit — 1 — clear
B1P	008	Pulse on B bit transition from 1
CI	039	Clear channel I
CI′	038	Clear channel I prime
CII	039	Clear channel II
CLCON	058	Clear confirm
CLCON′	055	Clear confirm prime
CLCTR	054	Clear CS counters
CLDT	039	Clear dibit flip-flop
CON′	059	Confirm prime
CO′	009	Carrier ON prime
COO	059	Carrier ON-OFF
CO1	007	Carrier ON-1
CO′1	008	Carrier OFF prime — 1
CPR	050	Clear prepare receiver
CPR′	050	Clear prepare receiver prime
CPR1	050	Clear prepare receiver — 1
CS	059	Clear to send
CS′	057	Clear to send prime
CS1	054	Clear to send — 1
CSC 0	056	Clear to send counter
CSC 1	056	" " " "
CSC 2	056	" " " "
CSC 3	056	" " " "
CSC 4	056	" " " "
CSC 5	056	" " " "
CSC 6	055	" " " "
CSC 7	055	" " " "
CSC 8	055	" " " "
CTR	001	Run counter output
CTR′	001	Run counter output prime
CTR 0	002	Counter run
CTR 1	002	" "
CTR 2	002	" "
CTR 3	002	" "
DCLK	058	Double clock rate
DFR	057	Clock — double rate — full speed — receive
DFT	058	Clock — double rate — full speed — transmit
DHR	057	Clock — double rate — half speed — receive
DHT	058	Clock — double rate — half speed — transmit
DL		Delay Line
DM	012, 014	Demodulator
DR	053	Clock — dibit receive
DR′C	001	Clock — dibit receive prime clear
DR′G	003	Clock — dibit receive prime gate
DR′G1	001	Clock — dibit receive prime gate — 1
DSR	059	Data set ready
DSR′	057	Data set ready prime
DSRS	054	Data set ready — series circuits
DT′	040	Clock — dibit transmit prime
DTI	059	Dibit timing internal
DT1	039	Clock — dibit transmit — 1
D90	038	90 degree pulse to phase logic
D180	039	180 degree pulse to phase logic

ABBREVIATION	CIRCUIT PACK	DEFINITION
E	040	Clock — envelope
EF	010	Emitter follower
EG	040	Clock — envelope gate
E'G	040	Clock — envelope prime gate
EPR	050	Enable prepare receiver
GRXG	001	Gated receive axis crossing
I90	037	Channel I — 90 degrees
I180	037	Channel I — 180 degrees
II 90	037	Channel II — 90 degrees
II 180	037	Channel II — 180 degrees
INHA	006	Inhibit add
INHD	006	Inhibit delete
MF		Multiple filter
NFR	009	Clock — normal rate — full speed — receive
NFT	058	Clock — normal rate — full speed — transmit
NHR	057	Clock — normal rate — half speed — receive
NHT	058	Clock — normal rate — half speed — transmit
NR	057	Clock — normal receive
NT	058	Clock — normal transmit
OSC	051	Oscillator
PL90	037	Phase logic 90 degrees
PL180	040	Phase logic 180 degrees
PR	059	Prepare receiver
PR'	050	Prepare receiver prime
PR1	050	Prepare receiver — 1
PRC 0	049	Prepare receiver counter
PRC 1	049	" " "
PRC 2	049	" " "
PRC 3	049	" " "
PRC 4	049	" " "
PRC 5	049	" " "
PSG	006	Phase select gate pulse
RAD	006	Receive add correction
RAD'	006	Receive add correction prime
RAD1	006	Receive add correction — 1
RAS	001	Receive add register input
RAR	005	Receive add register
RCLR	002	Run counter clear
RCLR1	006	Run counter clear

ABBREVIATION	CIRCUIT PACK	DEFINITION
RD	060	Receive data
RD'	007	Receive data prime
RDL	006	Receive delete correction
RDR	005	Receive delete register
RDS	001	Receive delete register input
RDZ'	003	Receive dead zone prime
RGRN	057	Regenerate
RGRN'	059	Regenerate prime
RMT	021	Remote test
RS'	059	Request to send — Prime
RS1	058	Request to send — 1
RSMC	003	Receive sample clear
RSMG	007	Receive sample gate
RTCON	053	Remote confirm
RTRC	003	Receive transfer clear
RTRS	053	Remote test, request to send
RTSS	054	Remote test, speed select
RXG	007	Receive axis crossing pulses
SCR	060	Serial clock receive
SCR1	057	Clock — serial receive — 1
SCT	060	Serial clock transmit
SCT1	058	Clock — serial transmit — 1
SCTE'	059	Serial clock transmit external — prime
SCTE2	009	Clock — serial transmit external — 2
SDBO	058	Send data B data bit clamp to 0
SD'	060	Send data — prime
SD'1	058	Send data prime — 1
SD2'	036	Send data prime — 2
SD2	057	Send data — 2
SD'2	038	Send data prime — 2
SFD	009	Single-frequency detector
SI 90	038	Set channel I — 90 degrees
SI 180	038	Set channel I — 180 degrees
SII 90	038	Set channel II — 90 degrees
SII 180	038	Set channel II — 180 degrees
SR	053	Clock — serial transmit — 1
SS		Speed select
SS'	059	Speed select prime
SS1	039	Speed select — 1
SS'1	039	Speed select prime — 1
SS2	057	Speed select — 2
ST	040	Clock — serial transmit
ST1	054	Clock — serial transmit — 1
STC	043	Clock — serial transmit clear
ST'C	043	Clock — serial transmit prime clear

ABBREVIATION	CIRCUIT PACK	DEFINITION
ST'C1	043	Clock — serial transmit prime clear — 1
STG	043	Clock — serial transmit gate
ST'G	042	Clock — serial transmit prime gate
ST'G1	039	Clock — serial transmit prime gate — 1
SXC	008	Transmit axis crossing pulse — clear
SXG	009	Transmit axis crossing pulse
SXRG	002	Transmit axis crossing pulse register
TAD	043	Transmit add correction
TAR	042	Transmit add register
TAS	043	Transmit add register input
TC1	001	True crossing register — 1
TC2	001	True crossing register — 2
TCR	005	True crossing register
TDL	043	Transmit delete correction pulse
TDR	042	Transmit delete register
TDS	043	Transmit delete register input
TDZ	042	Transmit dead zone
TO	044	Transmit output
TR	055	Transmit — receive
TR'1	054	Transmit — receive prime — 1
TR'2	054	Transmit — receive prime — 2
TRC	054	Clear transmit — receive switch counters
TRCLR	001	Receive clear pulse former input
TRCTR	054	Count input to transmit — receive switch counters
TRSW	019	Transmit — receive switch
VLSR		Variolosser
2SR	003	Clock — 2X serial receive
2ST'	041	Clock — 2X serial transmit prime
2TR'	055	2X Transmit — receive prime
3CS	041	Clock — 3X (Channel) serial
4SR	005	Clock — 4X serial receive
4SR'C	003	Clock — (4X serial receive) prime clear
4ST	041	Clock — 4X serial transmit
4STC	041	Clock — 4X serial transmit clear
4STC1	043	Clock — 4X serial transmit clear — 1
6CS	041	Clock — 6X (Channel) serial
8SR	005	Clock — 8X serial receive
8ST	041	Clock — 8X serial transmit
12SR	005	Clock — 12X serial receive
12ST	042	Clock — 12X serial transmit
24S	053	Clock — 24X serial
24ST	042	Clock — 24X serial transmit
24S1	007	Clock — 24X serial
24SR'1	006	Clock — 24X serial receive prime — 1
48S	053	Clock — 48 times serial clock rate
48S1	054	Clock — 48X serial
48S1'	049	Clock — 48X serial receive prime
48ST'	043	Clock — 48X serial transmit prime
90G	037	Gate pulse — 90 degree phase shift
1000'	058	Thousand code prime