# DATA SET 207-TYPE
# TRANSMITTER-RECEIVER
# IDENTIFICATION AND OPERATION

## 1. GENERAL

**1.01** This section contains descriptive and operational information for the Data Set 207-type Transmitter-Receiver. This section does not include information regarding the business machine used with the data set.

**1.02** For the purpose of this practice, reference to a business machine should be interpreted to mean any customer equipment having input and output signals in accordance with Military Standard 188B and MIL-M-55408 (EL).

**1.03** Data Set 207-type is a four-phase modem designed to be used either as terminal station equipment for service on four-wire switched or private lines, or as one-half of a regenerative repeater to be used at an intermediate point. Two half regenerator data sets, back-to-back, are required for one four-wire regenerative repeater.

**1.04** The data set provides synchronous serial binary data transmission and reception capability at 2400 bps over telephone facilities available under Type 3004 (Type 4B) Tariffs.

**1.05** The data set can operate over long haul facilities including sections of non-Bell System lines and equipment provided that they meet the requirements of 1.04. When transmission parameters do not meet these requirements, one or more regenerative repeaters can be inserted at intermediate points.

**1.06** A long term error rate of better than one error in $10^5$ bits, when transmitting random data at 2400 bps between two data sets, is the objective on facilities that meet Type 3004 requirements.

**1.07** The customer business machine is required to provide a transmitter timing clock signal on interface lead SCTE and, optionally, a receiver clock signal on interface lead SCRE. Accuracy of the provided clock signal directly affects the data set holdover capability. Holdover is briefly defined as the ability of the data set receiver to hold and maintain its recovered receive clock phase-locked without losing or gaining a cycle with respect to a remote transmit clock for some period of time during which transmission of the data signal is interrupted. When compatible data is restored within the holdover time limit, the receiver clock will be in bit synchronism with the remote transmit clock. If the supplied clock signal is accurate to within $\pm 5.8$ parts in $10^8$, a 30-minute holdover can be realized.

**1.08** The data set can be optionally supplied with an oscillator of an accuracy and stability which will provide a minimum holdover of 30 minutes. This internal oscillator is contained in an oven which maintains the crystal operating temperature between 65 and 75°C. Data set timing circuits are arranged to provide clock signals to external equipment. One Data Set 207-type (A2 or A4) using a 30-minute holdover oscillator can provide high-accuracy clock signals to several other Data Set 207-type (A1 or A3) units. All data sets connected to this oscillator can achieve the greater accuracy and long time holdover requirements as long as the high-accuracy oscillator functions normally.

**1.09** If the customer provides the high-accuracy clock signals, the data set can be provided with a different oscillator having an accuracy of $\pm 1$ part in $10^4$. The data set then relies on the customer-supplied signal to correct the circuit timing to provide the 30-minute holdover.

**1.10** Clock signals supplied by the customer must be at the desired bit rate or lower. Applied clock signals on SCTE and SCRE at 2400 bps limit the data set to this bit rate only. Applied clock signals on SCTE and SCRE at 150 bps provide data set operation for all BIT RATE switch selected speeds. Customer requirements for serial binary data transmission capability at 2400, 1200, 600, 300, and 150 bps rates are provided by Data Set 207-type. The desired transmission rate is selected

by the BIT RATE switch located on the front control panel (Fig. 1). Circuits controlled by the BIT RATE switch condition the transmitter, receiver, and all timing circuits to operate at the rate specified by the switch position. Phase-corrected receive clock signals and an uncorrected clock signal at the selected bit rate are also provided. Terminal data sets must operate at the same transmission rate in each direction of transmission. Regenerator data sets operate at 2400 bps regardless of the terminal data rate. Receiver timing may be controlled by the data set internal oscillator or by an external timing source, but an external bit rate clock must always be applied to the transmitter through interface lead SCTE. The transitions of Send Data (SD) must coincide with either positive or negative transitions of the applied clock on SCTE. Either condition is provided for by a strap option.

**1.11** All data sets are provided with both receive signal sensor circuits and an alarm circuit for loss of transmitter output signals for 0.2 second. Only Data Sets 207-type (A1, A2, B1, B2, C1, C2) are provided with delayed alarms to indicate:

(1) Loss of received carrier for two seconds or longer

(2) Loss of received data transitions for five seconds or longer

(3) Loss of Send Data transitions for five seconds or longer

These delayed alarms are not provided in Data Sets 207-type (A3, A4, B3, B4, C3, C4) which are the data sets used as regenerators.

**1.12** The receive signal sensor circuits made up of guard band and coherent detector circuits monitor the telephone line for compatible four-phase data signals and are provided with both terminal data sets and regenerator data sets. A guard band detector is provided in the receiver which distinguishes between four-phase line signals and noncompatible signals such as speech, telephone signaling, and noise. Receiver timing corrections from the line signal are inhibited when a four-phase signal is not present on the telephone line. A coherency detector is provided in the receiver to determine when the receiver is receiving coherent crossings and is in bit synchronism with the distant station transmitter. The status of this detector determines the timing recovery made. The sensor circuits in a half regenerator bypass noncompatible signals and effectively keep the data set off the telephone line. At both terminal and regenerator stations, if line signals with compatible data drop out and return within the holdover capability of the internal oscillator or external timing source, the receiver clock will be in synchronization (not gain or lose a "bit") with the return of the compatible line signal.

**1.13** Remote testing of the data set operating either as a terminal set or half regenerator is provided using a 904-type Data Test Center.

## 2. DESCRIPTION

### PHYSICAL DESCRIPTION

**2.01** Data Set 207-type is available in several configurations. Each configuration is designed to serve a definite requirement. The following paragraphs show the similarity and identify the differences.

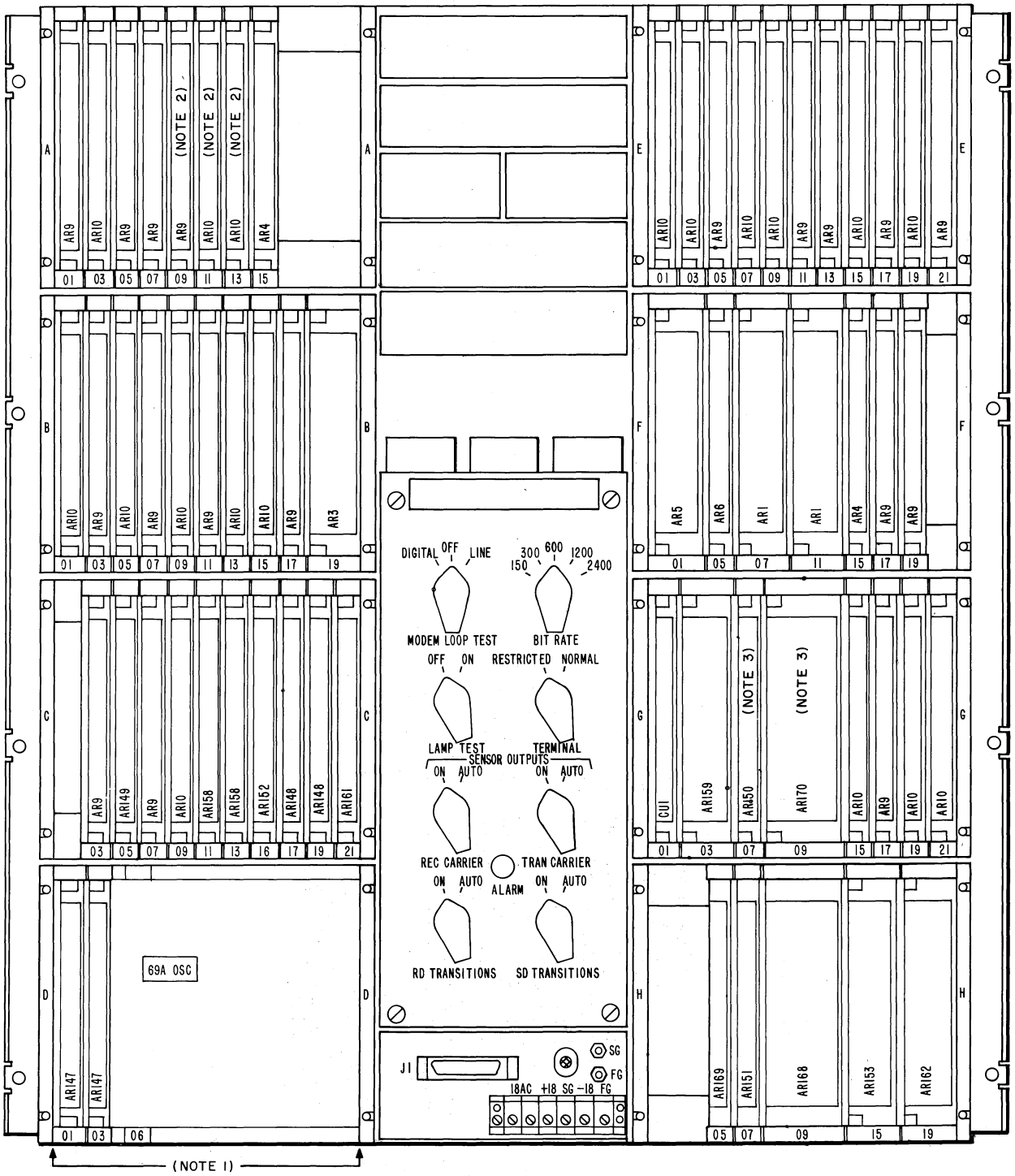
**2.02** Data Set 207A-type is the basic data set without power supply or mounting facilities. Data Set 207A-types are component parts of both Data Set 207B-types and Data Set 207C-types.

**2.03** Data Set 207A-type includes the following generation: (1) 207A1; (2) 207A2; (3) 207A3; and (4) 207A4. Each generation of the data set includes specific functions and has certain requirements. The following chart briefly defines the basic differences of the data set generation.

| NOMENCLATURE | OPERATION | TIMING SOURCE | DELAYED ALARMS |
|---|---|---|---|
| 207A1 | Terminal Set | Customer-Supplied | Yes |
| 207A2 | Terminal Set | Self-Timed, 30-Minute Holdover | Yes |
| 207A3 | Half Regenerator | Customer-Supplied | No |
| 207A4 | Half Regenerator | Self-Timed, 30-Minute Holdover | No |

**2.04** Fig. 1 illustrates a typical Data Set 207A-type. The data set is 24 inches high, 20.2 inches wide, and 9.4 inches deep.

**2.05** Data Set 207B-type consists of Data Set 207A-type equipped with a 32B1 Power Unit to supply operating voltages, and a mounting frame




NOTES:

1. DATA SETS 207A1 AND 207A3 USE ONLY AN AR160 (230.4KHZ OSCILLATOR) IN SLOT LOCATION D06. DATA SETS 207A2 AND 207A4 REQUIRE THE TWO AR147 BOARDS AND THE 69A OSCILLATOR AS SHOWN.
2. ONLY DATA SETS 207A1 AND 207A2 ARE PROVIDED WITH DELAYED ALARM CIRCUITS.
3. ONLY DATA SETS 207A3 AND 207A4 ARE PROVIDED WITH BYPASS AND TRANSFER CIRCUITS.

**Fig. 1—Typical Data Set 207A-Type**

to adapt both the data set and power unit to a standard 23-inch relay rack.

**2.06** The 32B1 Power Unit (Fig. 2) is provided with a ten-foot 120 vac power cord. If operation at 230 vac is required, the power cord must be replaced with one appropriate for 230 vac service. Voltage input and output characteristics are briefly tabulated in the following chart.

**2.07** Data Set 207B-type is supplied mounted on a bracket that adapts to a 23-inch relay rack. The power unit for Data Set 207B-type is mounted below the data set circuitry. Short individual wires connect the power unit output voltages to the data set voltage input through terminal strips on each unit. The connecting wires span a distance of approximately four inches between terminal strips.

| INPUT VOLTAGE | LINE FREQUENCY* | OUTPUT VOLTAGE | CURRENT LIMITS |
|---|---|---|---|
| 120 (+10%) (−20%) vac<br>or<br>230 (±10%) vac | 47.5 to<br>63.0 Hz | +18.0 (±0.9) vdc<br>−18.0 (±0.9) vdc<br>18.0 vac | 2.0 to 3.8 amps<br>0.4 to 1.6 amps<br>1.5 amps |

* Maximum limits


**Fig. 2—32B1 Power Unit, Front View**

**2.08** Data Set 207B-type includes the following generation: (1) 207B1; (2) 207B2; (3) 207B3; and (4) 207B4. Each generation of the data set includes specific functions and has certain requirements. The following chart briefly defines the basic differences of the data set generation. Each data set is provided with a 32B1 Power Unit.

| NOMENCLATURE | OPERATION | TIMING SOURCE | DELAYED ALARMS | RFI** SHIELD |
|---|---|---|---|---|
| 207B1 | Terminator | Customer-Supplied | Yes | No |
| 207B2 | Terminator | Self-Timed, 30-Minute Holdover | Yes | No |
| 207B3 | Half Regenerator | Customer-Supplied | No | No |
| 207B4 | Half Regenerator | Self-Timed, 30-Minute Holdover | No | No |

** Radio Frequency Interference

**2.09** Fig. 3 illustrates a typical Data Set 207B-type mounted in a relay rack. Fig. 4 and Fig. 5 show the rear view of a typical Data Set 207B-type with and without the back cover, respectively. Dimensions of the Data Set 207B-type are 38 inches high by 23 inches wide by 10.5 inches deep. Switch positions and functions are described in Part 3—OPERATION.

**2.10** The Data Set 207C-type consists of Radio Frequency Interference (RFI) shield which is designed to be mounted in a standard 23-inch relay rack. Data Set 207C-type consists of Data Set 207A-type and a 32A1 Power Unit all mounted within the RFI shield with the power unit mounted over the data set circuits.

**2.11** The 32A1 Power Unit is identical to the 32B1 Power Unit except that a power cord for the ac input is not provided and wire mesh gaskets are incorporated in the 32A1 unit to mate with the RFI shield. The tabulation in 2.06 for the 32B1 Power Unit also pertains to the 32A1 Power Unit.

**2.12** Data Set 207C-type includes the following generation: (1) 207C1; (2) 207C2; (3) 207C3; and (4) 207C4. Each generation of the data set includes specific functions and has certain requirements. The following chart briefly defines the basic differences of the data set generation. Each data set is provided with a 32A1 Power Unit.

| NOMENCLATURE | OPERATION | TIMING SOURCE | DELAYED ALARMS | RFI** SHIELD |
|---|---|---|---|---|
| 207C1 | Terminator | Customer-Supplied | Yes | Yes |
| 207C2 | Terminator | Self-Timed, 30-Minute Holdover | Yes | Yes |
| 207C3 | Half Regenerator | Customer-Supplied | No | Yes |
| 207C4 | Half Regenerator | Self-Timed, 30-Minute Holdover | No | Yes |

** Radio Frequency Interference

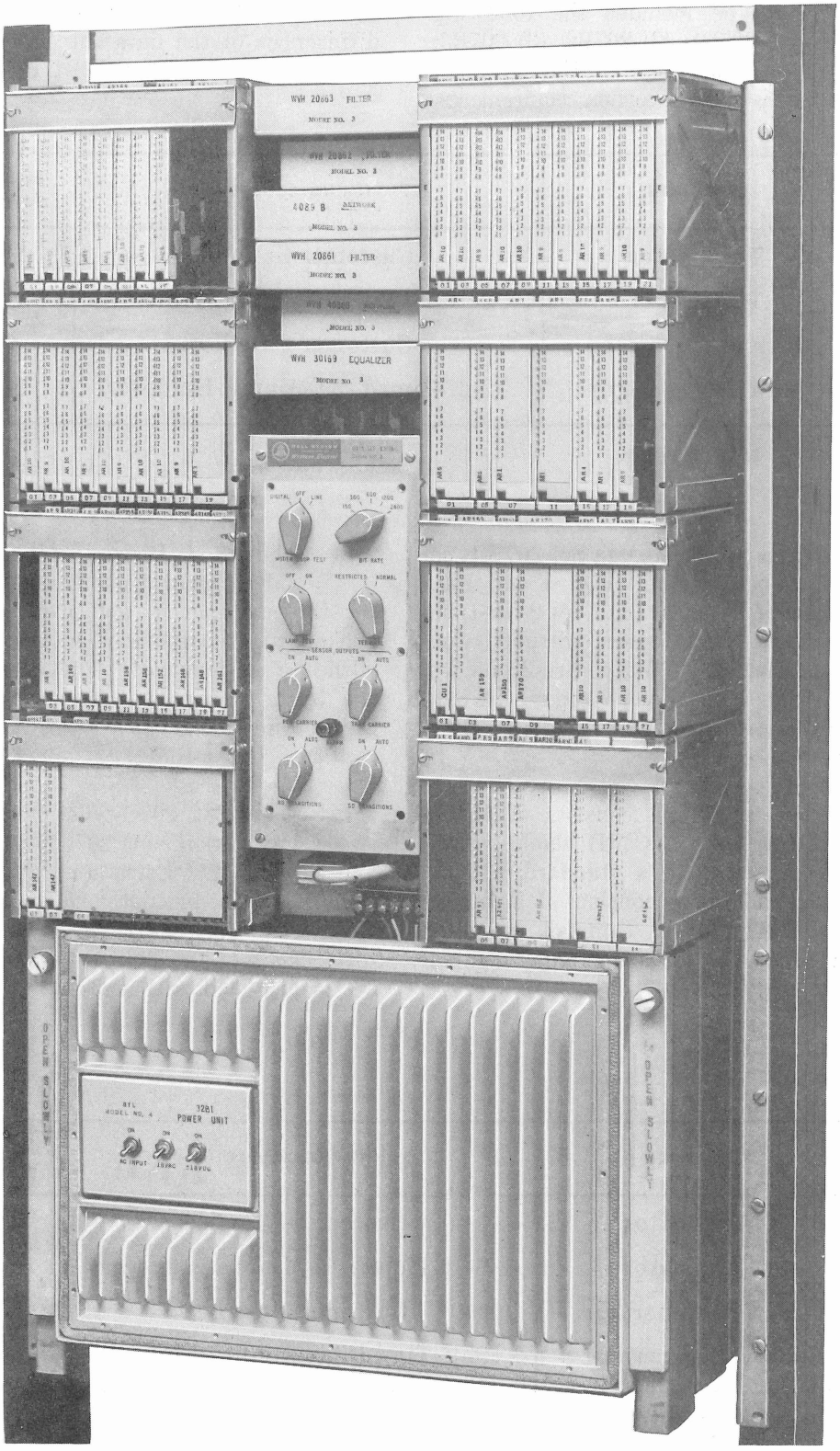



Fig. 3—Data Set 207B-Type, Front View

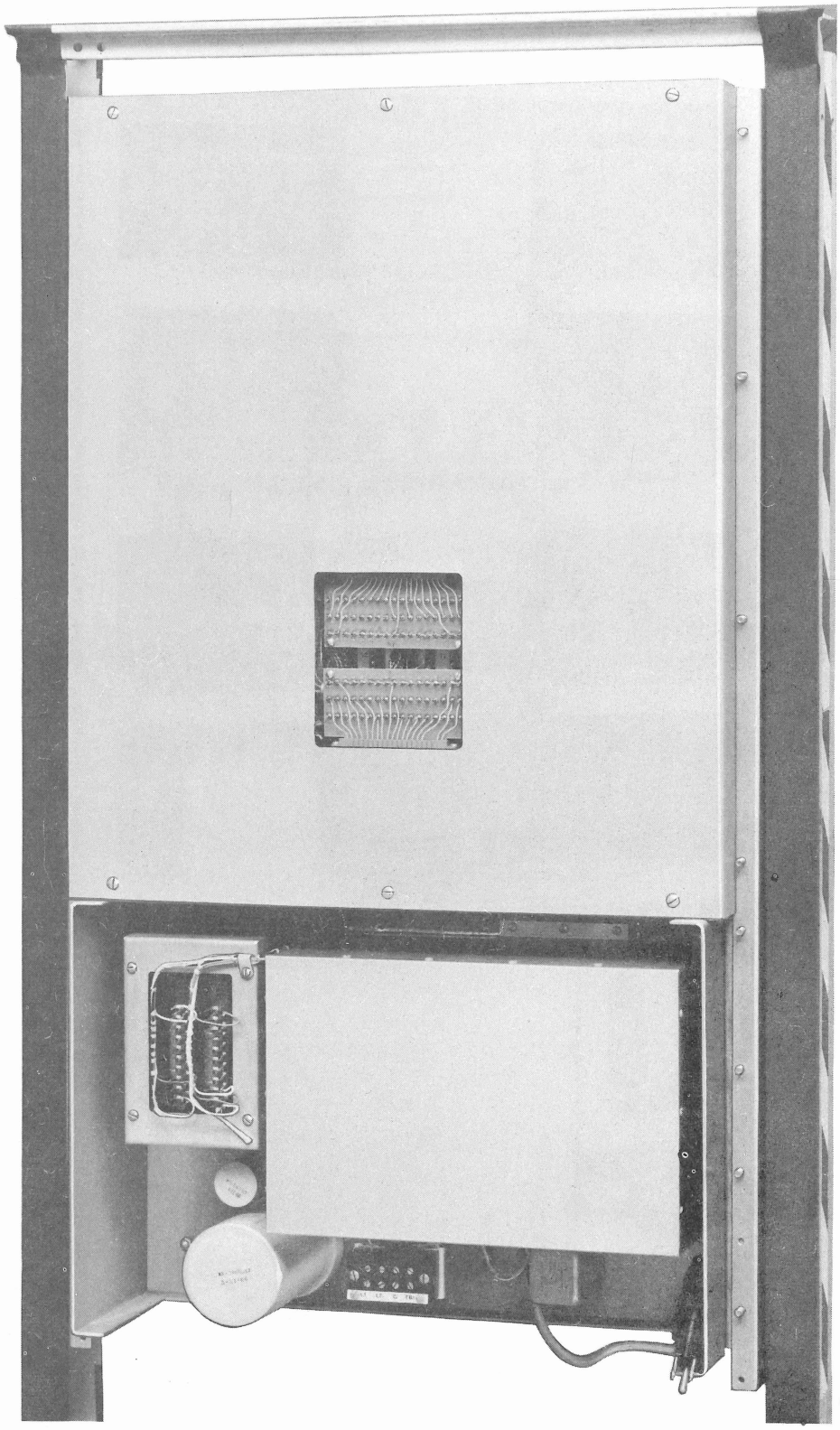


Fig. 4—Data Set 207B-Type, Rear View With Cover

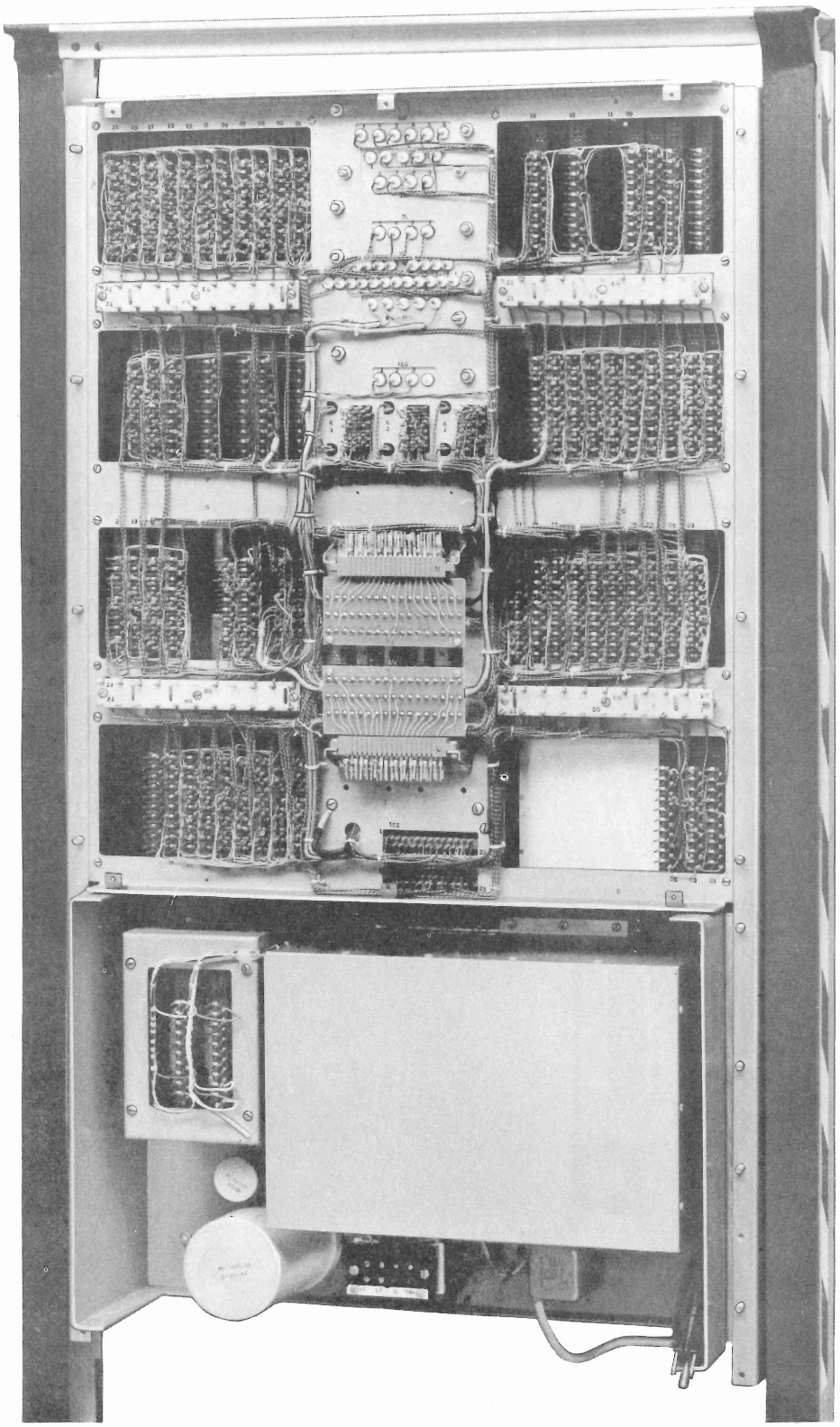


Fig. 5—Data Set 207B-Type, Rear View Without Cover

**2.13** Fig. 6 illustrates a typical Data Set 207C-type mounted in a RFI shield and set in a relay rack. Fig. 7 illustrates a typical Data Set 207C-type mounted in a relay rack without the front panel. Fig. 8 illustrates a rear view of a typical Data Set 207C-type with the access panels removed. Dimensions of the Data Set 207C-type including the RFI shield are 40 inches high by 23 inches wide by 13 inches deep. Switch positions and functions are described in Part 3—OPERATION.

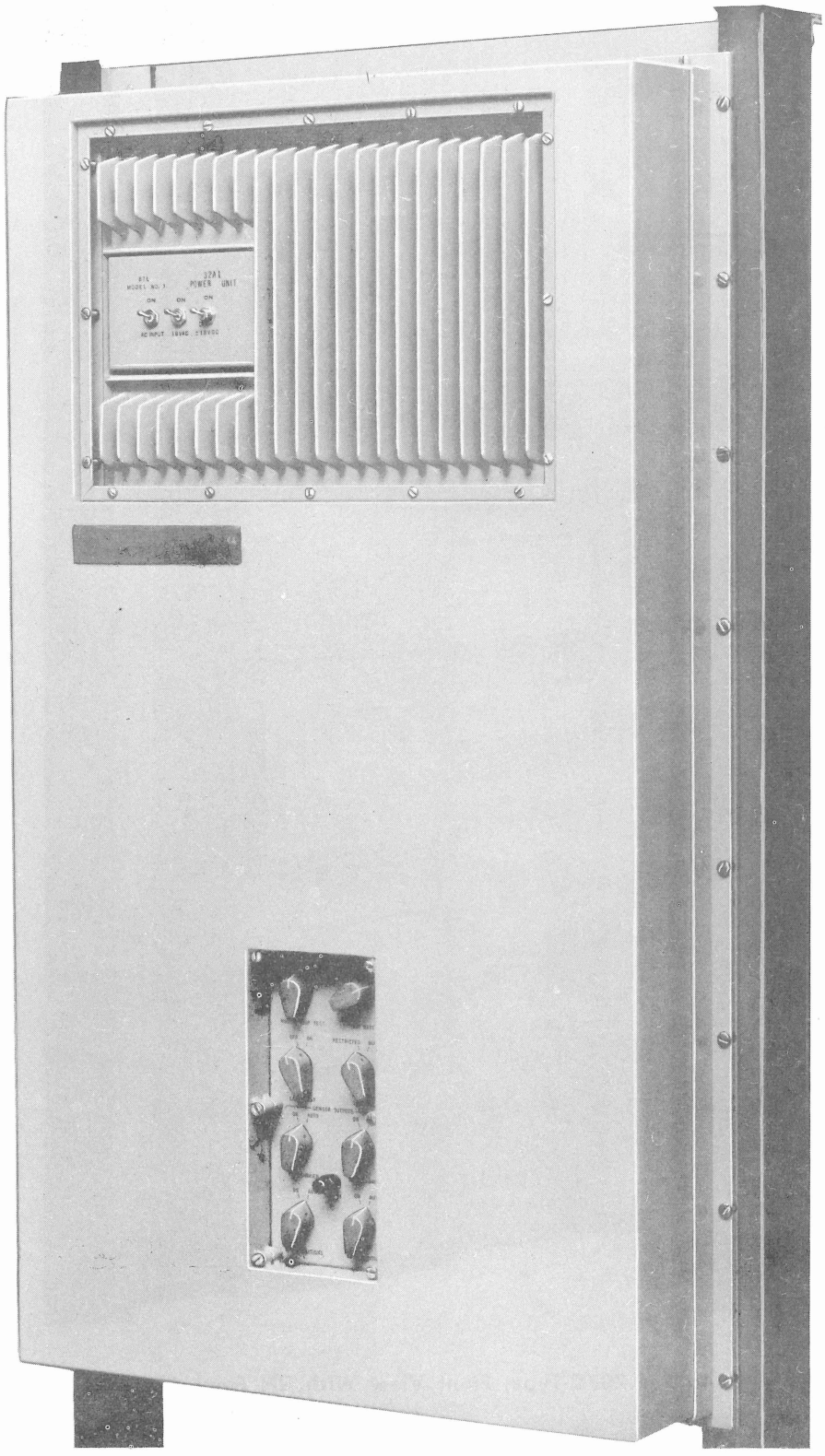


**Fig. 6—Data Set 207C-Type, Front View With RFI Front Cover in Place**

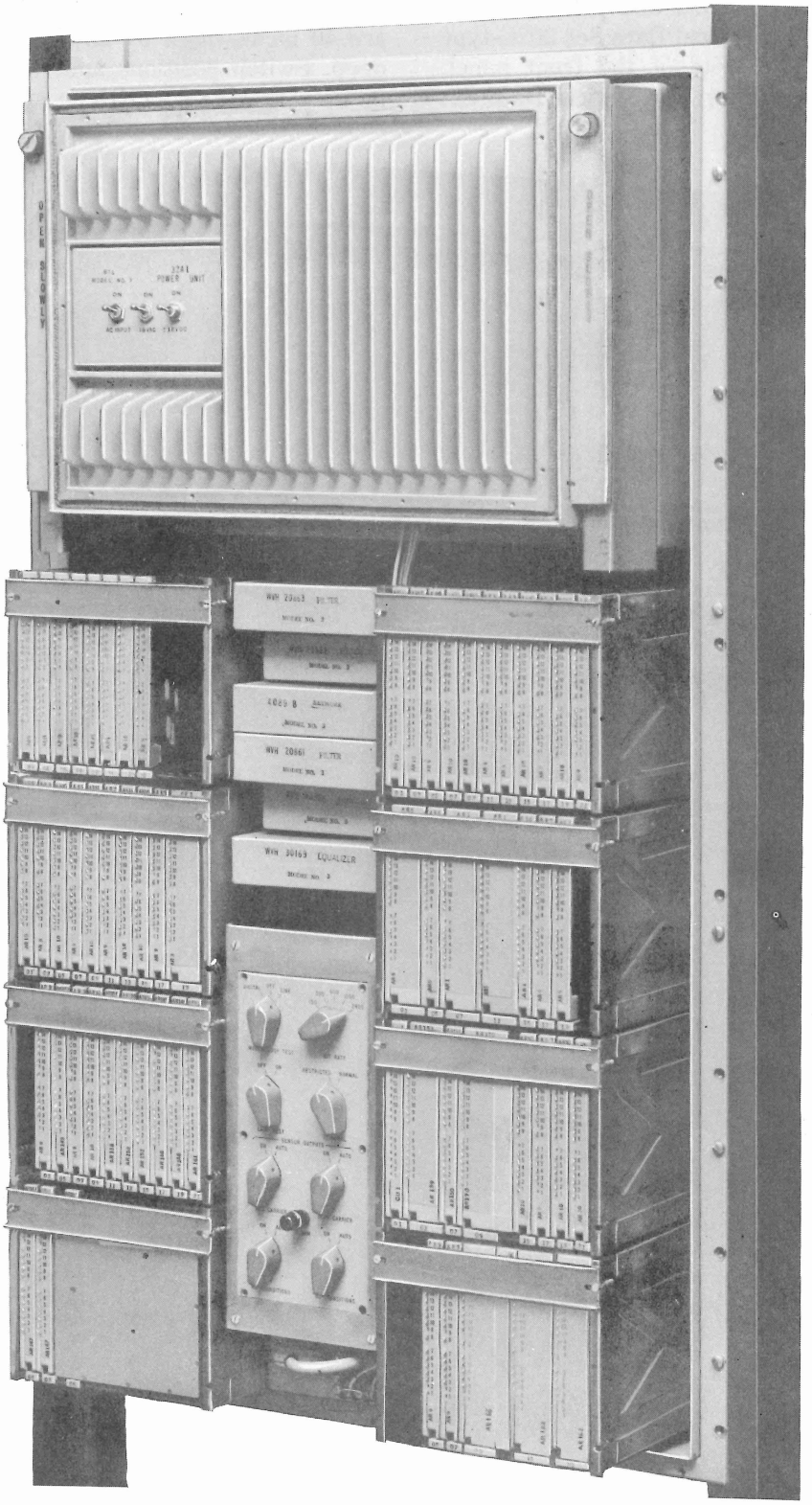



Fig. 7—Data Set 207C-Type, Front View With RFI Front Cover Removed

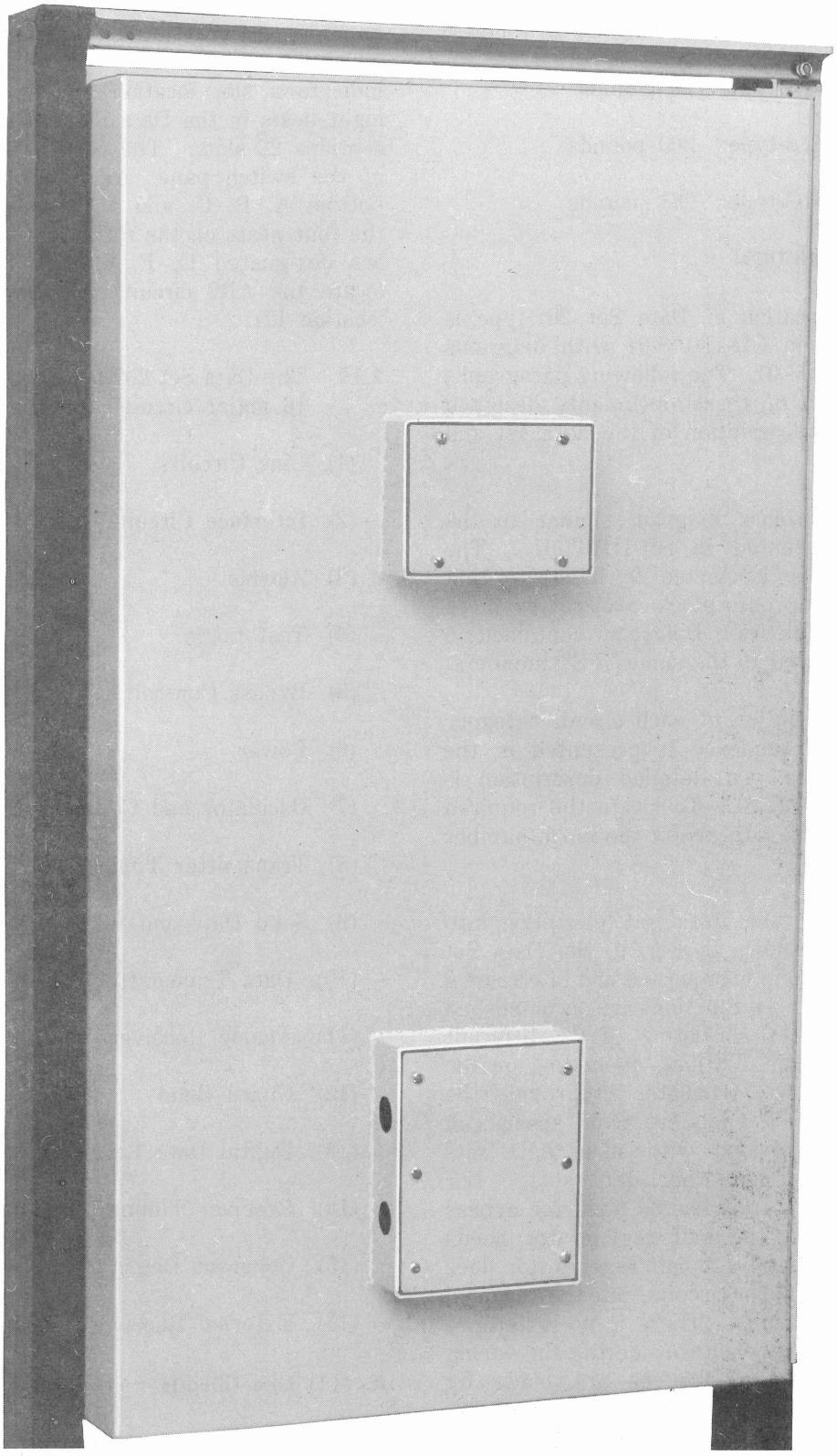


Fig. 8—Data Set 207C-Type, Rear View

**2.14** The weights of the data sets are as follows:

(a) Data Set 207A-type: 90 pounds

(b) Data Set 207B-type: 203 pounds

(c) Data Set 207C-type: 271 pounds

## FUNCTIONAL DESCRIPTION

**2.15** Detailed operation of Data Set 207-type is documented in CD-1D108-01 with diagrams provided in SD-1D108-01. The following paragraphs are a simplification of these documents designed to present a short description of the data set and its capability.

**2.16** Fig. 9 is a block diagram similar to the diagram presented in SD-1D108-01. The functional blocks are connected to illustrate that signals used within one block are received or delivered to other blocks. Diagrams contained in SD-1D108-01 are keyed to the same "FS" numbers.

**2.17** A brief description of each circuit category in numerical sequence is presented in the following paragraphs. A detailed description is presented in CD-1D108-01. To locate the required circuit category in the CD, prefix the block number with "FS".

**2.18** By grouping the data set circuitry into functions as shown in Fig. 9, the Data Set 207-type consists of 16 interconnected and interrelated functional groups. These functions are accomplished using 61 circuit packs consisting of 23 different types of specialized circuits and, depending on the option required, a 69A Oscillator to provide the electronic functions of the data set. Some specialized circuit packs are provided with some data sets and will be missing for other data sets. For example, a terminal station has no need for bypass control circuitry, but the half regenerator needs the circuitry. Conversely, a half regenerator does not use the delayed alarm circuits, but the terminal station uses these circuits. There is no difference between data set types when considering the wiring harness alone. The differences are made by incorporating some circuit packs and omitting others. It is possible to make a terminal data set into a half regenerator, or the reverse, by the proper selection of required circuit packs in the appropriate slot positions. The circuit pack numbers and reference location numbers on the data set are shown in Tables A and B. The equipment location numbers are correlated by letters which designate which "nest" uses the circuitry and numbers which indicate a slot location in the nest. There are eight nests in the Data Set 207-type and each nest contains 22 slots. The four nests on the left side of the switch panel are designated, from top to bottom, A, B, C, and D, respectively. Similarly, the four nests on the right side of the switch panel are designated E, F, G, and H. It is easy to locate the AR9 circuit pack in E17 (nest E, slot location 17).

**2.19** The Data Set 207-type contains the following 16 major circuit categories:

(1) Line Circuits

(2) Interface Circuits

(3) Alarms

(4) Test Logic

(5) Bypass Control

(6) Power

(7) Oscillator and Common Countdown

(8) Transmitter Timing

(9) Send Data and Idle Code Logic

(10) Data Transmitter

(11) Analog Receiver

(12) Guard Band

(13) Digital Data Receiver

(14) Receiver Timing

(15) Coherent Detector

(16) External Receiver Timing

### A. (1) Line Circuits

**2.20** The line circuits interface between data set circuitry and the four-wire telephone line for both terminator and regenerator modes of operation. Line circuits share terminals on adapter board A1 with the (2) Interface Circuits. The telephone line pairs are soldered to the appropriate

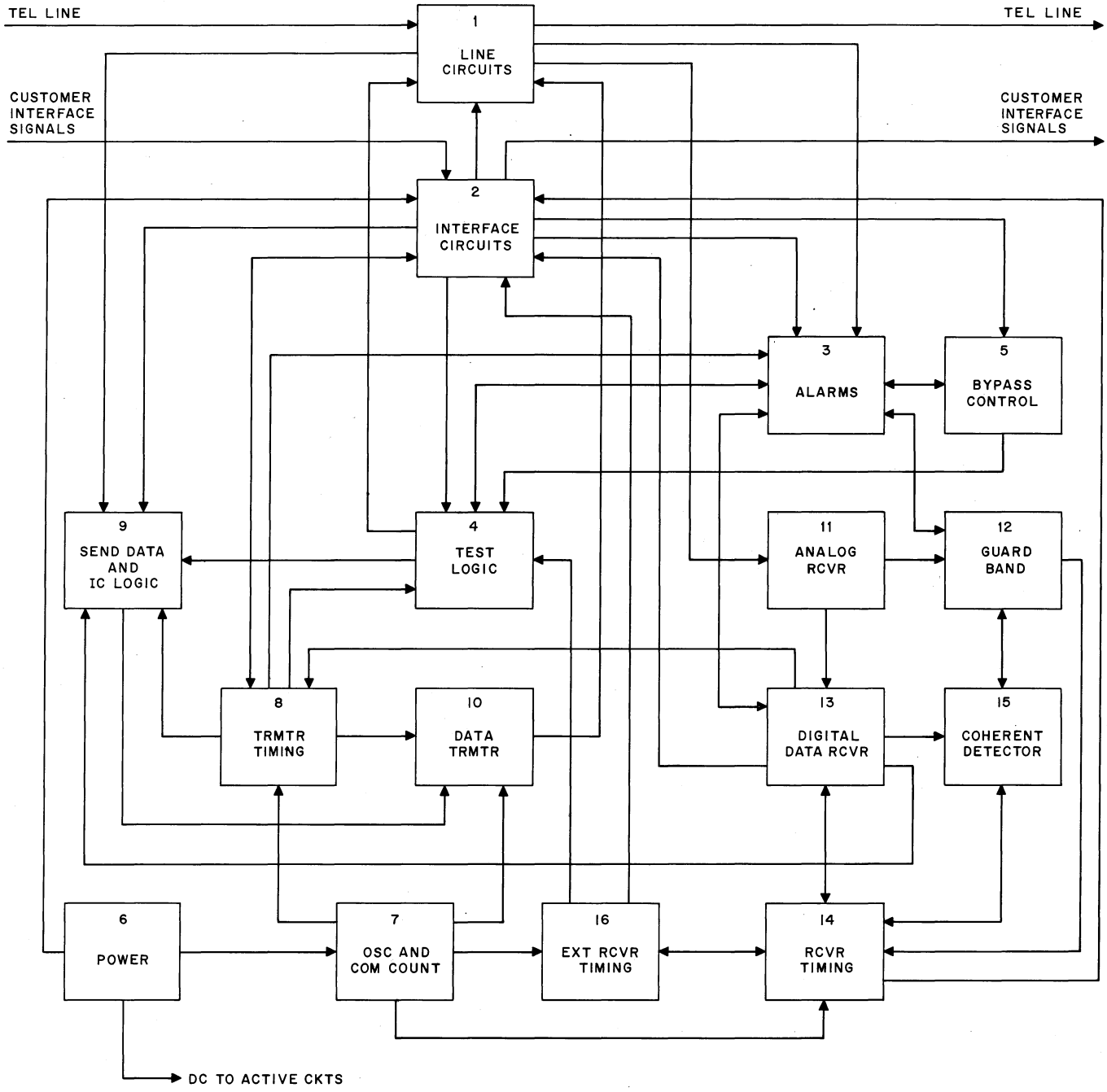



**Fig. 9—Data Set 207-Type, Block Diagram**

**TABLE A**

**CIRCUIT PACKS USED IN ALL DATA SETS 207-TYPE**

| FUNCTIONAL DESCRIPTION | CIRCUIT PACK CODE | USED IN LOCATIONS |
|---|---|---|
| Demodulator | AR1 | F07, F11 |
| Transmitter Output | AR3 | B19 |
| Monopulser | AR4 | A15, F15 |
| Automatic Gain Control I | AR5 | F01 |
| Automatic Gain Control II | AR6 | F05 |
| NOR Gate | AR9 | A01, A05, A07, B03, B07, B11, B17, C03, C07, E05, E11, E13, E17, E21, F17, F19, G17 |
| Complementary Flip-Flop | AR10 | AR3, B01, B05, B09, B13, B15, C09, E01, E03, E07, E09, E15, E19, G15, G19, G21 |
| Mil. Std. Interface | AR148 | C17, C19 |
| Shift Register | AR149 | C05 |
| Comparator | AR151 | H07 |
| Unipolar and Bipolar, Mil. Std | AR152 | C15 |
| Amplifier-Rectifier | AR153 | H15 |
| Six-Volt Interface | AR158 | C11, C13 |
| Line Circuit | AR159 | G03 |
| Strap Circuit | AR161 | C21 |
| Guard Band I | AR162 | H19 |
| Guard Band II | AR168 | H09 |
| Timer | AR169 | H05 |
| Terminator-Regenerator | CU 1 | G01 |

terminals of A1 and then connected to the data set circuitry through the mating connector of A1. The ALARM lamp, mounted on the switch panel, is included with the line circuits.

**Terminator Mode**

**2.21** Requirements for the normal terminator mode of operation are:

(a) CU 1 circuit pack in G01 arranged as TERMINATOR

(b) An AR9 circuit pack in location A07

(c) AR10 circuit packs in locations A11 and A13. The AR9 and AR10 circuit packs provide delayed alarms for a terminator as described in (3) Alarms. Components in the line circuits assist in both local and remote testing.

**Regenerate Mode**

**2.22** Requirements for the normal regenerate mode of operation are:

(1) CU 1 circuit pack in G01 arranged as REGENERATOR

(2) AR150 circuit pack in location G07

(3) AR170 circuit pack in location G09

Circuits in the AR150 (Bypass) and AR170 (Transfer) provide a "sniffer" amplifier with the required bypass relay contacts and components to place the data set on-line (when compatible data is received), or off-line (when detecting noncompatible signals). The "sniffer" amplifier bridges the receive T, R pair continuously, allowing the Receive Signal Sensor circuits to determine the signal compatibility and operate the bypass relays accordingly.

**TABLE B**

**CIRCUIT PACKS APPLICABLE TO SPECIFIC DATA SETS 207-TYPE**

| REQUIRED FOR | FUNCTIONAL DESIGNATION | CIRCUIT PACK CODE | SUPPLIED IN DATA SET LOCATION | | | |
|---|---|---|---|---|---|---|
| | | | 207A1, B1, C1 | 207A2, B2, C2 | 207A3, B3, C3 | 207A4, B4, C4 |
| Terminal Data Set | NOR Gate | AR9 | A09 | A09 | | |
| | Complementary Flip-Flop | AR10 | A11, A13 | A11, A13 | | |
| Regenerative Data Set | Bypass | AR150 | | | G07 | G07 |
| | Transfer | AR170 | | | G09 | G09 |
| 30-Minute Clock Holdover | 5.5 MHz Counter | AR147 | D01, D03 | | | D10, D03 |
| | 69A Oscillator | — | | D06 | | D06 |
| External Clock Supplied (For 30-Minute Holdover) | 230.4 KHz Oscillator | AR160 | D06 | | D06 | |

### B. (2) Interface Circuits

**2.23** The interface circuits center about adapter boards A1 and A2. Soldered connections to the boards provide continuity between the data set and (a) the customer business machine, (b) a companion modem (when used as a half regenerator), or (c) gateway office circuits, when applicable. Interface signals that can determine the operational capability of the data set are also connected through the test jack and plug. The test jack and plug, located beneath the switch panel and above the input voltage terminal strip, function only for local testing and continuity checks. Disconnection of the test jack and plug will not interrupt the external clock output (SCB) if the data set to be tested is supplying clock signals to other equipment.

**2.24** The interface circuits contain both the drivers and the terminators required for the clock and data leads. Relay contacts used for loop-back testing of the clock and data leads are an integral part of the interface circuits. Also contained in the interface circuits are the BIT RATE switch which determines the clock speed selections, and the option straps which are provided by circuit pack AR161 in location C21. Option strapping is detailed in Data Set 207-Type, Transmitter-Receiver, Installation Instructions (Section 592-020-200).

### C. (3) Alarms

**2.25** The alarm logic circuits monitor the data set circuitry for conditions which will initiate the generation, timing, and control of the alarms listed below [the last four are delayed alarms used in Data Set 207-type (A1, A2, B1, B2, C1, C2) only].

| FUNCTION | MNEMONIC SYMBOLS |
|---|---|
| Loss of receive carrier-1; -2 | RSS1; RSS2 |
| Loss of receive carrier, delayed | RSSD |
| Loss of transmit carrier | TSS |
| Loss of Receive Data transitions | RDTX |
| Loss of Send Data transitions | SDTX |

**2.26** When the alarm logic circuits operate, the condition is presented as a visual indication by the illumination of the ALARM lamp on the switch panel. This alarm indication is available only when the data set is used as terminal equipment and the alarm sensor switches are set to AUTO. The delayed alarms (i. e., RSSD, RDTX, and SDTX) are not provided unless the data set is supplied with circuit packs required for option Z. Option Z requires circuit packs in locations A09, A11, and A13.

### D. (4) Test Logic

**2.27** The test logic circuits contain several functions. The MODEM LOOP TEST switch conditions the data set for either looping the receiver to the transmitter on the line side and terminating the telephone line pairs into 600 ohms (LINE switch position), or looping the transmitter to the receiver on the digital data side (DIGITAL switch position). Depending upon the location and/or operation of the data set, these switch positions constitute local test and remote test. Detailed information for using the MODEM LOOP TEST switch is contained in Data Set 207-Type, Transmitter-Receiver, Installation Instructions (Section 592-020-200). In general, the test logic circuits provide control of the remote test sequence.

**2.28** The driver that illuminates the ALARM lamp is contained in the test logic circuits. The operation of the driver is controlled by signals developed in the alarm logic circuits. A LAMP TEST switch on the switch panel provides a substitute signal to test the lamp operation only. If the data set is operating as a half regenerator, the alarm logic circuits are inhibited, but the ALARM lamp will be illuminated by a power unit failure of either ±18 vdc or –18 vdc. Voltage necessary to illuminate the lamp is externally supplied through the interface connections from the 48 vdc central office battery.

**2.29** The test logic circuits are used to sequence the data set during remote testing by a Data Test Center. By using the controlled sequence, the Data Test Center can determine the capability of important data set circuits and the overall operational performance of the data set. These circuits also provide control of the transmitted Idle Code (IC).

### E. (5) Bypass Control

**2.30** The bypass control circuits are used only when the data set is operating as a half regenerator. Bypass control circuits consist of logic circuits, relays, and relay contacts that will remove the data set from the telephone line when noncompatible signals are detected and return the data set to the line when compatible data is received.

### F. (6) Power

**2.31** The circuits contained within the power unit regulate the supplied +18 vdc and –18 vdc required by the active data set circuits. The power unit also provides a Frame Ground (FG) to the interface circuits and the required 18 vac for the oscillator oven. Power unit requirements are listed in 2.06.

### G. (7) Oscillator and Common Countdown

**2.32** The oscillator and common countdown circuits generate the basic timing square waves used in both transmitter and receiver circuits. The oscillator is determined by the data set requirements. An oscillator, contained in circuit pack AR160, provides a 230.4 kHz square wave with an accuracy of 1 part in $10^4$. Externally provided timing is required. An optional oscillator, designated as 69A, operates at 5,529,600 Hz with an accuracy of 5.8 parts in $10^8$. The oscillator signal is processed by a countdown chain which is provided with a 69A Oscillator to derive a highly accurate 230.4 kHz to drive the remaining countdown circuits and provide a 30-minute holdover capability.

### H. (8) Transmitter Timing

**2.33** The transmitter timing circuits generate the timing waveform chains used in the (3) Alarm logic, (9) Send Data and Idle Code, and (10) Data Transmitter Circuits. The binary countdown chain of the transmitter timing circuits phase-locks to an external timing source through the interface SCTE lead. An input must always be supplied to SCTE. Basically, the functions of the transmitter timing circuits are as follows:

(a) Generate square-wave input signals to phase-modulate channel counters

(b) Generate the required pulse train to sample input data (SD)

(c) Generate accurate square-wave signals for encoding purposes

(d) Generate a square-wave input signal for the interface driver circuit (for DTI which is used for testing purposes)

(e) Generate square-wave input signals to operate the pulse modulators

(f) Generate six pulse trains to operate the phase logic channel counter transfer gates and perform other "set" or "clear" functions

(g) Generate a 2400 Hz square wave to operate the scrambler-descrambler shift registers.

(h) Generate square waves for generating the Idle Code at the selected bit rate

(i) Generate pulse trains to operate the transition detector in the test logic circuits

(j) Generate square waves to operate the alarm logic timing chains.

### I. (9) Send Data and Idle Code Logic

**2.34** The Send Data circuits generate and control the binary data signals applied to the (10) Data Transmitter. Together, the Send Data and Idle Code Logic circuits provide the following functions:

(a) Allow customer business machine Send Data signals to be transmitted

(b) Generate the appropriate Send Data sequences used when the data set is in the remote test mode

(c) Generate an Idle Code at the selected bit rate

(d) Scramble binary Send Data to provide data "crossings" on a dibit basis.

**2.35** The TERMINAL switch located on the switch panel is effective only at speeds of 1200 bps and lower. In the NORMAL position, the transmitted dibits are encoded such that the B bit is equal to the A bit. In the RESTRICTED position, the B bit is clamped at 0 to improve error performance over degraded facilities. The scrambler circuit is used at terminal data sets. The scrambler provides crossings on a dibit basis for either a dotting code or steady "1's" on SD. At a regenerator station, if the equipment consists of two Data Sets 207-type (B3, B4, C3, C4), the scrambler and descrambler circuits are strapped out and not used. If the regenerator equipment uses only one Data Set 207-type, the scrambler and descrambler are required.

### J. (10) Data Transmitter

**2.36** The data transmitter circuits encode serial binary data as a phase-modulated band-limited signal suitable for transmission over voiceband facilities.

### K. (11) Analog Receiver

**2.37** The analog receiver circuits (a) amplify the received phase-modulated band-limited signal to a fixed level, and (b) convert the receive line signal into two parallel signals which constitute demodulated data.

### L. (12) Guard Band

**2.38** The guard band circuits detect the presence of a compatible received line signal. The circuits reject all noncompatible signals such as voice, single-frequency tones, multifrequency signaling tones, and noise. The guard band circuits, together with Carrier ON-OFF circuits contained in the (11) Analog Receiver and (15) Coherent Detector, make the Receive Signal Sensor circuits which operate only when a compatible signal is received and the receiver is in-sync. During the time the data set receives a noncompatible signal, guard band circuits inhibit the receiver timing to prevent erroneous clock corrections. The receiver clock will remain synchronized for the time period limited by the accuracy of the clocks used at both the transmitter and receiver.

### M. (13) Digital Data Receiver

**2.39** The digital data receiver circuits perform the following functions:

(a) Convert demodulated data to standard logic signals

(b) Generate axis-crossing pulses for operating the timing recovery circuits

(c) Descramble and generate serial binary data for customer business machine use

**2.40** When the Receive Signal Sensor circuits remove the data set from the telephone line through detection of noncompatible signals, the

Receive Data (RD) lead may be clamped to either a Mark Hold or Space Hold condition, depending upon a strap option.

### N. (14) Receiver Timing

**2.41** The receiver timing circuits recover synchronized timing signals for the following functions:

(a) Sampling

(b) Regeneration of Receive Data

(c) Parallel-to-serial conversion of the Receive Data

(d) Use in the (15) Coherent Detector

### O. (15) Coherent Detector

**2.42** The coherent detector circuits generate a logic signal indicating that compatible signals are detected by circuits in the (12) Guard Band and that the recovered clock from (14) Receiver Timing is synchronized to the incoming compatible data signal-crossing pulses.

### P. (16) External Receiver Timing

**2.43** The external receiver timing circuits allow the (14) Receiver Timing to be frequency-locked by either the data set internal oscillator (option X) or by an externally supplied clock signal applied to interface lead SCRE (option Y). External receiver timing circuits also provide uncorrected bit rate clock signals on the interface SCA and SCB clock circuits.

## GROUNDING

**2.44** The Data Set 207-type provides the following two grounds: (a) Frame Ground (FG) is common to both chassis ground and the ac power third-wire ground, and (b) Signal Ground (SG) is used as a reference for all data, timing, and control signals. Signal Ground is connected to Frame Ground only when the SG1 terminal is strapped to the FG1 terminal in the data set. These terminals, located above and to the right of the input voltage terminal strip (Fig. 1), must not be strapped when the customer requires isolation of Frame Ground and Signal Ground at the data set.

## 3. OPERATION

**3.01** Operating voltages for the data set are supplied by an associated power unit through an output voltage terminal strip on the power unit chassis. A connection for each output voltage is individually wired to a similar input voltage terminal strip on the data set. Wire lengths vary between locating the power unit below the data set circuitry (as in the 207B-type equipment) or above the data set circuitry (as in the 207C-type equipment). The wiring harness used for Data Set 207C-type equipment must be positioned in a manner so not to interfere with the surface bonding requirements of the RFI shield. The ac input cord for the 32A1 Power Unit used with Data Set 207C-type must be supplied through a conduit which enters on the right side of the power unit access box as viewed from the rear. No ac input power cord is provided with the 32A1 Power Unit.

**3.02** The power unit is provided with three front panel switches that protect and control the power unit functions. Each switch is a circuit breaker type that will interrupt the connected supply if the load requirement is in excess of the operational capacity. The function of each switch is listed as follows:

| SWITCH DESIGNATION | FUNCTION |
|---|---|
| AC INPUT | ON-OFF switch provides input voltage protection. |
| 18 VAC | ON-OFF switch provides protection for the 18 vac output. |
| ±18 VDC | ON-OFF switch provides protection for both +18 vdc and −18 vdc outputs. |

**3.03** The four-wire telephone line is connected to the data set circuits through adapter board A1. The adapter board is accessible at the rear of the data set. Telephone lines are soldered to terminals on the adapter board which is mated and secured to the appropriate connectors. Customer business machine connections are soldered to appropriate terminals on the adapter boards A1 and A2. Connections for Data Set 207C-type equipment are brought through a conduit into the left side of the rear-mounted data set access box as viewed from the rear.

**3.04** Remaining interface connections, when required, are also soldered to the adapter board terminals to provide convenience for removing and replacing data set circuits with a minimum of time and effort.

**3.05** The transmitter output level may be adjusted between 0 and –18.0 dbm in 1.5 db increments using combinations of four loss pads contained on circuit pack AR159 in location G03 (Fig. 1).

**3.06** The receiver circuits contain an AGC circuit with a 30 db dynamic range and a maximum sensitivity of –34 dbm. Attenuation pads at the receiver input may be strapped to reduce the sensitivity. Loss pads providing 0, 5, 10, and 15 db attenuation may be inserted by selecting the proper strap conditions on circuit pack AR4 in location F01.

**3.07** Data set operation as either terminal or half regenerator equipment depends upon which end of the double-ended board, on circuit pack CU 1 in location G01, mates with the data set connector.

**3.08** Data Set 207-type can provide either polar, ±6 volts, or four-volt unipolar signals (on the SD and RD leads only) to the customer business machine by selecting the proper strapping on circuit pack AR152 in location C15.

**3.09** Data Set 207-type contains a scrambler circuit on the Send Data interface lead and a descrambler circuit on the Receive Data interface lead. The scrambler circuit encodes the binary Send Data signals so that a steady "1" (a positive voltage), or a repeated dotting signal, provides binary signals containing essential data crossings on a dibit basis. The only code which does not produce crossings is the steady "0." The distant receiver uses the data crossings to recover synchronization for receiver timing and to enable coherent detector operation. The scrambler-descrambler circuit can be optionally strapped out and is not used at a regenerator consisting of two Data Sets 207-type.

**3.10** The data set switch panel provides accessible front panel control of certain data set operations. The functions of the switches contained on the panel are briefly defined as follows:

MODEM LOOP TEST (S1): A three-position switch which provides for testing either locally or by a remote facility. The DIGITAL position disconnects the data set from the customer and loops the data and clock leads from the data set receiver to the data set transmitter to allow the demodulated receiver output signal to modulate the transmitter input. This allows remote testing of a terminal data set or half regenerator by a Data Test Center. The LINE position loops the data set transmitter output to the receiver input on the line side so that the modulated output of the transmitter circuits are connected to the receiver input. In addition, the telephone line pairs are disconnected and terminated in 600 ohms. This allows back-to-back testing of both terminal and regenerator data sets by the installer, and, in addition, allows remote testing of a full regenerator by a Data Test Center. The OFF position permits normal data set operation.

BIT RATE (S2): A five-position switch which conditions all data set circuitry to operate at the speed designated by the switch positions 150, 300, 600, 1200 and 2400 (bps). For regenerative repeater operation, the switch should normally be set at 2400 bps.

LAMP TEST (S3): A two-position ON-OFF switch which, in the ON position, simulates an alarm condition to test illumination of the ALARM lamp. Operation of this switch will not put an alarm signal on the interface leads. The OFF position permits normal alarm operation.

TERMINAL (S4): A two-position switch which, in the RESTRICTED position, encodes the transmitted data with the B bit clamped to 0 to effectively con-

centrate the transmitted line energy at 1200 bps or lower. This improves performance at the lower rates over degraded facilities. This switch has no effect when transmitting at 2400 bps. The NORMAL position permits normal operation at all transmission rates. A limiting factor affecting the use of the RESTRICTED mode is that all data sets used as regenerative repeaters must interchange clocks at 1200 Hz rather than 2400 Hz, and the far-end terminal data set must be able to interpret the preceding coding.

REC CARRIER (S5): A two-position ON-AUTO switch which, in the ON position, simulates a signal on the receiver signal sensor output that sensor circuits have detected compatible data signals. At a regenerator, this simulated signal allows connection of the data set receiver circuits to the telephone line without bypass control. The AUTO position activates the receiver sensor circuits to permit the sensor circuit to detect compatible data and reject noncompatible data.

TRAN CARRIER (S6): A two-position ON-AUTO switch which, in the ON position, simulates a signal on the transmitter signal sensor output that sensor circuits have detected a "signal present" condition. At a regenerator, this simulated signal allows connection of the data set transmitter circuits to the telephone line without bypass control. The AUTO position activates the transmitter signal sensor circuit such that if the transmitter output level drops an alarm is given.

RD TRANSITIONS (S7): A two-position ON-AUTO switch which, in the ON position, simulates a signal to the data set alarm logic circuits that RD crossings are present thereby locking out the receiver alarm circuits (RDTX). The AUTO position permits normal operation of the delayed alarm (RDTX).

SD TRANSITIONS (S8): A two-position ON-AUTO switch which, in the ON position, simulates a signal to the data set alarm logic circuits that SD crossings are present thereby locking out the transmitter alarm circuits (SDTX). The AUTO position permits normal operation of the delayed alarm (SDTX).

ALARM Lamp: A visual alarm display that is illuminated by alarms on either RSSD, TSS, SDTX, or RDTX leads for terminal data sets, or in the half regenerator data sets, displays a power unit failure alarm.

## DATA SET 207- TYPE TRANSMITTER CIRCUITS

**3.11** A simplified block diagram of the data set transmitter circuits is shown in Fig. 10. The customer business machine applies serial binary data signals to the data set through the interface Send Data (SD) lead. The signals are monitored by the SD transition sensor for SD transitions. If SD transitions are not monitored for approximately five seconds, the alarm circuit lead SDTX is operated. This alarm is only provided with terminal data sets.

**3.12** The scrambler receives either (1) signals on the SD lead, or (2) signals from the Remote Test and Idle Code logic circuits.

**3.13** The serial binary data is applied through a scrambler to generate data crossings on a dibit basis. The scrambler encodes SD to allow receiver synchronization and compatible signal sensor operation on the transmission of steady "1's" and reversals. The only code that does not contain timing information is the steady "0." Without the scrambler, the receiver cannot recover timing

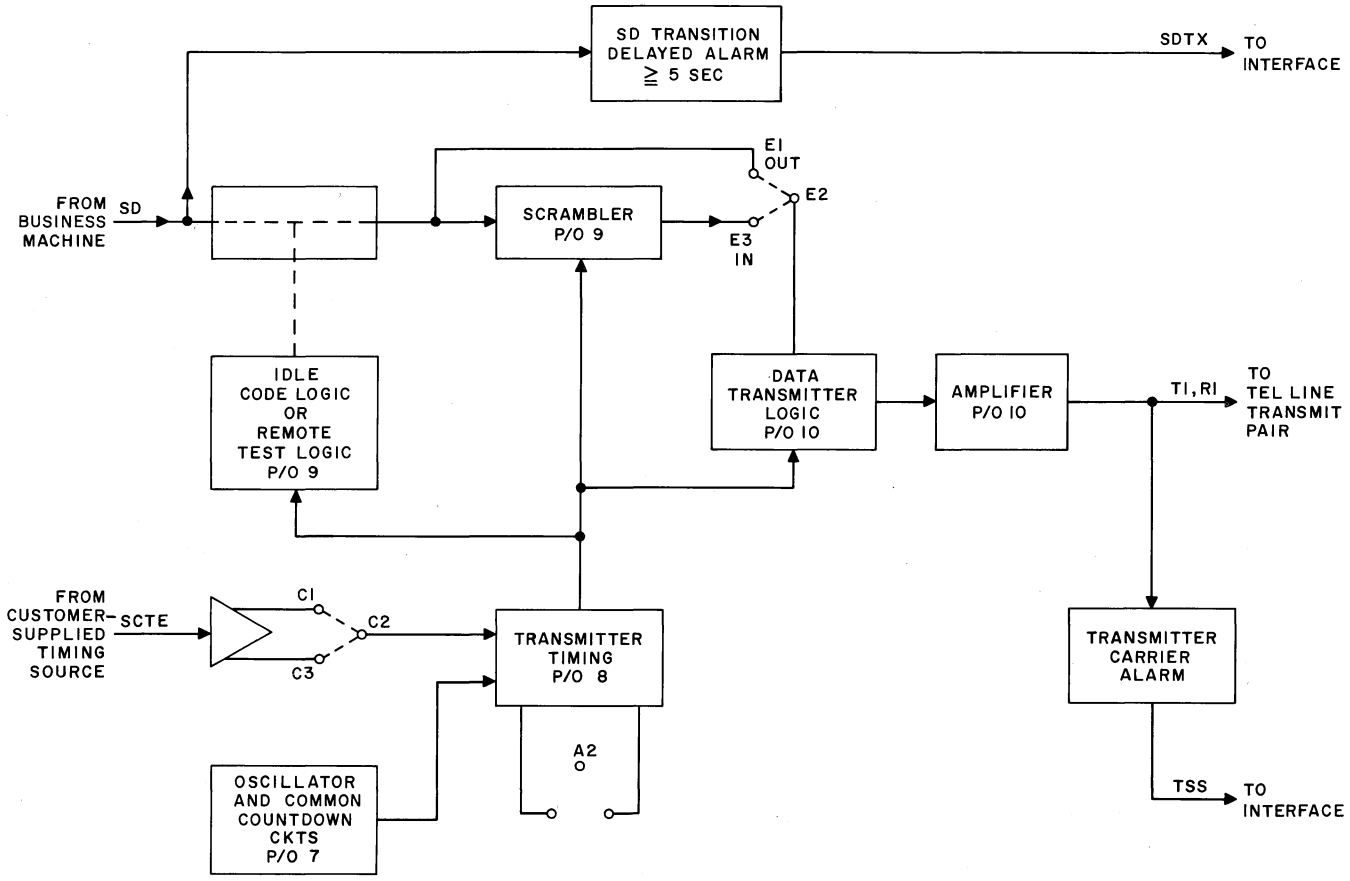



**Fig. 10—Data Set 207-Type Transmitter Circuits, Block Diagram**

from the transmission of steady "1's" and "0's" at any speed, or reversals at 2400 bps. After the scrambler, the signals are connected through an option shorting clip to the logic circuits in the data transmitter. The E2 shorting clip puts the scrambler in the circuit (E2 to E3) or out of the circuit (E2 to E1). At speeds of 1200 bps or lower, setting the TERMINAL switch in the RESTRICTED position causes the B bit at the input of the transmitter logic to be clamped to "0" for improved performance over degraded facilities.

**3.14** The data transmitter accepts the serial binary data (SD) at the selected data rate synchronous with the bit rate timing signal (SCTE) and produces the phase-modulated line signal which is applied to the telephone line on T1, R1. A timing option, or shorting clip C2, is provided to allow the transitions of SD to coincide with either the positive or negative transitions of the clock on SCTE. The transmitter output signal, when present, inhibits the transmitter carrier alarm providing that the TRAN CARRIER switch is in AUTO position.

**3.15** All data set transmitter circuits are timed synchronously from the (8) Transmitter Timing. The A2 shorting clip on circuit pack AR161 allows the transmitter clock to be synchronized with the dibit clock on SCTE (A2 to A1) for the regenerate mode, or the transmitter clock is synchronized with bit rate clock on SCTE (A2 to A3) for the terminal mode. Basic clock timing signals are supplied from the (7) Oscillator and Common Countdown circuits and the timing signals are synchronized to the customer's external clock source through the interface SCTE lead.

## DATA SET 207-TYPE RECEIVER CIRCUITS

**3.16** A simplified block diagram of the data set receiver circuits is shown in Fig. 11. The line signals are applied through the bandpass filter (BPF) to the AGC circuits. If the line signal is between -6 and -34 dbm (with a 0 pad loss in the AGC), the AGC circuits amplify the received line signal to a standard 2.5 (±0.3) volt peak-to-peak

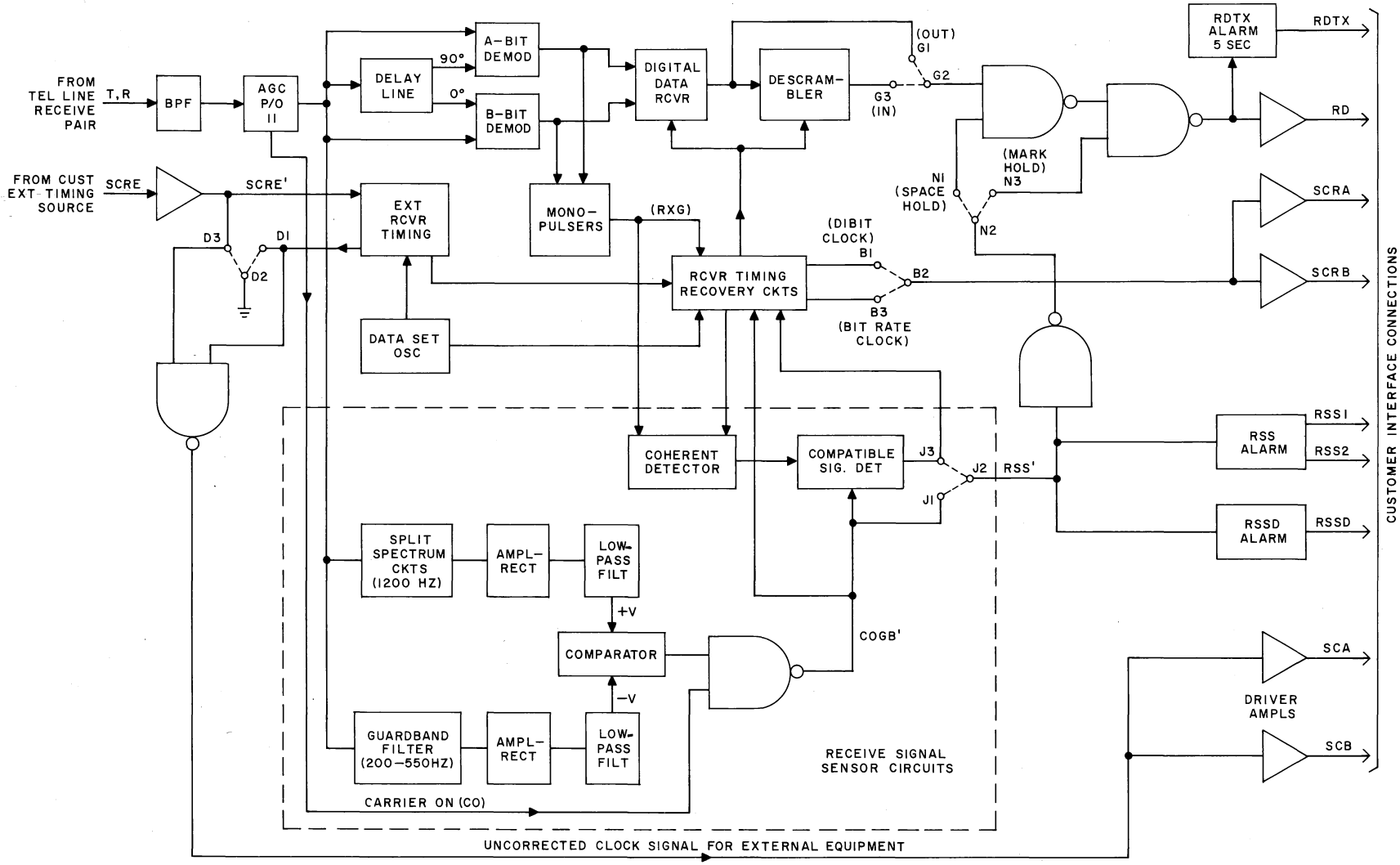



**Fig. 11— Data Set 207-Type Receiver Circuits, Block Diagram**

signal. Other AGC loss pads are available through option strapping to provide normal operation with line signal levels between +9 and -34 dbm.

**3.17** The AGC output signal is applied to both a delay line (DL) and a pair of demodulators. The delay line provides a signal delayed one dibit to the demodulators with the 0 and 90 degree signal phase relationships to develop the A bit and B bit demodulated (analog) signals. Demodulated A bit and B bit signals are applied to the (13) Digital Data Receiver. The outputs of the digital data receiver circuits are standard logic signals.

**3.18** The logic signals are applied through the descrambler to recover received data. Before the logic can be applied to the customer business machine, two gates must be conditioned by the Receive Signal Sensor circuits together with the requirement imposed through the N2 shorting clip on circuit pack AR161. Without compatible data, the RD can be held in Space Hold (N2 to N1, a negative voltage condition) or Mark Hold (N2 to N3, a positive voltage condition). When compatible data is present, RD is applied to the customer business machine while being monitored by the RD transition alarm circuits. With the RD TRANSITIONS switch in AUTO, loss of RD transitions for approximately five seconds will cause an alarm.

**3.19** The receive circuits are monitored and gated through the functions of the Receive Signal Sensor circuits. Amplified line signals from the AGC output are applied to both the guard band filter and the split spectrum circuits. When receiving compatible four-phase data signals, the guard band filter finds little or no line level energy in the frequency spectrum between 200 and 550 Hz (Fig. 12A and 12B). The guard band filter drives an amplifier-rectifier and a low-pass filter. The negative output voltage (-V) from the low-pass filter is applied to the comparator circuits.

**3.20** The split spectrum circuits (Fig. 12C) use both a high-pass filter and a low-pass filter which are centered about the 1800 Hz carrier. When receiving compatible data, the line level energy contains frequency components which are separated by 1200 Hz. The energy level from each filter is applied to a multiplier and through a 1200 Hz tuned filter. The tuned filter output is the recovered 1200 Hz difference frequency which is applied to the amplifier-rectifier and the low-pass filter to produce a positive voltage (+V) to be applied to the comparator.

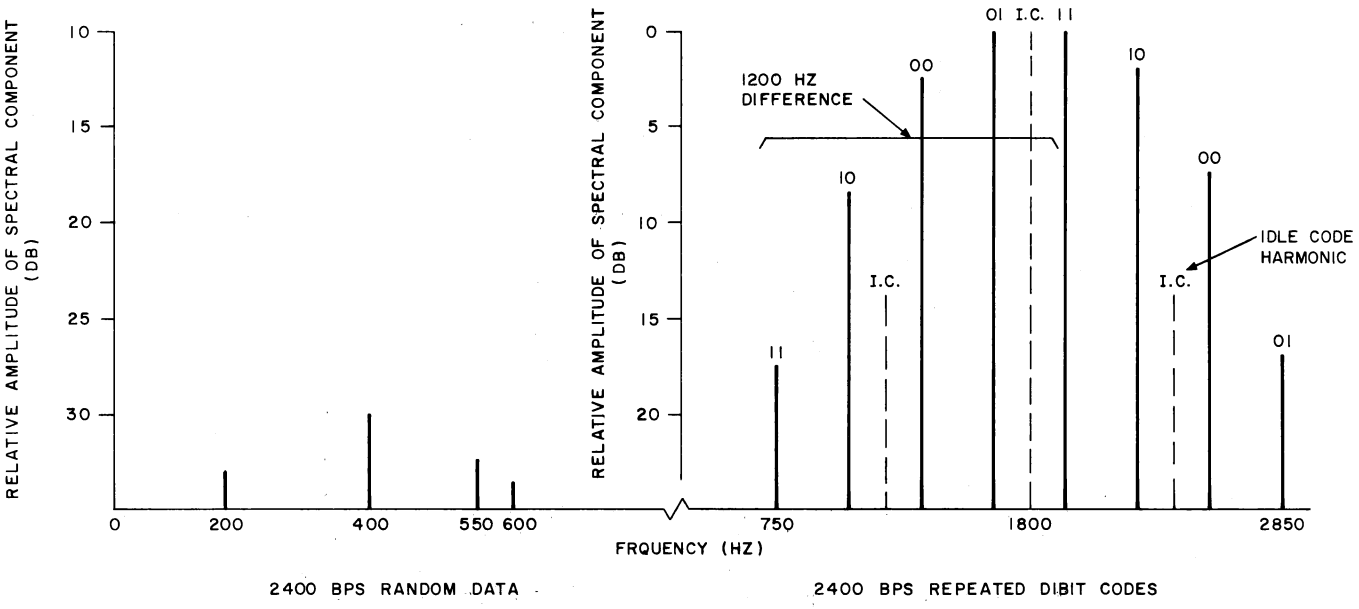
**3.21** The greater positive voltage is compared to the very small negative voltage by the comparator circuits. This condition exists only for compatible data; therefore, noncompatible data signals are detected and rejected by the comparator. The comparator output is gate-controlled by CO (a line level signal indication) from the AGC carrier detector circuit. When both conditions are satisfied, the comparator output releases an inhibit function on the receiver timing recovery circuits and enables the coherent detector and compatible signal detector.

**3.22** The outputs of both demodulators are applied to a monopulser to generate data axis-crossing pulses. The monopulser output is applied to both the receiver timing recovery circuits and the coherent detector circuits. The coherent detector provides an indication when compatible data axis-crossing pulses are received and only after the receiver timing has recovered sync. Output signals from the coherent detector and guard band circuits are used by the compatible signal detector to provide the Receive Signal Sensor (RSS) option through shorting clip J2 on circuit pack AR161. Shorting J2 to J1 does not provide RSS for receiver in-sync condition. Shorting J2 to J3 does provide receiver in-sync condition.

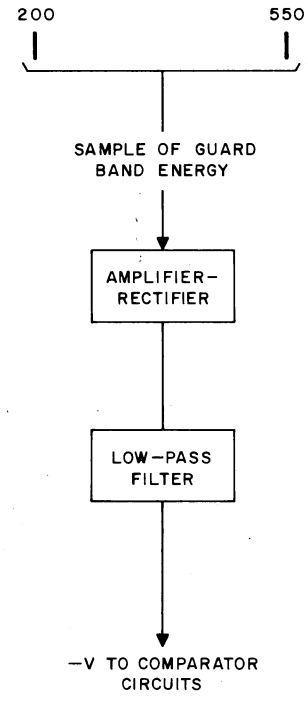
**3.23** The receive signal sensor output is provided to the customer through the interface connections. The output signals are also monitored by the Receive Signal Sensor alarm circuits (RSSD). An alarm is provided if compatible data is lost for approximately two seconds. This alarm is only provided with terminal data sets.

**3.24** The receiver timing recovery circuits obtain clock signals from (7) Oscillator and Common Countdown. Option X uses the highest accuracy oscillator (69A) to provide a minimum holdover of 30 minutes. Option Y uses the oscillator contained in circuit pack AR160 and holdover is determined by the accuracy of the externally supplied timing on SCRE. Correct use of shorting clip D2 on circuit pack AR161 is also part of option X or option Y. Shorting D2 to D1 allows external timing by SCRE of the (16) External Receiver Timing circuits (for option Y). Shorting D2 to D3 puts the SCRE′ lead at ground and relies on the internal accuracy for timing (option X).

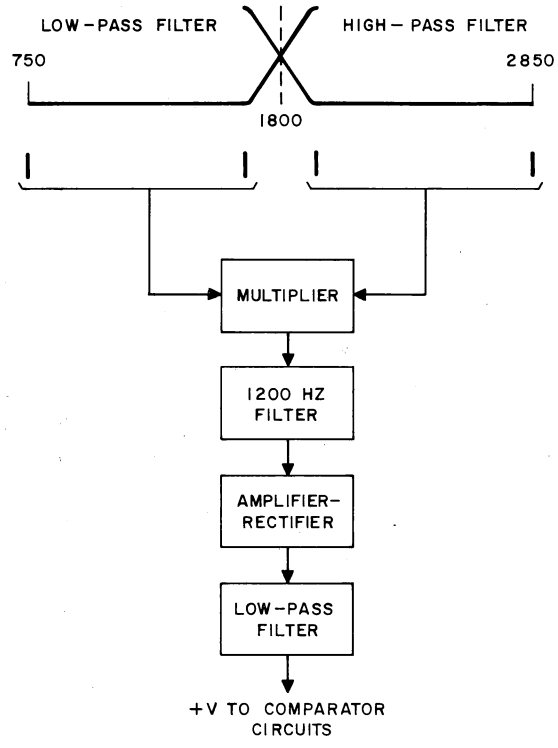
**3.25** The (16) External Receiver Timing circuits, using option Y, permit the receiver timing recovery circuits to be frequency-locked to an externally provided timing signal on SCRE. In




A. RECEIVED ENERGY SPECTRUM – COMPATIBLE FOUR – PHASE DATA




B. GUARD BAND FILTER




C. SPLIT SPECTRUM CIRCUITS

**Fig. 12—Simplified Receiver Circuit Operation**

addition, the circuits provide two identical uncorrected clock signals to the customer through interface leads SCA and SCB. These signals can be used to time other external equipment if desired.

## REGENERATION OPERATION

**3.26** Two compatible data sets connected in a back-to-back configuration on the digital side make the required circuitry necessary to regenerate data signals on a full-duplex basis. Regeneration is required when the transmission characteristics fail to meet requirements between the terminal stations. The block diagram shown in Fig. 13 illustrates a simplified regeneration hook-up.

**3.27** Two data sets are connected so that the receiver section of one set drives the

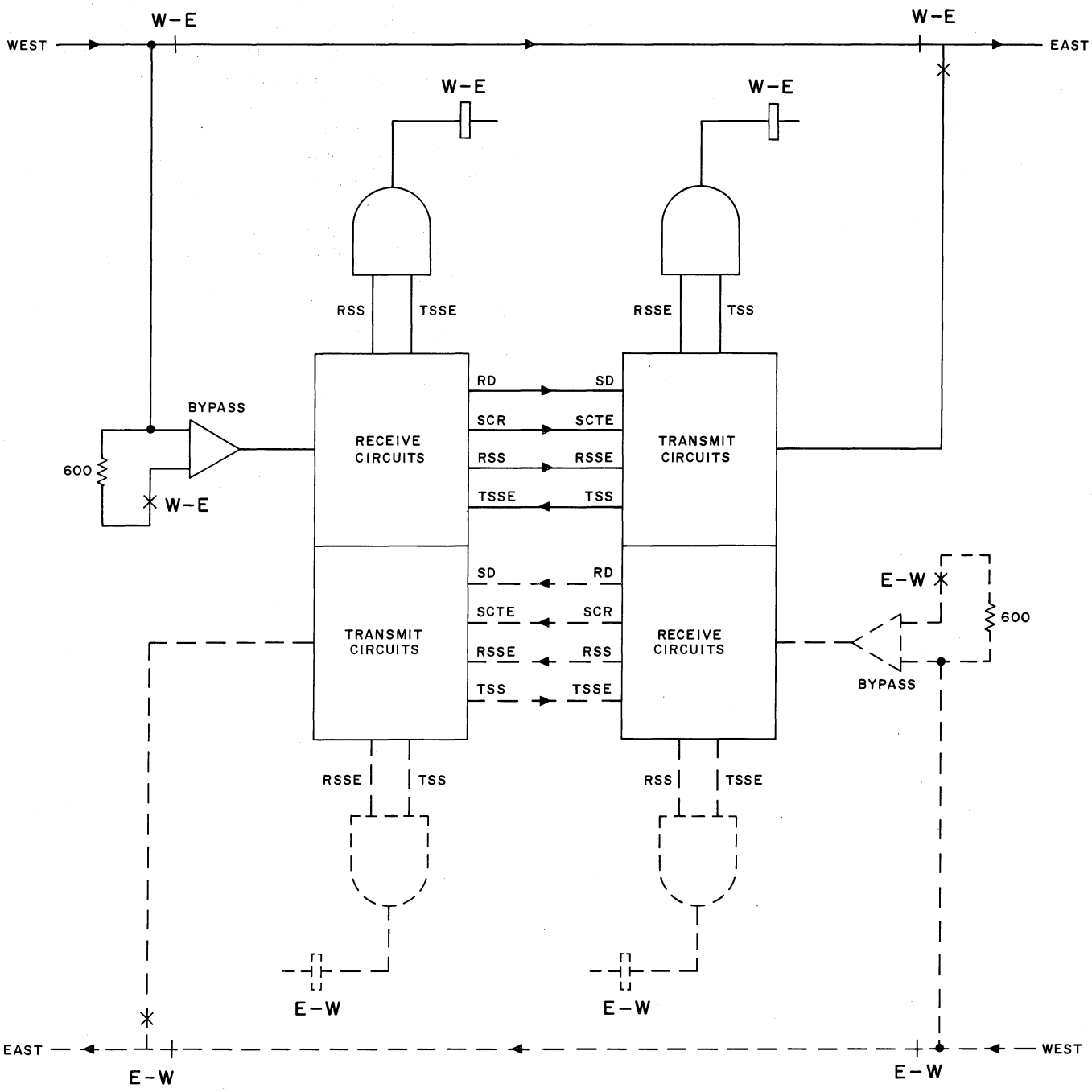



**Fig. 13—Simplified Regeneration Connections**

transmitter section of the second set. A regenerator may use either two Data Sets 207-type or one Data Set 207-type with a compatible data set of another type or manufacture. The regenerate options include the relays required to place the data set on-line when sensing compatible signals, or off-line when noncompatible signals are detected.

**3.28** The bypass control circuits provide relays to allow switching under the control of RSS and TSSE signals. Consider the transmission from a West-end station to an East-end station through a regenerator. When noncompatible signals are detected, the input and output of the regenerator are conditioned to prevent any transmission. The line is connected straight through and bypasses the regenerator circuits. The input presents a balanced load and the transmitter section is opened from the line through relay contacts controlled by each data set.

**3.29** When compatible signals are detected and provided a signal to indicate that transmit carrier is present, the bypass control circuits operate associated relays. The line is opened so that the compatible signals are applied through the regenerator receiver circuits. Receive Data (RD) output signals from the receiver are applied to the Send Data (SD), or transmitter input, of the second data set. Recovered receiver clock signals (SCR) are applied to the transmitter external clock lead (SCTE) to provide timing signals required for transmission. When the two half regenerators are Data Sets 207-type, the dibit clock is used to maintain the A bit and B bit identification. This requires option strapping of A1 to A2 and B1 to B2 on circuit pack AR161. Both data sets monitor their respective operations and provide each other with receive and transmit sensor signals. If a sensor signal is inhibited, both data sets remove their circuits from the line until the signal returns to normal.

**3.30** Operation is the same for both directions of transmission. The regenerator operates at 2400 bps only, and as such, repeats the incoming signals regardless of the bit rate at the terminal data sets. If both data sets of a regenerator are Data Set 207-type, the scrambler-descrambler circuits are not required.