

**DATA SET 212A**  
**TRANSMITTER-RECEIVER**  
**TEST PROCEDURES USING 921A DATA TEST SET**

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AL High-Speed Asynchronous Start-Stop Distortion Test—9-Bit Word . . . . .	16	1.01 This section contains test procedures to be followed when using a 921A-L1, -L2 (version II or later) data test set (DTS) to test a data set	
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(DS) 212A. These procedures are to be followed when investigating a trouble report or when needed during an installation. Test procedures using the 914 DTS are described in the section entitled Data Set 212A Transmitter-Receiver—Test Procedures (592-034-500).

**1.02** When this section is reissued, the reason for reissue will be contained in this paragraph.

**1.03** DS 212A provides full-duplex transmission and reception of serial binary data at two distinct bit rates over the switched network. In the low-speed mode, the maximum bit rate is 300 bits per second (bps). In the high-speed mode, operation is synchronous or character-asynchronous at 1200 bps. Additional information concerning DS 212A is contained in the section entitled Data Set 212A Transmitter-Receiver—Description and Operation (592-034-100).

**1.04** The 921A DTS is a portable, general purpose, serial data test set which provides the serial testing capabilities of the 914C DTS and is compatible with the 914C for end-to-end testing. In addition, the 921A DTS is compatible with the 911A and 911NA DTSs for end-to-end start-stop distortion measuring purposes. Additional information concerning the 921A DTS is contained in the section entitled 921A Data Test Set—Description (107-104-100).

**1.05** Input to the 921A DTS is made through the 20-button keyboard. The 32-character alphanumeric display provides operator prompting and diagnostic results. Refer to Fig. 1 for the location and nomenclature of connectors, switches, status indicators, input and output jacks, etc, which will be used in the course of testing DS 212A.

## **2. INSTALLATION TESTS**

**2.01** After the data set has been installed, it must be tested to determine if it is operating properly. Before proceeding with the test, verify that the local loop meets the requirements specified in the section entitled Data Systems—DATAPHONE® Service—Direct Distance Dialing Network—Test Requirements for Subscriber, Foreign Exchange and Remote Exchange Lines (314-205-501).

**2.02** Refer to Fig. 2 for the sequence of tests to be performed to verify proper installation. The 921A DTS is not required for installation testing, but may be used if needed.

## **3. MAINTENANCE TESTS**

**3.01** This part provides the sequence in which tests are to be performed during a maintenance visit. This test sequence provides a method of isolating a trouble to the data set, the transmission facility, or the customer-provided equipment (CPE).

**3.02** When a trouble report is received, the DTC is responsible for isolating the trouble to the data set or transmission facility. The procedure for doing this is shown in Fig. 3.

**3.03** If it is suspected that the trouble is in the data station equipment, a telephone company (telco) employee must be dispatched to conduct more extensive tests. The following equipment should be taken on a trouble visit:

- Spare DS 212A-L1A/2A
- 921 DTS (for conducting error tests through the interface).

**3.04** Refer to Fig. 4 for the sequence in which tests are to be performed by the telco employee at the data station. If the data set is replaced, the defective data set should be tagged with a tag describing the nature of the trouble, carefully packed and returned to a service center for repair. Verify that the replacement data set is equipped with the proper options before placing the data set in service.

**3.05** If the trouble persists, proceed as follows:

- (a) Check that the options installed in the data set agree with those specified on the service order.
- (b) Verify that the CPE has been tested and is operating properly.
- (c) Check for physical damage to the data station equipment.
- (d) Verify that all cords and connectors are properly connected.
- (e) Check for intermittent trouble in the station wiring.
- (f) Verify that the data set and CPE are connected to a common ground.

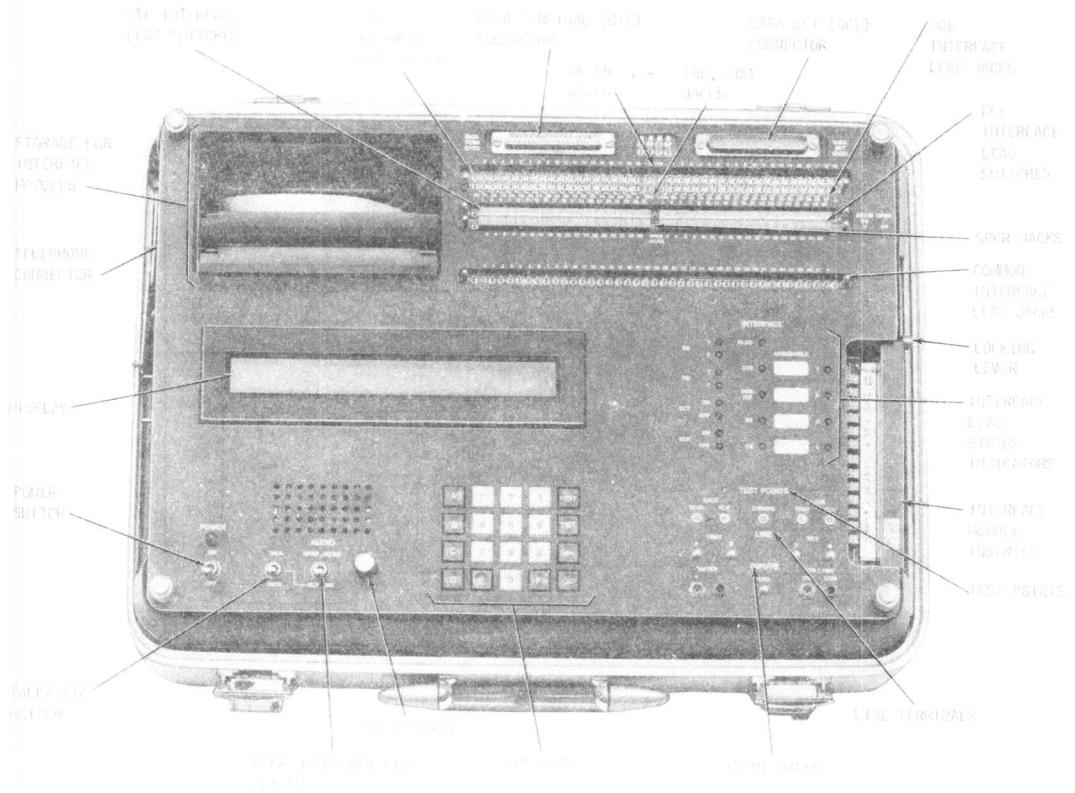


Fig. 1—921A Data Test Set—Front Panel

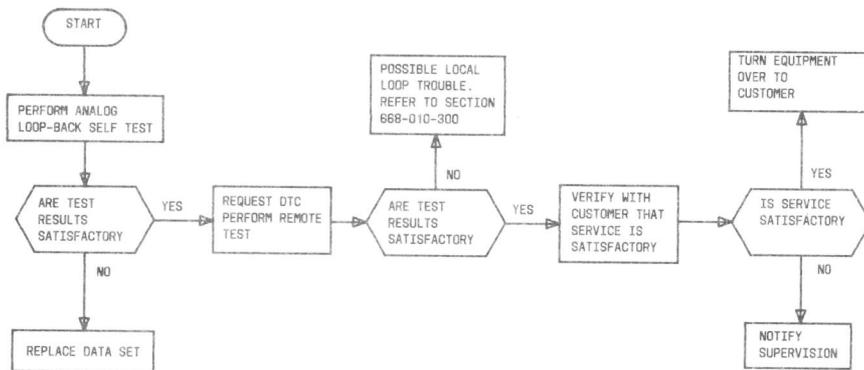


Fig. 2—Installation Test Sequence

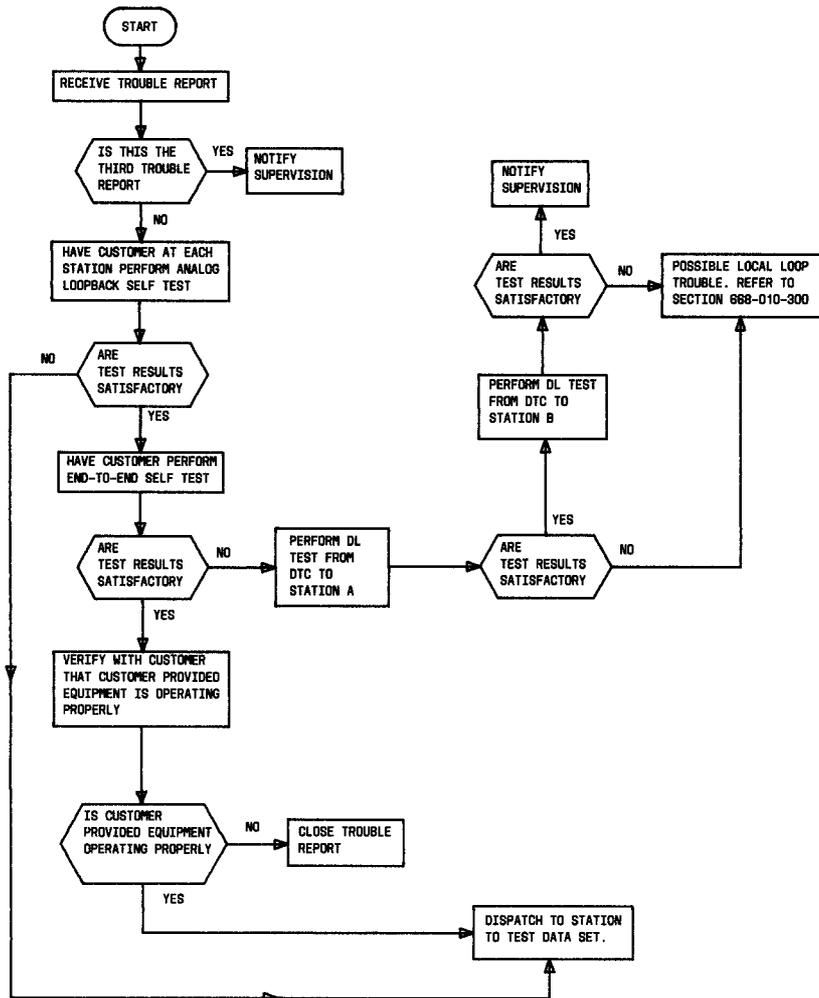


Fig. 3—Clearing Trouble Report

(g) If the trouble persists, request help from immediate supervisor.

4. TEST PROCEDURES

TEST CAPABILITIES

4.01 Test circuitry built into DS 212A permits the following self tests to be performed.

- Analog Loopback Self Test
- Digital Loopback Self Test
- End-to-End Self Test
  
- Remote Digital Loopback Self Test (High-Speed Mode).

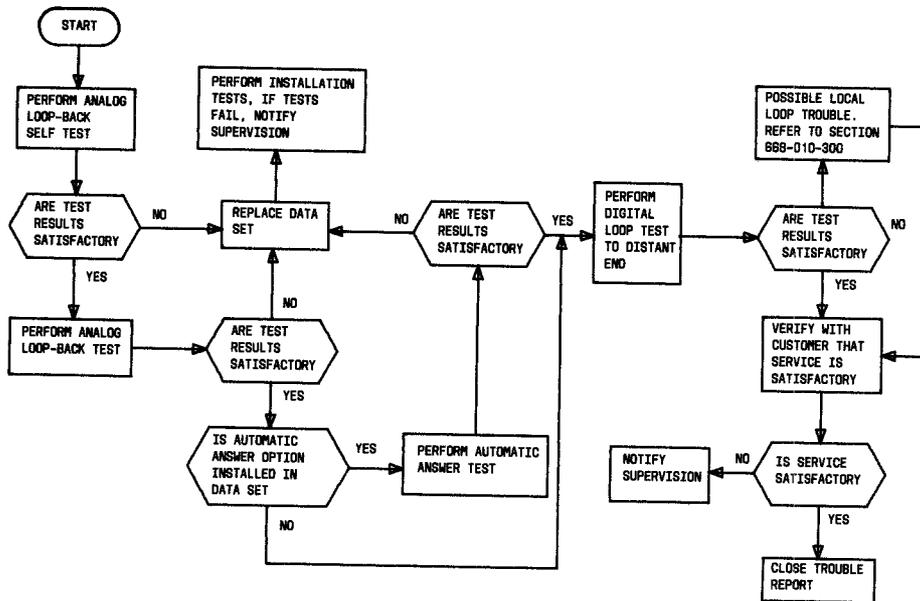


Fig. 4—Maintenance Test Sequence

4.02 If a 921 DTS is used, the analog loopback, digital loopback, and end-to-end tests can be done using pseudorandom data. By use of the 921 DTS, the customer interface circuits are tested and a more precise indication of bit and block errors can be obtained. Start-stop distortion test can be performed for asynchronous operation. The 921 DTS can also be used to perform a test of the data set automatic answer and interface circuits.

**A. Analog Loopback Self Test**

4.03 The analog loopback self test checks the data set transmitter and receiver (Fig. 5). The customer interface is not checked. Test data (dotting pattern) generated by the data set is looped from the transmitter output to the receiver input. The received data is compared to the transmitted data. This test can be performed in either the high-speed or low-speed mode. If the data set is operating in the low-speed mode, the MC lamp blinks if the distortion threshold (25 percent) is exceeded. If the data set is operating in the high-speed mode, the MC lamp blinks if a bit error is detected in the received data. The speed is

controlled by the HS switch and/or interface lead. Perform the test in the speed mode used by the CPE. Perform the test as follows:

- (1) Set the speed mode of the test by either setting the position of the HS button (IN for high-speed mode) through the customer interface.
- (2) Press the AL and ST switches on the data set.

**Requirement:** The MB and the TM indicators are lighted. The MC indicator goes off after the SD and RD indicators light. Disregard the TR indicator on DS 212A-L1; the TR indicator is either lighted or off depending on the state of the CD lead from the CPE. The TR indicator is lighted anytime ST or DL is depressed on DS 212A-L1A. The MR lamp is lighted if data set is equipped with option ZF.

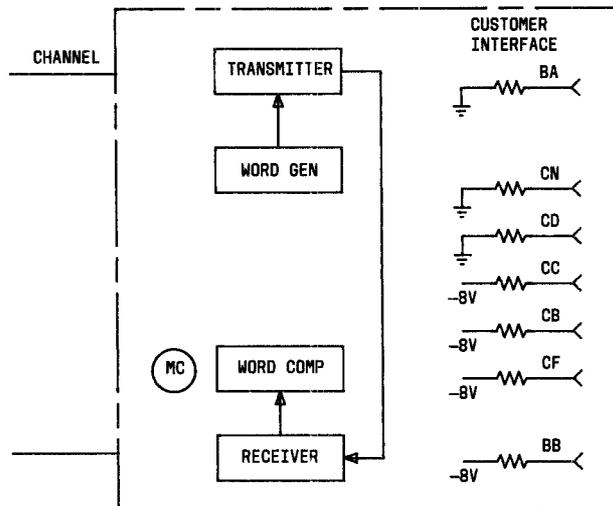


Fig. 5—Analog Loopback Self Test—Simplified Block Diagram

(3) Observe the MC indicator for 1 minute:

**Requirement:** MC indicator does not blink.

(4) Release the AL and ST switches.

**B. Digital Loopback Self Test**

**4.04** This test takes advantage of the digital loopback capability of the data set at one end and the self-test (pattern generating and comparing) capability of the data set at the other end (Fig. 6). The test is performed by putting one data set in the DL mode, placing the other data set in the ST mode, placing a call, and then going to the data mode. The MC indicator on the data set which is in the ST mode blinks when data distortion of a single bit exceeds 25 percent (low-speed) or if a received error occurs (high-speed).

**Note:** In the low-speed mode, the distant data set may be 103J, 113C, or 113D.

**4.05** Perform this test at the speed mode used most often by the CPE or in the speed

mode which is causing difficulty. The speed mode is selected by use of the HS button. The test is performed as follows:

- (1) Place a call to the distant end. If the distant data set is already in the DL mode, it will answer automatically.
- (2) If the distant data set does not answer automatically, instruct the attendant at the distant end to press the DL switch and go to the data mode.
- (3) On the local data set, press the ST switch and go to the data mode.
- (4) Observe the MC indicator for 2 minutes.

**Requirement:**

- Low-Speed—If the MC indicator stays off, both data sets and the line facilities are operating properly. If the MC indicator blinks or remains lighted, the round trip distortion is exceeding 25 percent. Since

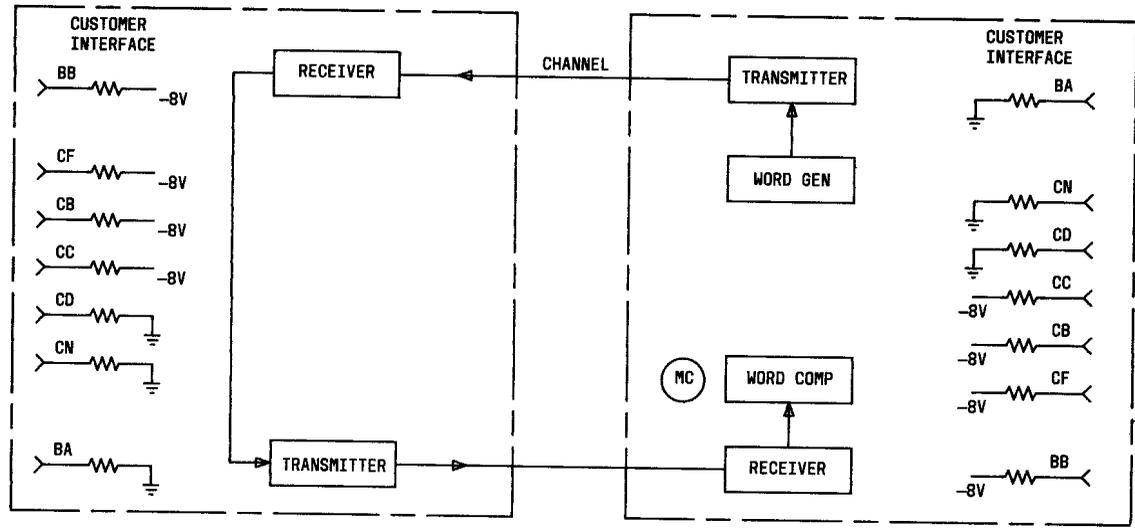


Fig. 6—Digital Loopback—Simplified Block Diagram

the distortion in the two directions may be additive, no conclusion about the proper operability of the data sets and the line facility may be drawn.

- High-Speed—Maximum of six blinks

- (5) Release the ST switch on the local data set. Call the distant end and have the DL switch released.

#### C. Remote Digital Loopback Self Test

**4.06** This test takes advantage of the remote digital loopback and self-test capabilities of the local data set and can be used to test both data sets and the communication channel in the high-speed mode only. The local data set is placed in the self-test mode by pressing the ST button. The distant data set is placed in the remote digital loopback mode by pressing the RDL switch on the local data set. The local data set pattern generator is used to send a signal to the distant end, where it is looped back and retransmitted. The error-detecting circuitry causes the MC indicator on the local data set to blink when an error is detected in the received data.



*If the distant data set is equipped with option YL (receiver responds to digital loop—OUT) or option ZG (automatic answer—OUT), this test cannot be done.*

**4.07** The test is performed as follows:

- (1) Press the HS, RDL, and ST switches on the local data set and verify that the TM indicator lights.
- (2) Dial a call to the distant data set.
- (3) When the distant data set has answered, place the local data set in the data mode.
- (4) Observe the MC indicator on the local data set for 2 minutes.

**Requirement:** Maximum of six blinks.

**Note:** If the MC indicator is lighted continuously, this may indicate that the distant data set is not in DL mode.

- (5) Release the RDL and ST switches on the local data set. Return the data set to the speed mode used by the CPE.

#### D. End-to-End Self Test

**4.08** This test can be used to check the local data set, the distant data set, and the communication channel. This test is performed by pressing the ST switch at each end, placing a call from one end to the other, and then going to the data mode. Each data set sends the test pattern to the other end. The speed mode of the test is selected at the originating station. The error-detecting circuitry at each end monitors the received data signal and causes the MC indicator to blink if the distortion threshold (25 percent) is exceeded (low-speed) or if an error is detected (high-speed).

**Note:** For low-speed testing, the distant end may be a DS 103J, 113C, or 113D.

**4.09** The test is performed as follows:

- (1) Call the distant end and arrange to conduct an end-to-end self test. At the originating station, the speed mode is selected by use of the HS button.
- (2) Press the ST switch on the front of each data set. Verify that the TM indicator lights.
- (3) Go to the data mode at each end. Verify that the MC indicator goes off after the SD and RD indicators light. Disregard the TR indicator on DS 212A-L1; the TR indicator is lighted or off, depending on the state of the CD lead from the CPE. The TR indicator is lighted anytime ST or DL is depressed on DS 212A-L1A. The HS indicator is lighted or off, depending on the speed mode of the test.
- (4) Observe the MC lamp on the front of the data set for 2 minutes.

#### **Requirement:**

- Low-Speed—If the MC indicator stays off, both data sets and the line facilities are operating properly. If the MC indicator blinks or remains lighted, the distortion is exceeding 25 percent.

- High-Speed--Maximum of two blinks

(5) At the end of the test, go to the talk mode and then release the ST switch.

**E. Initial Test Setup for 921A DTS**

**4.10** The initial test setup to test DS 212A using the 921A DTS is as follows:



**Ignore lamps on 921 DTS unless specifically designated.**

STEP	ACTION	VERIFICATION
1	Connect data set to DTS using interface and adapter cords provided with DTS.  <i>Note:</i> The interface cord is equipped with a 37-pin connector on each end. The 6-inch adapter cord matches the interface cord to the 25-pin interface connector on the data set.	
2	Connect DTS to a 105-129 Vac 60-Hz power source.	
3	Apply power to data set.	Data set ON lamp lights.
4	On front of DTS, set POWER switch to ON.	POWER lamp on DTS lights.
5	Press RST on input keyboard.  <i>Note:</i> If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display indicates version number of DTS (921A VERS #02). DTS then performs certain self tests. If DTS is defective, a TEST FAILED message appears on display. If DTS is satisfactory, display reads— DATA SET:
6	Remove Electronic Industries Association (EIA) RS-232-C interface card from storage and ensure that all 25 interface lead switches are in TERM position.	
7	On right side of DTS, ensure that latch is in OPEN position.	
8	Insert interface into slot.	
9	Move latch to CLOSE position.	
10	On front of DTS, ensure that: All 37 DCE interface lead switches are in	

STEP	ACTION	VERIFICATION
	NORM position. AUDIO switch is in RCV LINE position. TALK/DATA switch is in DATA position.	
<b>F. Analog Loopback Test With 921 DTS</b>		(2) Verify that DS 212A is in the low-speed mode (HS button out) if option XK is installed. Speed selection is automatic when option XJ is installed.
<b>4.11</b>	This test checks the data set interface and transmitter and receiver circuits. Test data is generated by a DTS and looped back from the data set transmitter output to the receiver input. The received data is compared to the original data by the DTS and errors are indicated on the DTS display.	(3) Depress the AL button on the data set. If option ZF is installed, verify that MR lamp on data set and DSR on the 921 DTS lights.
<b>4.12</b>	Perform this test in the speed mode used most often by the CPE or in the speed mode which is causing difficulty.	<b>4.14</b> Perform the test as follows:

**AL Low-Speed Bit Error Test**

**4.13** Condition DS 212A as follows:

- (1) Verify that option YP is installed.

STEP	ACTION	VERIFICATION
1	Press RST on input keyboard.  <i>Note:</i> If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display indicates version number of DTS (921A VERS #02). DTS then performs some self tests. If DTS is defective, a TEST FAILED message appears on display. If DTS is satisfactory, display reads— DATA SET:
2	Enter 36 on input keyboard.	Display reads— DATA SET: 36
3	Press GO.	Display reads— BIT RATE:
4	Enter 03.	Display reads— BIT RATE: 03
5	Press GO.	Display reads— TEST SEQ:
6	Enter 55.	Display reads— TEST SEQ: 55
7	Press GO.	Display reads: TRANSMITTER=? 1=921 2=914 3=903

STEP	ACTION	VERIFICATION
8	Enter 1.	Display reads (briefly)— TRANSMITTER=1 1=921 2=914 3=903 Display then reads— D=DT 0=SP 1=MK 2=2047 5=511 6=63
9	Enter 5.	Display reads (briefly)— 511 BIT ERROR TEST Display then reads— 1=BIT ERRORS 2=BLOCK ERRORS
10	Enter 1.	Display reads— ???? SECONDS
11	Enter 0060.	

**Note:** To perform functions listed below, press associated key.

**KEY            FUNCTION**

- A Repeat test.
- B Display time remaining in test.
- C Clear display.
- D End test.
- E Inject errors into data stream.
- F Force out-of-sync condition.

Display reads (briefly)—  
0060 seconds  
Display then reads—  
0000 BITS IN ERROR  
From this point, DTS counts the number of bit errors. If an out-of-sync condition occurs, display flashes OSYN. If this happens, the test must be restarted by pressing A. At the end of the test, the DTS display reads briefly each of the following messages:  
TEST COMPLETE  
XXXXX SYNC LOSSES  
XXXX BITS IN ERROR

**Requirement:** 0 errors.

**AL Low-Speed Start-Stop Distortion**

**4.16** Perform test as follows:

**4.15** Condition DS 212A as described in paragraph 4.13.

STEP	ACTION	VERIFICATION
1	Press RST on input keyboard.  <b>Note:</b> If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display indicates version number of DTS (921A VERS #02). DTS then performs some self tests. If DTS is defective, a TEST FAILED message appears on display. If DTS is satisfactory, display reads— DATA SET:
2	Enter 36 on input keyboard.	Display reads— DATA SET: 36

STEP	ACTION	VERIFICATION
3	Press GO.	Display reads— BIT RATE:
4	Enter 03.	Display reads— BIT RATE: 03
5	Press GO.	Display reads— TEST SEQ:
6	Enter 52 79.	Display reads— TEST SEQ: 52 79
7	Press GO.	Display reads— PARITY=? (0=EVEN, 1=ODD)
8	Enter 0.	Display reads (briefly)— PARITY=0 (0=EVEN, 1=ODD) Display then reads— TRMT=? (1=MAN 2=CONT)
9	Enter 2.	Display reads (briefly)— TRMT=2 (1=MAN 2=CONT) Display then reads— PRESS A TO START  <i>Note:</i> Ignore display "PRESS A TO START"
10	Press GO.	Display reads (briefly)— TEST INTERRUPTED Display then reads— MODE=? (1=RCV 2=RCV & TRMT)
11	Enter 2.	Display reads (briefly)— MODE=2 (1=RCV 2=RCV & TRMT) Display then reads— HITS OVER??% (MAX=49%)
12	Enter 08.	Display reads (briefly)— HITS OVER 08% (MAX=49%) Display then reads— ??? SECONDS
13	Enter 0060.	Test begins and runs for 60 seconds. Display reads— PEAK=XX% HITS=XX/08 AWG BIAS=XX%

*Note:* To perform functions listed below,  
press associated key.

*Note:* If the peak reading on the display is  
greater than 08% when the test begins, press

STEP	ACTION	VERIFICATION
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the C key to clear the display readings and allow test to continue.

KEY	FUNCTION
-----	----------

- A Repeat test.
- B Display time remaining in test.
- C Clear display.
- D End test.

After 60 seconds, the display cycles through two messages:  
PEAK=XX% HITS=XX/08 AVG BIAS=XX% and TEST COMPLETE

**Requirement:** PEAK=08% MAX HITS=00/08  
AVG BIAS=01% MAX

**AL High-Speed Synchronous Bit Error Test**

(2) Depress the AL and HS buttons on the data set.

**4.17** Condition data set as follows:

(1) Verify that option YH is installed.

**4.18** Perform the test as follows:

STEP	ACTION	VERIFICATION
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1 Press RST on input keyboard.

**Note:** If RST is pressed during a test, the test is ended and the DTS recycles to this step.

Display indicates version number of DTS (921A VERS #02). DTS then performs some self tests. If DTS is defective, a TEST FAILED message appears on display. If DTS is satisfactory, display reads—  
DATA SET:

2 Enter 66 on input keyboard.

Display reads—  
DATA SET: 66

3 Press GO.

Display reads—  
BIT RATE:

4 Enter 12.

Display reads—  
BIT RATE: 12

5 Press GO.

Display reads—  
TEST SEQ:

6 Enter 55.

Display reads—  
TEST SEQ: 55

7 Press GO.

Display reads—  
D=DT 0=SP 1=MK 2=2047 5=511 6=63

8 Enter 5.

Display reads (briefly)—  
511 BIT ERROR TEST  
Display then reads—  
1=BIT ERRORS 2=BLOCK ERRORS

STEP	ACTION	VERIFICATION
9	Enter 1.	Display reads— ??? SECONDS
10	Enter 0060.	
	<b>Note 1:</b> If sync is lost during the test, the right portion of the display will flash OSYN. If this occurs, the test must be restarted by pressing A.	
	<b>Note 2:</b> To perform functions listed below, press associated key.	
	<b>KEY</b>	<b>FUNCTION</b>
	A Repeat test.	Display reads (briefly)— 0060 SECONDS
	B Display time remaining in test.	Display then reads— 0000 BITS IN ERROR
	C Clear display.	
	D End test.	
	E Inject errors into data stream.	
	F Force out-of-sync condition.	After 60 seconds, the display cycles through these messages: TEST COMPLETE; XXXX SYNC LOSSES; XXXX BITS IN ERROR
		<b>Requirement:</b> Total bits in error are less than 12.

**AL High-Speed Asynchronous Start-Stop Distortion Test—10-Bits/Character** (2) Depress AL and HS buttons on the data sel.

4.19 Condition data set as follows:

- (1) Verify that options YG and YJ are installed.

4.20 Perform the test as follows:

STEP	ACTION	VERIFICATION
1	Press RST on input keyboard.  <b>Note:</b> If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display indicates version number of DTS (921A VERS #02). DTS then performs some self tests. If DTS is defective, a TEST FAILED message appears on display. If DTS is satisfactory, display reads— DATA SET:
2	Enter 36.	Display reads— DATA SET: 36
3	Press GO.	Display reads— BIT RATE:
4	Enter 12.	Display reads— BIT RATE 12

STEP	ACTION	VERIFICATION
5	Press GO.	Display reads— TEST SEQ:
6	Enter 52 79.	Display reads— TEST SEQ: 52 79
7	Press GO.	Display reads— BITS/CHAR=? (0=NINE 1=TEN)
8	Enter 1.	Display reads briefly— BITS/CHAR=1 (0=NINE 1=TEN) Display then reads— PARITY=? (0=EVEN, 1=ODD)
9	Enter 0.	Display reads (briefly)— PARITY=0 (0=EVEN, 1=ODD) Display then reads— TRMT=? (1=MAN 2=CONT)
10	Enter 2.	Display reads— TRMT=2 (1=MAN 2=CONT) Display then reads— PRESS A TO START  <b>Note:</b> Ignore display “PRESS A TO START”
11	Press GO.	Display reads (briefly)— TEST INTERRUPTED Display then reads— MODE=? (1=RCV 2=RCV & TRMT)
12	Enter 2.	Display reads— MODE=2 (1=RCV 2=RCV & TRMT) Display then reads— BITS/CHAR=? (0=NINE 1=TEN)
13	Enter 1.	Display reads (briefly)— BITS/CHAR=1 (0=NINE 1=TEN) Display then reads— HITS OVER??% (MAX=49%)
14	Enter 16.	Display reads (briefly)— HITS OVER 16% Display then reads— ???? SECONDS
15	Enter 0060.  <b>Note:</b> To perform functions listed below, press associated key.	Test begins and display then reads— PEAK=XX% HITS=XX/08 AWG BIAS=XX%  <b>Note:</b> If the peak reading exceeds 16% when the test begins, press the C key to clear the display readings and allow the test to continue.

STEP	ACTION	VERIFICATION
	<p><b>KEY</b></p> <p><b>FUNCTION</b></p> <p>A Repeat test.            B Display time remaining in test.            C Clear display.            D End test.            E Inject errors into data stream.            F Force out-of-sync condition.</p>	<p>After 60 seconds, the display reads—            TEST COMPLETE; then PEAK=XX%            HITS=XX/16 AVG BIAS=XX%</p> <p><b>Requirements:</b></p> <p>PEAK=16% MAX HITS=00/16 AVG BIAS=06%            MAX</p>

**AL High-Speed Asynchronous Start-Stop Distortion Test—9-Bit Word**

4.21 The 9-bit word test and requirements are the same as the test and requirements for the 10-bit word described in paragraphs 4.19 and 4.20 with the following changes:

- Install option YI.
- Step 8 enter “0” instead of “1”; the display reads briefly: BITS/CHAR=0 (0=NINE 1=TEN), display then reads TRMT=? (1=MAN 2=CONT).
- Omit Step 9.
- Step 13 enter “0” instead of “1”; the display reads briefly: BITS/CHAR=0 (0=NINE 1=TEN), then reads “HITS OVER??% (MAX 49)”.
- Step 14 enter 14 instead of 16; the display reads briefly: HITS OVER 14%, then reads “???? SECONDS”.
- Step 15 change requirements to: PEAK=14% MAX, HITS=00/14%, AVG BIAS=06% MAX.

**G. Digital Loopback Test With 921 DTS**

4.22 This test checks the transmitter and receiver of both data sets and the connecting facility. The distant data set can be a 103J, 113C, or 113D. The customer interface at the distant data set is not checked. Test data is generated by the DTS and transmitted by the local data set. This data is looped back from the receiver output to the transmitter input of the distant data set and retransmitted. The data is received by the local

data set and is compared to the original data. Data errors are indicated on the display of the DTS.



**This test cannot be done in the high-speed mode if option WI (transmitter timing—SLAVE) is installed in the local data set.**

4.23 Perform this test at the speed mode used most often by the CPE or in the speed mode which is causing difficulty.

4.24 DS 212A-type has the capability to force the distant data set into a digital loopback mode. The test can only be used when the data set is in the high-speed mode. The remotely activated digital loopback takes place at the distant data set only if options YK (receiver responds to digital loop—IN) and ZH (automatic answer—IN) are installed at that end and the CD (data terminal ready) lead is **on**. If option YE is installed, interface lead CN must be **off**.

4.25 Make sure the initial test setup using 921 DTS to test DS 212A is followed. Refer to paragraph 4.10.

**D1 Low-Speed Bit Error Test**

4.26 Condition DS 212A as follows:

- (1) Verify that DS 212A is in the low-speed mode (HS button out for DS 212A-L1 and either HS button out or interface control for DS 212A-L1A). Speed selection is controlled by interface lead CH (pin 23) going low when option XD is installed. Add strap between 10 and 23 of common interface terminal on DTS.

4.27 Perform test as follows:

STEP	ACTION	VERIFICATION
1	Press RST on input keyboard.  <i>Note:</i> If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display indicates version number of DTS (921A VERS #02). DTS then performs self tests. If DTS is defective, a TEST FAILED message appears on display. If DTS is satisfactory, display reads— DATA SET:
2	Enter 36 on input keyboard.	Display reads— DATA SET: 36
3	Press GO.	Display reads— BIT RATE:
4	Enter 03.	Display reads— BIT RATE: 03
5	Press GO.	Display reads— TEST SEQ:  <i>Note:</i> If the DL low-speed start-stop distortion test is to be performed, also enter 52, 79 at this time.
6	Enter 55.	Display reads— TEST SEQ: 55
7	Press GO.	Display reads— TRANSMITTER=? 1=921 2=914 3=903
8	Enter 1.	Display reads (briefly)— TRANSMITTER=1 1=921 2=914 3=903 Display then reads— D=DT 0=SP 1=MK 2=2047 5=511 6=63 Also observe that DTR on 921 DTS lights.
9	Enter 5.	Display reads (briefly)— 511 BIT ERROR TEST Display then reads— 1=BIT ERRORS 2=BLOCK ERRORS
10	Place call to distant end and request the attendant to depress the DL switch on the data set and go into data mode at both ends.	Verify that RLSD, DSR, and CS on 921 DTS are lighted.
11	Enter 1.	Display reads— ??? SECONDS
12	Enter 0300.	

*Note:* To perform functions listed below, press associated key.

STEP	ACTION	VERIFICATION
	<p><b>KEY</b></p> <p>A Repeat test. B Display time remaining in test. C Clear display. D End test. E Inject errors into data stream. F Force out-of-sync condition.</p>	<p>Display reads (briefly)— 0300 SECONDS Display then reads— 0000 BITS IN ERROR From this point, display counts the number of errors. If an out-of-sync condition occurs, display flashes OSYN. If this happens, the test must be restarted by pressing A. At the end of the test, the display indicates: TEST COMPLETE XXXXX SYNC LOSSES XXXX BITS IN ERROR</p> <p><b>Requirement:</b> 1 or less bits in error.</p> <p><i>If DL low-speed start-stop distortion test is going to be performed, do not hang up. Press GO, display reads briefly TEST INTERRUPTED: display then reads PARITY=? (0=EVEN, 1=ODD) Skip to Step 9 of paragraph 4.29 and proceed with test.</i></p>



**DL Low-Speed Start-Stop Distortion**

4.29 Perform test as follows:

4.28 Condition DS 212A as described in paragraph 4.26.

STEP	ACTION	VERIFICATION
1	<p>Press RST on input keyboard.</p> <p><b>Note:</b> If RST is pressed during a test, the test is ended and the DTS recycles to this step.</p>	<p>Display indicates version number of DTS (921A VERS #02). DTS then performs some self tests. If DTS is defective, a TEST FAILED message appears on display. If DTS is satisfactory, display reads— DATA SET:</p>
2	<p>Enter 36 on input keyboard.</p>	<p>Display reads— DATA SET: 36</p>
3	<p>Press GO.</p>	<p>Display reads— BIT RATE:</p>
4	<p>Enter 03.</p>	<p>Display reads— BIT RATE: 03</p>

STEP	ACTION	VERIFICATION
5	Press GO.	Display reads— TEST SEQ:
6	Enter 52 79.	Display reads— TEST SEQ: 52 79
7	Press GO.	Display reads— PARITY=? (0=EVEN, 1=ODD) Also observe that DTR on 921 DTS lights.
8	Place call to distant end and request the attendant to depress the DL switch on the data set, and go into data mode at both ends.	Verify that RLSD, DSR, and CS on 921 DTS are lighted.
9	Enter 0.	Display reads (briefly)— PARITY=0 (0=EVEN, 1=ODD) Display then reads— TRMT=? (1=MAN 2=CONT)
10	Enter 2.	Display reads (briefly)— TRMT=2 (1=MAN 2=CONT) Display then reads— PRESS A TO START  <b>Note:</b> Ignore display "PRESS A TO START"
11	Press GO.	Display reads (briefly)— TEST INTERRUPTED Display then reads— MODE=? (1=RCV 2=RCV & TRMT)
12	Enter 2.	Display reads (briefly)— MODE=2 (1=RCV 2=RCV & TRMT) Display then reads— HITS OVER??% (MAX=49%)
13	Enter 08.	Display reads (briefly)— HITS OVER 08% (MAX=49%) Display then reads— ??? SECONDS
14	Enter 0060.  <b>Note:</b> To perform functions listed below, press associated key.	Display reads (briefly)— 0060 SECONDS Display then reads— PEAK=XX% HITS=XX/08 AWG BIAS=XX%

**Note:** Initially if the peak reading is greater than 08%, press C to clear the display readings and allow test to continue.

STEP	ACTION	VERIFICATION
KEY	FUNCTION	
A	Repeat test.	After 60 seconds, the display cycles through two messages: PEAK=XX% HITS=XX/00 AVG BIAS=XX% and TEST COMPLETE
B	Display time remaining in test.	
C	Clear display.	
D	End test.	
		<b>Requirement:</b> PEAK=08% MAX HITS=00/08 AVG BIAS=01% MAX

**DL High-Speed Asynchronous Start-Stop Distortion Test—10-Bit Word**

4.30 Make sure the initial test setup using 921 DTS to test DS 212A is followed. Refer to paragraph 4.10.

4.31 Condition DS 212A as follows:

- (1) Verify that options YG and YJ are installed.

(2) Depress HS buttons on the data set. Verify that DS 212A is in the low-speed mode (HS button out for DS 212A-L1 and either HS button out or interface control for DS 212A-L1A) installed. Speed selection is controlled by interface lead CH (pin 23) going low when option XD is installed. Add strap between 10 and 23 of common interface terminal on DTS.

4.32 Perform the test as follows:

STEP	ACTION	VERIFICATION
1	Press RST on input keyboard.  <i>Note:</i> If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display indicates version number of DTS (921A VERS #02). DTS then performs certain self tests. If DTS is defective, a TEST FAILED message appears on display. If DTS is satisfactory, display reads— DATA SET:
2	Enter 36 on input keyboard.	Display reads— DATA SET: 36
3	Press GO.	Display reads— BIT RATE:
4	Enter 12.	Display reads— BIT RATE: 12
5	Press GO.	Display reads— TEST SEQ:
6	Enter 52 79.	Display reads— TEST SEQ: 52 79
7	Press GO.	Display reads— BITS/CHAR=? (0=NINE 1=TEN)
8	Enter 1.	Display reads (briefly)— BITS/CHAR=1 (0=NINE 1=TEN) Display then reads—

STEP	ACTION	VERIFICATION
		PARITY=? (0=EVEN, 1=ODD) Also observe that DTR on 921 DTS lights.
9	Place call to distant end and request the attendant to depress the DL switch on the data set and go into data mode at both ends.	Verify that RLSD, DSR, and CS on 921 DTS are lighted.
10	Enter 0.	Display reads (briefly)— PARITY=0 (0=EVEN, 1=ODD) Display then reads— TRMT=? (1=MAN 2=CONT)
11	Enter 2.	Display reads (briefly)— TRMT=2 (1=MAN 2=CONT) Display then reads— PRESS A TO START  <b>Note:</b> Ignore display "PRESS A TO START"
12	Press GO.	Display reads (briefly)— TEST INTERRUPTED Display then reads— MODE=? (1=RCV 2=RCV & TRMT)
13	Enter 2.	Display reads (briefly)— MODE=2 (1=RCV 2=RCV & TRMT) Display then reads— BITS/CHAR=? (0=NINE 1=TEN)
14	Enter 1.	Display reads (briefly)— BITS/CHAR=1 (0=NINE 1=TEN) Display then reads— HITS OVER??% (MAX=49%)
15	Enter 16.	Display reads (briefly)— HITS OVER 16% (MAX=49%) Display then reads— ???? SECONDS
16	Enter 0060.  <b>Note:</b> To perform functions listed below, press associated key.	Display reads— PEAK=XX% HITS=XX/16 AVG BIAS=XX%

**KEY            FUNCTION**

- A Repeat test.
- B Display time remaining in test.
- C Clear display.
- D End test.
- E Inject errors into data stream.
- F Force out-of-sync condition.

**Note:** Initially if peak reading greater than 16% appears after entering 0060 seconds, momentarily press C to clear display.

**Requirement:** PEAK=15% MAX HITS=00/16  
AVG BIAS=06% MAX

STEP	ACTION	VERIFICATION
		After 60 seconds have elapsed, display reads— TEST COMPLETE; then PEAK=XX% HITS=XX/16 AVG BIAS=XX%
<hr/>		
	<b>DL High-Speed Asynchronous Start-Stop Distortion Test—9-Bit Word</b>	1=TEN), display then reads HITS OVER??% (MAX=49%).
4.33	The 9-bit word test and requirements are the same as the test and requirements for the 10-bit word described in paragraphs 4.31 and 4.32 with the following changes: <ul style="list-style-type: none"> <li>• Install option YI.</li> <li>• Step 8 enter “0” instead of “1”; the display reads briefly: BITS/CHAR=0 (0=NINE 1=TEN), then display reads TRMT=? (1=MAN 2=CONT).</li> <li>• Omit Step 10.</li> <li>• Step 14 enter “0” instead of “1”; the display reads briefly: BITS/CHAR=0 (0=NINE</li> </ul>	<ul style="list-style-type: none"> <li>• Step 15 enter 14 instead of 16; the display reads briefly: HITS OVER 14% (MAX=49%), display then reads ??? SECONDS.</li> </ul>
		<b>DL High-Speed Synchronous Bit Error Test</b>
4.34	Condition data set as follows: <ol style="list-style-type: none"> <li>(1) Verify that option YH is installed.</li> <li>(2) Depress the HS buttons on the data set. Verify that DS 212A is in the low-speed mode (HS button out per DS 212A-L1 and either HS button out or interface control for DS 212A-L1A).</li> </ol>	
4.35	Perform the test as follows:	

STEP	ACTION	VERIFICATION
1	Press RST on input keyboard.  <i>Note:</i> If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display indicates version number of DTS (921A VERS #02). DTS then performs some self tests. If DTS is defective, a TEST FAILED message appears on display. If DTS is satisfactory, display reads— DATA SET:
2	Enter 66 on input keyboard.	Display reads— DATA SET: 66
3	Press GO.	Display reads— BIT RATE:
4	Enter 12.	Display reads— BIT RATE: 12
5	Press GO.	Display reads— TEST SEQ:
6	Enter 55.	Display reads— TEST SEQ: 55
7	Press GO.	Display reads— D=DT Q=SP 1=MK 2=2047 5=511 6=63 Also observe that DTR on 921 DTS lights.

STEP	ACTION	VERIFICATION
8	Enter 5.	Display reads (briefly)— 511 BIT ERROR TEST Display then reads— 1=BIT ERRORS 2=BLOCK ERRORS
9	Place call to distant end and request the attendant to depress the DL switch on the data set and go into data mode at both ends.	Verify that RLSD, DSR, and CS on 921 DTS are lighted.
10	Enter 1.	Display reads— ???? SECONDS
11	Enter 0300.	

**Note 1:** If sync is lost during the test, the right portion of the display will flash OSYN. If this occurs, the test must be restarted by pressing A.

**Note 2:** To perform functions listed below, press associated key.

**KEY            FUNCTION**

- A Repeat test.
- B Display time remaining in test.
- C Clear display.
- D End test.
- E Inject errors into data stream.
- F Force out-of-sync condition.

Display reads (briefly)—  
0300 SECONDS  
Display then reads—  
0000 BITS IN ERROR

After 300 seconds have elapsed, display cycles through three messages:  
TEST COMPLETE;  
00000 SYNC LOSSES; 0000 BITS IN ERROR

**Requirement:** Total errors are less than 12.

**H. End-to-End Test Using 921A DTS**

**4.36** The end-to-end test checks the transmitter and receiver of both data sets and the connecting facility. The customer interface at both data sets is also checked. Identical test data is generated by DTSs at both data sets. This data is transmitted by one of the data sets and compared to the data generated by the DTS at the receiving data set. Data errors are indicated on the DTS counter.

arranged to operate dual mode, perform the test in the speed mode which is causing difficulty.

**ETE Low-Speed Error Test**

**4.38** Make sure the initial test setup using 921 DTS to test DS 212A is followed. Refer to paragraph 4.10.

**4.39** Condition DS 212A as follows:

**4.37** Perform this test at the speed mode used most often by the CPE. If the CPE is

- (1) Verify that option YP is installed at both ends.

(2) Verify that DS 212A is in the low-speed mode (HS button out for DS 212A-L1, and either HS button out or interface control for DS 212A-L1A). Speed selection is controlled by interface lead CH (pin 23) going low when option XD is installed. Add strap between 10 and 23 of common interface terminals on DTS.

4.40 Establish voice communication between data stations and arrange to conduct an end-to-end test. Do not enter data mode until instructed to do so.

4.41 Perform the test as follows:

STEP	ACTION	VERIFICATION
1	Press RST on input keyboard.  <i>Note:</i> If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display indicates version number of DTS (921A VERS #02). DTS then performs some self tests. If DTS is defective, a TEST FAILED message appears on display. If DTS is satisfactory, display reads— DATA SET:
2	Enter 36 on input keyboard.	Display reads— DATA SET: 36
3	Press GO.	Display reads— BIT RATE:
4	Enter 03.	Display reads— BIT RATE: 03
5	Press GO.	Display reads— TEST SEQ:
6	Enter 55.	Display reads— TEST SEQ: 55
7	Press GO.	Display reads— TRANSMITTER=? 1=921 2=914 3=903
8	Enter 1, 2, or 3 to correspond to the type of data test set being used at the distant end.	Display reads (briefly)— TRANSMITTER=1 1=921 2=914 3=903 Display then reads— D=DT 0=SP 1=MK 2=2047 5=511 6=63
9	Enter 5.  <i>Note:</i> If distant end data test set is a 903, enter 6 instead of 5.	Display reads (briefly)— 511 BIT ERROR TEST Display then reads— 1=BIT ERRORS 2=BLOCK ERRORS
10	Enter 1.	Display reads— ???? SECONDS
11	Discuss with far end the length of the test. Then enter data mode at both ends.	
12	Enter 0900.	

STEP	ACTION	VERIFICATION
	<i>Note:</i> To perform functions listed below, press associated key.	
KEY	FUNCTION	
A	Repeat test.	Display reads (briefly)-- 0900 SECONDS
B	Display time remaining in test.	Display then reads-- 0000 BITS IN ERROR
C	Clear display.	From this point, display counts the number of errors. If an out-of-sync condition occurs, display flashes OSYN. If this happens, the test must be restarted by pressing A. At the end of the test, the display indicates test completed total errors.
D	End test.	TEST COMPLETE
E	Inject errors into data stream.	XXXXX SYNC LOSSES
F	Force out-of-sync condition.	XXXXX BITS IN ERROR

**Requirement:** 5 errors or less.

**ETE Low-Speed Stop-Start Distortion**

- 4.42 Connect and condition the 921 DTS per instructions in paragraph 4.10.
- 4.43 Condition DS 212A as follows:
- (1) Verify that option YP is installed.
  - (2) Verify that DS 212A is in the low-speed mode (HS button out for DS 212A-L1 and

either HS button out or interface control for DS 212A-L1A). Speed selection is controlled by interface lead CH (pin 23) going low when option XD is installed. Add strap between 10 and 23 of common interface terminals on DTS.

4.44 Establish voice communication between the data stations and arrange to conduct an end-to-end test.

4.45 Perform test as follows:

STEP	ACTION	VERIFICATION
1	Press RST on input keyboard.  <i>Note:</i> If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display indicates version number of DTS (921A VERS #02). DTS then performs some self tests. If DTS is defective, a TEST FAILED message appears on display. If DTS is satisfactory, display reads-- DATA SET:
2	Enter 36 on input keyboard.	Display reads-- DATA SET: 36
3	Press GO.	Display reads-- BIT RATE:
4	Enter 03.	Display reads-- BIT RATE: 03

STEP	ACTION	VERIFICATION
5	Press GO.	Display reads— TEST SEQ:
6	Enter 52 79.	Display reads— TEST SEQ: 52 79
7	Press GO.	Display reads— PARITY=? (0=EVEN, 1=ODD)
8	Enter 0.	Display reads (briefly)— PARITY=0 (0=EVEN, 1=ODD) then TRMT=? (1=MAN 2=CONT)
9	Enter 2.	Display reads (briefly)— TRMT=2 (1=MAN 2=CONT) Display then reads— PRESS A TO START  <b>Note:</b> Ignore display "PRESS A TO START"
10	Press GO.	Display reads (briefly)— TEST INTERRUPTED then MODE=? (1=RCV 2=RCV & TRMT)
11	Enter 2.	Display reads (briefly)— MODE=2 (1=RCV 2=RCV & TRMT) HITS OVER??% (MAX=49%)
12	Enter 08.	Display reads (briefly)— HITS OVER 08% (MAX=49%) Display then reads— ???? SECONDS
13	Discuss with far end the length of test. Then enter the data mode at both ends.	
14	Enter 0060.  <b>Note:</b> To perform functions listed below, press associated key.	Display reads— PEAK=XX% HITS=XX/08 AVG BIAS=XX%  <b>Note:</b> Initially if the peak reading exceeds 08%, press the C key to clear reading and allow test to continue.

**KEY            FUNCTION**

- A Repeat test.
- B Display time remaining in test.
- C Clear display.
- D End test.

After 60 seconds have elapsed, the display cycles through two messages:  
PEAK=XX% HITS=XX/08 AVG BIAS=XX%  
The display then reads—  
TEST COMPLETE

STEP	ACTION	VERIFICATION
		<b>Requirement:</b> PEAK=08% MAX HITS=00/08 AVG BIAS=01% MAX
15	Upon completion of test, disconnect test equipment and restore data set to pretest condition.	

<b>ETE High-Speed Synchronous Bit Error Test</b>		<b>4.47</b> Establish voice communication with the far end and arrange to conduct an end-to-end test.
<b>4.46</b> Condition data set as follows:		
(1) Verify that option YH is installed.		
(2) Depress the HS buttons on the data set.		<b>4.48</b> Perform the test as follows:

STEP	ACTION	VERIFICATION
1	Press RST on input keyboard.  <b>Note:</b> If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display indicates version number of DTS (921A VERS #02). DTS then performs some self tests. If DTS is defective, a TEST FAILED message appears on display. If DTS is satisfactory, display reads— DATA SET:
2	Enter 66 on input keyboard.  <b>Note:</b> To delete a wrong entry on input keyboard during any test, press back space arrow (←).	Display reads— DATA SET: 66
3	Press GO.	Display reads— BIT RATE:
4	Enter 12.	Display reads— BIT RATE: 12
5	Press GO.	Display reads— TEST SEQ:
6	Enter 55.	Display reads— TEST SEQ: 55
7	Press GO.	Display reads— D=DT 0=SP 1=MK 2=2047 5=511 6=63
8	Enter 5.  <b>Note:</b> If distant end data test set is a 903, enter 6 instead of 5.	Display reads (briefly)— 511 BIT ERROR TEST Display then reads— 1=BIT ERRORS 2=BLOCK ERRORS
9	Enter 1.	Display reads— ???? SECONDS

STEP	ACTION	VERIFICATION
10	Discuss with far end the length of the test. Then enter data mode at both ends.	

11 Enter 0900.

**Note 1:** If sync is lost during the test, the right portion of the display will flash OSYN. If this occurs, the test must be restarted by pressing A.

**Note 2:** To perform functions listed below, press associated key.

**KEY                    FUNCTION**

A	Repeat test.	Display reads (briefly)— 0900 SECONDS
B	Display time remaining in test.	Display then reads— 0000 BITS IN ERROR
C	Clear display.	After the 900 seconds have elapsed, the display cycles through three messages: TEST COMPLETE; XXXXXX SYNC LOSSES; XXXX BITS IN ERROR
D	End test.	
E	Inject errors into data stream.	
F	Force out-of-sync condition.	

**Requirement:** 18 errors or less.

**ETE High-Speed Asynchronous Start-Stop Distortion Test—10-Bit Word**

(2) Depress the HS button on the data set.

4.49 Connect and condition the 921 DTS per instructions in paragraph 4.10.

4.51 Establish voice communications between the data stations and arrange to conduct an end-to-end test.

4.50 Condition data set as follows:

(1) Verify that options YG and YJ are installed.

4.52 Perform the test as follows:

STEP	ACTION	VERIFICATION
1	Press RST on input keyboard.  <b>Note:</b> If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display indicates version number of DTS (921A VERS #02). DTS then performs some self tests. If DTS is defective, a TEST FAILED message appears on display. If DTS is satisfactory, display reads— DATA SET:
2	Enter 36.	Display reads— DATA SET: 36

STEP	ACTION	VERIFICATION
3	Press GO.	Display reads— BIT RATE:
4	Enter 12.	Display reads— BIT RATE: 1200
5	Press GO.	Display reads— TEST SEQ:
6	Enter 52 79.	Display reads— TEST SEQ: 52 79
7	Press GO.	Display reads— BITS/CHAR=? (0=NINE 1=TEN)
8	Enter 1.	Display reads (briefly)— BITS/CHAR=1 (0=NINE 1=TEN) Display then reads— PARITY=? (0=EVEN, 1=ODD)
9	Enter 0.	Display reads— PARITY=0 (0=EVEN, 1=ODD) Display then reads— TRMT=? (1=MAN 2=CONT)
10	Enter 2.	Display reads— TRMT=? (1=MAN 2=CONT) Display then reads— PRESS A TO START
		<b>Note:</b> Ignore display "PRESS A TO START"
11	Press GO.	Display reads (briefly)— TEST INTERRUPTED Display then reads— MODE=? (1=RCV 2=RCV & TRMT)
12	Enter 2.	Display reads— MODE=2 (1=RCV 2=RCV & TRMT) Display then reads— BITS/CHAR=? (0=NINE 1=TEN)
13	Enter 1.	Display reads briefly— BITS/CHAR=1 (0=NINE 1=TEN) Display then reads— HITS OVER??% (MAX=49%)
14	Enter 16.	HITS OVER 16% (MAX=49%) ??? SECONDS
15	Discuss with far-end length of test, then enter date mode at both ends.	

STEP	ACTION	VERIFICATION
16	ENTER 0060.  <i>Note:</i> To perform functions listed below, press associated key.	
	<b>KEY            FUNCTION</b>	
	A Repeat test.	Display reads— PEAK=XX%
	B Display time remaining in test.	HITS=XX/16 AVG BIAS=XX%
	C Clear display.	
	D End test.	
	E Inject errors into data stream.	<i>Note:</i> Initially if peak reading greater than 16% appears after entering 0060 seconds, momentarily press C to clear display.
	F Force out-of-sync condition.	
		After 60 seconds have elapsed, the display reads— TEST COMPLETE Display then reads— PEAK=XX% HITS=XX/16 AVG BIAS=XX%
		<i>Requirement:</i> PEAK=16% MAX HITS=00/16 AVG BIAS=06% MAX

**ETE High-Speed Asynchronous Start-Stop Distortion Test—9-Bit Word**

4.53 The 9-bit word test and requirements are the same as the test and requirements for the 10-bit word described in paragraphs 4.19 and 4.20 with the following changes:

- Install option YI in both data sets.
- Step 8 enter "0" instead of "1"; the display reads BITS CHAR=0 (0=NINE 1=TEN).
- Delete Step 9.
- Step 13 enter "0" instead of "1"; the display reads BITS/CHAR=0 (0=NINE 1=TEN).

- Step 14 enter 14 instead of 16; the display reads HITS OVER 14%.

**I. Automatic Answer Test**

- 4.54 This test checks the ability of the data set to answer a call, go to the data mode and terminate the call.
- 4.55 Connect and condition the 921 DTS per the instructions in paragraph 4.10.
- 4.56 Verify that option ZH (automatic answer-IN) and option U (send-space disconnect-OUT) are installed in DS 212A.
- 4.57 Perform the test as follows:

STEP	ACTION	VERIFICATION
1	Press RST on input keyboard.  <i>Note:</i> If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display indicates version number of DTS (921A VERS #02). DTS then performs certain self tests. If DTS is defective, a TEST FAILED message appears on display. If DTS is satisfactory, display reads— DATA SET:
2	Enter 36 on input keyboard.	Display reads— DATA SET: 36

STEP	ACTION	VERIFICATION
3	Press GO.	Display reads— BIT RATE:
4	Enter 03.	Display reads— BIT RATE: 03
5	Press GO.	Display reads— TEST SEQ:
6	Enter 40.	Display reads— TEST SEQ: 40
7	Press GO.	Display reads— WAITING FOR RI
8	Have a call made to the data set.	Display reads— RINGING (during ringing period). Assignable L1 follows the RI lead. After 3 or 4 rings, the DTR lead turns on and the DTR indicator lights. After 7 seconds, DSR indicator lights (data set ready lead <b>on</b> ). Display then reads— ANSWERED After approximately 2.5 seconds, the DTR indicator goes off (data terminal ready lead <b>off</b> ). After 1 more second, DSR indicator goes off (data set ready lead <b>off</b> ).  <b>Requirement:</b> If all of the above events occur, the display reads briefly— TEST PASSED followed by TEST COMPLETE. If any of the above events fail to occur, the display reads— TEST FAILED.

**J. Interface Test**

**4.58** This test checks the ability of the data set to respond to interface control and to provide indications through the interface. The signals which the data set will respond to and the indications given depend on the options installed. In this test, the DS 212A interface is checked using a 921 DTS. Some of these tests require assistance from the data test center (DTC).

**4.59 Test of CN Circuit:** This test checks the ability of the local data set to go into

the analog loop mode under control of the CN interface lead.

**4.60** Connect and condition the 921 DTS per the instructions in paragraph 4.10.

**4.61** Verify that option YE (CN circuit-IN) is installed.

**4.62** Perform the test as follows:

STEP	ACTION	VERIFICATION
1	Connect jumper wires on interface lead jacks:  For DS 212A-L1 or DS 212A-L1A with option XO installed—jumper 4 to 25.  For DS 212A-L1A with option XN installed—jumper 4 to 18.  For DS 212A-L1A with option XR installed—jumper 4 to 18 and 13 to 25.	
2	Press RST on input keyboard.  <b>Note:</b> If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display indicates version number of DTS (921A VERS #02). DTS then performs some self tests. If DTS is defective, a TEST FAILED message appears on display. If DTS is satisfactory, display reads— DATA SET:
3	Enter 36 on input keyboard.	Display reads— DATA SET: 36
4	Press GO.	Display reads— BIT RATE:
5	Enter 03.	Display reads— BIT RATE: 03
6	Press GO.	Display reads— TEST SEQ:
7	Enter 47 48 37.	Display reads— TEST SEQ: 47 48 37 Display then reads— :37 DTR=? (0 OR 1)
8	Enter 0.	Display reads— TEST SEQ: DTR=0 (0 OR 1)
9	Enter 38.	Display reads— TEST SEQ: 37 DTR=0 (0 OR 1) 38
10	Press GO.	Display reads (briefly)— TEST COMPLETE Display then reads— SW CONN: X=?? Y=??
11	Enter 05.	Display reads— SW CONN: X=05 Y=??
12	Enter 09.	Display reads (briefly)— SW CONN: X=05 Y=09

STEP	ACTION	VERIFICATION
		Display then reads— SW CONN: X=?? Y=??
13	Enter 16.	Display reads— SW CONN: X=16 Y=??
14	Enter 10.	Display reads (briefly)— SW CONN: X=16 Y=10 Display then reads— SW CONN: X=?? Y=??
15	Enter 11.	Display reads— SW CONN: X=11 Y=??
16	Enter 08.	Display reads (briefly)— SW CONN X=11 Y=08 Display then reads— SW CONN: X=?? Y=??
17	Press GO.  <i>Note:</i> S1 is controlled by input key Number 1; S2 is controlled by input key Number 2; S3 is controlled by input key Number 3. S4 is controlled by input key Number 4.	Display reads— TEST INTERRUPTED CROSS CONNECTIONS MANUALLY SET TEST COMPLETE CROSS CONNECTIONS MANUALLY SET The display then indicates the state of the assigned switches. S1=OFF S2=OFF S3=ON S4=ON
18	Press 1.	Display reads— S1=ON S2=OFF S3=ON S4=ON  <i>Requirement:</i> MB indicator lights on DS 212A.
19	Press 2.	Display reads— S1=ON S2=ON S3=ON S4=ON  <i>Requirement:</i> RLSD lights followed momentarily by CS lighting.  <i>Note:</i> If option XR is installed, observe that assignable L4 indicator lights.

**4.63 Test of Receive Space Disconnect**

*Feature:* This test checks the ability of the data set to disconnect (go on-hook) upon receiving a space signal from the distant data set.

**4.64** Connect and condition the 921 DTS per the instructions in paragraph 4.10.

**4.65** Verify that option V (receive space disconnect-IN) is installed.

**4.66** Perform the test as follows:

STEP	ACTION	VERIFICATION
1	Press RST on input keyboard.  <i>Note:</i> If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display indicates version number of DTS (921A VERS #02). DTS then performs certain self tests. If DTS is defective, a TEST FAILED message appears on display. If DTS is satisfactory, display reads— DATA SET:
2	Enter 36 on input keyboard.	Display reads— DATA SET: 36
3	Press GO.	Display reads— BIT RATE:
4	Enter 03.	Display reads— BIT RATE: 03
5	Press GO.	Display reads— TEST SEQ:
6	Enter 37.	Display reads— TEST SEQ: 37 DTR=? (0 OR 1)
7	Enter 1.	Display reads— TEST SEQ: 37 DTR=1 (0 OR 1)
8	Press GO.	Display reads— TEST SEQ:
9	Place call to DTC. Have the DTC place a call to the local data set; enter low-speed data mode; send approximately 10 seconds of spacing and then send at least 4 seconds of spacing.	
10	Answer the call. If option ZG (automatic answer-OUT) is installed, answer the call, go to the data mode, and place the handset on-hook.	On 921 DTS, verify that DSR indicator lights and shortly thereafter RLSD and CS indicators light.
11	When the DTC sends spacing.	Observe that RD-0 indicator lights and approximately 1-1/2 seconds later RLSD, DSR, and CS go off (data set drops call).

**4.67 Test of CB and CF Indications Option:**

When option A (CB and CF indications—COMMON) is selected, the clear-to-send (CB) interface circuit is forced *off* whenever the received line signal detector (CF) interface circuit goes *off*. This test checks proper operation of this feature.

**4.68** Connect and condition the 921 DTS per the instructions in paragraph 4.10.

**4.69** Verify that option A (CB and CF indications—COMMON) and option R (loss of carrier disconnect-OUT) are installed.

**4.70** Perform the test as follows:

STEP	ACTION	VERIFICATION
1	Press RST on input keyboard.  <i>Note:</i> If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display indicates version number of DTS (921A VERS #02). DTS then performs certain self tests. If DTS is defective, a TEST FAILED message appears on display. If DTS is satisfactory, display reads— DATA SET:
2	Enter 36 on input keyboard.	Display reads— DATA SET: 36
3	Press GO.	Display reads— BIT RATE:
4	Enter 03.	Display reads— BIT RATE: 03
5	Press GO.	Display reads— TEST SEQ:
6	Enter 37.	Display reads— TEST SEQ: 37 DRT=? (0 OR 1)
7	Enter 1.	Display reads— TEST SEQ: 37 DTR=1 (0 OR 1)
8	Press GO.	Display reads (briefly)— TEST COMPLETE Display then reads— TEST SEQ:
9	Place call to DTC and request the DTC to place a call to the local data set in the low-speed mode.	
10	Answer the call. If option ZG (automatic answer-OUT) is installed, answer the call, go to the data mode, and place the handset on-hook.  <i>Note:</i> The DTC should go to the data mode after receiving answer tone.	On 921 DTS, verify that DSR indicator lights and shortly thereafter RLSD and CS indicators light.
11	Have DTC go into data mode and then from the data mode to the talk mode without dropping the call (or go from TEST to TALK on 904 DTC).	Observe that RLSD and CS indicators go off and DSR remains lighted. Display reads— TEST COMPLETE

**4.71 Test of Carrier Fail Disconnect**

**Option:** When option S (loss of carrier disconnect-IN) is selected, the data set terminates the call if carrier disappears from the line for approximately 350 ms.

**4.73** Verify that option S (loss of carrier disconnect-IN) is installed.

**4.74** Perform the test as follows:

**4.72** Connect and condition the 921 DTS per the instructions in paragraph 4.10.

STEP	ACTION	VERIFICATION
1	Press RST on input keyboard.  <b>Note:</b> If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display indicates version number of DTS (921A VERS #02). DTS then performs certain self tests. If DTS is defective, a TEST FAILED message appears on display. If DTS is satisfactory, display reads— DATA SET:
2	Enter 36 on input keyboard.	Display reads— DATA SET: 36
3	Press GO.	Display reads— BIT RATE:
4	Enter 03.	Display reads— BIT RATE: 03
5	Press GO.	Display reads— TEST SEQ:
6	Enter 37.	Display reads— TEST SEQ: 37 DTR=? (0 OR 1)
7	Enter 1.	Display reads— TEST SEQ: 37 DTR=1 (0 OR 1)
8	Press GO.	Display reads (briefly)— TEST COMPLETE Display then reads— TEST SEQ:
9	Place call to DTC and request the DTC to place a call to the local data set in the low-speed mode.	
10	Answer the call. If option ZG (automatic answer-OUT) is installed, answer the call, go to the data mode, and place the handset on-hook.  <b>Note:</b> The DTC should go to the data mode after receiving answer tone.	On 921 DTS, verify that DSR indicator lights and shortly thereafter RLSD and CS indicators light.

STEP	ACTION	VERIFICATION
11	Have DTC go from the data mode to the talk mode without dropping the call (or go from TEST to TALK on 904 DTC).	RLSD and CS indicators go off immediately. DSR indicator goes off in approximately 350 ms or is delayed for approximately 4 seconds if option T is installed.

- 4.75 Test of Speed Mode Option:** When the data set is equipped with option YO (speed mode-HIGH), the data set will not pass data through the interface when in the low-speed mode. This test checks that low-speed data is blocked at the interface.
- 4.76** Connect and condition the 921 DTS per the instructions in paragraph 4.10.
- 4.77** Condition the data set as follows:
- (1) Verify that option YO (speed mode-HIGH) is installed.
  - (2) Depress the AL and HS buttons on the data set.
- 4.78** Perform the test as follows:

STEP	ACTION	VERIFICATION
1	Press RST on input keyboard.  <i>Note:</i> If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display indicates version number of DTS (921A VERS #02). DTS then performs certain self tests. If DTS is defective, a TEST FAILED message appears on display. If DTS is satisfactory, display reads— DATA SET:
2	Enter 36 on input keyboard.	Display reads— DATA SET: 36
3	Press GO.	Display reads— BIT RATE:
4	Enter 03.	Display reads— BIT RATE: 03
5	Press GO.	Display reads— TEST SEQ:
6	Enter 53 37.	Display reads— 53 37 DTR=? (0 OR 1)
7	Enter 1.	Display reads (briefly)— 53 37 DRT=1 (0 OR 1) Display then reads— :
8	Press GO.	Display reads (briefly)— SELECT ERROR TEST Display then reads— D=DT 0=SP 1=MK 2=2047 5=511 6=63
9	Press D.	Display reads— DOTTING BIT ERROR TEST

STEP	ACTION	VERIFICATION
10	Press GO.	Display reads (briefly)— TEST INTERRUPTED Display then reads— TEST COMPLETE Display then reads— TEST SEQ:  On 921 DTS, verify that indicators RLSD and CS light steadily and both SD and RD are flashing.
11	Release the HS button on DS 212A.	On 921 DTS, verify that indicators RLSD and CS go off and SD continues flashing. RD-1 is <b>on</b> and RD-0 is <b>off</b> .

**4.79 Test of Interface Speed Control Option (DS 212A-L1A Only):** When option XJ (interface) is selected, it enables high-speed or low-speed operation of an originating data set to be controlled through pin 23 of the customer's interface.

- 4.81** Condition the data set as follows:
- (1) Verify that option XJ (interface) is installed.
  - (2) Depress the AL button on the data set.

**4.80** Connect and condition the 921 DTS per instructions in paragraph 4.10.

**4.82** Perform the test as follows:

STEP	ACTION	VERIFICATION
1	Connect a jumper wire on common interface lead jack between 20 and 23.	
2	Press RST on input keyboard.  <i>Note:</i> If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display indicates version number of DTS (921A VERS #02). DTS then performs certain self tests. If DTS is defective, a TEST FAILED message appears on display. If DTS is satisfactory, display reads— DATA SET:
3	Enter 36 on input keyboard.	Display reads— DATA SET: 36
4	Press GO.	Display reads— BIT RATE:
5	Enter 12.	Display reads— BIT RATE: 12
6	Press GO.	Display reads— TEST SEQ:
7	Enter 47 48 37.	Display reads— :37 DTR=? (0 OR 1)

STEP	ACTION	VERIFICATION
8	Enter 1.	Display reads— TEST SEQ: 37 DTR=1 (0 OR 1)
9	Press GO.	Display reads (briefly)— TEST COMPLETE— Display then reads— SW CONN: X=?? Y=??  Observe that the HS indicator on the data set and assignable LED #1 on DTS are lighted.
10	Enter 10.	Display reads— SW CONN: X=10 Y=??
11	Enter 05.	Display reads (briefly)— SW CONN: X=10 Y=05
12	Press GO.	Display reads (briefly)— TEST INTERRUPTED Display then reads— CROSS CONNECTIONS MANUALLY SET Display then reads— TEST COMPLETE Display then reads— CROSS CONNECTIONS MANUALLY SET Display then reads— TEST SEQ: Observe that the HS indicator and assignable LED #1 go off. Test complete.

**K. Ground Noise Test**

**4.83 Signal Ground to Frame Ground**

**Connection:** When option Q is selected, (signal ground) interface lead is connected to frame ground. This arrangement provides additional margin against longitudinal power line noise. When option P is selected, the AB (signal ground) interface lead is disconnected from the frame ground. Due consideration should be given to possible noise conditions, ground potential differences, safety conditions, local electrical codes, and the data terminal manufacturer's recommendations.

**4.84** If the data set and CPE are not connected to the same ground, errors may be caused by a potential difference between data set ground and CPE ground. To detect the presence of noise potentials, a test should be made using the 6-type impulse counter. This counter is used to count the number of impulse noise peaks during a

measured time period. The counter registers only the peaks which exceed a preset level and which are separated by approximately 150 ms or more.

**4.85** Test equipment required for this test is as follows:

- 1—6H impulse counter (or equivalent)
- 1—921-type DTS
- 1—2W6A test cord for 6H impulse counter (310 plug on one end, alligator clips connected to tip and ring on the other end).

**Note:** For information pertaining to the 6H impulse counter, refer to the section entitled 6H and 6HR Impulse Counters (J94006H and J94006HR)—Description, Operation, and Maintenance (103-620-101). If the 6H impulse counter is not available, a 6A impulse counter

may be used. For information pertaining to the 6A impulse counter, refer to the section entitled J94006A (6A) Impulse Counter—Description, Operation, and Maintenance (103-620-100).

**4.86** In this test, the impulse counter is connected between the grounds of the data set and the CPE. The counter registers when potential differences of sufficient amplitude have developed between the separated grounds. The 921 DTS is used to gain access to the ground interface leads. If a 921-type DTS is not available, any suitable method of access (such as 901 test adapter) may be used.

**4.87** The 6H impulse counter is connected and the test is performed as follows:

- (1) Connect the 921 DTS DCE connector to the customer connector on the data set. Connect the 921 DTS DTE connector to the data set connector on the CPE. This test assumes that protective ground from the CPE appears at the customer interface.
- (2) On the 921 DTS, open all interface switches.
- (3) Connect one clip to the 2W6A cord to terminal 1 interface lead jack and the other clip to any clear, bare metal on the data set housing. Verify that power is applied to data set and CPE.
- (4) Insert the 310 plug into the 310 MEAS jack on the 6H impulse counter.
- (5) On the 6H impulse counter, set the DIAL-MEAS switch to MEAS and set the DBRN dial to 90.
- (6) Reset the counter on the 6H impulse counter to 0.
- (7) Set the minutes control to 15. After the 15-minute test has elapsed, record the number of indications on the counter.
- (8) Remove clips of 2W6A cord and connect to the terminal on the interface lead jack corresponding to terminal 7 of the CPE interface and terminal 7 of the data set interface.

(9) Reset the counter on the 6H impulse counter to 0.

(10) Set the minutes control to 15. After the 15-minute test has elapsed, record the number of indications on the counter.

**4.88** At the end of both of the 15-minute periods, there should be no indications on the counter of the 6H impulse counter. If there is an indication on the counter, the grounds must be bonded together according to local instructions. At the end of the test, disconnect the test equipment and restore the data set to pretest condition.

## 5. REFERENCES

**5.01** Additional information concerning the testing of DS 212A is contained in the following publications:

SECTION	TITLE
107-402-100	921A Data Test Set—Description and Operation
314-205-501	Data Systems—DATAPHONE® Service and Data Access Arrangements on Direct Distance Dialing Network—Test Requirements for Subscriber, Foreign Exchange, and Remote Exchange Lines
314-410-500	Voice Bandwidth Private Line Data Circuits—Tests and Requirements
592-034-100	Data Set 212A—Transmitter-Receiver—Description and Operation
592-034-200	Data Set 212A—Transmitter-Receiver—Installation and Connections
592-034-500	Data Set 212A—Transmitter-Receiver—Test Procedures Using 914-Type Data Test Set
666-511-501	Test of Data Services Provided by Data Set 201C From a Private Line Testroom

<b>SECTION</b>	<b>TITLE</b>	
668-010-300	Data Systems—DATAPHONE® Service on Direct Distance Dialing Network—Data Test Center— Trouble Analysis Procedures	<b>5.02</b> Detailed information concerning DS 212A is contained in CD- and SD-1D239-01.
999-100-138	Data Set 201C—How to Operate Manual	