48230 LOCAL AREA DATA SET

DESCRIPTION

1. GENERAL

1.01 This section covers the 48230 Local Area Data Set manufactured by Codex Corporation.

1.02 Whenever this section is reissued, the reason(s) for reissue will appear in this paragraph.

1.03 A description of the Local Area Data Set is contained in the attached reprint of the practice prepared by Codex Corporation.

1.04 Installation and connection procedures and maintenance and test procedures are covered in Sections 592-035-200 and 592-035-300, respectively.

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LOCAL AREA DATA SET
(48230)
DESCRIPTION

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PART NO. 05299, Rev B

1.0 GENERAL

1.01 The Codex 48230 and 48234 Local Area Data Sets (LADS), shown in Figures 1-1A and 1-1B, provide data transmission over unloaded, unconditioned telephone company local loops at selectable rates of 2400, 4800, 7200, 9600, and 19200 bits per second (bps). These synchronous data sets accommodate 4-wire full-duplex configurations (see Figure 1-2).

1.02 The LADS incorporates differential diphase modulation which provides immunity from background noise, and normally-encountered line distortion and parameter variation. Transmit timing is provided internally or derived externally from the data terminal. Receive timing is data-derived and utilizes a decision-directed feedback-recovery technique which eliminates potential data pattern sensitivities. A loopback timing mode is selectable in which timing for the entire link is derived from an external clock at the other end of the link.

1.03 The transmit output level is selectable in seven steps (installer optioned) from -20 to +3 dBm. Compatibility with the Bell System power-versus-frequency restrictions for private line metallic circuits is guaranteed by the proper transmit level option which is selected according to the data rate. Proper selection is determined as follows:

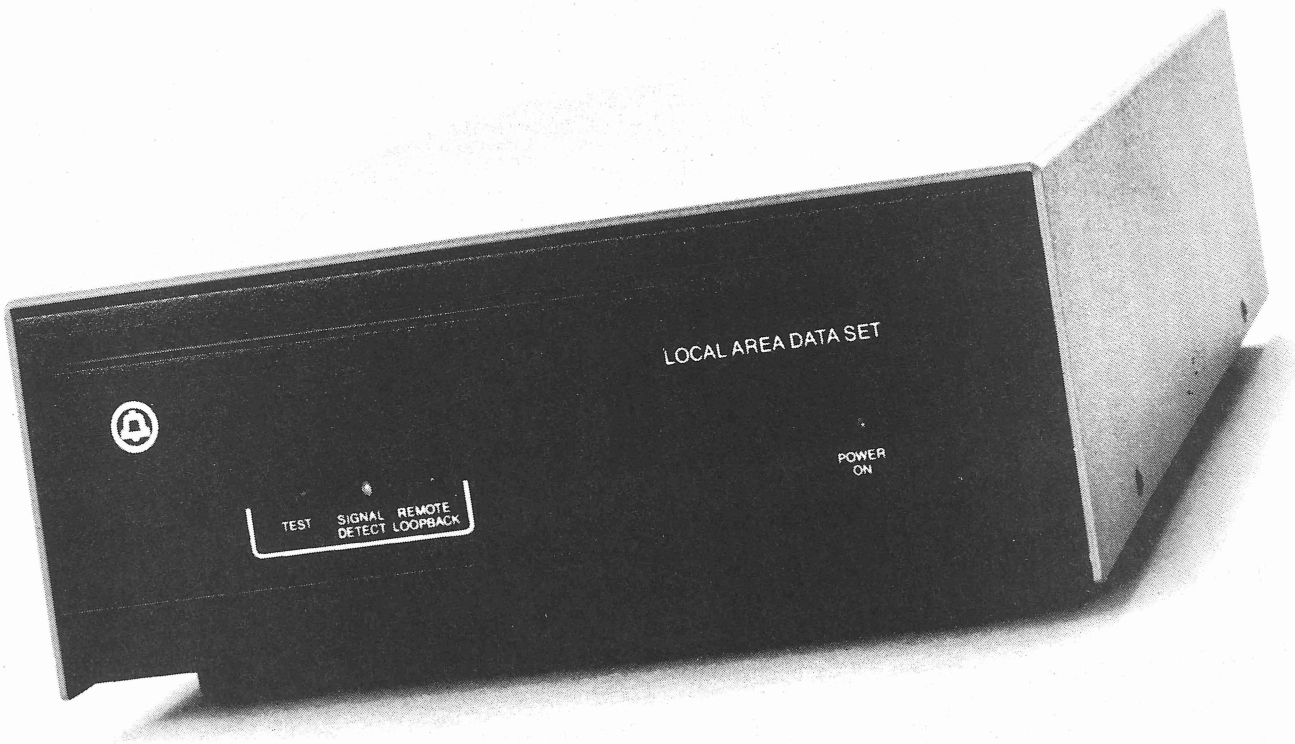

Figure 1-1A. Local Area Data Set 48230

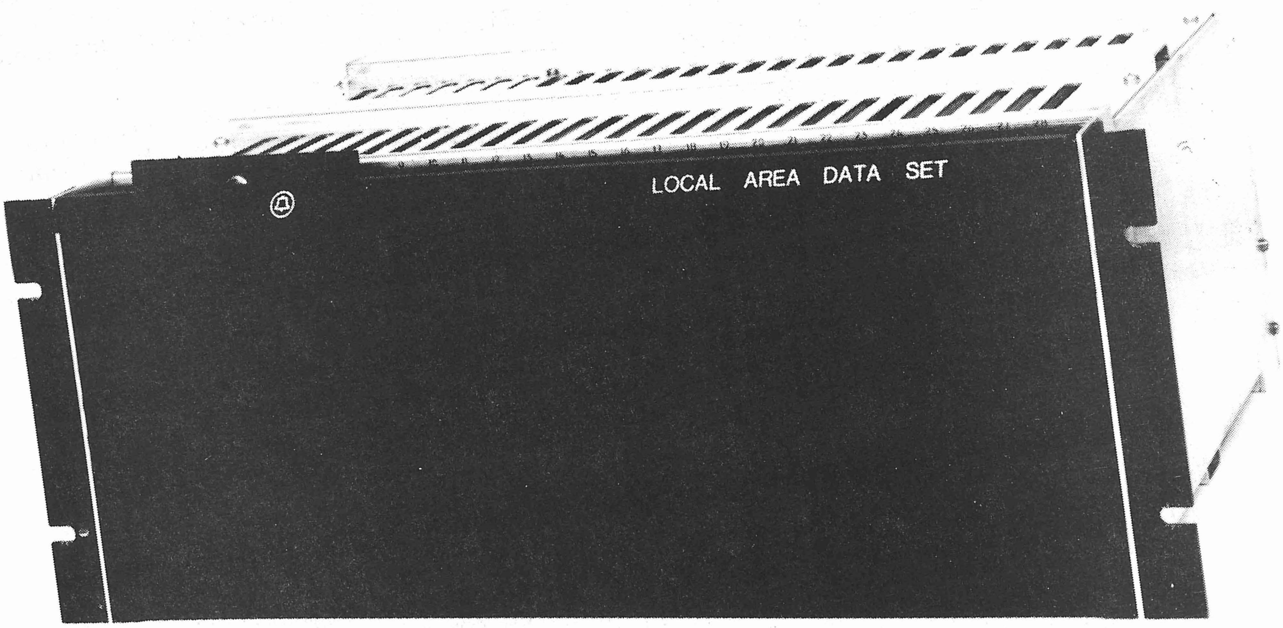

Figure 1-1B. Multiple Nest Assembly 48234

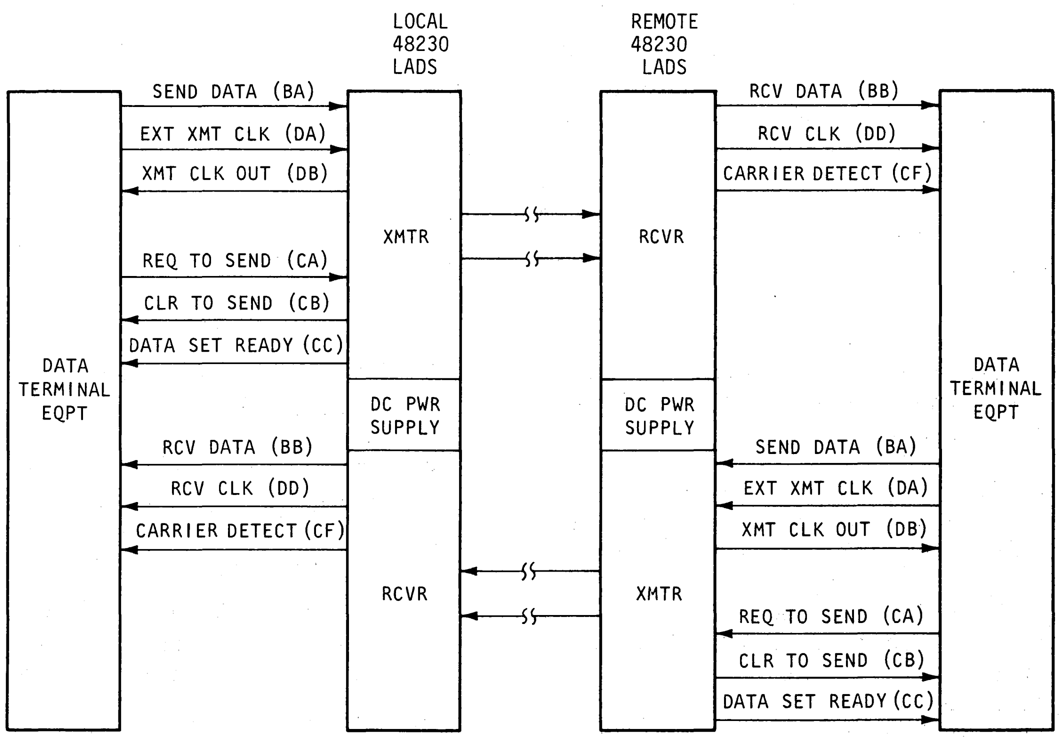

Figure 1-2. Typical 4-Wire System Application

Data Rate (bps)	Proper Output Power (dBm) Option Selection
2400	0
4800	-6
7200	-12
9600	-16
19200	-20

1.04 Equalization is accomplished through the use of a compromise equalizer. Integral test features help the operator to determine system performance and isolate faults in the communication link.

2.0 PHYSICAL DESCRIPTION

2.01 The LADS has a removable cover which allows access to the interior. Signal line and interface connectors and the ac line fuse are located on the rear panel. An integral 3-wire power cord and plug connects to a grounded 115 Vac power source. Equipment provided is listed in Table 2-1.

2.02 No switches are available on the front panel; only system status and mode indicators are present. This prevents the accidental depressing of any test switch.

TABLE 2-1. EQUIPMENT SUPPLIED

Item Name	Codex Part No.
Receive Card (A1)	34187
Transmit Card (A2)	34506
Power Supply Card	34204
Backplane Assembly	34021G1

A swing-down panel provides access to the test switches. The status lamps are visible through the front panel.

2.03 The receive and transmit circuit cards (A1 and A2) are horizontally-mounted and plug in to the vertically-mounted power and signal distribution board (backplane). A replaceable regulated dc power supply card is vertically mounted, front to rear, at the right side of the cabinet. The power supply accepts 115 volts ac. The supply furnishes regulated ±6.5 Vdc and unregulated 24 Vdc remote loopback voltage, and contains the 3.6864 MHz crystal oscillator for internal timings. Refer to Figure 2-1 for card locations.

TECHNICAL DATA

2.04 DIMENSIONS AND WEIGHT

a. Overall Dimensions:
48230 - 9-3/4" wide by 3-7/8" high by 13-5/16" deep.
48234 - 19" wide by 7" high by 15" deep.

b. Weight:
48230 - 8-3/4 lbs.
48234 - 28 lbs.

2.05 ENVIRONMENTAL CONDITIONS

a. Temperature: 0 to +50°C.

b. Altitude: 0 to 10,000 feet.

c. Relative Humidity: 5 to 95%.

2.06 PRIMARY POWER

a. Power: 115 Vac ±10%, 47 to 63 Hz.
48230 - 6 watts maximum.
48234 - 20 watts maximum.

b. Fuses:
48230 - 0.1 Amp.
48234 - 0.6 Amp, Slo-Blo.

2.07 TELEPHONE LINES

Refer to B.S.P. 314-410-311 and B.S.P. 314-410-312.

2.08 INTERFACE

a. EIA RS-232-C.

b. Pulse trains or square wave inputs and outputs at +6.5 volts, with a maximum frequency of 19,200 Hz (9600 maximum supported data rate).

2.09 DATA AND SIGNALING RATES

The standard data rates of the LADS are 2400, 4800, and 9600 bits per second.

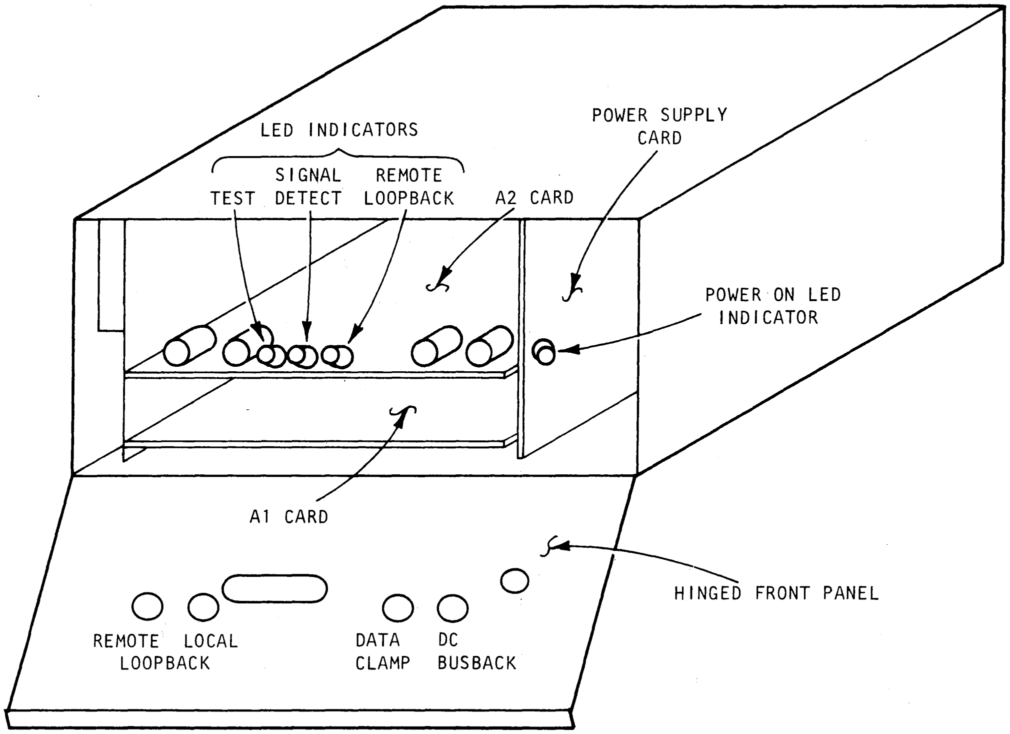

Figure 2-1. LADS Control/Indicator Locations

The LADS employs a baud line signaling rate equal to the data rate and utilizing differential diphase modulation.

OPERATING LEVELS

2.10 TRANSMIT OUTPUT LEVEL

The output power level is strap-selectable, as described in paragraph 1.03, as a function of data rate.

2.11 RECEIVER AGC RANGE

The receiver features a wide dynamic range AGC circuit of 50 dB, with a single compromise equalizer requiring no adjustments.

2.12 TIMING

a. An internal 3.6864 MHz crystal oscillator assembly, having a long term stability of 20 parts per million per year, is used as a reference.

b. External timing accuracy, EIA RS-334.

3.0 FUNCTIONAL DESCRIPTION

3.01 This chapter contains simplified functional descriptions of the Local Area Data Set, its transmitter, and receiver. These descriptions are keyed to the LADS functional block diagram, Figure 3-1.

3.02 The transmitter contains the traditional elements of any modem transmitter, with the addition that the clocks normally utilized are internally-derived but may be switched to externally-derived (from the data terminal equipment), or to data-derived (from the received data) for maintenance loopback conditions. The receiver contains a wide dynamic range front end whose AGC loop encompasses the receive filter and equalizer. Because no line conditioning or signal level management is present on wire pairs as it would in a standard VF telephone channel, the dynamic range requirement is greater than for a typical voice band modem. (The combination of transmitter output level variations and

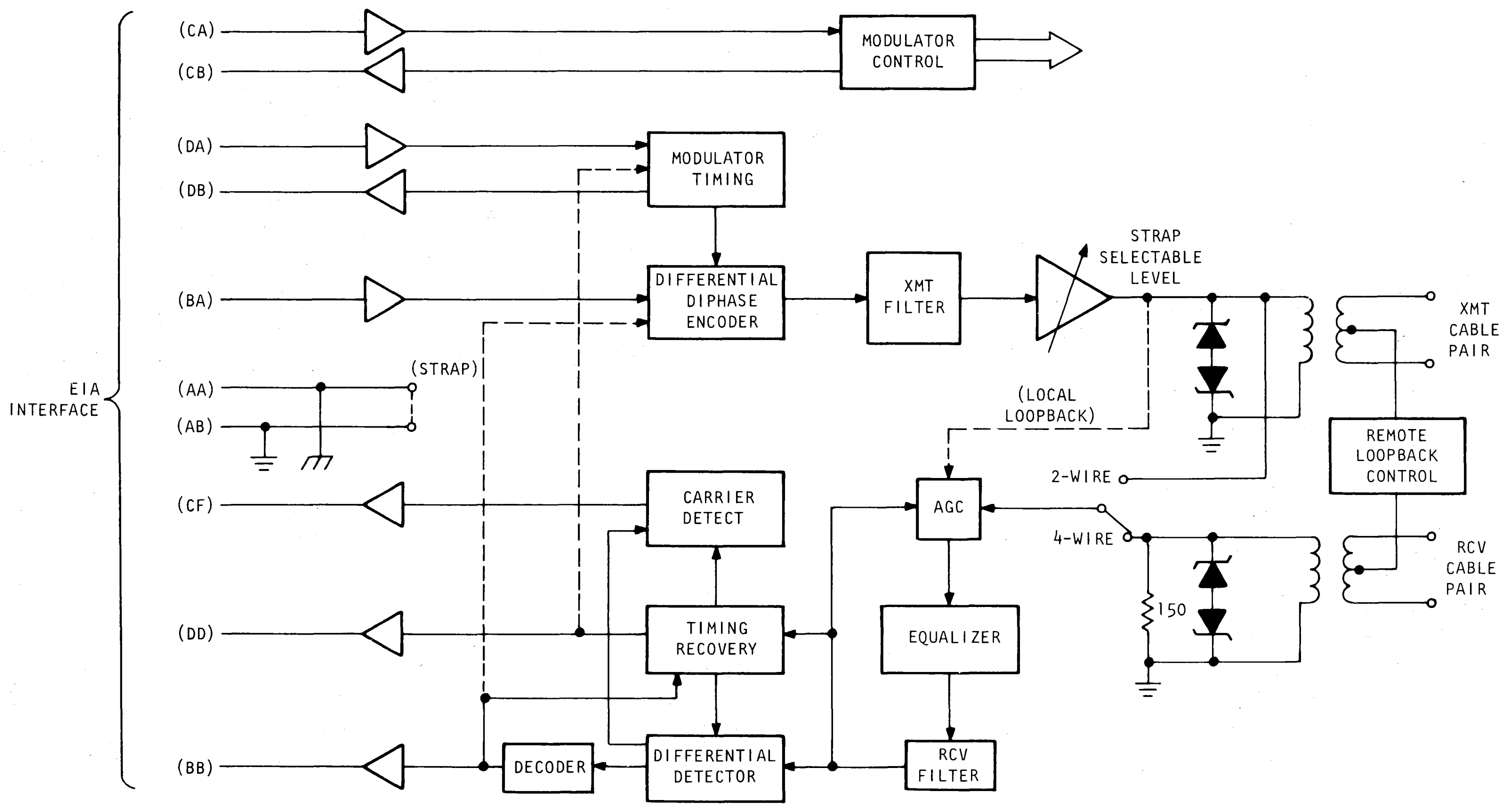

Figure 3-1. LADS Functional Block Diagram

the expected range of signal losses result in input signal variations of more than 60 dB.) The data recovery block is a coherent PSK detector, and the data decoder is a simple differential decoder. The clock recovery and signal presence contain some unique circuitry discussed later in this chapter.

3.03 Operation of the LADS is discussed in three parts: transmitter, receiver, and power supply. The transmitter discussion consists of modulation timing, modulation control, modulation, and filtering. The receiver discussion includes AGC and equalization, demodulation, clock recovery, and signal presence detection.

TRANSMITTER

3.04 MODULATION TIMING

Timing for the LADS is synchronized to the internal clock (115.2 kHz, derived from the 3.6864 MHz crystal oscillator on the power supply card of the LADS) or by an External Clock (DA) furnished by the data terminal. The choice of internal or external clock is strap-selectable. A loopback timing mode is available as a third timing alternative. Loopback timing is also strap-selectable and offers timing derived from the Receive Data source (DD) from the other (master) end of the link. The loopback timing feature allows one master clock to control the timing for the entire link. This is especially helpful when the master LADS is in external timing.

3.05 MODULATION CONTROL

Modulation control is determined prior to system operation by the strap-selectable choices of DX MODE and CARR CONT. Modulation is controlled by the following sets of conditions.

a. Full-Duplex, Carrier On. This mode allows simultaneous transmission and reception of data on 4-wire circuits. Clear to Send (CB) goes high after a selectable delay (0, 8, 16 ms) when CA is raised, and the carrier is transmitted on to the line at all times when power is on except when the LADS is in LOCAL LOOPBACK.

3.06 MODULATION

Modulation consists of a differential encoding of the Mark/Space input data and binary PSK modulation of a square wave carrier with the encoded data, where the carrier frequency is identically equal to the bit and baud frequencies.

3.07 Incoming data (BA) is clocked in and differentially encoded at the baud rate. The encoded data is Exclusive-OR'ed with the baud rate clock to produce the diphase signal input to the transmitter filter networks. These operations are shown in the waveforms of Figure 3-2.

3.08 The diphase signal is applied to the transmit filter networks (filtering levels are dependent upon the strap-selectable data rate), the strap-selectable output level circuit, and, in turn, the telephone lines, via the output transformer.

FILTERING

3.09 The selection of filters for the LADS is in compliance with Bell System voltage-versus-frequency restrictions on transmitter output, noise rejection in the receiver, and minimization of intersymbol interference at arbitrary cable lengths.

RECEIVER

3.10 Incoming data from the 150-ohm receive telephone line passes through an impedance-matching receiver input transformer and buffer amplifier to the automatic gain control (AGC) circuit. The AGC output passes through the receive portion of the filter network to the equalizer circuit.

EQUALIZATION

3.11 The equalizer provides a compromise between short range and long range operation so that setup adjustments and end-to-end coordination during installation are not required. A single compromise equalizer is successful in the LADS because of the superior intersymbol interference rejection characteristics of the diphase modulation/differential detection implementation.

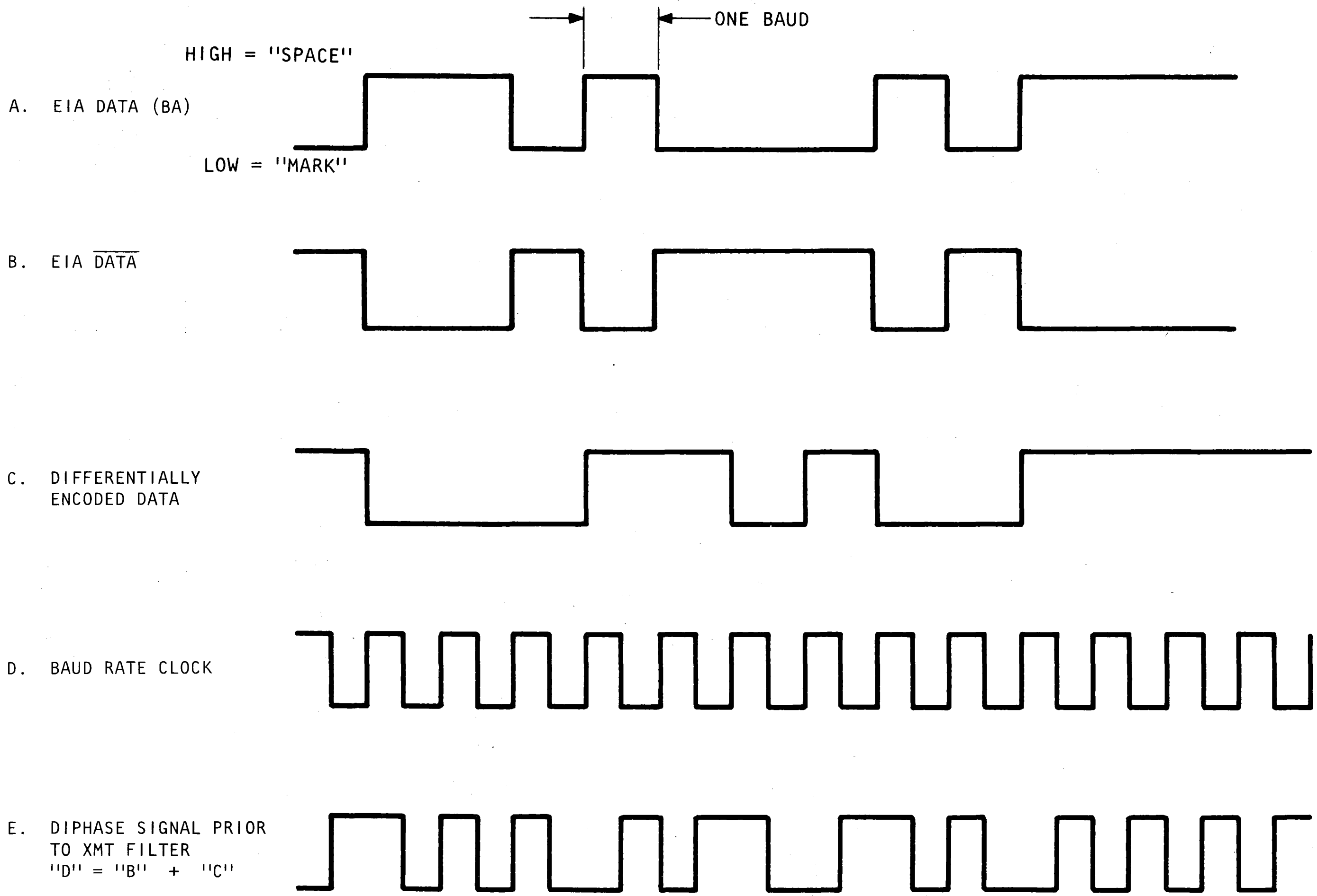

Figure 3-2. Generation of Differential Diphase Signal

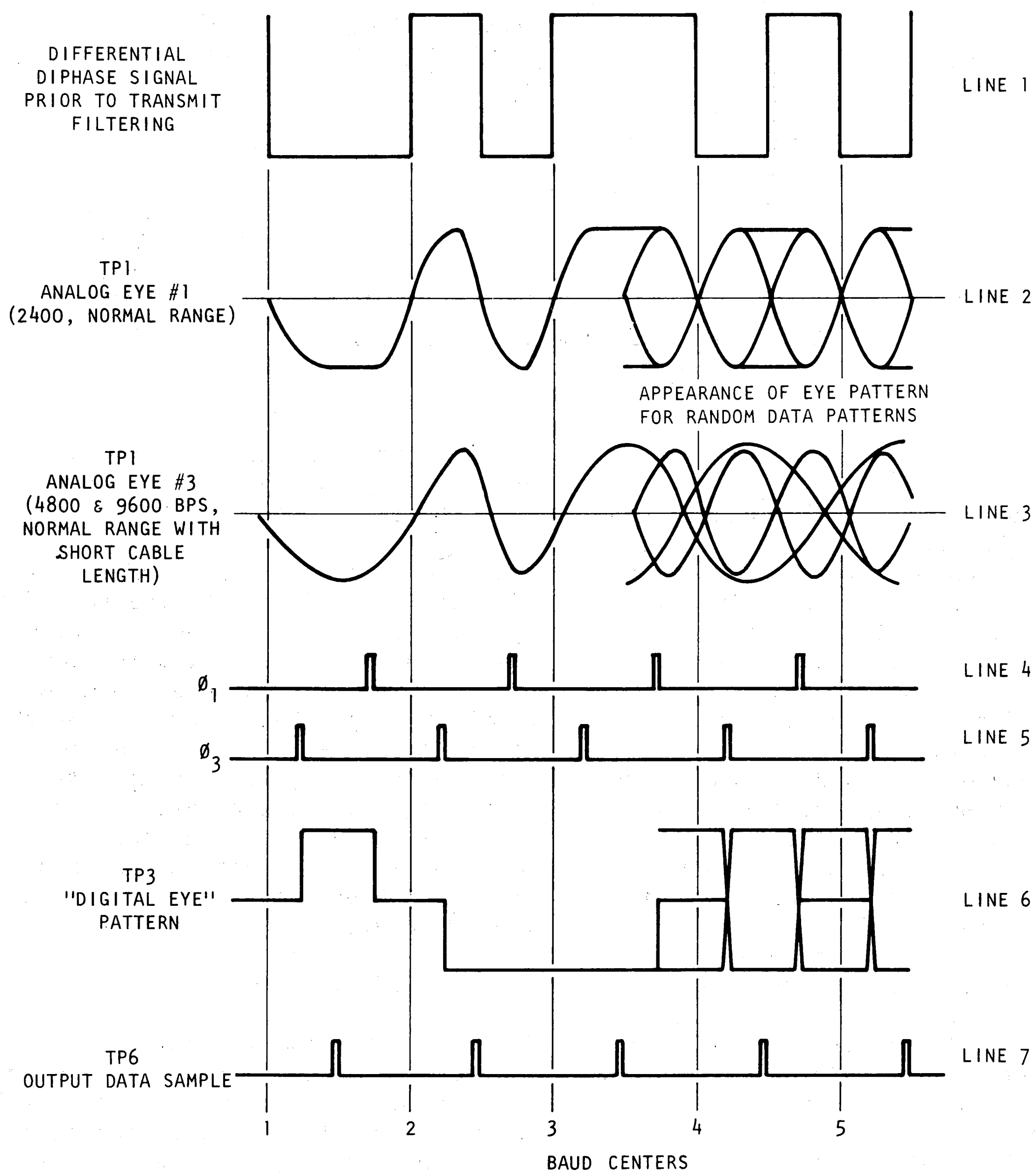

Figure 3-3. Codex LADS Receiver Waveforms

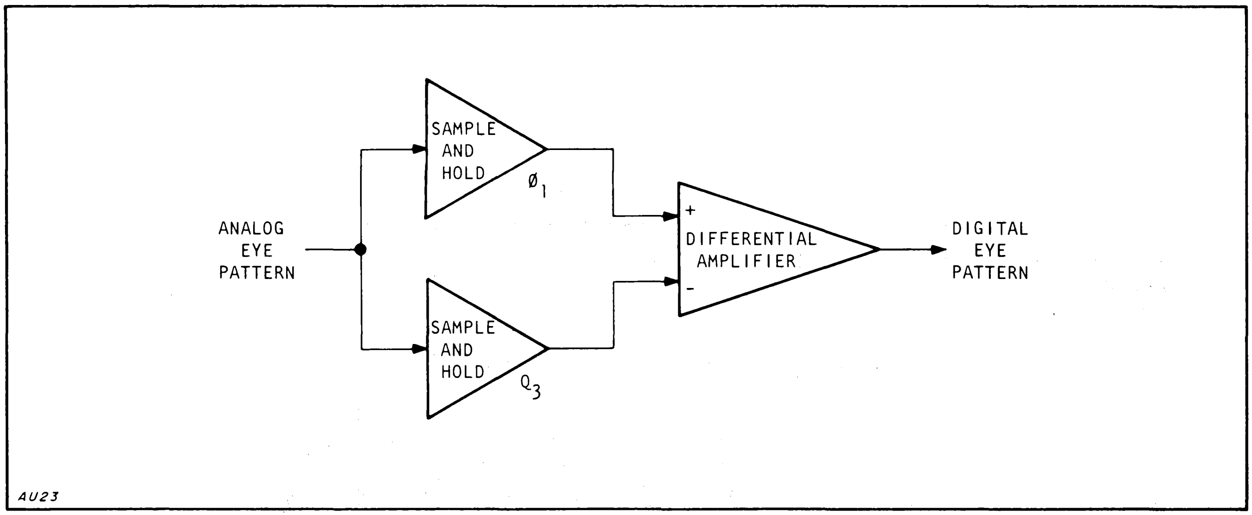

Figure 3-4. Data Recovery Circuit

DEMODULATION

3.12 The demodulation is equivalent to coherent binary PSK detection, closely approximating the theoretical matched filter detector. The signal is effectively sampled at the Nyquist rate, heterodyned to baseband with a coherent (data-derived and smoothed) reference, and integrated over one baud. The data decision in then based on the polarity of the integrate and dump filter at the end of the baud. Because the baud frequency is equal to the carrier frequency in this case, the complex-sounding process discussed above is accomplished simply by sampling and analog waveform at the 1/4- and 3/4-baud period instants, subtracting "sample 3/4" from "sample 1/4," and observing the polarity of the result.

3.13 Figure 3-3 illustrates some typical receive waveforms. The analog eye consists of the waveform out of the analog front end. For 2400 bps (with the RANGE strap set at NORM), the equalizer is not used; thus, the analog eye (line 2) is a smoothed version of the square wave modulator signal. For 4800, 7200, or 9600 bps (with the RANGE strap set at NORM or LONG), the equalizer is used, and it distorts the analog eye at zero range as shown on line 3. The sample windows are shown on lines 4 and 5. They control the sample and hold circuits shown in Figure 3-4.

3.14 The output of the differential amplifier of Figure 3-4 is termed the "digital eye" and is shown on line 6 of Figure 3-3. This signal contains valid information only one-half of the time, e.g., Sample $\emptyset_1$ (n) - Sample $\emptyset_3$ (n). The other half of the time the samples are skewed to span two different baud periods, e.g., Sample $\emptyset_1$ (n+1) - Sample $\emptyset_3$ (n). The polarity of the digital eye is sampled during the correct half as shown on line 7 of Figure 3-3, and the resultant 1-0 pattern is fed to the differential decoder.

CLOCK RECOVERY

3.15 Receive timing recovery relies on sensing zero crossings of the analog eye. These nominally occur in the center of each baud, but deliberate over-equalization results in variations in the zero crossing positions which are data pattern dependent. (Refer to Figure 3-3, line 3.) A standard timing recovery circuit would attempt to track the zero crossing variations, which would result in clock jitter and some performance degradation under high line noise conditions.

3.16 The LADS employs a decision-directed feedback feature which takes advantage of the fact that the zero crossing variations are data pattern dependent. Data pattern decisions (Mark/Space) are used to adjust the behavior of the timing tracker so that the receive clock jitter is minimized and the bit error rate performance is improved.

SIGNAL PRESENCE DETECTION

3.17 Signal presence detection (Receive Signal level) is keyed to the behavior of the digital eye pattern shown on line 6, Figure 3-3. When valid data is present, the eye is open during the output data sample times. As noise and intersymbol interference increase, the digital eye gradually closes and the bit error rate increases; for pure noise there is no eye opening. The LADS senses the relative eye opening and turns Receive Signal level on when that eye opening indicates that a valid signal is being demodulated.

3.18 The advantage of this signal presence detection method is that white noise at any level will not turn Receive Signal level on. Only a valid signal, or interference which looks like a valid signal, can trip the detector. Thus, there is no need for an adjustable threshold which would be needed with a signal-level based detector.

REGULATED DC POWER SUPPLY

3.19 The regulated dc power supply is mounted vertically on the right side of the LADS. The dc power supply contains a step-down transformer, rectifier, diode bridges, filtering, series pass transistors, and IC voltage regulators. The supply furnishes regulated dc outputs of +6.5V and -6.5V, and the 24V unregulated dc remote loopback voltage. The power supply card also contains the 3.6864 MHz crystal oscillator from which is derived the LADS internal timing signals. (See Figure 3-5.)

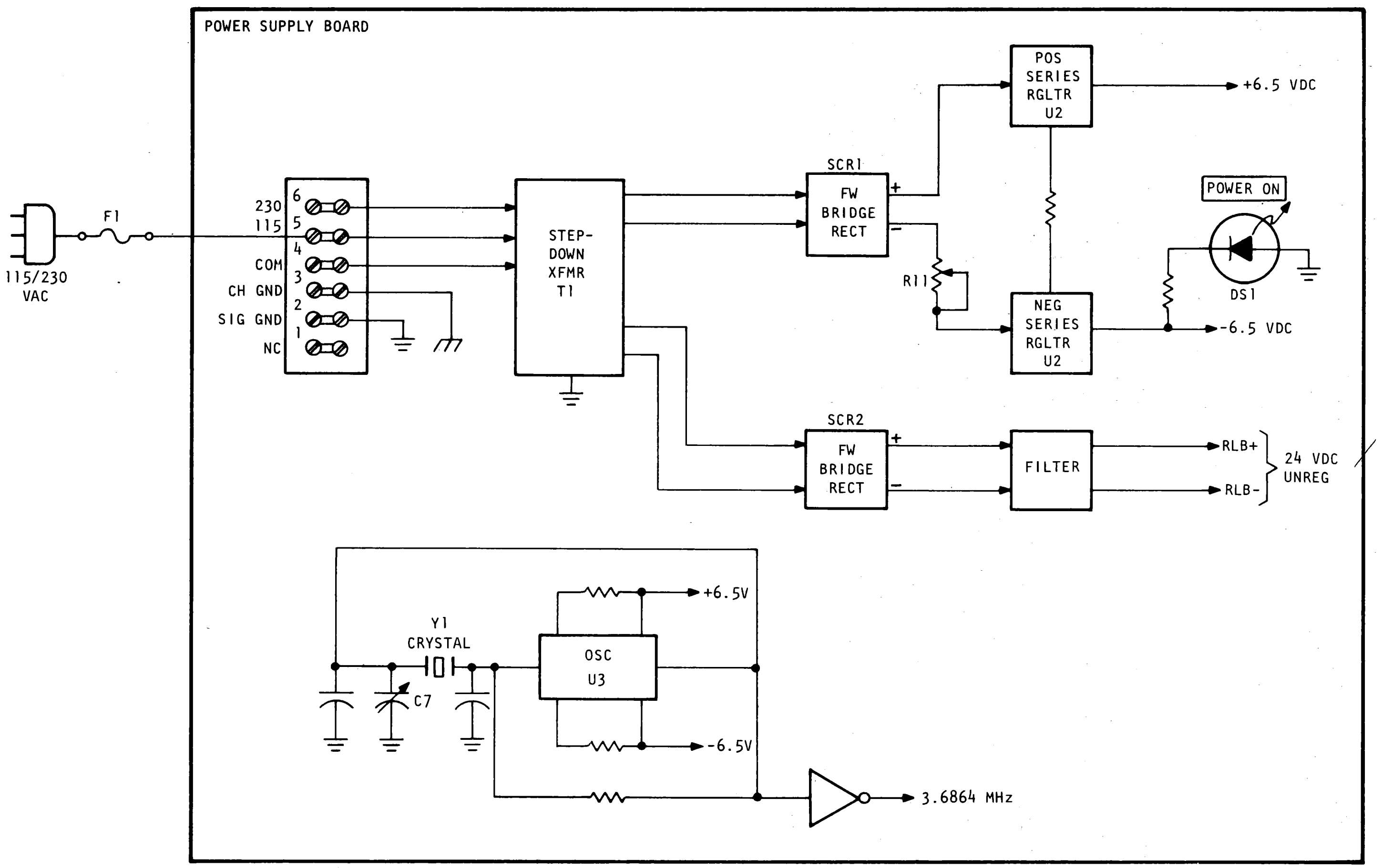

Figure 3-5. DC Power Supply Functional Block Diagram