DATA SET 212AR-L1A/2A

TEST PROCEDURES USING 921A DATA TEST SET

CONTENTS PAGE

1. GENERAL

1.01 This section contains test procedures to be followed when using a 921A (version 2 or higher) data test set (DTS) to test a data set (DS) 212AR. These procedures are to be followed when investigating a trouble report or when needed

during an installation. Test procedures using the 914C DTS are described in Section 592-039-500.

1.02 When this section is reissued, the reason for reissue will be contained in this paragraph.

1.03 The DS 212AR provides full-duplex transmission and reception of serial binary data at two distinct bit rates over the switched network. In the low-speed mode, the maximum bit rate is 300 bits per second (bps). In the high-speed mode, operation is synchronous or character-asynchronous at 1200 bps. Additional information concerning DS 212AR is contained in Section 592-039-100.

1.04 The 921A DTS is a portable, general purpose, serial data test set that provides the serial testing capabilities of the 914C DTS and is compatible with the 914C DTS for end-to-end testing. In addition, the 921A DTS is compatible with the 911A and 911NA DTSs for end-to-end start-stop distortion measurements. Additional information concerning the 921A DTS is contained in Section 107-402-100.

1.05 Input to the 921A DTS is made through a 20-button keyboard. A 32-character alphanumeric display provides operator prompting and diagnostic results. Refer to Fig. 1 for the location and nomenclature of connectors, switches, status indicators, input and output jacks, etc, that will be used in the course of testing DS 212AR.

2. INSTALLATION TESTS

2.01 After the data set has been installed, it must be tested to determine if it is operating properly. Before proceeding with the test, verify that the local loop meets the requirements specified in Section 314-205-501.

2.02 Refer to Fig. 2 for the sequence of tests to be performed to verify proper installation. The 921A DTS is not required for installation testing, but may be used if needed.

3. MAINTENANCE TESTS

3.01 This part provides the sequence in which tests are to be performed during a maintenance visit. This test sequence provides a method of isolating a trouble to the data set, the transmission facility, or the customer-provided equipment (CPE).

3.02 When a trouble report is received, the DTC is responsible for isolating the trouble to the data set or transmission facility. The procedure for doing this is shown in Fig. 3.

3.03 If it is suspected that the trouble is in the data station equipment, a telephone company (telco) employee must be dispatched to conduct more extensive tests. The following equipment should be taken on a trouble visit:

- Spare data set
- 921A DTS.

3.04 Refer to Fig. 4 for the sequence in which tests are to be performed by the telco employee at the data station. If the data set is replaced, the defective data set should be tagged with a tag describing the nature of the trouble, carefully packed, and returned to a service center for repair. Verify that the replacement data set is equipped with the proper options before placing the data set in service.

3.05 If the trouble persists, proceed as follows:

(a) Check that the options installed in the data set agree with those specified on the service order.

(b) Verify that the CPE has been tested and is operating properly.

(c) Check for physical damage to the data station equipment.

(d) Verify that all cords and connectors are properly connected.

(e) Check for intermittent trouble in the station wiring.

(f) Verify that the data set and CPE are connected to a common ground.

(g) If the trouble persists, request help from immediate supervisor.

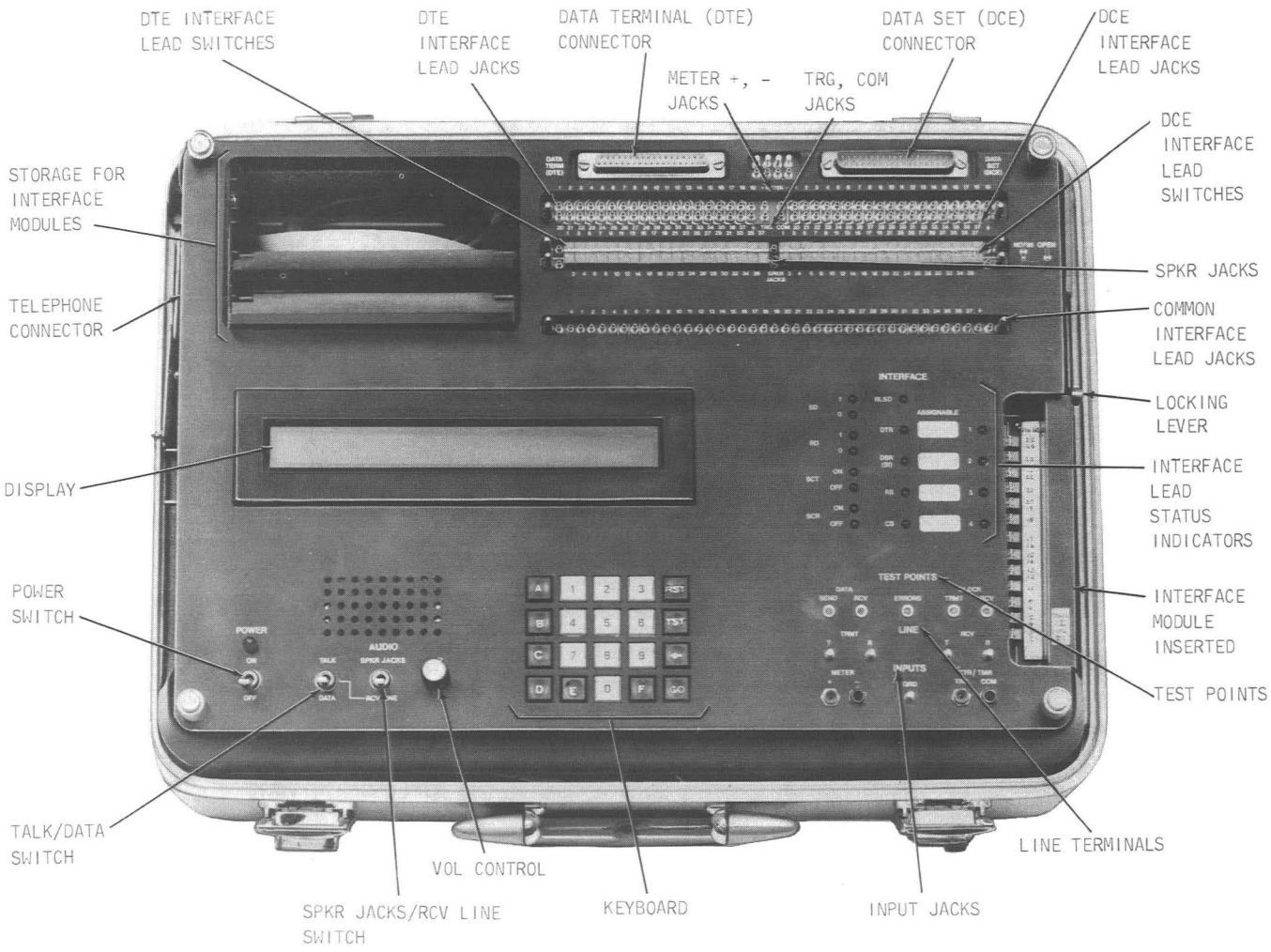

Fig. 1—921A Data Test Set—Front Panel

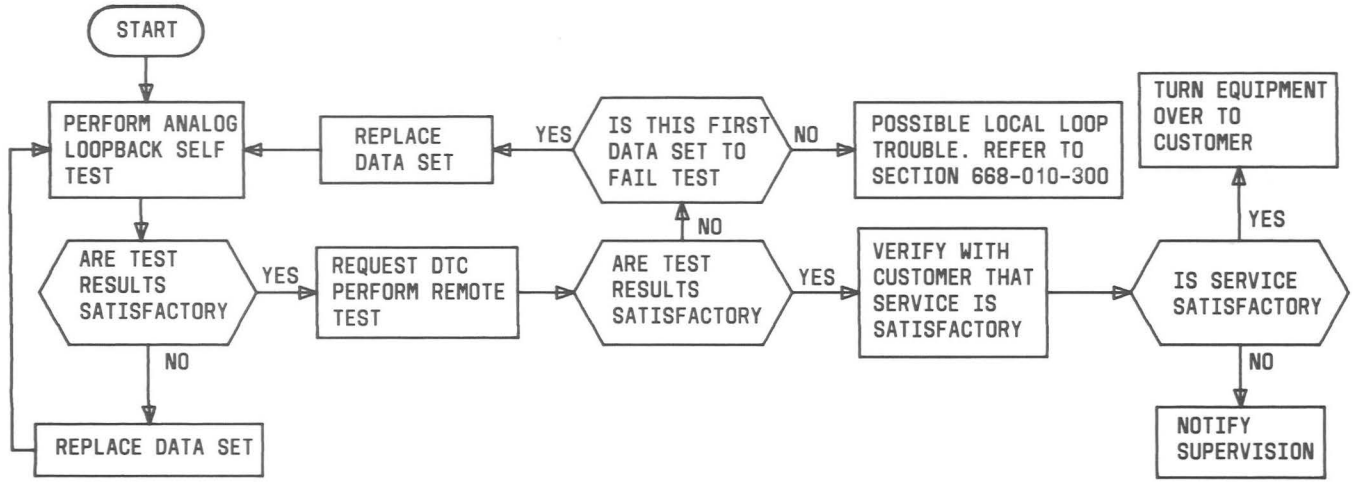

Fig. 2—Installation Test Sequence

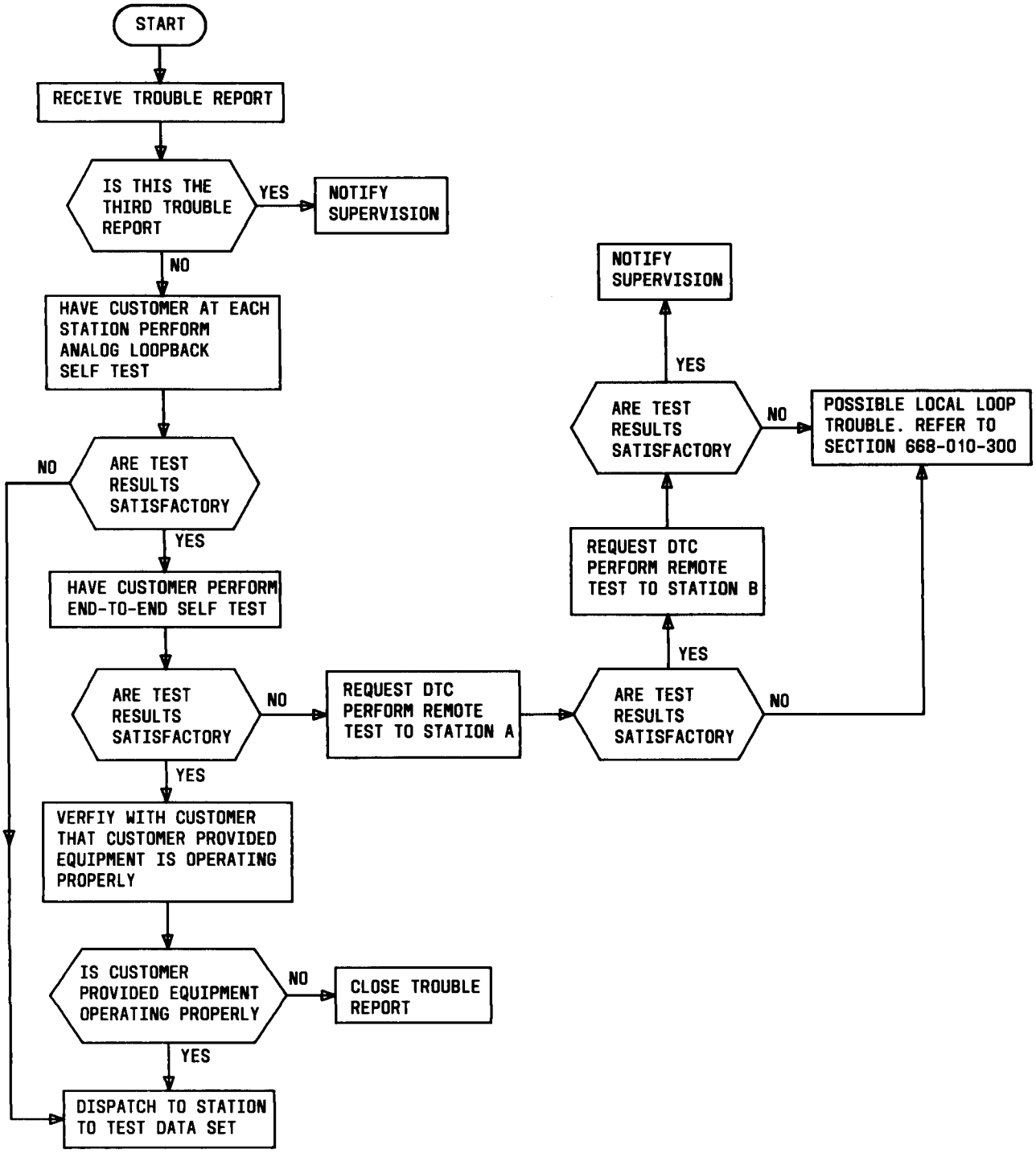

Fig. 3—Clearing Trouble Report

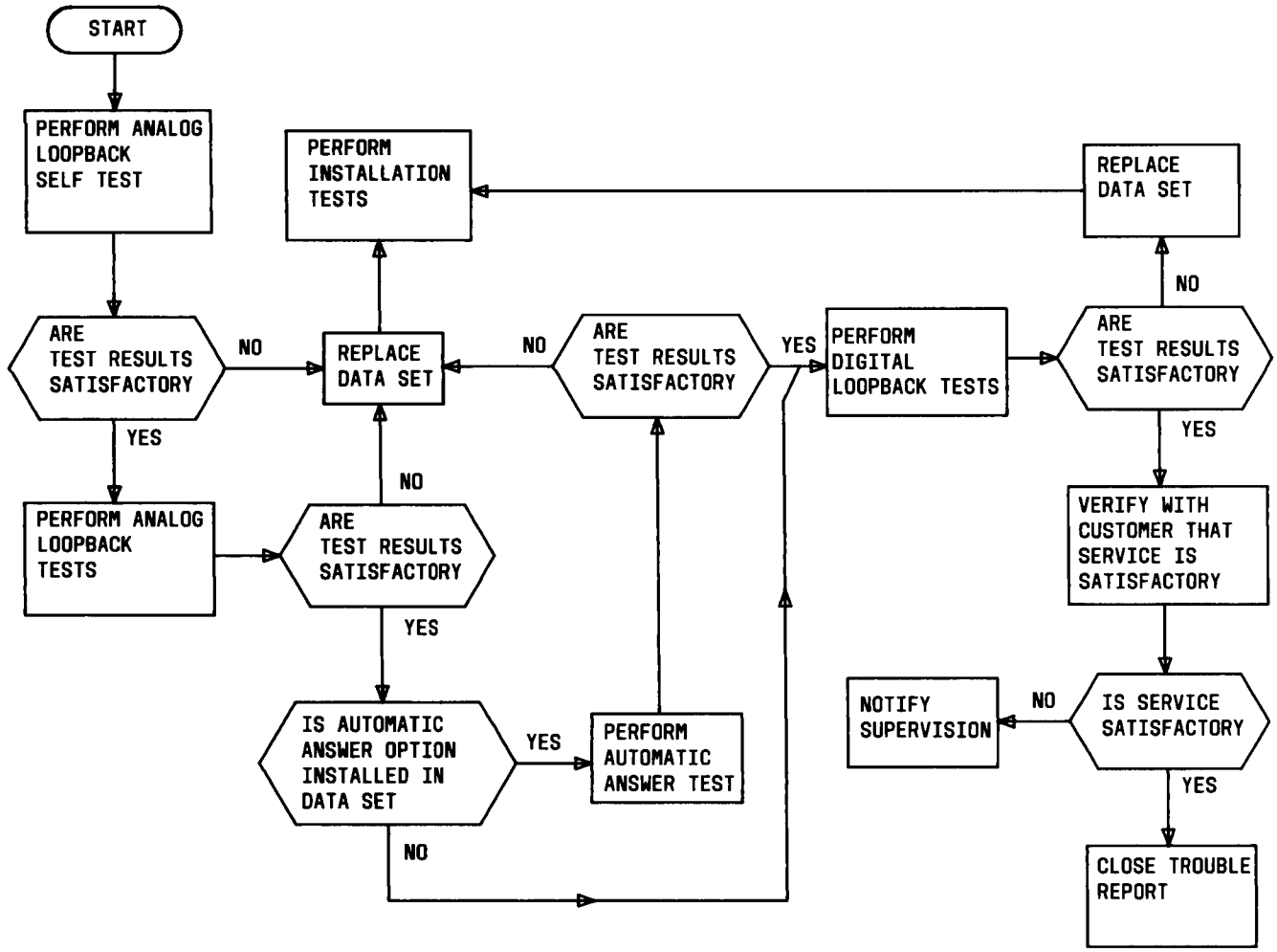

Fig. 4—Maintenance Test Sequence

4. TEST PROCEDURES

TEST CAPABILITIES

4.01 Test circuitry built into DS 212AR permits the following self tests to be performed.

- Analog Loopback Self Test
- Digital Loopback Self Test
- Remote Digital Loopback Self Test (High-Speed Mode).
- End-to-End Self Test

4.02 If a 921A DTS is used, the analog loopback, digital loopback, and end-to-end tests can be performed using pseudorandom data. By use of the 921A DTS, the customer interface circuits are tested and a more precise indication of bit and block errors can be obtained. Start-stop distortion tests can be performed for asynchronous operation. The 921A DTS can also be used to perform a test of the data set automatic answer and interface circuits.

A. Analog Loopback Self Test

4.03 The analog loopback self test checks the data set transmitter and receiver (Fig. 5). The customer interface is not checked. Test data (dotting pattern) generated by the data set is looped internally from the transmitter output to the receiver input. The received data is compared to the transmitted data. This test can be performed

in either the high-speed or low-speed mode. If the data set is operating in the low-speed mode, the MC lamp blinks if the distortion threshold (25 percent) is exceeded. If the data set is operating in the high-speed mode, the MC lamp blinks if a bit error is detected in the received data. Perform the test in the speed mode used by the CPE. The speed-mode is selected by use of the HS switch on the data set (depressed for high-speed mode, released for low-speed mode).

4.04 Perform the test as follows.

(1) Depress AL and ST switches on data set.

Requirements: MB and TM indicators are lighted. MC indicator goes off after SD and RD indicators light. TR indicator is lighted when ST or DL switch is depressed. MR indicator is lighted if option ZF is installed in data set.

(2) Observe MC indicator for 1 minute.

Requirement: MC indicator does not blink.

(3) Release AL and ST switches.

B. Digital Loopback Self Test

4.05 This test uses the digital loopback capability of the data set at one end and the self-test (pattern generating and comparing) capability of the data set at the other end (Fig. 6). The test is performed by putting one data set in the DL mode, placing the other data set in the ST mode, placing a call, and then going to the data mode. The MC indicator on the data set that is in the ST mode blinks if the distortion threshold (25 percent) is exceeded in the low-speed mode or if a bit error is detected in the received data in the high-speed mode. Perform the test in the speed mode used by the CPE. The speed mode is selected by use of the HS switch on the data set (depressed for high-speed mode, released for low-speed mode).

Note: In the low-speed mode, the distant data set may be 103J, 103JR, 113C, 113CR, 113D, or 113DR.

4.06 Perform the test as follows.

(1) Place a call to distant station. If distant data set is already in DL mode, it will answer automatically.

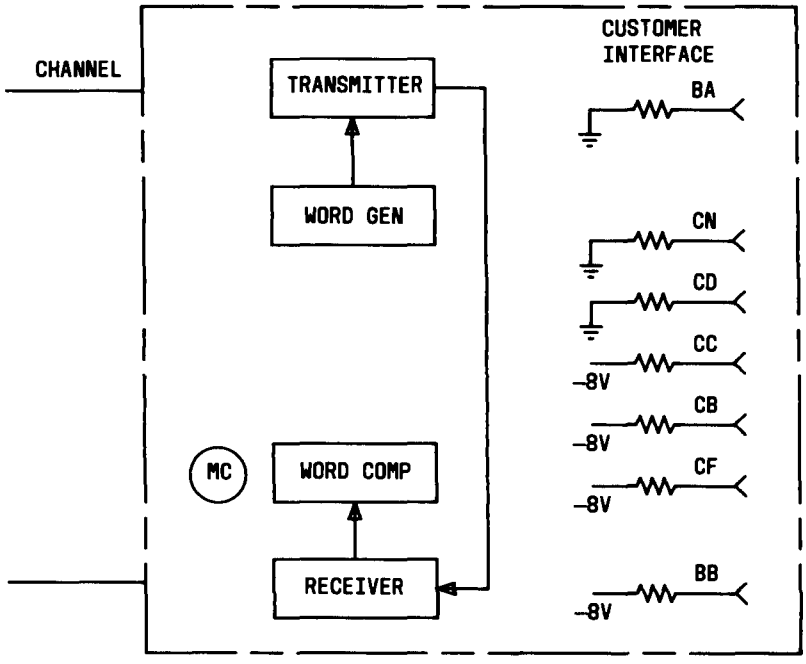

Fig. 5—Analog Loopback Self Test—Simplified Block Diagram

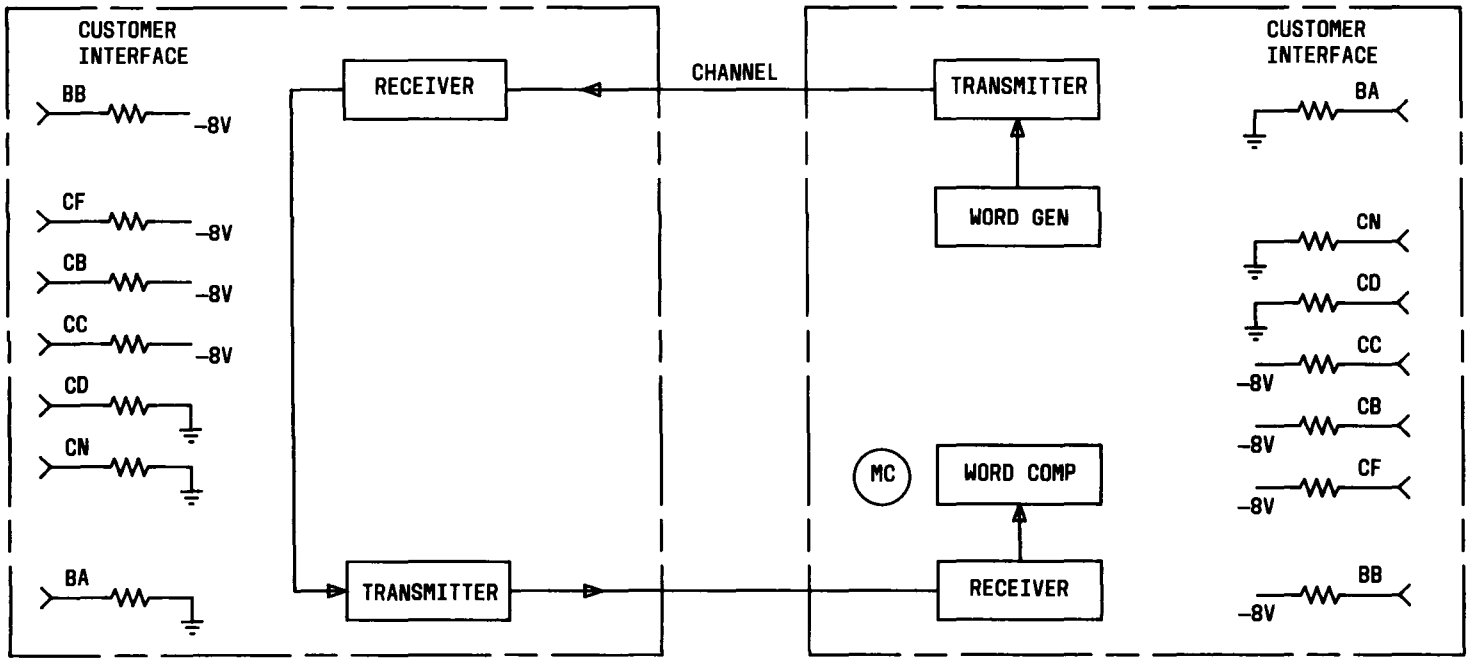

Fig. 6—Digital Loopback—Simplified Block Diagram

(2) If distant data set does not answer automatically, instruct attendant at distant station to depress DL switch and go to data mode.

(3) On local data set, depress ST switch and go to data mode.

(4) Observe MC indicator on local data set for 2 minutes.

Requirements:

- Low-Speed—If MC indicator stays off, both data sets and the line facilities are operating properly. If MC indicator blinks or remains lighted, the round-trip distortion is exceeding 25 percent. Since the distortion in the two directions may be additive, no conclusion about the proper operability of the data sets and the line facilities may be drawn.
- High-Speed—Maximum of six blinks

(5) Release ST switch on local data set. Call distant station and have DL switch released.

C. Remote Digital Loopback Self Test

4.07 This test uses the remote digital loopback and self-test capabilities of the local data set and can be used to test both data sets and the line facilities in the high-speed mode only. The local data set is placed in the self-test mode by depressing the ST switch. The distant data set is placed in the remote digital loopback mode by depressing the RDL switch on the local data set. The local data set pattern generator is used to send a signal to the distant data set, where it is looped back and retransmitted. The error-detecting circuitry causes the MC indicator on the local data set to blink when an error is detected in the received data.

Note: If the distant data set is equipped with option YL (receiver responds to digital loop—OUT) or option ZG (automatic answer—OUT), this test cannot be performed.

4.08 Perform the test as follows.

(1) Depress HS, RDL, and ST switches on local data set and verify that TM indicator lights.

(2) Dial a call to distant data set.

(3) When distant data set has answered, place local data set in data mode.

(4) Observe MC indicator on local data set for 2 minutes.

Requirement: Maximum of six blinks

Note: If MC indicator is lighted continuously, this may indicate that distant data set is not in DL mode.

(5) Release RDL and ST switches on local data set. Return local data set to speed mode used by CPE.

D. End-to-End Self Test

4.09 This test can be used to check the local data set, the distant data set, and the line facilities. This test is performed by depressing the ST switch at each end, placing a call from one end to the other, and then going to the data mode. Each data set sends the test pattern to the other end. The speed mode of the test is selected at the originating station. The error-detecting circuitry at each end monitors the received data signal and causes the MC indicator to blink if the distortion threshold (25 percent) is exceeded (low-speed) or if a bit error is detected (high-speed). Perform the test in the speed mode used by the CPE.

Note: For low-speed testing, the distant end may be a DS 103J, 103JR, 113C, 113CR, 113D, or 113DR.

4.10 Perform the test as follows.

(1) Call distant station and arrange to conduct an end-to-end self test. At originating station, speed mode is selected by use of HS switch on data set (depressed for high-speed mode, released for low-speed mode).

(2) Depress ST switch on each data set. Verify that TM indicator lights.

(3) Go to data mode at each station. Verify that MC indicator goes off after SD and RD indicators light. TR indicator is lighted when

ST or DL switch is depressed. HS indicator is lighted or off, depending on speed mode of test.

(4) Observe MC indicator on data set for 2 minutes.

Requirements:

- Low-speed—If MC indicator stays off, both data sets and the line facilities are operating properly. If MC indicator blinks or remains lighted, the distortion is exceeding 25 percent.
- High-Speed—Maximum of two blinks

(5) At end of test, go to talk mode and then release ST switch on each data set.

E. Initial Test Setup for 921A DTS

4.11 The initial test setup to test DS 212AR using the 921A DTS is as follows.

STEP	ACTION	VERIFICATION
1	Connect data set to DTS using interface cable and Electronic Industries Association (EIA) adapter cord provided with DTS. ***Note:*** The interface cable is equipped with two 37-pin connectors. The 6-inch adapter cord is equipped with a 37-pin female connector and a 25-pin male connector. Connect interface cable from DATA SET (DCE) connector on DTS to 37-pin connector on adapter cord. Insert 25-pin connector on adapter cord into customer interface connector on data set.	
2	Connect DTS to a 105-129 Vac 60-Hz power source.	
3	Apply power to data set.	Data set ON lamp lights.
4	On front of DTS, set POWER switch to ON.	POWER lamp lights.
5	Press RST on keyboard. ***Note:*** If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display reads (briefly) version number of DTS. DTS then performs self tests. If DTS is defective, display reads— TEST FAILED. If DTS is satisfactory, display reads— DATA SET:
6	Remove EIA RS-232-C interface module from storage and ensure that all 25 interface module switches are in TERM position.	
7	On right side of DTS, ensure that locking lever is in OPEN position.	
8	Insert interface module into slot.	
9	Move locking lever to CLOSE position.	

STEP	ACTION	VERIFICATION
10	On front of DTS, ensure that all 37 DCE interface lead switches are in NORM position.	

F. Analog Loopback Test With 921A DTS

4.12 This test checks the data set interface and transmitter and receiver circuits. Test data is generated by a DTS and looped back internally from the data set transmitter output to the receiver input. The received data is compared to the original data by the DTS and errors are indicated on the DTS display.

4.13 Perform this test in the speed mode used most often by the CPE or in the speed mode that is causing difficulty.

AL Low-Speed Bit Error Test

4.14 Connect and condition the 921A DTS per the instructions in paragraph 4.11.

4.15 Condition data set as follows.

(1) Verify that option YP is installed.

(2) Verify that data set is in low-speed mode (HS button released) if option XK is installed. Speed selection is automatic if option XJ is installed.

(3) Depress AL switch on data set. If option ZF is installed, verify that MR indicator on data set and DSR indicator on DTS light.

4.16 Perform the test as follows.

STEP	ACTION	VERIFICATION
1	Press RST on keyboard. *Note:* If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display reads (briefly) version number of DTS. DTS then performs self tests. If DTS is defective, display reads— TEST FAILED. If DTS is satisfactory, display reads— DATA SET:
2	Enter 36 on keyboard.	Display reads— DATA SET: 36
3	Press GO.	Display reads— BIT RATE:
4	Enter 03.	Display reads— BIT RATE: 03
5	Press GO.	Display reads— TEST SEQ:
6	Enter 55.	Display reads— TEST SEQ: 55
7	Press GO.	Display reads: TRANSMITTER=? 1=921 2=914 3=903
8	Enter 1.	Display reads (briefly)— TRANSMITTER=1 1=921 2=914 3=903

STEP	ACTION	VERIFICATION
		Display then reads (briefly)— SELECT ERROR TEST Display then reads— D=DT 0=SP 1=MK 2=2047 5=511 6=63
9	Enter 5.	Display reads (briefly)— 511 BIT ERROR TEST Display then reads— 1=BIT ERRORS 2=BLOCK ERRORS
10	Enter 1.	Display reads— ???? SECONDS
11	Enter 0060. ***Note:*** To perform functions listed below, press associated key. **KEY FUNCTION** A Repeat test. B Display time remaining in test. C Clear display. D End test. E Inject 8 errors into data stream. F Force out-of-sync condition.	Display reads (briefly)— 0060 SECONDS Display then reads— 0000 BITS IN ERROR From this point, display counts number of bits in error. If sync is lost during test, display flashes OSYN. If this occurs, test must be repeated by pressing A. At end of test, display reads TEST COMPLETE, total sync losses, and total bits in error. ***Requirement:*** No bits in error.
12	Release AL switch on data set.	

AL Low-Speed Start-Stop Distortion Test

4.17 Connect and condition the 921A DTS per the instructions in paragraph 4.11.

4.18 Condition data set as described in paragraph 4.15.

4.19 Perform the test as follows.

STEP	ACTION	VERIFICATION
1	Press RST on keyboard. ***Note:*** If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display reads (briefly) version number of DTS. DTS then performs self tests. If DTS is defective, display reads— TEST FAILED. If DTS is satisfactory, display reads— DATA SET:
2	Enter 36 on keyboard.	Display reads— DATA SET: 36

STEP	ACTION	VERIFICATION
3	Press GO.	Display reads— BIT RATE:
4	Enter 03.	Display reads— BIT RATE: 03
5	Press GO.	Display reads— TEST SEQ:
6	Enter 52 79.	Display reads— TEST SEQ: 52 79
7	Press GO.	Display reads— PARITY=? (0=EVEN, 1=ODD)
8	Enter 0.	Display reads (briefly)— PARITY=0 (0=EVEN, 1=ODD) Display then reads— TRMT=? (1=MAN 2=CONT)
9	Enter 2. ***Note:*** Ignore display, PRESS A TO START.	Display reads (briefly)— TRMT=2 (1=MAN 2=CONT) Display then reads— PRESS A TO START
10	Press GO.	Display reads (briefly)— TEST INTERRUPTED Display then reads— MODE=? (1=RCV 2=RCV & TRMT)
11	Enter 2.	Display reads (briefly)— MODE=2 (1=RCV 2=RCV & TRMT) Display then reads— HITS OVER ??% (MAX=49%)
12	Enter 08.	Display reads (briefly)— HITS OVER 08% (MAX=49%) Display then reads— ???? SECONDS
13	Enter 0060 and after about 2 seconds, press C. ***Note:*** To perform functions listed below, press associated key.	

KEY	FUNCTION	
A	Repeat test.	Display reads (briefly)—
B	Display time remaining in test.	0060 SECONDS
C	Clear display.	Display then reads—
D	End test.	PEAK=00% HITS=00/08 AVG BIAS=00%

STEP	ACTION	VERIFICATION
		At end of test, display reads TEST COMPLETE and test results. ***Requirements:*** 1. Less than 09% peak distortion. 2. Less than 01/08 hits. 3. Less than 02% average bias distortion.
14	Release AL switch on data set.	

AL High-Speed Synchronous Bit Error Test

4.20 Connect and condition the 921A DTS per the instructions in paragraph 4.11.

4.21 Condition data set as follows.

(1) Verify that option YH is installed.

(2) Depress AL and HS switches.

4.22 Perform the test as follows.

STEP	ACTION	VERIFICATION
1	Press RST on keyboard. ***Note:*** If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display reads (briefly) version number of DTS. DTS then performs self tests. If DTS is defective, display reads— TEST FAILED. If DTS is satisfactory, display reads— DATA SET:
2	Enter 66 on keyboard.	Display reads— DATA SET: 66
3	Press GO.	Display reads— BIT RATE:
4	Enter 12.	Display reads— BIT RATE: 12
5	Press GO.	Display reads— TEST SEQ:
6	Enter 55.	Display reads— TEST SEQ: 55
7	Press GO.	Display reads— D=DT 0=SP 1=MK 2=2047 5=511 6=63
8	Enter 5.	Display reads (briefly)— 511 BIT ERROR TEST Display then reads— 1=BIT ERRORS 2=BLOCK ERRORS

STEP	ACTION	VERIFICATION
9	Enter 1.	Display reads— ???? SECONDS
10	Enter 0060.	
	Note: To perform functions listed below, press associated key.	
	KEY FUNCTION	
	A Repeat test. B Display time remaining in test. C Clear display. D End test. E Inject 8 errors into data stream. F Force out-of-sync condition.	Display reads (briefly)— 0060 SECONDS Display then reads— 0000 BITS IN ERROR From this point, display counts number of bits in error. If sync is lost during test, display flashes OSYN. If this occurs, test must be repeated by pressing A. At end of test, display reads TEST COMPLETE, total sync losses, and total bits in error. ***Requirement:*** Total bits in error are less than 12.
11	Release AL switch on data set.	

AL High-Speed Asynchronous Start-Stop Distortion Test—10-Bit Word

4.23 Connect and condition the 921A DTS per the instructions in paragraph 4.11.

4.24 Condition data set as follows.

STEP	ACTION	VERIFICATION
		(1) Verify that options YG & YJ are installed.
		(2) Depress AL and HS switches.

4.25 Perform the test as follows.

STEP	ACTION	VERIFICATION
1	Press RST on keyboard. ***Note:*** If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display reads (briefly) version number of DTS. DTS then performs self tests. If DTS is defective, display reads— TEST FAILED. If DTS is satisfactory, display reads— DATA SET:
2	Enter 36.	Display reads— DATA SET: 36
3	Press GO.	Display reads— BIT RATE:
4	Enter 12.	Display reads— BIT RATE: 12

STEP	ACTION	VERIFICATION
5	Press GO.	Display reads— TEST SEQ:
6	Enter 52 79.	Display reads— TEST SEQ: 52 79
7	Press GO.	Display reads— BITS/CHAR=? (0=NINE 1=TEN)
8	Enter 1.	Display reads (briefly)— BITS/CHAR=1 (0=NINE 1=TEN) Display then reads— PARITY=? (0=EVEN, 1=ODD)
9	Enter 0.	Display reads (briefly)— PARITY=0 (0=EVEN, 1=ODD) Display then reads— TRMT=? (1=MAN 2=CONT)
10	Enter 2. ***Note:*** Ignore display, PRESS A TO START.	Display reads (briefly)— TRMT=2 (1=MAN 2=CONT) Display then reads— PRESS A TO START
11	Press GO.	Display reads (briefly)— TEST INTERRUPTED Display then reads— MODE=? (1=RCV 2=RCV & TRMT)
12	Enter 2.	Display reads (briefly)— MODE=2 (1=RCV 2=RCV & TRMT) Display then reads— BITS/CHAR=? (0=NINE 1=TEN)
13	Enter 1.	Display reads (briefly)— BITS/CHAR=1 (0=NINE 1=TEN) Display then reads— HITS OVER ??% (MAX=49%)
14	Enter 16.	Display reads (briefly)— HITS OVER 16% (MAX=49%) Display then reads— ???? SECONDS
15	Enter 0060 and after about 2 seconds, press C. ***Note:*** To perform functions listed below, press associated key.	

STEP	ACTION	VERIFICATION
	KEY FUNCTION A Repeat test. B Display time remaining in test. C Clear display. D End test.	Display reads (briefly)— 0060 SECONDS Display then reads— PEAK=00% HITS=00/16 AVG BIAS=00% At end of test, display reads TEST COMPLETE and test results. ***Requirements:*** 1. Less than 17% peak distortion. 2. Less than 01/16 hits. 3. Less than 07% average bias distortion.
16	Release AL switch on data set.	

AL High-Speed Asynchronous Start-Stop Distortion Test—9-Bit Word

4.26 The 9-bit word test and requirements are the same as the test and requirements for the 10-bit word described in paragraphs 4.23 through 4.25 with the following changes.

- Install option YI.
- Step 8 enter "0" instead of "1"; display reads briefly: BITS/CHAR=0 (0=NINE 1=TEN), display then reads TRMT=? (1=MAN 2=CONT).
- Omit Step 9.
- Step 13 enter "0" instead of "1"; display reads briefly: BITS/CHAR=0 (0=NINE 1=TEN), display then reads "HITS OVER ??% (MAX=49%)".
- Step 14 enter 14 instead of 16; display reads briefly: HITS OVER 14% (MAX=49%), display then reads "???? SECONDS".
- Step 15 change requirement 1 to less than 15% peak distortion and requirement 2 to less than 01/14 hits.

G. Digital Loopback Test With 921A DTS

4.27 This test checks the transmitter and receiver of both data sets and the connecting facility. The distant data set can be a 103J, 103JR, 113C, 113CR, 113D, or 113DR. The customer interface at the distant data set is not checked. Test data is generated by the DTS and transmitted by the local data set. This data is looped back internally from the receiver output to the transmitter input of the distant data set and retransmitted. The data is received by the local data set and is compared to the original data. Data errors are indicated on the display of the DTS.

> ***Note:*** This test cannot be performed in the high-speed mode if option WI (transmitter timing—SLAVE) is installed in the local data set.

4.28 Perform this test in the speed mode used most often by the CPE or in the speed mode that is causing difficulty.

4.29 The DS 212AR has the capability to force the distant data set into a digital loopback mode. The test can only be used when the data set is in the high-speed mode. The remotely activated digital loopback takes place at the distant data set only if options YK (receiver responds to digital loop—IN) and ZH (automatic answer—IN) are installed at that end and the CD (data terminal ready) lead is ***on.*** If option YE is installed, interface lead CN must be ***off.***

DL Low-Speed Bit Error Test

4.30 Connect and condition the 921A DTS per the instructions in paragraph 4.11.

4.31 Condition data set as follows.

(1) Verify that option YP is installed.

(2) Verify that data set is in low-speed mode (HS switch released) if option XK is installed.

Speed selection is automatic if option XJ is installed.

4.32 Connect a jumper wire between common interface lead jacks 10 and 23 on DTS.

4.33 Perform the test as follows.

STEP	ACTION	VERIFICATION
1	Press RST on keyboard. *Note:* If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display reads (briefly) version number of DTS. DTS then performs self tests. If DTS is defective, display reads— TEST FAILED. If DTS is satisfactory, display reads— DATA SET:
2	Enter 36 on keyboard.	Display reads— DATA SET: 36
3	Press GO.	Display reads— BIT RATE:
4	Enter 03.	Display reads— BIT RATE: 03
5	Press GO.	Display reads— TEST SEQ:
6	Enter 55. *Note:* If the DL low-speed start-stop distortion test is to be performed, also enter 52 79 following 55.	Display reads— TEST SEQ: 55 or TEST SEQ: 55 52 79
7	Press GO.	Display reads— TRANSMITTER=? 1=921 2=914 3=903
8	Enter 1.	Display reads (briefly)— TRANSMITTER=1 1=921 2=914 3=903 Display then reads (briefly)— SELECT ERROR TEST Display then reads— D=DT 0=SP 1=MK 2=2047 5=511 6=63 On DTS, DTR indicator lights.
9	Enter 5.	Display reads (briefly)— 511 BIT ERROR TEST Display then reads— 1=BIT ERRORS 2=BLOCK ERRORS

STEP	ACTION	VERIFICATION
10	Place a call to distant end and request attendant to depress DL switch on data set, and go into data mode at both ends.	On DTS, RLSD, DSR, and CS indicators are lighted.
11	Enter 1.	Display reads— ???? SECONDS
12	Enter 0300. ***Note:*** To perform functions listed below, press associated key.	
	KEY FUNCTION A Repeat test. B Display time remaining in test. C Clear display. D End test. E Inject 8 errors into data stream. F Force out-of-sync condition.	Display reads (briefly)— 0300 SECONDS Display then reads— 0000 BITS IN ERROR From this point, display counts number of bits in error. If sync is lost during test, display flashes OSYN. If this occurs, test must be repeated by pressing A. At end of test, display reads TEST COMPLETE, total sync losses, and total bits in error. ***Requirement:*** Total bits in error are less than 2.
	Note: If DL low-speed start-stop distortion test is going to be performed, do not hang up. Press GO, display reads briefly, TEST INTERRUPTED. Display then reads, PARITY=? (0=EVEN, 1=ODD). Skip to Step 9 of paragraph 4.37 and proceed with test.	
13	Remove jumper wire from common interface lead jacks on DTS.	

DL Low-Speed Start-Stop Distortion Test

4.34 Connect and condition the 921A DTS per the instructions in paragraph 4.11.

4.35 Condition data set as described in paragraph 4.31.

4.36 Connect a jumper wire between common interface lead jacks 10 and 23 on DTS.

4.37 Perform the test as follows.

STEP	ACTION	VERIFICATION
1	Press RST on keyboard. ***Note:*** If RST is pressed during a test, the test is ended and the DTS recycles to this	Display reads (briefly) version number of DTS. DTS then performs self tests. If DTS is defective, display reads—

STEP	ACTION	VERIFICATION
	step.	TEST FAILED. If DTS is satisfactory, display reads— DATA SET:
2	Enter 36 on keyboard.	Display reads— DATA SET: 36
3	Press GO.	Display reads— BIT RATE:
4	Enter 03.	Display reads— BIT RATE: 03
5	Press GO.	Display reads— TEST SEQ:
6	Enter 52 79.	Display reads— TEST SEQ: 52 79
7	Press GO.	Display reads— PARITY=? (0=EVEN, 1=ODD) On DTS, DTR indicator lights.
8	Place a call to distant end and request attendant to depress DL switch on data set, and go into data mode at both ends.	On DTS, RLSD, DSR, and CS indicators are lighted.
9	Enter 0.	Display reads (briefly)— PARITY=0 (0=EVEN, 1=ODD) Display then reads— TRMT=? (1=MAN 2=CONT)
10	Enter 2. ***Note:*** Ignore display, PRESS A TO START.	Display reads (briefly)— TRMT=2 (1=MAN 2=CONT) Display then reads— PRESS A TO START
11	Press GO.	Display reads (briefly)— TEST INTERRUPTED Display then reads— MODE=? (1=RCV 2=RCV & TRMT)
12	Enter 2.	Display reads (briefly)— MODE=2 (1=RCV 2=RCV & TRMT) Display then reads— HITS OVER ??% (MAX=49%)
13	Enter 08.	Display reads (briefly)— HITS OVER 08% (MAX=49%) Display then reads— ???? SECONDS

STEP	ACTION	VERIFICATION
14	Enter 0060 and after about 2 seconds, press C. ***Note:*** To perform functions listed below, press associated key. **KEY FUNCTION** A Repeat test. B Display time remaining in test. C Clear display. D End test.	Display reads (briefly)— 0060 SECONDS Display then reads— PEAK=00% HITS=00/08 AVG BIAS=00% At end of test, display reads TEST COMPLETE and test results. ***Requirements:*** 1. Less than 09% peak distortion. 2. Less than 01/08 hits. 3. Less than 02% average bias distortion.
15	Remove jumper wire from common interface lead jacks on DTS.	

DL High-Speed Synchronous Bit Error Test

4.38 Connect and condition the 921A DTS per the instructions in paragraph 4.11.

4.39 Condition data set as follows.

(1) Verify that option YH is installed.

(2) Depress HS switch.

4.40 Perform the test as follows.

STEP	ACTION	VERIFICATION
1	Press RST on keyboard. ***Note:*** If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display reads (briefly) version number of DTS. DTS then performs self tests. If DTS is defective, display reads— TEST FAILED. If DTS is satisfactory, display reads— DATA SET:
2	Enter 66 on keyboard.	Display reads— DATA SET: 66
3	Press GO.	Display reads— BIT RATE:
4	Enter 12.	Display reads— BIT RATE: 12

STEP	ACTION	VERIFICATION
5	Press GO.	Display reads— TEST SEQ:
6	Enter 55.	Display reads— TEST SEQ: 55
7	Press GO.	Display reads— D=DT Q=SP 1=MK 2=2047 5=511 6=63 On DTS, DTR indicator lights.
8	Enter 5.	Display reads (briefly)— 511 BIT ERROR TEST Display then reads— 1=BIT ERRORS 2=BLOCK ERRORS
9	Place a call to distant end and request attendant to depress DL switch on data set, and go into data mode at both ends.	On DTS, RLSD, DSR, and CS indicators are lighted.
10	Enter 1.	Display reads— ???? SECONDS
11	Enter 0300. ***Note:*** To perform functions listed below, press associated key. **KEY FUNCTION** A Repeat test. B Display time remaining in test. C Clear display. D End test. E Inject 8 errors into data stream. F Force out-of-sync condition.	Display reads (briefly)— 0300 SECONDS Display then reads— 0000 BITS IN ERROR From this point, display counts number of bits in error. If sync is lost during test, display flashes OSYN. If this occurs, test must be repeated by pressing A. At end of test, display reads TEST COMPLETE, total sync losses, and total bits in error. ***Requirement:*** Total bits in error are less than 12.

DL High-Speed Asynchronous Start-Stop Distortion Test—10-Bit Word

4.41 Connect and condition the 921A DTS per the instructions in paragraph 4.11.

4.42 Condition data set as follows.

(1) Verify that options YG and YJ are installed.

(2) Depress HS switch.

4.43 Connect a jumper wire between common interface lead jacks 10 and 23 on DTS.

4.44 Perform the test as follows.

STEP	ACTION	VERIFICATION
1	Press RST on keyboard. ***Note:*** If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display reads (briefly) version number of DTS. DTS then performs self tests. If DTS is defective, display reads— TEST FAILED. If DTS is satisfactory, display reads— DATA SET:
2	Enter 36 on keyboard.	Display reads— DATA SET: 36
3	Press GO.	Display reads— BIT RATE:
4	Enter 12.	Display reads— BIT RATE: 12
5	Press GO.	Display reads— TEST SEQ:
6	Enter 52 79.	Display reads— TEST SEQ: 52 79
7	Press GO.	Display reads— BITS/CHAR=? (0=NINE 1=TEN)
8	Enter 1.	Display reads (briefly)— BITS/CHAR=1 (0=NINE 1=TEN) Display then reads— PARITY=? (0=EVEN, 1=ODD) On DTS, DTR indicator lights.
9	Place a call to distant end and request attendant to depress DL switch on data set, and go into data mode at both ends.	On DTS, RLSD, DSR, and CS indicators are lighted.
10	Enter 0.	Display reads (briefly)— PARITY=0 (0=EVEN, 1=ODD) Display then reads— TRMT=? (1=MAN 2=CONT)
11	Enter 2. ***Note:*** Ignore display, PRESS A TO START.	Display reads (briefly)— TRMT=2 (1=MAN 2=CONT) Display then reads— PRESS A TO START
12	Press GO.	Display reads (briefly)— TEST INTERRUPTED Display then reads— MODE=? (1=RCV 2=RCV & TRMT)

STEP	ACTION	VERIFICATION
13	Enter 2.	Display reads (briefly)— MODE=2 (1=RCV 2=RCV & TRMT) Display then reads— BITS/CHAR=? (0=NINE 1=TEN)
14	Enter 1.	Display reads (briefly)— BITS/CHAR=1 (0=NINE 1=TEN) Display then reads— HITS OVER ??% (MAX=49%)
15	Enter 16.	Display reads (briefly)— HITS OVER 16% (MAX=49%) Display then reads— ???? SECONDS
16	Enter 0060 and after about 2 seconds, press C. ***Note:*** To perform functions listed below, press associated key. **KEY FUNCTION** A Repeat test. B Display time remaining in test. C Clear display. D End test.	Display reads (briefly)— 0060 SECONDS Display then reads— PEAK=00% HITS=00/16 AVG BIAS=00% At end of test, display reads TEST COMPLETE and test results. ***Requirements:*** 1. Less than 16% peak distortion. 2. Less than 01/16 hits. 3. Less than 07% average bias distortion.

DL High-Speed Asynchronous Start-Stop Distortion Test—9-Bit Word

4.45 The 9-bit word test and requirements are the same as the test and requirements for the 10-bit word described in paragraphs 4.41 through 4.44 with the following changes.

- Install option YI.
- Step 8 enter "0" instead of "1"; display reads briefly: BITS/CHAR=0 (0=NINE 1=TEN), display then reads TRMT=? (1=MAN 2=CONT).
- Omit Step 10.
- Step 14 enter "0" instead of "1"; display reads briefly: BITS/CHAR=0 (0=NINE 1=TEN), display then reads HITS OVER ??% (MAX=49%).
- Step 15 enter 14 instead of 16; display reads briefly: HITS OVER 14% (MAX=49%), display then reads ???? SECONDS.
- Step 16 change requirement 1 to less than 15% peak distortion and requirement 2 to less than 01/14 hits.

H. End-to-End Test With 921A DTS

4.46 The end-to-end test checks the transmitter and receiver of both data sets and the

connecting facility. The customer interface at both data sets is also checked. Identical test data is generated by DTSs at both data sets. This data is transmitted by one of the data sets and compared to the data generated by the DTS at the receiving data set. Data errors are indicated on the DTS counter.

4.47 Perform this test in the speed mode used most often by the CPE or in the speed mode that is causing difficulty.

ETE Low-Speed Bit Error Test

4.48 Connect and condition both 921A DTSs per the instructions in paragraph 4.11.

4.49 Condition both data sets as follows.

(1) Verify that option YP is installed.

(2) Verify that data sets are in low-speed mode (HS switch released) if option XK is installed. Speed selection is automatic if option XJ is installed.

4.50 Connect a jumper wire between common interface lead jacks 10 and 23 on both DTSs.

4.51 Establish voice communication between the data stations and arrange to conduct an end-to-end low-speed bit error test.

4.52 Perform the test as follows.

STEP	ACTION	VERIFICATION
1	Press RST on keyboard. *Note:* If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display reads (briefly) version number of DTS. DTS then performs self tests. If DTS is defective, display reads— TEST FAILED. If DTS is satisfactory, display reads— DATA SET:
2	Enter 36 on keyboard.	Display reads— DATA SET: 36
3	Press GO.	Display reads— BIT RATE:
4	Enter 03.	Display reads— BIT RATE: 03
5	Press GO.	Display reads— TEST SEQ:
6	Enter 55.	Display reads— TEST SEQ: 55
7	Press GO.	Display reads— TRANSMITTER=? 1=921 2=914 3=903
8	Enter 1, 2, or 3 to correspond to the type of data test set being used at the distant end.	Typical display reads (briefly)— TRANSMITTER=1 1=921 2=914 3=903 Display then reads (briefly)— SELECT ERROR TEST Display then reads— D=DT 0=SP 1=MK 2=2047 5=511 6=63

STEP	ACTION	VERIFICATION
9	Enter 5. ***Note:*** If distant end data test set is a 903, enter 6 instead of 5. Display reads (briefly)—63 BIT ERROR TEST.	Display reads (briefly)— 511 BIT ERROR TEST Display then reads— 1=BIT ERRORS 2=BLOCK ERRORS
10	Enter 1.	Display reads— ???? SECONDS
11	Discuss with far end the length of test. Then enter data mode at both ends.	
12	Enter 0900. ***Note:*** To perform functions listed below, press associated key. **KEY FUNCTION** A Repeat test. B Display time remaining in test. C Clear display. D End test. E Inject 8 errors into data stream. F Force out-of-sync condition.	Display reads (briefly)— 0900 SECONDS Display then reads— 0000 BITS IN ERROR From this point, display counts number of bits in error. If sync is lost during test, display flashes OSYN. If this occurs, test must be repeated by pressing A. At end of test, display reads TEST COMPLETE, total sync losses, and total bits in error. ***Requirement:*** Total bits in error are less than 6.
13	Remove jumper wire from common interface lead jacks on both DTSs.	

ETE Low-Speed Start-Stop Distortion Test

4.53 Connect and condition both 921A DTSs per the instructions in paragraph 4.11.

4.54 Condition both data sets as described in paragraph 4.49.

4.55 Connect a jumper wire between common interface lead jacks 10 and 23 on both DTSs.

4.56 Establish voice communication between the data stations and arrange to conduct an end-to-end low-speed start-stop distortion test.

4.57 Perform the test as follows.

STEP	ACTION	VERIFICATION
1	Press RST on keyboard. ***Note:*** If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display reads (briefly) version number of DTS. DTS then performs self tests. If DTS is defective, display reads— TEST FAILED.

STEP	ACTION	VERIFICATION
		If DTS is satisfactory, display reads— DATA SET.
2	Enter 36 on keyboard.	Display reads— DATA SET: 36
3	Press GO.	Display reads— BIT RATE:
4	Enter 03.	Display reads— BIT RATE: 03
5	Press GO.	Display reads— TEST SEQ:
6	Enter 52 79.	Display reads— TEST SEQ: 52 79
7	Press GO.	Display reads— PARITY=? (0=EVEN, 1=ODD)
8	Enter 0.	Display reads (briefly)— PARITY=0 (0=EVEN, 1=ODD) Display then reads— TRMT=? (1=MAN 2=CONT)
9	Enter 2. ***Note:*** Ignore display, PRESS A TO START.	Display reads (briefly)— TRMT=2 (1=MAN 2=CONT) Display then reads— PRESS A TO START
10	Press GO.	Display reads (briefly)— TEST INTERRUPTED Display then reads— MODE=? (1=RCV 2=RCV & TRMT)
11	Enter 2.	Display reads (briefly)— MODE=2 (1=RCV 2=RCV & TRMT) Display then reads— HITS OVER ??% (MAX=49%)
12	Enter 08.	Display reads (briefly)— HITS OVER 08% (MAX=49%) Display then reads— ???? SECONDS
13	Discuss with far end the length of test. Then enter data mode at both ends.	
14	Enter 0060 and after about 2 seconds, press C.	

STEP	ACTION	VERIFICATION
	Note: To perform functions listed below, press associated key.	
	KEY FUNCTION A Repeat test. B Display time remaining in test. C Clear display. D End test.	Display reads (briefly)— 0060 SECONDS Display then reads— PEAK=00% HITS=00/08 AVG BIAS=00% At end of test, display reads TEST COMPLETE and test results. ***Requirements:*** 1. Less than 09% peak distortion. 2. Less than 01/08 hits. 3. Less than 02% average bias distortion.
15	Remove jumper wire from common interface lead jacks on both DTSs.	

ETE High-Speed Synchronous Bit Error Test

4.58 Connect and condition both 921A DTSs per the instructions in paragraph 4.11.

4.59 Condition both data sets as follows.

(1) Verify that option YH is installed.

(2) Depress HS switch.

4.60 Establish voice communication between the data stations and arrange to conduct an end-to-end high-speed synchronous bit error test.

4.61 Perform the test as follows.

STEP	ACTION	VERIFICATION
1	Press RST on keyboard. *Note:* If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display reads (briefly) version number of DTS. DTS then performs self tests. If DTS is defective, display reads— TEST FAILED. If DTS is satisfactory, display reads— DATA SET:
2	Enter 66 on keyboard.	Display reads— DATA SET: 66
3	Press GO.	Display reads— BIT RATE:
4	Enter 12.	Display reads— BIT RATE: 12

STEP	ACTION	VERIFICATION
5	Press GO.	Display reads— TEST SEQ:
6	Enter 55.	Display reads— TEST SEQ: 55
7	Press GO.	Display reads— D=DT 0=SP 1=MK 2=2047 5=511 6=63
8	Enter 5. ***Note:*** If distant end data test set is a 903, enter 6 instead of 5. Display reads (briefly)—63 BIT ERROR TEST.	Display reads (briefly)— 511 BIT ERROR TEST Display then reads— 1=BIT ERRORS 2=BLOCK ERRORS
9	Enter 1.	Display reads— ???? SECONDS
10	Discuss with far end the length of test. Then enter data mode at both ends.	
11	Enter 0900. ***Note:*** To perform functions listed below, press associated key. **KEY FUNCTION** A Repeat test. B Display time remaining in test. C Clear display. D End test. E Inject 8 errors into data stream. F Force out-of-sync condition.	Display reads (briefly)— 0900 SECONDS Display then reads— 0000 BITS IN ERROR From this point, display counts number of bits in error. If sync is lost during test, display flashes OSYN. If this occurs, test must be repeated by pressing A. At end of test, display reads TEST COMPLETE, total sync losses, and total bits in error. ***Requirement:*** Total bits in error are less than 19.

ETE High-Speed Asynchronous Start-Stop Distortion Test—10-Bit Word

4.62 Connect and condition both 921A DTSs per the instructions in paragraph 4.11.

4.63 Condition both data sets as follows.

(1) Verify that options YG and YJ are installed.

(2) Depress HS switch.

4.64 Establish voice communications between the data stations and arrange to conduct an end-to-end high-speed asynchronous start-stop distortion test—10-bit word.

4.65 Perform the test as follows.

STEP	ACTION	VERIFICATION
1	Press RST on keyboard. ***Note:*** If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display reads (briefly) version number of DTS. DTS then performs self tests. If DTS is defective, display reads— TEST FAILED. If DTS is satisfactory, display reads— DATA SET:
2	Enter 36.	Display reads— DATA SET: 36
3	Press GO.	Display reads— BIT RATE:
4	Enter 12.	Display reads— BIT RATE: 12
5	Press GO.	Display reads— TEST SEQ:
6	Enter 52 79.	Display reads— TEST SEQ: 52 79
7	Press GO.	Display reads— BITS/CHAR=? (0=NINE 1=TEN)
8	Enter 1.	Display reads (briefly)— BITS/CHAR=1 (0=NINE 1=TEN) Display then reads— PARITY=? (0=EVEN, 1=ODD)
9	Enter 0.	Display reads (briefly)— PARITY=0 (0=EVEN, 1=ODD) Display then reads— TRMT=? (1=MAN 2=CONT)
10	Enter 2. ***Note:*** Ignore display, PRESS A TO START.	Display reads (briefly)— TRMT=2 (1=MAN 2=CONT) Display then reads— PRESS A TO START
11	Press GO.	Display reads (briefly)— TEST INTERRUPTED Display then reads— MODE=? (1=RCV 2=RCV & TRMT)
12	Enter 2.	Display reads (briefly)— MODE=2 (1=RCV 2=RCV & TRMT) Display then reads— BITS/CHAR=? (0=NINE 1=TEN)

STEP	ACTION	VERIFICATION
13	Enter 1.	Display reads (briefly)— BITS/CHAR=1 (0=NINE 1=TEN) Display then reads— HITS OVER ??% (MAX=49%)
14	Enter 16.	Display reads (briefly)— HITS OVER 16% (MAX=49%) Display then reads— ???? SECONDS
15	Discuss with far-end the length of test. Then enter data mode at both ends.	
16	ENTER 0060 and after about 2 seconds, press C. ***Note:*** To perform functions listed below, press associated key. **KEY FUNCTION** A Repeat test. B Display time remaining in test. C Clear display. D End test.	Display reads (briefly)— 0060 SECONDS Display then reads— PEAK=00% HITS=00/16 AVG BIAS=00% At end of test, display reads TEST COMPLETE and test results. ***Requirements:*** 1. Less than 17% peak distortion. 2. Less than 01/16 hits. 3. Less than 07% average bias distortion.

ETE High-Speed Asynchronous Start-Stop Distortion Test—9-Bit Word

4.66 The 9-bit word test and requirements are the same as the test and requirements for the 10-bit word described in paragraphs 4.62 through 4.65 with the following changes.

- Install option YI in both data sets.
- Step 8 enter "0" instead of "1"; display reads BITS/CHAR=0 (0=NINE 1=TEN).
- Omit Step 9.
- Step 13 enter "0" instead of "1"; display reads BITS/CHAR=0 (0=NINE 1=TEN).
- Step 14 enter 14 instead of 16; display reads HITS OVER 14% (MAX=49%).
- Step 16 change requirement 1 to less than 15% peak distortion and requirement 2 to less than 01/14 hits.

I. Automatic Answer Test

4.67 This test checks the ability of the data set to answer a call, go to the data mode, and terminate the call.

4.68 Connect and condition the 921A DTS per the instructions in paragraph 4.11.

4.69 Verify that option ZH (automatic answer—IN) and option U (send-space disconnect—OUT) are installed in data set.

4.70 Perform the test as follows.

STEP	ACTION	VERIFICATION
1	Press RST on keyboard. ***Note:*** If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display reads (briefly) version number of DTS. DTS then performs self tests. If DTS is defective, display reads— TEST FAILED. If DTS is satisfactory, display reads— DATA SET:
2	Enter 36 on keyboard.	Display reads— DATA SET: 36
3	Press GO.	Display reads— BIT RATE:
4	Enter 03.	Display reads— BIT RATE: 03
5	Press GO.	Display reads— TEST SEQ:
6	Enter 40.	Display reads— TEST SEQ: 40
7	Press GO.	Display reads— WAITING FOR RI
8	Place a call to data set from any convenient telephone set.	Display reads— RINGING (during ringing period—ring indicator lead **on**). ASSIGNABLE 1 indicator follows ring indicator lead. After 3 complete ringing cycles, DTR indicator lights (data terminal ready lead ***on***). After several seconds, DSR indicator lights (data set ready lead ***on***). Display then reads— ANSWERED After several more seconds, DTR indicator goes off (data terminal ready lead ***off***). Then DSR indicator immediately goes off (data set ready lead ***off***). ***Requirement:*** Display reads (briefly)— TEST PASSED

J. Interface Test

4.71 This test checks the ability of the data set to respond to interface control and to provide indications through the interface. The signals that the data set will respond to and the indications given depend on the options installed. In this test, the DS 212AR interface is checked using a 921A DTS. Some of these tests require assistance from the data test center (DTC).

4.72 ***Test of CN Circuit:*** This test checks the ability of the local data set to go into the analog loop mode under control of the CN interface lead.

4.73 Connect and condition the 921A DTS per the instructions in paragraph 4.11.

4.74 Verify that option YE (CN circuit—IN) is installed in data set.

4.75 Perform the test as follows.

STEP	ACTION	VERIFICATION
1	Connect jumper wires on DCE interface lead jacks as follows. If option XO is installed in data set, jumper 4 to 25. If option XN is installed in data set, jumper 4 to 18. If option XR is installed in data set, jumper 4 to 18 and 13 to 25.	
2	Press RST on keyboard. ***Note:*** If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display reads (briefly) version number of DTS. DTS then performs self tests. If DTS is defective, display reads— TEST FAILED. If DTS is satisfactory, display reads— DATA SET:
3	Enter 36 on keyboard.	Display reads— DATA SET: 36
4	Press GO.	Display reads— BIT RATE:
5	Enter 03.	Display reads— BIT RATE: 03
6	Press GO.	Display reads— TEST SEQ:
7	Enter 47 48 37.	Display reads (briefly)— TEST SEQ: 47 48 37 Display then reads— :37 DTR=? (0 OR 1)

STEP	ACTION	VERIFICATION
8	Enter 0.	Display reads— :37 DTR=0 (0 OR 1)
9	Enter 38 47.	Display reads— :37 DTR=0 (0 OR 1) 38 47
10	Press GO.	Display reads (briefly)— TEST COMPLETE Display then reads— SW CONN: X=?? Y=??
11	Enter 05 09.	Display reads (briefly)— SW CONN: X=05 Y=09 Display then reads— SW CONN: X=?? Y=??
12	Enter 16 10.	Display reads (briefly)— SW CONN: X=16 Y=10 Display then reads— SW CONN: X=?? Y=??
13	Enter 11 08.	Display reads (briefly)— SW CONN: X=11 Y=08 Display then reads— SW CONN: X=?? Y=??
14	Press GO. ***Note:*** S1 is controlled by key 1; S2 is controlled by key 2; S3 is controlled by key 3; S4 is controlled by key 4.	Display reads (briefly)— TEST INTERRUPTED Display then reads (briefly)— CROSS CONNECTIONS MANUALLY SET Display then reads (briefly)— TEST COMPLETE Display then reads (briefly)— CROSS CONNECTIONS MANUALLY SET Display then reads state of controlled switches. Display reads— S1=OFF S2=OFF S3=ON S4=ON
15	Press key 1.	Display reads— S1=ON S2=OFF S3=ON S4=ON ***Requirement:*** MB indicator lights on data set.
16	Press key 2.	Display reads— S1=ON S2=ON S3=ON S4=ON ***Requirements:*** On DTS, RLSD indicator lights and shortly thereafter CS indicator lights.

STEP	ACTION	VERIFICATION
		Note: If option XR is installed in data set, ASSIGNABLE 4 indicator lights on DTS.
17	Press GO.	Display reads (briefly)— TEST INTERRUPTED Display then reads (briefly)— CROSS CONNECTIONS MANUALLY SET Display then reads (briefly)— TEST COMPLETE Display then reads— TEST SEQ:
18	Remove jumper wires from DCE interface lead jacks.	

4.76 ***Test of Receive Space Disconnect—IN Option:*** This test checks the ability of the data set to disconnect (go on-hook) upon receiving a spacing signal from the distant data set.

4.77 Connect and condition the 921A DTS per the instructions in paragraph 4.11.

4.78 Verify that option V (receive space disconnect—IN) is installed in data set.

4.79 Perform the test as follows.

STEP	ACTION	VERIFICATION
1	Press RST on keyboard. *Note:* If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display reads (briefly) version number of DTS. DTS then performs self tests. If DTS is defective, display reads— TEST FAILED. If DTS is satisfactory, display reads— DATA SET:
2	Enter 36 on keyboard.	Display reads— DATA SET: 36
3	Press GO.	Display reads— BIT RATE:
4	Enter 03.	Display reads— BIT RATE: 03
5	Press GO.	Display reads— TEST SEQ:
6	Enter 37.	Display reads— TEST SEQ: 37 DTR=? (0 OR 1)
7	Enter 1.	Display reads— TEST SEQ: 37 DTR=1 (0 OR 1)

STEP	ACTION	VERIFICATION
8	Press GO.	Display reads (briefly)— TEST COMPLETE Display then reads— TEST SEQ:
9	Place a call to DTC and request DTC to place a call to local data set in low-speed mode and then send about 10 seconds of marking followed by at least 4 seconds of spacing.	
10	Answer call. If option ZG (automatic answer-OUT) is installed, answer call, go to data mode, and place handset on-hook.	***Requirements:*** On DTS, DSR indicator lights and shortly thereafter RLSD and CS indicators light.
11	When DTC sends spacing.	***Requirements:*** On DTS, RD-0 indicator lights and about 1-1/2 seconds later RLSD, DSR, and CS indicators go off (data set drops call).

4.80 ***Test of CB and CF Indications—COMMON Option:*** When option A (CB and CF indications—COMMON) is installed, the clear-to-send (CB) interface circuit is forced ***off*** whenever the received line signal detector (CF) interface circuit goes ***off.*** This test checks proper operation of this option.

4.81 Connect and condition the 921A DTS per the instructions in paragraph 4.11.

4.82 Verify that option A (CB and CF indications—COMMON) and option R (loss of carrier disconnect—OUT) are installed in data set.

4.83 Perform the test as follows.

STEP	ACTION	VERIFICATION
1	Press RST on keyboard. ***Note:*** If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display reads (briefly) version number of DTS. DTS then performs self tests. If DTS is defective, display reads— TEST FAILED. If DTS is satisfactory, display reads— DATA SET:
2	Enter 36 on keyboard.	Display reads— DATA SET: 36
3	Press GO.	Display reads— BIT RATE:
4	Enter 03.	Display reads— BIT RATE: 03

STEP	ACTION	VERIFICATION
5	Press GO.	Display reads— TEST SEQ:
6	Enter 37.	Display reads— TEST SEQ: 37 DTR=? (0 OR 1)
7	Enter 1.	Display reads— TEST SEQ: 37 DTR=1 (0 OR 1)
8	Press GO.	Display reads (briefly)— TEST COMPLETE Display then reads— TEST SEQ:
9	Place a call to DTC and request DTC to place a call to local data set in low-speed mode.	
10	Answer call. If option ZG (automatic answer-OUT) is installed, answer call, go to data mode, and place handset on-hook. ***Note:*** DTC should go to data mode after receiving answer tone.	***Requirements:*** On DTS, DSR indicator lights and shortly thereafter RLSD and CS indicators light.
11	Have DTC go from data mode to talk mode without dropping call (or go from TEST to TALK of 904 DTC)	***Requirements:*** On DTS, RLSD and CS indicators go off and DSR indicator remains lighted.

4.84 ***Test of Loss of Carrier Disconnect—IN Option:*** When option S (loss of carrier disconnect-IN) is installed, the data set terminates the call if carrier disappears from the line for approximately 350 ms. This test checks proper operation of this option.

4.85 Connect and condition the 921A DTS per the instructions in paragraph 4.11.

4.86 Verify that option S (loss of carrier disconnect—IN) is installed in data set.

4.87 Perform the test as follows.

STEP	ACTION	VERIFICATION
1	Press RST on keyboard. ***Note:*** If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display reads (briefly) version number of DTS. DTS then performs self tests. if DTS is defective, display reads— TEST FAILED. If DTS is satisfactory, display reads— DATA SET:
2	Enter 36 on keyboard.	Display reads— DATA SET: 36

STEP	ACTION	VERIFICATION
3	Press GO.	Display reads— BIT RATE:
4	Enter 03.	Display reads— BIT RATE: 03
5	Press GO.	Display reads— TEST SEQ:
6	Enter 37.	Display reads— TEST SEQ: 37 DTR=? (0 OR 1)
7	Enter 1.	Display reads— TEST SEQ: 37 DTR=1 (0 OR 1)
8	Press GO.	Display reads (briefly)— TEST COMPLETE Display then reads— TEST SEQ:
9	Place a call to DTC and request DTC to place a call to local data set in low-speed mode.	
10	Answer call. If option ZG (automatic answer-OUT) is installed, answer call, go to data mode, and place handset on-hook. ***Note:*** DTC should go to data mode after receiving answer tone.	***Requirements:*** On DTS, DSR indicator lights and shortly thereafter RLSD and CS indicators light.
11	Have DTC go from data mode to talk mode without dropping call (or go from TEST to TALK at 904 DTC).	***Requirements:*** On DTS, RLSD and CS indicators go off immediately. DSR indicator goes off in about 350 ms or after about 4 seconds if option T is installed in data set.

4.88 ***Test of Speed Mode—HIGH Option:*** When option YO (speed mode—HIGH) is installed, the data set will not pass data through the interface when in the low-speed mode. This test checks proper operation of this option.

4.89 Connect and condition the 921A DTS per the instructions in paragraph 4.11.

4.90 Condition data set as follows.

(1) Verify that option YO (speed mode—HIGH) is installed.

(2) Depress AL and HS switches.

4.91 Perform the test as follows.

STEP	ACTION	VERIFICATION
1	Press RST on keyboard. ***Note:*** If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display reads (briefly) version number of DTS. DTS then performs self tests. If DTS is defective, display reads— TEST FAILED. If DTS is satisfactory, display reads— DATA SET.

STEP	ACTION	VERIFICATION
2	Enter 36 on keyboard.	Display reads— DATA SET: 36
3	Press GO.	Display reads— BIT RATE:
4	Enter 03.	Display reads— BIT RATE: 03
5	Press GO.	Display reads— TEST SEQ:
6	Enter 53 37.	Display reads— TEST SEQ: 53 37 DTR=? (0 OR 1)
7	Enter 1.	Display reads (briefly)— TEST SEQ: 53 37 DTR=1 (0 OR 1) Display then reads—
8	Press GO.	Display reads (briefly)— SELECT ERROR TEST Display then reads— D=DT 0=SP 1=MK 2=2047 5=511 6=63
9	Press D.	Display reads— DOTTING BIT ERROR TEST
10	Press GO.	Display reads (briefly)— TEST INTERRUPTED Display then reads— TEST COMPLETE Display then reads— TEST SEQ: ***Requirements:*** On DTS, RLSD and CS indicators light steadily and both SD and RD indicators are flashing.
11	Release HS switch on data set.	***Requirements:*** On DTS, both RLSD and CS indicators go off and both SD indicators continue flashing. RD-1 indicator is on and RD-0 indicator is off.
12	Release AL switch on data set.	

4.92 ***Test of Speed Control—INTERFACE Option:*** When option XJ (speed control—INTERFACE) is installed, high-speed or low-speed operation of an originating data set is controlled through pin 23 of the customer's interface. This test checks proper operation of this option.

4.93 Connect and condition the 921A DTS per the instructions in paragraph 4.11.

4.94 Condition data set as follows.

(1) Verify that option XJ (speed control—INTERFACE) is installed.

(2) Depress AL switch.

4.95 Perform the test as follows.

STEP	ACTION	VERIFICATION
1	Connect a jumper wire between common interface lead jacks 20 and 23 on DTS.	
2	Press RST on keyboard. ***Note:*** If RST is pressed during a test, the test is ended and the DTS recycles to this step.	Display reads (briefly) version number of DTS. DTS then performs self tests. If DTS is defective, display reads— TEST FAILED. If DTS is satisfactory, display reads— DATA SET:
3	Enter 36 on keyboard.	Display reads— DATA SET: 36
4	Press GO.	Display reads— BIT RATE:
5	Enter 12.	Display reads— BIT RATE: 12
6	Press GO.	Display reads— TEST SEQ:
7	Enter 47 48 37.	Display reads (briefly)— TEST SEQ: 47 48 37 Display then reads— :37 DTR=? (0 OR 1)
8	Enter 1.	Display reads— :37 DTR=1 (0 OR 1)
9	Press GO.	Display reads (briefly)— TEST COMPLETE— Display then reads— SW CONN: X=?? Y=??
10	Enter 10 05.	Display reads (briefly)— SW CONN: X=10 Y=05 Display then reads— SW CONN: X=?? Y=?? ***Requirements:*** HS indicator on data set and ASSIGNABLE 1 indicator on DTS are lighted.

STEP	ACTION	VERIFICATION
11	Press GO.	Display reads (briefly)— TEST INTERRUPTED Display then reads (briefly)— CROSS CONNECTIONS MANUALLY SET Display then reads (briefly)— TEST COMPLETE Display then reads (briefly)— CROSS CONNECTIONS MANUALLY SET Display then reads— TEST SEQ: ***Requirements:*** HS indicator on data set and ASSIGNABLE 1 indicator on DTS go off.
12	Enter 47.	Display reads— TEST SEQ: 47
13	Press GO.	Display reads (briefly)— CROSS CONNECTIONS MANUALLY SET Display then reads (briefly)— TEST COMPLETE Display then reads— TEST SEQ:
14	Remove jumper wire from common interface lead jacks on DTS.	
15	Release AL switch on data set.	

5. REFERENCES

5.01 Additional information concerning the testing of DS 212AR is contained in the following publications:

SECTION	TITLE
107-402-100	921A Data Test Set—Description and Operation
314-205-501	Data Systems—DATAPHONE® Service and Data Access Arrangements on Direct Distance Dialing Network—Test Requirements for Subscriber, Foreign Exchange, and Remote Exchange Lines
592-039-100	Data Set 212AR-L1A/2A—Description and Operation
592-039-200	Data Set 212AR-L1A/2A—Installation and Connections
592-039-500	Data Set 212AR-L1A/2A—Test Procedures
668-010-300	Data Systems—DATAPHONE® Service on Direct Distance Dialing Network—Data Test Center—Trouble Analysis Procedures

5.02 Detailed information concerning DS 212AR is contained in CD- and SD-1D288-01.