DATASPEED TAPE-TO-TAPE SYSTEM

TYPE 1 AND TYPE 2 TAPE SENDERS AND RECEIVERS

ELECTRONIC CIRCUITRY

GENERAL DESCRIPTION AND PRINCIPLES OF OPERATION

CONTENTS PAGE

1. INTRODUCTION

1.01 This section presents both a general and detailed description of the electronic circuitry (with the exception of the power supply modules) used in the DATASPEED 1A and 2A Tape Senders and 1B and 2B Tape Receivers. Refer to related sections for information regarding the power supply module, and the electromechanical units, (ie, tape reader and tape punch) used in the Tape Sender and Tape Receivers.

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1.02 This section is reissued to incorporate information on the discrete calling feature, the break feature, the automatic answer and disconnect feature, and the new Y-connector kit. With the advent of the 202C and 202D data set and the provision of the reverse channel carrier facilities, the above features are applicable for send-receive terminals in a switched network system. This section also adds information with regard to the new application of existing kits. Refer to the section entitled "Type 1 and Type 2 Senders and Receivers, Installation and Checkout Procedures" for the data set terminal strapping requirements and/or Y-connector modifications of certain terminals. Arrows in the margins indicate changes and additions to the text.

1.03 The circuit description within this section assumes that the Tape Sender and/or Tape Receiver are operated with a Bell System type 202A data set. Provisions have been made for mounting these data sets directly within the Tape Sender or Tape Receiver cabinet.

2. GENERAL DESCRIPTION

TAPE SENDER

2.01 The Tape Sender converts the parallel output signals generated by the tape reader into a serial, start-stop signal for driving the modulator contained in the data set. A block diagram of a complete tape sender terminal is shown in the top half of Figure 1. The electronic components required to convert the parallel output signals from the reader into serial, start-stop form are a sending signal converter and a sending distributor. The signal converter and the sending distributor are each housed in separate electronic modular assemblies.

TAPE RECEIVER

2.02 The Tape Receiver converts the start-stop serial code from the data set to a parallel signal which will operate the tape reperforator. A block diagram of a complete tape receiver terminal is shown in the bottom half of Figure 1. The electronic components required to convert the start-stop serial code into parallel form are a receiving signal converter and a receiving distributor. The receiving distributor and the signal converter are each separately housed in electronic modular assemblies.

ELECTRONIC MODULES

2.03 The modules which house the electronics associated with the Tape Senders and Receivers are designed to provide easy access to the circuitry. They are of steel frame construction, and are 5-1/2 inches by 7 inches by 15 inches in dimension.

2.04 The electronic circuitry is contained on plug-in etched circuit cards. Each circuit card is equipped with accessible test points for voltmeter and oscilloscope checking. The modules are equipped with 15-pin connectors to accept each circuit card. Each connector is interconnected by surface wiring. All circuit components are contained on the pluggable circuit cards. All signal connectors and power supply connections are made through a connector mounted on the rear of each module.

TABLE 1 - MAXIMUM DC CURRENT DRAIN

Nominal Voltage	Sending Distributor (TTD)	Sending Signal Converter (TTSC)	Tape Sender Total Drain	Receiving Distributor (TRD)	Receiving Signal Converter (TRSC)	Tape Receiver Total Drain
+6	-	37MA	37MA	-	75MA	75MA
+1.5	131MA	4MA	135MA	130MA	135MA	265MA
-6	-	-	-	-	200MA	200MA
-6R	-21MA	-6MA	27MA	-25MA	-30MA	55MA
-12	170MA	51MA	221MA	230MA	240MA	470MA
-28	-	1900MA	1900MA	-	2200MA	2200MA

TABLE 2 - SIGNAL CHARACTERISTICS

Unit	Type	Code Levels	Baud	WPM
Sending Distributor	1 2	5 5 to 8	1050 1050	1050 1050
Sending Signal Converter	1 2	5 5 to 8	1050 1050	1050 1050
Tape Reader	1 2	5 5 to 8	1050 1050	1050 1050
Receiving Distributor	1 2	5 5 to 8	1050 1050	1050 1050
Receiving Signal Converter	1 2	5 5 to 8	1050 1050	1050 1050
Tape Reperforator	1 2	5 5 to 8	1050 1050	1050 1050

POWER AND SIGNAL REQUIREMENTS

A. Power Requirements

2.05 Power required for the above units is obtained from the power supply mounted in the lower enclosure of each terminal (multi-voltage rectifier (TP177149). Voltage and current requirements are listed in Table 1.

(a) Ac power - 115 v ac ±10 v ac 60 cycles.
250 watts (nominal max) Sender
300 watts (nominal max) Receiver

(b) Dc power - see Table 1.

B. Output Signal Requirements - Tape Sender

2.06 The tape sender terminal output signal has the following characteristics:

(1) Start-stop type polar signal.

(2) Nominal output signal voltage across a load of 1000 ohms.

(a) Space: +6 volts

(b) Mark: -6 volts

(3) Unit codes, code levels, baud (bits per second), and wpm (words per minute) are listed in Table 2.

C. Input Signal Requirements - Tape Receiver

2.07 The tape receiver terminal is designed to operate from an input signal with the following characteristics:

(1) Start-stop polar signal.

(2) Nominal input signal voltage from a 1,000-ohm source:

(a) Space: +3 v or more positive (+25 v maximum).

(b) Mark: -3 v or more negative (-25 v maximum).

(3) Unit codes, code levels, baud (bits per second), and wpm (words per minute) are listed in Table 2 above.

3. TAPE SENDER - PRINCIPLES OF OPERATION

GENERAL THEORY

A. Overall Operation

Note: Refer to tape sender terminal block diagram, Figure 2.

General

3.01 Electronic circuitry of tape sender terminal is physically and functionally divided into two parts: a sending signal converter and a sending distributor. The signal converter is represented by schematic diagram 3831WD and the sending distributor by 4439WD. All circuits are shown in symbolic logic. Each circuit is indicated by an EC number, an etched circuit board number, and a Z number which represents an element number. A detailed description of each circuit board can be obtained by referring to the respective part drawing. For information concerning power supply used with the above equipment, refer to appropriate 592 Division section.

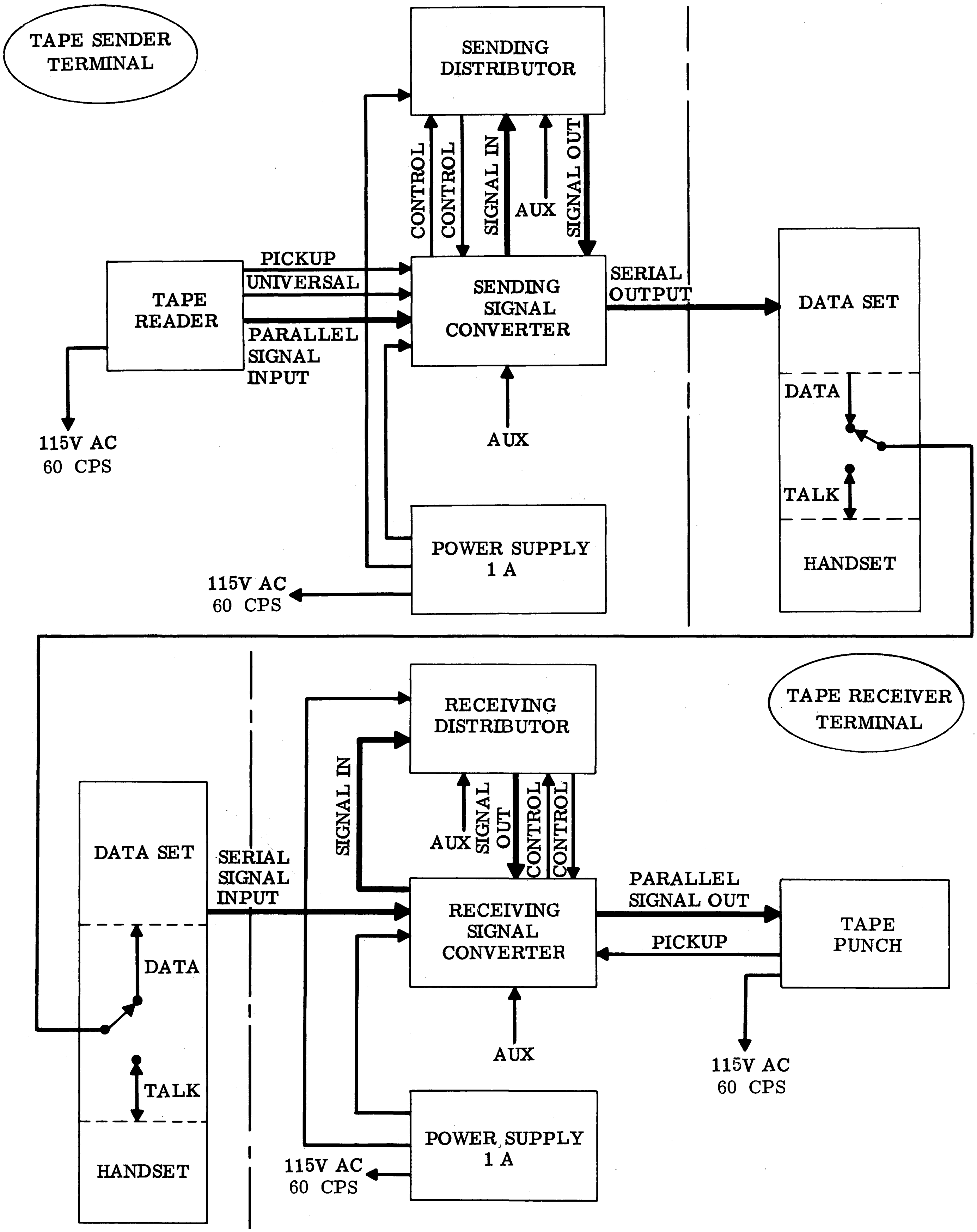


Figure 1-System Block Diagram

3.02 The function of the signal converter is to receive N-level parallel signals from the high speed tape reader, and convert the input to N standard output pulses (N refers to the number of code levels used). Type 1 units utilize 5-level code, while type 2 (universal) units may utilize 5- to 8-level code, depending upon selective conditions. The signal converter also converts the standard output of a sending distributor to signals suitable for driving the modulator of a data set.

3.03 The function of the sending distributor is to convert N parallel input pulses to an N-level binary start-stop code. The type 3 distributor contains 6 register elements and generates a 10-bit (1050 baud) code. The zero (0) level bit (which is the first bit after the start bit signal) is always transmitted as a mark. Bit levels 1 through 5 are used to transmit the serial information. After level 5 has been transmitted, a 3-bit stop pulse will follow where normally levels 6 and 7 along with the unity stop pulse bit are transmitted. The type 2 distributor contains 8 register elements, and will accept up to 8 information pulses. If level zero (0) is not used, it will be transmitted as a space pulse. If levels 6 and 7 are not used, each will be transmitted as a mark pulse along with the unity stop pulse.

Operation

3.04 The heart of the circuit operation is the signal register in the sending distributor. This group of circuit elements, commonly known as a shift register, is arranged so that each element of the register accepts one code information bit at the same time the respective level in the tape is sensed by the tape reader. This information is accepted in parallel form. Since only one bit can be transmitted at a time, the information is then shifted out of the register, each bit in succession, until all the bits have been transmitted. This occurs during the time the tape is being advanced to the next character. Before the next character is read, the register is reset to accept the new information.

3.05 The basic block diagram, Figure 2, is arranged to illustrate the functions of the various sections of the tape sender terminal. Note that there are two sources of timing in this unit. One timing signal is developed in a magnetic pickup on the tape reader, and is used to initiate the stop pulse for each character. This pulse, then, occurs at the character rate. The other timing signal operates at the bit rate and is used to advance the code in the shift register. This timing signal is generated by the start-stop oscillator (see Figure 2). During the stop interval, the start-stop oscillator is stopped, and is then restarted at the beginning of the next start pulse. This assures that the deviation in the bit rate will not be cumulative and that the first code bit will always occur at the proper instant with regard to the machine character rate.

B. Signal Converter (Sending)

3.06 The signal converter contains the signal inhibit gate, pickup pulse amplifier, and output signal amplifier.

3.07 The pickup pulse amplifier shapes and amplifies the magnetic pickup output, and sends it to the signal delay in the sending distributor.

3.08 The inhibit gates transmit the signal from the reader contacts to the signal register in the sending distributor.

3.09 The output amplifier converts the signal from the sending distributor to a signal having the characteristics necessary to drive the data set.

C. Sending Distributor

3.10 When the unit is initially turned on, a reset pulse is automatically generated to reset the output element of the signal register. The start-stop oscillator (advance pulse generator) is controlled by a bi-stable circuit called the oscillator control. The stop condition is initiated by the timing signal from the magnetic pickup. The timing signal is applied to the stop timer, a mono-stable device which develops a signal approximately equal in duration to the desired stop pulse. This signal is then applied to the start pulse gate through the start amplifier. If the gate is open, it will pass the trailing edge of the stop pulse (beginning of start) to the oscillator start lead of the oscillator control to provide the start condition. The start pulse gate is under the control of the universal contact in the tape reader. This contact closes for every character position on the tape as it is being pulled through the reader. Thus, if tape is being read, the oscillator will start; but if tape is not being read, the gate will remain closed, the oscillator will not start, and the unit will generate a continuous stop signal.

3.11 The sample delay circuit, which is also triggered at the end of the stop pulse, develops a pulse to control the inhibit gates in the signal converter, and to control the pulse control gate. This control pulse is delayed approximately one half a bit, since the signal register must have time to generate a start signal before the new character code is set into it. When this set "1" pulse is applied to the inhibit gates, the information from the reader contacts is supplied through the gates to set the elements of the signal register to record the code. When the contact is closed, it represents a MARK condition (a hole in the tape) and the corresponding shift register element is set to the "1" condition. If it is SPACE (no hole in tape) the register element remains in the "0" condition. When the sample delay is applied to the pulse control gate, it enables the set "0" side, providing a set "0" pulse for the signal registers, and inhibits the "advance pulses" side to prevent a false signal from being sent on the line. Upon relaxing, the set "0" is inhibited and the "advance pulse" side is enabled so information can be shifted through the register.

3.12 The last element of the signal register (labeled R on the block diagram, Figure 2) does not receive a code pulse. At the end of the previous character, this element was left in the "1" condition as will be shown below. When the set "0" pulse arrives, the R element will be shifted to the "0" condition, causing a space to be generated representing the start pulse. Immediately following this, the information is set into the register. The next advance pulse shifts this entire code one element to the right, bringing the first bit of the code from element 1 to element R. This produces an output signal corresponding to the first bit. With the next advance pulse, the code is advanced another position to the right so that now the second bit is in element R, producing an output signal which represents that bit. This action continues until all bits have been advanced out of the register, each bit producing its output signal in turn.

3.13 Element R is continuously primed in such a way that it will be shifted to the "1" state by the first advance pulse following reset, and will remain that way until the next set "0" pulse. This condition is transferred down the shift register, causing each element to go to the "1" state as the last code bit is shifted out of it. Thus, the stop pulse is generated in element R when the last bit is shifted out of it, since it will be set to the "1" state. It will remain in this state until the next set "0" pulse causes it to shift to SPACE to create the start pulse of the next character. If no code is to be transmitted, due to no tape in the reader or the reader having been stopped, advance pulses would not be generated since no start pulse would be received by the oscillator control (universal contact open). Thus, element R would remain in the "1" state generating a continuous mark or stop signal until the code transmission is resumed.

DETAILED CIRCUIT DESCRIPTION

A. Signal Converter (Sending)

Note: Refer to Schematic Wiring Diagram 3831WD.

Initial Conditions

3.14 The first action which takes place in the signal converter is automatic reset. This occurs when the power switch is turned on. At this time -6 volts is applied to terminal H of the integrator pulse shaper, Z210. This circuit, after a delay of about 300 milliseconds, provides a negative-going pulse on terminal K. The pulse is applied to the input terminal D, of the pulse amplifier circuit, Z211B. The pulse amplifier produces a positive-going -6 volt to 0 volt pulse and sends it to terminal C6 of connector J201. From terminal C6, the signal is sent to the reset of the output element of the signal register.

3.15 The timing signal from the magnetic pickup of the reader is applied to terminal C1 of connector J201 and from there to terminal A of Z209A. The lead on terminal B1 of J201 applies a -6 volt bias to the pickup coil and the pickup amplifier. The timing signal leaves terminal L of the pickup amplifier, and is inverted by Z209B. The output of Z209B is sent to the sending distributor through terminal C2 of connector J201.

Reader Input

3.16 The tape reader mark contacts are connected to integrators Z201A-E through Z202A-D. The integrators are used to clean up any noise which may be caused by the mechanical switching of the tape reader contacts. The outputs of the integrators are applied to the prime input of inhibit gates Z203 through Z206, and a sample pulse is sent from the sending distributor via connector J101, terminal F2, to the drive side of the inhibit gates. At this time, all inhibit gates which are primed by the integrators pass a positive-going -6 volts to 0 volt pulse to OR gates Z207A-D through Z208A-D, and from them via J201 to the sending distributor. The function of the OR gate is described in Paragraph 3.35.

Universal Input

3.17 The universal signal from the reader is applied to terminal E of the integrator, Z202D, through connector J201, terminal H9. The output, terminal P of Z202D, appears on terminal C4 of J201. Subsequently, this signal is applied to the sending distributor.

Polar Signal Output

3.18 The parallel input signal is transferred from the signal converter to the sending distributor, and the serial output signal from the distributor is applied to the data set 202A. It is necessary, therefore, to convert the dc neutral signal from the sending distributor to a polar signal capable of driving the data set. This signal conversion is accomplished by an amplifier, Z212A. The signal from the sending distributor is applied to terminal C10, connector J201; from there it goes to terminal B of Z211A, an inverter. The signal output of the inverter is applied to terminal F of output amplifier Z212A, which converts the signal to a +6 volts and -6 volts polar signal. The output of the amplifier terminal P, is sent to the data set through terminal D10, connector J201.

Request-to Send

3.19 The data set requires a signal to inform it that the sending distributor is ready to send. This signal is called the request to send. The signal is provided by applying some bias through element Z212B to an external switch (ie, reader motor switch). When the switch is open, -12 volts is applied to the data set via terminals E1 and D1 of J201. The request to send is off in the above condition. When the external switch is closed, +6 volts appears on the request to send lead; this is the on condition. On High Speed Tape-to-Tape System units, the data set request to send lead is permanently biased on with +17.5 volts.

Power Requirements

3.20 Power is applied through connector J201 to the module from the dc power supply. Minus 6 volts is found on terminal A4, +1.5 volts on terminal B8, -12 volts on terminal B7, and +6 volts on terminal B3. From these points the voltages are passed through filter elements Z213A-B through Z214A-B, which filter out extraneous noise. Terminal B4 has -28 volts; terminal B6 is circuit ground and terminal B5 is frame ground.

B. Sending Distributor

Note: Refer to Schematic Wiring Diagram 4439WD, and timing diagram, Figure 3.

Initial Conditions

3.21 The first action to occur in the sending distributor is automatic reset. When the power switch is put in the ON position, a -6 volt to 0 volt pulse is generated in the signal converter (see Paragraph 3.14) and applied to terminal C6, connector J101. This pulse is presented to the set "1A" input of the output element, Z110, terminal C, in the signal register switching the normal output, terminal L, to 0 volt. This places a stop signal on the line, keeping it closed.

Clock Pulse

3.22 While the reader motor is running, a clock pulse, shaped in the signal converter, is applied through terminal C2, connector J101, to the signal delay input. The signal delay output, which is identical to its input only delayed about 50 microseconds, is applied to the stop timer's set "1" input and the oscillator control's set "0A" input. The clock pulse applied to terminal D of Z104, the oscillator control, switches the normal output, terminal L, to -6 volts to turn off the start-stop oscillator, Z108. The clock pulse is also applied to the set "1" input of the stop timer, Z101, terminal C, causing the output, terminal L, to go from -6 volts to 0 volt and remain at that potential for a period of time a little less than a bit in length.

Stop Timer

3.23 When the Z101 one-shot times out, its normal output will relax and produce a negative transition from 0 to -6 volts. This negative transition is applied to terminal B of start amplifier Z102A, a pulse amplifier, which generates a positive-going -6 volt to 0 volt pulse on its output, terminal K.

Oscillator Control

3.24 The positive pulse from Z102A is applied to the inhibit gate, Z103B, terminal N. If there is no tape in the reader, the universal contact will be open and zero volt appears on terminal D of inhibit gate Z103B. If a tape is in the sensing head and the reader is operating, the universal contact is closed and a -6 volts or greater signal is sent from the signal converter to connector J101, terminal C4, and from there to terminal D of the inhibit gate. The presence of this signal on terminal D permits the positive signal applied on terminal N to pass through the inhibit gate and on to the oscillator control flip-flop.

3.25 The oscillator control flip-flop, Z104, receives the positive-going pulse on terminal C. The pulse causes the circuit to switch and the normal output, terminal L, goes to 0 volt. This signal is now applied to the sample delay circuit, Z105, and the start-stop oscillator, Z108.

Sample Delay

3.26 The positive-going signal from the oscillator control, Z104, is received on the set "1" input, terminal C, of the sample delay, Z105. This one-shot serves two functions: (1) it provides the initial signal for the sample lead, and (2) it provides one pulse for the signal register reset. The sample delay one-shot goes negative on its inverted output, terminal K, and positive on its normal output, terminal L. The negative transition primes the set "0" side of the pulse control gate, Z106A, terminal B and permits the first pulse from the squaring amplifier to pass through this gate to set "0" all the signal registers (Z110 through Z115, Z116, Z117, or Z118 depending on number of levels). When the sample delay one-shot, Z105, relaxes, its inverted output goes to 0 volt and removes the prime from the set "0" side of the pulse control gate, Z106A. Simultaneously, the normal output of Z105 goes to -6 volts and primes the advance pulse side of the pulse control gate, Z106B, terminal D, allowing pulses from the squaring amplifier to pass through. The negative transition from the normal output is also sent to the input of the set "1" amplifier, Z102B, terminal D.

Start-Stop Oscillator

3.27 The start-stop oscillator, Z108, receives a -6 volt to 0 volt signal from the oscillator control flip-flop as described in Paragraph 3.25. The oscillator begins to oscillate as soon as the 0 volt signal is applied to its input terminal. The output appears as sinusoidal oscillations on terminal A, and is sent to the input of the squaring amplifier, Z109, terminal H. The squaring amplifier shapes the sine-wave in such a way as to produce a positive going -6 volts to 0 volt transition every cycle. Thus, one pulse is produced in every period of the sine-wave cycle. The time interval between the clock pulses and the frequency of the start-stop oscillator will permit only N+2 pulses on terminal A of Z109.

Squaring Amplifier

3.28 The pulses from the squaring amplifier are applied to the pulse control gate, Z106A and Z106B, on terminal A and terminal N, respectively. The sample delay one-shot primes terminal B of the pulse control gate long enough to permit the first pulse from the squaring amplifier to pass through to terminal K. This positive-going pulse is applied to the set "0A" input, terminal D, of the signal register, and resets all the registers to the set "0" condition prior to their receiving information from the signal converter.

Pulse Control Gate

3.29 The positive signal from the sample delay closes the advance pulses side of the pulse control gate, terminal D, Z106B, long enough to prevent the first pulse from the squaring amplifier from passing through the gate. The N+1 remaining pulses are passed through the gate's output, terminal L, and on to the set "1B" and set "0B" inputs on all the signal registers and the output element (terminals E and F, Z110 to Z118).

3.30 The negative-going signal which occurs when the sample delay one-shot, Z105, relaxes appears on terminal L. This signal is applied to terminal D of pulse amplifier Z102B, which generates a positive-going pulse, -6 volts to 0 volt, on its output at terminal L. The pulse is sent to terminal B of emitter follower Z103A. The output of Z103A is wired to connector J101, terminal C3, and is designated as the sample lead. The positive-going pulse on the sample lead is sent to the signal converter to trigger the inhibit gates passing the reader information into the signal register elements (refer to Paragraph 3.16).

Sample Pulse

3.31 When the sample pulse is sent from the set "1" amplifier (Z102B and Z103A) in the sending distributor to the inhibit gates in the signal converter, any inhibit gate which has a MARK condition on its input (-6 volts on terminal B or D) will pass a positive-going pulse to the sending distributor via connector J101, terminals D2 through D9, and from there to the storage registers set "1A" input, terminal C or Z111 through Z115, Z116, Z117, or Z118 (depending on number of code levels). Thus, if a

MARK condition appears in the reader, the corresponding signal register flip-flop switches to a set "1" condition (terminal L of flip-flops at 0 volt).

Signal Register

3.32 For purposes of description, assume that a MARK input is appearing only in the 4th level. Thus, only the flip-flop, Z114, will go into the set "1" condition; in this condition, its normal output, terminal L, will be at 0 volt and its inverted output, terminal K, will be at -6 volts. The normal output is wired to the prime "1B" input of the 3rd level flip-flop, Z113, terminal J, and the inverted output is wired to the prime "0B" input of Z113, terminal H. In this particular example, the 3rd level flip-flop will have its prime "1B" input primed, and when the 1st advance pulse arrives at the set "1B" input, terminal E, this flip-flop switches from the set "0" state to the set "1" state.

3.33 When the MARK pulse is passed from the 4th level to the 3rd level (that is, from Z114 to Z113), the 2nd level prime "1B" terminal is primed and the prime "0B" terminal remains at -6 volts. Thus, when the second advance pulse arrives at terminals E and F of Z112, and as each advance pulse comes in, this MARK signal is passed from the 3rd element to the 2nd element and so on until the N+1 advance pulse arrives. At this time the MARK signal is transferred into the output element of the register and then to the data set. Emitter follower Z107, passes the output signal from element Z110 to terminal C10 of connector J101.

C. Auxiliary Connections

3.34 All auxiliary connections, needed to operate in conjunction with supplementary equipment, are available at connector J202 of the singal converter.

3.35 Additional levels 0 through 7 are available, (terminals F3, F4, F5, F6, F7, F8, F9, and G2) to permit insertion of additional characters in the signal registers through OR gates Z207A to D through Z208A to D.

3.36 The sample lead is connected to terminal F2 of connector J201, and is used to let the auxiliary equipment know that the information has been passed into the signal registers.

3.37 Terminals G3, G4, and G5 on J201 in the signal converter are used to provide -28 volts, signal ground, and frame ground connections.

3.38 A start lead is connected to terminal C5, J101 in the sending distributor. This lead is wired to the output of the start amplifier, Z102A, terminal K, and will permit the auxiliary equipment to use the clock pulse as described in Paragraph 3.15.

3.39 The oscillator control is connected to terminal C1 of connector J101 in the sending distributor. This lead is wired to the set "1B" input of the oscillator control flip-flop, terminal E, Z104. It provides a means for equipment to turn on the oscillator.

4. TAPE RECEIVER - PRINCIPLES OF OPERATION

GENERAL THEORY

A. Overall Operation

Note: Refer to tape receiver terminal block diagram, Figure 4.

General

4.01 The electronic circuitry of the tape receiver terminal is physically and functionally divided into two parts: a receiving signal converter and a receiving distributor. The signal converter is represented by schematic 3833WD, and the receiving distributor by 4441WD. All circuits are shown in symbolic logic. Each circuit is indicated by an EC number, an etched circuit board number, and a Z number which represents an element number. A detailed description of each circuit can be obtained by referring to the respective drawing. For information concerning the power supply used with the above equipment refer to the appropriate 592 Division section.

4.02 The function of the receiving distributor is to separate the N-bit serial input telegraph code into an N-level parallel binary output signal (N refers to the number of code levels used). The function of the receiving signal converter is to provide buffer storage and change the N-level parallel electrical pulses into an N-level driving signal for the tape reperforator. Type 1 units utilize 5-level code, while type 2 (universal) units may utilize 5 to 8 level code depending upon selective conditions.

Operation

4.03 Like the tape sender terminal (Paragraph 3.04), the operation of the receiving terminal centers around the signal register. In the receiving terminal, however, the code is advanced into the register as it arrives, and then is shifted out of each element simultaneously to a storage register as shown in the block diagram, Figure 4. The code remains in the storage register until the punch is ready to operate, and is then transferred into magnet pulsers which cause the proper punch position to be energized.

4.04 Since the operation of this system depends upon synchronizing mechanical motion of the punch at the receiving terminal with the motion of the tape reader at the tape sender terminal, the control functions at the receiver are considerably more complex than at the transmitter. So that there will always be a new character position available on the tape, the tape punch is made to run slightly faster than the tape reader. In this way, a character will never be lost for want of a place in which to punch it.

4.05 The major control function in the receiving distributor is accomplished by the control register. In Figure 4, the output lead of the control register has been labeled control bus to show its importance in the operation of this equipment. The control register is responsible for the following:

(a) Starting and stopping the sensing operation of the signal register.

(b) Shifting the code from the signal register to storage in the signal converter.

(c) Priming the storage register to allow transfer of the code to the magnet pulsers.

4.06 The basic operation of the receiving distributor and the receiving signal converter can be best understood by following the sequence of events which occurs as a code group for a character arrives. The following conditions exist prior to receiving the character.

(a) Signal register: Set "1"

(b) Advance pulse generator: Off

(c) Control register: Set "0"

(d) Signal gate: Open

(e) Transfer prime: Set "1"

(f) Storage register: Storing last character

(g) Input gate: Open

(h) Start OR gate: Closed

(i) Start AND gate: Open

4.07 Two distinct timing operations occur in the receiver terminal. These are related to the basic operating actions (ie, code punching and code registering), and occur throughout the same interval.

B. Signal Converter (Receiving)

4.08 The first operation to be considered is the punching process. The above list of conditions (Paragraph 4.06) following the reception of the last complete character, shows that the character is stored in the storage register. A timing pulse generated in the magnetic pickup on the punch is converted to a pulse by the pickup pulse amplifier and presented to the variable delay circuit. The variable delay acts like a one-shot whose delay time changes as a function of the transfer prime's condition. Since the transfer one-shot is primed by the transfer prime, the trigger pulse will be passed through the transfer pulse generator to operate the magnet pulsers. The magnet pulsers are so arranged that the feed magnet is energized together with the code magnets that are primed from the code in the storage register. Thus, holes are punched in the tape representing the code stored in the storage register.

4.09 The punching operation must take place within the character interval following the shifting of code into the storage register. Thus, the punch period must be less than this time (about 95 to 98 per cent of the character interval).

C. Receiving Distributor

4.10 During the waiting period for the punching to take place, a new code group may be forming in the signal register. This action, that is code registering, will be considered next. An input signal applied to the signal gate, finding the gate open, passes through this gate and actuates the register drive circuit. The register drive circuit reshapes the input signal so that the transitions between bits displays the rapid rise time desired, and corrects for some of the deterioration of the signal that may have occured along the line. The output of the register drive is applied to the signal register, where it is advanced into the register one bit at a time under the control of the advance pulses.

4.11 The start-stop oscillator is turned off between code groups and must, therefore, be turned on again before the signal can be registered. The start-stop oscillator determines the bit rate. Since this is one of the circuits controlled by the control register, the control register must be in the "1" state in order to get the start-stop oscillator started. The incoming code group, after being shaped in the register drive, is applied to one of the inputs on the now open input gate. The first element (bit) of this code group is the start pulse, which triggers the start delay circuit after it passed through the input gate. The signal developed is equal to approximately one-half of a bit in length, and is used to delay the sampling of each bit until about its midpoint. This position was selected as being the most reliable under poor transmission conditions.

4.12 The output of the start delay is applied to the start OR gate which was opened when the start pulse passed through the signal delay circuit. This delay is provided to aid in the prevention of false starts. Since the action here is more of the integrator type action, only pulses of long duration will pass through it. Thus, short noise pulses ("hits") on the line will not be applied to the start gate, and this gate will not open to a false start. When a true start pulse is applied through the delay to the start gate, the gate will open and the pulse from the start delay circuit will pass through the start gate. The trailing edge of this pulse is formed into a trigger pulse in the start pulse amplifier, and applied to the control register.

4.13 Upon receipt of the trigger pulse, the control register shifts to its "1" state and causes the following action to take place:

(a) Start-stop oscillator starts.

(b) Start AND gate closes.

(c) Prime is removed from start delay.

The first advance pulse is generated about 50 microseconds after the start-stop oscillator is turned on, and causes the start pulse to register in the Nth element of the signal register. Since this is a space, it causes this element to return to the "0" state. (All signal register elements were set in the "1" state before the code arrived.)

4.14 The closing of the start AND gate, and removal of the prime from the start delay prevents any further transitions in the code input from feeding through to the control register and causing it to operate too soon.

4.15 All the register elements will receive a shift pulse, but no shift takes place since all but the first (Nth) element in the signal register are in the "1" state and the prime is in the "1" state.

4.16 About the middle of the first code bit, the second advance pulse occurs causing the "0" condition of the Nth element to advance to element N-1, and the code bit to be registered in the Nth element. With the arrival of the next advance pulse, the "0" condition in element N-1 moves to element N-2; the state of element N moves to element N-1, and the new code bit is registered in the Nth element. This continues as each advance pulse arrives until, with the N-1 code bit, the start pulse, registered as state "0", will have advanced to element 1, and the N registered bits will be recorded in elements 2 through N. The next advance pulse moves all code bits and the start pulse one position to the right, advancing the start pulse into the control register and registering the last code bit in element N. The control register, upon receipt of the start pulse, shifts from the "1" state to the "0" state, causing the following action to take place:

(a) Start-stop oscillator stops.

(b) Stop inserter develops signal, priming synchronizer flip-flop.

(c) Synchronizer flip-flop triggers, closing signal gate.

(d) Start delay is primed.

(e) Start AND gate opens.

(f) The 100-microsecond shift delay circuit is triggered.

(g) The 200-microsecond set "1" delay circuit is triggered.

4.17 With the signal gate closed, no further transitions on the line will affect the operation of the receiver until the stop inserter acts to open the signal gate. After an elapse of 100 microseconds, the signal applied to the shift delay circuit emerges and causes each element of the storage register to shift to the same state as its corresponding element in the signal register. Thus, the information is cleared from the signal register and stored in the storage register. There, 200 microseconds after the last advance pulse, the set "1" pulse emerges from the set "1" delay circuit. This pulse is used to reset the signal register to its "1" condition, and the transfer prime to its "1" condition. The signal register is now prepared to accept a new code.

4.18 The transfer prime circuit, together with the variable delay, determines the amount of time the transfer pulse is delayed from the pickup pulse. This delay is necessary to prevent loss of a character due to the jitter of the incoming signal.

4.19 The synchronizer flip-flop, which is triggered by the stop inserter, keeps the signal gate closed during the stop time. The gate then opens, and is ready to accept a start signal at any time after this. With the next start pulse, the cycle will begin over again, and the same sequence of operation will be repeated to register and punch the next code character.

DETAILED CIRCUIT DESCRIPTION

A. Signal Converter (Receiving)

Note: Refer to Schematic Wiring Diagram 3833WD.

Initial Conditions

4.20 Initially, when the power switch is turned ON, -6 volts is applied to terminal H of the integrator pulse shaper Z405. After a delay of about 100 to 300 milliseconds, Z405 provides a negative going transition on its output, terminal K. This signal is applied to the input of pulse amplifier Z408B, terminal D, which produces a positive-going pulse, -6 volts to 0 volt, on its output, terminal L. This positive pulse is sent to terminal E4 of connector J401, and from there to the receiving distributor to reset the control register (see Paragraph 4.37).

Storage Register

4.21 The normal and inverted sides of the signal register in the receiving distributor are applied through connector J401 to the prime "1B" and prime "0B" inputs of the signal converter storage register elements, terminals E and F of Z411 through Z418. Thus, if a particular bit is a MARK in a signal register element, that element will be in the set "1" condition and its normal output will prime the "1B" input of the corresponding flip-flop in the storage register. When the shift pulse from the receiving distributor, which comes in on terminal C1 of connector J401, is applied to the set "1B" input of this storage register element. it switches to the set "1" condition. If a SPACE condition exists in a signal register element, the corresponding storage register element will shift to the set "0" condition when the shift pulse comes in on its set "0B" lead, terminal F of Z411, Z412, or Z413 through Z418, depending on the number of code levels used.

4.22 If any of the elements in the storage register are in the set "1" condition, this provides a prime for their respective magnet pulsers on terminal E. A transfer pulse on the input of the magnet pulser, terminal B, will cause the primed magnet pulsers to fire and remain on for a period of approximately 4.5 milliseconds. The output of this card, terminal A, Z419 through Z427, is applied to the punch magnets. When triggered, the output of the magnet pulser, terminal A, switches from -28 volts to ground.

Transfer Circuitry

4.23 One hundred (100) microseconds after the information is passed from the signal register into the storage register, a transfer prime pulse from the set "1" delay appears at terminal B1 of connector J401. This pulse is sent to the set "1A" input of the transfer prime flip-flop, terminal C of Z403, causing this flip-flop to switch to the set "1" condition. The normal output, terminal L, goes to 0 volt and is sent to the prime "1" input of the transfer one-shot, Z407. The inverted side of the transfer flip-flop, terminal K, goes to -6 volts and is applied to the bias input of the variable pulse delay circuit, terminal A of Z406. The pickup pulse is received from the punch on terminal D1 of connector J402 and is sent to the pickup amplifier, terminal A, Z404A. The output of the pickup amplifier, terminal L, is applied to the input of the pickup inverter circuit, terminal F, Z404B. The output of Z404B produces a positive-going pulse (-6 volts to 0 volt) which is applied to the set "1" input of the variable pulse delay, terminal C.

4.24 The variable pulse delay circuit now acts like a one-shot triggered by the output of the pickup inverter; however, the time duration of the variable pulse delay circuit depends on the amount of time the bias signal exists on terminal A of Z406, and the pickup pulse is applied to the set "1" input, terminal C. Thus, after a period of time, the variable pulse delay relaxes and produces a positive going pulse on its inverted output, terminal K. This output is applied to terminal C of Z407, the transfer one-shot, causing it to fire. The time-out of the pulse delay varies between 0.4 to 1.2 milliseconds.

4.25 A positive transition occurs initially on the normal output of Z407, terminal L, and is applied to the set "0A" input of the transfer prime flip-flop, terminal D of Z403, switching it to the set "0" condition. A negative transition occurs on the normal output of the transfer one-shot 100 microseconds after the receipt of a pulse from the variable pulse delay, and is applied to the input of pulse amplifier Z408A, terminal B. See Paragraphs 4.28 through 4.34 for a detailed description of the variable pulse delay circuit, and Paragraphs 4.35 through 4.36 for a detailed description of the transfer circuitry timing.

Magnet Pulsers

4.26 The pulse amplifier produces a positive-going pulse, -6 volts to 0 volt, and applies it to the input of inhibit gate Z402B, terminal N. The pulse is passed through the gate and is applied to the input of emitter follower Z409, terminal B. The output of Z409 is applied to terminal B of all the magnet pulsers, Z419 through Z427, causing all the magnet pulsers primed by the set "1" condition of the storage registers to fire. Since the feed magnet pulser, Z419, is continuously primed (ground on terminal E), it always fires upon the receipt of a transfer pulse. The firing of the magnet pulsers provides a ground path for the corresponding magnets in the punch. This causes those magnets to energize, punching the stored information into the tape.

Incoming Signal

4.27 The incoming signal from the data set is received on terminal D10 of connector J401 in polar form. This input is converted to a -6 volt to 0 volt signal by passing it through the receiver input amplifier, Z401. The output of Z401 appears at terminal C10 of connector J401. From here, the signal is applied to the signal input of the receiving distributor.

B. Variable Pulse Delay Circuit

General

4.28 The variable delay is used in the tape receiver terminal for two reasons. First, to develop a proper time relationship between the pickup and the transfer prime, and second, to generate a transfer pulse for the magnet pulsers. The reader, at the tape sender terminal, has inherent mechanical jitter which appears on the signal, causing the start pulse to occur at slightly different times each cycle. At a critical time in the punching operation, this jitter could possibly cause the loss of a whole character. The variable delay circuit prevents this from occuring.

4.29 The variable delay circuit is a stable-state device which may be switched to a semi-stable condition. It will remain in its semi-stable state for a length of time determined by a bias prime which acts to effect the time-out of the circuit. Figure 5(A) is a schematic representation of this circuit. Its element number is Z406 (EC351), and it is used in the receiving signal converter (3833WD).

Operation - Fixed Bias Prime

4.30 Stable state: In the normal stable-state condition of the circuit, Q2 is forward biased and Q1 is reverse biased. Q2 is forward biased by virtue of the -6 volt potential on its base through R10 and R2. Its collector potential, about 0.85 volt, holds Q1 in the OFF condition. The 0.85 volt potential at the collector of Q2 is derived from the emitter side of R9 and, therefore, also appears at the emitter of Q1.

4.31 Triggering:

Note: During the following discussion, reference is made to Figure 5(B). This figure portrays the wave forms which appear at the various points mentioned below, and which are circled on Figure 5(A).

A positive going square wave applied at the input, C, of the differentiator network produces a positive pulse at point A. This pulse reverse biases Q2, turning it OFF. The collector of Q2 drops to -6 volts (point B), clamped at that potential by CR3. The negative transition is coupled to the base of Q1 (point C) forward biasing that transistor. When Q2 conducts, its collector voltage rises to 0.85 volt (point D) from its -6 volt clamp level. The base of Q2 now swings positive at point E, due to the previously changed condition of C3 (plus to minus as indicated on Figure 5(A)). Capacitor C3 immediately begins to discharge toward the voltage level V1 or V2, depending on the prime voltage level at the bias input A. Levels V1 and V2 are established by the voltage divider action of R11 and R3. The rate of discharge of C3 is determined by R11, R3, and R2.

4.32 Time-out: Assuming a -6 volt bias input, C3 begins to discharge toward that level. The time the circuit remains in this semi-stable state is determined by the time required for C3 to discharge to a level which allows Q2 to turn ON. The discharge of C3 follows the expotential decoy shown for point E until a level more negative than about 1 volt is reached at t1. When this point is reached, Q2 turns ON and Q1 turns OFF. Capacitor C3 recharges to its 6 volt potential during the stable state condition. Diode CR2 is reverse biased while C3 charges, preventing any distortion of the Q1 collector wave form. If the bias input voltage level had been 0 volt instead of -6 volts, it would have taken C3 a longer time (t2) to discharge to the level where Q2 turned ON, resulting in a longer time-out for the circuit.

Operation - Variable Bias Prime

4.33 General: The above paragraphs consider the cases when the bias is fixed at either -6 volts (V1) or 0 volt (V2) throughout a complete operating cycle. This, however, is not the normal operating condition of the circuit. Normally, the bias input will switch from 0 volt to -6 volts somewhere between times t1 and t2. This will cause the circuit to operate in its semi-stable state for a period of time (t3) occurring between t1 and t2.

4.34 Operation: The wave forms in Figure 5(C) are those associated with the points mentioned below, and which are circled on Figure 5(A). Note that wave forms A, B, and E, Figure 5(C), represent the same points as A, B, and E, Figure 6. During normal operation, the bias prime switches from 0 volt to -6 volts somewhere between t1 and t2. When the trigger pulse at point A switches Q2 OFF, C3 discharges toward the 0 volt bias prime level, V2. At some time, t, the bias prime level switches to -6 volts, V1, causing C3 to change its discharge rate. The voltage at the base of Q2 now reaches the forward bias level (about 1 volt) at time t3 - before t2, but after t1. Transistor Q2, therefore switches ON at this time. Times t1 and t2, Figure 5(C), indicate the time durations for C3 to discharge to about 1 volt if the bias had been fixed at either -6 volts or 0 volt.

C. Transfer Circuitry Timing

4.35 Figure 6 is a timing diagram of the transfer circuitry during the critical time after a character has been inhibited and remains in storage until the next cycle. Referring to the timing diagram, a shift pulse, (A), transfers the information from the signal register to the storage register. 100 microseconds after the shift occurs, the set "1" delay pulse, (C), sets the transfer prime flip-flop, Z403, to the set "1" condition (normal output, (D), goes positive). The clock pulse, (K), which triggers the variable pulse delay circuit Z406, (F), has come in and the variable pulse delay begins its time out. The inverted output, (E), of the transfer prime flip-flop provides bias for the variable pulse delay circuit. Since the transfer prime is in the set "0" condition, the variable pulse delay circuit times out to its longest pulse width. The normal output of the transfer prime flip-flop primes transfer one-shot Z407, (G), and the positive transition of the variable pulse delay triggers the one-shot. In Figure 6, the first character, A, has been shifted, the variable pulse delay has timed out, and the transfer prime flip-flop is still in the set "0" condition (normal output at -6 volts). Thus, the transfer prime one-shot will not be triggered, a transfer pulse, (H), will not be generated, and character A will not be punched. The character will remain in storage until the next punch cycle. The set "1" delay pulse comes in and the transfer prime flip-flop goes to the set "1" condition.

4.36 When the next clock pulse comes in, the variable pulse delay circuit, Z406, times out to its shortest pulse width and triggers the transfer one-shot, Z407. The positive transition of the transfer one-shot is used to reset the transfer prime flip-flop to the set "0" condition. The negative transition, which occurs 100 microseconds later, generates a transfer pulse which triggers the magnet pulser (J). Character A is punched. The dotted signals in the timing diagram indicate the worst possible condition if the start pulse of the next character, B, appeared earlier in the cycle and the motor speed reduced causing jitter in the clock pulse. As indicated, character A will be punched and character B will remain in storage until the next punch cycle. Figure 7 is a similar timing diagram of the transfer circuitry, but illustrates several cycles of operation.

D. Receiving Distributor

Note: Refer to schematic wiring diagram of receiving distributor 4441WD and receiving terminal timing diagram Figure 8.

Initial Conditions

4.37 Approximately 150 to 300 microseconds after the power switch is operated to the ON position, the -6 volt to 0 volt reset pulse generated in the receiving converter appears at terminal E4 of connector J301, the set "1B" terminal of control register Z310, and the set "0A" terminal of element Z320. The reset pulse places element Z320 in the set "0" condition, and the control register flip-flop in the set "1" condition. The events are as follows:

(a) The start-stop oscillator turns on for one cycle, generating one advance pulse.

(b) The control register is triggered after completion of one cycle of oscillation, and the oscillator is turned off.

(c) The stop inserter one-shot is turned on and starts its time out.

(d) At the completion of the stop inserter time out, the synchronizer flip-flop is triggered to the set "1" condition.

(e) The start OR gate, Z301A, is opened to accept a start pulse.

(f) The start AND gate, Z301, is opened.

(g) The input gate on the start delay is primed.

Signal Input

4.38 The receiving distributor receives a +1 volt to -6 volt start signal from the receiving signal converter on terminal C10 of connector J301. This start signal is applied through the operate switch to terminal C of the signal gate, Z301A. The start signal is also applied to the set "1B" and prime "1A" input of the synchronizer flip-flop. The signal will pass through the gate, Z301A, on terminal A provided the synchronizer flip-flop, Z324 (output on terminal K) is in the set "1" condition.

Register Drive

4.39 From the output of the signal gate, the signal is sent to the input of emitter follower Z302A, terminal D, and from terminal N of Z302A, to the first inverter of the register drive, Z303A, terminal B. The output of Z303A, terminal K, applies the inverted signal to:

(a) The prime "0B" side of the last element in the signal register, terminal H (element Z313, Z314, or Z315, depending on number of code levels).

(b) The input of the next inverter, Z303B, terminal D.

(c) The input of the start delay, Z305, terminal C.

4.40 The second inverter, Z303B, inverts the signal so that it is back to normal. From the output of Z303B, terminal L, the signal is applied to:

(a) The prime "1B" side of the last flip-flop of the signal register (element Z313, Z314, or Z315, depending on number of code levels).

(b) To the input terminal of the signal delay, Z304.

4.41 A start transition consists of a +1 to -6 volt transition lasting for a period of one bit. When this transition passes through the first inverter it becomes a -6 to 0 volt pulse. This pulse is sent to the set "1" input of the start delay one-shot, terminal C, Z305, causing it to begin a time-out for approximately a half a bit. The normal output of this one-shot, terminal L, goes from -6 to 0 volt and is applied to terminal N of Z301B, the start OR gate.

4.42 The second inverter, Z303B, brings the -6 to 0 volt transition from the output of the first inverter, Z303A, terminal K, back to the original 0 to -6 volt transition, and applies it to the input of the signal delay, terminal C, Z304. The output of the signal delay, terminal L, delays the 0 to -6 volt transition by 40 microseconds, to prevent a false start, and sends this delayed transition to terminal M of Z301B.

Start Circuits

4.43 The output of the start OR gate, Z301B, is 0 volt, if 0 volt appears on any of its inputs, and -6 volts, if -6 volts appears on all of its inputs. This is an important fact to remember while trying to understand how the start OR gate performs its function in the circuit. If a true start signal has been sent, then 40 microseconds after the signal is received, terminal M of Z301B goes to -6 volts for a period of one bit. Terminal N of Z301B goes from -6 volts to 0 volt as soon as the start transition is received, and remains at 0 volt until the start delay timer, Z305, relaxes (about one-half bit time duration). The start delay relaxes before terminal M of the OR gate has a chance to return to 0 volt. This results in a 0 to -6 volt transition on terminal N of the OR gate, which will appear on the output, terminal L. If a false start is received (ie, a short 0 to -6 volt transition), terminal M of the OR gate will be at 0 volt when the false start arrives on terminal N of the OR gate, preventing the 0 to -6 volt transition from appearing on the output. See timing diagram, Figure 8.

4.44 The negative transition from terminal L of the start OR gate is passed through the start AND gate, terminal F, Z301C, to the input of the start pulse amplifier, Z302B, terminal B. The start pulse amplifier shapes the negative transition on its input into a positive going -6 to 0 volt pulse on its output, terminal K. This pulse is applied to the set "1A" input of the control register, terminal C, Z310, switching it to the set "1" condition.

4.45 When control register Z310 switches to the set "1" condition, the following events take place:

(a) Start-stop oscillator Z311 starts, due to the 0 volt potential appearing on its input, terminal H, from the normal output of the control register.

(b) Start gate Z301C, closes due to the -6 volt potential on its input, terminal E, from the inverted output of the control register.

Start-Stop Oscillator

4.46 The start-stop oscillator, Z311, receives a -6 volt to 0 volt signal from the control register flip-flop as described in Paragraph 4.45. The oscillator begins to oscillate as soon as a 0 volt signal is applied to its input, terminal H, and the output appears as a sinusoidal oscillation on terminal A. This output is sent to the input of the squaring amplifier, Z312, terminal H. The squaring amplifier shapes the sine wave to produce a positive going -6 to 0 volt advance pulse every cycle. One advance pulse is produced for each period of the sine wave output. The advance pulses are applied to both the set "1B" and set "0B" inputs of the signal register flip-flops, terminals E and F of Z313 through Z320, and to the set "0B" input of the control register, terminal F, Z310.

Signal Register

4.47 The signal input is applied to the prime inputs of the Nth register element - Z313, Z314, Z315, or Z316 depending on the level of operation (8, 7, 6, or 5 respectively) being considered. Although 8-level operation is assumed in the following discussion, theory of the other levels is similar, the signal input priming the correct element of the signal register.

4.48 The input signal advances through the signal register bit by bit. To analyze operation of the register, consider what happens as a start pulse is shifted through the register.

(a) The start pulse, after passing through Z301A and Z302A, appears at the input of the first of the two register drive inverters, Z303A and Z303B. The first inverter output applies a 0 volt prime signal to the "P0B" input of the Nth element in the signal register (terminal H of Z313 for 8-level operation).

(b) This same 0 volt signal is applied to the input of the second inverter, Z303B. Its output, a -6 volts signal, is applied to the "P1B" input of the Nth element, terminal J.

(c) The Nth element is now primed for set "0." When the first advance pulse arrives at terminal F, the Nth element flip-flop switches. Its inverted output, terminal K, applies a prime to the "P0B" input of the next register element, and its normal output, terminal L, applies a prime to the "P1B" input of the same register element (Z314).

(d) When the second advance pulse appears at the set "0B" input of Z314, this register element switches to the set "0" condition. Simultaneously, the next bit passes through the double inverter, Z303A and Z303B, priming the Nth signal register element as described in Sub-Paragraph (a) above.

(e) Thus, the signal is inserted into the signal register bit by bit until the N+1 advance pulse shifts the start pulse into the control register, Z310. The start pulse primes the "P0B" input of Z310, and the advance pulse causes this flip-flop to switch to the "0" state.

4.49 When the control register flip-flop switches to the set "0" condition, seven things happen.

(1) The start-stop oscillator stops and suspends further generation of advance pulses.

(2) The 100-microsecond shift delay one-shot, Z307, begins to time out.

(3) The 200-microsecond set "1" delay one-shot, Z306, begins to time out.

(4) The start AND gate, Z301C, opens.

(5) The start delay one-shot, Z305, is primed.

(6) The start inserter one-shot starts its time out.

(7) The synchronizer flip-flop is triggered.

Shift Delay

4.50 The shift delay one-shot, Z307, becomes active on receiving the -6 to 0 volt transition on its set "1" input, terminal C, from the control register. After a period of 100 microseconds, the circuit relaxes, and sends a negative going pulse from its normal output, terminal L, to the input of pulse amplifier Z308A. Pulse amplifier Z308A provides a positive going -6 to 0 volt pulse on its output, terminal K. This pulse is applied to the input of an emitter follower circuit, terminal B, Z309A, which provides power amplification of the pulse. From the output of the emitter follower, terminal A, the pulse is sent to terminal C1 of connector J301. From there it passes to the signal converter to shift the information in the signal register into the storage register.

Set "1" Delay

4.51 Two hundred microseconds after the positive transition from the control register excites the set "1" delay one-shot, Z306, a negative transition is generated at its normal output, terminal L. This transition is fed to pulse amplifier Z308B, terminal D, and appears as a positive -6 to 0 volt transition on the output, terminal L. The pulse is sent to emitter follower Z309B, terminal D, for power amplification, and from the output of the amplifier, terminal N, to the set "1A" input of all the signal register flip-flops (terminal C of elements Z313 through Z320). The positive transition on the set "1A" input of the flip-flops causes them to reset to the set "1" state, since all the elements are primed with +1.5 volts on terminal M, the "P1A" input.

4.52 Thus, 100 microseconds after the control register goes into the set "0" condition, the shift delay transmits a pulse to the signal converter to shift the information in the signal register into the storage register. And, 200 microseconds after the control register goes into the set "0" condition, the set "1" delay transmits a pulse to reset the signal registers to the set "1" condition. In addition to reset, the set "1" delay performs another function. The output of emitter follower Z309B is also applied to terminal B1 of connector J301. From there the output of Z309B (-6 to 0 volt transition) is sent to the transfer prime, Z403, in the signal converter. This informs the signal converter that the signal is in the storage register and is ready to be punched.

4.53 The -6 to 0 volt transition from the inverted output of the control register is applied to terminal E of the start AND gate, Z301C, keeping the gate open. The purpose of this gate, which closes while the control register is in the set "1" state, is to prevent signals from being applied to the control register while the start-stop oscillator is in operation. The same positive transition, when applied to the prime "1" input of the start delay one-shot, primes the start delay gate so that it can be triggered to generate a start pulse when the start-stop oscillator is not oscillating.

Synchronizing Flip-Flop

4.54 The positive transition from the control register is also applied to the set "1" input of stop inserter Z321, terminal C. This element triggers, producing a -6 to 0 volt transition on its normal output, terminal L. This signal is applied to the set "0A" input of the synchronizer flip-flop, triggering this circuit to the set "0" condition. Refer to Paragraph 5.29 through 5.34 for a detailed description of the resynchronizer circuit.

Test Conditions

4.55 With the TEST-OPERATE switch in the TEST position, a -12 volt bias is applied to terminal C of input gate Z301A. This simulates an open line condition.

4.56 In the TEST position, the circuit path from the resynchronizer circuit to terminal D input of the signal gate is opened, and an alternate path is provided from the stop inserter. This condition results in local regeneration of blank characters, the stop inserter applying the stop pulse. Local electronic testing can, therefore, be performed. Note that the resynchronizer circuit will not be triggered; it will remain in the set "0" condition.

4.57 A jack, J302, has been provided to facilitate local testing and to permit receiving margins to be taken using a 905A or 905B data test set. The test signal applied shall be -6 volts for SPACE and 0 volt for MARK working into a 1200 ohm load. With a test signal applied, the resynchronizer circuit will be triggered randomly.

E. Auxiliary Connections

4.58 Receiving distributor:

(a) Set "1" delay, terminal E2, connector J101 informs the auxiliary equipment that the character in the signal register has been transferred to the storage register.

(b) Start-stop control lead, terminal E3, connector J301 is used to permit the auxiliary equipment to turn the start-stop oscillator on and off.

4.59 Signal converter:

(a) Signal blind, terminal E9, connector J401, is used to permit the auxiliary equipment to prevent the Receiver from receiving the incoming signal.

(b) Clock, terminal F1, connector J401, is used to monitor the shaped magnetic pickup and to provide timing in the auxiliary equipment.

(c) Transfer inhibit, terminal E7, connector J401, is used to inhibit the punch magnets.

(d) Transfer, terminal E6, connector J401, is used to monitor the transfer pulse for use in the auxiliary equipment.

(e) Terminals E2 and E3, connector J401, are used in conjunction with auxiliary equipment for vertical parity checks.

5. OPTIONAL FEATURES

TAPE SENDER

A. Signal Converter (Sending) With Rubout Delete

General

5.01 The signal converter with rubout delete feature is basically identical to the signal converter described in Paragraphs 3.02, 3.06 through 3.09 and 3.14 through 3.20. The important difference between these units is the rubout delete feature - a feature which prevents the transmission of an all MARK signal from the Tape Sender to the Tape Receiver.

5.02 In certain data systems the operator, while preparing a message tape, may insert errors into the tape. To "erase" these mistakes, the errored characters are deleted by punching all levels (rubout) of the entire group of characters involved. The correct message is then repunched into the tape in a new location.

5.03 When the tape is transmitted, the receiving station would normally receive all information sensed by the tape reader at the sending station, including the all MARK or rubout characters. If, however, a sending signal converter with rubout delete is utilized at the sending station, the all MARK (rubout) signals will be suppressed. Consequently, only the valid data information will be reproduced by the Tape Receiver.

Detailed Circuit Description

Note: Refer to Schematic Wiring Diagram 5917WD.

5.04 General: Since the circuit analysis of this signal converter is similar to that already covered elsewhere in this section (see Paragraph 5.01), reference will be made to the applicable paragraphs whenever possible.

5.05 The rubout delete function of this signal converter is controlled by five logic elements: Z215A, Z215B, Z216A, Z216B, and Z217A. These elements function to control operation of the start-stop oscillator in the sending distributor.

5.06 Initial conditions: Refer to Paragraphs 3.14 and 3.15.

5.07 Reader input: Refer to Paragraph 3.16.

5.08 Rubout delete: The universal contact signal from the reader is applied to integrator Z202D via terminal H9 of J201. The output of Z202D, terminal P, is applied to OR gate Z215B, terminal P. This signal is gated with the inverted output of Z215A, and is applied to terminal R of emitter follower Z216B. The output of Z216B is connected to terminal C4 of J201, and is applied to the start inhibit gate in the receiving distributor. When the output from Z216B is 0 volt, the start-stop oscillator in the distributor is prevented from starting (refer to Paragraph 3.24).

(a) SPACE and MARK input: If any one of the levels sensed by the reader is SPACE, the corresponding integrator output is about 0 volt. A MARK signal, on the other hand, produces a -10 volt signal. When the MARK and SPACE signals are gated together in OR gate Z215A, its output, terminal B, will assume the most positive potential (0 volt). This 0 volt signal is amplified through emitter follower Z216A, and applied to pin B of inverter Z217A. The inverter output, terminal K, goes to -6 volts and is gated with the universal input in Z215B, causing the output of Z215B to go to -6 volts. This -6 volt level is amplified by Z216B and applied, via terminal C4 of J201, to the start inhibit gate in the distributor. A -6 volt input to the start inhibit gate allows the start-stop oscillator to start, and the character sensed by the reader to be transmitted to the receiving station.

(b) All MARK input: If all levels are MARK, however, the output of Z215A will go to -6 volts, and the inverter, Z217A, will present a 0 volt signal to OR gate Z215B. The output of Z215B remains at 0 volt even though the universal contact closes. Consequently, the start-stop oscillator in the distributor will be inhibited, and the all MARK character will not be transmitted to the receiving station.

5.09 Polar signal output: Refer to Paragraph 3.18.

5.10 Request to send: Refer to Paragraph 3.19.

5.11 Power requirements: Refer to Paragraph 3.20.

B. Line Break and Automatic Answer Kit

General

5.12 The line break and automatic answer feature allows a tape sender terminal to automatically transmit its message tape in answer to a call placed by a tape receiver terminal. Operation of both terminals is controlled by the operator at the Receiver location. This feature is available in kit form (TP146527) for field or factory installation.

5.13 Proper operation of the line break and automatic feature depends upon use of a data set with the following features:

(a) Unattended answering.

(b) Reverse channel carrier.

These data set features are now available with the advent of the 202C2 and 202D2 data sets and the automatic answer feature added to existing Tape Senders may be used.

- Another modification kit - interim unattended answer - is available which allows Tape Senders equipped with the line break and automatic answer feature to make use of that feature until the necessary data set features are available (see Paragraph 5.19).

- The following discussion assumes availability of reverse channel carrier and unattended answering.

Detailed Circuit Description

Note: Refer to Schematic Wiring Diagrams 3843WD, 4772WD and 5941WD.

5.14 Manual operation with line break: The Tape Sender is prepared to operate in the manual mode when the following conditions exist:

- Tape reader loaded with a message tape; tape-out contact closed.

- Tape reader and tape winder motor switches OFF.

- Data set in TALK condition; telephone receiver on hook.

- Interlock and line break outputs at 0 volt and -8 volts respectively.

- TEST-OPERATE switch, S101A and S101B, in OPERATE position.

- Automatic-manual switch in MANUAL position.

- Normally open tape-out contact closed.

- Tape reader RUN-STOP switch in STOP position (open).

(a) A call may be placed by the operator at either the Receiver or Sender location. When verbal agreement is reached to start transmission, the operator at the Sender location starts the tape reader and winder motors by placing their respective switches in the ON position. Next, he depresses the DATA button. The data set goes into the DATA mode, placing the Sender on the line and switching the voltage level on the interlock output (terminal 6 of J601) from 0 volt to +8 volts. Since the automatic - manual switch is in the MANUAL position (breaking the circuit between relay driver Z601B and the motor start relay), the motor start relay will not energize on this +8 volt input.

(b) When the operator at the Receiver location places his data set in the DATA mode, a line break signal (400 cycles per second tone) is transmitted continuously. In the data set at the Sender location, a detector recognizes this signal and causes the line break output to switch from -8 volts to +8 volts. The +8 volt signal is applied through S101A to terminal F of relay driver Z601A. The relay output, terminal J, switches from -28 volts to 0 volt, energizing the line break relay via the tape-out contacts. When the line break relay energizes, normally closed contact C4 opens and normally open contact C5 closes.

(c) The Tape Sender operator (after a few seconds wait to allow the Tape Receiver operator time to place his data set in the DATA mode) operates the RUN-STOP switch on the reader to the RUN position. This completes the energizing circuit to the reader clutch coil; from ground, through the run-stop contacts, through the normally closed B9 contact and the normally open C5 contact, to one side of the clutch magnet. The tape reader starts sensing tape. Note that the tape reader will not start sensing tape unless contact C5 is closed. Contact C5 is controlled via the data set at the Receiver location; if the Tape Receiver is not in DATA mode, or the line is disconnected, contact C5 is opened. If this is the case, and if the RUN-STOP switch is in the RUN position, then the alarm relay will energize actuating the audible and visual alarms to indicate a line break condition. The reader will start, pending Receiver action.

(d) When an end-of-message (EOM) condition occurs (in this case, end-of-tape), the tape-out contacts open. The line break relay de-energizes, and contacts C4 and C5 return to their normal conditions. Contact C5 opens the energizing path to the reader clutch coil, stopping the reader, and contact C4 completes the energizing path to the alarm relay; from ground, through the RUN-STOP switch, through the normally closed B9, B10 and C4 contacts, then through the alarm relay to -28 volts. Both the audible and visual alarm indicators are energized, and the auxiliary alarm circuit is conditioned to operate.

(e) The alarms are disabled when the operator at the Sender location moves the RUN-STOP switch to the STOP position. The reader and winder motors can now be de-energized. If verbal confirmation to disconnect is required, the Sender operator may contact the Receiver operator via his telephone handset after depressing the TALK button. If no verbal confirmation is necessary, the disconnect can be made in the normal manner.

5.15 Operation of line break: If for some reason (trouble at the Tape Receiver location, for example) the Receiver operator wants to stop transmission and contact the Sender operator, all he need do is remove his telephone handset from hook and depress the TALK button. This interrupts the line break signal tone, causing the line break output from the Sender data set to switch to -8 volts. The output of relay driver Z601A, terminal J, switches to -28 volts, and the line break relay de-energizes operating contacts C4 and C5 as outlined in Paragraph 5.14 (d). The alarms are disabled when the RUN-STOP switch is operated to the STOP position. The Sender operator may talk to the Receiver operator by lifting his telephone handset off hook and depressing the TALK button. Transmission may be restarted at the discretion of the Sender operator.

5.16 Automatic answer and line break: The Tape Sender is prepared to operate in the automatic mode when the following conditions exist.

- Automatic-manual switch in AUTO position.
- Tape reader and tape winder motors OFF.
- Tape reader loaded with a message tape; tape-out contact closed.
- Data set in AUTO position; telephone receiver on hook.

(a) If the above conditions are met, the automatic answer relay will be energized via the tape-out contact and the automatic-manual switch. When energized, the automatic answer relay closes normally open contact B11, shorting the remote control common and ready leads to the data set. This primes the Tape Sender data set to automatically answer an incoming call.

(b) A call is originated by the operator at a Tape Receiver location. The Tape Sender data set will answer this call (1200 cycles per second tone) and, after several seconds, go into the DATA mode. When it does, its interlock output switches from 0 volt to +8 volts. This +8 volt signal causes the output of relay driver Z601B to switch from -28 volts to 0 volt, energizing the motor start relay via the automatic-manual switch. Normally open contacts K1 and K3 close, energizing the tape reader and winder motors.

(c) Upon hearing the answer tone from the Sender data set, the Receiver operator places his data set in the DATA mode. A line break signal (400 cycles per second tone), transmitted from the Receiver terminal data set to the Sender terminal data set, causes the line break output at the Sender location to switch from -8 to +8 volts. A +8 volt input to relay driver Z601A switches its output to 0 volt, energizing the line break relay which operates contacts C4 and C5. The energizing path for the reader clutch coil is from ground, through normally open contacts B9 and C5, the reader clutch coil, and the 25 ohm resistor to -28 volts. The Tape Receiver operator can control transmission, therefore, depending upon the operating mode of the Receiver data set.

5.17 End-of-message: When the message tape is exhausted, the tape-out contact opens de-energizing the automatic answer and line break relays. These relays return their associated contacts to their normal conditions, causing disconnect of the automatic answer prime to the Sender data set (contact B11) and stopping the tape reader (contacts B9 and C5). The interlock output at the sender terminal switches from +8 volts to 0 volt, causing the output of relay driver Z601B to switch from 0 volt to -28 volts. The motor start relay de-energizes, disconnecting the tape reader and winder motors. The Receiver operator can now take action to disconnect his terminal. Future calls placed to the sender terminal will not activate the sender terminal. Since the automatic answer relay is de-energized, contact B11 is open and the initial automatic answer conditions are not satisfied (Paragraph 5.16). To complete the automatic answer conditions, a message tape must be loaded into the tape reader.

5.18 TEST-OPERATE switch: The TEST-OPERATE switch must be in the OPERATE position for normal operation in both the manual and automatic modes. When in TEST position, this switch places a +6 volt bias on the Z601A and Z601B relay driver inputs. This simulates the DATA mode of the data set, permitting local testing and trouble shooting.

- When installed in Tape Senders before reverse channel carrier and unattended answering are available - and if the interim unattended answer modification kit (Paragraph 5.19) has not been installed - the TEST-OPERATE switch must be in the TEST position.

C. Interim Unattended Answer Kit (Early Design)

General

5.19 The interim unattended answer feature, when used in conjunction with the line break and automatic answer kit (Paragraph 5.12), provides facilities for automatically starting an unattended Tape Sender from a remote Receiver location. It is specifically designed to be used with the line break and automatic answer kit until the data set reverse channel carrier and unattended answer features are available (Paragraph 5.13). The interim unattended answer kit (TP148161) is now used on a private line installation only. Recognizer kit TP199551 with generator kit TP199550 supersedes TP148161 and also provides additional features for the system.

Detailed Circuit Description

Note: Refer to Schematic Wiring Diagrams 3843WD, 4772WD, and 5941WD, the TP177543 etched circuit board drawing and Figure 9.

5.20 Unattended automatic answer: The following conditions should exist at the Tape Sender for unattended automatic answer:

- Power on.
- TEST-OPERATE switch in TEST position.
- Tape reader loaded with a message tape.
- Tape reader RUN-STOP switch in RUN position.
- Automatic-manual switch in AUTO position.
- Data set in AUTO mode; telephone receiver on hook.

(a) A call is originated by the operator at the Receiver location in the normal manner. If the above initial conditions are satisfied, the automatic answer relay will be energized: from ground, through the relay, the 250 ohm resistor, the automatic-manual switch, and the tape-out contacts (closed when reader is loaded with tape) to -28 volts. Normally open contacts B8, B9 and B11 will be closed, conditioning the circuit for automatic answer. The Sender terminal data set automatically answers the incoming call (contact B11 closed), transmitting a 1200 cycles-per-second tone. Within 4 seconds after hearing this tone, the Receiver operator must depress the DATA button on his data set, placing the receiver terminal on line.

(b) The Sender data set, after a period of several seconds, automatically goes into the DATA mode, and its interlock output switches from 0 volt to +8 volts. This +8 volts is applied through the TEST-OPERATE switch, to the input, terminal M, of the motor start relay driver (Q4 and Q5). The relay driver turns on, and the motor start relay energizes to activate the tape reader and winder motors.

(c) The output of the relay driver (0 volt) is applied to the emitter of Q1, a unijunction transistor, which is part of a time delay circuit. Between about 4.5 seconds and 8.5 seconds after the trigger from the relay driver is applied (time-out determined by the size of C1 and R1), a positive pulse is coupled from the base of Q1 to the gate of Q2, a silicon controlled rectifier (SCR). The SCR turns on (contact B8 closed), turning on amplifier Q3. The output of Q3, terminal J, switches to 0 volt, energizing the line break relay (C) via the tape-out contact. When the line break relay energizes, normally open contact C5 closes and completes the energizing path for the tape reader clutch coil: from ground, through normally open contacts B9 and C5, the clutch coil, and the 25 ohm resistor to ground. The reader starts to sense tape.

(d) When the tape is exhausted, the tape-out contact opens causing the automatic answer relay (B) and the line break relay (C) to de-energize. Normally open contacts B8, B9, B11 and C5 are returned to their normal state. Contact B8 causes the SCR to turn off, which in turn switches amplifier Q3 off. Contact B11 disconnects the data set, and contacts B9 and C5 operate to disconnect the tape reader clutch circuit. The tape reader stops sensing tape.

(e) When the tape reader stops transmitting, the Receiver operator should disconnect his terminal. The Sender terminal data set will automatically disconnect, and its interlock output will switch from +8 volts to 0 volt. This causes the motor start relay driver to turn off, motor start relay to de-energize and the tape reader and winder motors to turn off. The sender terminal will not automatically answer any future incoming calls until the tape reader is reloaded with a message tape.

5.21 Manual operation: The Tape Sender may be operated manually in the normal manner (see the appropriate section) by not depressing the data set AUTO button, and leaving the automatic-manual switch in the AUTO position. When the Sender operator depresses the DATA button, the tape reader will start after a 4.5 second to 8.5 second delay.

5.22 The unattended automatic answer feature can be disabled by operating the TEST-OPERATE switch to the TEST position. This switch bypasses the relay driver and time delay circuitry on the TP177543 (EC543) circuit board, and operates the line break relay. This switch also provides a means for local testing and trouble shooting of the sender terminal.

5.23 When reverse channel carrier is available, the sender terminal may be enabled to operate with this data set feature by substituting circuit board TP177543 (EC543) with circuit board TP146520 (EC520). Operation will then be as described in Paragraphs 5.12 through 5.18. These paragraphs cover operation of the line break and automatic answer feature.

D. Discrete Calling—Recognizer Kit

General

5.24 This feature is the recommended method of providing unattended service at a send station operating on the switched network, and it replaces the arrangement described in 5.19. The disconnect function is part of the discrete calling modification kit for send stations. Use terminal kit TP199610 with recognizer kit to couple send-receive set to data set.

Theory of Operation (Figures 11, 12 and 13)

Circuit Description - Refer to Schematic Wiring Diagrams 7027WD, 7029WD, 172497, 303650 and the actual wiring diagrams.

5.25 A protected unattended transmitter Tape Sender set of parts provides security against an unauthorized call triggering the Sender into action when the unit is placed in its unattended mode of operation. The companion set of parts is required at the remote Receiver to provide the identification signals which must be recognized by the Sender before a bonifide request to send is allowed to initiate the transmission. A Tape Sender is placed in the unattended mode of operation when the controls have been positioned as follows:

(1) Automatic-manual switch; AUTO/MANUAL set in its AUTO position.

(2) Tape reader RUN-STOP switch set in its RUN position.

(3) TAPE-OUT switch; tape (perforated with message to be transmitted) present and threaded into its normal tape path.

Note: When any of the above conditions are not met, the Sender is in the MANUAL mode of operation.

5.26 The logic which establishes the unattended mode of operation consists of relay K-835L. This relay is operated directly from relay "B" of the line break and automatic answer assembly (TP146527) through contacts 11 and 11M. Contact 11 of relay B is grounded by way of the cable assembly (TP199556).

5.27 In the unattended mode of operation, relay K-835L remains in its operated position until a tape-out condition appears. With the manual mode of operation selected, the recognizer logic is not activated.

5.28 The recognizer logic consists of a signal generator assembly Z828, etched circuit board assemblies EC650/Z829 and EC497/Z830 and four relays; K-814, K-817L, K-817U and K-835U. The signal generator is an electromechanical device consisting of a coded disc driven by a 20 RPM synchronous motor. The mechanism provides the sequential control signals to initiate the recognition and code comparison cycle. The Z828 coded disc must be identical with the coded disc at the remote receiver terminal to assure identical start signal and coded pulses. The locally generated start signal is compared bit by bit with the start signal of the remote terminal and when the incoming signal is in full agreement with the local signal, the transmitter is permitted to start. In this manner the Sender is protected against the receipt of an unauthorized call (wrong number) triggering the transmitter when it is in the unattended mode of operation. One rotation of the disc through its control segments and 14 coded elements provides the continuity that is checked with the incoming start signal.

5.29 The relay drivers located on the etched circuit boards may be conditioned to turn on and energize the relay when its return (ground) is completed through the sampling segment on the revolving disc. The four relays K-814, K-817L, K-817U and K-835U provide the switching and signal comparison functions. Relay K-814 is a double coil mechanical latching relay with a separate winding to release the latched up armature. When a nonvalid transmitter start signal is detected, the relay K-814 is latched up and remains latched until the disc nears the end of its rotation. Relay K-817L operates the motor clutch or brake release on the signal generator drive motor.

5.30 The break feature is controlled by an ON/OFF switch (S801) attached to a +6 volt power source. When this feature is not in use, a +6 volt potential is directed through the break lead terminal and automatic answer assembly (TP146527) to the reader clutch resulting in continuous clutch operation. When the break feature is used, the reader clutch will be operated by the reverse channel feature of the data set. A +6 volt potential (reverse channel mode) directed to the reverse channel receive terminal will operate the reader. Conversely, a -6 volt potential (absence of reverse channel signal) will stop the reader.

5.31 Two separate output connections are provided for the data set control circuit to allow unattended send-receive operation of units equipped with send-receiver terminal modification kit (TP199610). These connections are identified as follows: (a) request to send (A/M), this output provides a +6 volt potential for a send-only station; (b) request to send (A), this output provides a +6 volt potential for a data set at an unattended send-receive station.

5.32 The disconnect logic circuit consists of an etched circuit board EC497/Z830 and the thermal sensitive time delay switch K-813. The circuit board contains an emitter-follower amplifier Z830A and a relay driver Z830B having a two-input gate. When a positive potential of approximately 8 volts appears at the interlock terminal C2/J801, a standard voltage of +6 volts is obtained at the output of Z830A. This output is directed to terminal D of Z830B. The other input to the gate (terminal N) is connected to C4/J801, the carrier detect lead from the data set. A -8 volt potential at the latter terminal coincident with the positive input at C2/J801 causes the relay driver, Z830B, to conduct. When the relay driver, Z830B, is turned on, the thermal sensitive switch K-813 will open its normally closed contacts after approximately a 30 second delay. In this manner, the data set release leads are open circuited after a 30 second interval. This will place the data set at the unattended station in the "on hook" mode of operation. The break contacts return to their normally closed condition about ten seconds after a call has been dropped.

5.33 Manual Operation - (a) relays K-814, K-817L, K-817U, K-835L and K-835U remain in their unoperated position; (b) with relay K-835L unoperated, the data set ready lead is open circuited so as to inhibit the data set from automatically answering a manual call; (c) the terminal marked request to send (A/M) is at a +6 volt level and the terminal marked request to send (A) is at a -6 volt level.

5.34 Unattended Operation - Refer to timing diagram for the recognizer logic shown in Figure 13.

(a) Relay B of the line break automatic answer kit (TP146527) operates when the conditions of unattended mode of operation are established (Par. 5.25). Then the make contacts of relay K-835L close to provide continuity to the data set ready lead for automatic answering (A8/J801).

(b) Emitter-follower amplifier EC497/Z830A will accept a +8 volt interlock signal from the data set connection at terminal C2/J801. The output is directed to relay driver EC497/Z830B as mentioned in Paragraph 5.32 and to relay driver EC650/Z829H. Thus, the K-817U relay is locked up until the interlock pulse is dropped so as to initiate the following functions:

(1) The normal +6 volt potential is removed from terminal C1/J801 - request to send (A/M) connection to the data set.

(2) Contacts 12M and 12 are closed to energize the clock motor and release its clutch/brake mechanism. One rotation of the motor drive shaft moves the disc through its cycle of operation in three seconds. This signal generator, Z828, provides the control pulses and 14 code bit recognization sequence for comparison with the received signal.

(3) Connects the data set received data input lead A2/J801 to the recognizer logic - etched circuit board EC650/Z829. The function of the normally open contacts is to prevent the signal generator from starting when a transmitter signal is being transmitted by a receiver of a send-receive terminal.

5.35 Recognizer Logic; EC497 & 650: Inverter, Z829A, accepts a ±8 volt input signal from the received data terminal A2/J801 of the recognizer module - see 7027WD in the appropriate section. The output of the inverter is a -12 volt potential for a spacing signal (spacing is positive on data set) and a zero voltage output for a marking input. At the beginning of a transmitter start signal, the input to the oscillator (Z829B) is a -12 volt potential which turns the oscillator on in order to initiate a time-out sequence of approximately 45 milliseconds. A zero voltage input to the oscillator control (Q5) causes the oscillator (Q4) to recycle and shut off oscillation. The output at base number one of the unijunction transistor triggers the (primed) flip-flop Z829-C to its set "one" state. The normal output (Q7, 0 volt) of the flip-flop is gated with an output from the inverter Z829A. When the incoming signal goes marking and the flip-flop output is zero voltage, the output of AND gate Z829D is zero voltage. Inverter Z829E provides a -12 volts or zero voltage (inverse of its input) to one input of the AND gate Z829F. The other input is a -28 or +6 volt level. When both inputs are positive the input to relay driver Z829G is positive. A negative output voltage turns the relay driver on. With relay K-817L operated, the clutch (break) coil of the Z828 clock motor (signal generator) is energized to initiate one revolution of the coded disc. Parallel brushes sense the continuity of the multipath circuit that are momentarily bridged by the various segments of the revolving disc. The 3000 millisecond interval for one rotation of the disc provides the timing sequence for the respective elements - see Figure 11. This initial control signal, recognizer homing, is generated to lock up relay K-817L for one recognition cycle. After approximately 2915 MS, the recognizer homing pulse is cut off and relay K-817L drops out.

5.36 On relay K-814, coil number one (local signal) and coil number two (received signal) are opposed windings (bucking) which compare each of the coding bits of both transmitter start signals. A sampling pulse is impressed upon the common terminal of the relay at the midpoint of each bit - see Figure 13. When either or both of the relay drivers are conditioned to fire by the local and/or the received signal, the respective coil is momently bridged by the various segments of the revolving disc. Thus, an unauthorized call will cause the relay to pick up and latch since the received transmitter start signal will not compare identically (element by element) with the locally generated transmitter start signal. As long as both coils are either marking or spacing which is the condition when identical signals are present, then the relay does not operate and latch up.

5.37 Also signal generator Z828 provides a control signal (GO) after the transmitter start signal has been received. The control signal operates relay K-835U if the recognizer K-814 did not operate and latch up on the received signal. The K-835U relay locks up until a tape-out condition occurs.

5.38 The closure of the make contacts on relay K-835U provide both the request to send (A/M) lead connection and the request to send (A) lead connection to the data set with a +6 volt potential for a duration of 250 milliseconds. This signal (GO) will cause the data set to generate a mark hold signal. The purpose of the 250 MS mark hold signal is to turn the echo suppressors (associated with telephone lines) around.

5.39 Signal generator Z828 will release the control signal (GO) and the recognizer homing control signal as the coded disc completes its cycle. Relay K-817L drops out causing one of two things to happen: (a) the release of the latched recognizer relay K-814 on a nonvalid transmitter start signal or (b) the engagement of the reader clutch on a valid transmitter start signal.

Note 1: It is necessary that the disc at the remote Receiver have the same coding as the disc at the Sender, since the discs are compared (element by element) at approximately the same time. Exercise care in handling the disc so that the surface of the segments is not damaged. Deep scratches will tend to deflect the brushes from their intended path of travel.

Note 2: The 199556 cable assembly connects the protected unattended transmitter recognizer module (TP199555) to the data set, the line break and automatic answer assembly (TP146527) and the ac power. The cable assembly also contains a 2.7K resistor which connects the +17.5 volt lead and the reverse channel lead of the data set together. This arrangement generates a continuous reverse channel tone when a reverse channel type data set is used.

TAPE RECEIVER

A. Automatic Answer Kit

General

5.40 The automatic answer feature allows a tape receiver terminal to automatically answer to a call placed by a tape sender terminal. Operation of both terminals is controlled by the operator at the Sender location. This feature available in kit form (TP146528) for field or factory installation is superseded by modification kit TP199593 - see 5. 45.

Detailed Circuit Description

Note: Refer to Schematic Wiring Diagrams 3845WD and 4773WD.

5.41 Automatic answer, or unattended operation, of the Tape Receiver requires that the following conditions exist at the Receiver locations:

- Data set in AUTO condition; telephone receiver on hook.
- Data set properly wired (see the appropriate section).
- Sufficient tape supply.

5.42 A call is originated by the operator at the Sender location in the normal manner. The Receiver data set automatically answers the call, and goes into the DATA mode.

(terminals 19, 20 and 21 of J501 strapped together). When in DATA mode, the data set transmits a brief 1200 cycles-per-second tone to the Sender terminal data set. Simultaneously, the interlock output switches from 0 volt to +8 volts. This +8 volt level is applied to the input of the motor control relay driver, Z501A, terminal F, causing its output, terminal J, to go to 0 volt. The motor control relay (B) energizes, closing the tape punch and tape winder motor contacts (B3 and B1), turning the punch and winder motors on. The Receiver input amplifier, Z501B, acts to blind the receiver signal amplifier, Z401, in the receiving signal converter (refer to schematic wiring diagram 3833WD, terminal E9 of J401). The output of Z501B is determined by the condition of the carrier on-off signal from the data set. When in the OFF condition (ie, no transmission in process) -8 volts is applied to the input, terminal N, of Z501B. Its output, about +1.5 volts, holds the output of Z401 (EC355) at a positive potential simulating a MARK (or stop) condition.

5.43 Upon hearing the answer-back tone from the Receiver data set, the Sender operator places his data set in the DATA mode. The Receiver data set carrier detector recognizes the 1200 cycles-per-second tone now being transmitted by the Sender data set, and switches the carrier signal from OFF to ON (+8 volts). This +8 volt input to Z501B causes its output to go to -6 volts, unblinding the receiver signal amplifier, Z401, in the receiving signal converter. The receiver terminal is now prepared to accept data.

5.44 At the end-of-message, the Sender operator disconnects his data set by lifting the telephone receiver off hook, depressing the data set TALK button, and replacing the receiver on hook. The Receiver data set disconnects automatically, returning the interlock output to 0 volt – to turn off the winder and punch motors – and returning the carrier on-off signal to OFF – to blind the Receiver signal input. The Receiver is now prepared to accept the next incoming call.

B. Automatic Answer and Disconnect

General

5.45 The automatic answer modification kit (TP199593) causes an unattended Receiver to automatically answer and terminate incoming calls. Termination of a call is sensed by monitoring the data set data carrier detector lead. After a 30 second interval in which the data carrier detector is OFF, the call is automatically terminated. Since the disconnect feature senses the data carrier detector lead output, reliable operation of the disconnect cannot be assured with the 202A and 202B data sets in all locations. Therefore, 202C or 202D data sets should be used when a disconnect problem is encountered.

Theory of Operation

Theory of Operation; refer to Schematic Wiring Diagram 7279WD.

5.46 The automatic answer logic consists of an etched circuit board EC521/Z501, EC497/Z502 the relay K-501. The circuit board combination contains the electronic logic to function with the type 202 data set. The normally opened contacts of relay K-501 are actuated by this logic to energize the tape punch motor and the tape winder motor.

5.47 The automatic disconnect feature consists of etched circuit board EC497/Z502B and the thermal actuated contacts K-502 to provide 30 seconds of ON time before the release lead connection is opened. Also, amplifier EC521/Z501B is connected to the same input to provide a standard output for blinding the receiving distributor when there is no carrier detect signal.

5.48 Automatic Answer Logic: When a +8 volt potential appears on the interlock terminal lead of the data set (6/501), emitter-follower EC497/Z501A consisting of Q1 and Q2 (see EC521). This circuit operates with inputs of +8 volts and zero voltage levels. Transistor Q1 is cut off with the +8 volt input potential and the resulting -6 volt output turns on Q2 to energize the K-501 relay. With the normally opened contacts of K-501 closed, the 117 volt input leads to the tape punch motor and the tape handling motor are energized. However, the punch is not enabled until the carrier signal is detected.

5.49 Blinding Logic: The input amplifier EC521/Z501B senses the potential at terminal 8/P501, the carrier detect lead to the data set. This input is either at a +8 volt level or a -8 volt level. When the +8 volt signal is present (carrier), Z501B is biased to cutoff and its output becomes a standard value of -6 volts. With -8 volts at input (N) the transistor conducts and its output shifts to a standard zero voltage level. Thus, the 0 volt potential used to blind the receiving distributor (data set not detecting carrier on the line) is removed to enable the punch when the carrier is detected.

5.50 The automatic disconnect logic consists of circuit board EC497/Z502B (relay driver) and a thermal sensitive switch K502. The relay driver has two gated inputs. Input N is attached to terminal 8/P501, carrier detect lead to the data set and input D is attached to terminal 12/P501, interlock lead connection to the data set. The relay driver will conduct only when the input at D (interlock) is approximately +8 volts and input N (carrier detect not present) is approximately -6 volts. Under this condition, inhibit gate Q1 output will be approximately +6 volts (normally -12 volts) and the inverter Q2 is turned off to allow Q3 to conduct. With Q3 conducting relay K-502 is energized. After approximately 30 seconds the break contacts (K-502) will open circuit the data set release leads. This procedure places a manually operated or unattended data set "on hook". The break contacts close 10 seconds after a call has been dropped.

C. Resynchronizer Modification Kit

General

5.51 The purpose of the resynchronizer circuit feature is to guarantee resynchronization of a Tape Receiver with the incoming signal, when a synchronization error has occurred due to a noise burst on the line. The circuit will achieve positive resynchronization under all random code structures or transmission conditions.

5.52 This feature is available in kit form (TP148153) for field or factory installation.

Detailed Circuit Description

Note: Refer to Schematic Wiring Diagram 4441WD.

5.53 Normal operation: Operation, as described below, assumes the following conditions:

- TEST-OPERATE switch in OPERATE position.
- Unit receiving traffic.

(a) The stop inserter, Z321, is a one-shot circuit which, when triggered, will turn on and remain on for a preadjusted time interval (for example, the time out for 5-level units is adjusted to 2.9 ±0.1 milliseconds; for universal 5- to 8-level units, however, the stop inserter time out is 0.95 ±0.1 milliseconds). In the following description, a 5-level unit is considered.

(b) The function of the stop inserter is to locally regenerate a stop pulse, at the end of each received character cycle, to prevent the premature start of the receiving distributor due to line noise. When a pulse is received, the start delay one-shot Z305, is triggered and times out for one-half a bit (475 microseconds at 1050 baud). The output, terminal L, of Z305 triggers OR gate Z301B which, in turn, triggers the Z301C AND gate to produce a 0 volt to -6 volt transition. This negative going pulse triggers the start pulse amplifier, Z302B, generating a -6 to 0 volt pulse. This pulse is applied to the set "1A" input of the control register flip-flop, Z310, placing it in the set "1" condition. The normal output (L) of Z310 goes to 0 volt turning on the start-stop oscillator which generates advance pulses. The pulse, followed by information bits, is shifted down the signal register until it reaches the last element, Z320. This element (0 level) primes the control register input (P0B) so that the next advance pulse generated by the oscillator will place the control register in the "0" condition.

(c) The oscillator will turn off and simultaneously, the stop inserter, Z321, will be triggered. The normal output (L) of the stop inserter goes from -6 to 0 volt. This signal is applied to the set "0A" input of the synchronizing flip-flop, Z324.

(d) The inverted output signal (K) of the synchronizing flip-flop goes from -6 to 0 volt. This positive pulse passes through the TEST-OPERATE switch to terminal D of signal gate Z301A. The output of Z301A goes to 0 volt and remains at this level (or slightly more positive) until the incoming transition of the next character, or until the synchronizing flip-flop goes to the set "1" condition. The latter action takes place when the stop inserter completes its time out and the inverted out (K) switches from -6 volts to 0 volt. This signal, when applied to the set "1A" input of the synchronizing flip-flop, triggers it to set "1" only if the prime 1A input is at 0 volt, or if a MARK signal appears at terminal C10 of J301. The synchronizing flip-flop action follows the stop inserter whenever the received unit is in synchronization with the incoming signal.

5.54 Resynchronization: In the timing diagram (Figure 10), character 1 contains an errored start pulse. The next MARK to SPACE transition occurs on receipt of the third bit. The Receiver accepts this SPACE signal (ie, bit 3) as a start pulse, resulting in a "late start" or "out of sync" condition. At the end of the character cycle, the stop inserter begins its time out during the middle of the start pulse of character 2. The resynchronizer flip-flop is also triggered at this time. However, it is not reset when the stop inserter finishes timing out because a SPACE bit (bit 2 of character 2) is present at the signal input. This SPACE signal is applied to inputs M (prime "1A") and E (set "1B") of the synchronizing flip-flop, while the prime "1B" input (J) is primed by the output (K) of the stop inserter. The overall effect of the above action is to move the next start signal to the right. The fifth bit of character 2 is now recognized as the start signal. In character 3, similar action takes place, and by character 4 the Receiver is resynchronized with the incoming signal. During correction (or resynchronization) of the above error condition, two incorrect characters would have been recorded by the unit.

5.55 Automatic reset: If power is interrupted for some reason and restored, the synchronizer flip-flop could possibly be triggered to the set "1" condition. This would place a 0 volt signal on the input gate, preventing passage of a start pulse through the gate. To eliminate this problem, the automatic reset is utilized. When power is turned on, a reset pulse is generated and applied to the set "0A" input of the 0-level flip-flop and also to the set "1B" input of the control register flip-flop. This turns the start-stop oscillator on for one cycle to generate one shift pulse. The control register is triggered to the set "0" condition, and its inverted output (K) goes from -6 volts to 0 volt. This signal is applied to the stop inverter. The normal output (L) of the stop inserter is applied to the set "0A" input of the synchronizer flip-flop, resetting the circuit and preparing the unit to receive data.

5.56 Test conditions: With the TEST-OPERATE switch in the TEST condition, a -12 volt bias is applied to pin C of OR gate Z301A to simulate an open-line condition. In the TEST position, the circuit path from the synchronizer circuit to the pin D input of the signal gate is opened, and an alternate path is provided from the stop inserter. This allows local regeneration of blank characters (the stop inserter applying the stop pulse), so that local electronic testing can be carried out. Note that the synchronizer circuit will not be triggered; it will remain in the set "0" condition. A jack, J302, has been provided to facilitate local testing and to determine receiving margins. Using a data test set TSG801 or 800 (905A or 905B) working into a 1200 ohm load, apply a -6 to 0 volt (SPACE to MARK) test signal at this point. With the test signal applied, the synchronizer circuit will be triggered randomly.

D. Discrete Calling - Generator Kit

General

5.57 Since the discrete calling feature guards against tapes being released from unattended Tape Senders on unauthorized calls, the purpose of the receiver modification kit is to generate a valid call. Therefore, the calling station must generate the correct discrete 14-bit character for recognition at the unattended station before the tape will be released.

Operating Procedure to Initiate a Call

5.58 Procedure: (a) Place a call to the unattended Sender; (b) when the unattended sender terminal goes to the data mode on the completion of the 1200 cps (beep) tone, depress the data button on the data set at the receiving station to establish the data mode of operation; (c) then depress the transmitter start switch located on the new panel (TP199554); (d) data will be received at the receiver terminal following the three second recognizer cycle, provided that the sender and receiver terminals have been coded identically.

Theory of Operation

Detailed Description (Refer to 7025WD)

5.59 The sequence of operation of the discrete calling feature is shown graphically in Figure 11. A call is placed and the sending terminal data set answers. It responds with a marking tone if a 202A set is used, or a 2025 cps beep tone if a 202C set is used and then reverts to the receiving mode. The calling data set is then placed in the data mode by depressing the button marked DATA. The operator depresses the transmitter start button at the receiver terminal which turns on the data set request to send function and starts the generator (Z732). This is time 0.000 in Figure 11. The generator sends a 0.352 second space followed by a 0.230 second mark which is used to start the recognizer at the sending terminal. A sequence of 14 bits (0.167 seconds each) is then sent and compared at the recognizer on a bit by bit basis. At the end of this sequence the generator stops, the request to send function is turned off and the Receiver is now prepared to receive. At the Sender, if the recognizer found that all bits were valid, the request to send function is turned on and after a brief delay (timed by continued rotation of disc), the reader will be activated and the recognizer disc will stop. Should any received bit be invalid during the sequence of 14 bits, the reader will not be engaged and no transmission will begin. Thus, an unauthorized caller will not be able to start an unattended Sender. When the calling party hangs up, the Sender will disconnect automatically after a 30 second time out period.

5.60 The identifier logic consists of an electromechanical signal generator (TP-199570) and two relays; K-716L and K-716U. The signal generator is identified in wiring diagram 7025WD and the text as Z732. The multisegment disc of Z732 is rotated by a clock motor to provide the three second (current/no current) pattern for the coded signal and relay switching functions. One cycle of the disc (TP199580) provides the long space and fourteen element coded signal (local signal) as the respective brush rides against the successive segments. Another brush makes contact with an inner circle of the disc to provide the (identifier) homing signal. In this manner, a start-stop identification pattern is generated to key the data set which in turn supplies the outlying unattended transmitter with the transmitter start signal for the comparison check.

5.61 During one cycle of the disc, the local signal segments pulse the K-716U relay. The initial element is a long spacing signal (no current) followed by a 231MS marking pulse and fourteen codeable elements of unit length. When the normally open contacts 5 and 5M of relay K-716L are closed, the local signal sequence is directed to terminal A1/J701 - the send data lead to the data set. Relay K-716L is also used to energize the motor and release the clutch/brake and to activate the receiving distributor.

5.62 Signal Generator - Z732 consists of an ac synchronous motor which drives a codeable etched circuit board commutator (Fig. 15) having multiple levels or concentric rings of segments. Multiple (stationary) brushes make contact with the respective rings to sense the intelligence set up. The 20 RPM motor is energized by a 117 volt ac potential through contacts 1 and 1M of K-716L and the common lead. Note the clutch/brake release feature of the motor to restrain overtravel. Refer to Figure 14 for the timing diagram of the generator output.

5.63 When a call is initiated through the data set to the unattended station and the transmitter start switch located on the new panel is depressed, relay K-716L is energized. This relay is held in its operated position for the duration of the (identifier) homing pulse; refer to Figure 15. This relay starts the motor and energizes the clutch/brake to allow the disc to rotate. The relay drops out after the disc completes one cycle (approximately three seconds).

5.64 With relay K-716L operated, contacts 4 and 4M close to energize terminal C1/J701 - the request to send lead (+6 volts) to the data set.

5.65 A fifteen-bit transmitter start signal is generated by the (local signal) slip connection with the outer ring of the disc. This signal consists of a long spacing stop bit (350 MS - no current) followed by a marking start pulse and the fourteen mark or space coding bits. A marking signal is generated when continuity exists between the respective codeable segments (14 total) and the associated sampling segment to the common slip connector and the -28 volt supply. A spacing pulse occurs on coded segments not joined by the narrow ribbon. Thus, relay K-716U is energized on the marking pulses of the transmitter start signal. When this relay operates, the normally closed contacts 8 and 8B are opened to remove the +6 volt potential directed through K-716L toward terminal A1/J701 - the send data lead to the data set. Absence of a positive potential at the data set will provide a marking pulse to the line.

5.66 The receiving distributor and reperforator are blinded during the generation of a transmitter start signal. This is achieved by open circuiting the blind lead of the receiving distributor through relay K-716L.

5.67 The cable assembly (TP199553) connects the protected unattended transmitter identifier module, the automatic answer assembly (TP146528), the transmitter start switch and the ac power to the data set. The cable assembly also contains a 2.7K resistor. The resistor connects the +17.5 volt lead and the reverse channel send lead of a data set. This will generate a continuous reverse channel tone when a reverse channel type of data set is used.

E. Break Feature

5.68 The break feature makes use of the optional reverse channel feature, available with data sets 202C2 and 202D2, for circuit assurance and the break function. This feature is used to stop transmission automatically if circuit continuity is lost, and permits the receiving operator to interrupt transmission because of low tape, etc by pressing the data set TALK button. Sending stations in customer's systems that are arranged for the break feature can only transmit to Receivers also equipped with this feature. Shop instructions in the Installation section cover the changes needed to generate the steady reverse channel signal. Only terminal sets manufactured prior to December, 1964 and using the style Y-connector will require the addition of a 2700 ohm resistor in the plug connectors to the data set. Also a rearrangement of the connections to terminals 4 & 9 on the sender plug and terminals 9 & 11 on the receiver plug are made. These changes appear on all units manufactured after the December date.

TAPE SENDER AND RECEIVER

A. Transmit-Receive Terminal Kit (Early Design)

General

5.69 The transmit-receive terminal modification kit provides a means of connecting a tape sender terminal and a tape receiver terminal - located at the same installation - to a common model 202A or 202B data set. This feature allows both terminals to be serviced alternately by one data set.

5.70 Switching of the common data set from one terminal to the other terminal is facilitated by a three-position switch mounted on the front of the Tape Sender cabinet. Either terminal may be selected to operate with the data set. It is not possible, however, to operate both terminals at the same time. This feature available in kit form (TP146532) for field or factory installation is superseded by modification kit TP199610.

Detailed Circuit Description

Note: Refer to Schematic Wiring Diagram 4799WD.

5.71 The selector switch mounted on the front of the Tape Sender cabinet has three positions: TEST, RECEIVE, and SEND. Depending upon which position the switch is in, either the sender or receiver terminal is connected to the data set, or the terminals are tied together for test purposes.

(a) In the TEST position, the interlock signal path is completed to both the sender and receiver terminals and the request to send path is completed to the data set, turning on the modulator. In this condition, the sender terminal can transmit to the receiver terminal for local test purposes. The remote control common path to the receiver terminal is also open, disabling the automatic answer feature.

(b) In the RECEIVE position, the interlock signal path is completed to the receiver terminal only, turning on the tape punch and tape winder motors. The request to send path to the data set is open, disabling the modulator in the data set. The remote control common path to the Receiver is completed, enabling the automatic answer circuit at the receiver terminal.

(c) In the SEND position, the interlock signal path is completed to the sender terminal only, turning on the tape reader and tape winder motors. The request to send path to the data set is completed, enabling the modulator. The remote control common path is completed to the Sender, enabling the line break and automatic answer feature at the sender terminal.

5.72 For automatic operation, the Tape Sender line break and automatic answer TEST-OPERATE switch must be in OPERATE position, and the AUTO-MANUAL switch must be in AUTO position. The data set AUTO and DATA push buttons must be depressed.

5.73 Until the line break feature is incorporated in the 202A and 202B data sets, the tape reader motor and tape winder motor must be manually turned on, and the tape reader manually started. To manually energize these motors, the AUTO-MANUAL switch must be in the MANUAL position. The respective motor switches may then be operated to their ON position. The tape reader is started by first loading the reader with tape, and then operating the RUN-STOP switch to the RUN position.

5.74 Full duplex operation with the 202B data set is available when the transmit-receive selector switch is in the TEST position.

B. Send-Receive Terminal Kit (Later Design)

General

5.75 The new "Y" connector differs from the old one in that a new SEND-RECEIVE switch position is added. The test position is retained for use in (a) reperforating tapes locally by sending intelligence through the data set and back to its send-receive station, and (b) full duplex operation on 4-wire facilities. The kit (TP199610) replaces the current cable connector TP146532.

Theory of Operation

5.76 The TP199620 "Y" cable assembly is used to connect a Sender and a Receiver together to a common type 202A, B, C or D data set. The cable assembly contains the send-receive (S-R) switch, two optional resistors and two optional straps.

5.77 The send-receiver (S-R) switch is a four position rotary switch. The position designations are send, receive, send-receive, and test clockwise respectively.

(a) In the send position, the terminal will allow manual or unattended send-only operation. In this position the sender terminal is operated by the data set ready lead. The data set send data, request to send, ready, and data terminal ready leads are controlled by the sender terminal. The request to send lead is controlled by the sender terminal interface lead 4, request to send (A/M). This interface lead is used when the sender terminal is operated in the unattended (automatic) or manual modes.

(b) In the receive position, the terminal will allow manual or unattended receive only operation. In this position, the receiver terminal is operated by the data set ready lead. The send data, request to send, ready, and data terminal ready leads are controlled by the receiver terminal.

(c) In the send-receive position, the terminal will allow unattended send or receive (half-duplex) operation. In this position, the sender and the receiver terminals are operated by the data set ready lead. The send data and request to send leads are controlled by the sender terminal. The ready and data terminal ready leads are controlled by the receiver terminal.

(1) The request to send lead is controlled by the sender terminals interface lead 14, request to send (A). This interface lead is used when the sender terminal is operated in the unattended (automatic) mode.

(2) A data set with a contact interface for automatic answering will automatically answer a call if terminals 20 and 21 of the receiver terminal connector RT are connected together. (The AUTO button of the data set must be depressed also.) After a call has been answered by a data set, it is necessary for terminals 20 and 21 to remain connected on the receiver terminal connector RT and for terminals 19 and 20 to be connected together on the sender terminal connector ST. This will prevent the data set from dropping a call. At end of transmission, the sender terminal must open the connection between 20 and 21 of the sender terminal connector ST in order to automatically drop a call.

(d) In the test position, the terminal will allow terminal testing (two-wire transmission), or manual or unattended send and receive (full-duplex) operation (four-wire transmission). In this position, the sender and the receiver terminals are operated by the data set ready lead. The data set send data and request to send leads are controlled by the sender terminal. The ready and data terminal ready leads are controlled by the receiver terminal. The request to send lead is controlled by the sender terminal interface lead 4, request to send (A/M). This interface lead can only be used when a sender terminal permanently applies a request to send signal.

5.78 The data set receive data, clear to send, signal ground, and ring indicator leads are connected to both sender and receiver terminal connectors ST and RT respectively. The data set carrier detect and reverse channel receive and release are leads connected to the sender terminal connector ST. Because the release lead is connected to the sender terminal only, an automatic disconnect can only be initiated by a sender terminal. The data set reverse channel send lead is connected to the receive terminal connector RT.

5.79 Two optional resistors are provided. They terminate on the send-receive (S-R) switch and are connected to the data set +17.5 volt lead. Resistor R2001 is used to supply a permanent request to send when the send-receive (S-R) switch is in the send or test positions. This resistor is not necessary and must be removed when the sender terminal is equipped with the 199551 protected unattended transmitter modification kit. R2002 is used to supply a permanent reverse channel send and is intended to be optionally removed in the future.

5.80 Two optional straps are provided. They terminate on the send-receive (S-R) switch and are used to provide appropriate receiver terminal blinds. Strap A is used to connect the data set carrier detect lead to the receiver terminal connector RT. This strap must be removed when the sender terminal is equipped with the TP199551 protected unattended transmitter modification kit. Strap B is used to connect the sender interface lead 13, blind to the receiver terminal interface lead 8, carrier detect. This strap is intended to be optionally removed in the future.

Operating Procedures

5.81 Two-Wire Transmission.

(a) Manual Operation: Select either the send or the receive position before or after depressing the DATA button on the data set. It is necessary for the terminals to be in the manual mode of operation.

(b) Unattended Operation: Select either the send, the receive or the send-receive position before depressing the AUTO button on the data set. It is necessary for the terminals to be in the unattended (AUTO) mode of operation.

(c) Terminal Testing: Select the test position before depressing the DATA button on the data set and then engage the reader to transmit. The Receiver will monitor the sender terminals transmission under proper data set operation. It is necessary for the terminals to be in the manual mode of operation.

5.82 Four-Wire Transmission.

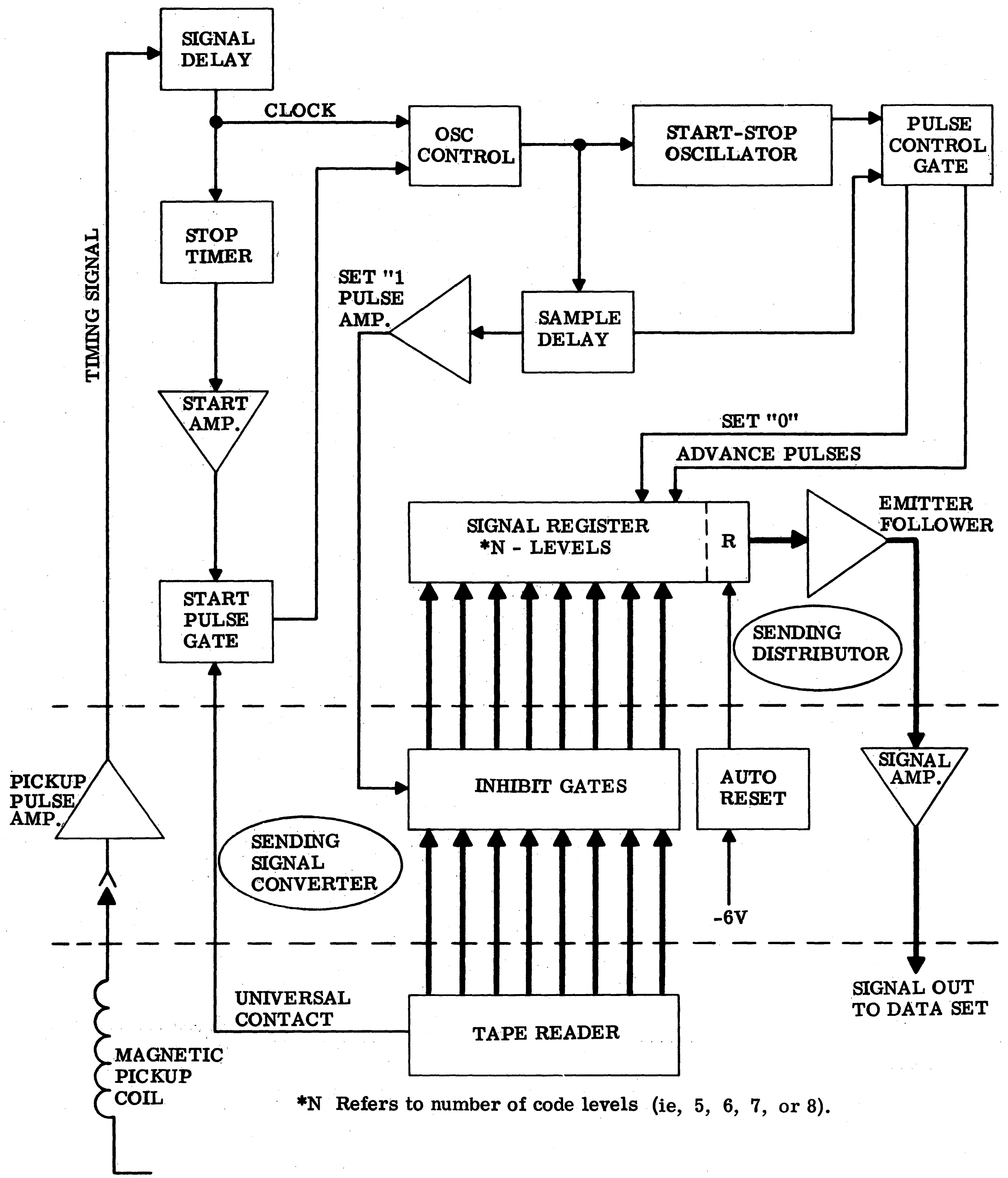
(a) Manual Operation: Select the test position before depressing the DATA button on the data set. It is necessary for the terminals to be in the manual mode of operation.

(b) Unattended Operation: Select the test position before depressing the AUTO button on the data set. It is necessary for the terminals to be in the unattended (AUTO) mode of operation.

Test Procedures

5.83 To test the modification kit, it will be necessary for the data test center to call send-receive terminal and check the terminal operations in its various possible modes of operation.

Note: Remove resistor R2001 and strap A (yellow wire) when sender terminals VS217 and VS219 are equipped with a TP199551 protected unattended transmitter modification kit. Refer to 7024WD.



*N Refers to number of code levels (ie, 5, 6, 7, or 8).

Figure 2 - Tape Sender Block Diagram

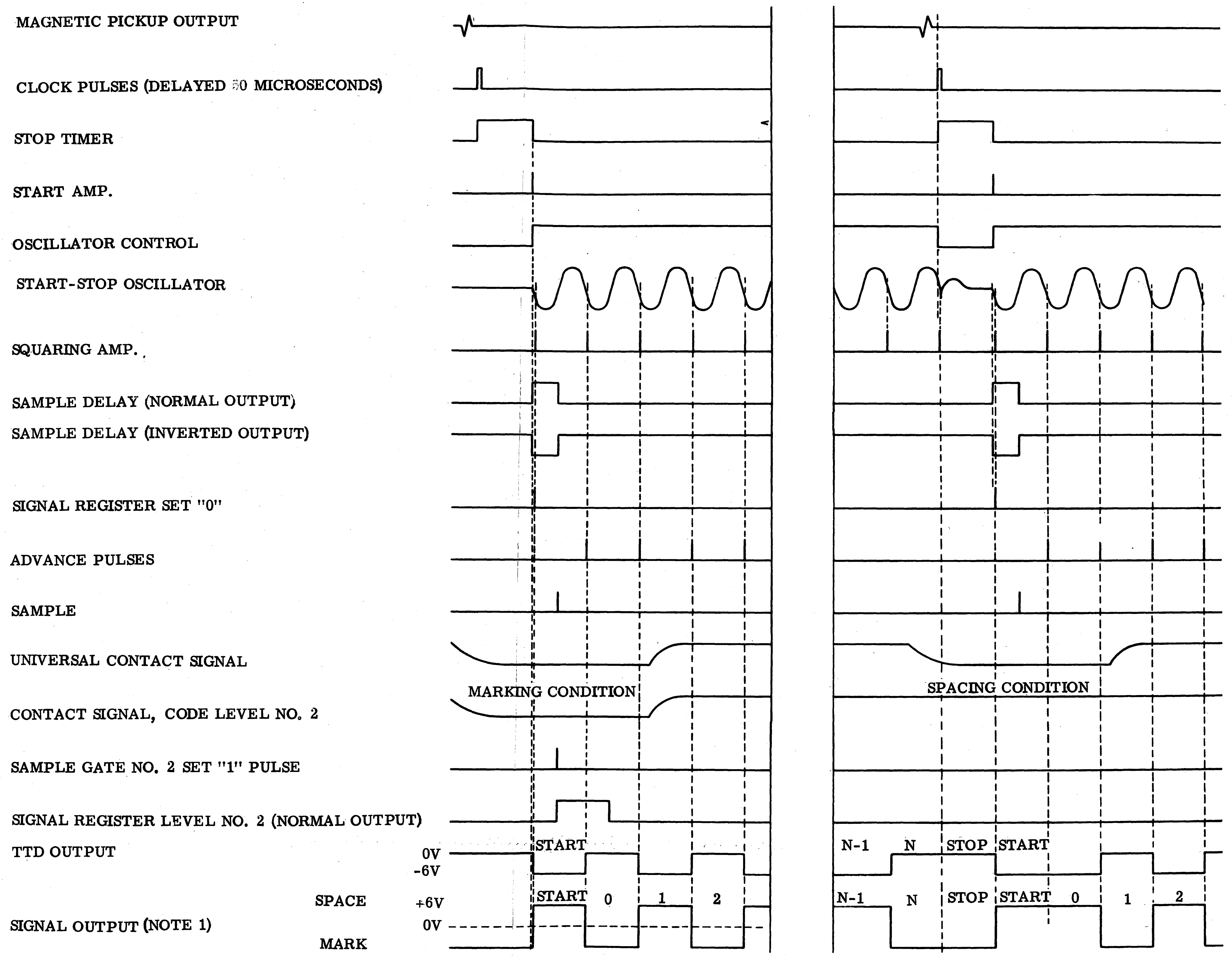
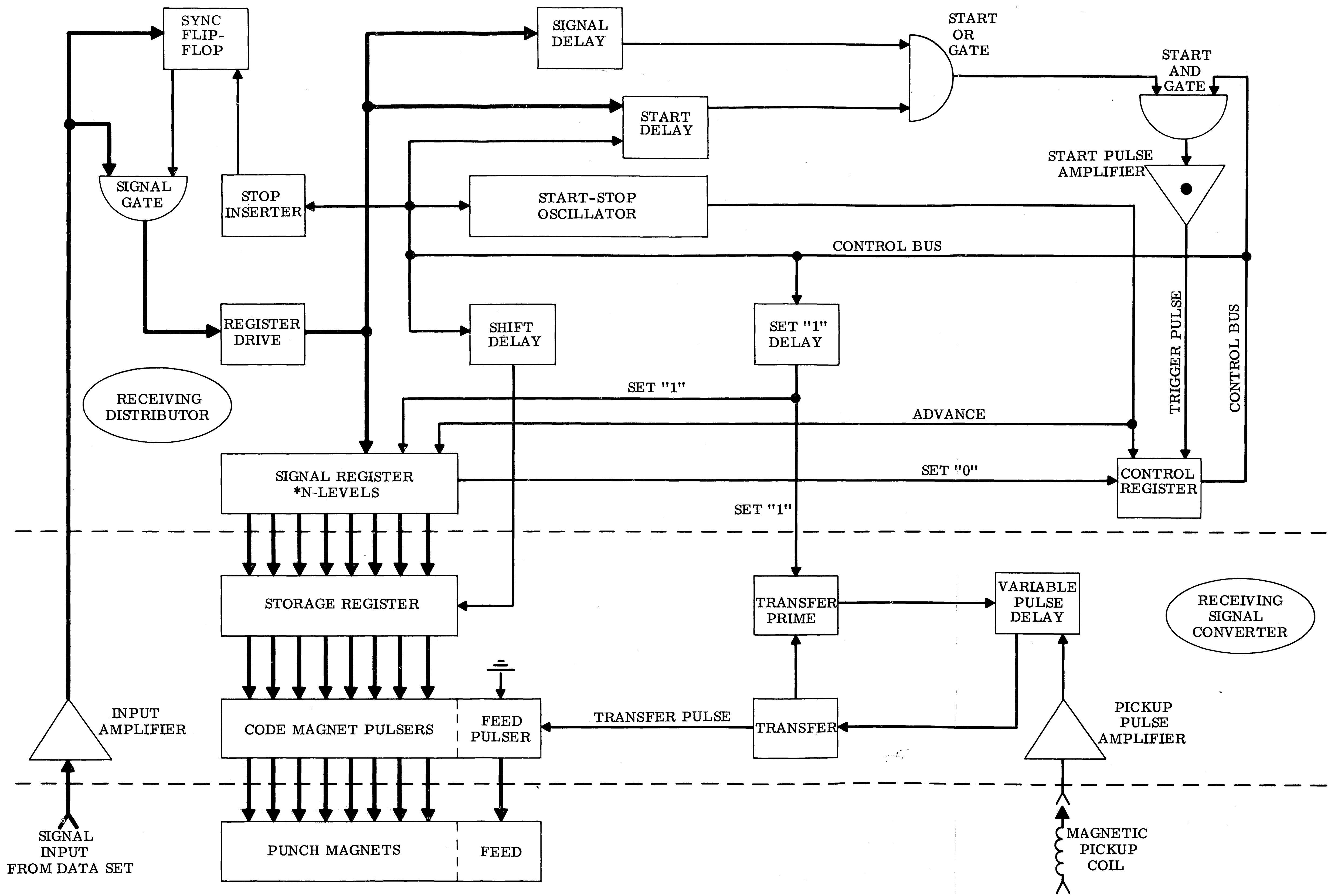
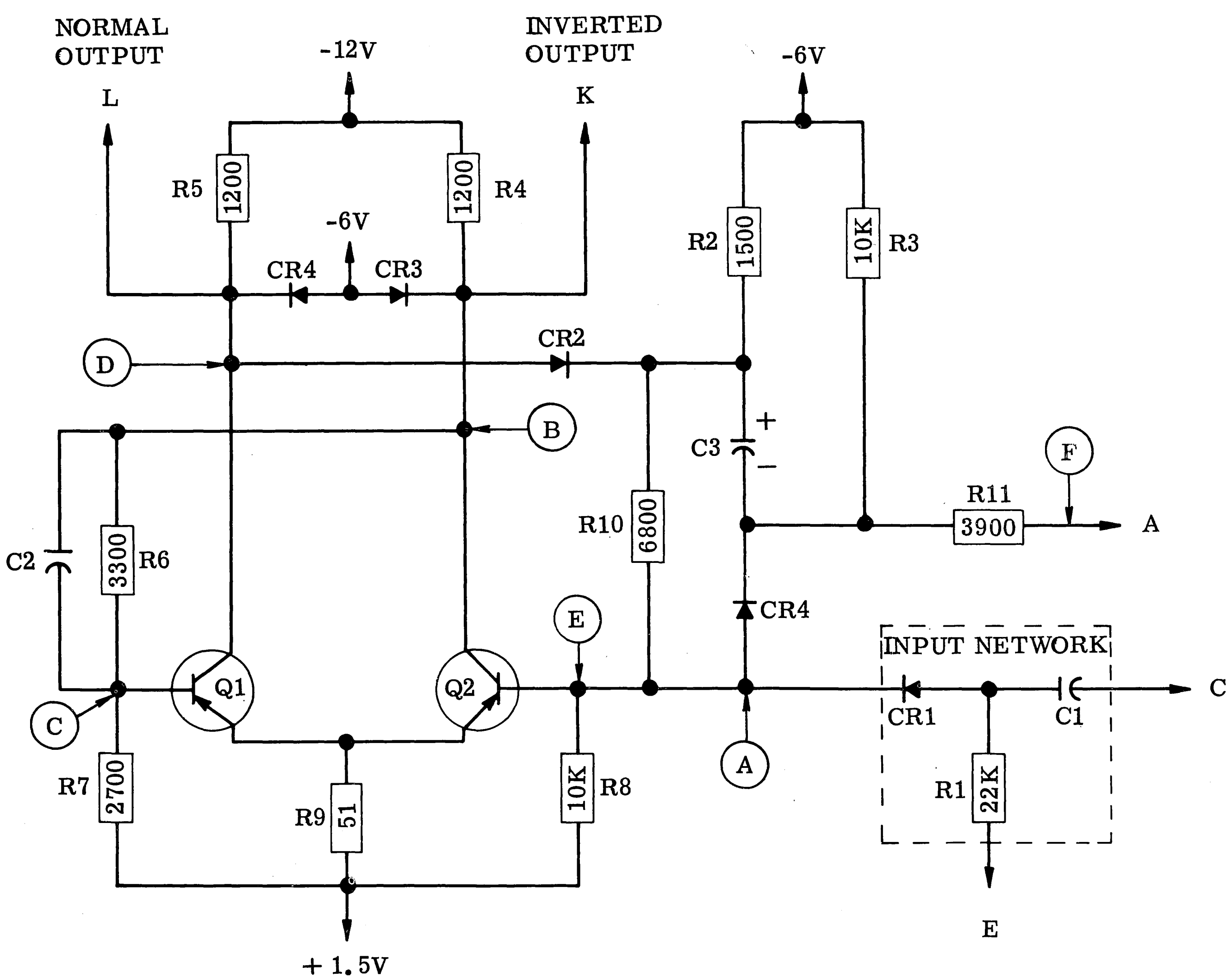


Figure 3 - Tape Sender Timing Diagram

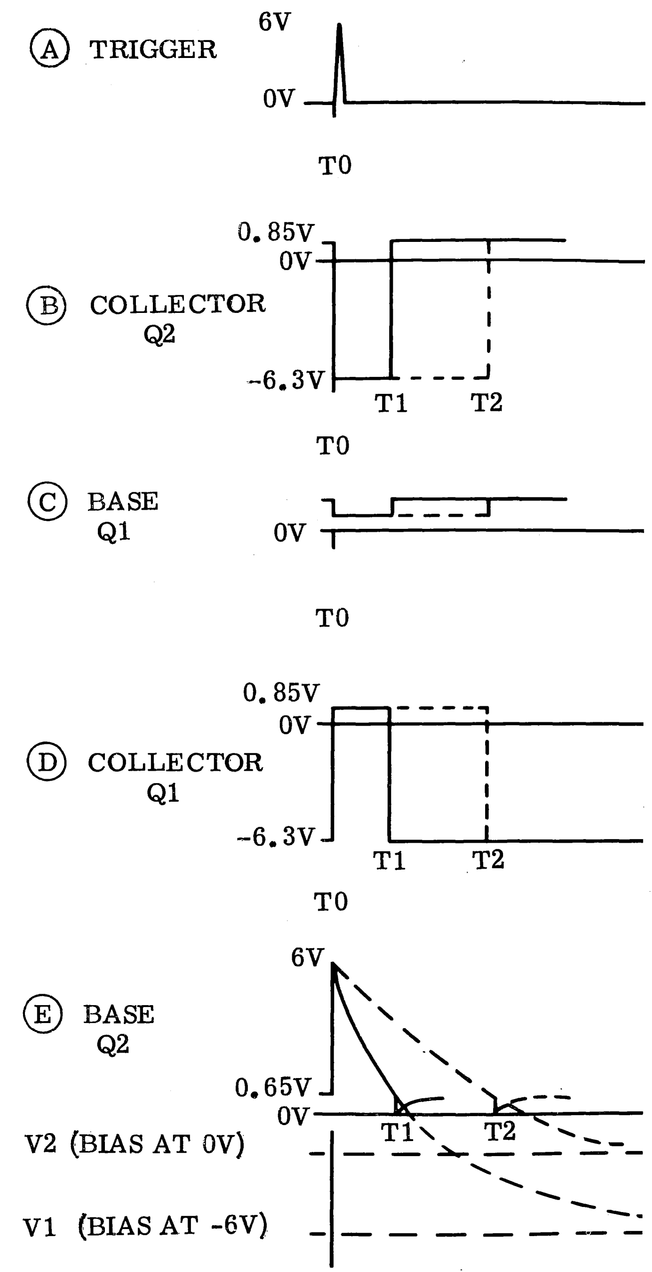


*N REFERS TO NUMBER OF CODE LEVELS (IE, 5, 6, 7 OR 8).

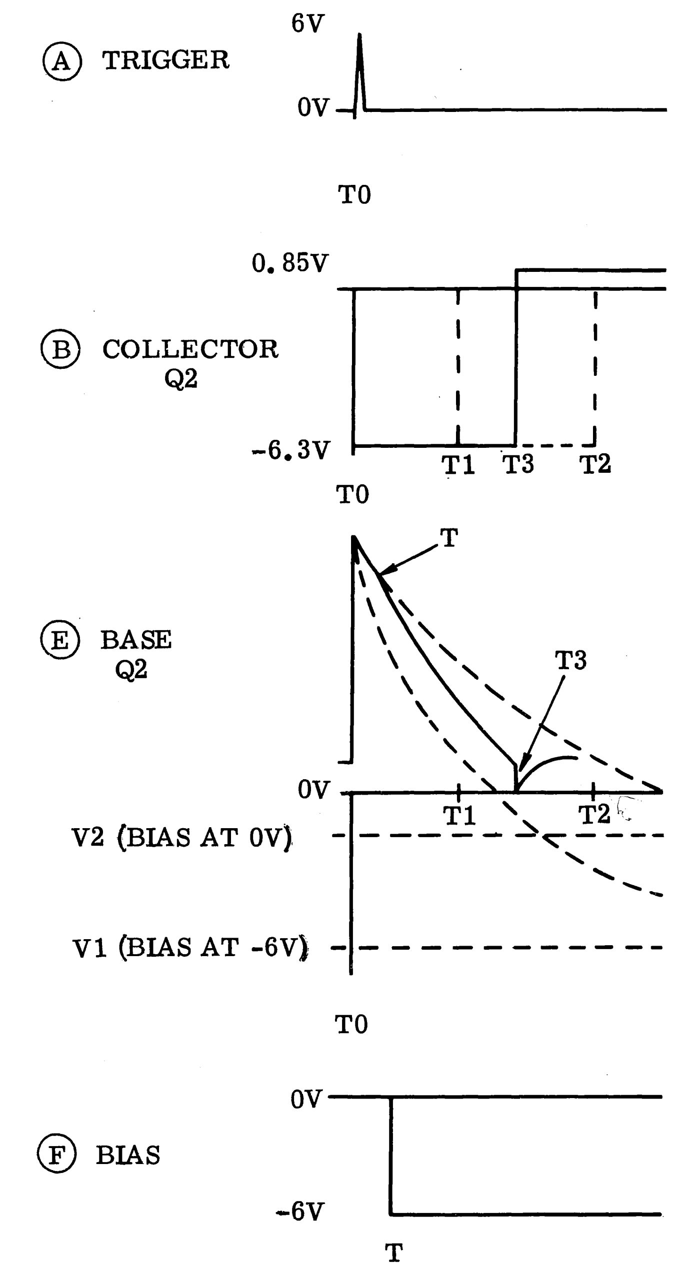
Figure 4 - Tape Receiver Block Diagram



(A) Variable Pulse Delay Circuit



(B) Variable Delay Waveforms, Fixed Bias Condition



(C) Variable Delay Waveforms, Variable Bias Condition

Figure 5 - Variable Pulse Delay

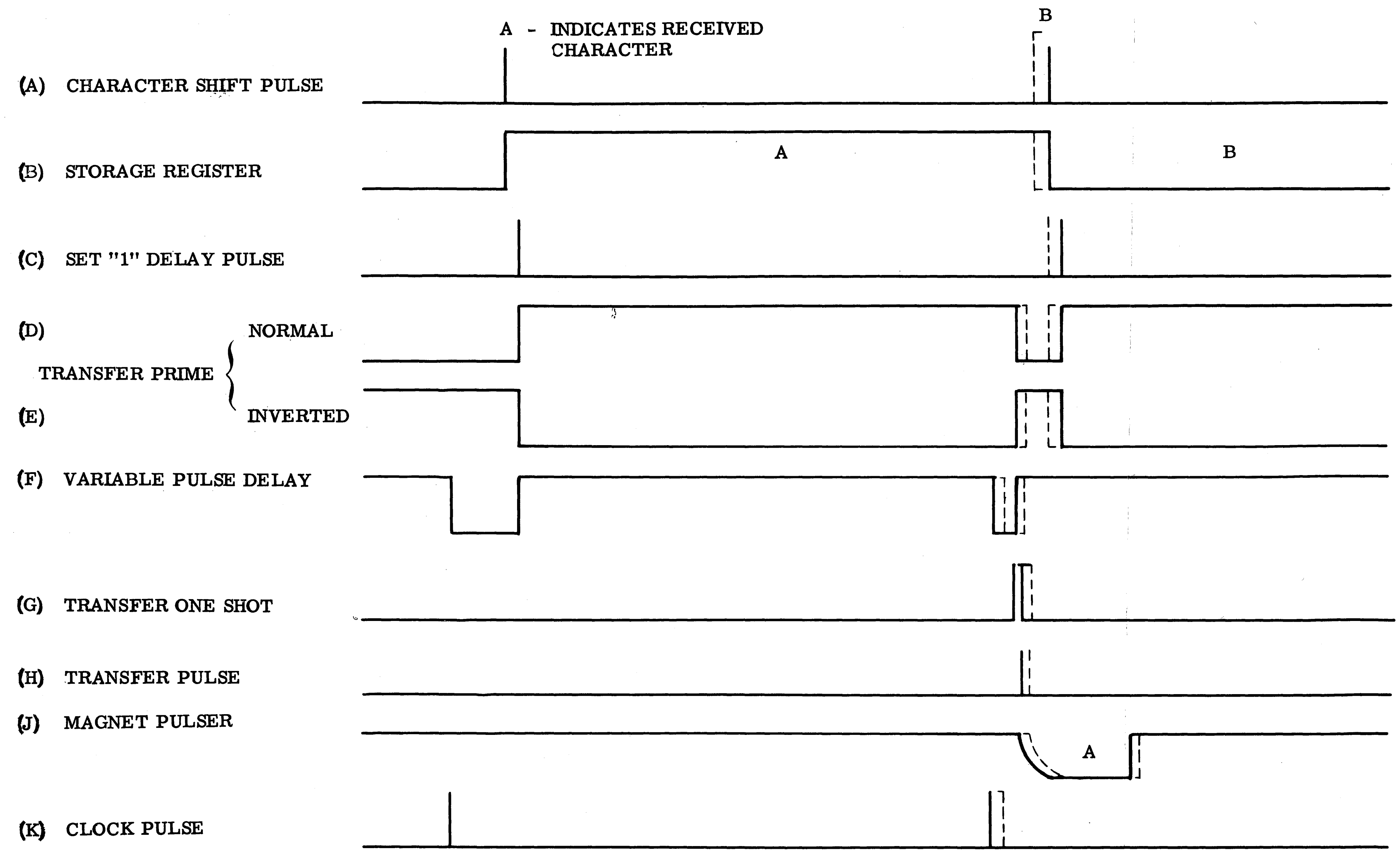


Figure 6 - Transfer Circuitry Timing Diagram, One Cycle of Operation

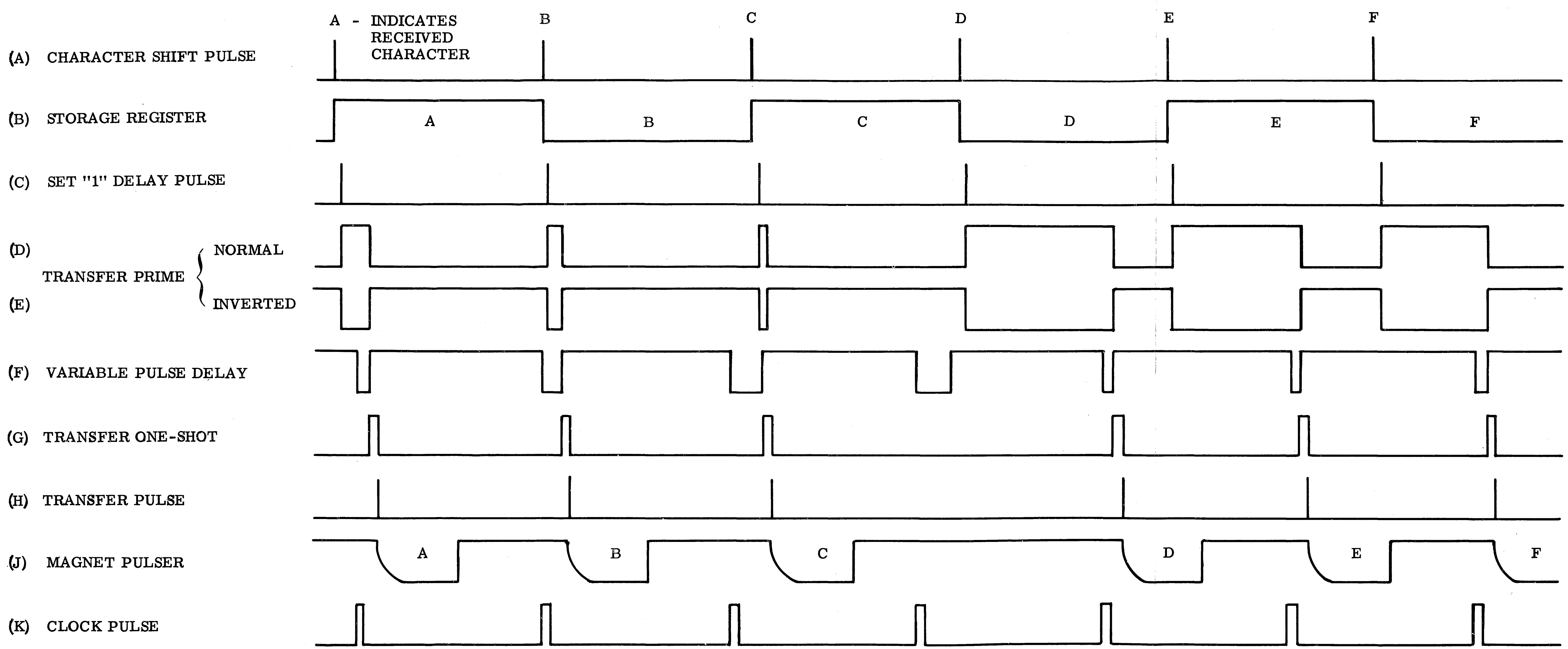


Figure 7 - Transfer Circuitry Timing Diagram, Several Cycles of Operation

NOTE 1: BIT WIDTH

BAUD	OSCILLATOR FREQUENCY	BIT WIDTH MILLISECONDS
600	600 CPS	1.66
750	750 CPS	1.33
900	900 CPS	1.11
1050	1050 CPS	0.95

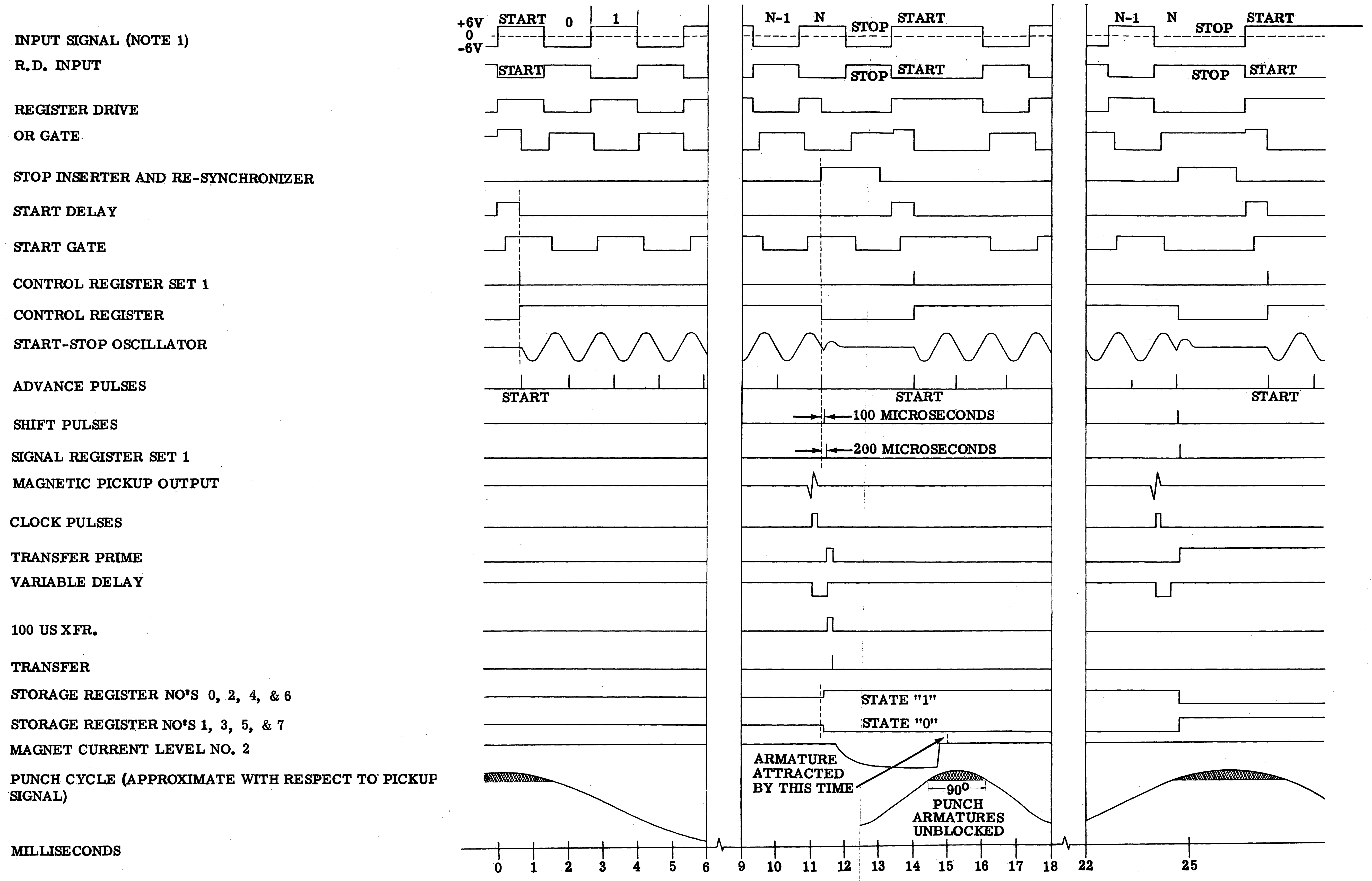


Figure 8 - Tape Receiver Timing Diagram

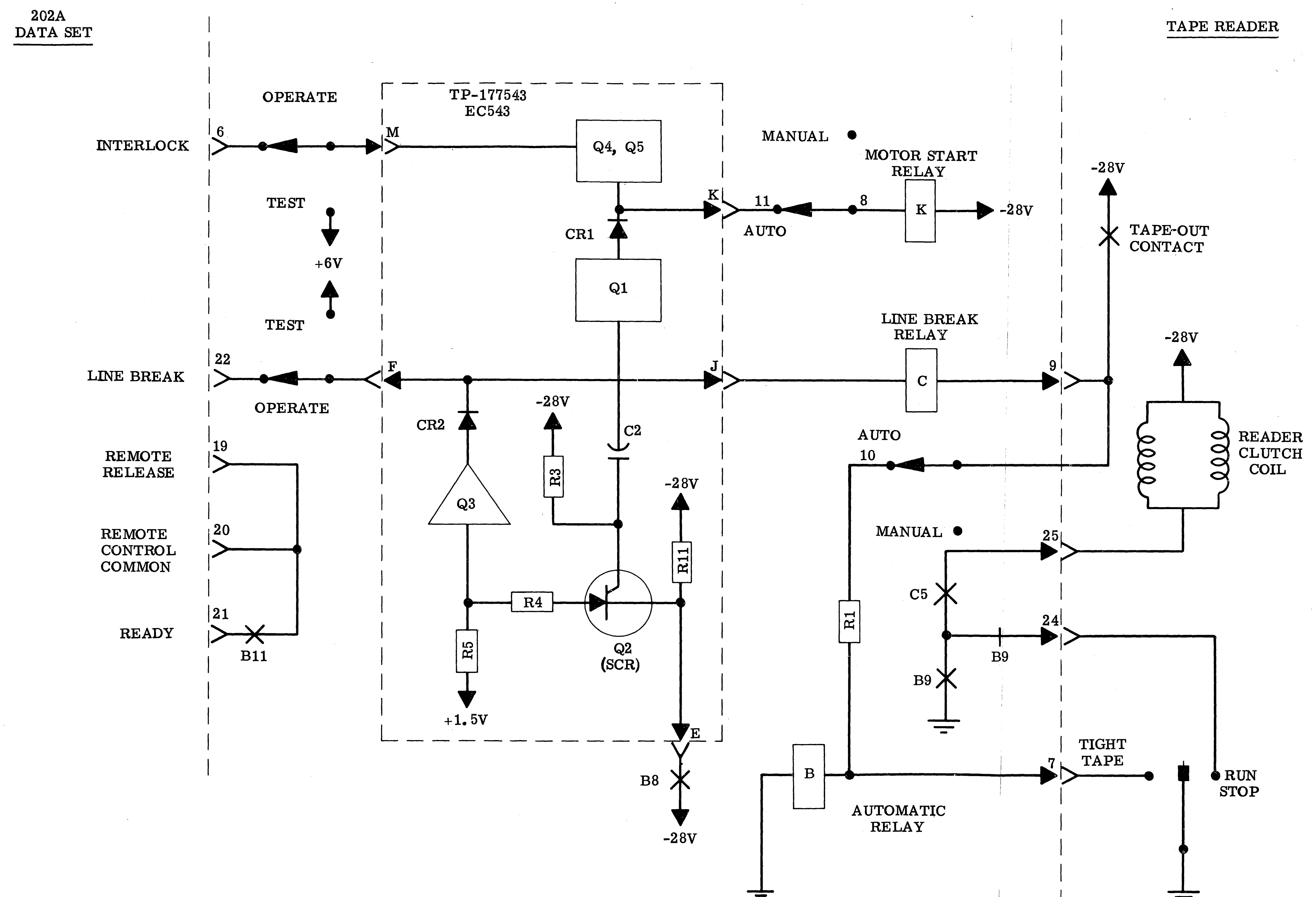


Figure 9 - Interim Unattended Answer Circuit

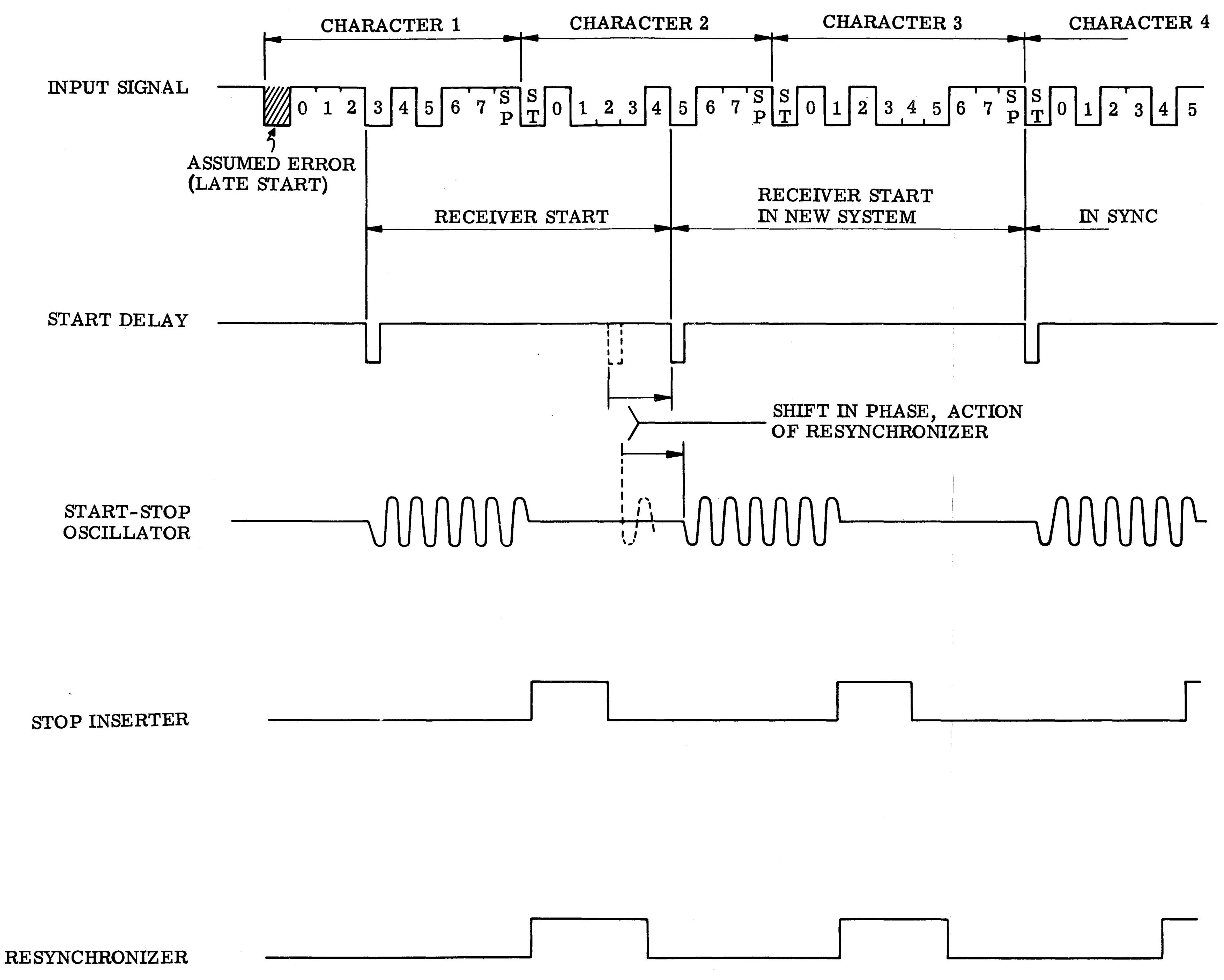


Figure 10 - Resynchronizer Circuit
Timing Diagram

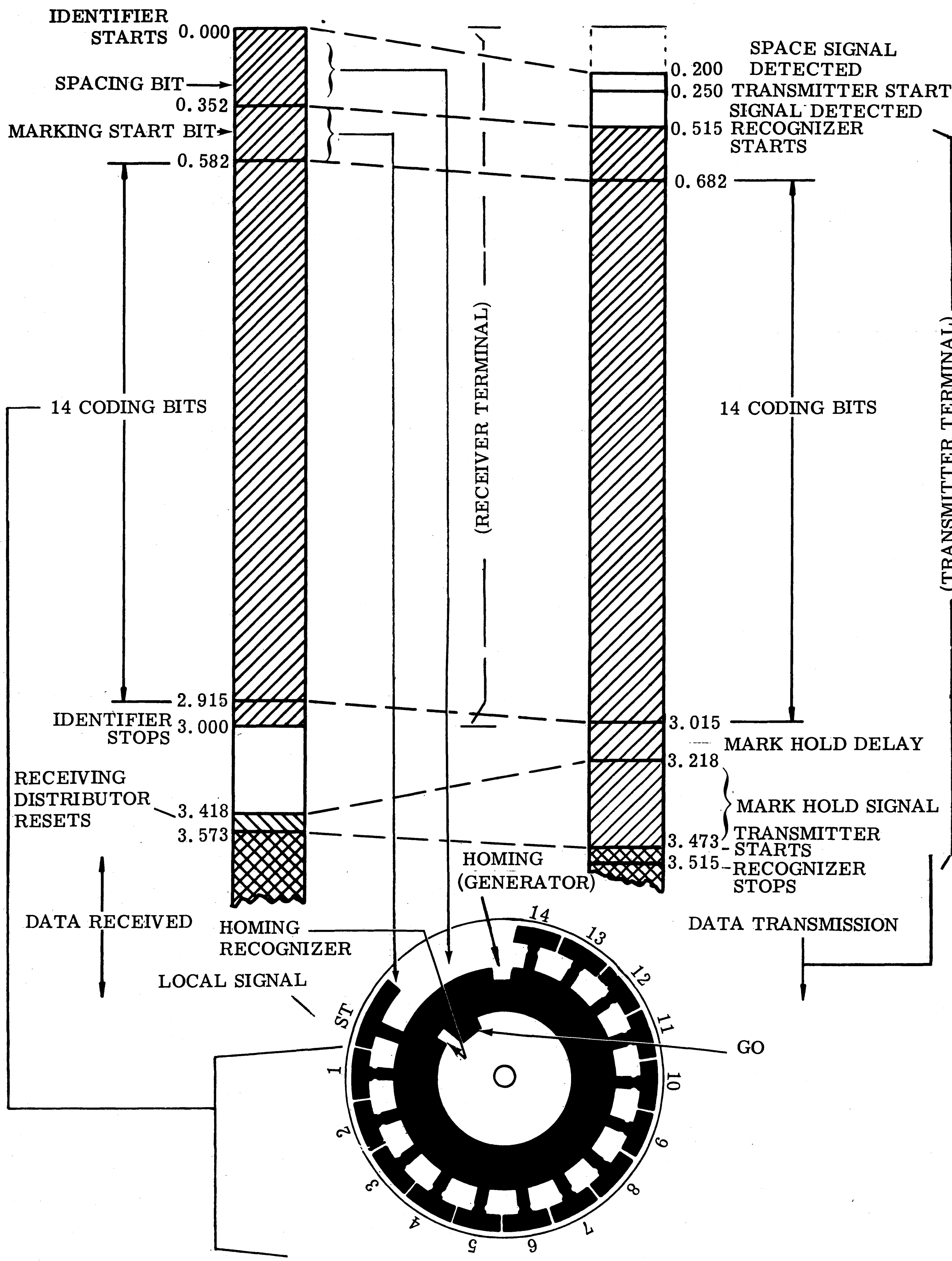


Figure 11. Timing Diagram for Tape-to-Tape System with the Protected Unattended Transmitter Feature

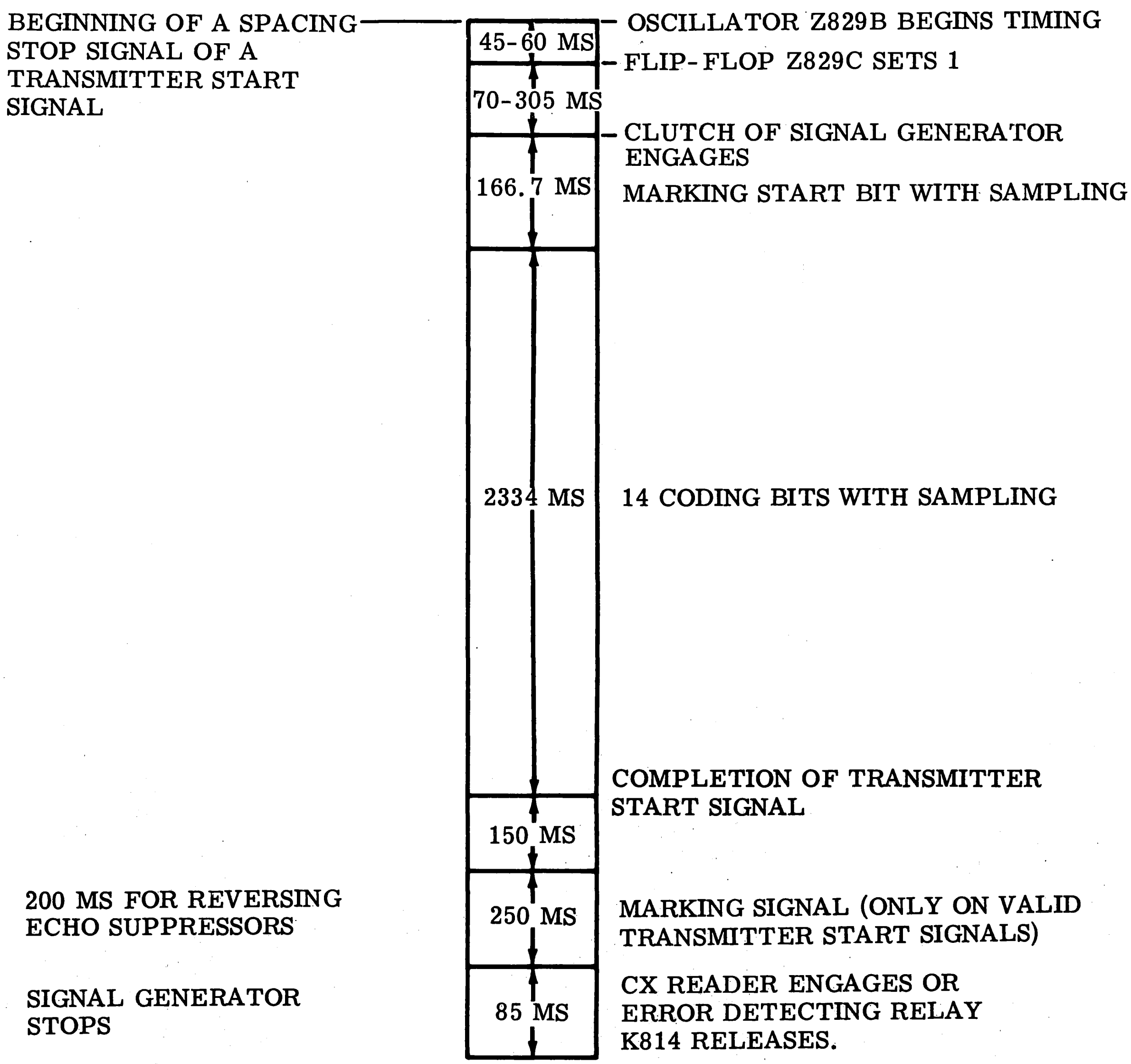


Figure 12. Timing Diagram for Discrete Calling, Unattended Transmitter

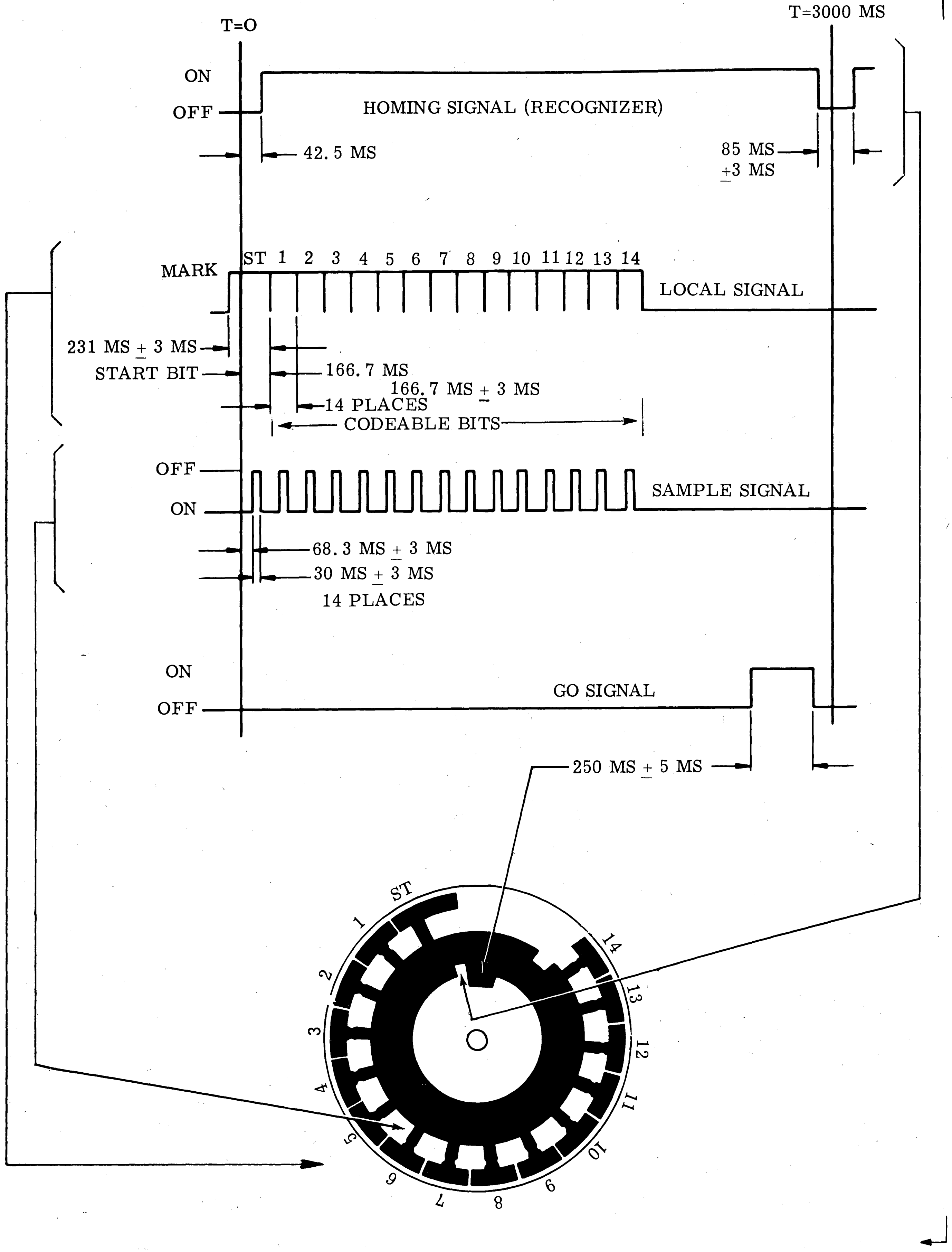


Figure 13. Recognizer Signal Pattern (Sender Unit)

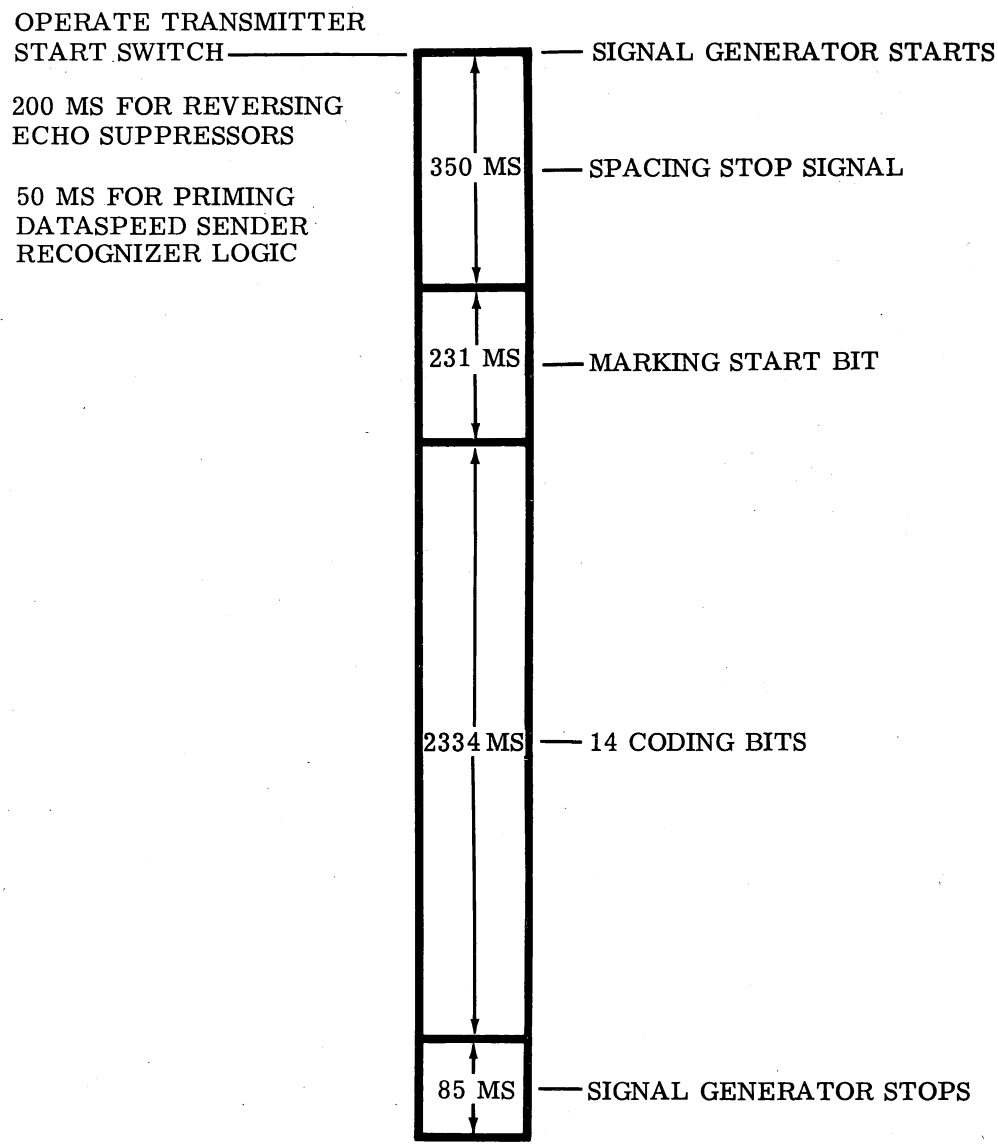
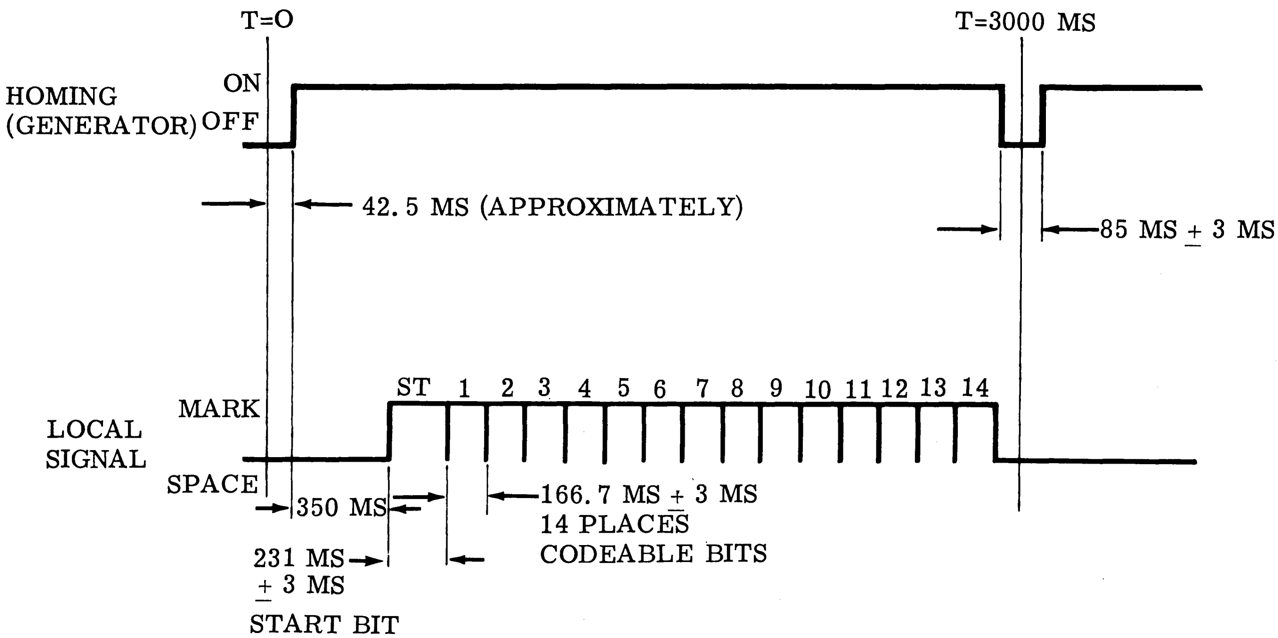


Figure 14. Timing Diagram for Discrete Calling, Attended Receiver



NOTE: CODEABLE BITS MUST BE IDENTICAL TO CODED DISC OF TRANSMITTER RECOGNIZER.

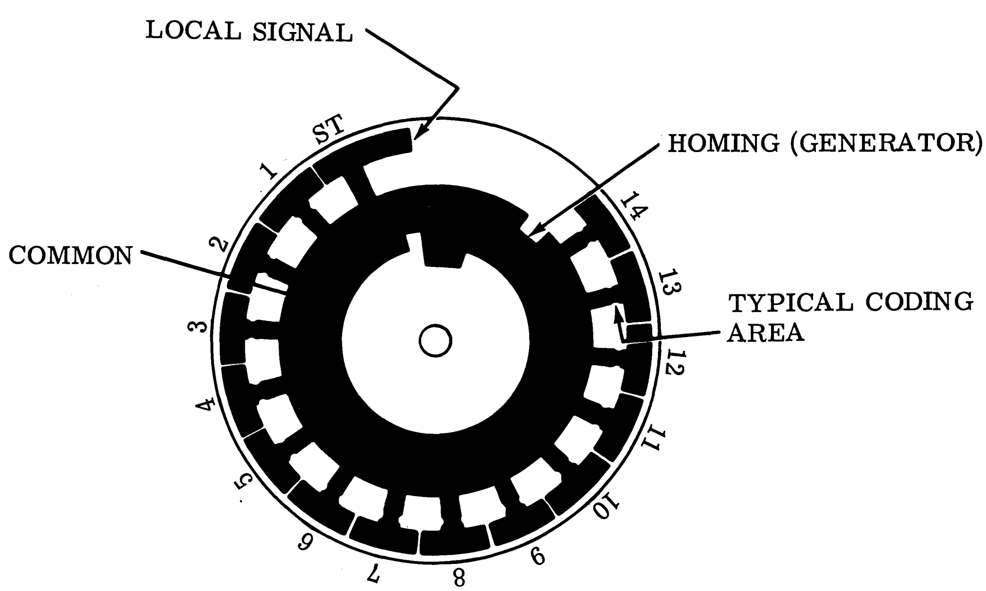


Figure 15. Identifier Timing Diagram - Receiver