REPLACING PAGE ADDENDUM
Filing Instructions:

1. REMOVE FROM THE SECTION THE PAGES NUMBERED THE SAME AS THOSE ATTACHED TO THIS PINK SHEET.
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"DATASPEED"* TAPE SENDER

WITH ERROR DETECTION AND CORRECTION

TYPE 4A

DESCRIPTION AND OPERATION

1. GENERAL

1.001 This addendum, which supplements Section 592-811-100, Issue 1, is issued to incorporate engineering changes and to add coverage on the Module Features and the Shift Register Operation. Arrows in the margin indicate changes and additions.

1.002 Insert the attached pages in accordance with the filing instructions above.

Attached:
Page 29 dated April 1973, revised
Page 30 dated April 1973, reissued
Page 47 dated April 1973, reissued
Page 48 dated April 1973, revised
Page 49 dated April 1973, revised
Page 50 dated April 1973, reissued
Page 53 dated April 1973, reissued
Page 54 dated April 1973, revised

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DESCRIPTION AND OPERATION

CONTENTS PAGE

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Prepared for American Telephone and Telegraph Company by Teletype Corporation

CONTENTS PAGE

1. GENERAL

1.01 This section provides the description and operation for the "DATASPEED" Tape Sender Type 4A. The sender has error detection and correction (EDC) capabilities and is used in a high speed punched tape data transmission system.

1.02 The sender converts information in punched tape into sequential binary data suitable for transmission at 1050 wpm over standard switched telephone networks or private lines. An alternate speed of 1200 wpm may be obtained using accessory equipment. The data set used is type 202.

1.03 Error detection is accomplished by using block-by-block transmission with redundancy information (check characters) included at the end of each 80-character block. Errors are corrected by deletion of the errored block by over punching at the receiver terminal, and then retransmission.

1.04 Refer to the appropriate sections for a description of the tape reader (DX type) and 202-type data set.

2. COMPONENTS

2.01 The major sender components are a high speed tape reader (DX-type), a tape transport assembly, a high speed error detection and correction (HSEDC) transmitter control module, a high speed transmitter distributor module, a station control module, and a cabinet. See Figures 1 through 8. Schematic wiring diagrams are:

Tape Sender 4A -	7038WD
Cabinet, ac cabling -	7035WD
Tape transport assembly -	7065WD
HSEDC transmitter control module -	7056WD
Transmitter distributor module -	7410WD
Station control module -	7403WD

2.02 The sender cabinet is 54 inches high, 20-1/2 inches wide and 24 inches deep.

2.03 The reader and tape transport assembly are mounted in the upper portion of the cabinet, above the data set.

2.04 The sender electronics is contained on etched circuit boards in two modules (HSEDC transmitter control and transmitter distributor) in the lower cabinet, and in the station control module, located behind the data set.

3. TECHNICAL DATA

3.01 The sender converts parallel output signals generated by a high speed tape reader and by the error detection and correction (EDC) electronics into a standard binary serialized data signal suitable for driving a 202-type data set.

3.02 The reverse channel feature provided by the data set is used by the sender to determine that an error was detected at the receiving terminal. If the feature is not provided with the data set, an auxiliary telephone circuit is required.

3.03 The sender transmits data in blocks of 80 characters. The tape being read does not have to be divided into discrete 80 character blocks.

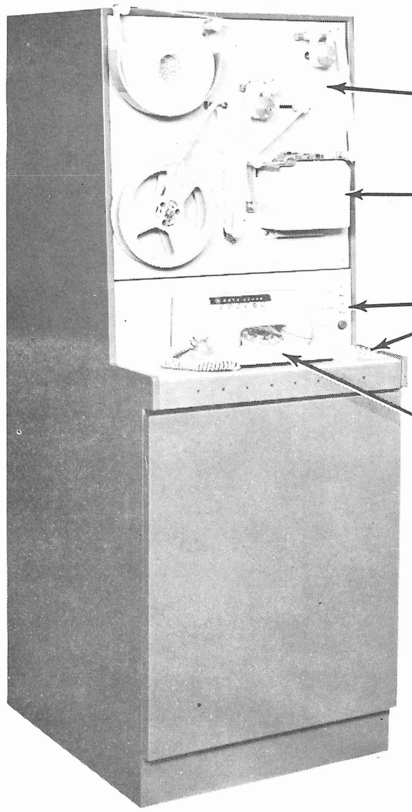

Figure 1 - Tape Sender 4A

3.04 Before transmission of the data, the sender inserts and sends SR (sender ready) characters. These characters are transmitted until the receiver detects them and turns on reverse channel.

3.05 When the sender recognizes reverse channel on, it sends a BN (block number) character. There are three different BN characters. One each is transmitted before successive blocks and thereafter repeated during transmission of the data type. These characters are used to maintain block synchronization with the receiver.

3.06 After transmission of a BN character, the sender transmits 80 information characters followed by an EOB (end of block) character. During transmission of the EOB character, the reverse channel is sampled. Then two longitudinal parity check characters, CK1 (check character 1) and CK2 (check character 2), are transmitted. CK1 is derived from a horizontal parity check of the 80 information characters and CK2 is derived from a spiral parity check of the 80 information characters.

3.07 If the reverse channel was on when sampled, the next block is transmitted, preceded by the next block number and followed by the EOB character and the two derived check characters.

3.08 The sender is told an error has been detected by the removal of reverse channel. Since the receiver does not detect the error until after the check characters are sent, the reverse channel will not be detected as being off until the end of the block following the errored block. When the loss of reverse channel is detected, the sender advances to the error correction mode. The check characters are deleted, the

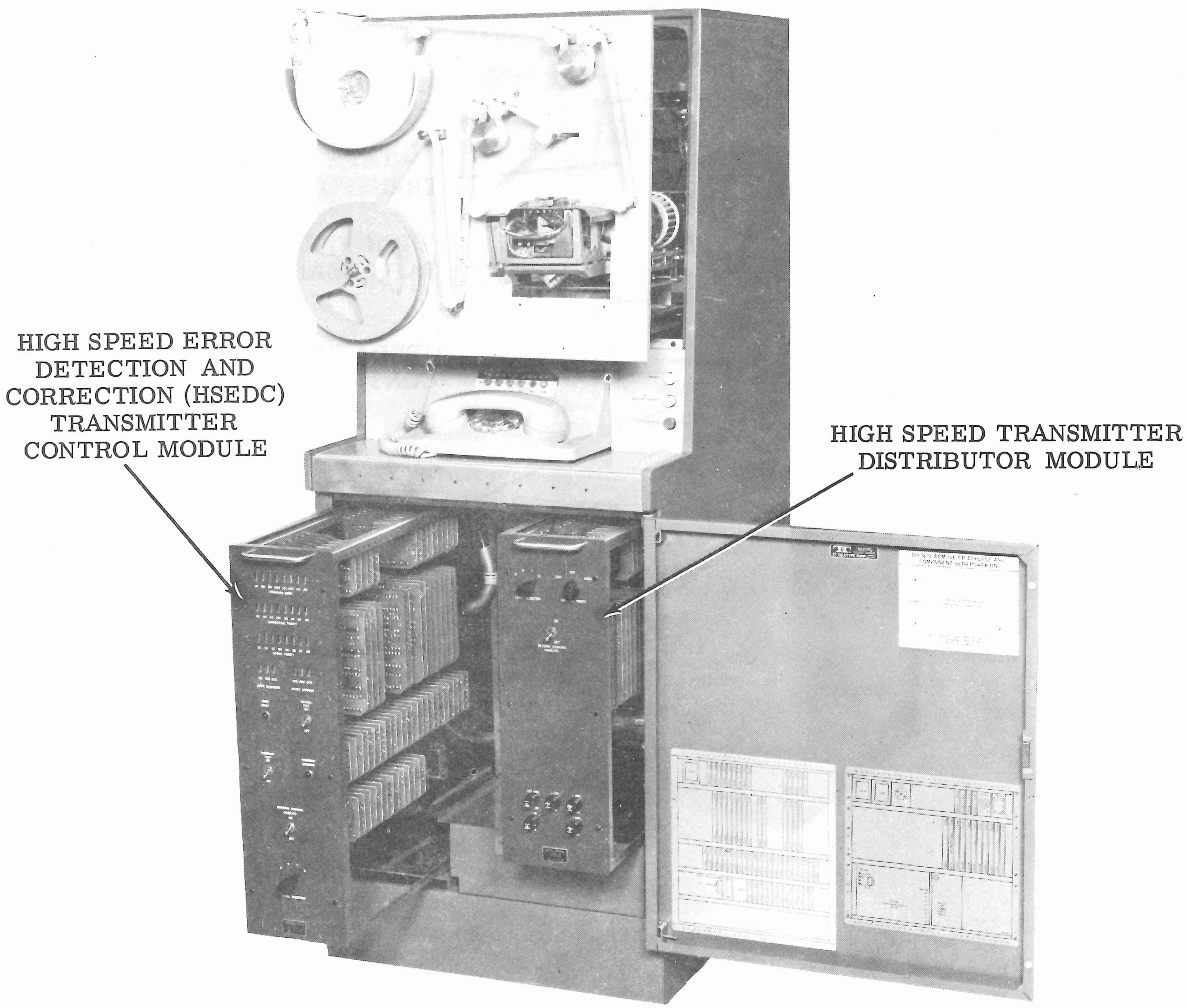

Figure 2 - Tape Sender 4A

reader reverses, backing up the tape two blocks (160 characters) to the beginning of the errored block and stops, and the sender starts sending SR characters, in this case signaling it is ready to retransmit the errored block. During the error correction mode, the sender keeps a steady marking signal on the data communications channel.

3.09 The number of consecutive retransmissions following the detection of an error is limited to three.

3.10 The basic sender provides for transmission under manual control. It is capable of operating in the normal EDC mode or in a selectable NON-EDC mode for transmission to a High Speed Tape-to-Tape System (Type 2) receiving terminals equipped with the reverse channel feature. For transmission to these receiving terminals not equipped with the reverse channel feature, a switch mounted on the front plate of the transmitting distributor module simulates the reverse channel feature.

3.11 A pushbutton (STOP/ALARM-RESET) is provided on the front panel for the operator to interrupt and stop transmission without breaking the telephone and data communications channel. An indicator light (RECEIVER STOPPED) provided on the front panel, lights when reverse channel is lost and is used to notify the sender operator that the receiver operator wishes to communicate over the telephone circuit. Since the loss and recovery of reverse channel is a normal part of the EDC operation, the indicator light on for a period of time less than 60 seconds has no meaning.

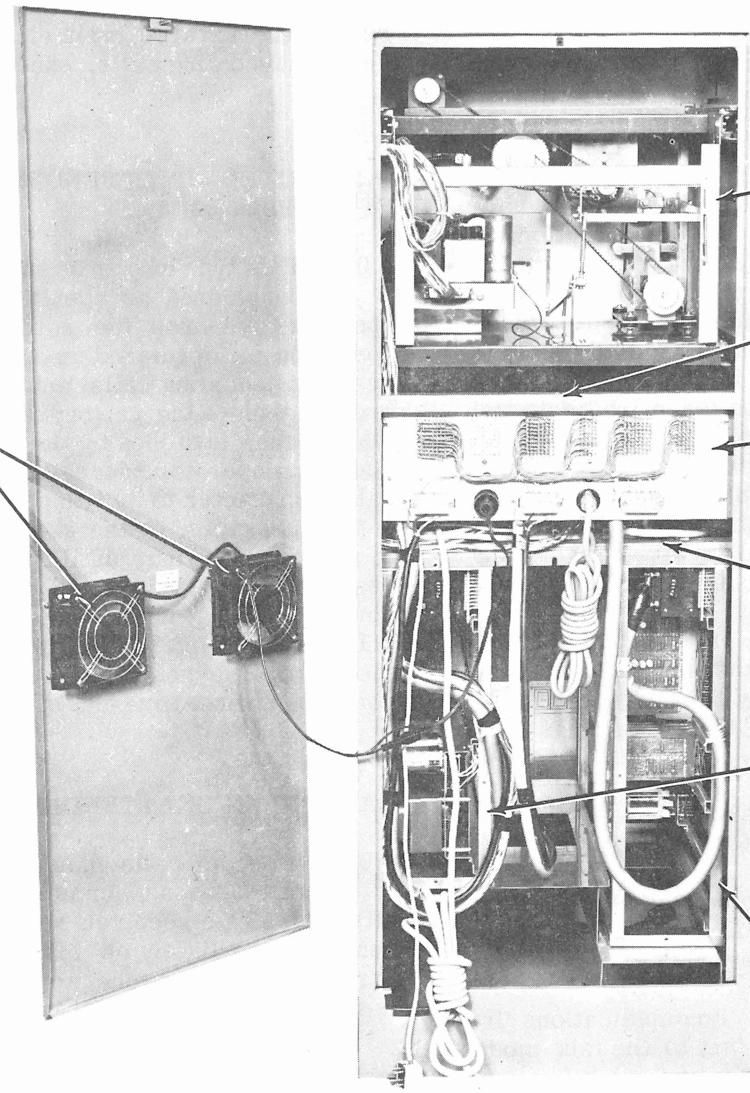

Figure 3 - Tape Sender 4A, Rear View

3.12 Indicator lamps, a PROGRAM TEST switch, and a READER TEST switch are located on the front panel of the EDC electronics module and may be used in troubleshooting.

3.13 The sender requires approximately 3 amperes at 117 v ac when it is operating.

3.14 A variable feature (TP308510) causes a vertical parity check bit to be generated for each character and transmitted in place of the unused 8th level of any 5, 6, or 7 level data.

3.15 A standard wiring option provides unattended service, permitting the sender to answer incoming calls automatically. This option may be either key-controlled only or key and tape out/alarm - controlled. In addition, an optional automatic disconnect can be provided in conjunction with the unattended service.

3.16 An optional feature (TP308513) is the protected unattended transmitter recognizer unit. This unit permits the sender to answer incoming calls automatically if tape is in the reader and no alarm is present and to send the tape if the calling station is a properly authorized receiver. Optionally, the sender can answer all calls and return a no traffic signal if there is no tape to send.

4. METHOD OF OPERATION (Figure 4)

ATTENDED OPERATION

4.01 Prior to the start of transmission, the sending operator inserts tape in the reader and determines the mode of operation by depressing either the MANUAL button for normal EDC operation or the NON-EDC button for non-EDC operation. Either the sender or the receiver may initiate the call using normal dialing procedure. After voice communication is established, the operator at the called terminal first places his data set in the data mode; a lamp under the TALK button of the data set lights indicating the terminal is the called station. Upon hearing the 2025 Hz tone, the operator at the calling terminal places his data set in the data mode. At the sender, the reader motors turn on when the data set goes into the data mode and transmission begins shortly thereafter.

4.02 The operator at the sender may stop transmission at any time by depressing the STOP/ALARM-RESET button. At this time he may choose one of three courses of action:

(a) Resume transmission by resetting the STOP/ALARM-RESET button;

(b) Drop the call, if the sender is the calling terminal, by returning the data set to the talk mode and placing the handset on hook, or;

(c) Reestablish voice communications by returning the data set to the talk mode and waiting until the receiver operator returns to the talk mode. Data transmission may then be started again by returning to the data mode as outlined in 4.01 or the call may be dropped by placing the handset on hook.

UNATTENDED OPERATION

4.03 The operator prepares the sender for unattended operation by placing tape in the reader and depressing the UNATTEND button. For unattended non-EDC operation, the operator must depress both the NON-EDC and UNATTEND buttons simultaneously. The set then answers incoming calls automatically and begins transmission when the receiving terminal is ready to accept traffic. Transmission continues until the end of the tape is reached. When the automatic disconnect feature is provided, the data set drops the call after 60 seconds by either the tape out alarm condition or by the loss of the reverse channel. The sender then ignores incoming calls, except as described in 3.10.

PROTECTED UNATTENDED TRANSMITTER OPERATION

4.04 This type of operation is optional and not considered as standard operation. The operator prepares the sender for unattended operation as described in 4.03. The set then answers incoming calls automatically and returns a tone to the calling station. The calling station then switches to the data mode and the receiving operator causes a low speed identification character to be transmitted. Recognition of this character by the sender causes sending to start and continue until the end of the tape is reached. The sender then disconnects and ignores incoming calls, except as described in 3.10. If no identification character is sent or the wrong character is sent, the sender disconnects after a time-out of 60 seconds.

CALLING AN UNATTENDED RECEIVER

4.05 A sender calls an unattended receiver in the same manner as if the receiver were attended. The receiver returns a tone to the sender immediately on answering and is ready to receive when the tone stops. A receiver which is not able to receive will ignore incoming calls.

5. PRINCIPLES OF OPERATION

TRANSMISSION START

5.01 Prior to the start of transmission, the operator at the sender terminal turns power on, loads tape into the reader, and selects the mode of operation for the terminal.

5.02 When power is turned on, the terminal may operate for a short time. This action occurs while the programmer in the HSEDC transmitter control module resets the electronic logic.

5.03 A detailed description of the tape threading procedure is given in Part 6. A decal on the tape boat of the tape transport shows a detailed picture of the tape path. A summary of the threading procedure is given in 5.04.

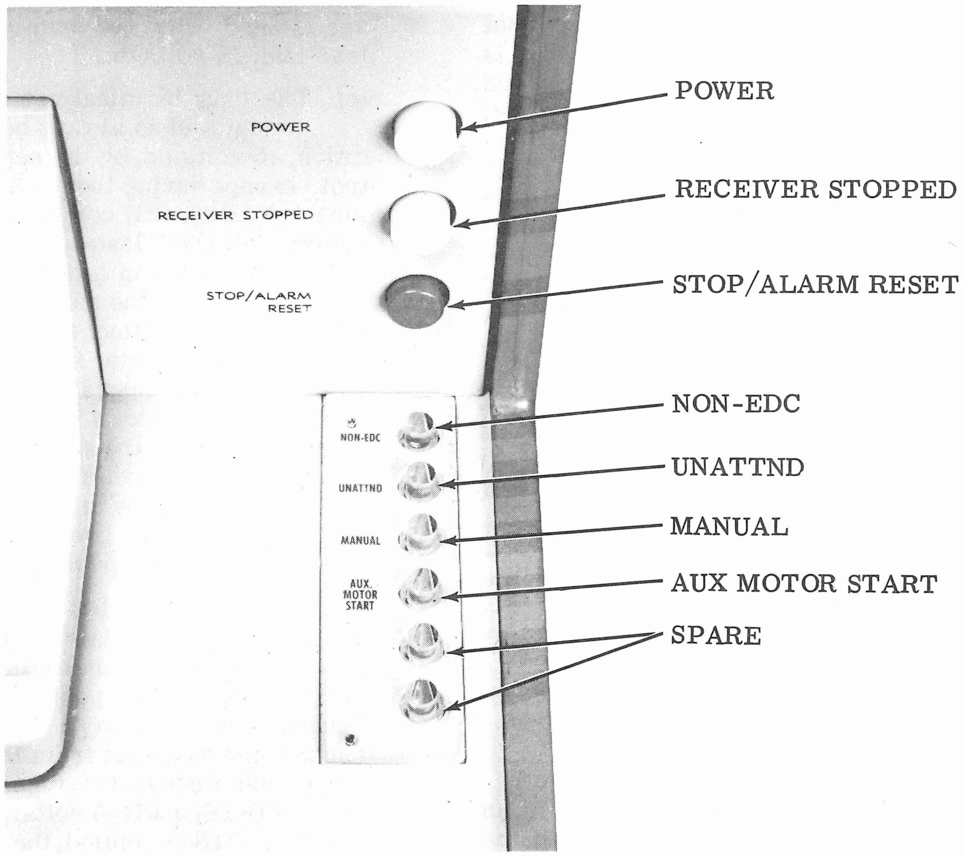

Figure 4 - Sender Operating Controls

5.04 Place the tape in the tape boat with the three-hole side (counting from the feed holes) closest to the panel and provide a leader of approximately nine feet for threading. Run the tape from the tape boat to the tape puller located in the upper right-hand corner of the panel and down to the reader, following the path shown on the decal. Load the tape into the reader. There should be at least 8 inches of meaningless information in the tape to the right of the reader since this information could be ignored if the sender terminal and the distant terminal have to synchronize themselves at the start of transmission. Run the tape from the reader through the yield arms and the second tape puller and start the tape in the take-up reel following the path shown on the decal. Any information in the tape between the reader and the take-up reel should be meaningless.

5.05 A set of pushbuttons located on the horizontal control panel of the sender terminal provides a means for selecting the mode of operation for the terminal. Two modes of operation are available: one mode provides the normal error detection and correction (EDC) feature and the other mode disables the EDC feature to provide a means for transmitting to a terminal not equipped with the EDC feature.

5.06 To select the EDC mode, the operator must depress the MANUAL button on the control panel. The button illuminates when this mode is selected.

5.07 To select the non-EDC mode, the operator must depress the NON-EDC button on the control panel. The NON-EDC and MANUAL buttons both illuminate when this mode is selected.

5.08 No signal lead is attached to the MANUAL pushbutton switch. A lead from a normally-open contact on the NON-EDC pushbutton switch goes to the HSEDC transmitter control module. When this lead is open, the terminal operates in the EDC mode. When this lead is closed to ground, the EDC feature is disabled and the terminal operates in the non-EDC mode.

5.09 The motors on the reader and tape transport assembly are turned off when there is no call in progress or when there is an alarm present. An AUX. MOTOR START button is provided to turn on the motors when desired. The button illuminates when it is pushed. A lead from a normally-open contact on this pushbutton switch supplies a ground connection to a motor start relay in the station control which supplies ac power to the motors.

5.10 A call is initiated between the sender and a distant terminal using normal dialing procedure. Either terminal may make the call. After voice communication is established, the operator at the called terminal places his data set in the data mode by depressing the DATA button. When the operator at the calling terminal hears a tone on the telephone line, he places his data set in the data mode by depressing the DATA button.

5.11 The sender station control provides an interface between the data set and the terminal equipment. The signals to and from the data set are EIA standard interface signals. The sender station control converts the EIA input and output signals as explained in 5.12. The EIA signal format is:

Data-Binary State	One	Zero
Data-Signal Condition	Marking	Spacing
Paper Tape	Hole	No Hole
Voltage	Negative	Positive
Control Function	OFF	ON

5.12 The signals also have the following electrical characteristics.

(a) The input control voltages do not exceed ±25 volts dc with respect to signal ground. Minimum acceptable voltages for control are ±3 volts dc. Signal conditions are not defined when the terminal voltages are in the range -3 to +3 volts dc. Maximum short circuit current between any two leads (including ground) does not exceed 1/2 ampere.

(b) The terminating impedance of an output signal has a dc resistance of not less than 3000 ohms and the voltage in open circuited condition does not exceed two volts. The effective loading capacitance does not exceed 2500 picofarads. When the effective load is 3000 ohms and the open circuit voltage is zero volts, the terminal voltage is not less than ±5 volts dc.

(c) The data terminal ready (DTR) lead to the data set is always held in the on condition, +6 volts dc, by the sender station control, except during the ringing cycle. When ring indication (RI) comes on, +6 volts dc, it causes the DTR lead to go off, -6 volts dc. DTR must be on in order for the data set to go in and stay in the data mode. Thus, if the sender is the calling station, ringing never occurs and the data set goes into the data mode when the operator pushes the DATA button. If the sender is the called terminal, ringing prevents the data set from entering the data mode. When the operator interrupts the ringing cycle by answering the call manually, the data set goes into the data mode when the operator pushes the DATA button.

(d) Approximately 100 ms after the data set goes into the data mode, the data set ready (DSR) lead from the data set will come on (+6 volts). The positive voltage on this lead operates a relay in the sender station control and a contact from this relay, through a gate and a converter, turns on the request-to-send (RTS) lead (+6 volts); 200 ms, ±50 ms, after the RTS is applied, the data set turns on the clear-to-send (CTS) lead. The RTS on causes a time-out to begin which puts a spacing tone on the line for 1 to 3 seconds.

5.13 The tape-out contact on the reader is brought to the sender station control. This contact closes to ground when there is no tape in the reader and the ground signal is applied to the station control to activate the TO relay.

5.14 The STOP/ALARM-RESET pushbutton on the cover panel of the cabinet is provided to manually stop and start the terminal once the terminal is in the data mode. A contact on the pushbutton causes two relays ST and HO to operate as a binary counter. If the relays are not operated, a momentary closure of the button operates the relays and produces the STOP/ALARM condition. If the relays are operated, a momentary closure causes the relays to drop out. A contact from the TO relay, which closes to ground when the relay is operated, pulls in the ST and HO relays and produces the STOP/ALARM condition.

5.15 The clear-to-send signal is combined with contacts off the TO relay, the DSR relay, and the ST and the HO relays to produce a start signal. Thus, when the data set is in the data mode, tape is available, no alarms are present, CTS is ON, and the 1 to 3 second time-out is completed, the start lead will be at 0 volts. If any of these conditions are not met, the start lead will be at -6 volts.

ADDITIONAL START FUNCTIONS

5.16 When DSR comes on and operates the DSR relay, a normally-open contact to ground operates the motor start (MS) relay to provide power to the tape handling motors and the reader motors.

5.17 At the end of the 1 to 3 second time-out, a gate in the sender station control is primed to allow the send data lead from the transmitter distributor module to pass through to the data set.

TRANSMISSION CHARACTERISTICS

A. Error Detection and Correction Operation

5.18 The HSEDC transmitter control module controls the operation of the sender terminal during transmission. The control functions are selected and performed by the programmer in the module. The programmer has eight modes; each mode determines the type of character to be transmitted and/or the type of action required. The programmer advances to each mode sequentially and in the following order: SR mode, BN mode, BK mode, EOB mode, CK1 mode, CK2 mode, R1 mode, R2 mode and back to the SR mode. If no errors are detected, a feedback circuit allows the programmer to reset to the BN mode from the CK2 mode. For a detailed description of the HSEDC transmitter control module, refer to Part 7. The transmitter distributor module converts the parallel character signal into a serial data signal for transmission over the telephone line and provides the internal timing for the terminal. For a detailed description of the transmitter distributor module, refer to Part 8. Figure 5 shows a simplified block diagram of the sender.

5.19 At the beginning of transmission, the programmer in the HSEDC transmitter control module is in the SR mode. The start lead from the sender station control comes into the module and is combined with the EDC-non-EDC lead from the NON-EDC pushbutton and a tape-out lead from the sender station control. The EDC-non-EDC lead and the tape-out lead are both open-circuited. The reverse channel lead from the sender station control is at 0 volts or off. These conditions cause a series of pulses to appear on the TD start lead. These pulses are positive going transitions, -6 volts to 0 volts, 10 microseconds wide, and spaced 40 milliseconds apart. Since the programmer is in the SR mode, the SR character is presented to the inputs of the shift register in the transmitter distributor module. Each pulse on the TD start lead will cause the transmitter distributor to cycle once. Half a bit after the start of the character cycle, a sample pulse is generated which inserts the SR character into the distributor shift register. The distributor then shifts the character out of the register bit by bit. The serialized character goes to the sender station control where it is converted to an EIA signal and presented to the data set and sent out over the line. The sample pulse is also presented to the HSEDC transmitter control module to sample the reverse channel. If the reverse channel is off, no action takes place and the next pulse on the TD start lead causes another SR character to be transmitted; as long as the reverse channel is off, these characters are sent continually. The sample pulses are positive going transitions, -6 volts to 0 volts, and 10 microseconds wide.

5.20 The SR character (see Table 2) is a fixed 8-level character which consists of a marking bit in the 1st, 5th, 6th, and 7th levels of the character and a spacing bit in the 2nd, 3rd, 4th, and 8th levels of the character.

5.21 The timing for the terminal is derived from a tuning fork oscillator (TP308512) located in the transmitter distributor module. The output of the tuning fork oscillator is a square wave with a period of 0.952 milliseconds. The negative transition of this signal is used to provide the bit timing. The positive transitions are used to provide character timing and to perform various functions within the terminal. These signals alternate between -6 volts and 0 volts. See the timing diagrams in Figures 6, 7, and 8.

5.22 When a pulse appears on the TD start lead, the distributor cycles once. The first negative transition on the transmit clock lead after the pulse occurs is used to reset the shift register. The following positive transition generates the sample pulse which inserts the character at the inputs of the shift register into

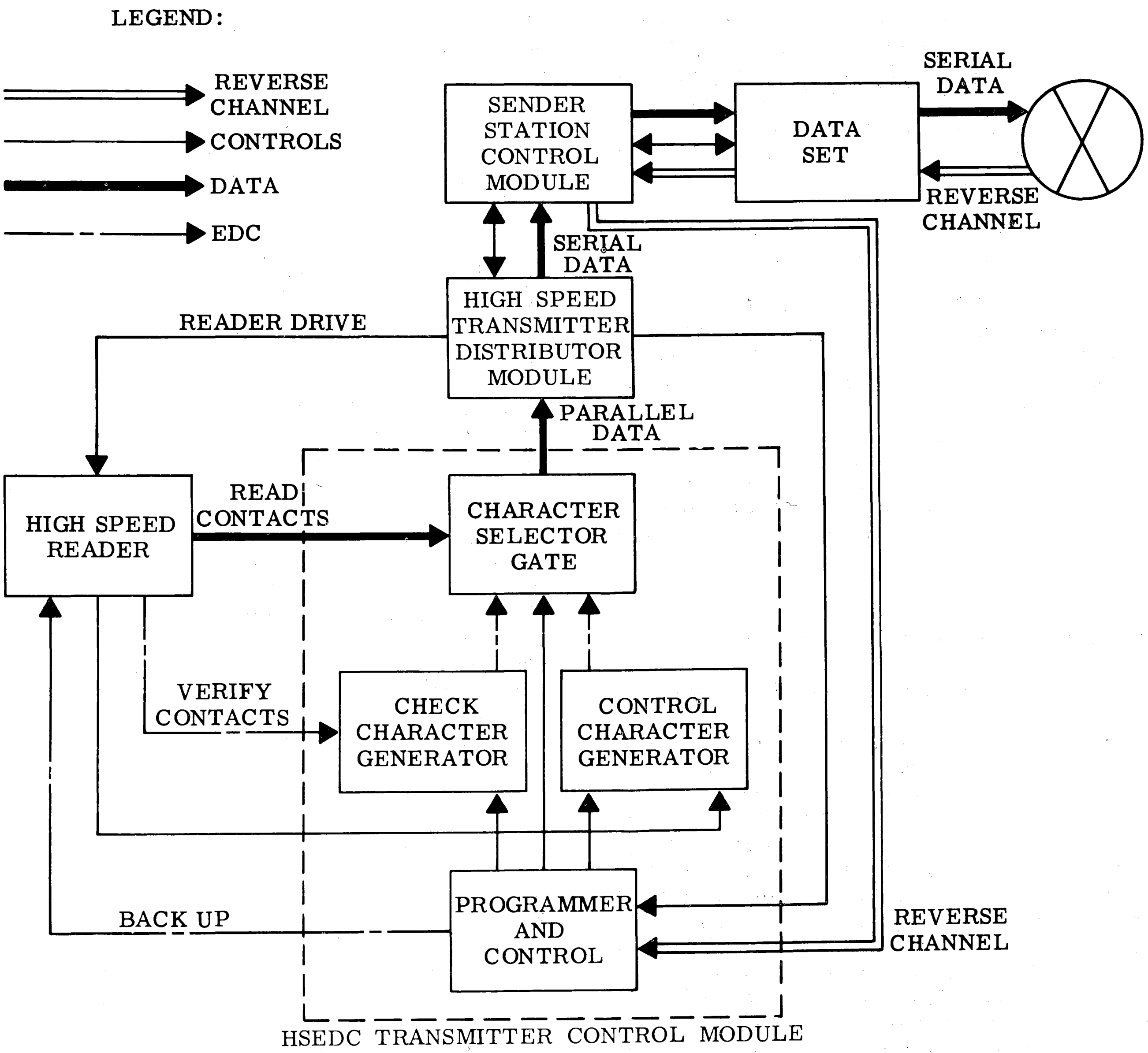

Figure 5 - Block Diagram of Tape Sender 4A

the shift register. The next nine negative transitions shift the character out of the shift register. The stop bit remains in the last element of the register and keeps a steady marking signal on the send data lead and stays in this state until another pulse appears on the TD start lead or until the TD start lead goes to 0 volts. A 0-volt signal on the TD start lead causes the distributor to cycle continuously and shift out characters on the send data lead, one after another.

5.23 A reader drive pulse is generated at the end of every character shifted out of the shift register and this pulse occurs half a bit after the start of the stop bit. The reader drive pulses go to the HSEDC transmitter control module where they are passed on to the reader

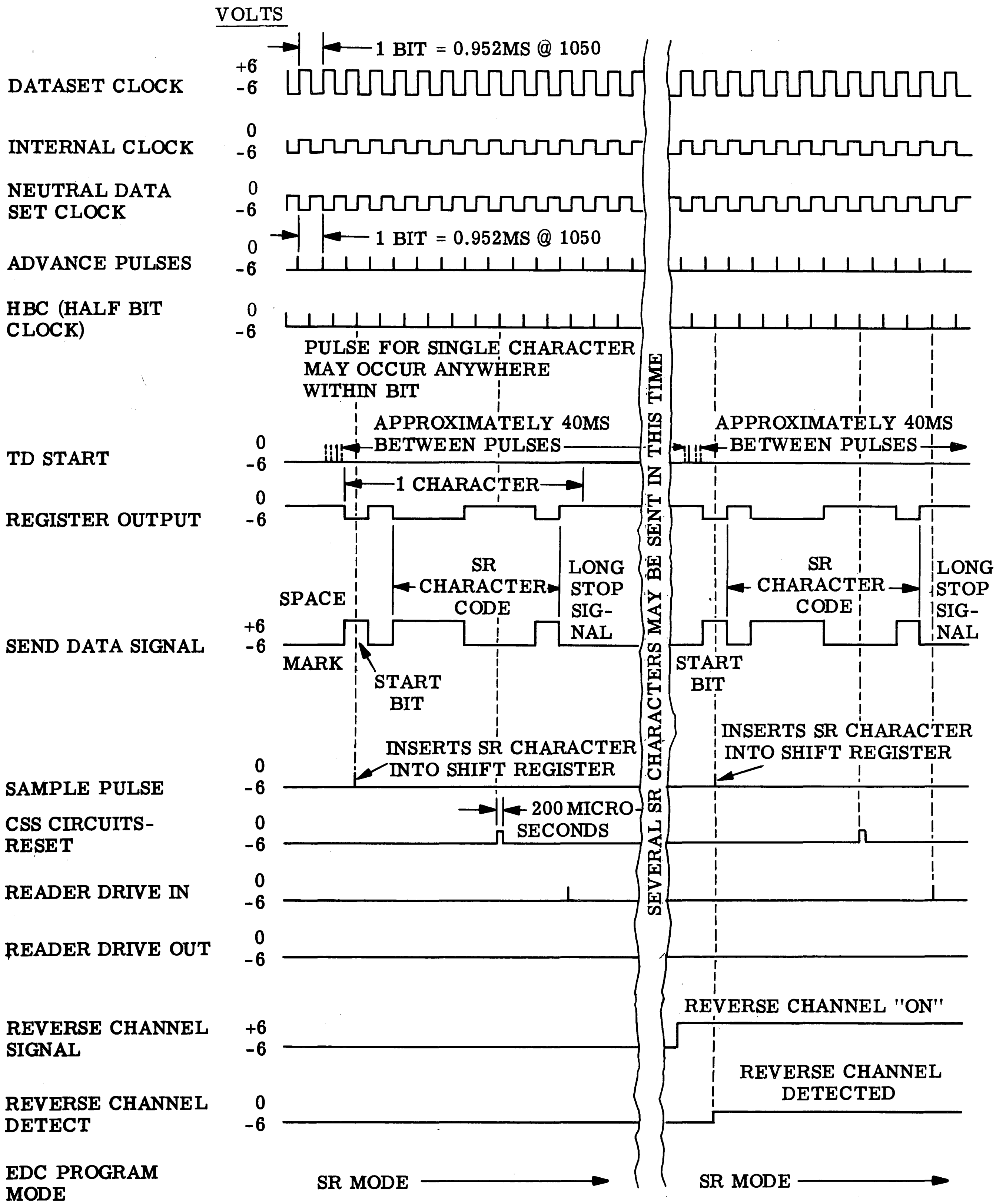

Figure 6 - Transmitter Distributor Timing - SR Character and Reverse Channel Detect

driver in the transmitter distributor and reader drive module to step the reader to the next character; the pulses are only passed by the HSEDC transmitter control module during the BK mode of the programmer. The reader drive pulses are positive going transitions, -6 volts to 0 volts, and 10 microseconds wide.

5.24 As long as the reverse channel is off, the sender terminal transmits an SR character every 40 milliseconds. When the receiver recognizes the SR characters, it turns on the reverse channel. When reverse channel comes on at the sender, the sender terminal transmits two more SR characters. The sample pulse from the first of these characters comes into the HSEDC transmitter control module and switches a flip-flop to indicate a reverse channel detected condition. This flip-flop then primes a gate which allows the sample pulse from the next SR character to come through and advance the programmer, 200 microseconds later, to the BN mode.

5.25 When the programmer advances to the BN mode, the TD start lead goes to 0 volts and remains at that potential. When the distributor finishes serializing and sending the last SR character, it immediately resets itself and samples and sends the next character at its inputs. The next character is one of three block numbers. The reader drive pulse generated at the end of the SR character is not passed by the HSEDC transmitter control module; see the timing diagram in Figure 7.

5.26 The three possible block numbers are fixed 8-level characters which consist of the following (refer to Table 2):

(a) BN1 — 1st, 3rd, 6th, and 8th levels marking and 2nd, 4th, 5th, and 7th levels spacing.

(b) BN2 — 2nd, 4th, 5th, and 7th levels marking and 1st, 3rd, 6th, and 8th levels spacing.

(c) BN3 — 1st, 2nd, 7th, and 8th levels marking and 3rd, 4th, 5th, and 6th levels spacing.

5.27 The block numbers are initially produced from a set of three contacts associated with a special cam on the reader. The gear makes one-third of a revolution for every 80 steps of the reader. Spaced 120^{o} apart on the gear are three detents. When one of the detents on the cam comes into position, the associated contact falls into it and makes a connection between a -6 volt bias supply and one of three inputs to the HSEDC transmitter control module. Each contact closure is centered about the end-of-block position which is described later. If the reader is stepping in the forward direction, the contacts make and break in such a way as to produce the following sequence of block numbers: BN1, BN2, BN3, BN1, BN2, BN3, BN1, etc. When the reader steps in the reverse direction, the sequence of block numbers is reversed: BN1, BN3, BN2, BN1, BN3, etc.

5.28 The block numbers are used to maintain block synchronization between the sender terminal and the receiver terminal. The receiver terminal looks at the transmitted block number and compares it to the block number it expects to receive. If the numbers agree, no error is recorded. If there is no agreement, an error is recorded with various actions occurring depending on the type of error recorded.

5.29 If a character other than one of the three fixed block numbers is received, an error is recorded and the reverse channel is turned off at the end of a block. The receiver punches whatever data comes in and then deletes this information from the tape. The sender does not detect the reverse channel off condition until the end of two blocks of 80 characters at which time it stops the reader, backs up the reader two blocks (160 characters), and starts again.

5.30 If a low block number is transmitted, that is, BN1 sent and BN2 expected, the receiver ignores the incoming data signals and keeps the reverse channel on until it is ready to receive the next block; it will still expect BN2. The sender has received no knowledge about the error and it continues into the next block, this time sending the correct block number, BN2.

5.31 If a high block number is received, that is, BN3 sent and BN2 expected, the receiver turns off the reverse channel immediately and deletes the information punched in the tape. The sender detects the reverse channel off condition at the end of block 3, backs up two blocks to the beginning of block 2, and then starts again.

5.32 Depending on the input primed by the contacts on the block number gear on the reader, the HSEDC transmitter control module presents one of the three block numbers to the

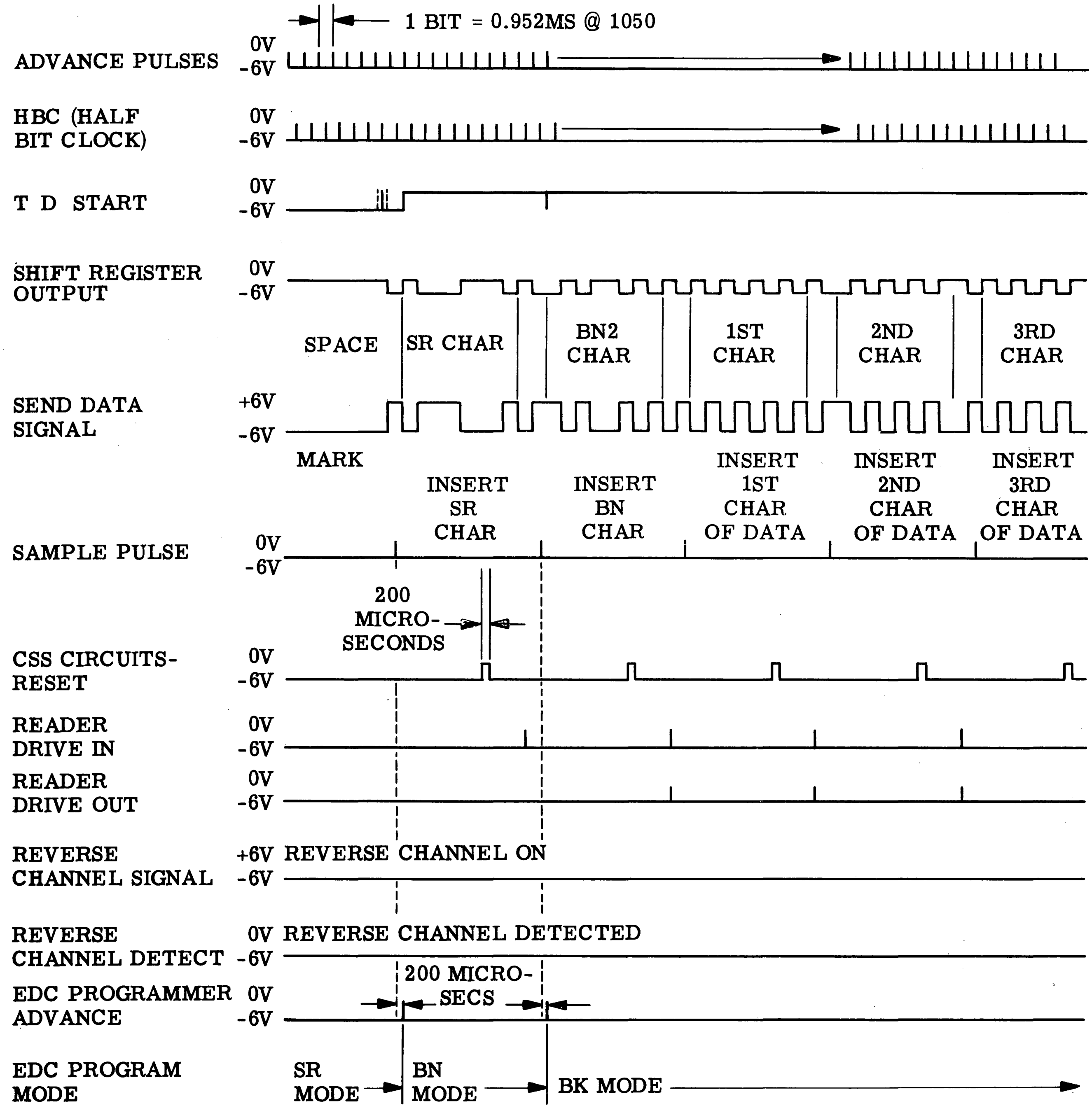

Figure 7 - Timing Diagram - Advance from SR to BN and BN to BK Modes

inputs of the distributor shift register. After the shift register has shifted the SR character out, it resets itself, sets in the block number at its inputs, and shifts out the block number as a serial character to be transmitted to the receiver terminal. The sample pulse which sets the block number into the shift register comes into the HSEDC transmitter control module and, 200 microseconds later, the programmer advances to the BK mode. The TD start lead remains at 0 volts.

5.33 Once the programmer is in the BK mode, the reader drive pulses generated at the end of the distributor character cycle are passed by the HSEDC transmitter control module to the driver and power supply in the sender tape transport assembly. See timing diagram in Figure 7.

5.34 Each pulse into the driver causes the reader to advance the tape one character. The first pulse accepted occurs at the end of the transmission of the BN character and, as long as the programmer is in the BK mode, each subsequent drive pulse from the distributor through the HSEDC transmitter control module causes the reader to advance the tape one character.

5.35 The reader has two sets of eight code-reading drag sense contacts. The first set of contacts that the tape sees as it moves in the forward direction, called the read contacts, is used to present the data characters to the inputs of the distributor to be serialized and then transmitted. The parallel characters go through the HSEDC transmitter control module first and are only presented to the distributor inputs when the programmer is in the BK mode. The second set of contacts, called the verify contacts, are spaced one character past the first set of contacts to read the tape a second time. The information read from the second set of contacts is used by the HSEDC transmitter control module to generate two redundancy characters. The generation of these characters is described in 5.41.

5.36 The data characters in the tape are read by the read contacts of the reader and transmitted in blocks of 80 characters during the BK mode of the programmer. These same characters are read a second time by the reader verify contacts to generate two redundancy characters, called CK1 (check character 1) and CK2 (check character 2), which are transmitted at the end of the 80-character block. The 80 characters are counted mechanically by a special gear on the reader. A contact associated with the gear determines the end of a block.

5.37 At the end of the transmission of the BN character, the distributor sets the first data character (character 1) from the read contacts into the shift register and then shifts the character out of the distributor for transmission over the line. The drive pulse generated at the end of BN character causes the reader to step the tape and move the first character (character 1) off the read contacts and move the second character (character 2) over the read contacts. The tape does not actually begin to move until character 1 is set into the distributor. After character 1 is transmitted, character 2 is set into the distributor and transmitted. The drive pulse generated at the end of character 1 now moves character 3 over the read contacts. At the end of the character 2, character 3 is set into the distributor and the drive pulse generated at the end of character 2 moves character 4 over the read contacts. This sequence continues until the first block of 80 characters is set into the distributor and transmitted over the line. Character 80 is moved off the read contacts and character 1 of the second block is now over the read contacts ready to be read when the next block is to be transmitted. See the timing diagram in Figure 7.

5.38 The reader contains a cam which mechanically counts 80 characters. The cam makes one revolution for every 80 steps of the reader. On the cam are two detents with a wire spring contact associated with each detent. One contact is used when the reader is going in the forward direction and the second contact is used for the reverse direction. As the detent in the cam comes into position, the contact falls into the detent and makes a connection to ground. The connection is brought to the HSEDC transmitter control module and is used to determine the end of an 80-character block. During the BK mode, only closures from the forward EOB (end-of-block) contact are recognized.

5.39 Throughout the transmission of the 80-character block, the HSEDC transmitter control module samples the forward EOB contact during each character cycle. The sample pulse from the transmitter distributor module is used to sample the contact. The sample pulses from the 1st character through the 78th character of the block find the EOB contact open and no output is produced. At the end of the 78th character, the distributor sets the 79th character

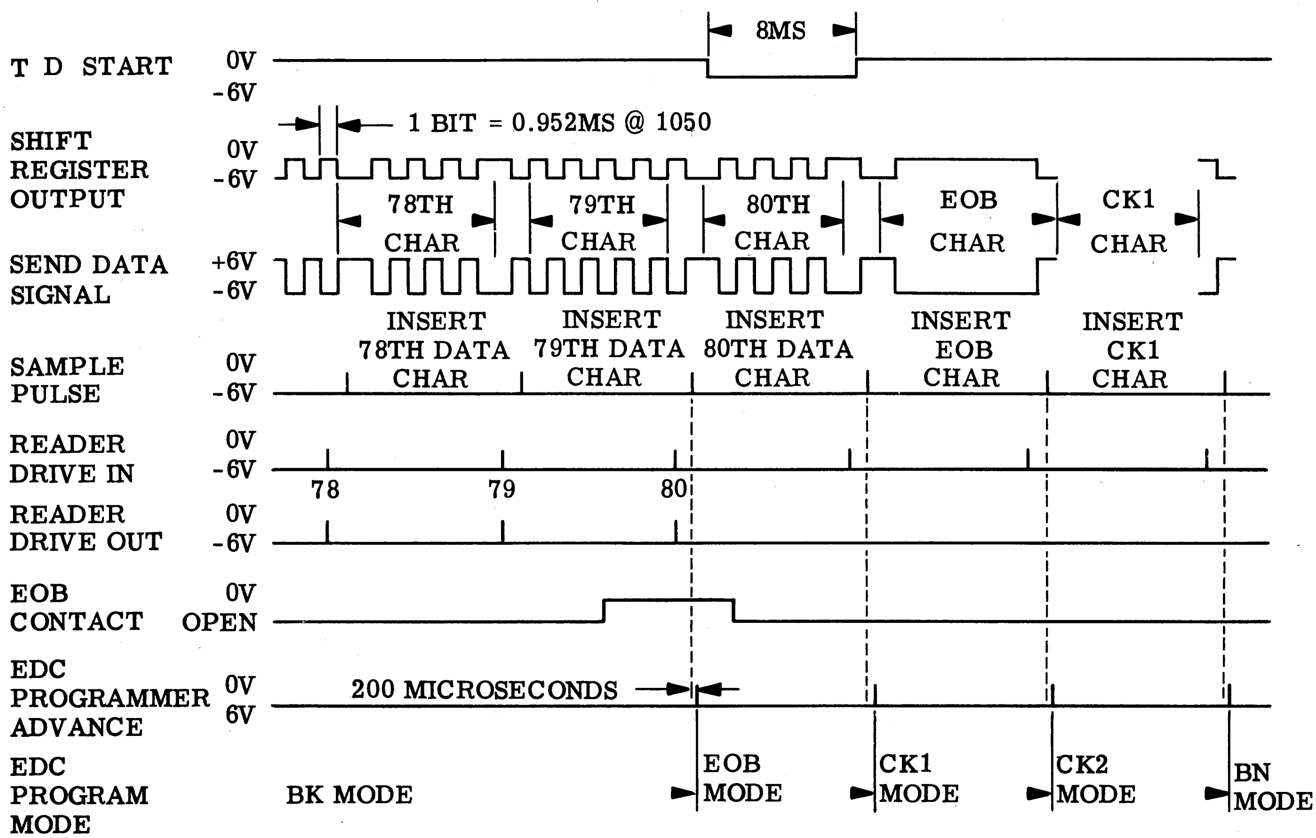

Figure 8 - EOB Contact Sampling and Mode Delay Timing (1050 WPM)

into the shift register. The sample pulse from the 79th character also finds the EOB contact open. During the 79th character, the reader has moved the 80th character over the read contacts due to the drive pulse generated at the end of the 78th character. When the 80th character is over the read contacts, the forward EOB contact is closed. The distributor sets the 80th character into the shift register. The sample pulse from the 80th character finds the forward EOB contact closed and the output produced causes the programmer to advance out of the BK mode and into the EOB mode. During the transmission of the 80th character, the drive pulse from the 79th character causes the reader to move the 80th character off the read contacts onto the verify contacts and the forward EOB contact opens. The drive pulse generated at the end of the 80th character is inhibited by the HSEDC transmitter control module from stepping the reader. See the timing diagram in Figure 8.

5.40 When 7-level tape is being read and transmitted, the 8th level of each character in the 80-character block is always read as a mark. When 6-level tape is being read and transmitted, the 7th and 8th levels of each character in the 80-character block are always read as marks. When 5-level tape is being read and transmitted, the 1st level of each character in the 80-character block is always read as a space and the 7th and 8th levels of each character are always read as marks.

5.41 The programmer advances to the EOB mode 200 microseconds after the sample pulse from the 80th character of the data block. A delay in the HSEDC transmitter control module causes the TD start lead to go to -6 volts for approximately 6-8 milliseconds. At the end of the delay, the TD start lead returns to 0 volts. The delay is not significant and the transmitter distributor finishes sending out the 80th character. By the time the end of the character is reached, the delay is completed, the TD start lead will be at 0 volts and the transmitter distributor immediately resets and inserts the EOB character presented by the HSEDC transmitter control module into the shift register. The delay is required to allow the punch at the receiving terminal to advance the last character punched to a position over the photoreader for reading when generating the check characters at that terminal. After the TD start lead has gone to 0 volts, the transmitter distributor resets and inserts the EOB character into the shift register. The sample pulse which sets the EOB character into the shift register comes into the HSEDC transmitter control module to advance the programmer to the CK1 mode. After the EOB character is sent, the distributor inserts the first check character (CK1) into the shift register. The sample pulse from CK1 comes into the HSEDC transmitter control module to advance the programmer to the CK2 mode. At the end of the transmission of CK1, the second check character (CK2) is inserted into the distributor shift register and sent out. When the programmer advances to the CK1 mode, a pulse is generated which samples the reverse channel. If the reverse channel is on when it is sampled, the HSEDC transmitter control module does not initiate an error correction sequence. The sample pulse which sets CK2 into the shift register comes into the HSEDC transmitter control module and resets the programmer to the BN mode. At the conclusion of the transmission of CK2, the next block of 80 characters is sent, preceded by the appropriate block number and followed by the EOB character and the two check characters. As long as no errors are detected by the receiver terminal and the reverse channel does not go off, the data information will continue to be sent in blocks of 80 characters in the manner described above. The reader drive pulses generated during the transmission of the EOB character and the two check characters are inhibited by the HSEDC transmitter control module from stepping the reader. See the timing diagram in Figure 8.

5.42 The EOB character is a fixed 8-level character with a spacing bit in the 1st level and marking bits in the 2nd, 3rd, 4th, 5th, 6th, 7th, and 8th levels of the character (refer to Table 2).

5.43 The two check characters (CK1 and CK2) are generated during the BK mode from the data information read by the verify contacts of the reader. The verify characters are set into two storage registers in the HSEDC transmitter control module. One storage register is used to generate CK1 and the other is used to generate CK2. These check character generators essentially add the 80 characters of a block together to produce the two check characters. The two check characters are then set into the distributor shift register to be transmitted during the CK1 mode and the CK2 mode.

5.44 The two check character generators are reset when the programmer advances to the BK mode. The sample pulse is used to set the verify character in each check character generator. The sample pulse is inhibited until the reader has moved character 1 of the block from the read contacts of the reader to the verify contacts. Thus, character 1 is set into the check character generators at the same time that character 2 is set into the distributor shift register. This sequence continues until the programmer advances out of the EOB mode. Character 80 is set into the check character generators at the same time that the EOB character is set into the distributor shift register.

5.45 Check character 1 (CK1) is derived from a horizontal parity check of the 80-character block. Each level of CK1 is derived by summing the marks in the appropriate level of each of the 80 characters in a block. If the sum of the marks for a level is an even number, that level is transmitted as a mark in CK1. If the sum of the marks for a level is an odd number, that level will be transmitted as a space in CK1.

5.46 Check character 2 (CK2) is derived from a spiral parity check of the 80-character block. Each level of CK2 is derived by summing the number of mark bits that occur along a spiral pattern in the block of 80 characters. An even number of marking bits produces a mark for the check character level. An odd number of marking bits produces a space for the check character level. Table 1 provides a means to determine which level of each character is used to derive a specific check character level. The lower section of the table shows the 80-character block. The upper section of the table indicates which level of each character is to be used, the particular line being chosen to correspond to the check character level being generated. As an example, if the bit for the 4th level of CK2 is being generated, the level line begins with a 4. Read down the table to see which characters will have the 4th level used in the sum. The 4th level is used from characters 1, 9, 17, 25, etc. Similarly, the 5th level of characters 2, 10, 18, 26, etc, is used, the 6th level of characters 3, 11, 19, 27, etc, is used and so on.

5.47 When the two check characters (CK1 and CK2) are derived from 7-level tape, the 8th level of each character read by the verify contacts is always read as a mark. When the check characters are derived from 6-level tape, the 7th and 8th levels of each character read by the verify contacts are always read as marks. When the check characters are derived from 5-level tape, the 1st level of each character read by the verify contacts is always read as a space and the 7th and 8th levels are always read as marks.

5.48 The sender is told an error has been detected at the receiving terminal by the removal of the reverse channel. Since the receiver does not detect the error and turn off the reverse channel until after the two check characters are sent, the sender will not detect the reverse channel off condition until the end of the block following the errored block.

5.49 The reverse channel is detected as being off during the EOB mode. The programmer advances from the EOB mode to the CK1 mode and from the CK1 mode to the CK2 mode. The distributor serializes the two check characters for transmission, although the output of the distributor is prevented from reaching the data set. Instead, a continuous marking signal is presented to the data set for transmission over the line at the end of the transmission of the EOB character.

5.50 The sample pulse from the distributor which would normally come into the HSEDC transmitter control module to reset the programmer to the BN mode instead advances the programmer from the CK2 mode to the R1 mode. Once the programmer is in the R1 mode, a reader reverse lead from the HSEDC transmitter control module goes to 0 volts and actuates the motor reverse relay in the sender station control causing the reader to reverse direction. A signal from the motor reverse relay comes into the HSEDC transmitter control module and controls a relay which now allows the reverse EOB contact to be sampled for the end-of-block position. A contact off this relay causes an oscillator to turn on which provides the pulses required to step the reader in the reverse direction.

5.51 The reader drive pulses continually sample the reverse EOB contact. After the 79th step backwards, the reverse EOB contact closes and the 80th drive pulse comes through and advances the programmer to the R2 mode. The 80th step of the reader causes the reverse EOB contact to open. In the R2 mode, the drive pulses continue to step the reader backwards. After the 79th step backwards through the second block, the reverse EOB contact closes again and the 80th drive pulse comes through and resets the programmer to the SR mode. Once in the SR mode, the reader reverse lead goes back to -6 volts which de-energizes the motor reverse relay and the reader reverses back to the forward direction. The relay in the HSEDC transmitter control module which selects the proper EOB contact switches back to accept the forward EOB contact. During the two-block backup, the BN cam on the reader rotates in the reverse direction, decreasing the block number by two numbers. During the two-block backup, the sender keeps a steady marking signal on the telephone line.

5.52 When the programmer goes back to the SR mode, the sender begins sending the SR characters. During the reverse modes (R1 and R2) the tape in the reader was backed up to the start of the block in which the error occurred. The SR characters indicate that the sender is ready to resume transmission and retransmit the errored data. When the receiving terminal recognizes the SR characters, it turns on the reverse channel indicating it is ready to accept the retransmitted block. The sender detects a reverse channel on condition and transmits the 80-character block. It continues to transmit the data in blocks of 80 characters, correcting any errors that occur by backing up the tape and retransmitting the block that contains the error.

B. Non-Error Detection and Correction Operation

5.53 The sender is capable of operating with the error detection and correction (EDC) feature disabled for transmission to remote terminals without the EDC feature. Non-EDC operation is selected with the NON-EDC pushbutton on the sender control panel. When the button is pushed, the terminal is primed to operate in the non-EDC mode. The reverse channel feature provided by the data sets is required for non-EDC operation. However, if the feature is not available, a switch on the HSEDC transmitter distributor module simulates the reverse channel to allow the sender to transmit the data tape. If this method is used, the remote terminal will be unable to control the startup and stopping of the sender.

5.54 A call is established and the terminal is prepared for data transmission in the manner described in 5.01. The terminal is ready to transmit when the start lead from the sender station control to the HSEDC transmitter control module goes to 0 volts. With the NON-EDC button pushed, the EDC/non-EDC lead into the HSEDC transmitter control module is at 0 volts. If there is tape in the reader, the tape-out lead is open-circuited.

5.55 With the sender terminal in the non-EDC mode, the programmer in the HSEDC transmitter control module will be locked in the SR mode, although SR characters are inhibited from being transmitted. When the reverse channel comes on, the BK mode lead from the programmer is primed which causes the TD start lead to go to 0 volts. The TD start lead on causes the transmitter distributor to continuously run through its character serialization cycle. With the BK mode lead on, the data characters read by the read contacts of the reader are presented to the inputs of the transmitter distributor.

5.56 The data in the tape is read character by character. The first transition on the timing lead resets the distributor shift register and samples the character read by reader contacts. The distributor serializes the character but the output of the shift register is prevented from reaching the data set for transmission. At the end of the character cycle, a reader drive pulse is generated which causes the reader to advance one character. The tape in the reader does not actually begin to move until after the start of the next character cycle.

5.57 After the reader drive pulse is detected, the next sample pulse unblinds the distributor output. At the end of the character cycle, the distributor is reset and the first character is again inserted into the shift register. The character is serialized and transmitted over the line. During this cycle the reader advances one character and the second character is ready to be read. At the end of serializing character 1, character 2 is inserted into the shift register. The drive pulse generated at the end of the character 1 cycle causes the reader to move character 3 over the read contacts during character 2's cycle. Transmission continues in this manner until the end of message or until the sender is told to stop.

C. Stopping Transmission

5.58 The sender terminal can be stopped in three different ways: automatically by the remote terminal, manually by the action of the operator at the sender terminal, or automatically if alarms are present in the sender terminal.

5.59 The remote terminal can stop the sender by removing the reverse channel. In the EDC mode, the reverse channel off condition causes the sender to stop at the end of the block and then back up the reader two blocks. At the end of the back-up, the sender stops and begins sending SR characters. In the non-EDC mode, the sender stops as soon as the reverse channel is detected as being off. No data is transmitted until the remote terminal turns the reverse channel on again. With the reverse channel off, the RECEIVER STOPPED indicator light on the sender front panel lights, indicating the operator at the remote terminal wishes to communicate to the sender operator over the telephone channel. The sender operator can establish voice communication by lifting the data set handset, pushing the TALK button on the data set, and waiting until the remote terminal's operator comes on the line. To reestablish data communication, the operator at the called station places his data set in the data mode by depressing the DATA button. When the operator at the calling station hears a tone on the telephone line, he places his data set in the data mode by depressing the DATA button.

5.60 The sender operator can manually stop the sender in two ways. The primary means of manually stopping the sender is to depress the STOP/ALARM-RESET button which pulls in the ST and HO relays in the sender station control and causes the start lead to go from 0 volts to -6 volts. This essentially inserts an error into the 80-character block being transmitted and inhibits the reverse channel signal. The STOP/ALARM-RESET button lights to indicate the presence of the error and the subsequent alarm. At the end of the block, the reverse channel is detected as off and the reader stops and starts to back up. Since the sender stopped at the end of the block in which the error was inserted, the reader need only back up one block. At the end of the one-block backup, the programmer in the HSEDC transmitter control module is reset to the SR mode and the sender stops. The sender operator can now go to the talk mode of the data set by lifting the handset and pushing the TALK button. The second means of stopping the sender manually is to place the data set in the talk mode directly. This causes the DSR relay in the sender station control to drop out and the start lead to go to -6 volts. With the start lead at -6 volts, the sender stops the reader at the end of the block, backs up the reader one block and then stops. In the non-EDC mode, either of the above actions stops the sender immediately and no reader backup occurs. Data communication can begin again by returning the data set to the data mode. If the sender was stopped by use of the STOP/ALARM-RESET button only, transmission can be resumed by resetting the button.

5.61 The sender stops automatically if an alarm condition occurs in the terminal. The two alarm conditions recognized are tape-out and no tape-motion detected.

5.62 The tape-out condition is detected through the tape-out contact on the reader. With no tape in the reader, the contact closes to 0 volts. The 0-volt signal operates the TO relay in the sender station control and a 0-volt signal off a contact on the TO relay comes into the HSEDC transmitter control module to indicate the tape-out condition. The sender continues to the end of the block in which the tape-out condition occurred and then stops. The programmer is reset to the SR mode and no back up of the reader occurs. The tape-out condition also causes the start lead to go to -6 volts and causes the ST and HO relays to operate. The STOP/ALARM-RESET button lights to indicate the alarm condition. In the non-EDC mode, the sender stops as soon as the tape-out condition is detected. To start again, tape must be loaded into the reader and then the STOP/ALARM-RESET button reset.

5.63 A circuit in the HSEDC transmitter control module is used to detect tape motion. If the paper tape in the reader has a section with torn feed holes, no transitions will occur on the lead from the reader feed detect contact and the tape-motion detect circuit produces a 0-volt signal which drives the TO relay in the sender station control and the terminal reacts in the manner outlined for the tape-out alarm condition.

5.64 During the time the sender is stopped because of a tape-out or no-tape motion detected condition or because of a stop due to the operator manually introducing an alarm with the STOP/ALARM-RESET button, the sender keeps a steady marking signal on the data communications channel.

5.65 If the sender is the calling station, the sender operator can drop the call at any time by returning the data set to the talk mode and lifting the handset and placing the handset on hook. If the sender is the called station, the operator can only return the data set to the talk mode and wait until the operator at the remote station returns to the talk mode and drops the call at which time the sender operator can hang up.

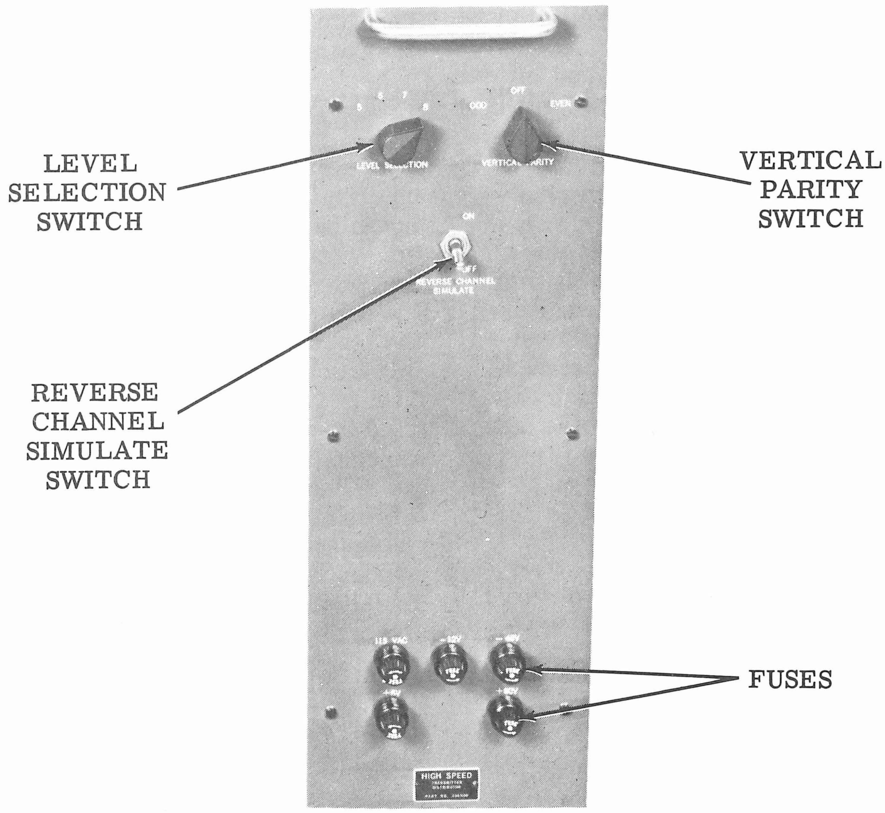

Figure 9 - High Speed Transmitter Distributor, Module C, Front View

D. Options and Features

5.66 Unattended Answering: A button labeled UNATTND is always provided on the control panel. It is intended for use when the unattended answering feature is provided with the terminal. The feature may be either key-controlled only or key and tape-out-controlled by the selection of the proper option.

5.67 When option A1 in the sender station control is selected, the unattended answering feature is key-controlled only. This option allows a ground signal to come through to the sender station control when the UNATTND button is pushed to pull in the UA relay. A contact from the UA relay then breaks the ring indicator lead, preventing it from inhibiting the data terminal ready lead. With the DTR lead on during the ringing cycle, the terminal answers the incoming call automatically and the data set goes into the data mode. Operation of the terminal proceeds as described in 5.12(c). An additional contact from the UA relay causes the UNATTND button to light.

5.68 Option A2 in the sender station control provides unattended answering that is key and tape-out controlled. The UA relay pulls in when the UNATTND button is pushed. The contact from the UA relay opens the connection between the ring indicator lead and DTR lead but the A2 option provides an alternative path if the TO relay is pulled in. The terminal only answers automatically if the UNATTND button is pushed and there is tape in the reader; the UNATTND button illuminates if these conditions are met.

5.69 Automatic Disconnect: In conjunction with the unattended answering option, an automatic disconnect is provided. It requires the addition of a DT plug-in relay to the sender station control. If the terminal is operating in the unattended mode and the tape-out condition occurs at the reader or the reverse channel is lost for more than a minute, the DT (disconnect) relay pulls in after a 60-second delay. A contact from the DT relay turns off the DTR lead and the data set automatically drops the call.

5.70 The protected unattended transmitter recognizer feature unit is an accessory used to prevent a sender from transmitting to an unauthorized receiver and is used in conjunction with the unattended answering option. The data set answers the call if there is tape in the reader but the recognizer unit prevents RTS from coming on and monitors the received data lead for a coded signal. If the received signal is the correct signal, the recognizer unit relinquishes control of the terminal, turns on RTS, and transmission begins. If the received signal is not the proper signal, the recognizer unit initiates a disconnect, within 60 seconds.

5.71 The option is available, by the addition of a circuit card to the transmitter distributor module, to generate a vertical parity bit for each character and to transmit that bit in place of the unused eighth level of any 5, 6, or 7-level data. Odd or even parity can be chosen or the vertical parity option can be disabled with a switch (Figure 9) on the transmitter distributor module.

E. Troubleshooting Features

5.72 Several switches and indicator lights are available in the terminal for testing and troubleshooting purposes.

5.73 A TEST/OPERATE switch (Figure 10) on the sender station control is used to operate the terminal when no data set is provided. The normal position of this switch is OPERATE. When the switch is placed in the TEST position, the DSR relay is energized and the CTS lead is locked in the on position. This prepares the terminal for operation, although some means must now be used to simulate the reverse channel. A switch (Figure 10) on the HSEDC transmitter control module, REVERSE CHANNEL SIMULATE, performs this function.

5.74 Switches are available on the front of the HSEDC transmitter control module (Figure 11) to provide a means of testing the EDC program and to test the reader. When the PROGRAM TEST switch is placed in the ON position, the EDC program can only be advanced to each successive mode through the action of the PROGRAM ADVANCE pushbutton switch. The READER TEST switch provides a means of checking the reading ability of the two sets of code-reading contacts on the reader. In normal operation, only the verify set presents characters to the check character generators. In the TEST position of the READER TEST switch, the characters presented by the read contacts are also inserted into the check character generators. The first sample pulse that occurs after the program is set to the BK mode is ignored; and 200 microseconds after the sample pulse, a pulse is derived to sample the cumulative output of the horizontal check character generator. All the elements of the generator should be in the 0 state. One millisecond after the sample pulse, another pulse is derived to set the character which is over the read contacts into the horizontal check character generator. The reader advances the tape one character and the next sample pulse inserts the character which is over the verify contacts into the horizontal check character generator. If the characters read off both sets of contacts are the same, all the elements in the check character generator are reset to the 0 state. The pulse 200 microseconds after the sample pulse which checks the outputs of the generator finds no element in the 1 state and no error is recorded. This procedure continues for the remainder of the eighty-character block and the programmer cycles through its normal sequence with no error detected. When the programmer again advances to the BK mode, it continues to read a character and then verify that same character as already described. If the characters read by both sets of contacts are not the same, at least one element of the horizontal check character generator is not reset to the 0 state and the pulse which samples the outputs sets a flip-flop to record the error. At the end of the block, the reader stops and backs up two blocks. The error causes the RTA lamp on the HSEDC transmitter control module to light. To restart, the READER TEST switch must be placed in the OFF position and then in the ON position again.

5.75 Indicator lights are mounted on the front plate of the HSEDC transmitter control module to show the state of various portions of the EDC logic.

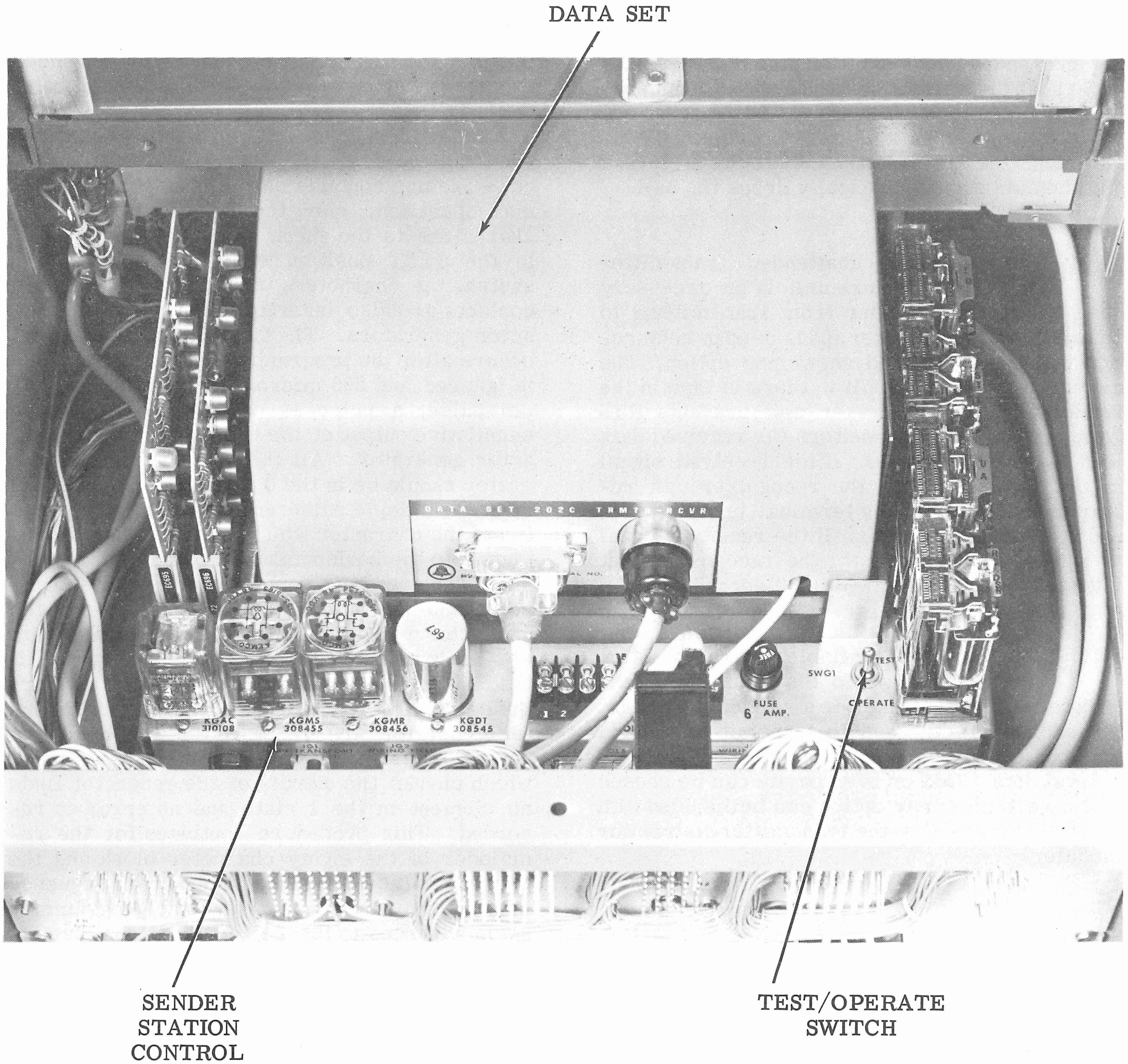

Figure 10 - Sender Station Control, Module G, Top-Rear View

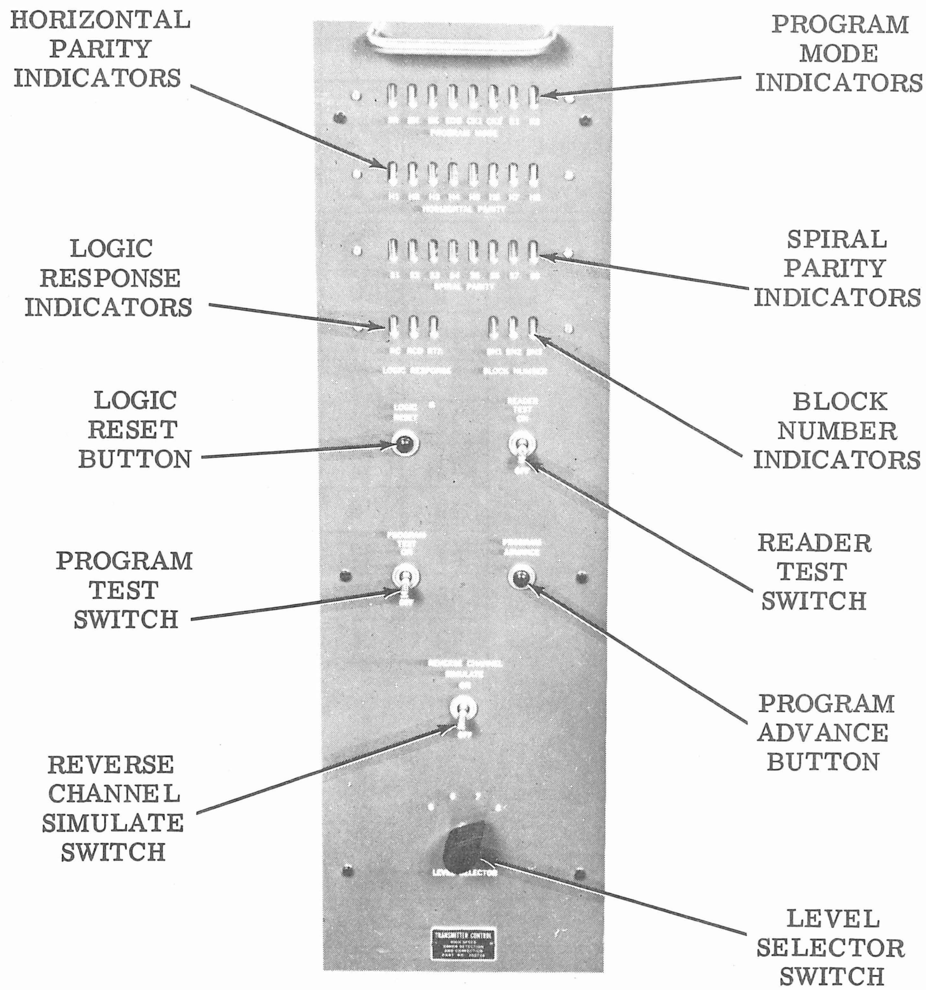

Figure 11 - HSEDC Transmitter Control, Module A, Front View

TABLE 1. CHECK CHARACTER (CK2) GENERATION

		Block Character Level							
CK2 Level (Check Character Level)	1st Level	1	2	3	4	5	6	7	8
	2nd Level	2	3	4	5	6	7	8	1
	3rd Level	3	4	5	6	7	8	1	2
	4th Level	4	5	6	7	8	1	2	3
	5th Level	5	6	7	8	1	2	3	4
	6th Level	6	7	8	1	2	3	4	5
	7th Level	7	8	1	2	3	4	5	6
	8th Level	8	1	2	3	4	5	6	7
Character Number (80-Character Block)		1	2	3	4	5	6	7	8
		9	10	11	12	13	14	15	16
		17	18	19	20	21	22	23	24
		25	26	27	28	29	30	31	32
		33	34	35	36	37	38	39	40
		41	42	43	44	45	46	47	48
		49	50	51	52	53	54	55	56
		57	58	59	60	61	62	63	64
		65	66	67	68	69	70	71	72
		73	74	75	76	77	78	79	80

TABLE 2. HSEDC CONTROL CHARACTERS

Character	Input	Outputs							
		Level 1	Level 2	Level 3	Level 4	Level 5	Level 6	Level 7	Level 8
	Pin No.	26	25	24	23	20	19	18	17
SR	7	Mark	Space	Space	Space	Mark	Mark	Mark	Space
BN1	15	Mark	Space	Mark	Space	Space	Mark	Space	Mark
BN2	21	Space	Mark	Space	Mark	Mark	Space	Mark	Space
BN3	28	Mark	Mark	Space	Space	Space	Space	Mark	Mark
EOB	35	Space	Mark	Mark	Mark	Mark	Mark	Mark	Mark

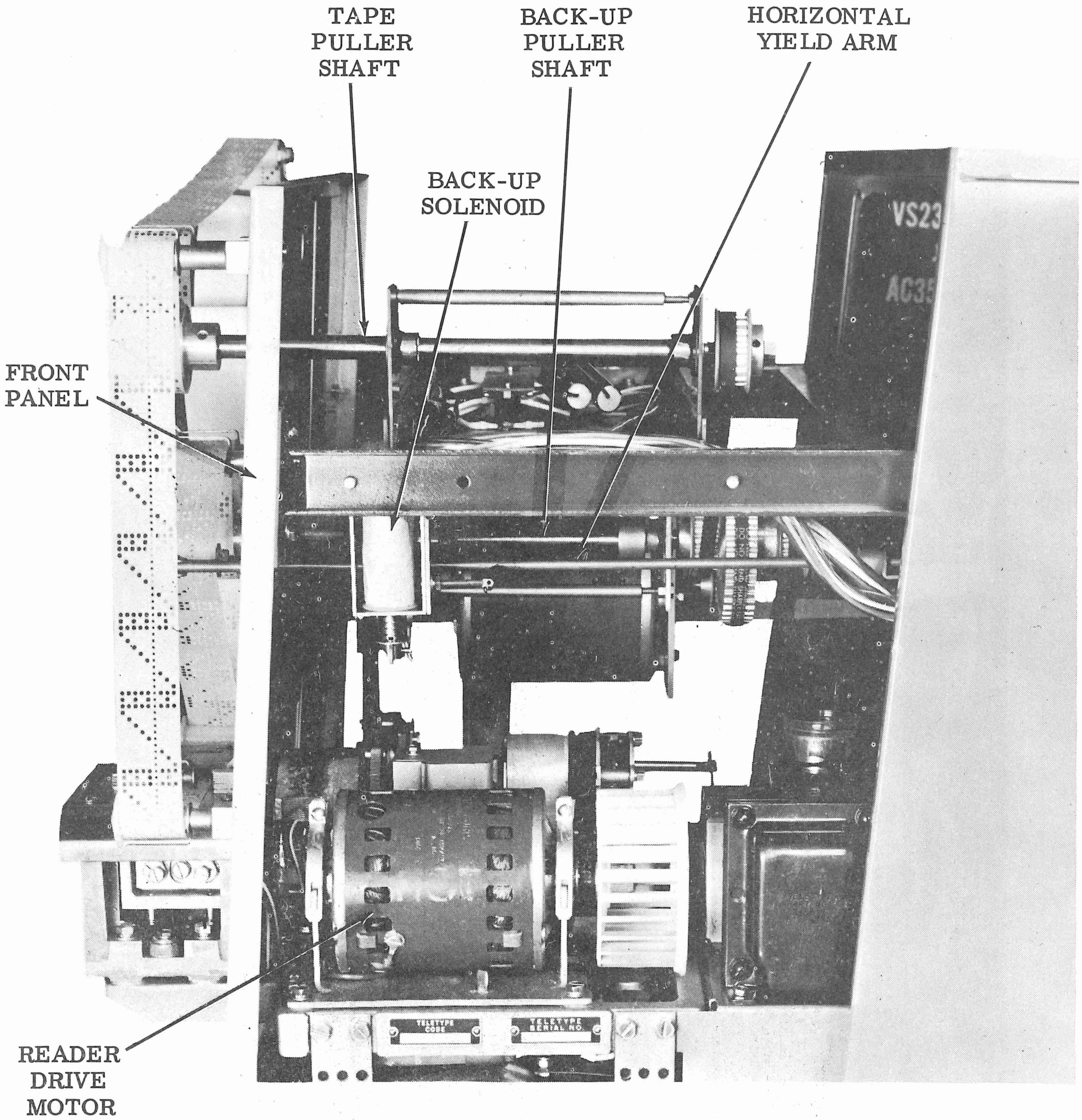

Figure 12 - Reader and Tape Transport Assembly, Right Side View

6. READER AND TAPE TRANSPORT ASSEMBLY

DESCRIPTION

6.01 The upper portion of the sender (Figures 12 and 13) houses the high speed tape reader and provides the necessary tape handling facilities. The tape transport components and reader are mounted on a slide-mounted panel 19-3/8 inches wide and 18 inches high.

6.02 The reader mounts on the transport assembly through vibration isolators. The reader protrudes through the panel and is covered by a removable cover.

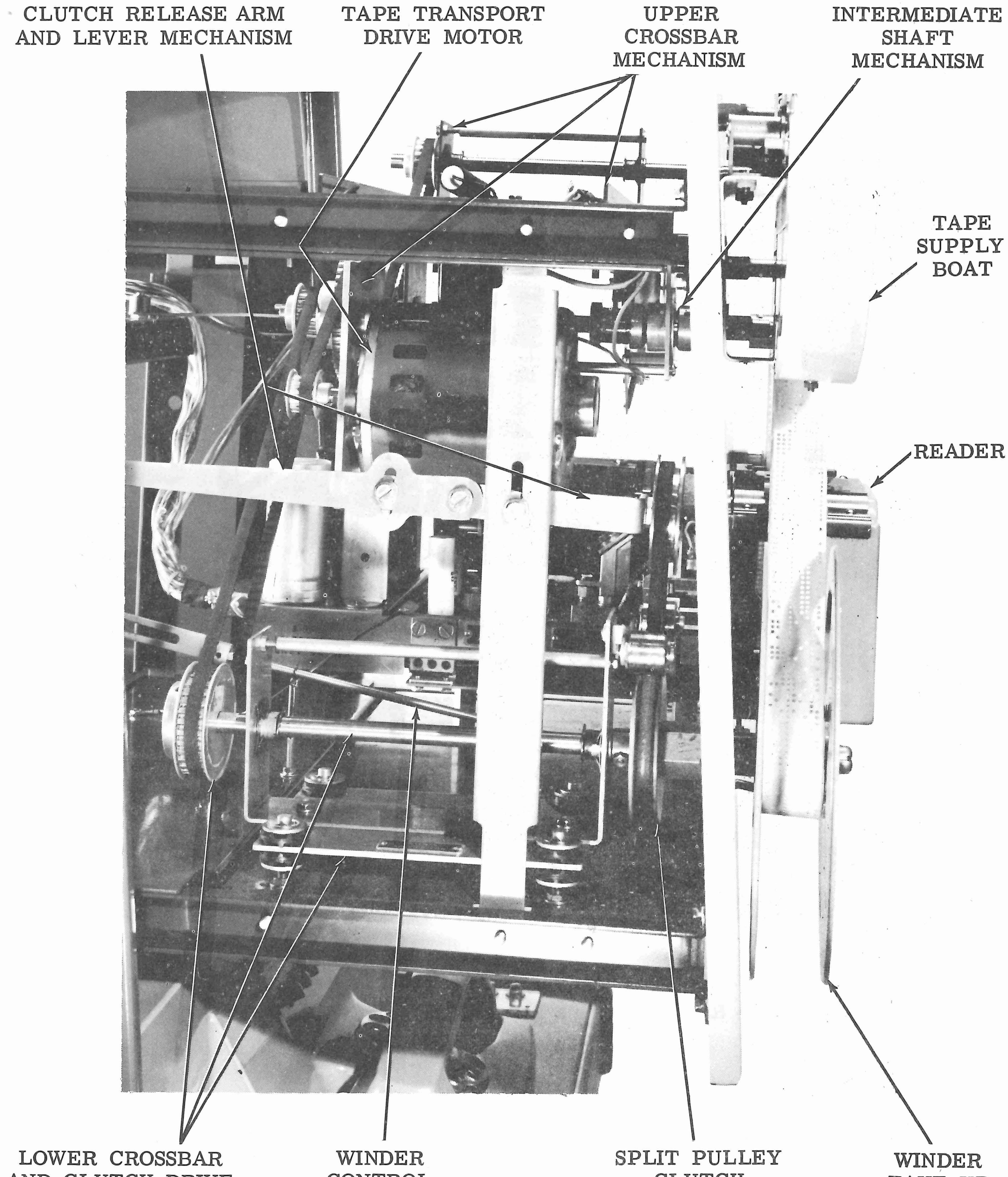

Figure 13 - Reader and Tape Transport Assembly, Left Side View

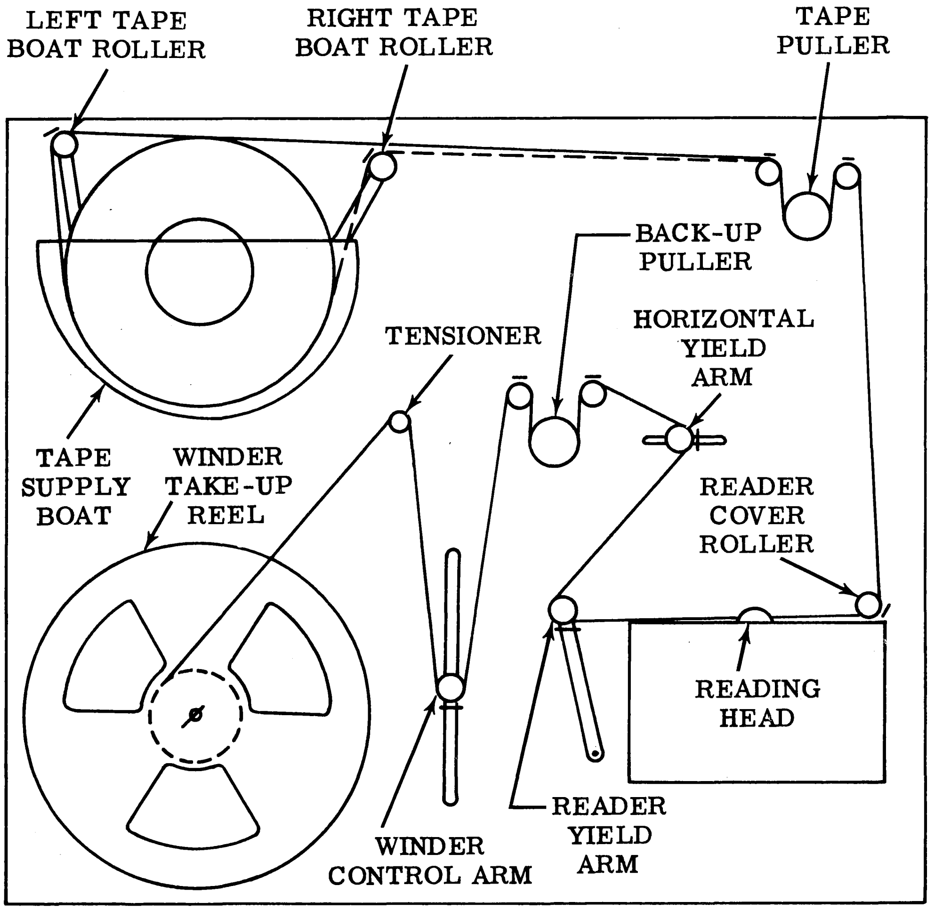

Figure 14 - Path of Tape

OPERATION

A. General

6.03 The following paragraphs describe the operation of the reader and tape transport assembly in terms of the way in which the tape is loaded and handled. Figure 14 illustrates the path of the tape when it has been loaded.

B. Tape Supply

6.04 The supply tape is placed in the tape boat with the three-hole side (counting from the feed holes) closest to the panel and a leader of approximately eight feet provided for threading. Sixty inches of leader is required to go from the reading head to the take-up reel. The tape is run over the left tape boat roller if the loose end of the tape roll is on the left side of the tape boat. If the loose end of the tape roll is on the right side of the tape boat, the tape is run over the right tape boat roller as shown by the dashed line in Figure 14. The tape is then run over the roller to the left of the puller, under the puller, and over the roller to the right of the puller. The tape puller rotates continuously, but only pulls when the tape is tightened around it by tension from the reader. The tape is next run down the right side of the panel and under the roller to the right of the reading head and placed in the reading head.

C. Tape Take-Up

6.05 From the reading head, the tape is placed under the roller on the yield arm to the left of the reading head, then up and on the right side of the roller on the horizontal yield arm. The tape is next run over the roller to the right of the back-up puller, under the back-up puller, and over the roller to the left of the back-up puller. Finally, the tape is run under the roller on the control arm, over the tensioner, and started on the take-up reel.

6.06 With the forward movement of tape, a slack condition develops between the reader and the tensioner. This allows the control arm to move downward and through a system of levers, the belt clutch is tightened, and the excess tape is wound on the take-up reel. As the excess tape is wound, the control arm moves upward and loosens the belt clutch.

6.07 When the reader runs in the reverse direction, the back-up solenoid is energized and, through a lever, activates the clutch on the back-up puller. The back-up puller is then powered in a counterclockwise direction and, as tension is produced in the tape between the reader and back-up puller, the tape moves in the reverse direction. As the tape moves in the reverse direction, it first causes the loop around the control arm to shorten, thus moving the arm upward and releasing the tape take-up clutch. Then, as additional tape is required for pull-back, it is unwound from the take-up reel.

6.08 After pull-back is completed, the reader motor is reversed (to the forward direction) and the back-up solenoid is de-energized. The transport is then ready for the forward movement of tape.

7. HSEDC TRANSMITTER CONTROL MODULE

DESCRIPTION

A. General

7.01 The HSEDC transmitter control module (Figure 15) is the basic component of the sender terminal. It provides the electronic logic required for the error detection and correction (EDC) feature of the terminal.

7.02 The function of the HSEDC transmitter control module is to transfer the parallel output signals generated by the high speed tape reader to the transmitter distributor module alternately with control and parity characters generated by the HSEDC transmitter control module and to control the operation of the transmitter distributor module for block rerun error correction.

B. Input and Output Signals

7.03 The input signals to the HSEDC transmitter control module come from two sources. The first source is the read contacts of the reader through the transmitter distributor module. The signals are 8 levels of parallel data where 0 volts indicates a mark and -6 volts indicates a space. The second source is the verify contacts of the reader. The signals from the verify contacts are contact closures from each of the 8 contacts, where 0 volts indicates a mark and an open circuit indicates a space.

7.04 The output of the HSEDC transmitter control module is 8 levels of parallel data representing either the data information read by the read contacts of the reader or control characters generated by the HSEDC transmitter control module internally or from the reader verify contacts.

C. Operational Features

7.05 The HSEDC transmitter control module operates at 105 characters per second and 5, 6, 7, or 8 code levels may be utilized.

7.06 The error detection and correction (EDC) feature may be disabled by controls (see Figure 4) external to the module.

7.07 The HSEDC transmitter control module functions in conjunction with controls and indicators located on the cabinet of the sender. Auxiliary controls and indicators for testing and troubleshooting are located in the module (see Figure 11) to simulate normal operation.

D. Operating Conditions

7.08 Power required for the HSEDC transmitter control module is obtained from the transmitter distributor module. Voltage and current requirements are listed below.

VOLTAGE	CURRENT
1v ac	1 amp
+50v dc	15 ma
+6v dc	225 ma
-6v dc	225 ma
-12v dc	1 amp
-48v dc	30 ma

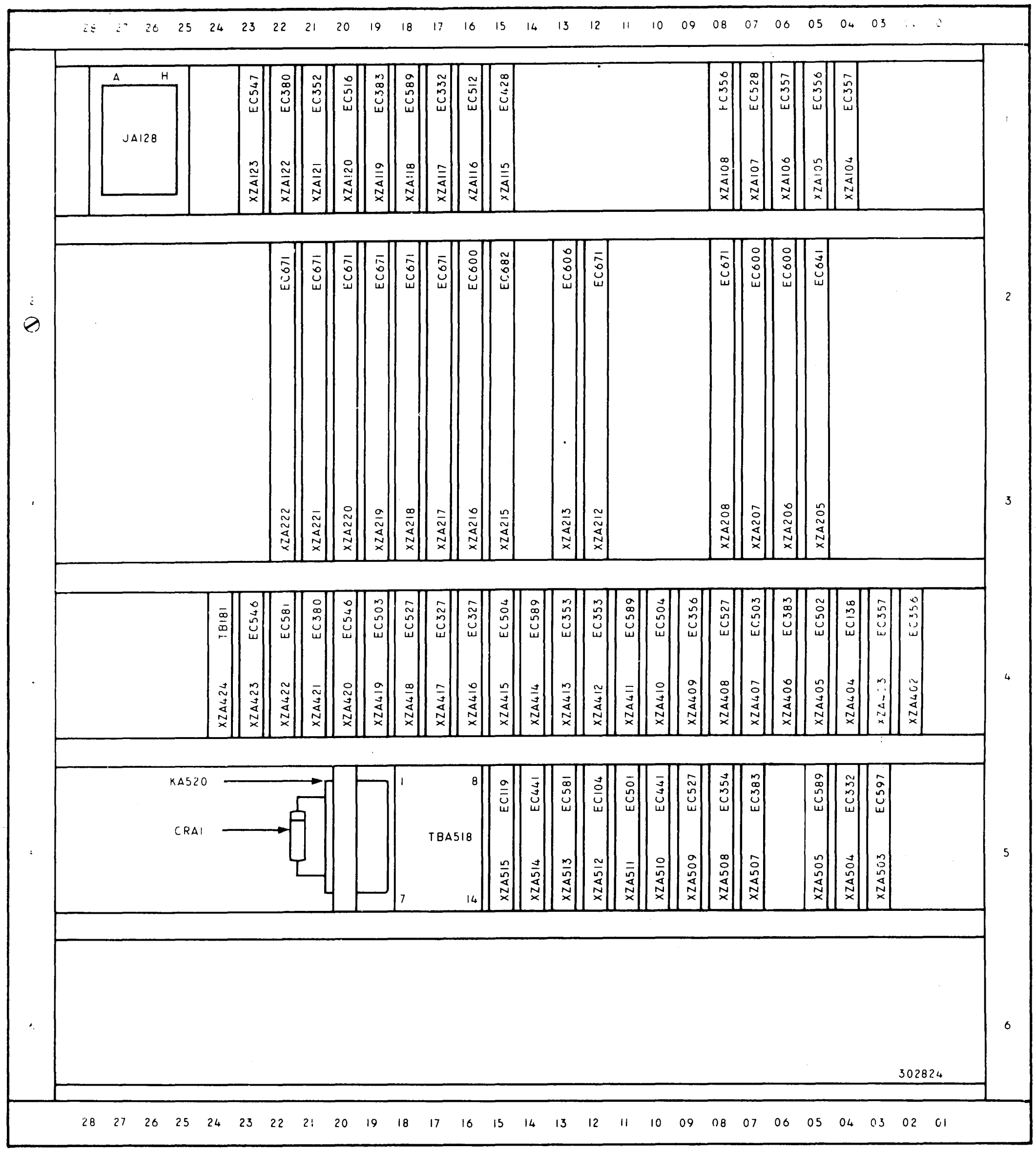

Figure 15 - HSEDC Transmitter Control, Module A, Left Side View

OPERATION

A. General

7.09 The HSEDC transmitter control module electronics are represented by schematic wiring diagram 7056WD. All circuits are shown in symbolic logic and each circuit is indicated by an EC number and a ZA number which is an element number. The schematic diagrams and a detailed description of each circuit appear in other sections.

7.10 To understand the functions of the HSEDC transmitter control module, a brief description of the operation of the sender is included here.

7.11 The sender terminal transmits data in blocks of 80 characters. It uses the reverse channel as a means of determining when to start or stop transmission. Before transmission of the data, the sender inserts and sends SR (sender ready) characters. These characters are transmitted until the receiver terminal detects them and turns on reverse channel. When the sender recognizes reverse channel is on, it sends a BN (block number) character. There are three different BN characters and these are used to maintain synchronization with the receiver; one of each is transmitted before successive blocks and thereafter repeated during transmission of the data tape. After transmission of the BN character, the sender transmits 80 information characters followed by an EOB (end-of-block) character. During transmission of the EOB character, the reverse channel is sampled. After the EOB character, two longitudinal parity check characters, CK1 (check Character 1) and CK2 (check character 2) are transmitted. CK1 is derived from a horizontal parity check of the 80 information characters and CK2 is derived from a spiral parity check of the 80 information characters. If the reverse channel was on when sampled, the next block will be transmitted, preceded by the next BN character and followed by the EOB character and the two derived check characters.

7.12 The sender is told an error has been detected by the removal of reverse channel. Since the receiver does not detect the error until after the check characters are sent, the reverse channel is not detected as off until the end of the block following the errored block. When the loss of reverse channel is detected, the sender advances into the error correction mode. The check characters are deleted; the reader reverses, backs up the tape two blocks (160 characters), and stops. The sender then begins sending SR characters, in this case, signalling it is ready to retransmit the errored block.

7.13 The HSEDC transmitter control module electronics can be functionally divided into four separate areas: the programmer and control logic, the control character generator, the check character generators, and the character selector gates. The programmer and control logic area is the most important because of its ultimate control of the operation of the sender terminal. The programmer has eight modes and each mode determines the type of character to be transmitted and/or the type of action required. The programmer advances to each mode sequentially and in the following order: SR mode, BN mode, BK mode, EOB mode, CK1 mode, CK2 mode, R1 mode, R2 mode, and back to the SR mode. This sequence encompasses all modes and includes the modes required for the error correction operation. A feedback feature allows the programmer to advance from the CK2 mode to the BN mode, skipping the SR, R1 and R2 modes, for normal operation with no errors detected. The control logic determines the starting and stopping of operation, the recognition of the state of the reverse channel, and provides for the advancing of the programmer from one mode to another.

7.14 When power to the sender terminal is initially turned on, the programmer may be set to any of the eight possible modes. In order for the terminal to start properly, the programmer must be in the SR mode and, although power may be on in the terminal, power is not given to the reader until a data communication line is established to the terminal. With no power to the reader, the programmer is not able to cycle back to the SR mode. Inverter ZA104D and power amplifier ZA422B are provided to energize the motor start relay in the sender station control and supply power to the reader. As long as the programmer is not in the SR mode, pin P of inverter ZA104D is at -6 volts and the output of ZA104D, pin S, is at 0 volts. This 0-volt potential is supplied to pin K of power amplifier ZA422B to enable the amplifier and supply power to energize the motor start relay. Pin S of ZA422B will be at 0 volts where it is brought to terminal G10 of connector JA128 for distribution to the sender station control. When the programmer returns to the SR mode, pin P of ZA104D will go to 0 volts, causing the output (pin S) and the input of ZA422B (pin K) to go to -6 volts and the output of ZA422B (pin S) to go to -6 volts. Once a communications line is established, the motor start relay is energized by logic in the sender station control of the terminal.

B. Programmer and Programmer Advance

7.15 The programmer is made up of two circuit cards, ZA416 and ZA417, consisting of ring distributor elements. Ring reset circuits ZA412A and ZA413A and the wiring between circuits on ZA416 and ZA417 determine which modes the programmer will advance to during each state of its sequence. One-shot ZA411 and ring drive circuit ZA412B provide the pulses for advancing the programmer.

7.16 The signals to advance the programmer are positive-going pulses, 10 microseconds long, and from -6 volts to 0 volts. The source of these pulses is described later and it is sufficient to say here that each pulse produces a programmer advance pulse. The 10-microsecond pulse is presented to the set input (pin L) of one-shot ZA411. The prime input (pin K) of ZA411 is permanently held at 0 volts. The inverted output of one-shot ZA411 is tied to the input (pin F) of ring driver ZA412B. The inverted output of ZA411 is normally at 0 volts. When a positive-going transition appears at the set input (pin L) the one-shot will start a time-out of 200 microseconds. The output (pin J) goes to -6 volts and, at the end of 200 microseconds, returns to 0 volts. This positive-going transition is applied to pin F of ring driver ZA412B to trigger the ring driver circuit and produce a negative-going, 0 volts to -6 volts, pulse at pin N of ZA412B. The negative-going pulse from pin N of ZA412B is then applied to the inputs (pins N, P, R and S) of ring distributor elements ZA416 and ZA417 to advance the programmer.

7.17 When the programmer is in the SR mode, the output, pin H of ring element ZA416A, is at 0 volts and the outputs of all the other elements in the programmer are at -6 volts. The output of pin H of ZA416A is applied to pin R of ring reset circuit ZA412A where it is passed through to the output of ZA412A (pin P) and presented to pin F of ZA417A to prime the programmer to advance to the BN mode. When the advance pulse comes into the programmer, it is accepted by pin P of ZA416A to turn off the SR ring element. The transition from 0 to -6 volts at pin H of ZA416A comes in to pin F of ZA417A through ZA412A to turn on the BN ring element and place the programmer in the BN mode. Pin H of ZA417A goes to 0 volts which is then applied to pin A of ZA416D to prime the BK ring element. The next advance pulse is accepted by pin P of ZA417A to turn off the BN ring element causing the output (pin H) to go to -6 volts. The negative transition is applied to pin A of ZA416D to turn on the BK ring element causing its output (pin D) to go to 0 volts. The programmer is now in the BK mode. When the next advance pulse comes in, it is accepted by pin S of ZA416D to turn off the BK ring element. The output (pin D) goes to -6 volts and this negative-going transition is applied to pin J of ZA416B to turn on EOB ring element causing its output (pin K) to go to 0 volts, placing the programmer in the EOB mode. The next programmer advance pulse is accepted by pin R of ZA416B to turn off the EOB ring element. The output (pin K) goes to -6 volts and this negative-going transition is applied to pin L of ZA416C to turn on the CK1 ring element causing its output (pin M) to go to 0 volts, placing the programmer in the CK1 mode. To advance the programmer to the CK2 mode, pin N of ZA416C accepts the next advance pulse, turning off the CK1 ring element and causing its output (pin M) to go to -6 volts. The negative-going transition at pin M is applied to pin A of ZA417D to turn on the CK2 ring element.

7.18 The programmer advances out the CK2 mode when the next advance pulse comes in. The programmer advance pulse is accepted by pin S of ZA417D, turning off the CK2 ring element and causing the output (pin D) to go to -6 volts. Which mode the programmer advances to now depends on whether the reverse channel has been detected as on or off.

7.19 If the reverse channel has been detected as on, pin 14 of flip-flop ZA212B is at 0 volts which holds 0 volts at pin K of ring reset ZA412A. The negative transition from pin D of ZA417D is presented to pin H of ZA412A through emitter followers ZA213F and ZA213P at the same time it is applied to pin J of the R1 ring element ZA417B. The negative-going transition at pin H of ZA412A produces a negative-going pulse at the output (pin P) which is applied to pin F of the BN ring element ZA417A. While the transition at pin J of ZA417B attempts to turn on the R1 ring element, the pulse at pin F of the BN ring element lasts longer and the BN ring element turns on instead, resetting the programmer to the BN mode. Once in the BN mode, the programmer advances through its normal sequence as described in paragraph 7.17.

7.20 If the reverse channel has been detected as off, pin K of ZA412A is at -6 volts and the negative-going transition at pin H is ignored by the ring reset circuit. The negative transition is accepted by pin J of ZA417B, causing the R1 ring element to turn on and placing the programmer in the R1 mode. The output of ZA417B (pin K) goes to 0 volts. The next programmer advance pulse is accepted by pin R of ZA417B, turning off the R1 ring element and causing the output (pin K) to go to -6 volts. The negative-going transition at pin K is applied to pin L of ZA417C, causing the R2 ring element to turn on. The output of ZA417C (pin M) goes to 0 volts and the programmer is in the R2 mode. The next advance pulse is accepted by pin N of ZA417C, turning off the R2 ring element and causing the output (pin M) to go to -6 volts. The negative-going transition at pin M is applied to pin R of ring reset circuit ZA413A. The resulting negative-going transition from pin M of ZA413A goes to pin F of the SR ring element ZA416A to turn on the SR element and place the programmer in the SR mode. Pin H of ZA416A goes to 0 volts. Once in the SR mode, the programmer advances through its normal sequence as described in 7.17.

7.21 The output of each element of the programmer is distributed to other points in the HSEDC transmitter control module through two emitter followers which provide power amplification. The SR ring element output (pin H of ZA416A) feeds the inputs (pins 29 and 9) of ZA213A and ZA213J and is presented to the module on pins 19 and 17 of ZA213A and ZA213J. The output of the BN ring element (pin H of ZA417A) goes in pins 30 and 10 of emitter followers ZA213B and ZA213K and comes out to the module on pins 33 and 13. The BK ring element output (pin D of ZA416D) feeds pin P of OR gate ZA415D whose output (pin S) goes to pins 31 and 11 of emitter followers ZA213C and ZA213L. The outputs of ZA213C and ZA213L (pins 34 and 14) then present the BK mode condition to the module. The second input (pin N) of OR gate ZA415D is used to provide an artificial BK mode condition when the terminal is used with the non-EDC feature. The output (pin K) of the EOB ring element ZA416B feeds the inputs of emitter followers ZA213D and ZA213M (pins 32 and 12) and is presented to the module through the output terminals, pins 35 and 15. The output of the CK1 ring element (pin M of ZA416C) goes to pins 21 and 1 of emitter followers ZA213E and ZA213N and goes to the module from the output, pins 20 and 18. The CK2 ring element output (pin D of ZA417D) drives the inputs (pins 22 and 2) of emitter followers ZA213F and ZA213P and comes out on pins 25 and 5. The R1 ring element output (pin K of ZA417B) goes to the inputs of emitter followers ZA213G and ZA213Q (pins 23 and 3) and comes to the module from the outputs (pins 26 and 6). The output of the R2 ring element (pin M of ZA417C) feeds the inputs (pins 24 and 4) of emitter followers ZA213H and ZA213R and presents the R2 mode condition to the module through the outputs of ZA213H and ZA213R (pins 27 and 7).

7.22 The initial starting of operation is controlled by the run/stop signal and the tape-out signal. In addition, the EDC/non-EDC signal determines whether the module, and consequently the terminal, operates in the EDC mode or the non-EDC mode. The run/stop signal comes into the HSEDC transmitter control module on terminal A1 of connector JA128. 0 volts indicates the run condition and -6 volts represents the stop condition. The tape-out signal comes in on terminal A10 of JA128. An open circuit indicates there is tape in the reader. A ground signal (0 volts) indicates the tape-out condition and is used to prevent the terminal from operating without a message to send. The EDC/non-EDC signal comes into the module on terminal A2 of JA128. An open circuit indicates the EDC mode and a ground signal (0 volts) indicates the non-EDC mode.

7.23 The output (pin H) of a clamp circuit on ZA424, which consists of resistor R4 and diode CR4, is tied to the EDC/non-EDC lead to bias the lead to -6 volts when the lead is open-circuited. The -6 volt signal is applied to pin C of inverter ZA403C causing its output (pin A) to go to 0 volts which holds the inhibit input (pin E) of inhibit gate ZA402D at 0 volts. With 0 volts on pin E, the output (pin J) of ZA402D is at -6 volts regardless of the potential at the emitter input (pin C) and the -6 volts potential is applied to the inputs (pins P and B) of emitter followers ZA408D and ZA504-1/2, holding the outputs (pins D and A) at -6 volts. This inhibits AND gate ZA407B which, through emitter follower ZA408A, keeps pin N of ZA415D at -6 volts and prevents an artificial BK mode condition. In addition, OR gate ZA511B, which will pass a 0-volt signal, does not accept the -6 volt signal applied to its input (pin F) by emitter followers ZA408D and ZA504-1/2. The -6 volts bias on the EDC lead is also applied to the base inhibit input (pin F) of inhibit gate ZA402C to prime that gate to accept the signal at the emitter input (pin A).

7.24 If there is no tape in the reader, 0 volts will be applied to pin J of integrator ZA123E which causes its output (pin B) to go to 0 volts and inhibits gate ZA409B, thus preventing the module from starting to operate. However, with tape in the reader, pin J of integrator ZA123E is open-circuited and the output (pin B) is at -6 volts which is applied to pin M of ZA409B and primes this gate to accept the run/stop signal applied to its emitter input (pin P). The tape-out signal from pin B of ZA123E is also applied to the prime 1B input (pin 32) of flip-flop ZA212A for use in resetting the programmer if the tape-out condition occurs during operation.

7.25 With the base inhibit input (pin M) primed at -6 volts, inhibit gate ZA409B will accept the 0-volt run signal at its emitter input (pin P) and the output (pin L) of ZA409B goes to 0 volts. This signal is applied to pin A of inhibit gate ZA402C and pin C of inhibit gate ZA402D. However, the signal is ignored by ZA402D since the base input (pin E) is held at 0 volts but the signal is accepted by ZA402C, whose base input (pin F) is primed at -6 volts and the output (pin H) will go to 0 volts. The 0 volts at pin H is applied to pin S of emitter follower ZA408F and pin D of emitter follower ZA504-1/2 which amplify the signal and produce a 0-volt signal at the outputs of the emitter followers (pin A of ZA408F and pin N of ZA504-1/2) which signifies EDC-run. The EDC-run 0-volt signal is applied to pin D of AND gate ZA405C to prime the gate to accept the reverse channel signal and it goes to pin N of inverter ZA403A which then gives a -6 volt signal to the prime 1A input (pin 35) of flip-flop ZA212A. If the EDC-run signal goes to -6 volts, the output of inverter ZA403A goes to 0 volts and primes the ZA212A flip-flop to reset the programmer. The EDC-run signal (0 volts) also goes to pin N of ZA424, through diode CR6 and comes out on pin M to the inverted output of flip-flop ZA212A (pin 13) to force it to 0 volts which forces the normal output (pin 12) to -6 volts. The ZA212A flip-flop's normal output (pin 12) then puts -6 volts on the input to OR gate ZA511B (pin E) which, in conjunction with the -6 volts on pin F, holds the output (pin B) at -6 volts. This -6 volt signal then feeds the input to ring reset ZA413A (pin D) causing its output (pin M) to -6 volts and removing the holding signal from pin F of the SR ring element ZA416A. The removal of the holding signal from pin F allows the programmer to advance out of the SR mode when it receives an advance pulse.

C. SR Mode Operations

7.26 When the programmer is in the SR mode, the output of inverter ZA104D (pin S) is at -6 volts which is applied to pin H of IPS circuit ZA508. After the -6 volt signal is present at the input for more than 500 milliseconds, the output (pin K) goes to -6 volts. This signal is sent to pin M of inhibit gate ZA402B, which is connected as an inverter. The output of ZA402B (pin L) will go to 0 volts and is tied to pin L of AND gate ZA419B. The EDC-run signal (0 volts) is applied to pin K of AND gate ZA419B. The input of gated oscillator ZA420 (pin P) is always held at -6 volts which produces a stream of positive-going, -6 to 0 volt pulses of 10 microseconds duration and spaced approximately 40 milliseconds apart. This stream of pulses is applied to pin M of AND gate ZA419B. With inputs K and L at 0 volts, each pulse at pin M passes through the AND gate and appears at pin R. From pin R, the pulse goes in pin N of emitter follower ZA509A, out of pin K, and into pin F of OR gate ZA421. From the output of OR gate ZA421 (pins J and K) the pulse goes into pin J of emitter follower ZA418C, comes out on pin E. and goes to terminal A8 of connector JA128. Thus, when the programmer is in the SR mode, a 10-microsecond pulse will appear on the transmitter distributor start lead every 40 milliseconds.

7.27 The SR mode output of the programmer also performs other functions. This 0-volt signal is applied to pin P of OR gate ZA405A which causes its output (pin R) to go to 0 volts. This signal is then sent to the base input (pin E) of inhibit gate ZA409D to prevent any signals on pin C from going through. The SR mode signal also goes to pin E of AND gate ZA405B. In addition, the SR mode 0-volt signal is applied to pin D, the emitter input of inhibit gate ZA105A. The base input (pin N) is at -6 volts since the BK mode signal is at -6 volts; therefore, the output of ZA105A (pin K) is at 0 volts. The 0-volt signal from pin K then goes to pin 7 of the diode matrix circuit ZA205 to generate the SR character.

7.28 The diode matrix circuit (ZA205) is the control character generator mentioned in 7.13. The outputs of the matrix circuit are normally biased at -6 volts by the outputs of gate circuits ZA206 and ZA207. There are eight outputs and each output corresponds to a particular level in an 8-level character. Output pin 26 corresponds to level 1, pin 25 corresponds to level 2, pin 24 corresponds to level 3, pin 23 corresponds to level 4, pin 20 corresponds to level 5, pin 19 corresponds to level 6, pin 18 corresponds to level 7, and pin 17 corresponds to level 8. These outputs tie to terminals E1 through E8 of connector JA128 to send the character to the inputs of the transmitter distributor module for insertion into the character shift register and eventual transmission.

7.29 Depending on which input is energized, the outputs of matrix circuit ZA205 go to 0 volts, corresponding to a marking condition, or they will remain at -6 volts, corresponding to a spacing condition. When pin 7 is at 0 volts, the SR character is generated. Pin 15 produces the BN1 (block number one) character, pin 21 produces the BN2 character, pin 28 produces the BN3 character, and pin 35 produces the EOB character. The actual characters generated are shown in Table 2 (see Part 5).

7.30 Every time a pulse appears on the transmitter distributor start lead into the transmitter distributor module, the transmitter distributor triggers and sends one character. Timing is generated by a clock signal in the transmitter distributor which produces bit timing and character timing. After receiving the TD start pulse, the transmitter distributor waits for the proper clock transition before sending the character. At that time it resets the shift register and then, one-half bit later, it generates a sample pulse which inserts the character into the register. The character it sets is the SR character described in paragraph 7.27. One-half bit after the start of the sixth bit of any character, the transmitter distributor generates a reset pulse for use by CSS (contact signal shaping) circuits which store the signals from the reader code-reading contacts. One-half bit after the start of the character's stop bit, a pulse is generated for use in stepping the reader from one character to the next character. The sample pulse and the reader drive pulse are each 10 microseconds long and positive-going. The CSS reset pulse is a positive-going pulse but its length is 200 microseconds. The CSS reset pulse is used by both transmitter distributor module and the HSEDC transmitter control module. It comes into the module on terminal A5 of connector JA128. The reader drive pulse is controlled by the HSEDC transmitter control module. It comes into the module on terminal A6 of connector JA128 and goes to pin P of AND gate ZA419D. AND gate ZA419D only passes these pulses when the programmer is in the BK mode. The sample pulses are brought to the module on terminal A7 of connector JA128.

7.31 The sample pulse for the SR character is used to perform two major functions in the HSEDC transmitter control module. Its first function is to detect the presence of the reverse channel and its second function is to try to advance the programmer out of the SR mode. The reverse channel is not turned on until the distant receiver terminal detects the SR characters; and, until the reverse channel on signal comes to the sender, several more SR characters will have been sent.

7.32 The reverse channel detect flip-flop (ZA212B) is in the 0 state with its normal output (pin 14) at -6 volts. The -6 volts is applied to pin H of AND gate ZA405B which inhibits the gate from passing the sample pulses that appear on pin F and advancing the programmer. With the reverse channel off, the prime 1B input (pin 24) of flip-flop ZA212B is at -6 volts to prevent the sample pulses at pin 25 from setting the flip-flop.

7.33 The reverse channel signal comes into the module on terminal A4 of connector JA128. A 0-volt signal means the reverse channel is off and a -6 volt signal means the reverse channel is on. When the reverse channel comes on, the input of inverter ZA106C (pin C) goes to -6 volts causing the output (pin A) to go to 0 volts which then applies 0 volts to pin E of OR gate ZA415A. With 0 volts at the input (pin E) the output of ZA415A (pin B) goes to 0 volts which is applied to pin H of IPS circuit ZA404. After a delay of approximately 20 milliseconds, to prevent noise from being recognized as the reverse channel, the output of IPS circuit ZA404 (pin K) goes to 0 volts and sends this signal to pin C of AND gate ZA405C. Since pin D of ZA405C is at 0 volts due to the EDC-run signal, the output of AND gate ZA405C (pin A) goes to 0 volts which is applied to the prime 1B input (pin 24) of flip-flop ZA212B. When the next SR sample pulse comes in, it is still inhibited at AND gate ZA405B by the -6-volt signal on pin H but it is accepted by the set 1B input (pin 25) of flip-flop ZA212B causing the normal output (pin 14) to go to 0 volts. This 0 volts is now applied to pin H of ZA405B to enable the gate to accept the next sample pulse and it is also applied to pin K of ring reset circuit ZA212A to enable this circuit. The inverted output of flip-flop ZA212B (pin 17) goes to -6 volts and inhibits AND gate ZA419A (pin E), which is used to blind the output of the transmitter distributor in the error correction mode.

7.34 When the next SR sample pulse comes in to pin F of AND gate ZA405B, it is passed through the gate and from the output (pin B) it goes to the input (pin N) of emitter follower ZA418B for amplification. From the output of ZA418B, (pin F) the SR sample pulse goes to OR gate ZA410A (pin F) which sends it from its output (pin B) to the input of one-shot ZA411 (pin L); 200 microseconds later, the programmer advances out of the SR mode and into the BN mode. The SR mode signal goes to -6 volts and, through OR gate ZA405A, enables the base input (pin E) of inhibit gate ZA409D and it also inhibits AND gate ZA405B. In addition, through inverter ZA104D, IPS circuit ZA508, and inhibit gate ZA402B, a -6 volt signal is applied to pin L of ZA419 to prevent any more pulses from going to OR gate ZA421. It also removes the mark and space signals for the SR character from the inputs to the transmitter distributor shift register.

D. BN Mode Operation

7.35 When the programmer advances to the BN mode, a 0-volt signal is applied to pin A of OR gate ZA421 and from the output (pins J and K) through emitter follower ZA418C to the TD start lead (terminal A8); and, 0 volts on this lead indicates that the transmitter distributor is to continue to transmit characters, one after another. Thus, at the end of sending the SR character that is still in the register, it resets immediately and inserts the next character. The next character is one of the three possible BN characters.

7.36 The BN mode 0-volt signal comes in to the emitter inputs of three inhibit gates, pin A of ZA105C, pin C of ZA105D and pin P of ZA105B. Each gate is thus primed to accept a signal from a contact on a special EDC assembly located on the reader. The contacts close to -6 volts and come into the module to energize the respective inhibit gate; only one of the contacts is closed at any time. When the BN1 contact is closed, the -6 volt signal comes in terminal G1 of connector JA128 to input pin F of ZA105C which causes the output (pin H) to send a 0-volt signal to pin 15 of matrix circuit ZA205 and produce the BN1 character at the outputs of ZA205. The -6 volt signal from the BN2 contact comes in on terminal G2 of connector JA128, goes to pin E of inhibit gate ZA105D, comes out on pin J as a 0-volt signal, and is sent to pin 21 of matrix circuit ZA205 to produce the BN2 character. The -6 volt signal from the BN3 contact comes in on terminal G3 of connector JA128, goes to pin M of inhibit gate ZA105B, comes out on pin L as a 0-volt signal, and is sent to pin 28 of ZA205 to generate the BN3 character. Only one character is generated at any one time. The outputs of the matrix card ZA205 are sent to the TD shift register inputs through terminals E1-E8 of connector JA128. Refer to Table 2 in Part 5 to determine which levels are mark and which levels are space for each of the BN characters.

7.37 The closures of the BN contacts are centered about the closures of the EOB (end-of-block) contacts described in paragraph 7.43.

7.38 Immediately after sending the last SR character, the TD shift register is reset. One-half bit later, the BN character is inserted into the register by the sample pulse. The sample pulse comes into the HSEDC transmitter control module to pin C of inhibit gate ZA409D and, with pin E enabled, the pulse comes out on pin J and goes to pin E of OR gate ZA410A. The sample pulse passes through the gate and comes out on pin B to the set input (pin L) of one-shot ZA411; 200 microseconds later, the programmer advances out of the BN mode and into the BK mode.

E. BK Mode Operation and Check Character Generation

7.39 BK Mode Operation: When the programmer steps out of the BN mode, the 0-volt signal is removed from pin A of OR gate ZA421; but, the BK mode 0-volt signal applied to pin C, through OR gate ZA421 and emitter follower ZA418C, keeps the TD start lead positive and allows the transmitter distributor to continue to transmit characters. The BK mode signal is applied to pin M of OR gate ZA405A, through the gate, and applied to pin E of inhibit gate ZA409D to prevent subsequent sample pulses from coming through to advance the programmer. The signal is also applied to pin N of AND gate ZA419D to enable the gate to pass the reader drive pulses from the transmitter distributor; in addition, the signal goes to pin E of inverter ZA106B which is the BK mode input to the character selector gates. It produces a -6 volt signal on the output of ZA106B (pin B) which is sent in pin J of emitter follower ZA107C and out pin E to the base inputs (pin 36) of special inhibit gates of ZA207. The -6 volts on the base of each gate of ZA207 enables each gate to pass the signal from one level of the reader read-contacts. The -6 volt BN mode signal now prevents inhibit gates ZA105C, ZA105D, and ZA105B from priming the inputs to ZA205 to generate a BN character.

7.40 At the end of transmitting the BN character, the transmitter distributor resets and the sample pulse inserts the next character at the transmitter distributor inputs into the shift register. This is the first character of the 80 characters that are read from the tape for transmission. These characters come from the information read by the reader read-contacts, go through CSS circuits in the transmitter distributor which shape the contact signal, and then go from the outputs of the CSS circuit to the HSEDC transmitter control module for gating. If a contact is closed to ground (0 volts) it indicates a mark (or hole) in the tape. If a contact is open, it indicates a space (or no hole) in the tape. For a mark at the input, the output of a CSS circuit is 0 volts; a space at the input produces a -6 volt signal at the output of a CSS circuit. These signals come into the HSEDC transmitter control module on terminals C1-C8 of connector JA128. The signal for level 1 comes in on terminal C1, level 2 on C2, and so on for the other 6 levels. From terminals C1-C8, the signals go to the emitter inputs of selector gates ZA207 whose base inputs have been primed by the BK mode signal: a mark (or 0-volt signal) on the emitter input of a gate produces a mark (or 0-volt signal) at the output; a space (or -6 volt signal) on an input produces a -6 volt-signal at the output. The outputs from the selector gates then tie to terminals E1-E8 of connector JA128 which sends the character signals to the inputs of the TD shift register.

7.41 The level 1 signals come into pin 34 of ZA207, out on pin 19, and tie to terminal E1 of JA128. The level 2 signals come into pin 31 of ZA207, out on pin 17, and tie to terminal E2. The level 3 signals come into pin 22 of ZA207, out on pin 18, and tie to terminal E3. The level 4 signals come into pin 25 of ZA207, out on pin 20, and tie to terminal E4. The level 5 signals come into pin 4 of ZA207, out on pin 9, and tie to terminal E5. The level 6 signals come into pin 6 of ZA207, out on pin 10, and tie to terminal E6. The level 7 signals come into pin 14 of ZA207, out on pin 13, and tie to terminal E7. The level 8 signals come into pin 7 of ZA207, out on pin 29, and tie to terminal E8.

7.42 The reader drive pulses from the transmitter distributor come in to the HSEDC transmitter control module on terminal A6 of Connector JA128 and go to pin P of AND gate ZA419D. With input pin N at 0 volts from the BK mode signal, the pulses pass through the gate, come out on pin S and are sent to pin S of emitter follower ZA418F. From the output of ZA418F (pin A) the pulses go to pin C of OR gate ZA415C, come out on pin A, and go to terminal G4 of connector JA128. Any pulse that appears on terminal G4 goes to an inverter in the transmitter distributor and then to the reader and causes the reader to step the tape to the next character. The first reader drive pulse to step the reader is the one generated at the end of the transmission of the BN character. Since it takes about 4.5 milliseconds for the reader to step the tape to the next character, the first character in the tape will still be inserted into the transmitter distributor before the reader steps the tape. In the middle of transmitting the characters, the reset pulse for the CSS circuit empties the CSS circuits to accept the next character. The second character of the block is then presented to the inputs of the TD shift register. At the end of transmitting the first character, a reader drive pulse is generated, which comes through the HSEDC transmitter control module to step the tape in the reader from the second to the third character. The TD shift register then resets and inserts the second character from the reader, through the CSS circuits and the HSEDC transmitter control module selector gates, into the shift register. The reader then advances the third character in the tape over the read contacts. In the middle of sending the second character, the CSS circuits are reset and the third character is stored in them. The reader drive pulse generated at the end of character two now commands the reader to step the tape and place character four over the read-contacts. After sending character two, the transmitter distributor resets, inserts character three into the shift register, and transmits that character. Character four then moves over the reader read-contacts, the CSS circuits are reset, the fourth character is then stored and, at the end of sending character three, another drive pulse is generated which commands the reader to move the fifth character over the read contacts. Then the fourth character is set into the TD shift register to be sent. As long as the programmer is in the BK mode, the above sequencing is followed.

7.43 The sender terminal transmits characters in blocks of 80 when it is operating in the EDC mode. The counting of the 80 characters is accomplished through the use of a special cam on the EDC portion of the reader. The cam makes one revolution for every 80 steps of the reader. A wire spring contact follows this cam and once every revolution, it is allowed to fall into an indent on the cam and close the contact to ground. The output of the contact is brought to the HSEDC transmitter control module for sampling to determine the end of an 80-character block. A second cam and contact are used for counting when the reader runs in the reverse direction.

7.44 The signal from the forward EOB contact comes in on terminal G7 of connector JA128 and goes to the make side of transfer switch 6 of relay KA520; the signal from the reverse EOB contact comes in on terminal G8 of JA128 and goes to the break side of transfer switch 6 of relay KA520. Relay KA520 is normally held energized by a ground signal from a contact off the motor reverse relay in the sender station control and the make side of transfer switch 6 is closed which allows the forward EOB contact signal to pass through and go to the input (pin M) of integrator ZA123C; the reverse EOB is ignored in this sequence. Integrator ZA123C is used to eliminate the bouncing of the signal from the EOB contact closures. The EOB contact is normally open which causes the output of ZA123C (pin D) to be at -6 volts; this -6 volt signal is applied to pin L of AND gate ZA511A to inhibit the gate.

7.45 The sample pulse from the transmitter distributor is used to sample the EOB contact to determine the end of an 80-character block. The sample pulse comes in to pin C of OR gate ZA511C, goes through the gate to the output (pin A), and is sent to pin K of AND gate ZA511A to sample the EOB contact. The sample pulses from the 1st character through the 78th character of the block find the EOB contact open and no output is produced at the output of AND gate ZA511A (pin R). At the end of the 78th character, the transmitter distributor sets the 79th character into the shift register. The sample pulse from the 79th character also finds the EOB contact open. During the transmission of the 79th character, the reader has moved the 80th character over the read contacts due to the drive pulse generated at the end of the 78th character. When the 80th character is over the read contacts, the forward EOB contact is closed and a 0-volt signal is applied to pin L of ZA511A. The distributor sets the 80th character into the TD shift register. The sample pulse from the 80th character finds the EOB contact closed and a positive-going, 10-microsecond pulse is produced at the output (pin R) of ZA511A. During transmission of the 80th character, the drive pulse from the 79th character causes the reader to move the 80th character off the read contacts and position the 1st character of the next block over the read contacts. The 80th step of the reader also causes the forward EOB contact to open. The EOB pulse from pin R of ZA511A goes in pin J of emitter follower ZA509C, comes out on pin E, and goes to pin H of OR gate ZA410A which passes the pulse from its output (pin B) to the input (pin L) of one-shot ZA411 to advance the programmer; 200 microseconds later, the programmer will advance out of the BK mode and into the EOB mode. The BK mode signal goes to -6 volts which, when applied to pin N of AND gate ZA419D, inhibits that gate so the drive pulse generated at the end of sending the 80th character is prevented from going through to step the reader.

7.46 Check Character Generation: The two check characters that are transmitted at the end of each block are generated during the BK mode by reading the tape a second time with a second reading head of contacts on the reader, called the verify contacts. The verify contacts are spaced one character past the read contacts and read the tape after each character has moved off the read contacts. Two sets of storage registers accept the signals from the verify contacts to generate the check characters. CK1 (check character 1) is generated in the first storage register from a horizontal parity count of the 80 characters in a block and CK2 (check character 2) is generated in the second storage register from a spiral parity count of the 80 characters. The outputs of the registers then feed two sets of selector gates which send the check characters to the transmitter distributor for transmission during the CK1 mode and the CK2 mode of the programmer. Flip-flops ZA222A, B, and C; ZA221A, B, and C; and ZA220A and B make up the horizontal check character registers and flip-flops ZA217A, B, and C; ZA218A, B, and C; and ZA219A and C make up the spiral check character register.

7.47 The positive transition that occurs on the BK mode lead when the programmer enters the BK mode is applied to pin E of power pulser ZA120 to reset the check character generator registers. The pulser produces a positive pulse at pin H which is applied to the set 0A inputs of the CK1 register flip-flops. Since the prime 0A inputs are permanently held at ground, the flip-flops are set to the 0 state with all the normal outputs at -6 volts and the inverted outputs at 0 volts. The positive pulse also goes to input pins J and K of fan-out gate ZA121 and appears on pins A, B, C, D, E, L, M, and N which apply the pulse to the inverted outputs of the spiral check character registers and force the registers to the 0 state. In the 0 state, the normal outputs are at -6 volts and the inverted outputs at 0 volts.

7.48 The sample pulses which set each character into the TD shift register are also used to insert the characters read by the verify contacts into the check character registers. However, the first sample pulse must be inhibited until the first character of the block has moved from the read contacts to the verify contacts; flip-flop ZA212C accomplishes this function. The inverted output of ZA212C (pin 2) is at 0 volts and the 0-volt signal is applied to pin N of inhibit gate ZA409A to prevent the sample pulses, that appear on pin D, from going through the gate. The sample pulses are also applied to the set input (pin L) of one-shot ZA414 whose prime input (pin K) is permanently held at 0 volts. The inverted output of one-shot ZA414 (pin J) is normally at 0 volts and goes to -6 volts for 200 microseconds every time a sample pulse comes in to the input. At the end of the 200-microsecond time, the positive transition back to 0 volts is applied to the set 1A input (pin 8) of flip-flop ZA212C and is ignored by flip-flop ZA212C unless the prime 1A input (pin 9) is at 0 volts. The prime 1A is at 0 volts only when the programmer has entered the BK mode. The sample pulse which sets the BN character into the transmitter distributor also causes the programmer to advance to the BK mode. The pulse is inhibited by ZA409A and it causes the 200-microsecond time-out of one-shot ZA414. The transition at the end of the 200 microseconds is ignored and the programmer advances to the BK mode and applies 0 volts to the prime 1A input (pin 9) of ZA212C. The sample pulse from the 1st character of the block is also inhibited by ZA409A. The positive transition that occurs at the end of the 200-microsecond time-out of one-shot ZA414 caused by the 1st character sample pulse is now accepted by the set 1A input (pin 8) and it sets the ZA212C flip-flop to the 1 state. The inverted output of ZA212C goes to -6 volts which, when applied to pin N of ZA409A, enables the inhibit gate to accept future sample pulses. The sample pulse which sets the 2nd character of the block into the transmitter distributor now comes in to pin D of inhibit gate ZA409A, passes through that gate, and comes out on pin K. From pin K, it goes in pin N of emitter follower ZA418A and comes out on pin K of ZA418A where it is used to insert the 1st character of the block, which is now over the verify contacts, into the check character registers.

7.49 The sample pulses for the verify contacts come in to pin D of inverter ZA116-1/2 which produces a negative-going 10-microsecond pulse at the output (pin L). From pin L, it goes in pin D of emitter follower ZA117-1/2 and comes out on pin N. These negative-going pulses now are used to set the characters into the registers. The verify sample pulses also go in pin L of one-shot ZA118, whose prime input is held at 0 volts, to set the one-shot and produce a 200-microsecond, positive-going pulse at the normal output (pin J). At the end of the 200-microsecond pulse, the normal output returns to -6 volts and this negative transition, applied to pin F of pulse amplifier ZA119A, produces a positive-going, 10-microsecond pulse at the output of ZA119A (pin N). The pulses out of pin N of ZA119A are the spiral check character register shift pulses.

7.50 The signals from the reader verify contacts come into the module on terminals D1-D8 of connector JA128, go to CSS circuits ZA215, and are presented to the emitter inputs of the inhibit gates on ZA216 for sampling. If a contact is closed to ground, it indicates a mark (hole) in the tape and the output of the CSS circuit is 0 volts. If a contact is open, it indicates a space (no hole) in the tape and the output of the CSS circuit is -6 volts. 0 volts primes the emitter inputs of ZA216 and -6 volts inhibits the inputs. When the negative-going sample pulse comes in on pin 36 of ZA216, it is accepted by those gates whose emitters are primed and it produces a positive-going pulse at the output of the gates; no pulse is produced by those gates whose emitters are inhibited.

7.51 The signal from the level 1 verify contact comes in on terminal D1 of JA128. The level 2 signal comes in on D2, the level 3 signal on D3, and so on to level 8 which comes in on D8. The signals from the level 1, 7, and 8 contacts go through LEVEL SELECTION switch SWA601, which is discussed more fully in 7.61.

7.52 The contact signal shaper reset pulse is used to reset the CSS circuits to accept each new character and occurs after the new character has been moved over the contacts. The 200-microsecond, positive-going reset pulse resets each of the circuits to the spacing condition. It remains for the marking signal on each contact to set the particular CSS circuit to the mark condition; the CSS circuit stores the mark signal even if the contact opens.

7.53 The level 1, 2, 3, 4, 5, 6, 7, and 8 signals feed the inputs of CSS circuit ZA215, pins 6, 14, 13, 11, 17, 18, 19, and 20 respectively. The outputs of the CSS circuits, pins 7, 8, 12, 10, 33, 30, 32, and 31 feed input pins 34, 31, 22, 25, 4, 6, 14, and 7 of inhibit gate ZA216.

7.54 Horizontal Check Character (CK1): The horizontal check character (CK1) is generated in flip-flops ZA222A, B, and C; ZA221A, B, and C; and ZA220A and B. Each level of the character is generated by summing the number of marking bits that occur in that level during the 80-character block. If the number of marking bits in a level is an odd number, the CK1 bit transmitted for that level is a space; if the number of marking bits in a level is an even number, the CK1 bit transmitted for that level is a mark. The generation of the parity bit for level 1 of CK1 is described here; the bits for levels 2-8 are generated in an identical manner.

7.55 Flip-flop ZA222A generates the level 1 bit for CK1. It is initially reset to the 0 state. The normal output (pin 12) is at -6 volts and the inverted output (pin 13) is at 0 volts which primes the prime 1B input (pin 32). The pulses from the output of inhibit gate ZA216 (pin 19), which indicate marking bits, are presented to the set 0B and the set 1B inputs of flip-flop ZA222A (pins 31 and 33). The first mark pulse is rejected by the set 0B input but it is accepted by the set 1B input and the flip-flop is set to the 1 state. The inverted output goes to -6 volts and removes the P1B prime signal and the normal output goes to 0 volts which primes the P0B input (pin 30). The next mark pulse is now accepted by the set 0B input (pin 31) and the flip-flop is set back to the 0 state. Subsequent pulses set the flip-flop to the 1 state if it is in the 0 state or they set it to the 0 state if it is in the 1 state. At the end of the 80-character block, the flip-flop is in the 0 state if an even number of mark pulses have been accepted or it is in the 1 state if an odd number of mark pulses have been accepted. The inverted outputs are then fed to the CK1 emitter inputs of selector gate ZA206 to insert the horizontal check character (CK1) into the transmitter distributor for transmission during the CK1 mode.

7.56 For level 1, the output of ZA222A (pin 13) feeds pin 34 of ZA206. For level 2, the output of ZA222B (pin 17) feeds pin 31 of ZA206. For level 3, the output of ZA222C (pin 2) feeds pin 22 of ZA206. For level 4, the output of ZA221A (pin 13) feeds pin 25 of ZA206. For level 5, the output of ZA221B (pin 17) feeds pin 4 of ZA206. For level 6, the output of ZA221 (pin 2) feeds pin 6 of ZA206. For level 7, the output of ZA220A (pin B) feeds pin 14 of ZA206. For level 8, the output of ZA220B (pin 17) feeds pin 7 of ZA206.

7.57 Spiral Check Character (CK2): The spiral check character (CK2) is generated in flip-flops ZA217A, B, and C; ZA218A, B, and C; and ZA219A and C. Each level of the spiral check character is generated by summing the number of mark bits that occur along a spiral pattern in the block of 80 characters. An even number of marking bits will produce a space for the check character level. An odd number of marking bits produces a mark for the check character level. Table 1 (see Part 5) provides a means to determine which level of each character is used to derive a specific check character level. The lower section of the table shows the 80-character block. The upper section of the table indicates which level of each character is to be used, the particular line being chosen to correspond to the check character level being generated. As an example, if the bit for the 4th level of CK2 is being generated, the level line begins with a 4. Read down the table to see which characters will have the 4th level used in the sum. The 4th level will be used from characters 1, 9, 17, 25, etc. Similarly, the 5th level of characters 2, 10, 18, 26, etc, will be used, the 6th level of characters 3, 11, 19, 27, etc, will be used and so on.

7.58 Each character is inserted into the spiral check character register in the same way it is set into the horizontal check character register. When the flip-flops are initially reset to the 0 state, the inverted output of each flip-flop goes to 0 volts and primes its own PIB input and the normal output goes to -6 volts. The mark pulses from the output of ZA216 tie in to the set 1B and set 0B inputs of these flip-flops. A mark pulse on the inputs causes a flip-flop in the 0 state to change to the 1 state and a flip-flop in the 1 state to change to the 0 state.

7.59 The inverted outputs of the spiral register flip-flops are tied to the prime 0A inputs of the next higher level flip-flop (1 is the next higher level for 8); and, if the inverted output is at 0 volts, it primes that flip-flop to set to the 0 state. The normal outputs are tied to the prime 1A inputs of the next higher flip-flop; and, if the normal output is at 0 volts, it primes that flip-flop to set to the 1 state. 200 microseconds after the sample pulse has generated the mark pulses which set the character into the spiral check character register, the spiral check register shift pulse applied to the set 0A and set 1A inputs of each flip-flop causes the mark or space bits in each register element to shift to the next higher element. As an example, suppose the mark bits in the first character have changed the spiral register flip-flops to the following states: 1, 0, 1, 0, 1, 0, 1, and 0 for levels 1-8. The shift pulse then shifts the flip-flops to the 0, 1, 0, 1, 0, 1, 0, and 1 states. The mark bits for the next character is added to the shifted bits and then the sum is shifted. This continues for 80 characters. At the end of the 80 characters, the inverted outputs of the spiral register flip-flops are then fed to the CK2 emitter inputs of selector gate ZA206 to insert the spiral check character (CK2) into the transmitter distributor for transmission during the CK2 mode.

7.60 For level 1, the output of ZA217C (pin 2) feeds pin 35 of ZA206. For level 2, the output of ZA217A (pin 13) feeds pin 32 of ZA206. For level 3, the output of ZA217B (pin 17) feeds pin 24 of ZA206. For level 4, the output of ZA218C (pin 2) feeds pin 26 of ZA206. For level 5, the output of ZA218A (pin 13) feeds pin 3 of ZA206. For level 6, the output of ZA218B (pin 17) feeds pin 5 of ZA206. For level 7, the output of ZA219C (pin 2) feeds pin 11 of ZA206. For level 8, the output of ZA219A (pin 13) feeds pin 8 of ZA206.

7.61 Level Selection: When the tape in the reader contains only 7 levels of information, the eighth level is always read as a mark. The LEVEL SELECTION switch for the verify contacts is SWA601 which is mounted on the front plate of the HSEDC transmitter control module. When the switch is in the 7 level position, a 0-volt signal is continuously applied to the input (pin 20) of the level 8 CSS circuit on ZA215; this is always recognized as a mark and the output (pin 31) is 0 volts.

7.62 When tape with 6 levels of information is in the reader, both the seventh and eighth levels are read as marks. The LEVEL SELECTOR switch (SWA601) is in the sixth level position. A 0-volt signal is applied to the level 8 CSS circuit as described in 7.61 and is always recognized as a mark. A 0-volt signal is also applied to the input of the level 7 CSS circuit of ZA215 (pin 19) which produces a 0-volt signal at the output (pin 32) to continuously generate a mark for that level.

7.63 When tape with five levels of information is in the reader, the first level is always read as a space and the seventh and eighth levels are always read as marks. With the LEVEL SELECTOR switch (SWA601) in the five level position, marks are generated for the seventh and eighth levels as described above. The input to the level 1 CSS circuit (pin 6) of ZA215 is always open-circuited to produce a -6 volt signal at the output (pin 7) which is always recognized as a space.

F. EOB Mode Operation

7.64 When the programmer advances out of the BK mode, the BK mode signal goes to -6 volts; and, when applied to pin N of AND gate ZA419D, the signal inhibits the drive pulse generated at the end of the 80th character from going through to step the reader. The -6 volt BK mode signal is also presented to pin M of OR gate ZA405A and causes the output (pin R) to go to -6 volts. When this -6-volt signal is applied to pin E of inhibit gate ZA409D, it enables the next sample pulse to come through. The -6 volt BK mode signal applied to pin E of ZA106B inhibits gates ZA207 and no more signals from the CSS circuits for the read contacts are allowed to pass through to the transmitter distributor. Pin C of OR gate ZA421 and pin 9 of flip-flop ZA212C also go to -6 volts due to the BK mode. With the programmer in the EOB mode, the EOB mode signal goes to 0 volts. When this signal is applied to pin 35 of matrix circuit ZA205, it causes the circuit to generate the EOB character at its outputs. The EOB character signals go to terminals E1-E8 of JA128 to be presented to the inputs of the TD shift register for insertion and transmission. Refer to Table 2 (see Part 5) to determine which levels are mark and which levels are space for the EOB character.

7.65 The EOB mode 0-volt signal is applied to the input (pin H) of IPS circuit ZA512 which delays presenting the 0-volt signal at the output (pin K) for approximately 8 milliseconds. Thus, for the period of the delay, pin B of OR gate ZA421 is at -6 volts, along with the -6 volts at pin C from the BK signal, and the -6 volt signals at the other inputs which keep the output (pin J and K) at -6 volts to hold the TD start lead at -6 volts. At the end of the delay, the output of IPS circuit ZA512 (pin K) goes to 0 volts, applies this signal to pin B of ZA421, and the TD start lead goes to 0 volts and enable the transmitter distributor to start sending the next character. At a speed of 1050 wpm, this delay is not significant. The transmitter distributor finishes sending out the 80th character of the block just read. By the time the end of the character is reached, the 8 milliseconds delay is completed, the TD start lead goes to 0 volts, and the transmitter distributor immediately resets to send the EOB character. The delay is required to allow the punch at the receiving terminal to advance the last character punched to a position over the photo-reader for reading when generating the check characters at that terminal. After the end of the character and the TD start lead has gone to 0 volts, the transmitter distributor resets and the sample pulse inserts the EOB character, at the TD inputs, into the shift register. The sample pulse from the EOB character comes in to pin C of inhibit gate ZA409D, through the gate to OR gate ZA410A, which then presents the pulse to pin L of one-shot ZA411. 200 microseconds later, the programmer advances out of the EOB mode into the CK1 mode. This same sample pulse also goes to the check character generators to insert the 80th character of the block, now positioned over the verify contacts, into the registers to complete the generation of the two check characters.

7.66 When the programmer advances out of the EOB mode, the EOB mode signal goes from 0 volts to -6 volts. The negative-going transition is applied to pin H of pulse amplifier ZA406 and produces a positive-going 6-volt pulse, 10 microseconds wide, at the output (pin D) which is sent to the set 0B input (pin 23) of flip-flop ZA212B to sample the reverse channel. If no errors were detected in the previous block, the reverse channel is on, the prime 0B input (pin 22) of ZA212B is at -6 volts, and the pulse at the set 0B input is ignored. In addition, pin 35 of ZA205 goes to -6 volts and removes the EOB character signals from the inputs to the transmitter distributor and pin H of ZA512 goes to -6 volts to remove the 0-volt signal at pin B of ZA421.

G. CK1 Mode and CK2 Mode Operation

7.67 When the programmer advances into the CK1 mode, the CK1 mode signal goes from -6 volts to 0 volts. The positive transition is applied to the set 0A input (pin 4) of flip-flop ZA212C, and with the prime 0A input (pin 5) held at ground permanently, the flip-flop is set to the 0 state. The inverted output (pin 2) goes to 0 volts which inhibits gate ZA409A and prevents any further sample pulses from going into the check character generators. The 0-volt CK1 mode signal goes to pin D of OR gate ZA421 to keep the TD start lead on. The CK1 mode signal also goes to pin P of inverter ZA106D which inverts the signal and sends a -6 volt signal from pin S, through emitter follower ZA107A, to pin 36 of ZA206 to enable the horizontal check character selector gates. The outputs of the CK1 register pass through the gates and are presented to the inputs of the transmitter distributor via terminals E1-E8 of connector JA128. At the end of sending the EOB character, the transmitter distributor resets and inserts the CK1 character into the shift register. The sample pulse for the CK1 character comes in to pin C of inhibit gate ZA409D, goes through the gate, and goes through OR gate ZA410A to the input of one-shot ZA411; 200 microseconds later, the programmer advances out of the CK1 mode and into the CK2 mode.

7.68 When the CK1 mode signal goes to -6 volts, the horizontal check character selector gates are inhibited. The 0-volt CK2 mode signal goes to pin N of inverter ZA106A which inverts the signal. From pin R, the signal passes through emitter follower ZA107B which presents -6 volts to pin 1 of ZA206 to enable the spiral check character selector gates. The outputs of the CK2 register pass through the gates and present the spiral check character to the inputs of the transmitter distributor via terminals E1-E8 of connector JA128. At the end of sending the CK1 character, the transmitter distributor resets and inserts the CK2 character into the shift register. The sample pulse for the CK2 character comes in to pin C of inhibit gate ZA409D, goes through the gate, and goes through OR gate ZA410A to the input of one-shot ZA411; and, 200 microseconds later, the programmer advances out of the CK2 mode. When the programmer goes out of the CK2 mode, the CK2 mode signal goes to -6 volts, and passes through inverter ZA106A and emitter follower ZA107B, which inhibits the spiral check character selector gates.

7.69 If the reverse channel was on when it was sampled, the normal output of flip-flop ZA212B then remained at 0 volts which would prime pin K of ring reset circuit ZA412A. When the programmer advanced out of the CK2 mode, it would be reset to the BN mode. (See 7.19.) During the stepping of the reader through the previous 80-character block, the block number cam would rotate one-third of a revolution and the next higher block number contact would close to prime the control character matrix for the proper BN character. A module will now go through the operations described in 7.35 through 7.66. If no errors are detected, the reverse channel will remain on and the programmer will be reset to the BN mode from the CK2 mode every time.

H. Error Detection and Correction

7.70 The sender terminal is told an error has been detected by the removal of the reverse channel. Since the receiver does not detect the error until after the check characters are sent, the reverse channel is not detected as off until the end of the block following the errored block. When the loss of the reverse channel is detected, the sender advances into the error correction mode. The check characters are deleted; the reader reverses, backs up the tape two blocks (160 characters) to the start of the errored block, and stops; and the sender begins sending out SR characters, in this case signalling it is ready to retransmit the errored block.

7.71 Reverse Channel Off Detect: The reverse channel signal comes into the HSEDC transmitter control module through terminal A4 of connector JA128. When the reverse channel is on, the signal is -6 volts and it goes through inverter ZA106C, OR gate ZA415A, IPS circuit

ZA404, and AND gate ZA405C which presents a 0-volt signal to pin 24 of ZA212B and pin E of ZA403B. When the reverse channel goes off, the signal goes to 0 volts which then presents -6 volts to pin 24 of ZA212B and pin E of ZA403B. Inverter ZA403B then sends a 0-volt signal from the output (pin B) to the prime 0B input of ZA212B (pin 23). When the programmer advances out of the EOB mode, the pulse generated by pulse amplifier ZA406B is accepted by the set 0B input (pin 23) of ZA212B and the flip-flop is set to the 0 state; the normal output (pin 14) goes to -6 volts which inhibits ring reset circuit ZA412A and prevents the programmer from resetting to the BN mode when it advances out of the CK2 mode. The inverted output (pin 17) goes to 0 volts which is applied to pin E of AND gate ZA419A to prepare the gate to blind the transmitter distributor output.

7.72 Transmitter Distributor Blind: The programmer advances out of the EOB mode into the CK1 mode, and from the CK1 mode it advances to the CK2 mode. The CK1 mode 0-volt signal and the CK2 mode 0-volt signal, in addition to the functions described in paragraph 7.67, are applied to pins L and K, respectively, of OR gate ZA410B and present a 0-volt signal from the output (pins R and A) through emitter follower ZA418D to pin F of AND gate ZA419A. This signal, in conjunction with the 0-volt signal on pin E from the reverse channel off signal, produces a 0-volt signal at the output (pin B) which is sent through emitter follower ZA418E to pin K of OR gate ZA415B. The 0-volt signal passes through the gate, and from the output (pin R) it goes to terminal A9 of connector JA128 which sends the signal to the transmitter distributor. The signal is applied to one input of a gate in the transmitter distributor which holds the send data lead in a continuous marking condition. Since the EOB character is being sent out during the CK1 mode and the transmitter distributor is blinded right after the start of the character, the EOB character is changed to an all-mark character; and although the transmitter distributor attempts to send the CK1 character and the CK2 character, they never appear on the send data lead as long as the output of the transmitter distributor is blinded.

7.73 R1 Mode and R2 Mode Operation: When the programmer steps out of the CK2 mode, it is prevented from resetting back to the BN mode. Instead, the programmer advances into the R1 mode. In the R1 mode, the reader is reversed and backed up 80 characters. At the end of 80 characters, the programmer is advanced to the R2 mode. In the R2 mode, the reader is backed up another 80 characters; and, at the end of the second back-up, the reader is switched back to the forward direction and the programmer is reset to the SR mode. During the R1 and R2 modes, the output of the transmitter distributor is blinded which holds the send data lead marking and the TD start lead is held at -6 volts which prevents the transmitter distributor from cycling.

7.74 As soon as the programmer steps into the R1 mode, each input to OR gate ZA421 is at -6 volts which holds the TD start lead at -6 volts. The transmitter distributor finishes shifting out the last character in its register but it never resets to send further characters. When the programmer is in the R1 mode, the 0-volt signal from the R1 element is applied to pin M of OR gate ZA410B, and in the R2 mode, the R2 mode 0-volt signal is applied to pin C of OR gate ZA410C. Both signals produce a 0-volt signal at the output (pins R and A) which serves to blind the output of the transmitter distributor. In addition, the 0-volt signals from the R1 and R2 mode elements are applied to pins L and K, respectively, of OR gate ZA405A which holds pin E of ZA409D at 0 volts and inhibits that gate. Thus, only end-of-block pulses can advance the programmer.

7.75 When the programmer enters the R1 mode, a 0-volt signal is applied to pin N of OR gate ZA410D and appears on the output (pin 5), then goes in pin H of emitter follower ZA408E, and comes out on pin C. From pin C of ZA408E, the 0-volt signal goes to pin C of AND gate ZA419C to prime the gate and it also goes to pin H of power amplifier ZA422A. A 0-volt signal is produced at the output of the power amplifier (pin A) and inserted into the integrator TBA518, pin 7. The output (pin 14) goes to terminal G5 of connector JA128. From terminal G5, the signal goes to the sender station control in the sender terminal to energize the MR (motor reverse) relay. This relay switches the ac power on one winding of the reader and causes it to reverse direction. Through a normally-closed contact on the MR relay a 0-volt signal, through terminal G6 of connector JA128, holds relay KA520 energized. When the MR relay is energized, the contact breaks, the 0-volt signal is removed, and relay KA520 drops out. The 0-volt signal that occurs when the programmer is in the R2 mode comes into pin P of OR gate ZA410D which keeps 0 volts on pin H of ZA422A, holds the MR relay energized, and relay KA520 de-energized.

7.76 The 0-volt signal from pin C of emitter follower ZA408E is presented to pin C of AND gate ZA419C when the programmer is in the R1 mode and the R2 mode. Pin D of AND gate ZA419C is normally held at -6 volts through a clamp circuit on ZA424 consisting of resistor R1 and diode CR1. It takes approximately 300 milliseconds for relay KA520 to drop out. The 300-millisecond delay is used to allow the reader motor to come up to speed in the reverse direction. When the drop-out is completed, break contact 8 closes and puts 0 volts on pin D of AND gate ZA419C. This produces 0 volts at the output (pin A) which goes to pin P of inverter ZA403D whose output (pin S) goes to -6 volts. The output of ZA403D goes to the input of gated oscillator ZA423, pin P; with 0 volts on pin P, the output of ZA423 is -6 volts. When -6 volts is applied to pin P, ZA423 starts oscillating and a series of positive-going, -6 volts to 0 volts, 10-microsecond pulses appear at the output (pin A). These pulses are used to step the reader in the reverse direction. When relay KA520 drops out, transfer contacts 6 switch so the reverse end-of-block contact can come into the module for sampling. The contact signal comes in terminal G8 of connector JA128 and goes through the KA520 relay contacts to pin M of integrator circuit ZA123C. If the EOB contact is open, the output of ZA123 is -6 volts and if it is closed, the output is 0 volts.

7.77 The pulses that appear on pin A of gated oscillator ZA423 go to pin D of OR gate ZA415C, come out pin A, and go through terminal G4 of JA128 which sends the pulses to the reader driver. Each pulse causes the reader to step once. The pulses from ZA423 also go to pin L of one-shot ZA503 to generate a pulse to sample the reverse EOB contact. Each pulse on pin L triggers the one-shot and the normal output (pin J) goes to 0 volts for 2 milliseconds. At the end of 2 milliseconds, the output returns to -6 volts and this negative-going transition is applied to pin F of pulse amplifier ZA406A which produces a positive-going, 10-microsecond pulse at the output (pin N) of ZA406A. The pulse produced at pin N goes to pin D of OR gate ZA511C which passes the pulse from pin A to pin K of AND gate ZA511A to sample the EOB contact. The EOB contact is normally open and the pulses produced by ZA406A due to the 1st through 79th drive pulses are ignored. When the reader completes the 79th step, the reverse EOB contact closes. The 80th drive pulse causes the reader to step once again and the pulse generated by ZA406A, due to the 80th drive pulse, finds the reverse EOB contact closed and the pulse thus passes through AND gate ZA511A and comes out on pin R. When the reader completes the 80th step, the EOB contact opens. The pulse at pin R of AND gate ZA511A goes through emitter follower ZA509C to pin H of OR gate ZA410A, and from the output of ZA410A (pin B) to pin L of one-shot ZA411 to advance the programmer; 200 microseconds later, the programmer advances from the R1 mode to the R2 mode. The conditions that allowed the reverse stepping in the R1 mode remain the same in the R2 mode. The drive pulses continue to step the reader backward. At the end of the 80th step backwards, an EOB pulse is generated which resets the programmer from the R2 mode to the SR mode.

7.78 When the programmer steps out of the R2 mode, the 0-volt signal is removed from pin H of power amplifier ZA422A which de-energizes the MR relay in the sender station control. When the MR relay drops out, the 0-volt signal from the contact on the MR relay is reapplied to relay KA520 to pick up the relay. This switches the relay contacts from passing the reverse EOB contact closures to passing the forward EOB contact closures. When the 0-volt signal is removed from pin C of AND gate ZA419C, it prevents gated oscillator ZA423 from generating further drive pulses.

7.79 When the programmer steps into the SR mode, the output of the SR ring element, through inverter ZA104D, applies a -6 volt signal to the input of IPS circuit ZA508 (pin H). Approximately 1 second after the -6 volt signal is applied, the output of ZA508 (pin K) goes to -6 volts which is applied to pin M of inhibit gate ZA402B which produces a 0-volt signal from the output (pin L) that goes to pin L of AND gate ZA419B. As long as the terminal has not been stopped, the pulses that appear on pin M of ZA419B pass through to the TD start lead and trigger the transmitter distributor to send an SR character. The 1 second delay is to allow the motor on the reader to come up to speed when it is switched to the forward direction. Once the programmer returns to the SR mode, the HSEDC transmitter control module operates in the manner described in 7.26.

7.80 When the sender terminal is operating in the normal EDC mode, stopping the sender is accomplished by the removal of the reverse channel at the receiving terminal. This causes the HSEDC transmitter control module to back up the reader two blocks (160 characters) to return the tape to the start of the errored block. The terminal can also be stopped by the operator at the sender terminal or it can be stopped when an alarm condition occurs. The operator stops the terminal by pressing the STOP-ALARM/RESET button on the front of the sender cabinet. This causes the run/stop lead into the HSEDC transmitter control module to go off. An alarm condition such as tape-out or the failure to detect feed pulses automatically sets the circuitry that the STOP-ALARM/RESET button actuates and causes the run/stop lead into the module to go off. In addition, the signals produced by the alarm condition are recognized and cause additional actions to take place. When the terminal has been stopped by the removal of the reverse channel, the reader is backed up two blocks to the start of the errored block. When the STOP-ALARM/RESET button is pushed, it essentially introduces an error into the block being transmitted. The terminal then stops at the end of that block, and from that point the reader need only back up one block to return to the start of the errored block; it remains stopped at that point until the RESET button is pushed and the run/stop lead comes back on. When an alarm occurs, the terminal stops at the end of the block the alarm occurred in with no back-up.

7.81 When the STOP-ALARM/RESET button is pushed, the circuitry in the sender station control causes the run/stop lead to go to -6 volts. The -6 volt signal comes into the HSEDC transmitter control module and causes the EDC-run signal from the outputs of emitter followers ZA408F and ZA504-1/2 pins A and N respectively, to go to -6 volts. This signal is then applied to pin D of AND gate ZA405C to inhibit the reverse channel signal and cause it to be detected as off, even if it has remained on. When the programmer steps from the EOB mode to the CK1 mode at the end of sending a block, the programmer is primed to go into the error correction mode, and when the programmer steps out of the CK2 mode, it advances to the R1 mode. The module now causes reader to back up as described in 7.71. The -6 volt signal from pins A and N of emitter followers ZA408F and ZA504-1/2 is also applied to pin K of AND gate ZA419B and pin N of inverter ZA403A. The signal on AND gate ZA419B prevents the SR mode pulses from appearing on the TD start lead when the programmer eventually resets to the SR mode and the TD start lead remains at -6 volts and no SR characters are sent. The -6 volt signal on pin N of inverter ZA403A produces a 0-volt signal on the output (pin R) which is sent to the prime 1A input of flip-flop ZA212A. The -6 volt signal now applied to pin N of diode CR6 on ZA424 allows flip-flop ZA212A to set to the 1 state when it is told to do so. When the reader finishes backing up one block, the programmer advances from the R1 mode to the R2 mode. The R2 mode signal goes to 0 volts and this positive transition is applied to the set 1A input (pin 34) of flip-flop ZA212A and sets it to the 1 state. In the 1 state, the normal output (pin 12) goes to 0 volts and this signal is applied to pin E of OR gate ZA511B, comes out on pin B, and goes to pin D of ring reset circuit ZA413A. Pin M of ZA413A goes to -6 volts which is applied to pin F of the SR ring element ZA416A, and the programmer goes into the SR mode. The reader is only allowed to back up one block, then it is switched back to the forward direction, and the terminal stops. To start again, the STOP-ALARM/RESET button must be reset which causes the run/stop lead to go to 0 volts and the terminal begins operating as described in 7.22.

7.82 When the tape-out condition occurs at the reader, the tape-out signal into the HSEDC transmitter control module goes to 0 volts which produces a 0-volt signal at pin B of integrator ZA123E that is applied to pin M of inhibit gate ZA409B. This causes the EDC-run lead to go to -6 volts which inhibits the reverse channel and advances the programmer through to the error correction mode as described in 7.81. The 0-volt tape-out signal also goes to the prime 1B input (pin 32) of flip-flop ZA212A. When the programmer advances from the CK2 mode into the R1 mode, the R1 mode signal goes to 0 volts and this positive-going transition is applied to the set 1B input (pin 33) of ZA212A to set it to the 1 state. The normal output (pin 12) goes to 0 volts and this signal, through OR gate ZA511B and ring reset circuit ZA413A, sets the programmer to the SR mode immediately. In this case, the reader is not backed up at all. The terminal remains stopped until the alarm has been corrected.

7.83 The feed detect circuit is used to determine that the tape in the reader is actually moving during the BK mode. Since the feed hole in the tape is considerably smaller than a code hole, the sampling of the signal from the feed contact is not as reliable. Instead, the transitions on the feed contact signal are recognized as adequate indications.

7.84 The feed contact signal comes into the module on terminal F1 of connector JA128 and goes to pin H of pulse amplifier circuit ZA119B. Any negative transitions that occur on the feed contact signal, as the contact makes and breaks, produce positive-going, 10-microsecond pulses at the output of pulse amplifier ZA119B. These pulses then go to the set 0B input (pin 6) of flip-flop ZA220C; the prime 0B input (pin 7) is held at 0 volts permanently.

7.85 The BK mode signal goes to pin F of inhibit gate ZA108C. Pin A of ZA108C is tied to 0 volts so that ZA108C acts as an inverter. When the programmer is not in the BK mode, the signal at pin F of ZA108C will be -6 volts and the output pin H, will be at 0 volts. The 0 volt signal is applied to pin S of fan out gate ZA407. From pin N of fan out gate ZA407, 0 volts is applied to the inverted output pin 2 of flip-flop ZA220C and from pin P of ZA407, 0 volts is applied to the inverted output pin K, of ZA515. These signals hold the flip-flop in the 0 state and the normal outputs will be at -6 volts. The normal output pin L of ZA515 goes to pin N of emitter follower ZA509B and the output of ZA509B, pin F, goes to pin H of power amplifier ZA513A. The output of ZA513, pin A, goes to terminal F2 of connector JA128 which then ties to the input at the TO (tape out) relay TO in the station control assembly. As long as the programmer is not in the BK mode, the output of ZA515, pin L, will be at -6 volts and the lead to the relay will be essentially open-circuited and will have no effect when the programmer is in the BK mode, the signals from pins N and P of ZA407 will have no effect.

7.86 When the programmer goes to the BK mode, reader drive pulses will appear at pin A of emitter follower ZA418F. These are applied to the set 1A inputs, pin 8 and pin C of flip-flop ZA220C and ZA515. With flip-flop ZA220C in the 0 state, 0 volts from the inverted output, pin 2, is applied to the prime 1A input pin 9, of ZA220C and the flip-flop will be set to the 1 state. The normal output, pin 1, will go to 0 volts. The signal is then applied to pin M of ZA515 to prime that flip-flop. The reader drive pulse which sets ZA220C to the 1 set will be ignored by the set 1A input of ZA515. Pulses from pin D of ZA119B due to the feed contact transitions will set flip-flop ZA220C back to the 0 state and the 0 volt signal will be removed from the prime 1A input of ZA515. The next reader drive pulses will be ignored by ZA515 also. If no transitions occur from feed contact for a short time, flip-flop ZA515 will be set to the 1 state along with ZA220C. The normal output, pin L, will go to 0 volts and attempt to pull in the TO relay. When a transition does occur from the feed contact, it will reset both flip-flops ZA220C and ZA515 and the TO relay will not pull in. When the programmer steps out of the BK mode, the 0 volt signal from ZA407 will hold both flip-flops in the 0 state as described above.

7.87 If the tape in the reader has torn feed holes or the tape is jammed, no transitions occur on the feed contact. The first reader drive pulse after this occurs, sets flip-flop ZA220C to the 1 state and 0 volts is applied to the prime 1A input of ZA515. The next reader drive pulse is accepted by the set 1A input (pin C) of ZA515 and sets ZA515 to the 1 state. This causes the lead to the TO relay to go to 0 volts and pull in the TO relay. The feed alarm has now generated a tape-out alarm and the terminal responds in the manner described in 7.82.

I. Rerun Counter

7.88 General: The CK2 and R2 modes are monitored to limit the number of consecutive tape reruns through the reader to three attempts.

7.89 Three Consecutive Reruns: An error in transmission causes the transmitting control to go through its rerun cycle. A positive R2 transition on pin 7 of ZA213 is presented to pin 34 of flip-flop ZA208A. Since the inverted output of ZA208A pin 13 is at 0 volts it will prime P1A to accept the positive transition of R2 to set the flip-flop to the 1 state. The normal output pin 12 will go to 0 volts. The normal output pin 12 will now prime P0A pin 29 to accept the next positive transition of R2. The next positive transition of R2 is presented to pin 28 of ZA208A and the flip-flop is set to back to 0 state. The inverted output goes to 0 volts to prime P1A again. The positive transition of the inverted output is also applied to pin 27 of ZA208B. Because the prime P1A, pin 17 ZA208B was at 0 volts, the inverted output pin 17 will go to -6 volts. This -6 volts is then presented to pin E of inhibit gate ZA108D. Because pin 12 of ZA208A is now at -6 volts, and this signal is presented to pin C of ZA108D, no action occurs at the output pin J of ZA108D. The next positive R2 transition that occurs is presented to pin 34 of ZA208A and because P1A pin 35 is at 0 volts, the flip-flop is set to the 1 state. The normal output pin 12 goes to 0 volts. This 0 volts is then presented to pin C of ZA108D. The output pin J of ZA108D will then go positive to 0 volts and is presented to pin H of relay driver ZA513A to simulate a tape-out condition. This tape-out condition will cause an alarm and the transmitter will cease to send data. When this alarm is set, terminal A1 of JA128 will go to -6 volts. This signal is then applied to pin M of inverter ZA108B and pin N of inverter ZA108A. The inverted outputs pin L of ZA108B and pin K of ZA108A will go to 0 volts. These signals are then applied to the inverted outputs pin 13 of ZA208A and pin 17 of ZA208B to reset the flip-flop and remove the simulated tape-out condition of 0 volts from relay driver ZA513A, pin H. The tape-out relay is de-energized but the alarm is set and operator intervention is needed.

7.90 Less than Three Consecutive Reruns: The counter ZA208A and B will be set as explained in 7.89 without any change; however, the CK2 mode will now be monitored to detect resumption of good transmission. A positive CK2 transition pin 5 of ZA213 will be presented to pin 8 of ZA208C. Because prime P1A pin 9 is at 0 volts, the normal output pin 1 of ZA208C will go to 0 volts to prime P0A pin 5. If an error occurred and reverse channel was detected off, the transmitter will go to the rerun mode and the programmer will go to the R1 and then to the R2 mode. A positive transition of R2 (pin 7 of ZA213) is presented to pin 6 of ZA208C.

7.91 Since pin 7 prime P0B is permanently at 0 volts, the flip-flop is set back to the 0 state. The inverted output (pin 2) will go positive to 0 volts. The counter ZA208A and B will advance one count and not be reset even though there is a positive transition at pin 2 of ZA208C and which is presented to pin 31 of ZA208A and pin 23 of ZA208B. The flip-flops are not reset because, during the reversal modes, reverse channel is off and -6 volts is applied to pin 30 of ZA208A and pin 22 of ZA208B, both being the prime P0B for reset. The reverse channel detect signal is picked up at pin A of ZA106. After the counter is advanced the programmer in the transmitter control will attempt to resume transmission. After transmission is resumed, a positive transition of CK2 will set the ZA208C flip-flop to the 1 state. If no error occurred and reverse channel was detected on, the programmer will advance to the BN, BK, EOB and CK1 mode. The next positive transition of CK2 will be presented to pin 4 of ZA208C and because pin 5, P0A, is at 0 volts the flip-flop will be set back to the 0 state. The inverted output of ZA208C pin 2 will go to 0 volts. Because transmission is continued, reverse channel is on and this 0 volts from pin A of ZA106 is presented to pin 30 of ZA208A and pin 22 of ZA208B. Then the positive transition at pin 2 of ZA208C will be presented to pin 31 of ZA208A and pin 23 of ZA208B to reset the flip-flops to the 0 state.

7.92 The flip-flop ZA208C will continue to monitor CK2 and shift states until a R2 mode is detected to resume a rerun count. If an alarm condition occurs at any time during transmission or during counter advance, the counter will automatically be reset as operator intervention is needed.

7.93 The BK mode signal goes to pin F of inhibit gate ZA108C. Pin A of ZA108C is tied to 0 volts so that ZA108C acts as an inverter. When the programmer is not in the BK mode, the signal at pin F of ZA108C will be -6 volts and the output pin H, will be at 0 volts. The 0 volt signal is applied to pin S of fan-out gate ZA407. From pin N of fan-out gate ZA407, 0 volts is applied to the inverted output pin 2 of flip-flop ZA220C and from pin P of ZA407, 0 volts is applied to the inverted output pin K, of ZA515. These signals hold the flip-flop in the 0 state and the normal outputs will be at -6 volts. The normal output pin L of ZA515 goes to pin N of emitter follower ZA509B and the output of ZA509B, pin F, goes to pin H of power amplifier ZA513A. The output of ZA513, pin A, goes to terminal F2 of connector JA128 which then ties to the input at the TO (Tape Out) relay TO in the station control assembly. As long as the programmer is not in the BK mode, the output of ZA515, pin L, will be at -6 volts and the lead to the relay will be essentially open-circuited and will have no effect when the programmer is in the BK mode. The signals from pins N and P of ZA407 will have no effect.

7.94 When the programmer goes to the BK mode, reader drive pulses appear at pin A of emitter follower ZA418F. These are applied to the set 1A inputs, pin 8 and pin C of flip-flop ZA220C and ZA515. With flip-flop ZA220C in the 0 state, 0 volts from the inverted output, pin 2, is applied to the prime 1A input pin 9, of ZA220C and the flip-flop will be set to the 1 state. The normal output, pin 1, will go to 0 volts. The signal is then applied to pin M of ZA515 to prime that flip-flop. The reader drive pulse which set ZA220C to 1 will be ignored by the set 1A input of ZA515. Pulses from pin D of ZA119B due to the feed contact transitions will set flip-flop ZA220C back to the 0 state and the 0 volt signal will be removed from the prime 1A input of ZA515. The next reader drive pulses will be ignored by ZA515 also. If no transitions occur from feed contact for a short time, flip-flop ZA515 will be set to the 1 state along with

ZA220C. The normal output, pin L, will go to 0 volts and attempt to pull in the TO relay. When a transition does occur from the feed contact, it will reset both flip-flops ZA220C and ZA515 and the TO relay will not pull in. When the programmer steps out of the BK mode, the 0 volt signal from ZA407 will hold both flip-flops in the 0 state as described above.

J. Module Features

7.95 Non-EDC Operation: The HSEDC transmitter control module has the capability of allowing the sender terminal to operate with the EDC (error detection and correction) feature disabled. In the non-EDC mode, information is read from the tape in the reader and set into the TD shift register which then sends out a serial character. The reader is stepped after each character is sent. Only information in the tape is read and it is transmitted until the end of the tape is reached or until the terminal is stopped.

7.96 The terminal is placed in the non-EDC mode by depressing the NON-EDC button on the control panel of the sender cabinet. This causes the EDC/non-EDC lead into the HSEDC transmitter control module to go to 0 volts. The 0-volt signal is applied to pin F of inhibit gate ZA402C which prevents an EDC-run condition. The 0-volt signal also goes to the input of inverter ZA403C (pin C) which produces a -6 volt signal at the output (pin A) that goes to pin E of inhibit gate ZA402D. With tape in the reader and the terminal in the run condition, the signal going to pin C of inhibit gate ZA402D is 0 volts and causes the output (pin J) to go to 0 volts. This signal goes in pin P of emitter follower ZA408D and pin B of emitter follower ZA504-1/2 which amplify the signal and produce a 0-volt, non-EDC-run signal at the output (pin D of ZA408D and pin A of ZA504-1/2). This signal goes to pin F of OR gate ZA511B which sends a 0-volt signal from its output (pin B) to pin D of ring reset circuit ZA413A. From pin M of ZA413A, a -6 volt signal goes to pin F of the SR ring element (ZA416A) to hold the programmer in the SR mode and prevent it from advancing to any other mode. The programmer stays locked in the SR mode as long as the non-EDC-run signal is at 0 volts. The 0-volt non-EDC-run signal also goes to pin K of AND gate ZA407B.

7.97 The sender terminal requires the reverse channel signal to operate in the non-EDC mode. When the reverse channel comes on, a 0-volt signal comes from pin K of IPS circuit ZA404 and goes to pin L of AND gate ZA407B; and with 0 volts on pin K, the output of ZA407B (pin R) goes to 0 volts. The 0-volt signal goes through emitter follower ZA408A which sends it to pin N of OR gate ZA415D to produce an artificial BK mode signal. The BK mode signal causes the TD start lead to go to 0 volts and the transmitter distributor starts setting characters into the shift register for transmission. The BK mode signal also enables the inhibit gates on ZA207 to allow the characters sent from the tape to pass through to the transmitter distributor inputs. The terminal and the HSEDC transmitter control module now operates as if the programmer was in a perpetual BK mode; and, although EOB advance pulses are generated every 80 characters, they are ignored.

7.98 The terminal is stopped when the non-EDC-run lead goes to -6 volts. This would be caused by a tape-out condition or by the run/stop lead going to -6 volts when the operator pushes the STOP-ALARM/RESET button. The terminal can also be stopped by the removal of the reverse channel. This would remove the artificial BK mode signal which would prevent further characters from being sent. The programmer, however, would still remain locked in the SR mode.

7.99 Reverse Channel Simulate: Proper operation of the HSEDC transmitter control module and the sender terminal requires the use of the reverse/channel. If the reverse channel feature is not provided for the terminal, the REVERSE CHANNEL SIMULATE switch SWA501 on the front panel of the HSEDC transmitter control module will provide an artificial reverse channel. However, use of this switch forbids operation of the terminal in the EDC mode since there is no means for a distant receiver to communicate that an error has occurred. However, this switch can be used to great advantage when testing the EDC operation locally. Another switch, located in the transmitter distributor module, also provides a reverse channel on condition. The output of the switch comes into the HSEDC transmitter control module on terminal A3 of connector JA128 and goes to pin H of OR gate ZA415A. The output of switch SWA501 also goes to pin H of ZA415A, and so both switches essentially perform the same function. When either switch is placed in the ON position, a 0-volt signal is applied to pin H of ZA415A which causes pin K of IPS circuit ZA404 to go to 0 volts after 20 milliseconds and produce the reverse channel on signal. When the terminal is operating in the non-EDC mode and the reverse channel feature is not provided, it is preferred that the switch in the transmitter distributor be used to simulate reverse channel. In any other circumstance, it will be more desirable to use switch SWA501 in the HSEDC transmitter control module to simulate the reverse channel on condition.

7.100 Logic Reset: Pushbutton switch SWA301 is provided on the module front panel for logic reset. Pushing the button applies 0 volts to pin E of OR gate ZA511B which resets the programmer to the SR mode immediately and holds the programmer in the SR mode for as long as the button is pushed.

7.101 Program Test: Two switches are provided on the front panel of the module to test the programmer and associated circuitry. The programmer will operate in the manner described in 7.15 except that the advance pulses are generated manually. PROGRAM TEST toggle switch SWA401 transfers the electronics into the program test mode by breaking the lead from pin B of ZA410A to pin L of ZA411 to prevent the normal advance pulses from coming in to step the programmer. Switch SWA401 then connects the output of IPS circuit ZA510 to pin L of one-shot ZA411. PROGRAM ADVANCE pushbutton switch SWA402 generates the pulses to manually step the programmer. Resistor R6 on ZA424 provides a negative bias voltage to the input of IPS circuit ZA510. When switch SWA402 is pushed, it allows a 0-volt signal to pass through the switch to pin H of ZA510; 500 microseconds later, the output of ZA510 goes to 0 volts and the positive transition triggers one-shot ZA411 and causes the programmer to advance. Each time the PROGRAM ADVANCE switch is pushed, the programmer advances to the next mode. When the PROGRAM TEST switch is thrown back to the OFF position, normal operation can proceed.

7.102 Reader Test: A READER TEST switch SWA302 on the HSEDC transmitter control module front panel is provided to test the reader signal contacts. In the reader test mode the signals from the verify contacts are compared to signals from the read contacts. During the test mode, an artificial reverse channel signal is provided. In addition, the terminal must be prepared to operate in the EDC mode. The comparison of the contact signals is done on a character-by-character basis during the BK mode. When an error is detected, the reverse channel is turned off and the reader stops at the end of the block, backs up, and stops. An indication of the error is given. During the reader test mode, the output of the terminal is held marking.

7.103 Flip-flop ZA219B is used to provide the error indication. When READER TEST switch SWA302 is in the OFF position, a 0-volt signal is applied to the inverted input of ZA219B and the normal output is -6 volts. The -6 volt signal is applied to pin N of inhibit gate ZA402A; but since the emitter input (pin D) is open, the output of ZA402A is -6 volts. In the OFF position of the switch, resistor R2 and diode CR2 clamp pin D of AND gate ZA407C and pin L of OR gate ZA415B to -6 volts. When the READER TEST switch is thrown to the ON position, a 0-volt signal is applied to pin D of inhibit gate ZA402A which causes the output (pin K) to go to 0 volts and this signal goes to pin F of OR gate ZA415A to provide a reverse channel on signal. The 0-volt EDC-run signal goes through switch SWA302 to pin D of AND gate ZA407C to prime the gate and it is also applied to pin L of OR gate ZA415B to blind the output of the transmitter distributor during the test mode.

7.104 The comparing of the signals from the contacts of the reader is done in the horizontal check character generator. The output of each element of the check character generator goes to one of the inputs of OR gate ZA122, pins M, L, F, E, D, C, B, and A, for elements 1 through 8 of the generator and the output of the OR gate is sampled for a wrong
→comparison. To sample the output of OR gate ZA122 and the sample pulse also goes to one-shot ZA506 to generate a pulse to set the signal from the read contacts into the check character generator. These pulses are generated only during the BK mode.

7.105 The output of OR gate ZA122 (pins J and K) goes through emitter follower ZA509F to the prime 1A input (pin 26) of flip-flop ZA219B. If an error in reading occurred, this input is at 0 volts when sampled and the flip-flop is set to the 1 state to indicate the error.

7.106 The sample pulse goes into pin L of one-shot ZA505 and if the programmer is in the BK mode, pin K is at 0 volts and the normal output (pin J) of the one-shot goes to 0 volts for 200 microseconds. When the output returns to -6 volts, the negative transition applied to pin H of pulse amplifier ZA507B produces a positive-going, 10-microsecond pulse at pin D which goes to the set 1A input (pin 27) of flip-flop ZA219B to sample the outputs of the check character generator for an error.

7.107 The sample pulse at pin J of one-shot ZA505 is used to generate the "Read Gates" signal. At the end of the 200 microseconds pulse, the output (pin J) returns to -6 volts and the negative-going transition applied to pin F of pulse amplifier ZA507A produces a positive-going, 10-millisecond pulse at the output (pin N) to sample the read contact signals. This pulse goes to pin C of AND ZA407C and appears at the output, pin A. From the output of ZA407C, the pulse goes through emitter follower ZA408B to pin B of inverter ZA116-1/2 which sends a negative-going pulse from its output (pin K) through emitter follower ZA117-1/2 to pin 1 for the base inputs of a second set of inhibit gates on ZA216.

7.108 When the programmer enters the BK mode, the elements in the horizontal check character generator are set to the 0 state and the output of OR gate ZA122 is at -6 volts. The next sample pulse which comes into the module generates a pulse to sample the output of OR gate ZA122 200 microseconds later; since the generator elements are still in the 0 state, it is ignored. At the same time, the read gate pulse samples the signals from the reader read contacts. These signals come into the module through terminals C1-C8 of connector JA128 and they go to pins 35, 32, 24, 26, 3, 5, 11, and 8 of the second set of inhibit gates on ZA216. If the signal for a particular level is marking, the read gate pulse at the output of the gate sets the check character generator element for that level to the 1 state. The reader then steps and moves the 1st character from over the read contacts to a position over the verify contacts and the 2nd character is moved over read contacts. The first sample pulse is prevented from looking at the verify contact signals in the manner described in 7.48. The next sample pulse into the module examines the verify contact signals and a mark pulse is generated for each level that is marking. The character on the verify contacts should be the same as the one read previously on the read contacts and mark pulses should be generated for the same levels. These pulses set the generator elements back to the 0 state. The elements for the levels that were spacing should still be in the 0 state. 200 microseconds later, the pulse generated by one-shot ZA505 goes to the set 1A input of ZA219B, but if all the check character generator elements are in the 0 state, the prime 1A input is at -6 volts and no error is recorded. Then, at the same time, a read gate pulse sets the second character from the read contacts into the check character generator and the tape then steps. The next sample pulse reads this same character from the verify contacts and sets the generator elements back to the 0 state. When the output of the OR gate ZA122 is sampled, no error is recorded if all the elements are in the 0 state. This comparison continues for 80 characters until the end of a block. If no error is recorded, the programmer is reset to the BN mode from the CK2 mode and the next block is compared.

7.109 If the character read by one set of contacts does not agree with the character read by the other set of contacts, one or more of the generator elements is in the 1 state and the output of OR gate ZA122 is 0 volts which primes the P1A input of flip-flop ZA219B. When the pulse comes into the set 1A input, flip-flop ZA219B is set to the 1 state and the normal output (pin 14) goes to 0 volts. The 0-volt signal goes to pin N of inhibit gate ZA402A which causes the output (pin K) to go to -6 volts and turns off the reverse channel. At the end of the block, the programmer goes through the error correction mode, resets to the SR mode, and operation stops. The error is recorded, although the exact character in error is unknown. To reset, READER TEST switch SWA302 must be returned to the OFF position. If the test can proceed for several minutes with no error recorded, it can be assumed the reader contacts are good. If an error is recorded frequently, a closer examination of the signals for each contact is required.

7.110 Indicator Lights: Indicator lights are provided on the front panel of the module for a visual indication of the state of important circuits in the module. A 0-volt signal to each lamp causes it to light and a -6 volt signal to the lamp keeps it off. The first row of lights (DSA101) is connected to the outputs of the elements in the programmer; the second row of lights (DSA102) goes to the outputs of the CK1 horizontal check character register; and the third row of lights (DSA201) goes to the outputs of the CK2 spiral check character register. The LOGIC RESPONSE lights in the fourth row (DSA202) go to various points in the module for an indication of logic response: the RC light goes to pin E of OR gate ZA415A to indicate the reverse channel on signal; the RCD light goes to pin 14 of flip-flop ZA212B to indicate that the reverse channel has been detected; and the RTA light goes to pin 14 of flip-flop ZA219B to indicate that a reader test error has been recorded. BN1, BN2, and BN3 BLOCK NUMBER lights go to pins R, B, and A of inverters ZA104A, ZA104B, and ZA104C to indicate which block number will be transmitted when the programmer is in the BN mode.

7.111 DC Power: No power supply is provided in the module. Power for the circuits comes into the module on row H of connector JA128. The following list shows the terminals for each voltage.

TERMINAL	VOLTAGE
H1	Frame Ground
H2	Signal Ground
H3	Circuit Ground
H4	+6 volts dc
H5	-6 volts dc
H6	-12 volts dc
H7	-48 volts dc
H8	+50 volts dc
H9	1 volt ac (For Indicator Lights)
H10	1 volt ac (For Indicator Lights)

8. TRANSMITTER DISTRIBUTOR MODULE

DESCRIPTION

A. General

8.01 The function of the transmitter distributor module (Figure 16) is to convert the parallel signals from the sender EDC electronics into serial form for transmission. The module also determines the timing for the electronics in the sender, provides for the operation of the reader, and supplies the dc power required for operation of the electronics.

B. Input and Output Signals

8.02 The basic input to the transmitter distributor module is 8 levels of parallel data representing either data information read by the reader from paper tape or control characters generated by the HSEDC transmitter control module. A 0-volt signal on an input lead indicates a marking condition and a -6 volt signal indicates a spacing condition.

8.03 The output of the transmitter distributor (TD) module is a 10.0-unit start-stop serial code alternating between -6 volts for a space and 0 volts for a mark. The output of the TD is synchronous by bit and asynchronous by character, meaning the stop pulse of a character may be any integral number of bits in length.

C. Operational Features

8.04 The transmitter distributor module operates at a speed of 105 characters per second which is derived internally by a tuning fork oscillator; 5, 6, 7, or 8 code levels may be used.

8.05 The transmitter distributor module functions in conjunction with controls and indicators located on the cabinet of the sender. Its operation, however, is controlled by the HSEDC transmitter control module of the sender.

8.06 The TD module requires 117 vac (±10%) at 60 Hz (±.75%). The power supplies in the TD module produce dc power capable of handling the electronics in the transmitter distributor module, the HSEDC transmitter control module, and the sender station control of the sender.

8.07 All signal and voltage connections to the module are made through a connector mounted in the frame. In addition, a second connector in the frame provides a direct interface with the reader.

8.08 The transmitter distributor module contains a multivoltage power supply and a 48-volt power supply to provide dc power to the electronics.

8.09 The transmitter distributor module is able to accept the vertical parity accessory available with the sender. It requires the addition of one circuit card to the existing electronics. With the accessory provided, odd or even parity can be selected with a switch on the module. It causes a parity bit to be inserted into the unused 8th level of any 5, 6, or 7 level tape.

OPERATION

A. General

8.10 The primary function of the transmitter distributor module is to convert the 8-level parallel character signals presented at its

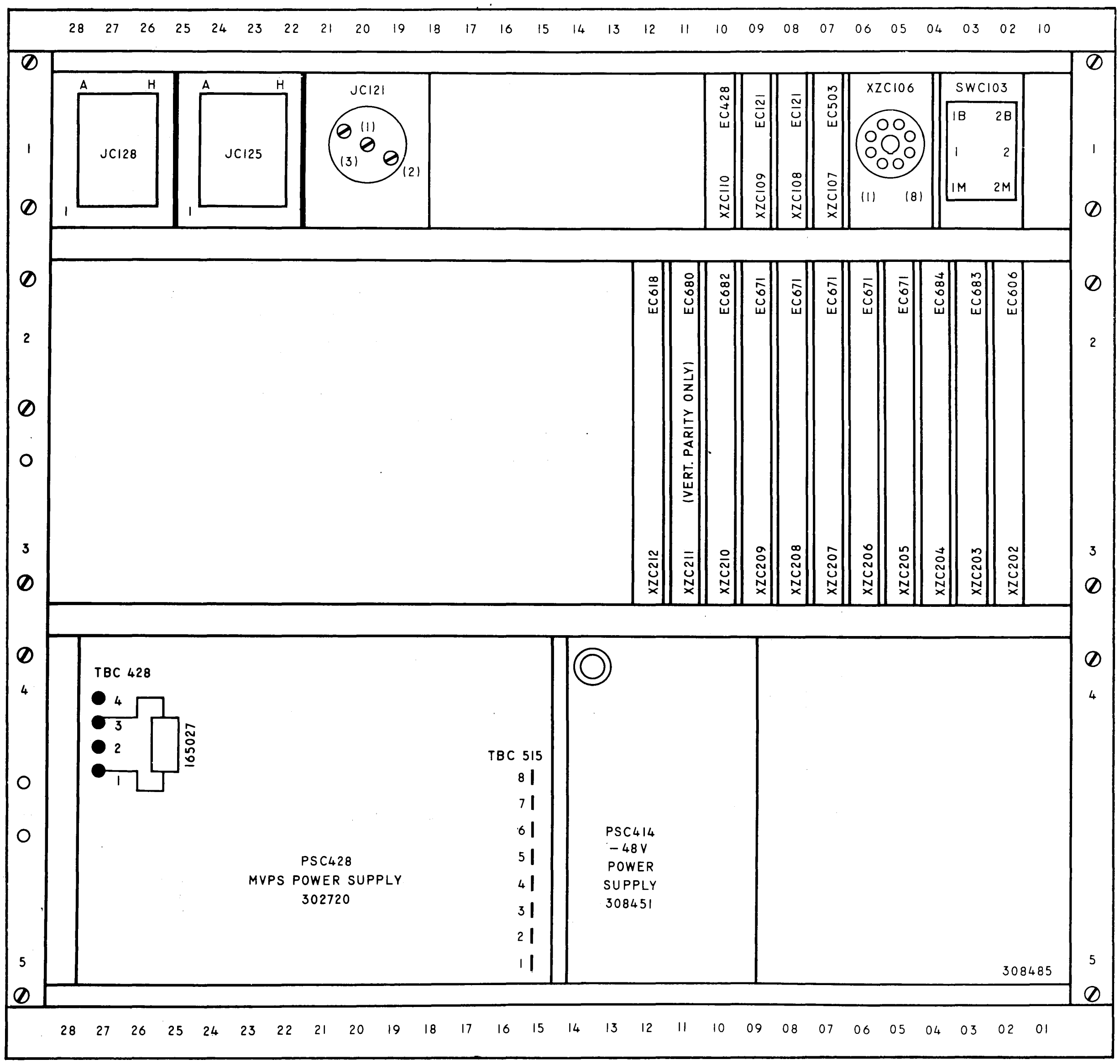

Figure 16 - High Speed Transmitter Distributor, Module C, Left Side View

inputs by the HSEDC transmitter control module into serial signals suitable for transmission. The actual serialization of each character presented to the TD module is performed by a shift register in the module. A block diagram of the shift register and some of its control logic is shown in Figure 17. The remainder of the register control logic and the logic for the transmitter distributor is shown in Figure 18. Refer to 7410WD, the schematic wiring diagram for the TD module, for a more detailed illustration of the transmitter distributor logic.

B. Shift Register Operation

8.11 Whenever a character is inserted into the shift register, the register shifts that character out until the state of the register is a mark in the first element and a space in the rest

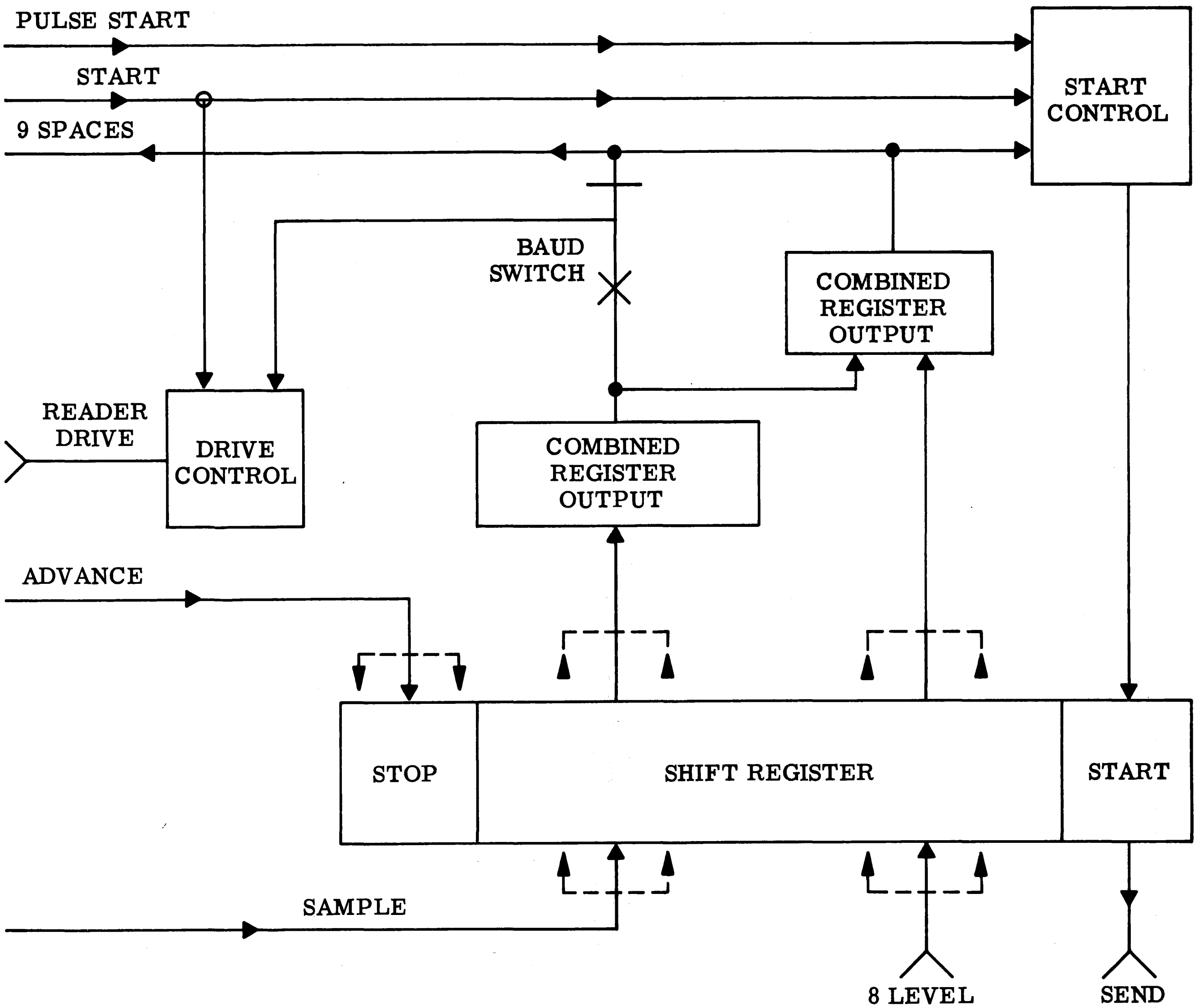

Figure 17 - Transmitter Distributor Shift Register

of the elements. A mark in the first element indicates a stop bit on line and this stop bit can be present for any length of time. The register stays in the above state until it receives an indication to start and transmit another character. The start indication causes a space to be inserted into the first element of the shift register. The space in the first element is the start bit of the new character. Half a bit after the start of the start bit, the new character is inserted into the register and a mark is inserted into the last element of the register. The character is then shifted out of the register, bit by bit, until the mark that was in the last element is in the first element, indicating the stop bit of the character. If the start indication is still present at the end of the character, the stop signal is only one bit long and the next character is inserted into the register for serializing.

8.12 Clock timing for the transmitter distributor is shown in timing diagram Figure 19. The output of tuning fork oscillator ZC106 is a square wave alternating between -6 volts and 0 volts with a frequency of 1050 Hz. This signal is applied to pin E of pulse amplifier ZC108B. Only the negative-going transitions of the signal are accepted by ZC108B and each

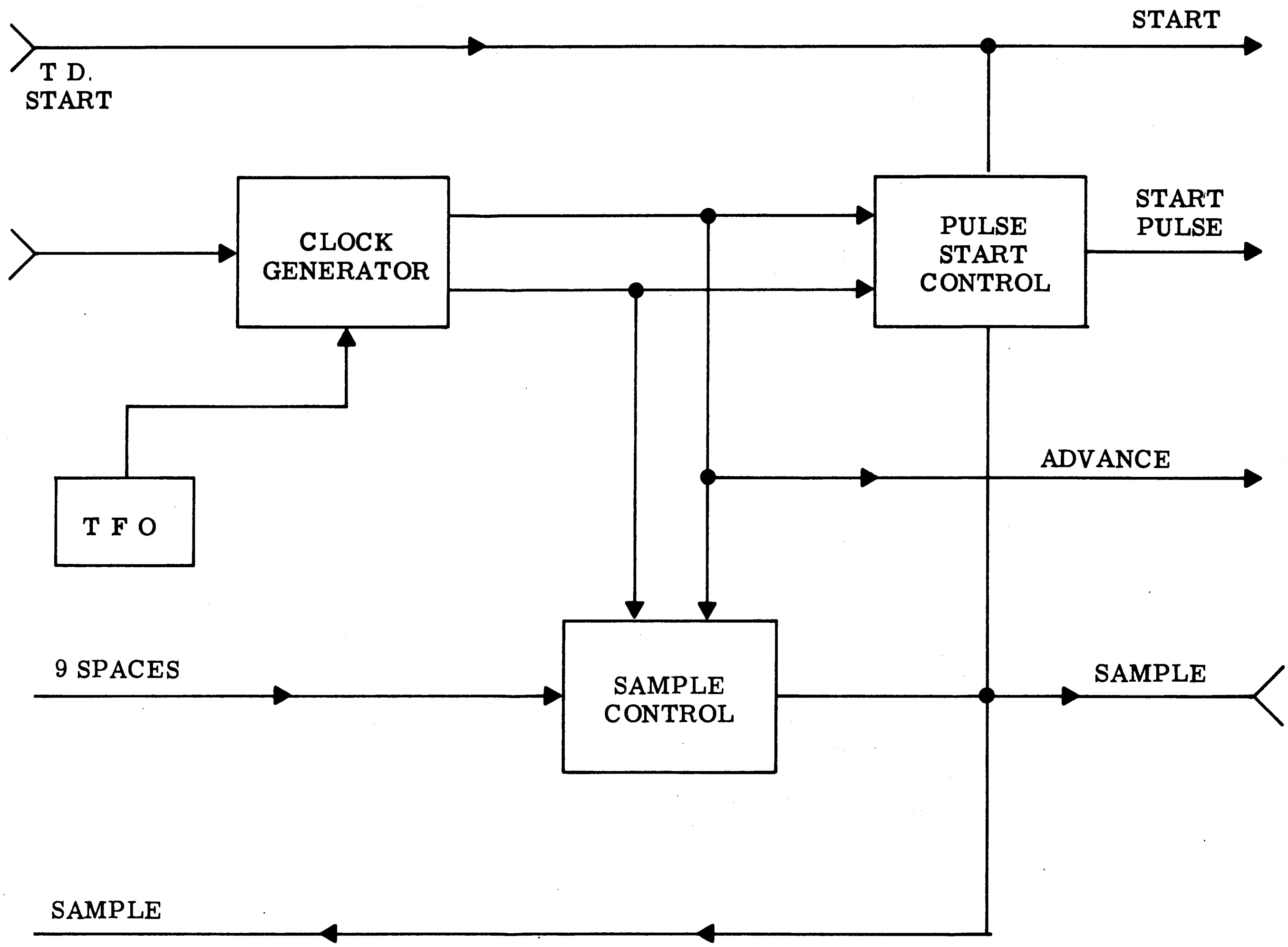

Figure 18 - Transmitter Distributor Register Control

transition produces a positive-going, -6 volts to 0 volts, 10-microsecond pulse at the output (pin B). This stream of pulses is called the HB (half bit) clock. The square wave signal is also applied to pin 5 of inverter ZC203B and an inverted square wave signal is sent from pin 7 of ZC203B to pin C of pulse amplifier ZC108A. The negative-going transitions at pin C, corresponding to the positive transitions of the signal from the tuning fork oscillator, produce a stream of positive-going, -6 volts to 0 volts, 10-microsecond pulses at pin A of ZC108A. These pulses are called advance pulses. At 1050 Baud, the time between successive advance pulses and between successive HB clock pulses is 0.952 milliseconds. Since the clock sources used by the sender are free-running, advance pulses and HB clock pulses are continually produced.

8.13 The start indication to the shift register is derived from the TD start lead from the HSEDC transmitter control module in the sender. The TD start signal may be either a pulse or a steady on signal. If the signal is a pulse, it indicates the transmitter distributor is to send one character and then wait until another

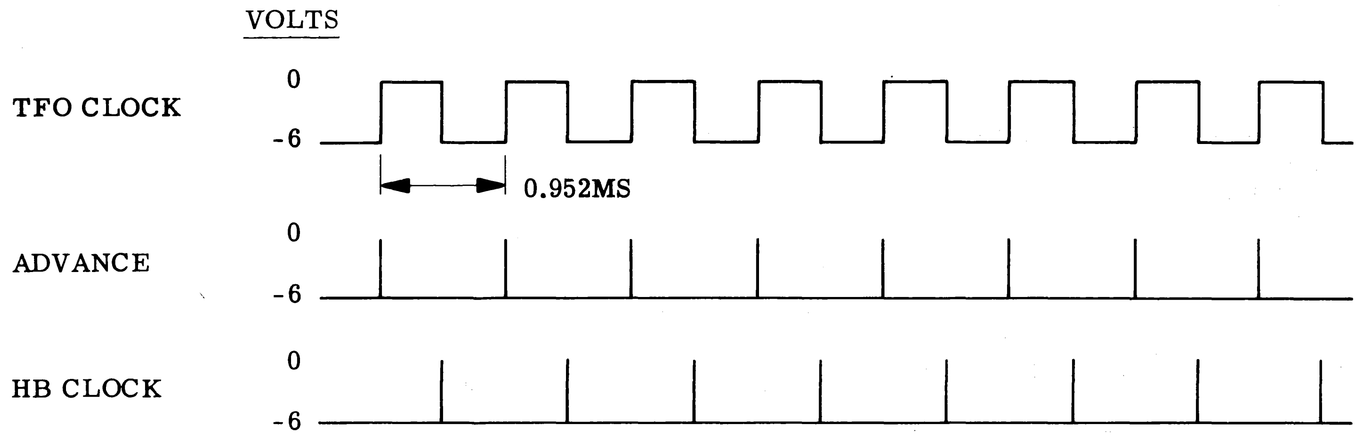

Figure 19 - Transmitter Distributor Clock Signal Timing (1050 Baud)

signal to start comes in. A steady on signal on the TD start lead means the transmitter distributor is to start sending characters and to continue sending characters until the TD start lead goes off.

8.14 The TD start lead comes into the transmitter distributor module on terminal B9 of connector JC128 and goes to pin 31 of INH gate ZC203J. The output ZC203J (pin 29) goes to the input of (pin 34) of INH gate ZC203K. The output of ZC203K (pin 32) produces the TD start indication. The TD start lead is normally at -6 volts which produces a -6 volt signal at the output of ZC203K (pin 32). This signal is applied to pin 6 of OR gate ZC204B, will inhibit that input of the OR gate and prevent the shift register from starting. The signal from the output of INH gate ZC203K is also applied to the pulse start detect flip-flop ZC205C and -6 volts will prevent the flip-flop from setting. The flip-flop is normally in the 0 state and the normal output (pin 1) is at -6 volts. The -6 volt signal from the normal output of ZC205C is applied to pin 7 of OR gate ZC204B, and through the OR gate, prevents the shift register from starting.

8.15 The pulse start detect flip-flop is used to detect the presence of a pulse on the TD start lead and to give a pulse start indication to the shift register. Since a pulse indicates the transmitter distributor is to send only one character, the pulse start indication must be removed after the start of sending a character so the shift register will stop at the end of the character. The pulses that appear on the TD start lead are positive-going, -6 volts to 0 volts, 10-microsecond pulses. A pulse coming in is applied through INH gates ZC203J and ZC203K to the 1A input (pin 8) of flip-flop ZC205C. Since the prime 1A input (pin 9) is permanently held at 0 volts, the flip-flop is set to the 1 state and the normal output (pin 1) goes to 0 volts. The 0-volt signal is applied to pin 7 of OR gate ZC204B and a 0-volt signal is sent from the output of ZC204B which primes the shift register to start the next character. The character begins when an advance pulse occurs and the HB clock pulse that follows causes sample flip-flop ZC205A to generate a sample pulse. An explanation of the operation of the shift register and the generation of the sample pulse is given later but it is sufficient to say now that the sample flip-flop goes to the 1 state when the sample pulse is generated. The normal output of sample flip-flop ZC205A (pin 12) goes to 0 volts and this signal is applied to the prime 0B input (pin 7) of pulse start detect flip-flop ZC205C. The advance pulses are always applied to the set 0B input (pin 6) of the pulse start detect flip-flop; and the advance pulse that occurs after the generation of the sample pulse is accepted by the set 0B input and flip-flop ZC205C sets back to the 0 state and the normal output goes to -6 volts. This removes the pulse start indication from OR gate ZC204B but the shift register maintains itself until the end of the character is reached. See the timing diagram in Figure 20.

8.16 When the TD start lead goes to 0 volts, it indicates the transmitter distributor is to begin sending characters and to continue sending the characters for as long as the on signal remains. The positive transition that occurs when the TD start lead goes to 0 volts causes the pulse start detect circuit to react in

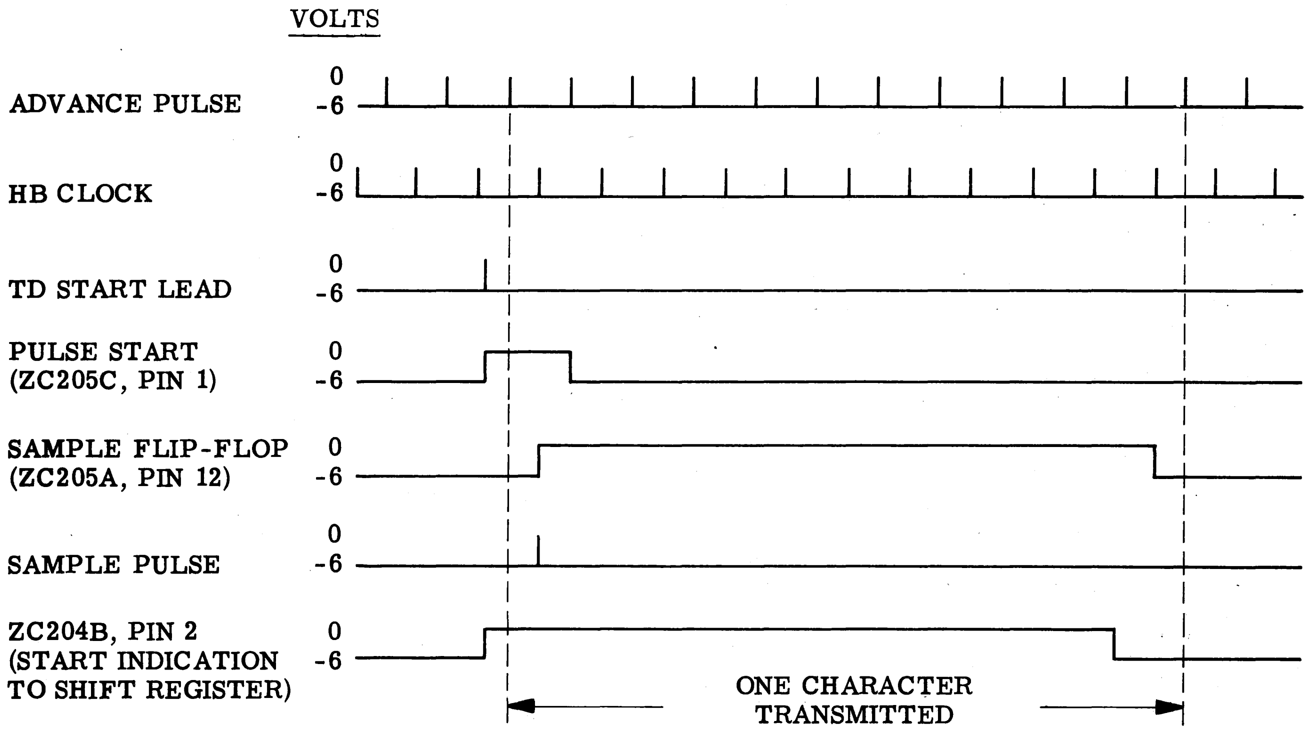

Figure 20 - Pulse Start Detect Timing

the manner described in 8.15 and a 0-volt signal is applied to pin 7 of OR gate ZC204B. The 0-volt start signal is applied to pin 6 of OR gate ZC204B. Both signals into the OR gate ZC204B have the same effect and a 0-volt signal is sent from the output (pin 2) of ZC204B which primes the shift register to start sending characters. After the start of the first character, the pulse start detect circuit is reset and the signal to pin 7 of ZC204B goes to -6 volts. The 0-volt start signal is still applied to pin 6 and at the end of the character, the shift register is primed to continue and send the next character. As long as the start signal remains on, the transmitter distributor continues to send characters, one after another.

8.17 The shift register in the transmitter distributor module consists of 10 flip-flops designated R0 through R9 which are made up of flip-flops ZC206A, ZC207A, B, and C; ZC208A, B, and C; and ZC209A, B, and C. Element R0 (ZC206A) stores the start bit of each parallel character and the normal output produces the serial character signal. Element R9 (ZC209A) stores the stop bit of each parallel character and elements R1 through R8 store the 1st through 8th levels of the actual character prior to its being shifted out of the register. The actual insertion of a character into the shift register is accomplished by sample flip-flop ZC205A which is indirectly controlled through the shift register by the start signal and pulse start detect flip-flop ZC205C.

8.18 The initial state of the shift register is considered as being a mark in the first element (R0) and a space in the remainder of the elements (R1 through R9). If the register is not in this state when power is first turned on, the register cycles until a mark reaches the R0 element and there is a space in each of the other elements. Circuitry in the sender station control prevents the partial character from being transmitted.

8.19 When an element of the shift register is in the 0 state, it indicates a space in the element, the normal output is at -6 volts, and the inverted output is at 0 volts. When an element is in the 1 state, it indicates a mark in the element, the normal output is at 0 volts, and the inverted output is at -6 volts. With a space in each of elements R1 through R9, the normal output of each element is at -6 volts; these signals, through OR gates ZC204H and ZC204G, produce a -6 volt signal at pin 8 of OR gate ZC204B. With no start indication, the other inputs to OR gate ZC204B are at -6 volts and a -6 volt signal is sent from the output of ZC204B (pin B) to inhibit AND gate ZC204F. This prevents the space in element R1 from being shifted into element R0 and the register remains in its initial condition.

8.20 The inverted output of element R9 (ZC209A) is pin 13 which is connected to the prime 0B input (pin 22) of element R8 (ZC209B) to allow a space to advance from element R9 to element R8. The normal output (pin 12) of element R9 is connected to the prime 1B input (pin 24) of element R8 (ZC209B) to allow a mark to advance from element R9 to element R8. The normal output of R9 is also connected to input pin 30 of OR gate ZC204H.

8.21 The inverted output (pin 17) of element R8 (ZC209B) is connected to the prime 0B input (pin 7) of element R7 (ZC209C) to allow a space to advance from element R8 to element R7. The normal output (pin 14) of element R8 is connected to the prime 1B input (pin 21) of element R7 to allow a mark to advance from element R8 to R7. The normal output of R8 is also connected to input pin 29 of OR gate ZC204H.

8.22 The inverted output (pin 2) of element R7 (ZC209C) is connected to the prime 0B input (pin 30) of element R6 (ZC208A) to allow a space to advance from R7 to R6. The normal output (pin 1) of R7 is connected to the prime 1B input (pin 32) of element R6 to allow a mark to advance from R7 to R6. The normal output of R7 is also connected to input pin 28 of OR gate ZC204H.

8.23 The inverted output (pin 13) of element R6 (ZC208A) is connected to the prime 0B input (pin 22) of element R5 (ZC208B) to allow a space to advance from R6 to R5. The normal output (pin 12) of R6 is connected to the prime 1B input (pin 24) of R5 to allow a mark to advance from R6 to R5. The normal output of R6 is also connected to input pin 27 of OR gate ZC204H.

8.24 The inverted output (pin 17) of element R5 (ZC208B) is connected to the prime 0B input (pin 7) of element R4 (ZC208C) to allow a space to advance from R5 to R4. The normal output (pin 14) of R5 is connected to the prime 1B input (pin 21) of element R4 to allow a mark to advance from R5 to R4. The normal output of R5 is also connected to input pin 26 of OR gate ZC204H.

8.25 The inverted output (pin 2) of element R4 (ZC208C) is connected to the prime 0B input (pin 30) of element R3 (ZC207A) to allow a space to advance from R4 to R3. The normal output (pin 1) of element R4 is connected to the prime 1B input (pin 32) of element R3 to allow a mark to advance from R4 to R3. The normal output of R4 is also connected to input pin 25 of OR gate ZC204H.

8.26 The inverted output (pin 13) of element R3 (ZC207A) is connected to the prime 0B input (pin 22) of element R2 (ZC207B) to allow a space to advance from R3 to R2. The normal output (pin 12) of element R3 is connected to the prime 1B input (pin 24) of element R2 to allow a mark to advance from R3 to R2. The normal output of R3 is also connected to input pin 33 of OR gate ZC204G.

8.27 The inverted output (pin 17) of element R2 (ZC207B) is connected to the prime 0B input (pin 7) of element R1 (ZC207C) to allow a space to advance from R2 to R1. The normal output (pin 14) of element R2 is connected to the prime 1B input (pin 21) of element R1 to allow a mark to advance from R2 to R1. The normal output of R2 is also connected to input pin 32 of OR gate ZC204G.

8.28 The inverted output (pin 2) of element R1 (ZC207C) is connected through AND gate ZC204F to the prime 0B input (pin 30) of element R0 (ZC206A) to allow a space to advance from R1 to R0 if a start indication to the shift register is present at the second input to the AND gate. The normal output (pin 1) of element R1 is connected to the prime 1B input (pin 32) of element R0 to allow a mark to advance from R1 to R0. The normal output of R1 is also connected to input pin 31 of OR gate ZC204G.

8.29 The output of OR gate ZC204H is pin 35 which is connected to input pins 2 and 22 of emitter followers ZC202P and F. If there is a mark in one or more of elements R4 through

R9, one or more of the inputs to OR gate ZC204H is at 0 volts and the output of ZC204H is at 0 volts. If there is a space in each of the elements R4-R9, the outputs of ZC202P and F are -6 volts. The signal on the outputs of ZC202P and F (pins 5 and 25) then feeds pin 34 of ZC204G. If the signal is 0 volts, then the output (pin 36) of OR gate ZC204G is 0 volts. If the signal is -6 volts, then the signals on the other inputs of ZC204G determine what the output of ZC204G is. A mark in one or more of elements R1-R3 puts 0 volts on one or more of input pins 31, 32, and 33, and the output of ZC204G is 0 volts. If there is a space in each of the elements R1-R3 and pin 34 is at -6 volts, then the output of ZC204G (pin 36) is -6 volts. The output of ZC204G goes to the inputs of emitter followers ZC202A and ZC202J, pins 29 and 9. A 0-volt signal into the emitter followers produces 0 volts at the outputs (pins 19 and 17) and a -6 volt signal into the emitter followers produces -6 volts at the outputs. The 0-volt signal applied to pin 8 of OR gate ZC204B puts 0 volts at the output (pin 2) of ZC204B and primes AND gate ZC204F to allow a character to advance out of the shift register. The -6 volt signal from the outputs of emitter followers ZC202A and J produces the 9 spaces condition that is described later.

8.30 When the start signal comes on or when the pulse start signal comes on, pin 2 of OR gate ZC204B goes to 0 volts and the 0-volt signal is applied to pin 19 of AND gate ZC204F. With a space in element R1, the inverted output of ZC207C (pin 2) is at 0 volts and this signal is sent to pin 20 of AND gate ZC204F. With 0 volts on both inputs, the output of ZC204F (pin 23) goes to 0 volts and applies this signal to the prime 0B input (pin 30) of the R0 element (ZC206A). The advance pulses generated by the clock source are always applied to the set 1B and set 0B inputs of elements R0 through R8 and to the set 0B input of element R9. The first advance pulse that occurs after the start of pulse start indication comes on and the prime 0B input to element R0 goes to 0 volts, is accepted by the set 0B input (pin 31) of element R0 (ZC206A) and a space is inserted into the R0 element. The R0 element is set to the 0 state and the normal output (pin 12) goes to -6 volts and the inverted output (pin 13) goes to 0 volts. Since the normal output of element R0 represents the data in serial form, the space in the R0 element indicates the start bit of the character to be sent.

8.31 Prior to receiving the start indication, elements R1-R9 were in the 0 state of spacing and the normal output of each element was at -6 volts. These -6 volt signals, combined through emitter followers ZC202P and F and ZC204G, produce a -6 volt signal at the outputs of emitter followers ZC202A and ZC202J (pins 19 and 17). The -6 volt signal from the emitter followers ZC202A and ZC202J indicates the 9 spaces signal. This signal is applied to pin 14 of inverter ZC203D and produces a 0-volt signal at the output (pin 12) of ZC203D which is sent to pin N of AND gate ZC107C and pin K of AND gate ZC107D to prime those gates. With a mark still in element R0, the normal output of the R0 element is 0 volts and this signal applied to pin P of AND gate ZC107C produces a 0-volt signal at the output (pin S) which is sent to the prime 0A input (pin 29) of sample flip-flop ZC205A to allow flip-flop ZC205A to be set to the 0 state by one of the HB clock pulses. The sample flip-flop ZC205A is thus in the 0 state at the start of the character to be sent, the inverted output (pin 13) is at 0 volts, and the normal output (pin 12) is at -6 volts. The advance pulse that occurs after a start signal comes on sets a space into the R0 element and the normal output goes to -6 volts and the inverted output goes to 0 volts. The 0-volt signal from the inverted output of the R0 element is applied to pin M of AND gate ZC107D and since the 9 spaces signal still exists, pin K is at 0 volts and the output of ZC107D (pin R) goes to 0 volts and produces the 10 spaces signal.

8.32 The 0-volt 10 spaces signal is applied to the prime 1A input (pin 35) of sample flip-flop ZC205A, and it is also applied to the prime 1B input (pin 32) of the R9 element (ZC209A). The HB clock pulses are always applied to the set 1B input (pin 33) of the R9 element (ZC209A), the set 1A input (pin 34), and the set 0A input (pin 28) of the sample flip-flop ZC205A. The HB clock pulse which occurs after the 10 spaces signal is established, is accepted by the set 1B input (pin 33) of the R9 element and the R9 element is set to the 1 state, indicating a mark. The normal output goes to 0 volts and the inverted output goes to -6 volts. The same HB clock pulse is accepted by the set 1A input (pin 34) of sample flip-flop ZC205A and the sample flip-flop is set to the 1 state. The normal output (pin 12) goes to 0 volts and the inverted output (pin 13) goes to -6 volts. The negative transition from 0 volts to -6 volts that occurs on the inverted output of sample flip-flop ZC205A is applied to the input (pin N) of pulse amplifier ZC108C and produces a positive-going, -6 volts to 0 volts, 10-microsecond, sample pulse at the output (pin R) of the pulse amplifier. This sample pulse is used to set the 8-level parallel character signals into the shift register.

The sample pulse is also sent to pins 31 and 11 of emitter followers ZC202C and ZC202L and an amplified sample pulse is sent from the outputs (pins 34 and 14) of the emitter followers to terminal D4 of connector JC128 for use by the HSEDC transmitter control module in the sender.

8.33 The sample pulse from pin R of pulse amplifier ZC108C is applied to the set 1A inputs of all the elements in the shift register, R0-R9, to insert a character into the register. The prime 1A input of element R0 is always held at -6 volts, and the sample pulse into the R0 element has no effect and the space in the element remains there. The prime 1A input of element R9 is always held at 0 volts to insure that a mark, representing the stop bit, is set into the R9 element, even though this is provided for by the HB clock pulse and the 10 spaces signal. The 8 levels of the parallel character signal are applied to the prime 1A inputs of elements R1-R8.

8.34 The 8-level parallel character signals comes into the transmitter distributor module on terminals B1-B8 of connector JC128. The level 1 signal comes into the module on terminal B1 and goes to the prime 1A input of element R1; the level 2 signal comes in on terminal B2 and goes to the prime 1A input of element R2, and so on for all the other levels. A 0-volt signal applied to a prime 1A input, indicating a mark, allows the sample pulse to set the associated element to the 1 state; and a -6 volt signal applied to a prime 1A input causes the element to ignore the sample pulse and the element remains in the 0 state. After the sample pulse has inserted the parallel character into the register, the full character, including start bit and stop bit, is ready to be shifted out.

8.35 For the purpose of description, assume that a mark appeared in only the 4th level of the character; thus, only element R4 would be set to the 1 state. The normal output goes to 0 volts and the prime 1B input of element R3 is primed. Since the R5 element stayed in the space condition (0 state) the inverted output of R5 is at 0 volts and this primes the prime 0B input of R4. When the 1st advance pulse comes in, it is accepted by the set 1B input of element R3 and R3 is set to the 1 state. The advance pulse is also accepted by the set 0B input of element R4 and R4 is set to the 0 state. The mark in R4 has been shifted into R3 and the space in R5 has been shifted into R4. The 2nd advance pulse shifts the mark in R3 into R2 and the space in R4 into R3. As the advance pulses come in, each successive bit in the character is shifted into element R0 and the normal output of R0 develops the serial character.

8.36 The sample pulse which sets the character into the register also sets a mark into element R9. This mark represents the stop bit of the character. The 1st advance pulse which shifted the character in the register advances the marking stop bit to element R8. The prime 0B input of element R9 is held at 0 volts and as the mark is advanced out, a space is inserted into element R9. Each advance pulse continues to advance the marking stop bit through each element of the register and each element that the marking stop bit leaves is set to a space. When the mark reaches element R0, all the other elements (R1-R9) of the shift register have been set to spaces.

8.37 The normal output (pin 12) of element R0 alternates between 0 volts for a mark and -6 volts for a space, depending on the nature of the character being shifted out of the register. When the mark stop bit reaches element R0, the normal output will go to 0 volts. The serial character signal from the normal output of R0 is sent to pin 10 of OR gate ZC204C and the output of ZC204C (pin 3) follows the signal on the input. From the output of ZC204C, the signal goes to pins 30 and 10 of emitter followers ZC202B and ZC202K which amplify the signal and send it from the outputs (pins 33 and 13) to terminal D1 of connector JC128. From terminal D1 of JC128, the serial send data signal is sent to the sender station control in the sender which converts it to a polar signal suitable for driving a data set. The other inputs of OR gate ZC204C are normally at -6 volts which allows the output of the OR gate to follow the signal at input pin 10. These inputs are used to blind the output under various conditions.

8.38 As the mark stop bit advances through the shift register, the outputs of emitter followers ZC202P and F are at 0 volts until the mark is advanced from element R4 to element R3; then, with a space in each of the element R4-R9, the outputs of ZC202P and F (pins 5 and 25) go to -6 volts. The mark continues to advance through elements R3, R2, and R1 until it reaches R0. The output of OR gate ZC204G remains at 0 volts until the mark is shifted into element R0 at which time the output of ZC204G goes to -6 volts which passes through emitter followers ZC202A and ZC202J to produce the 9 spaces signal.

8.39 The 9 spaces signal goes through inverter ZC203D, is applied to pin N of AND gate ZC107C, and with a mark in element R0, the output of ZC107C (pin S) goes to 0 volts and primes the prime 0A input (pin 29) of sample flip-flop ZC205A. The next HB clock pulse that occurs is accepted by the set 0A input of ZC205A and sets the flip-flop to the 0 state. This prepares it to generate the sample pulse for the next character in the manner described in 8.31 and 8.32.

C. Continuous Operation and Stopping the Shift Register

8.40 If the TD start signal is held on, pin 6 of OR gate ZC204B is at 0 volts and produces a continuous 0-volt signal at the output (pin 2) which is applied to pin 19 of AND gate ZC204F and keeps the AND gate primed to allow the register to continue sending characters. The advance pulse, that occurs after the mark stop bit is set into element R0, sets the space in element R1 into element R0 to indicate the start bit of the next character. The sample pulse is generated, the next character is inserted into the register, and shifted out. The register continues to send characters out as long as the start indication remains on.

8.41 If the TD start signal goes off or if the start indication to the shift register was due to a pulse start, pins 6 and 7 of OR gate ZC202B will be at -6 volts. However, the mark stop bit inserted into element R9, through OR gates ZC204H, ZC204G, and ZC204B, keeps a 0-volt signal on pin 19 of AND gate ZC204F. When the mark stop bit is advanced into the R0 element, pin 19 of AND gate ZC204F goes to -6 volts and prevents a space from being shifted into R0 and no new character is inserted into the register and shifted out. The register begins operating again when another start indication comes in on the TD start lead.

8.42 When the shift register is operating, it performs two other functions not described above. Half-way through the shifting out of each character, a pulse is generated for use by the CSS (contact signal shaper) circuits that interface with the signal contacts of the reader. At the end of each character, a pulse is generated to command the reader to step.

8.43 Six bits after the start of each character, the mark stop bit advances into element R3 and the outputs of emitter followers ZC202P and F (pins 5 and 25) go to -6 volts. This -6 volts is applied to pin 5 of inverter ZC203G. The output of ZC203G (pin 16) goes to 0 volts and this signal is applied to pin 9 of flip-flop ZC206B to prime that element. The first half-bit clock pulse, that occurs after the flip-flop is primed, causes the output (pin 14 of flip-flop ZC206B) to go to -6 volts. This negative-going transition is applied to pin P of pulse amplifier ZC108D and produces a positive going, -6 volts to 0 volts, 20-microsecond pulse at the output (pin S). This reset pulse is applied to pin 25 of the CSS circuits (ZC210) for the read contacts on the reader. The reset pulse is also applied to the inputs (pins 32 and 12) of emitter followers ZC202D and M which amplify the pulse and send it from the outputs (pins 35 and 15) to terminal D3 of connector JC128 for use by the CSS circuits in the HSEDC transmitter control module of the sender.

8.44 The CSS circuits for the read contacts of the reader are located on the circuit card in the transmitter distributor module in position ZC210. The signals from the levels 1-8 read contacts come into the module on terminals A1-A8 of connector JC125 and go to the inputs of the CSS circuits. The outputs of the CSS circuits are sent to terminals A1-A8 of connector JC128, where they go to the HSEDC transmitter control module for gating before being sent back to the TD shift register for transmission at the proper time. The outputs of the CSS circuits for levels 1-7 are also used by ZC211 if the vertical parity option is provided in the module.

8.45 If a contact is closed to ground, it indicates a mark or hole in the tape and the output of the CSS circuit is 0 volts. If a contact is open, it indicates a space or no hole in the tape and the output of the CSS circuit is -6 volts. The CSS reset pulse is used to reset the circuits to accept each new character. It occurs after the new character has been moved over the contacts and resets each of the circuits to the spacing condition. It remains for the marking signal on each contact to set the particular CSS circuit to the mark condition. The CSS circuit stores the mark signal, even if the contact opens.

D. Level Selection

8.46 When the tape in the reader contains only 7 levels of information, the 8th level is always read as a mark. The LEVEL SELECTOR switch for the reader read contacts is SWC1,

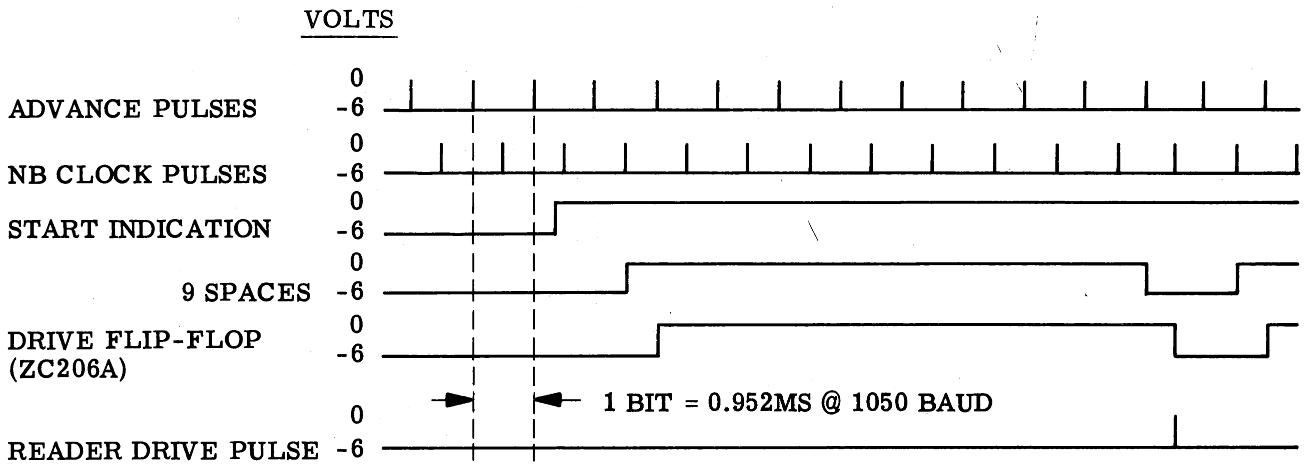

Figure 21 - Reader Drive Pulse Timing

mounted on the front plate of the transmitter distributor module. When the switch is in the 7 level position, a 0-volt signal is continuously applied to the input (pin 20) of the level 8 CSS circuit on ZC210. This is always recognized as a mark and the output (pin 31) is 0 volts.

8.47 When tape with 6 levels of information is in the reader, both the seventh and eighth levels are read as marks; LEVEL SELECTOR switch SWC1 is in the six level position. A 0-volt signal is applied to the level 8 CSS circuit as described above and is always recognized as a mark. A 0-volt signal is also applied to the input of the level 7 CSS circuit of ZC210 (pin 19) which produces a 0-volt signal at the output (pin 32) to continuously generate a mark for that level.

8.48 When tape with five levels of information is in the reader, the first level is always read as a space and the seventh and eighth levels are always read as marks. With LEVEL SELECTOR switch SWC1 in the 5 level position, marks are generated for the seventh and eighth levels as described above. The input to the level 1 CSS circuit (pin 6) of ZC210 is always open-circuited to produce a -6 volt signal at the output (pin 7) which is always recognized as a space.

8.49 At the end of each character transmitted, a reader drive pulse is generated to cause the reader to step to the next character. At the speed of 1050 Baud, the pulse is generated half a bit before the end of the character. The generation of drive pulses also depends on the presence of a start signal. See the timing diagram in Figure 21.

8.50 The reader drive pulses are generated through drive flip-flop ZC206A. The drive flip-flop is in the 0 state initially and the normal output (pin 1) is at -6 volts. When the start indication comes on, 0 volts is applied to pin 12 of AND gate ZC204A. Both the 9 spaces signal and the reset signal are at -6 volts; and either one of the two signals holds -6 volts on pin 14 of AND gate ZC204A. When the character is inserted into the shift register, both signals go to 0 volts, one of the two signals puts 0 volts on pin 14 of AND gate ZC204A, and the output of ZC204A (pin 1) goes to 0 volts. The 0-volt signal from ZC204A is applied to prime 1A input (pin 9) of drive flip-flop ZC206A. The advance pulses are applied to the set 1A input (pin 8) of ZC206A; and the next advance pulse sets the drive flip-flop to the 1 state and the normal output goes to 0 volts.

8.51 The 9 spaces signal is used to control the drive flip-flop. Nine bits after the start of the character, the 9 spaces signal goes to -6 volts and this signal is applied to pin 20 of inverter ZC203H. The output of inverter ZC203H goes to 0 volts and this signal is applied to the prime 0A input (pin 5) of ZC206A. The next HB clock pulse is accepted by the set 0A input (pin 4) of ZC206A and the drive flip-flop is set to the 0 state. The normal output goes to

-6 volts, and the negative-going transition applied to pin C of pulse amplifier ZC109A, produces a positive-going, -6 volts to 0 volts, 10-microsecond reader drive pulse at the output (pin A) of ZC109A. The reader drive pulse is sent to terminal D5 of connector JC128 for gating by the HSEDC transmitter control module of the sender. At the start of the next character, the drive flip-flop is set to the 1 state in preparation for the generation of the next reader drive pulse.

E. Start Blind

8.52 A circuit is provided in the transmitter distributor module to blind the output of the shift register during the transmission of the first character. The circuit is required because of the stepping characteristics of the reader and the timing of the reader drive pulse. As described before, a reader drive pulse is generated at the end of each character. It takes the reader approximately 2.5 milliseconds to start to step and move the next character in the tape into position. At the start of transmission, the first character is inserted in the shift register and sent out. At the end of the character, a reader drive pulse is generated and then the register inserts the next character. However, the reader has not started to step yet and the register would insert the same character that had just been transmitted. Then the reader would step and a new character would be available. The start blind circuitry blinds the output of the register during the first character so that character is only sent once; this circuit is used only in the non-EDC mode.

8.53 The start blind function is controlled by flip-flop ZC205B. Before a start indication comes on, -6 volts is applied to pin 11 of inverter ZC203C and a 0-volt signal from the output (pin 9) is applied to pin E of AND gate ZC107B. The 9 spaces signal, through inverter ZC203D, puts 0 volts on pin F of ZC107B. The pulse start detect flip-flop is in the 0 state and a 0-volt signal from the inverted output (pin 2) is applied to pin H of AND gate ZC107B. The output of ZC107B (pin B) is then at 0 volts and applies the 0-volt signal to the prime 1A input (pin 26) of start blind flip-flop ZC205B. The advance pulses are applied to the set 1A input (pin 23) and set the flip-flop to the 1 state. The inverted output (pin 17) goes to -6 volts, and this signal is applied to pin 25 of ZC203F and holds a mark on the send data lead, no matter what the condition of the other inputs. When the start indication comes on, the first character is sent out of the shift register but only a mark hold signal appears on line. The start indication removes 0 volts from pin E of AND gate ZC107B and applies 0 volts to the prime 0A input (pin 19) of ZC205B. At the end of the character, the 9 spaces signal causes the output of inverter ZC203D to go to 0 volts and the transition applied to the set 0A input (pin 18) of the start blind flip-flop ZC205B which sets the flip-flop to the 0 state and removes the blind signal from pin 11 of OR gate ZC204C. The output of the shift register is now presented to the line for transmission.

8.54 A pulse start indication causes the start blind flip-flop to set back to the 0 state at the start of the character. This allows the character to pass through OR gate ZC204C.

F. Transmitter Distributor Cycle

8.55 An input to the transmitter distributor module is available to cause the shift register to cycle, but prevents reader drive pulses from being generated. By placing 0 volts on terminal B10 of connector JC128, a 0-volt signal is applied through OR gate ZC204E to the prime 1B input (pin 21) of the pulse start detect flip-flop ZC205C. This generates continuous pulse start indications and the shift register continues to shift characters out. Since pin 12 of AND gate ZC204A is at -6 volts, the drive flip-flop is not used and no reader drive pulses are generated.

8.56 A lead is available into the transmitter distributor to blind the output of the shift register. By putting 0 volts on terminal G1 of connector JC128, pin 9 of OR gate ZC204C is at 0 volts and a continuous mark hold signal is generated on the send data lead.

G. Power Supplies

8.57 The transmitter distributor module uses the TP302720 multivoltage power supply to generate dc power. The power supply receives 117v ac from terminals 1 and 2 of connector JC121; terminal 3 is ground. The ac supply is applied to terminals 1 and 3 of TBC428 in the PSC428 power supply and ground is applied to terminal 2. The outputs of the power supply appear at TBC515 of TBC428. Terminals 1 and 2 supply 1v ac for indicating lamps used in the HSEDC transmitter control module. Terminal 3 supplies -12 volts dc. The -12 volts goes through 4-ampere fuse FC2 and is then distributed to the module. It is also returned to terminal 4 of the power supply to develop -6 volts dc which appears on terminal 5; +6 volts dc appears on terminal 6 and is fused at 1 ampere by FC4 before being distributed to the module. Terminal 8 supplies +50 volts dc and is fused at 1/2 ampere by FC6. The +50 volts dc is also used for the indicating lamps in the transmitter control module. Terminal 7 of the power supply is a common ground for all the power supply voltages.

8.58 The transmitter distributor module uses the TP308451 power supply to develop -48 volts dc. The S (slate) and W (white) leads of power supply PSC414 bring in 117v ac. The O (orange) lead is tied to the ground lead of the PSC428 power supply and establishes circuit ground. The -48 volts dc is developed on the BK (black) lead of the power supply and is fused at 1-1/2 amperes by FC3.

8.59 All of the dc voltages produced are tied to connector JC128 for external use. The terminals they appear on are shown in the following list.

Terminal	Voltage
H1	Frame Ground
H2	Signal Ground
H3	Circuit Ground
H4	+6 volts dc
H5	-6 volts dc
H6	-12 volts dc
H7	-48 volts dc
H8	+50 volts dc
H9	1 volt ac
H10	1 volt ac Return

8.60 Connector JC125 in the transmitter distributor module provides an interface for the signal leads from the reader. The leads from the read contacts of the reader come in on terminals A1-A8 and are used by the transmitter distributor module. The other signals are connected to terminals on connector JC128 for use by other components. The verify contacts signals come in on terminals B1-B8 of connector JC125 and go to terminals C1-C8 of connector JC128. The signals from the feed detect contact and the tape-out contact come in on terminals C1 and C2 of JC125 and go to terminals C9 and C10 of JC128. The special signals from the EDC assembly on the reader come in on terminals D1-D7 of connector JC125 and go to terminals G3-G9 of connector JC128 for use by the HSEDC transmitter control module in the sender.

8.61 The reader drive signals originate in the HSEDC transmitter control module. The drive signals come into the module on terminal D6 of JC128, are inverted by inverter ZC203A, and sent out on terminal C6 of connector JC125. These signals are then fed into the magnet driver network on the reader assembly. The negative — going transitions that appear at the input of the dual-magnet driver energize the coils of the step magnets on the reader and cause the reader to step.

H. Module Features

8.62 REVERSE CHANNEL SIMULATE switch SWC3 is mounted on the front plate of the transmitter distributor module to help control the reverse channel relay in the sender station control. With the switch in the OFF position, 0 volts is held on terminal D9 of connector JC128 and energizes the RC relay if reverse channel is lost. In the ON position, 0 volts is applied to terminal D10 of JC128 to simulate the reverse channel.

8.63 VERTICAL PARITY selector switch SWC2 is provided on the front panel to the transmitter distributor module for use when the vertical parity accessory is used.

9. SENDER STATION CONTROL

GENERAL

9.01 The sender station control circuitry consists of a control assembly, 6 relays, and 2 circuit cards. These are mounted on the sender station control chassis. See Figure 22.

9.02 The schematic diagrams, contained in another section are:

7402WD - sender station control
7070WD - controls assembly

AC POWER DISTRIBUTION

9.03 The ac power comes into the sender station control on the ac line cord supplied. The hot side of the line goes through fuse FG1, which fuses the line at 10 amps, and goes to terminal 17 of connector JG3. From terminal 17, one lead takes the ac power signal to the POWER ON/OFF switch SW11. The other side

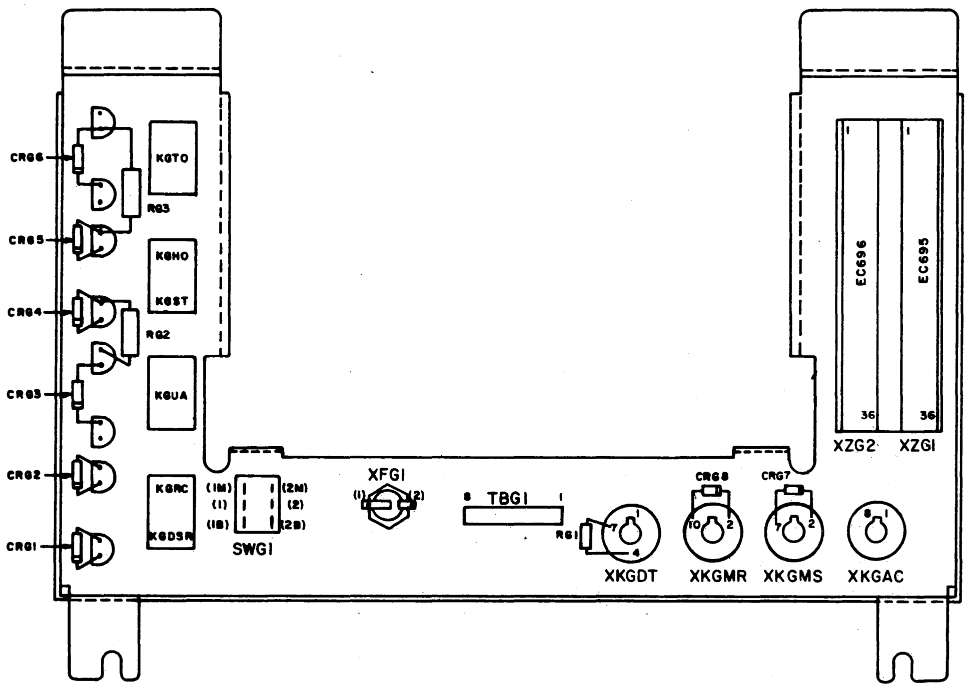

Figure 22 - Sender Station Control, Module G, Bottom View

of this switch is returned to terminal 19 of JG3 and connected to terminal 2 of the ac relay. The other side of the ac relay (terminal 7) is connected to the other side of the ac power line. When the switch is pushed to turn power on, two sets of contacts from the ac relay send switched ac power back to the station control on two leads and to terminals 1 and 2 of JG3. The common side of the ac line is not fused. The switched ac power is also sent to the MS (motor start) relay contacts to be distributed to the sender terminal's motors.

9.04 When ac power comes to the transmitter distributor module, it will energize the power supplies in the module to produce dc power. The sender station control uses +6 volts, -6 volts, -12 volts, -48 volts, signal ground, and circuit ground. These voltages come into the sender station control on pins 44, 45, 46, 47, 42, and 43 respectively, of connector JG4. From the sender station control, -48 volts, signal ground, and circuit ground are sent to the controls assembly on pins 20, 22, and 23 of connector JG3.

9.05 When the POWER ON/OFF switch is pushed on and circuit ground is established, the ground signal, through pin 12 of connector JG3, will cause the indicator in POWER switch DS11 to light.

DATA SET INTERFACE LOGIC

9.06 The sender station control provides an interface for the data set. The signals to and from the data set are EIA standard interface signals. The sender station control converts the EIA signals to neutral signals and it converts neutral signals to EIA signals. The following table applies to the EIA signals:

Data-Binary State	One	Zero
Data-Signal Condition	Marking	Spacing
Paper Tape	Hole	No Hole
Voltage	Negative (-3v to ·25v)	Positive (+3v to +25v)
Control Function	Off	On

9.07 In order for the data set to be able to enter the data mode, the DTR (data terminal ready) lead must be on. This lead is normally held on by the output of polar-to-polar amplifier Z1H whose input is held off by the RI (ring indicator) lead. The RI lead comes in on pin 10 of connector JG4 and goes to pin 32 of Z1H. A negative voltage on this lead (-6 volts) will produce a positive voltage (+6 volts) at the output, pin 31, which goes to pin 8 of JG4 to hold the DTR lead on. When a call is made at the sender terminal, the data set will enter the data mode when the operator pushes the DATA button on the data set. If a call comes into the sending terminal, however, the RI lead will go positive during the ringing cycle, causing the DTR lead to go negative and since the data set will only enter the data mode during the ringing cycle, the data set will never answer. This requires that the operator manually answer the call and manually cause the data set to go to the data mode by pushing the DATA button. Since ringing stops when the call is answered, the DTR lead will be on and the data set will enter the data mode.

9.08 When the data set enters the data mode, the DSR (data set ready) lead comes on (+6 volts). This signal comes in pin 4 of connector JG4 to the input (pin 34) of relay driver Z1G which sends a 0-volt signal to the DSR relay to operate the relay. Diode CR1, across the DSR relay coil, is used to prevent voltage spikes when the relay is de-energized. From the DSR relay, break contact 2 holds a ground signal on pin 27 of OR gate Z1J which, through OR gate Z1J and N/P amplifier Z1K, holds the RTS (request-to-send) lead off (-6 volts). When the DSR relay operates, the ground signal is removed from pin 27 which puts +6 volts on terminal 2 of connector JG4 to turn on the RTS lead. When the data set detects RTS on, it turns on the CTS (clear-to-send) lead. The CTS lead comes into the sender station control on pin 3 of connector JG4 and goes to pin 18 of P/N amplifier Z1A which converts the signal to a neutral signal. CTS on (+6 volts) will produce a -6 volt signal at pin 7 of Z1A for use by the sender station control.

9.09 The polar transmit clock signal comes into the sender station control on terminal 6 of connector JG4 and goes to pin 19 of P/N amplifiers Z1B which converts the signal to a neutral signal and sends it from pin 12 of Z1B to terminal 16 of connector JG4. The transmit clock signal determines the timing for the sender at high speeds of operation.

REVERSE CHANNEL

9.10 The polar reverse channel signal comes into the send station control on terminal 5 of connector JG4 and goes to pin 20 of P/N amplifier Z1C which converts it to a neutral signal and sends it from pin 17 of Z1C to terminal 15 of connector JG4 for use by the HSEDC transmitter control module in the sender. The neutral reverse channel signal also goes to pin 6 of relay driver Z1F.

9.11 Relay driver Z1F is used to drive the RC (reverse channel) relay. When the RC relay is de-energized, it means the reverse channel is on and when it is energized, it means the reverse channel is off. Pin 10 of Z1F primes the relay driver to enable it to pull in the RC relay. It requires a 0-volt signal. A switch in the transmitter distributor module is used to supply the priming signal and the position of the switch depends on whether the reverse channel feature is supplied with the data set. If the feature is not supplied, the switch in the REVERSE CHANNEL SIMULATE-ON position will withhold a 0-volt signal to pin 10 of Z1F and the RC relay will never be pulled in. In the REVERSE CHANNEL SIMULATE-OFF position, a 0-volt signal is sent to terminal 22 of connector JG4 of the sender station control. This signal then goes through make contact 1 of the DSR relay before it goes to pin 10 of Z1F. This requires that the data set be in the data mode and the DSR relay be energized for the 0-volt signal to reach pin 10. With 0 volts on pin 10, the signal on pin 6 now determines whether the RC relay is energized or not. If the reverse channel signal is off, pin 6 will be at 0 volts which will cause relay driver Z1F to energize the RC relay. When the reverse channel comes on, pin 6 goes to -6 volts and RC relay is de-energized.

9.12 The reverse channel is the only communications link from a receiver to the sender. When the reverse channel is lost and the RC relay pulls in, make contact 8 of the RC relay closes to ground and sends the signal, through terminal 13 of connector JG3, to the RECEIVER STOPPED indicator (DS12) to light the lamp and indicate the receiver is stopped.

9.13 Diode CR2, across the RC relay coil, is used to prevent voltage spikes when the RC relay de-energizes.

CONTROL LOGIC

A. Tape-Out Relay

9.14 The TO relay in the sender station control is used to recognize the tape-out condition. It is driven by the tape-out contact of the reader in the sender. The signal from the tape-out contact comes into the sender station control on terminal 20 of connector JG4 and goes to the TO relay. If tape is in the reader, the tape-out contact will be open and the TO relay will be in the de-energized state. If tape-out exists at the reader, the tape-out contact will be closed to ground and the TO relay will be pulled in. The TO relay is also driven by the feed detect alarm circuitry in the sender transmitter control module to simulate a tape-out condition.

B. Stop and Hold Relays

9.15 Two relays in the sender station control assembly, ST (stop) and HO (hold), are provided to stop and alarm the terminal. They are controlled by the STOP-ALARM/RESET button and by a contact from the TO relay. If the relays are de-energized, they are pulled in when the STOP-ALARM/RESET button is pushed or when tape-out occurs. If they are automatically pulled in by the TO relay, the alarm must be corrected before the ST and HO relays can be reset. To reset the relays, the STOP-ALARM/RESET button must be reset. When the STOP-ALARM/RESET button is pushed or when tape-out occurs, the ST relay is pulled in which causes the HO relay to pull in. When they are reset, the ST relay drops out which causes the HO relay to drop out.

9.16 The -48 volt bias supply for the ST relay goes through resistor R2 to pin 2L of the ST relay coil. The -48 volt bias supply for the HO relay goes through resistor R3 to pin 2U of the HO relay. The opposite sides of the ST and HO relay coils, 1L and 1U respectively, are connected together and are also connected to a make contact to ground 9, from the TO relay in parallel with a series combination of a make contact, 5, from the ST relay and a make contact, 5, from the DSR relay to ground. A make contact to ground from the STOP-ALARM/RESET button comes into the station control on terminal 7 of connector JG3 and goes through transfer contacts 8, from the HO relay to the 2L and 2U sides of the ST and HO relay coils.

9.17 With no call in progress, the DSR relay is not pulled in and make contact 5 of that relay is always open and the ST and DSR contact combination has no effect on the ST and HO relays. If the STOP-ALARM/RESET button is pushed, a ground signal momentarily drives pin 2U of the HO relay to ground and this signal, through the HO relay to pin 1L of the ST relay, pulls in the ST relay. However, nothing holds pin 1L at ground if the STOP-ALARM/RESET button is released and the ST relay drops out. If the TO relay pulls in, however, make contact 9 from the TO relay pulls in. When the TO relay drops out, it causes the ST and HO relays to drop out.

9.18 With a call in progress, the DSR relay is pulled in and make contact 5 from the DSR relay closes to ground. Now, when the STOP-ALARM/RESET button is pushed and the ST relay pulls in, a ground signal from the DSR-ST contact combination holds the ST relay energized even when the button is released. This also causes the HO relay to pull in. When the HO relay pulls in, transfer contacts 8 from the HO relay then allow the signal from the STOP-ALARM/RESET button to go to pin 2L of the ST relay. When the RESET button is then pushed, pin 2L of the ST relay goes to ground and the ST relay drops out. This opens make contact 5 of the ST relay and removes the ground signal from pin 1U of the HO relay. When the RESET button is released, the HO relay drops out and transfer contacts 8 from the HO relay switch back and allow the next signal from the STOP-ALARM/RESET button to go to pin 2U of the HO relay.

If the relays are energized when the call is dropped, the ST and HO relays also drop out.

9.19 If the TO relay pulls in at any time, it causes the ST and HO relays to pull in. They remain energized even if the TO relay drops out. The STOP-ALARM/RESET button must be reset to drop out the ST and HO relay when a call is in progress.

9.20 A make contact, 1, from the ST relay and a make contact, 12, from the HO relay are connected to terminal 14 of connector JG3. When either the ST relay or the HO relay or both are energized, a ground signal is applied to lamp DS13 in the STOP-ALARM/RESET button to indicate the alarm.

9.21 Diode CR6 across the TO relay coil is used to prevent voltage spikes when the relay drops out.

9.22 Make contact, 10, from the TO relay goes to terminal 48 of connector JG4 for use by the transmitter control module in the sender.

C. Motor Start and Motor Reverse Relays

9.23 AC power is supplied to the motors of the sender through the MS (motor start) relay. When the MS relay pulls in, the hot side of the ac line goes to terminal 1 on JG1 and through the MR (motor reverse) relay contacts. The common side of the ac line will be on terminal 2 on JG1 and through the MR relay contacts. The MR relay switches the hot and common side of the ac line between terminals 3, 4, and 5 to cause the reader to change directions.

9.24 Power is normally supplied to the motors only when a call is in progress and the data set is in the data mode and no alarms are present. With the DSR relay pulled in, a ground signal goes through make contact 5 to break contact 5 of the ST relay. From the output (pin 7) of Z2K, the ground signal goes through break contact 9 of the HO relay to pin 2 of the MS relay coil and the MS relay pulls in. If an alarm occurs, the ground signal is removed and the MS relay drops out and turns off the motors.

9.25 The MS relay can be energized and the motors turned on through two auxiliary sources. A 0-volt signal can be applied to the MS relay coil from the HSEDC transmitter control module in the sender. This signal comes into the sender station control on pin 26 of connector JG4 to turn on the motors while the electronic logic recycles. The second source is the AUX MOTOR START button on the sender cabinet. When the button is pushed, a 0-volt signal is applied to the MS relay through pin 3 of connector JG3 to turn on the motors.

9.26 When the AUX MOTOR START button is pushed, the AUX MOTOR START indicator, DS3 lights.

9.27 The MR (motor reverse) relay, driven by a signal from the HSEDC transmitter control module, comes in terminal 27 of connector JG4, and 0 volts pulls in the MR relay. When the MR relay pulls in, the hot side of the ac line is switched from terminal 3 of JG1 to terminal 4 and the common side of the line is switched from terminal 4 to terminal 3 of JG1 and the reader on the sender reverses direction. When the MR relay drops out, the reader is switched back to run in the forward direction.

9.28 A normally-closed contact from the MR relay applies a 0-volt signal to the HSEDC transmitter control module. When this contact opens, after the MR relay pulls in, it indicates that the motors on the reader have been reversed.

9.29 Diode CR7 across the MS relay coil and diode CR8 across the MR relay coil are used to prevent voltage spikes when the relays drop out.

D. Start Control Logic

9.30 The function of the start control logic is to develop a run/stop signal for the sender electronics, indicating the data set is in the data mode and no alarms are present. It also gates in the send data signal and converts it to a polar signal to drive the data set. The run/stop lead goes to terminal 17 of connector JG4; 0 volts indicates run and -6 volts indicates stop. The neutral send data signal comes in on terminal 11 of connector JG4 and 0 volts indicates mark and -6 volts indicates space. When the send data signal is converted to a polar signal, -6 volts indicates mark and +6 volts indicates space. The polar send data signal goes through terminal 1 of connector JG4 to the data set.

9.31 The run/stop signal is developed through OR gates Z10 and Z2E, delay inverter Z2F, and emitter follower Z2C. The run/stop signal will be held off if any input to either of the OR gates is at 0 volts. This causes the outputs of the OR gates, which are tied together, to be at 0 volts. The 0-volt signal goes to the input (pin 8) of delay inverter Z2F which sends a -6-volt signal from its output (pin 12) through emitter follower Z2G to terminal 17 of connector JG4.

9.32 The run/stop signal is controlled by several sources. First, the data set must be in the data mode and the DSR relay must be pulled in. This opens break contact 2 of the DSR relay and removes a ground signal from pin 5 of OR gate Z2E. DSR on turns request-to-send on and causes the data set to turn on clear-to-send. CTS on puts a -6 volt signal on pin 3 of OR gate Z10. Request-to-send also controls the run/stop signal through pin 4 of OR gate Z10. This is described in the following paragraphs.

9.33 For the run/stop signal to come on, the terminal must not be alarmed. With a no tape-out condition, make contact 8 of the TO relay is open which opens input pin 4 of OR gate Z2E. With no alarm condition, make contact 4 of the ST relay and make contact 10 of the HO relay are open which opens input pin 5 of OR gate Z10. A start blind signal comes into the sender station control through terminal 18 of connector JG4 to pin 2 of OR gate Z10 and is available for the sender electronics to hold the run/stop signal off; normally, this lead is open.

9.34 When request-to-send comes on, the output of OR gate Z1J goes to -6 volts. This signal is applied to pin 25 of OR gate Z1E and with no alarm, the output of Z1E goes to -6 volts. The -6 volt signal goes to the input (pin 13) of inverter Z2B and produces a 0-volt signal at the output (pin 10) of Z2B. The positive-going transition from the output of Z2B goes into the set 1A input of flip-flop Z2D and sets it to the 1 state. The normal output (pin 26) of flip-flop Z2D goes to 0 volts and the 0-volt signal, applied to pin 4 of OR gate Z10, holds the run/stop signal off. The normal output of Z2D also primes its own prime 0A input. The inverted output of Z2D (pin 25) goes to -6 volts and the -6 volts signal triggers timer Z2D. The input of timer Z2D and the output of flip-flop Z2D are tied together internally on the circuit card. These points are also tied to one input of AND gate Z2H on the same circuit card. When its input goes to -6 volts, timer Z2D starts a time-out of approximately 1 to 3 seconds. At the end of the time-out, a positive-going pulse is generated at the output of the timer which is applied to the set 0A input of flip-flop Z2D and the flip-flop is set back to the 0 state. The normal output of flip-flop Z2D goes to -6 volts and if all the other inputs to OR gates Z10 and Z2E are open or at -6 volts, the run/stop lead goes to 0 volts. The inverted output of flip-flop Z2D goes to 0 volts.

9.35 During the 1 to 3-second time-out, the negative voltage on pin 25 of AND gate Z2H holds the output of the gate (pin 28) at -6 volts which puts a spacing signal on the line for 1 to 3 seconds. The purpose of the spacing signal is to disable any echo suppressors on the line to permit two-way communication. When pin 25 to AND gate Z2H goes back to 0 volts, the send data signal on pin 23 passes through the AND gate, is converted to a polar signal by N/P amplifier Z2J, and goes to the data set through terminal 1 of connector JG4.

FEATURES AND ACCESSORIES

A. General

9.36 A switch on the controls assembly selects the non-EDC operation for the sender terminal. When the NON-EDC button is pushed, a contact is closed to ground on the switch. The 0-volt signal comes into the sender station control on terminal 1 of connector JG3 and goes to terminal 21 of connector JG4 which sends it to the HSEDC transmitter control module in the sender terminal to indicate the non-EDC mode. When the NON-EDC button is pushed, a second contact on the switch also closes to ground and causes the NON-EDC indicator (DS6) to light.

9.37 Switch SW1, TEST/OPERATE, is provided on the sender station control to operate the unit when the terminal is not connected to a data set. The normal position of the TEST/OPERATE switch is OPERATE. When the switch is thrown to the TEST position, a ground signal is applied to the DSR relay coil to operate the DSR relay. The switch also breaks the clear-to-send lead to provide the run/stop on signal.

9.38 Spare contacts from the DSR, RC, TO, UA, ST, and ST-HO relays are available at connector JG4 for external use.

B. Unattended Answering

9.39 Two options are available to provide the unattended answering feature. Option A1 provides unattended answering under control of the UNATTND button on the controls assembly. Option A2 provides unattended answering only when the UNATTND button is pushed and no tape-out condition exists. The options are available through terminal board TB1 using TP306087 terminal jumpers.

9.40 When option A1 is chosen, terminals 1 and 2 of TB1 are connected together. When the UNATTND button is pushed, a 0-volt signal goes through a break contact on the AUX. MOTOR START switch and passes through a make contact on the UNATTND switch to terminal 2 of connector JG3. From terminal 2 of JG3, the signal goes to the coil of the UA relay to energize the relay. Option A1 also provides strapping together of terminals 3 and 4 of terminal board TB1. When the UA relay pulls in, make contact 8 of the UA relay closes and a 0-volt signal passes through terminal 11 of connector JG3 to the UNATTND button indicator (DS5) and causes it to light. The MANUAL button indicator (DS4) goes off when the UNATTND button is pushed. If the AUX. MOTOR START button is pushed, the 0-volt signal to the UA relay is inhibited and the UA relay is not pulled in. However, both the non-EDC mode and the unattended mode can be chosen simultaneously.

9.41 When the UA relay pulls in, break contact 3 of that relay opens and inhibits the ring indicator signal from coming in and turning off the data-terminal-ready signal. Thus, if a call comes into the sender terminal, the data-terminal-ready signal is on and the call is answered automatically. The call is dropped when the distant terminal disconnects.

9.42 Make contact 6 of the UA relay also closes when the UA relay is energized. This allows a 0-volt signal to pass through to pin 16 of OR gate Z1J to withhold the request-to-send signal if a tape-out condition exists and make contact 6 of the TO relay is closed. Since the request-to-send signal initiates the carrier signal to the distant terminal, the absence of the carrier signal tone at the distant terminal is recognized as an alarm at the sender.

9.43 If option A2 is chosen for the unattended answering feature, terminals 1 and 2 of TB1 are still strapped together to allow the UA relay to pull in when the UNATTND button is pushed. The strap between terminals 3 and 4 of TB1 is removed and a strap is placed between terminals 4 and 5. This allows the 0-volt signal which causes the UNATTND indicator to light to pass through only if the tape-out condition does not exist and the TO relay is not pulled in. If the tape-out condition exists, the UNATTND indicator does not light. A third jumper is provided with the A2 option which ties terminals 6 and 7 of TB1 together. Break contact 3 of the UA relay inhibits the ring indicator signal, but an alternate path is provided through make contact 3 of the TO relay, if the tape-out condition exists, that allows the ring indicator signal to turn off the data-terminal-ready signal and prevent the terminal from answering automatically. If the tape-out condition does not exist, incoming calls are answered automatically.

C. Automatic Disconnect

9.44 The automatic disconnect feature is provided in the sender station control by the addition of DT thermal relay TP308545. The automatic disconnect feature is only effective when the terminal is in the unattended mode.

9.45 In the unattended mode and with the UA relay pulled in, make contact 5 of the UA relay is closed. After a call is answered and the DSR relay is energized, if a tape-out condition occurs make contact 7 of the TO relay is closed and a ground signal through make contact 4 of the DSR relay is applied to pin 2 of the DT relay; and after approximately 60 seconds, the DT relay pulls in. In the same way, if reverse channel goes off, make contact 12 of the RC relay closes and a ground signal is applied to pin 2 of the DT relay; and after approximately 60 seconds, the DT relay pulls in.

9.46 When the DT relay pulls in, the make contact of the DT relay closes. This allows a -6 volt signal, through resistor R1, to pass through the contact and cause the data-terminal-ready lead to go to -6 volts. When the data-terminal-ready lead goes off, the data set drops the call.

9.47 A call may be answered manually and then automatically dropped at the conclusion of transmission. To accomplish this, the operator waits for transmission to begin before pushing the UNATTND button. Make contact 5 of the UA relay closes and the call is dropped as described in 9.45 and 9.46.

D. Private Line/Switched Network Control

9.48 When the sender terminal is used on the switched network, the 1 to 3-second spacing signal, provided by flip-flop Z2D in the sender station control, is required to disable echo suppressors on the line in addition to allowing the terminal's motors to come up to speed. When operating on private lines in the unattended mode, however, terminal 24 of connector JG4 is provided to lock out the spacing signal and keep the terminal motors energized.

9.49 When terminal 24 of JG4 is tied to ground, a 0-volt signal through make contact 1 of the UA relay goes to pin 3 of OR gate Z2K which energizes the MS relay to allow ac power to go to the motors in the sender. The 0-volt signal also goes through diode CR11 of Z2L and clamps the inverted output of flip-flop Z2D at 0 volts to lock out the spacing signal.

E. Discrete Calling Recognizer Accessory

9.50 The sender station control is capable of operating with the discrete calling recognizer accessory. The sender station control must have the unattended answering feature provided. The automatic disconnect feature may or may not be provided.

9.51 In the unattended mode, make contacts 4 and 6 of the UA relay are closed. When a call comes into the sender terminal, it is answered automatically. Make contact 4 of the DSR relay closes when the data set enters the data mode and a 0-volt signal is presented to terminal 37 of connector JG4 to prime the discrete calling recognizer. A 0-volt signal from the recognizer comes in terminal 13 of connector JG4 and goes through make contact 6 of the UA relay to pin 16 of OR gate Z1J to hold request-to-send signal off. The recognizer now waits for the proper identification code from the distant terminal. If the proper code is received, the recognizer causes the request-to-send signal to come on and the sender is allowed to start transmitting. If the proper code is not received, the request-to-send signal does not come on and the sender does not start transmitting.

9.52 During the time the recognizer is waiting for the proper identification code, a 0-volt signal is presented to terminal 23 of connector JG4. If the automatic disconnect feature is not provided, this has no effect. With the DT relay pulled in, the 0-volt signal starts the 60-second time-out. If the proper code is not recognized within 60 seconds, the DT relay will not operate and transmission will start.

9.53 The tape-out condition causes terminal 37 to remain open. If a call is answered automatically (under option A1) the discrete calling recognizer keeps the request-to-send signal off and, with the DT relay provided, the discrete calling recognizer initiates a disconnect, even if the proper identification code is received.

9.54 With the discrete calling recognizer accessory, a call may be answered manually and dropped automatically in the same manner as described in 9.47.

F. Send/Receive Accessory

9.55 The sender station control is wired to accept the send/receive accessory when it becomes available.

10. SENDER CABINET

10.01 The basic function of the sender cabinet is to house a Tape Transport Assembly containing a high speed tape reader, electronic control modules, an electronic distributor and accessory module, and a data set.

10.02 The sender cabinet shell measures 20-1/2 inches wide, 54-1/4 inches high and 24-3/8 inches deep. The cabinet weighs approximately 40 pounds. Housing facilities for a data-set are provided. Facilities for mounting switches and indicator lamps are also provided. The lower portion of the cabinet is enclosed by a flush mounting door which is held closed by a magnetic latch; this portion of the cabinet has facilities to mount three electronic modules. The upper portion of the cabinet contains mounting facilities for the tape transport assembly. The back of the cabinet contains a full size door for easy access to the equipment; the door also contains two cooling fans.

10.03 The tape transport assembly components are mounted on a slide mounted panel 19-3/8 inches wide by 18 inches high. The tape transport assembly is supported by and slides on the TP145909 and TP145910 channels.