VERTICAL PARITY INSERTER (TP308510)

FOR

FIVE TO SEVEN LEVEL OPERATION OF "DATASPEED"* TAPE SENDER 4A

1. GENERAL

1.01   This section provides description, operation, and installation information for the vertical parity inserter TP308510 used with Tape Sender 4A.

1.02   The vertical parity inserter requires no periodic lubrication or adjustment. For maintenance information, refer to the Tape Sender 4A troubleshooting section.

2. DESCRIPTION

2.01   The vertical parity inserter provides for parity insertion at the tape sender at speeds up to 1200 wpm. The unit, contained entirely on an electronic circuit card (EC 680), provides for either odd parity or even parity when used with 5, 6, or 7 level signals. The eighth level is used for parity insertion. A schematic wiring diagram of the unit is included at the back of this section.

2.02   Vertical parity is used for error detection purposes. Parity information is based on the number of marking bits in each character. This count determines whether a space or a mark bit is to be inserted into the eighth level. Either of two forms may be used: odd parity or even parity. With odd parity, an odd number of marking bits in a character results in the insertion of a space bit in the eighth level; if the count of marking bits is even, a mark bit is inserted into the eighth level. With even parity, an even number of marking bits in a character results in the insertion of a space bit in the eighth level; if the marking bit count is odd, a mark bit is inserted.

2.03   The input to the vertical parity inserter consists of 8 levels of parallel data which represent the information obtained from the tape reader. At each level, a mark is 0 volts and a space is -6 volts.

2.04   The output of the vertical parity inserter is one signal which is either 0 volts or -6 volts, depending on both the parity selection (odd or even) and the marking bit count.

2.05   The unit may be installed in the prewired transmitter distributor module in either the factory or the field.

3. OPERATION

GENERAL

3.01   Since the operation of the vertical parity inserter is related to tape sender operation, refer to the appropriate section for a description of the various tape sender modules. Refer also to these wiring diagrams:

    (a) Tape Sender 4A - 7038WD

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(b) Transmitter Distributor Module - 7410WD

(c) Transmitter Control Module - 7056WD

(d) Vertical Parity Detector - 303680

3.02   The contact signal shaper circuits for the tape reader read contacts are on the circuit card in position ZC210 of the transmitter distributor module. Signals from the read contacts, levels 1 through 8, come into this module on terminals A1 through A8 of connector JC125 and are applied to the inputs of the contact signal shaper circuits. The outputs of these circuits go to terminals A1 through A8 of connector JC128. From this point they go to the transmitter control module for gating before they are returned to the transmitter distributor shift register for transmission at the proper time. Output signal levels 1 through 7 of the contact signal shaper circuits are also used by EC680/ZC211 for vertical parity generation in the transmitter distributor module.

7-LEVEL OPERATION

A. Odd Parity

3.03   Odd parity is generated when LEVEL SELECTOR switch SWC1 is placed in the 7th level position and PARITY SELECTOR switch SWC2 is in the ODD position. Pin 20 of the contact signal shaper (ZC210) then remains grounded and pin 31 remains in a marking condition. This marking signal is applied to terminal 2 of PARITY SELECTOR switch SWC2. Since switch SWC2 is in the ODD position, the signal on terminal 2 is not accepted in the eighth level, and the level is free for parity insertion.

3.04   The level 1 through 7 outputs of the contact signal shaper circuits, pins 7, 8, 12, 10, 33, 30, and 32 of ZC210 respectively, are inserted in the vertical parity unit (ZC211) on pins 2, 3, 13, 14, 22, 23, and 34 respectively. The output (pin 17) of the vertical parity inserter is then

-6 volts (space) for an odd number of marking bits or

0 volts (mark) for an even number of marking bits

in the 7-level input signal. The output signal is applied to emitter follower ZC202E and N (pins 1 and 21). The outputs of ZC202E and N (pins 18 and 20) are applied to the transmitter control module, via terminals 1 and 3 of SWC2 and terminal A8 of connector JC128; for gating before returning to the transmitter distributor module for transmission. Therefore, if levels 1 through 7 contain an odd number of marking bits, a space bit is inserted in the eighth level; for an even number of marking bits, a mark bit is inserted.

B. Even Parity

3.05   Even parity insertion is generated by placing LEVEL SELECTOR switch SWC1 in position 7 and placing PARITY SELECTOR switch SWC2 in the EVEN position. The eighth level output of the contact signal shaper circuits is ignored, but output levels 1 through 7 are inserted in the vertical parity unit (ZC211), as described for odd parity insertion. Since PARITY SELECTOR switch SWC2 is in the EVEN position, pin 35 of ZC211 remains at -6 volts. The output (pin 17) of the vertical parity unit is then

-6 volts (space) for an even number of marking bits or

0 volts (mark) for an odd number of marking bits

in the 7-level input signal. The output signal is applied to emitter followers ZC202E and N (pins 1 and 21). The outputs of ZC202E and N (pins 18 and 20) are applied to the transmitter control module, via terminals 1 and 3 of SWC2 and terminal A8 of connector JC128, for gating before returning to the transmitter distributor module for transmission. Therefore, if levels 1 through 7 contain an even number of marking bits, a space is inserted in the eighth level; for an odd number of marking bits, a mark is inserted.

C. Parity Off

3.06   Parity insertion is disabled when PARITY SELECTOR switch SWC2 is in the OFF position and LEVEL SELECTOR switch SWC1 is in position 7. Pin 20 of ZC210 remains grounded to simulate a marking condition. Output pin 31 of ZC210 remains at 0 volts which is applied to the transmitter control module, via terminal 2 of switch SWC2, to indicate an all-marking condition for level 8.

3.07   The level 1 through 7 outputs of the contact signal shaper circuits, pins 7, 8, 12, 10, 33, 30, and 32 of ZC210 respectively, are inserted in the vertical parity inserter (ZC211) on

pins 2, 3, 13, 14, 22, 23, and 34 respectively. The output (pin 17) of the vertical parity inserter is then

-6 volts for an odd number of marking bits or
0 volts for an even number of marking bits

in the 7-level input signal. The output signal is applied to emitter followers ZC202E and N (pins 1 and 21). The outputs of ZC202E and N (pins 18 and 20) are applied to terminals 1 and 3 of VERTICAL PARITY switch SWC2. Since the switch is in the OFF position, the signals at terminals 1 and 3 are not used for vertical parity generation. Therefore, level 8 remains in an all-marking condition, as determined by LEVEL SELECTOR switch SWC1.

6-LEVEL OPERATION

3.08   Parity insertion in the eighth level is in the same for 6-level operation as with 7-level operation. However, some signal provision must be made for level 7. Output level 7 of contact signal shaper ZC210 (pin 32) remains in a marking condition (0 volts). This signal is applied to pin 34 of the vertical parity inserter

(ZC211) and counted as a marking bit for level 7. Odd or even parity insertion is then performed as described for 7-level operation.

5-LEVEL OPERATION

3.09   Parity insertion in the eighth level is the same for 5-level operation as with 7-level operation. However, some signal provision must be made for levels 1 and 7. A steady spacing signal is obtained from pin 7 (level 1) and a steady marking signal is obtained from pin 32 (level 7) of contact signal shaper ZC210. These signals are applied to the vertical parity inserter in ZC211 for parity counting. Odd or even parity insertion is then performed as described for 7-level operation, effectively providing for the 6 information levels, parity opposite that selected by the PARITY SELECTOR switch.

4.   INSTALLATION

4.01   The transmitter distributor module in the tape sender is pre-wired to accept the vertical parity inserter. To install the unit, simply insert it (card EC 680) into position ZC211 in the transmitter distributor module.
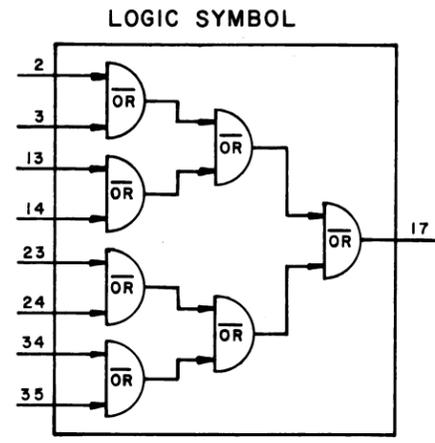
PARITY LOGIC

303680

300116 COVER
2 PLACES

144495 PAD
14 PLACES

EC680   303680

308474
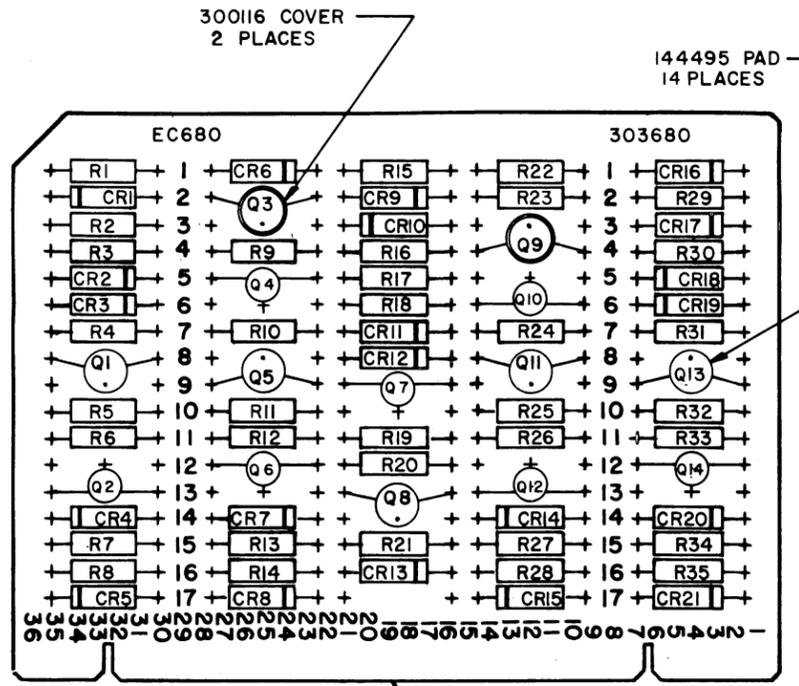
NOTE:
REFER TO 6050WD FOR BASIC MARKING INFORMATION

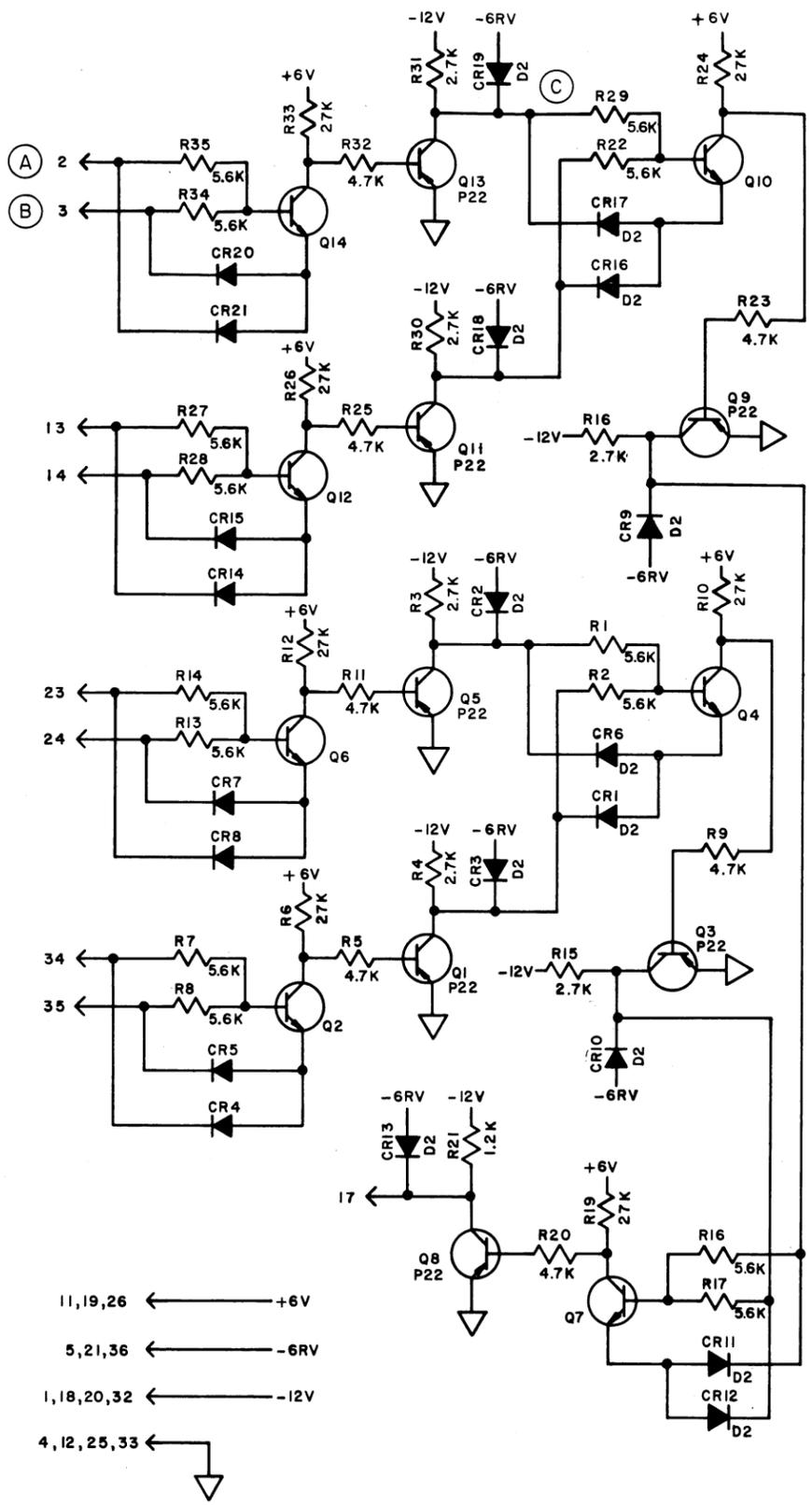C (COLLECTOR)
B (BASE)
BOTTOM VIEW OF TRANSISTOR
E (EMITTER)
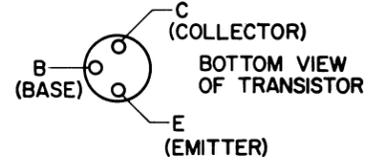
THIS CARD CONTAINS SEVEN EXCLUSIVE "OR" GATES CONNECTED TOGETHER TO FORM A PARITY TREE. A TYPICAL EXCLUSIVE "OR" GATE HAS THE FOLLOWING TRUTH TABLE (SEE TABLE BELOW) WITH INPUTS Ⓐ & Ⓑ BOTH AT 0 VOLTS OR AT -6 VOLTS, TRANSISTOR Q14 IS BIASED "OFF" AND THE COLLECTOR OF Q14 IS CLAMPED AT +6 VOLTS TO BIAS TRANSISTOR Q13 "OFF". THE OUTPUT Ⓒ IS CLAMPED AT -6 VOLTS. WITH INPUT Ⓐ AT 0 VOLTS AND INPUT Ⓑ AT -6 VOLTS OR INPUT Ⓐ AT -6 VOLTS AND INPUT Ⓑ AT 0 VOLTS, TRANSISTOR Q14 IS BIASED "ON". THE COLLECTOR OF Q14 WILL BE CLAMPED AT -6 VOLTS AND BIAS TRANSISTOR Q13 "ON". THE OUTPUT Ⓒ WILL BE CLAMPED AT 0 VOLTS. THE PARITY TREE CIRCUIT CONTAINS EIGHT INPUTS AND ONE OUTPUT. IF AN ODD NUMBER OF INPUTS IS AT 0 VOLTS, THE OUTPUT WILL BE CLAMPED AT 0 VOLTS. IF AN EVEN NUMBER OF INPUTS IS AT 0 VOLTS OR -6 VOLTS, THE OUTPUT WILL BE CLAMPED AT -6 VOLTS.

INPUTS		OUTPUT
Ⓐ	Ⓑ	Ⓒ
0 V	0 V	-6 V
-6 V	-6 V	-6 V
0 V	-6 V	0 V
-6 V	0 V	0 V

LOGIC SYMBOL

11,19,26 ← +6V
5,21,36 ← -6RV
1,18,20,32 ← -12V
4,12,25,33 ←