REPLACING PAGE ADDENDUM
Filing Instructions:

1. REMOVE FROM THE SECTION THE PAGES NUMBERED THE SAME AS THOSE ATTACHED TO THIS PINK SHEET.
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"DATASPEED"* TAPE RECEIVER

WITH ERROR DETECTION AND CORRECTION

TYPE 4B

DESCRIPTION AND OPERATION

1. GENERAL

1.001 This addendum, which supplements Section 592-812-100, Issue 1, is issued to incorporate engineering changes and to add coverage on the Timing Figures and EDC Module operation. Arrows in the margin indicate changes and additions.

1.002 Insert the attached pages in accordance with the filing instructions above.

Attached:
Page 7 dated April 1973, revised
Page 8 dated April 1973, reissued
Page 19 dated April 1973, revised
Page 20 dated April 1973, reissued
Page 21 dated April 1973, revised
Page 22 dated April 1973, revised
Page 23 dated April 1973, reissued
Page 24 dated April 1973, revised
Page 57 dated April 1973, reissued
Page 58 dated April 1973, revised

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DESCRIPTION AND OPERATION

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Prepared for American Telephone and Telegraph Company by Teletype Corporation

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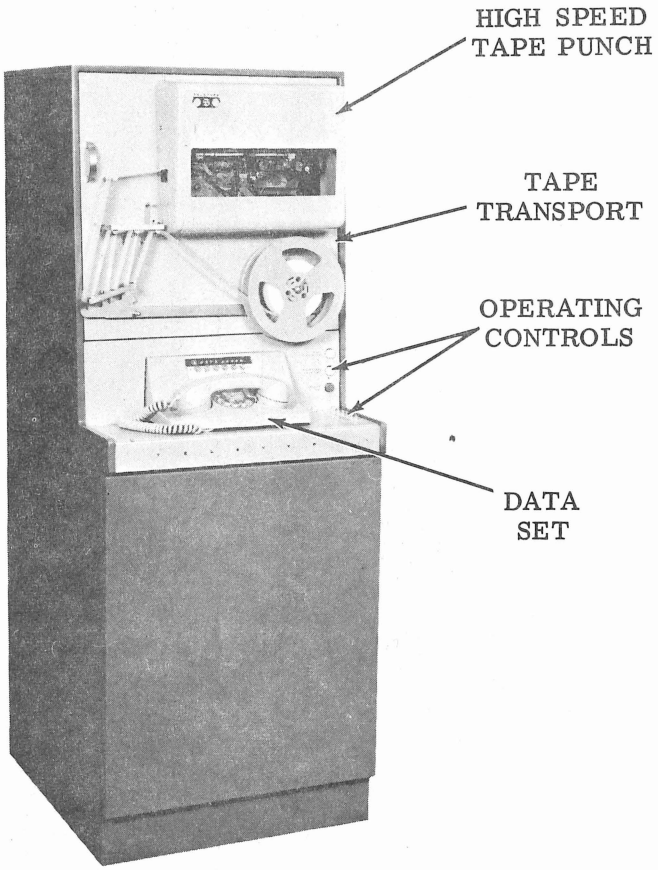

Figure 1 - Tape Receiver 4B

1. GENERAL

1.01 This section provides description and operation for the "DATASPEED" Tape Receiver, Type 4B, with automatic error detection and correction (EDC) capabilities. The receiver is used in a high speed punched tape data transmission system.

1.02 The major receiver components are a punch unit with photoreaders and back-up features, a tape transport, a station control module, a high speed receiver distributor and punch driver module, and an HSEDC (high speed error detection and correction) receiver control module. See Figures 1, 2, and 3. The receiver can operate over private lines or switched networks at a speed of 105 characters per second using either a 202C2 or a 202D2 type data set.

1.03 The receiver reproduces the transmitted punched tape which is identical to the transmitted message in every respect except for an extra 80 characters of delete (all marks) where an error has been detected. Data is transmitted in 80 character blocks with error detection being derived from redundancy information, in the form of two check characters, transmitted at the end of each block. Error correction is accomplished by retransmission of the errored block, the received errored block being deleted by overpunching with 80 all marks characters (rub out).

1.04 The receiver may be operated without the EDC (error detection and correction) feature.

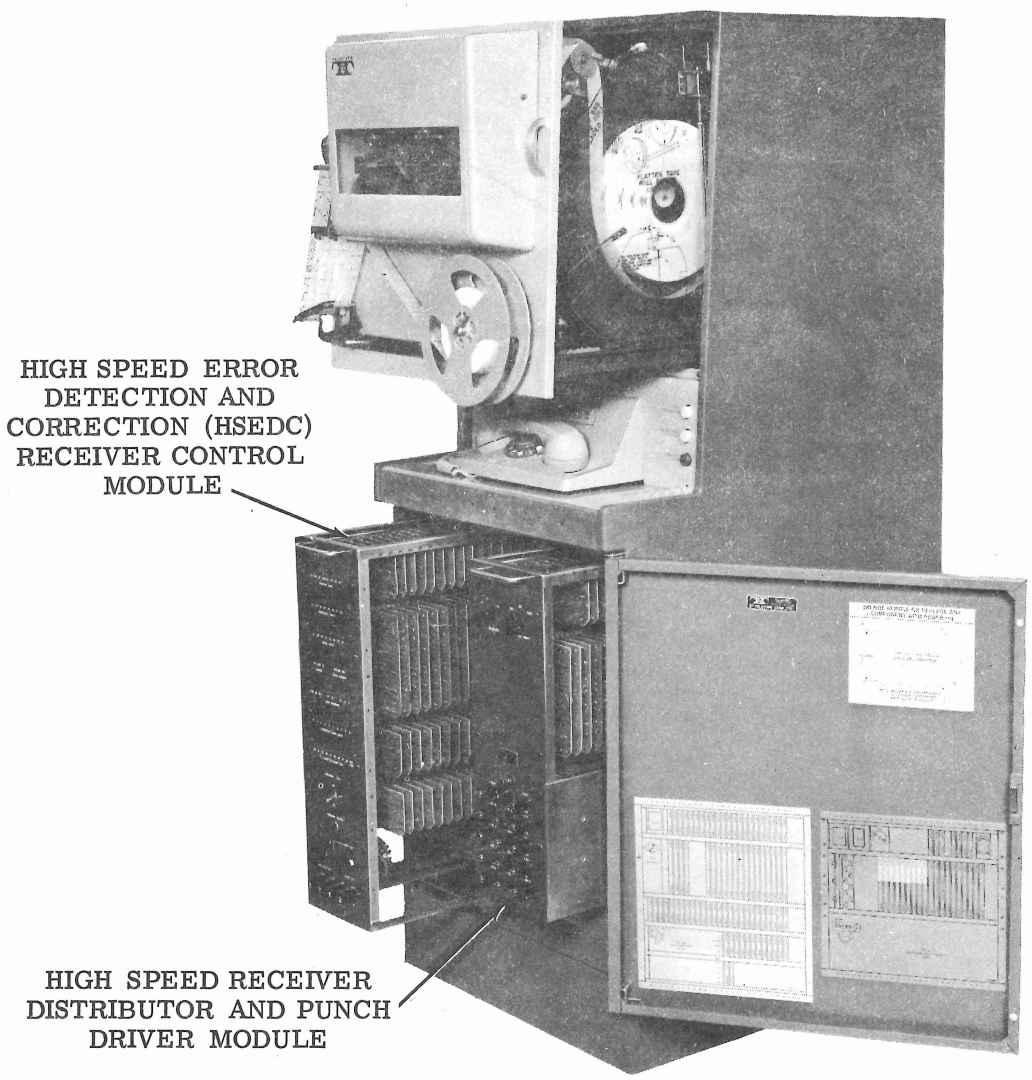

Figure 2 - Tape Receiver 4B

1.05 An alternate speed of operation is 120 Hz and requires the use of accessory equipment. See 3.22.

1.06 Refer to the appropriate sections for a description of the data sets, high speed tape punch, (DRPE-type), and for adjustment and servicing information for the receiver.

2. COMPONENTS

2.01 The receiver contains the following components or units:

(a) Cabinet

(b) Tape punch (equipped with back-up mechanism and photo verifier)

(c) Photo verifier light source

(d) Tape transport

(e) High speed receiver distributor and punch driver module

(f) Receiver station control module

(g) HSEDC receiver control module

(h) Receiver accessory module

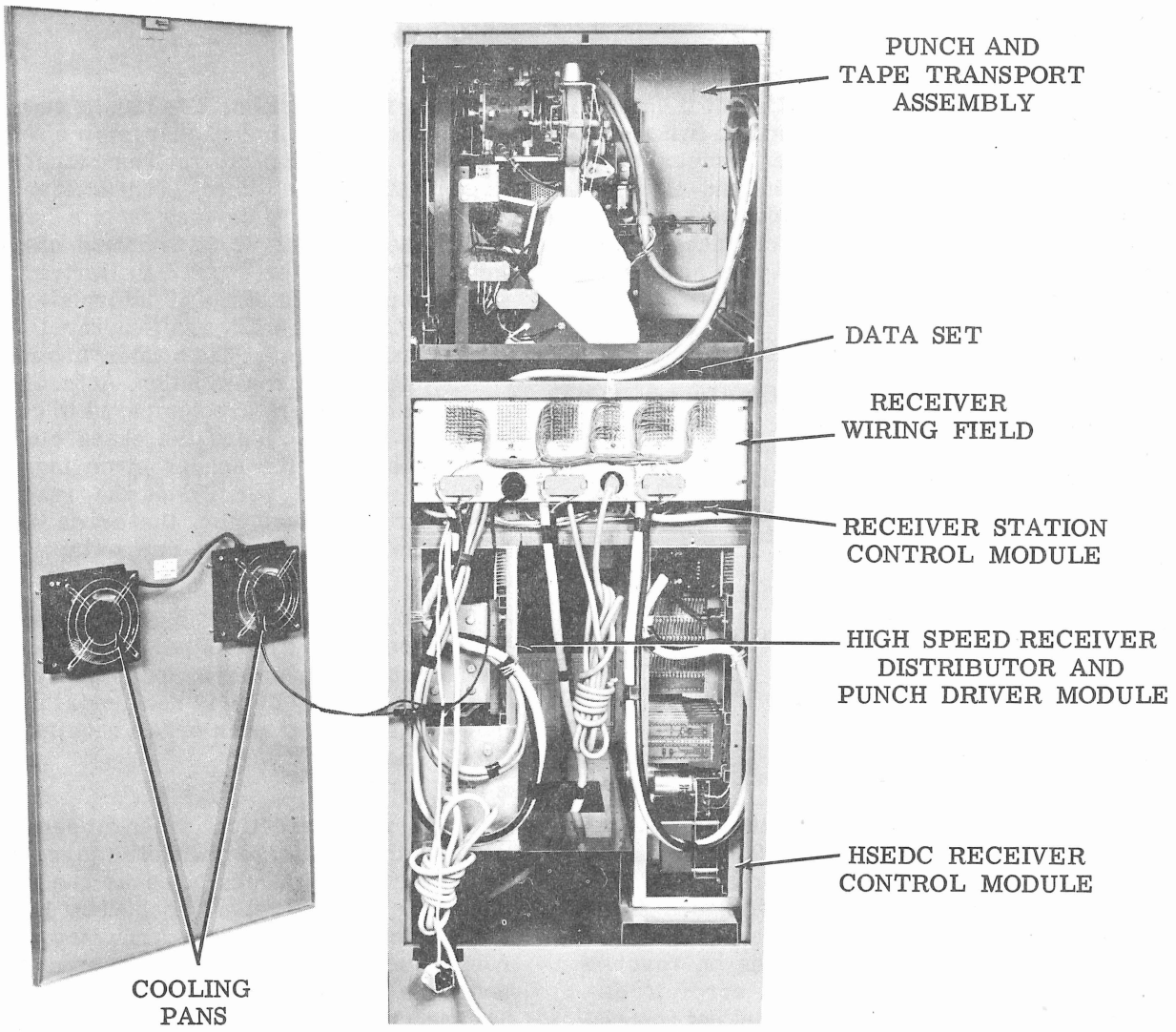

Figure 3 - Tape Receiver 4B, Rear View

2.02 Schematic wiring diagrams for the modules, contained in another section, are:

(a) HSEDC receiver control module 7063WD

(b) High speed receiver distributor and punch driver module 7412WD

(c) Receiver station control module 7406WD

(d) Punch and tape transport assembly 7042WD

2.03 The components are installed in the floor-mounted cabinet which also includes space for the data set.

3. TECHNICAL DATA

GENERAL

3.01 Code Type: A 10.0 unit, start-stop code is used. When 6 or 7 level tape is being read, the unused levels (7 and 8) will be trans-

mitted as marks, and when reading 5 level tape, level 1 will be transmitted as a space.

3.02 Input: The input to the receiver must be a standard EIA signal. The input data is received in blocks of 80 characters (when operating EDC), preceded by a block number character (BN), and followed by an end-of-block character (EOB) and two check characters (CK1 and CK2). The BN and EOB characters are fixed. The check characters will vary according to the transmitted data.

3.03 Output: The output is a 5 to 8 level tape which is a duplicate of the transmitted tape except for 80 characters of delete (all marks) data in the place where an error has been corrected. There are no other block indications. The punch can accept 5, 6, 7, or 8 level tape width. There is a 3000 foot tape supply and an 800 foot takeup reel.

3.04 Power Requirements: The receiver requires 115v ac at 4.5 amperes in standby, and 6.7 amperes when running.

OPERATIONAL FEATURES

3.05 Reverse Channel: The reverse channel feature of the 202C2 and 202D2 data sets is used as a control link from the receiver to the sender. When the sender is ready to send, it sends SR (sender ready) characters. Upon receipt of an SR, the receiver turns on reverse channel and keeps it on until an error is detected. Removal of reverse channel notifies the sender of the error, requesting a retransmission of the errored block.

3.06 Block Synchronization: After recognizing an SR character and turning on reverse channel, the receiver then looks for a block number character (BN). Three distinct block numbers are used for maintaining synchronization. The sender inserts a block number for each block sent and advances to the next block number. The receiver advances one block number for each block successfully received. If the received BN is lower than the one expected, the receiver leaves reverse channel on and waits for the correct BN before punching. If the received BN is high, it means a block has been missed so reverse channel is turned off to tell the sender to back up. When the sender sends the correct BN, that block will be punched. A block preceded by a BN that is low will be ignored. This feature is especially important in cases of momentary line breaks, unusual noise conditions, etc.

3.07 Error Detection: The tape is read by the photo verifier one character after it has been punched. The photo verifier output is used to generate the two check characters. Check character 1 (CK1 is derived from a horizontal parity check of the 80 information characters and check character 2 (CK2) is derived from a spiral parity check of the 80 information characters. CK1 and CK2 are generated by both sender and receiver. The sender inverts these characters before transmission. At the receiver, the check characters are compared to check the block for errors. Since the check characters are developed at the sender by an independent reading head and verified at the receiver by reading the product tape, the error detection loop actually extends from tape to tape.

3.08 End of Block: The EOB character is checked by the receiver after punching the last character of each block. If any character other than the EOB is received, this condition will be treated as an error, requiring error correction.

3.09 Error Correction: When an error is detected, reverse channel is turned off and the receiver mechanically backs the tape up 1 block (80 characters). This backup is counted electronically to verify its accuracy. The errored block is then deleted by overpunching all levels of the 80 characters of the errored block. The receiver then waits for the errored block to be retransmitted.

3.10 Figures Detect Circuit: When transmitting 5 level tape, a delete character will be interpreted as a letters character. The receiver stores the figures character and if it is present before a delete, an additional figures character is added to the tape before the next block is punched.

3.11 Feed Error Detect: A tape feed must occur every time a tape feed command is given to the punch to maintain synchronization between received character count and tape character count. If the tape fails to feed, an alarm is actuated by the feed level photoelectric reader. This could be caused by tangled, torn, or tight tape and represents a condition requiring operator attention.

MAINTENANCE AIDS

3.12 When the PUNCH TEST switch is turned on, the receiver will punch and verify any incoming data on a character by character basis. If any character is not verified, the punch is stopped and the malfunction can then be traced.

3.13 Indicator lamps are included which show various important program and logic states.

3.14 Plugable logic elements are used throughout for easy replacement.

3.15 With the PROGRAM TEST switch turned on, the programmer may be advanced manually for servicing.

3.16 The punch, back-up mechanism, and tape transport assembly are located on a slide-out front panel in the upper portion of the cabinet.

3.17 The module electronics is built on both small and large etched circuit boards and are located in the lower portion of the cabinet.

ACCESSORY FEATURES

3.18 The basic receiver provides for reception under manual control. It is capable of operating in the normal EDC mode or in a selectable non-EDC mode. In the non-EDC mode, the receiver is fully compatible with and can receive from any type 2 sender.

3.19 Unattended service wiring option, permitting the receiver to answer incoming calls automatically is included. This option is key controlled and low tape and alarm control can be added.

3.20 An available accessory feature (TP308512) is the protected unattended transmitter modification unit. This unit generates a discrete character which can be recognized by a sender equipped with the protected unattended transmitter recognizer unit. Data will not be sent by the sender equipped with this unit unless the proper code is recognized. If the sender has tape and is ready to send, data will be sent upon recognizing the authorized receiver. If the sender is not ready to send, a no traffic signal will be returned.

3.21 An available feature (TP308511) causes a vertical parity check bit to be generated for each character punched so that it may be compared to a similar check bit from the sender. This bit is transmitted in place of the 8th level in 5, 6, or 7 level data transmissions.

3.22 When operation at the alternate speed of 1200 wpm is desired, the following oscillator is required: Receiver LCO Oscillator, TP303137.

OPERATIONAL FEATURES (Figure 4)

3.23 A pushbutton (STOP/ALARM-RESET) is provided on the front panel for the operator to interrupt and stop transmission without breaking the telephone and data communications channel. This pushbutton will light when an alarm condition has been detected. After the malfunction has been corrected, the logic is reset by pushing the button.

3.24 A front panel indicator light (SENDER STOPPED) lights when the sender stops sending and carrier is not detected. Momentary stops are normal in EDC operation but if the condition lasts for longer than 30 seconds it indicates that the sender operator wishes to communicate over the telephone circuit. If the receiver is in unattended operation when this condition occurs, the receiver will be disconnected.

3.25 An indicator light (FLASH-LOW TAPE) is located within the power switch on the front panel. It provides a flashing signal when the tape supply is low.

4. METHOD OF OPERATION (Figure 4)

ATTENDED OPERATION

4.01 Before any operation, the paper supply must be checked to insure that enough supply is available for the incoming data. Empty the chad bag if a new 3000 foot supply roll is installed. Turn on the punch motors by depressing the AUX MOTOR START button. Thread the tape and check proper feed by depressing the BLANK FEED button. When proper feed is established, press the STOP/ALARM-RESET button if it is lighted.

Note: Whenever ac power is turned on to the receiver tape transport, the ALL FEED button must be depressed first to insure proper tape feed.

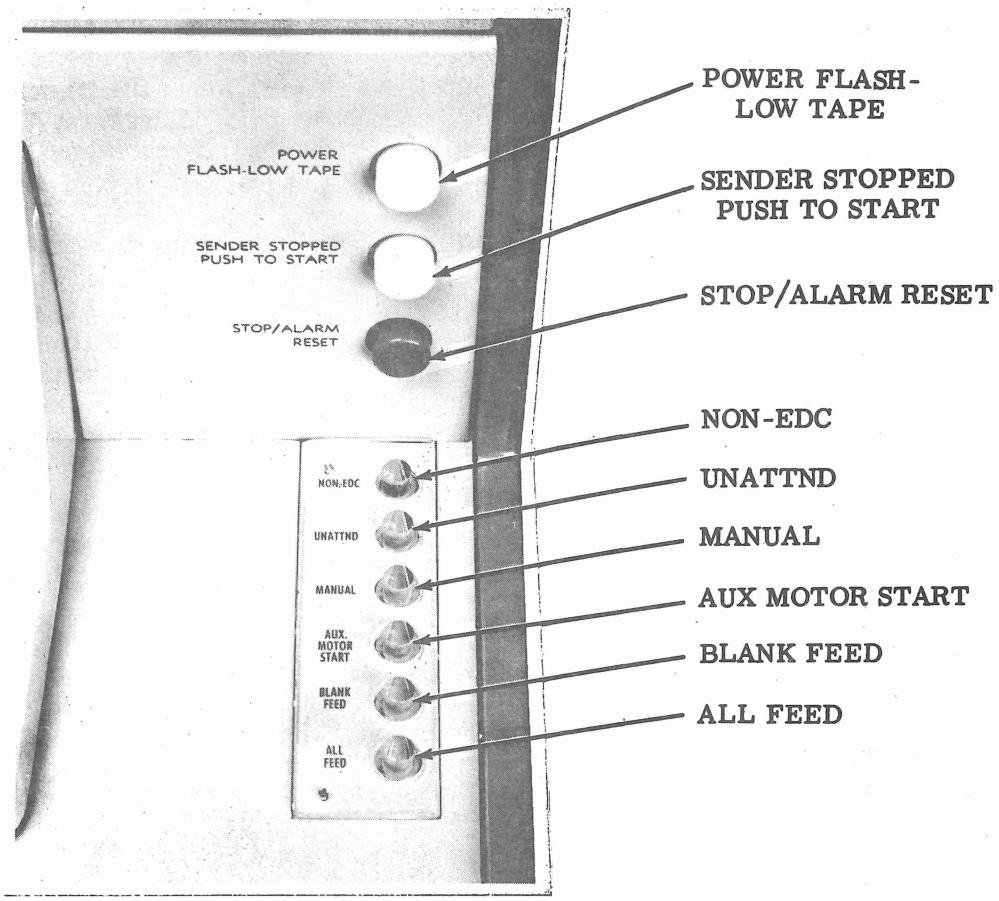

Figure 4 - Receiver Operating Controls

4.02 Select the mode of operation by depressing the MANUAL button for normal EDC operation or by depressing the NON-EDC button for NON-EDC operation. Either the sender or the receiver may initiate the call using the normal dialing procedure. After voice communication is established, the operator at the called terminal places his data set in the data mode first. A lamp under the TALK button on the data set will light if the terminal is the called terminal. Upon hearing the 2025 Hz tone, the operator at the calling terminal places his data set in the data mode. This will start the motors and transmission can begin. The operator at the receiver may stop transmission at any time by depressing the STOP/ALARM-RESET pushbutton. At this time he may:

(a) Resume transmission by resetting the STOP/ALARM-RESET button, or

(b) Drop the call, if the receiver is the calling terminal, by returning the data set to the talk mode and placing the handset on the hook, or

(c) Re-establish voice communication by returning the data set to the talk mode and waiting until the sender operator returns to the talk mode after which data transmission can be established as in (4.02).

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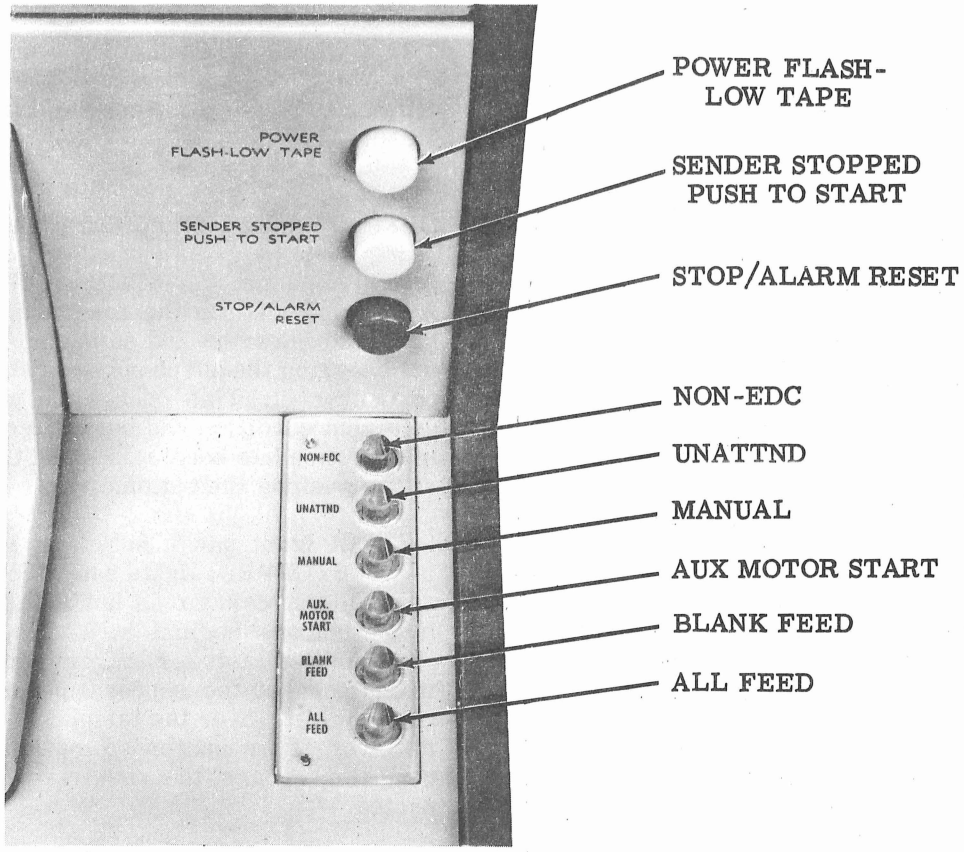


Figure 4 - Receiver Operating Controls

for NON-EDC operation. Either the sender or the receiver may initiate the call using the normal dialing procedure. After voice communication is established, the operator at the called terminal places his data set in the data mode first. A lamp under the TALK button on the data set will light if the terminal is the called terminal. Upon hearing the 2025 Hz tone, the operator at the calling terminal places his data set in the data mode. This will start the motors and transmission can begin. The operator at the receiver may stop transmission at any time by depressing the STOP/ALARM-RESET pushbutton. At this time he may:

(a) Resume transmission by resetting the STOP/ALARM-RESET button, or

(b) Drop the call, if the receiver is the calling terminal, by returning the data set to the talk mode and placing the handset on the hook, or

(c) Re-establish voice communication by returning the data set to the talk mode and waiting until the sender operator returns to the talk mode after which data transmission can be established as in (4.02).

UNATTENDED OPERATION

4.03 Depress the UNATTND button to prepare for unattended EDC operation. For unattended NON-EDC operation, the NON-EDC and UNATTND buttons must be pressed simultaneously. The set will now answer incoming calls automatically and will receive data when the sender begins transmission. Disconnect will be accomplished 30 seconds after end of transmission, low tape, or an alarm. The receiver will ignore incoming calls if an alarm or low tape condition exists.

CALLING AN UNATTENDED SENDER

4.04 The receiver calls an unattended sender in the same manner as if the sender were attended. The sender returns a tone upon answering and is ready to send when the tone stops. A sender which is not able to transmit will ignore incoming calls.

CALLING A PROTECTED UNATTENDED SENDER

4.05 If the sender called is protected with a protected unattended transmitter recognizer unit (3.20) it will answer the call as in 4.04. Before transmitting data, however, the sender must recognize a valid identification code. This code is sent from the receiver by depressing the SENDER STOPPED, PUSH TO START button. Normal transmission can then be accomplished. If no identification character is sent or the wrong character is sent, the sender will disconnect after 30 seconds.

TERMINAL CONTROLS AND INDICATING LIGHTS

A. Receiver Operating Controls (Figure 4)

4.06 Controls on the front vertical panel located to the right and slightly below the tape take-up reel include the following.

4.07 Power, Flash-Low Tape: This switch controls the ac power to the whole terminal. The switch is a two-state push button switch. One push closes the switch and the next push opens the switch. When the switch is closed, ac power is supplied to all modules of the terminal and the button will illuminate (white). If there is a LOW TAPE condition of less than 400 feet, a mercury switch on the tape supply closes and picks up a low tape (LT) relay in the station control. This relay energizes a flasher in the station control which flashes the POWER, FLASH-LOW TAPE light, which calls attention to the low tape condition. If the UNATTND button is also pressed, the UNATTND light will also flash, calling attention to the fact that an unattended terminal has a low tape condition.

4.08 Sender Stopped, Push to Start: Pressing this normally open pushbutton starts the discrete calling generator accessory, when the terminal is so equipped. This initiates a 14 bit code which a remote sender must recognize before transmission can begin. This button will light up an amber color when the sending terminal stops transmitting. Loss of carrier in the data set will cause the carrier detect lead to go to -6 volts. This will cause the CD relay in the station control to pick up and a normally open contact on the relay will close, illuminating the light.

4.09 Stop/Alarm, Reset: This normally open pushbutton is used to manually start and stop the terminal. The ST-HO relays in the station control operate as a binary counter and pressing this pushbutton will change the state of the relays. When the relays are picked up the pushbutton will illuminate a red color representing the stop/alarm condition. When the relays are dropped out, the light will be out, representing the reset condition. Thus, one press of the button will stop the terminal and the next press of the button will restart the terminal. The alarm condition will be produced if an alarm is detected in the EDC module. Three alarm conditions are possible:

(a) Feed alarm - produced if the tape fails to feed after each punch command.

(b) Back-up alarm - produced if the tape fails to back up properly when the terminal is correcting a detected error.

(c) Punch-test alarm - produced when a punch error has been detected when the terminal is operating in the punch test mode.

4.10 When any of the above alarm conditions exists, a 0 volt signal will appear on the input to a power amplifier in the EDC module causing it to saturate, which in turn causes the AL relay in the station control to pick up. A normally open contact on the AL relay will close, causing the ST-HO relays to go the stop/alarm condition.

4.11 The reset condition produced by momentarily pressing the pushbutton resets the ST-HO relays in the station control and causes a reset pulse to reset the logic in the EDC module.

4.12 Controls on the horizontal panel located just below the three pushbuttons described above include the following.

4.13 Non-EDC: This button is used for operating the receiving terminal with the error detection and correction features disabled. When this button is pressed, the terminal will punch all incoming data. The NON-EDC button is a normally open pushbutton switch that latches in the closed position when it is depressed. One side of the switch is grounded. A lead from the other side of the switch is strapped in the station control and goes on to the EDC module where it has its control action. When the switch is closed to ground, the EDC module is locked in the non-EDC mode.

4.14 This pushbutton illuminates whenever depressed indicating the non-EDC mode is present. The terminal may be operated in the non-EDC mode either attended or unattended by depressing two pushbuttons at the same time, the NON-EDC button, and the appropriate additional pushbutton. The NON-EDC pushbutton is released by depressing any one of the next three buttons (UNATTND, MANUAL, or AUX MOTOR START).

4.15 Unattnd: Pressing this pushbutton allows the terminal to respond to incoming calls automatically without the need for any operator, providing no alarm condition exists. This is a normally open pushbutton switch that latches in the closed position when it is depressed. When the switch is closed, it provides a path to ground to pick up the UA relay in the station control. A contact on the UA relay closes to ground causing the UNATTND button to light. This light will be shut off if an alarm condition occurs and it will be flashed if a low tape condition exists.

4.16 The UNATTND button may be pressed at the same time as the NON-EDC button as described in 4.13. The UNATTND pushbutton is released by pressing any one of the other of the first four pushbuttons (ie, NON-EDC, MANUAL, AUX MOTOR START).

4.17 Manual: This pushbutton does not have a switch associated with it. Pressing the MANUAL pushbutton releases the three latching pushbuttons (NON-EDC, UNATTND, AUX MOTOR START). The MANUAL pushbutton will illuminate whenever the UNATTND or AUX MOTOR START pushbuttons are not depressed.

4.18 Aux Motor Start: This pushbutton is a normally open latching pushbutton switch. When it is depressed, it provides a path to ground which picks up the MS relay in the station control which starts the motors of the terminal. Whenever it is depressed, the AUX MOTOR START pushbutton will light up and neither the UNATTND light or the MANUAL light can illuminate. This is because the AUX MOTOR START button is intended to be used only for off-line terminal set up and any other lights would be meaningless.

4.19 When the MS relay picks up, several normally open contacts close. The motor for the punch and the tape transport become energized. The lamp for the photo verifiers turns on.

4.20 Blank Feed: This is a normally open momentary pushbutton switch. When it is depressed, it provides 0 volt potential to the feed lead of the receiving distributor which starts the feed out oscillator. (This lead is strapped in the station control.) If the motors are running in the terminal, the tape will feed out blank tape with only feed holes punched. There is no light in this button.

4.21 All Feed: This pushbutton performs the same operation as the BLANK FEED button just described with all punch levels being primed so an all marks character is punched in addition to each feed hole. This is used for quickly determining if all levels of the punch are working. The feed drive lead from the receiving distributor is strapped in the station control and then goes to the EDC module for gating, and returns to the receiving distributor as the letters drive signal to drive all punch levels of the punch drivers. This button does not contain a light.

B. HSEDC Receiver Control Module (Figure 5)

4.22 Controls located on the front panel of the module include the following.

4.23 Program Test: When this switch is on, it puts the module into a condition which allows the programmer to be manually advanced for testing purposes.

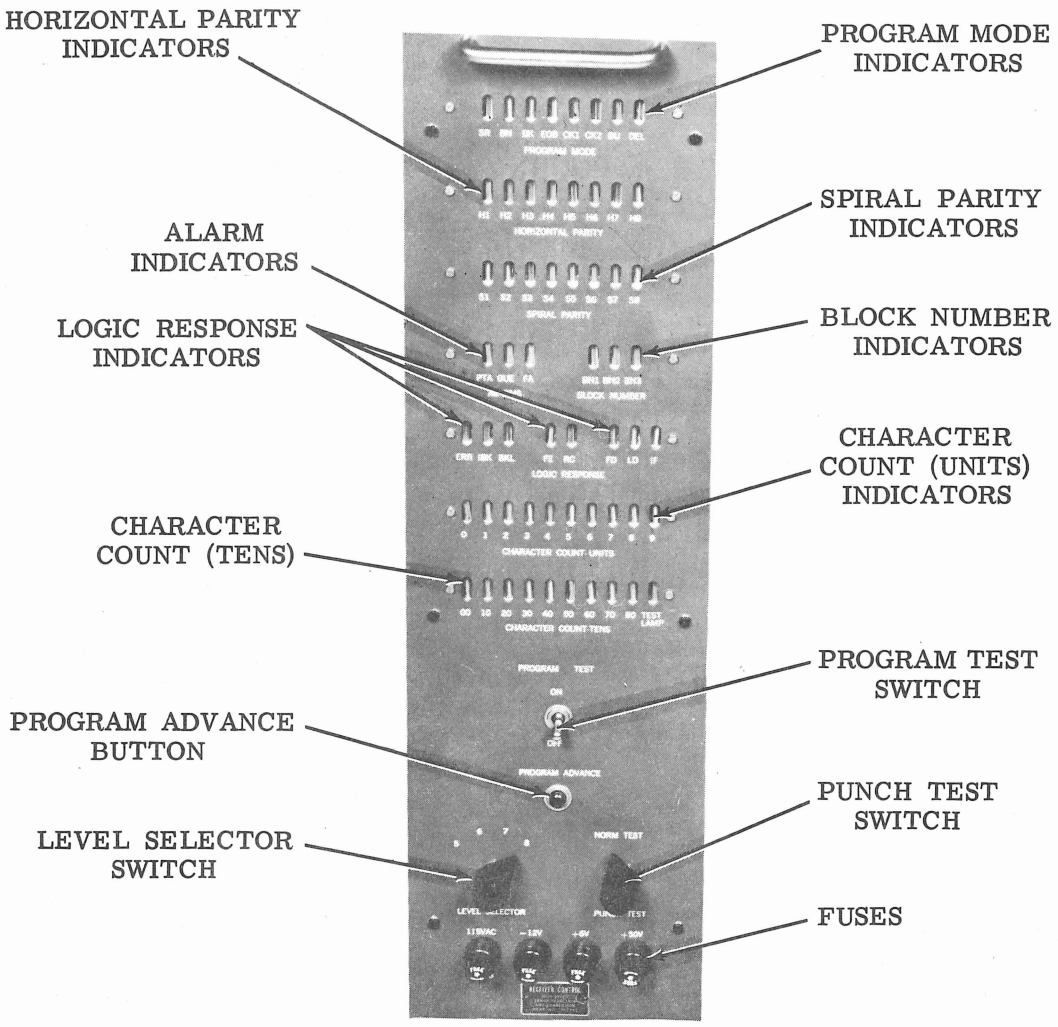


Figure 5 - HSEDC Receiver Control, Module B, Front View

4.24 Program Advance: This pushbutton switch is used to advance the programmer when the PROGRAM TEST switch is on. Each press of the pushbutton advances the programmer to the next mode following this sequence: SR, BN, BK, EOB, CK1, CK2, BU, DEL, and then back to SR.

4.25 Level Selector: This rotary switch must be pointing to the proper level of data reception when operating EDC. It makes the necessary adjustments to the check character generators.

4.26 Punch Test: When this rotary switch is placed in the TEST position the terminal will operate in the punch test mode wherein all incoming data will be punched and compared on a character-by-character basis. Punching will continue until an error has been detected, with the punch being stopped immediately.

4.27 The following indicator lights are provided for information on terminal operation, type of alarm present, reverse channel operation, and other test information.

4.28 Program Mode: These lights will light one at a time, from left to right, to show which mode the terminal is in (SR, BN, BK, EOB, CK1, CK2, BU, DEL).

4.29 Horizontal Parity and Spiral Parity: The horizontal parity lights follow the states of the horizontal check character register. They

can be used to help spot bad levels in the register. The spiral parity lights follow the states of the spiral check character register. They do not display the proper check characters when the receiver is stopped.

4.30 Alarms: Alarms are indicated as follows:

(a) PTA — lights when an error has been detected while operating in the punch test mode (punch test alarm).

(b) BUE — lights when the back-up mechanism has failed to properly back the tape up (back-up error).

(c) FE and FA — when both lights are lighted, a punch command was not followed by a corresponding feed pulse from the photo verifier, meaning that the tape did not move (feed error and feed alarm).

4.31 Block Numbers: The block numbers BN1, BN2, BN3 will light one at a time, indicating the number being generated in the module. At the beginning of transmission, the BN can be checked if necessary.

4.32 Logic Response: Logic response indications are as follows:

(a) ERR — shows when an error has been detected. In normal operation it is normal for this light to flash on and off momentarily, even though no error has been detected.

(b) IBK — shows when an incomplete block has been received. The incomplete block will be completed with fill characters and will then be corrected.

(c) BKL — lights when a received block number is low and resynchronization is taking place.

(d) FE — lights when a punch pulse is received and goes out when the corresponding photo feed pulse is received.

(e) RC — shows when reverse channel is turned on.

(f) FD — when receiving 5-level data, this light shows the presence of a FIGS character (levels 2, 3, 5, 6 marking using 8-level numbering).

(g) LD — shows when the letters character (all levels marking) has been detected.

(h) IF — lights when the insert FIGS register is set and the figs character will be inserted after a delete.

4.33 Character Count - Units and Character Count - Tens: This electronic counter counts the 80 characters during the BK mode, BU mode, and DEL mode.

4.34 Test Lamp: This lamp can be used to detect -6 volts dc and 0 volts dc when trouble-shooting the electronic circuitry (-6 volts = not lighted, 0 volts = lighted).

C. High Speed Receiver Distributor and Punch Driver Module (Figure 6)

4.35 Controls located on the front panel of the module are as follows:

4.36 Level Selector: This rotary switch must be set to the proper level data being received. This switch prevents the unused levels from being punched in the tape when operating at 5, 6, or 7 levels.

4.37 Vertical Parity: This switch selects ODD or EVEN vertical parity when the terminal is equipped with the vertical parity accessory.

4.38 Baud: This switch is located on the top rail of the module, immediately behind the front panel and has two positions. Placing it down to 1050 BAUD activates an internal oscillator for the terminal clock. Throwing the switch up to 2000/2400 BAUD selects the external data set clock for the terminal. (This feature is not presently available.)

TERMINAL SET UP

4.39 Turn power on by pressing the POWER pushbutton. Press the AUX MOTOR START button to start terminal motors.

4.40 Loading Tape: Load a new roll of tape if there is an insufficient supply for the incoming messages. The LOW TAPE light will flash with less than 400 feet of supply tape. Pull the punch assembly out to check supply; follow decal on tape supply.

Note: Always empty chad bag before installing a new 3000 foot roll of tape.

4.41 Depress the BLANK FEED button to see if tape is feeding properly.

4.42 Depress the ALL FEED button to see if all punch levels are operating properly.

4.43 Correct any punch difficulties and press the RESET button if the red light is lighted.

4.44 Depress the MANUAL, UNATTND, and/or NON-EDC button(s) to select mode of operation desired.

ESTABLISHING A CALL

4.45 If the terminal is to be an unattended called terminal, press the UNATTND button.

4.46 To place a call, press the TALK button on the data set and dial in the normal manner.

4.47 When the operator at the calling terminal hears a tone, he places his data set in the data mode by depressing the DATA button. A light will illuminate under the button when the data set is in the data mode.

RECEIVER STATION CONTROL MODULE

4.48 The receiver station control module (Figure 7) provides an interface between the data set and the receiver. The signals to and from the data set are EIA standard RS232B interface signals. The receiver station control module converts the incoming and outgoing signals. EIA signals are converted to system signals. The following table applies to EIA signals.

Data - Binary State	One	Zero
Data - Signal Condition	Marking	Spacing
Paper Tape	Hole	No Hole
Voltage	Negative	Positive
Control Function	Off	On

4.49 The signals have the following electrical characteristics. The input control voltages do not exceed ±25 volts dc with respect to signal ground. Minimum voltages which will be accepted for control should be ±3 volts dc. Signal conditions are not defined when the terminal voltages are in the range -3 volts dc to +3 volts dc. Maximum short circuit between any two leads (including ground) should not exceed one-half ampere.

4.50 The data terminal ready (DTR) lead from the receiver station control module to the data set is always held in the on condition, +6 volts dc, except during the ringing cycle. When ring indicator comes on, +6 volts dc, it causes the DTR lead to go off, -6 volts dc. This will stay at off if the station is not unattended and if a low tape or alarm condition exists so the data set will not go the data mode. Thus if the receiver is the calling station, ringing will never occur and the data set must be put into the data mode by manually pressing the DATA button. When the operator interrupts the ringing cycle by answering the call manually, the data set will go into the data mode when the DATA button is pressed.

4.51 Approximately 100 ms after the data set goes into the data mode, the data set ready (DSR) lead from the data set will turn on, +6 volts dc. This will operate the DSR relay in the station control which will start the motors in the terminal and will turn on the light for the photo verifier. A contact on the DSR relay enables the receiver station control module to detect carrier. When carrier is detected in the data set, the carrier detect (CD) lead will come on, +6 volts dc. This will be detected in the receiver station control module where a reverse channel blind will be removed, and the SENDER STOPPED light will be turned off. The punch blind lead from the receiver station control module to the receiver distributor and punch driver module will go to -6 volts dc and will enable the punch.

4.52 With carrier on, the serial data will now appear on the received data lead of the data set. From here the data goes to the receiver station control module where it is converted to normal system signals and then sent to the high speed receiver distributor and punch driver module.

RECEIVER DISTRIBUTOR

4.53 The timing for the receiver distributor (Figure 6) is derived from a start-stop oscillator located in the high speed receiver distributor and punch driver module. The output of the start-stop oscillator is a square wave with a period of 0.952 milliseconds.

4.54 The receiver distributor is prevented from operating as long as a mark (stop bit, 0 volt dc) appears on the receive data lead. When a start bit (spacing, -6 volt dc) appears on

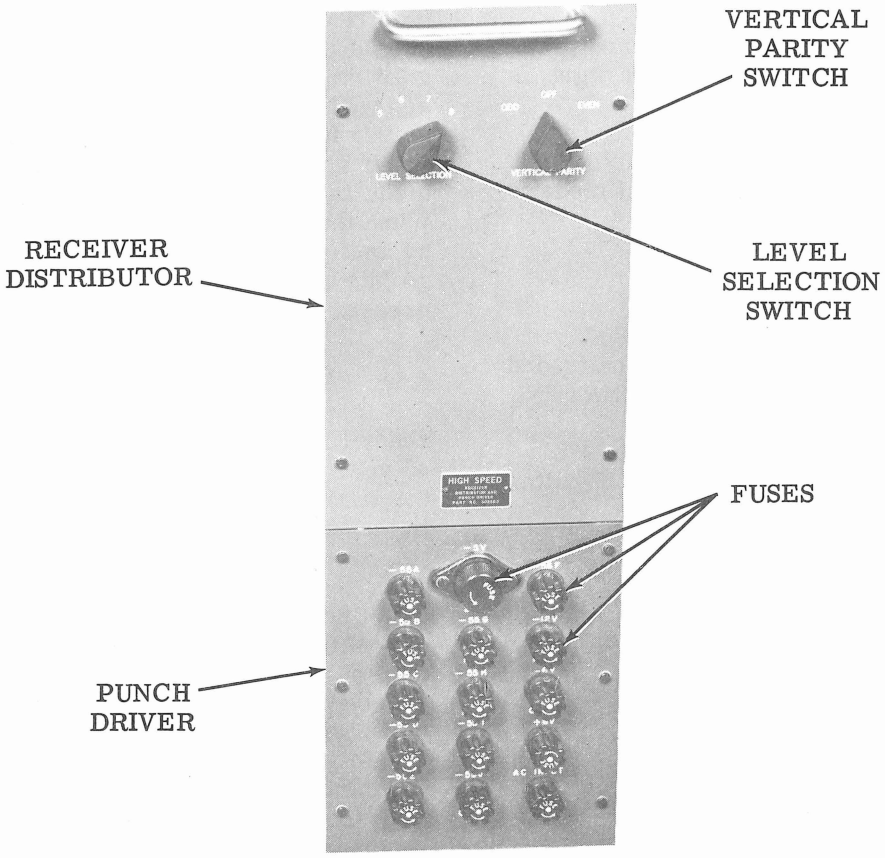


Figure 6 - High Speed Receiver Distributor and Punch Driver, Module D, Front View

the receive data lead, the receiver distributor will be started. The clock pulses advance the incoming character into the shift register bit by bit. When the character is fully into the distributor and is ready to be read out, a positive going pulse, -6 volts to 0 volt, one bit wide will appear on the character sample lead. The character appears in parallel form on the 8 data level leads of the receiver distributor for the total duration of the character sample. Signals on the data level leads are all normal system signals with -6 volts dc a space and 0 volt dc a mark. The character sample appears on the RD sample lead of the EDC module. After a character sample pulse is sent, the distributor stops and will not respond until the start of the next character appears on the receive data lead.

REVERSE CHANNEL

4.55 When operating in the EDC (error detection and correction) mode, the receiving terminal uses the reverse channel feature of the data sets to communicate with the sending terminal. Reverse channel can be either on or off. Each state is used to notify the sender to take certain actions such as begin transmission, retransmit or resynchronize. The EDC module turns reverse channel on by placing -6 volts dc

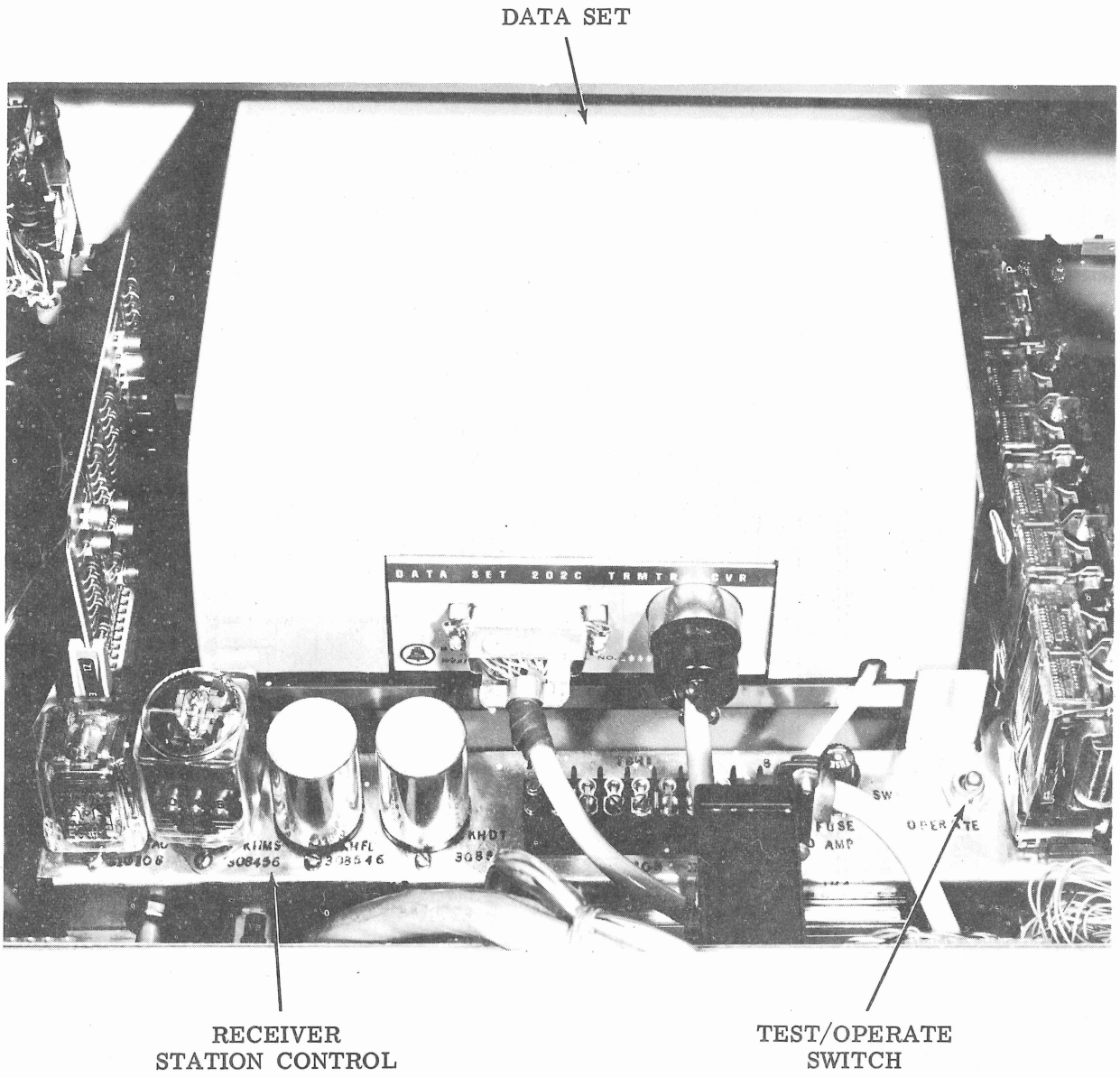


Figure 7 - Receiver Station Control, Module H, Top-Rear View

on the send reverse channel lead. This is gated in the station control with other reverse channel blinds and is converted from a neutral signal (-6 volts dc) to a polar signal (+6 volts dc) before being presented on the send reverse channel lead of the data set for transmission on the telephone line. To turn reverse channel off, the EDC module places 0 volts dc on the send reverse channel lead and the data set will turn off reverse channel. Reverse channel will always be turned off in the stop/alarm condition.

5. GENERAL OPERATION

ERROR DETECTION AND CORRECTION OPERATION

A. Programmer Operation

5.01 The high speed error detection and correction (HSEDC) receiver control module controls the operation of the receiver terminal. The control functions are selected and performed

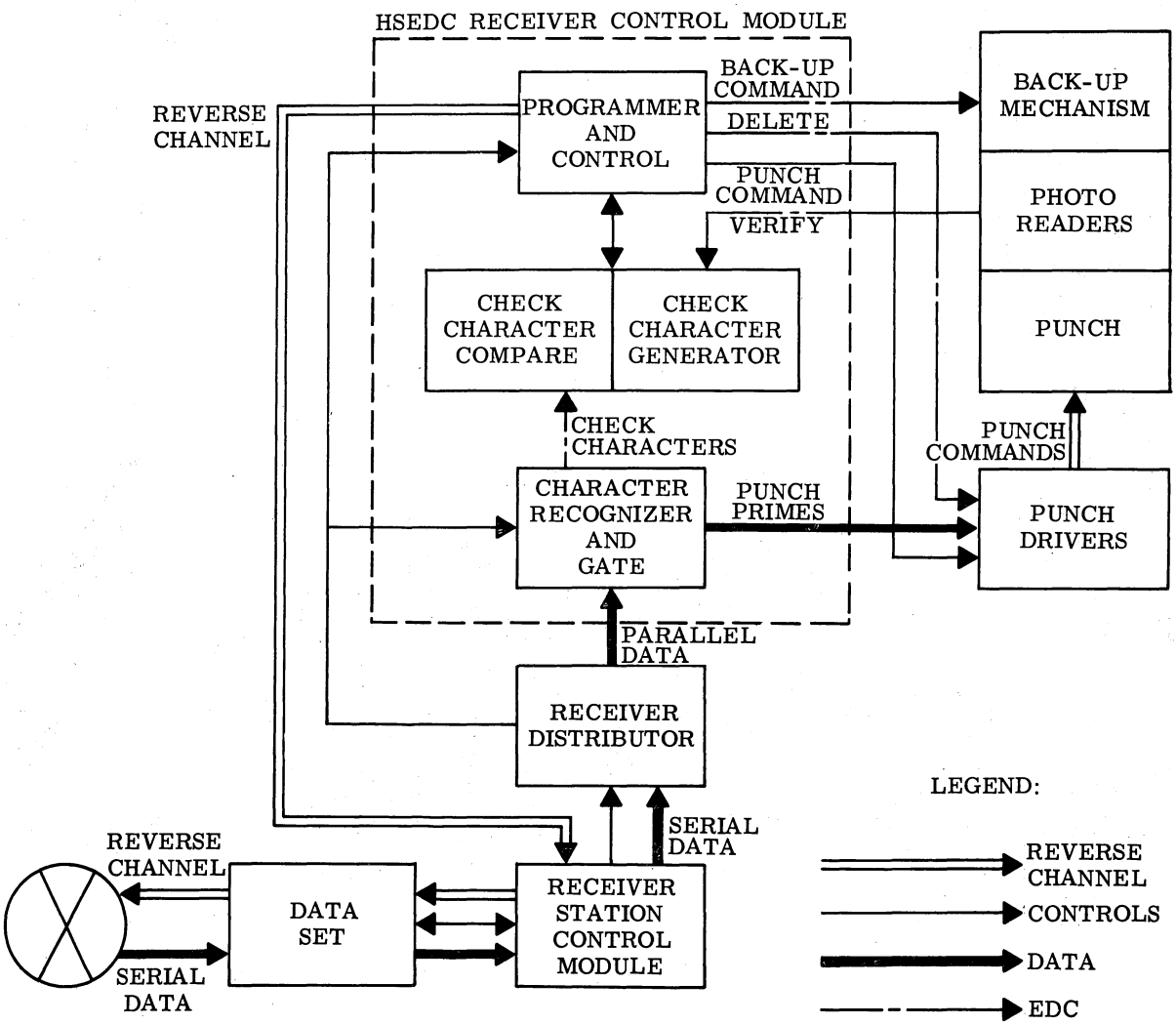


Figure 8 - Block Diagram of Tape Receiver 4B

by the programmer in the module. Figure 8 shows a simplified block diagram of the receiver and Figure 9 shows the logic for EDC operation of the receiver. The programmer has eight modes and certain actions are taken in each mode. The programmer advances to each mode sequentially and in the following order: SR mode, BN mode, BK mode, EOB mode, CK1 mode, CK2 mode, BU mode, DEL mode, and then back to the SR mode.

5.02 When power is first turned on, the programmer will advance through its sequence until it reaches the SR mode. This may cause a delete cycle to occur but should cause no operational difficulties.

5.03 With the programmer in the SR mode the EDC module will do nothing until it detects an SR character (levels 1, 5, 6, 7 marking). The programmer advance pulse is a positive going pulse -6 volts dc to 0 volts dc, 10 microseconds wide, occurring 50 microseconds after the leading edge of the RD sample pulse (see Figure 10). When an SR character is detected, a gate is primed so that the programmer advance pulse can advance the programmer into the BN mode.

5.04 When the programmer steps into the BN mode a flip-flop is set which turns reverse channel on. Additional SR characters are applied to an inhibit gate which prevents programmer advance pulses from advancing the programmer. The programmer will not advance until a character that is not an SR is received. In EDC operation the first non-SR character will be a block number (BN). This character will advance the programmer to the BK mode and will set the error block register enabling the terminal to check for errors.

B. Block Number Synchronization

5.05 Block numbers are used for maintaining synchronization between sender and receiver to insure that no data is lost, especially when stopping and restarting the terminals and in cases of momentary interruption of transmission. The three possible block numbers are fixed 8 level characters:

(a) BN1 - levels 1, 3, 6, 8 marking

(b) BN2 - levels 2, 4, 5, 7 marking

(c) BN3 - levels 1, 2, 7, 8 marking

5.06 The block numbers are generated in a 3-element ring counter which is advanced one number after each successfully received block (block advance pulse). The incoming block numbers are recognized in a diode matrix which yields a 0 volt output at the appropriate terminal, ie, BN1 detected, BN2 detected, or BN3 detected. The locally generated block number is compared to the incoming block number using nine two input AND gates. Three AND gates have inputs that are the same BN. When an output occurs from one of these three gates the BN-OK condition is detected. The other 6 AND gates compare unlike block numbers. Three of these conditions are detected as BN-high and the remaining three are detected as BN-low, depending on whether the received BN is lower or higher than the locally generated one.

5.07 A BN-high condition primes the reverse channel register so that the next RD sample pulse will shut off reverse channel.

5.08 A BN-low condition will set the block low register flip-flop which will prevent the block advance pulse from advancing the block counter. The punch will be blinded and the incoming characters will be counted.

5.09 With the BN-OK condition the error block register will be primed so that an error free block will be detected as correct.

5.10 Regardless of the BN condition the first non-SR character advances the programmer into the BK (block) mode.

C. Block Mode

5.11 When the programmer is in the BK mode, a gate is primed which allows the RD sample pulse (delayed 50 microseconds) to produce the gated clock pulse. The gated clock pulse drives a 2ms one-shot which provides the punch sample pulse for driving the punch. The punch sample pulse, thus, is a positive going -6 volts dc to 0 volt dc, 2 milliseconds wide, occurring 50 microseconds after the RD sample pulse. (See Figure 11.) The gated clock is inhibited when a block low condition exists, thus preventing the punch from punching.

5.12 The punch primes are eight leads which go from the HSEDC receiver control module to the punch drivers in the high speed receiver distributor and punch driver module.

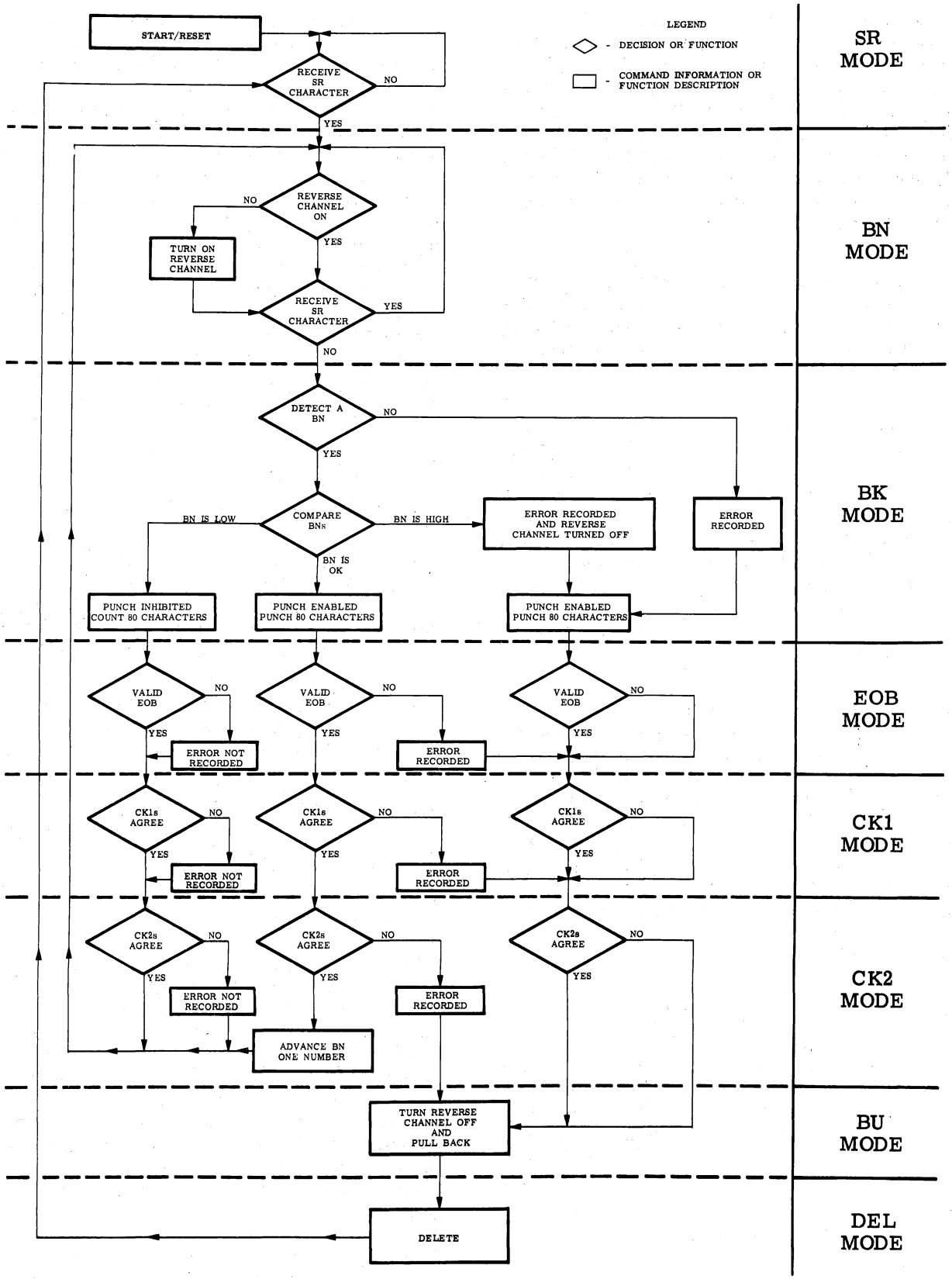
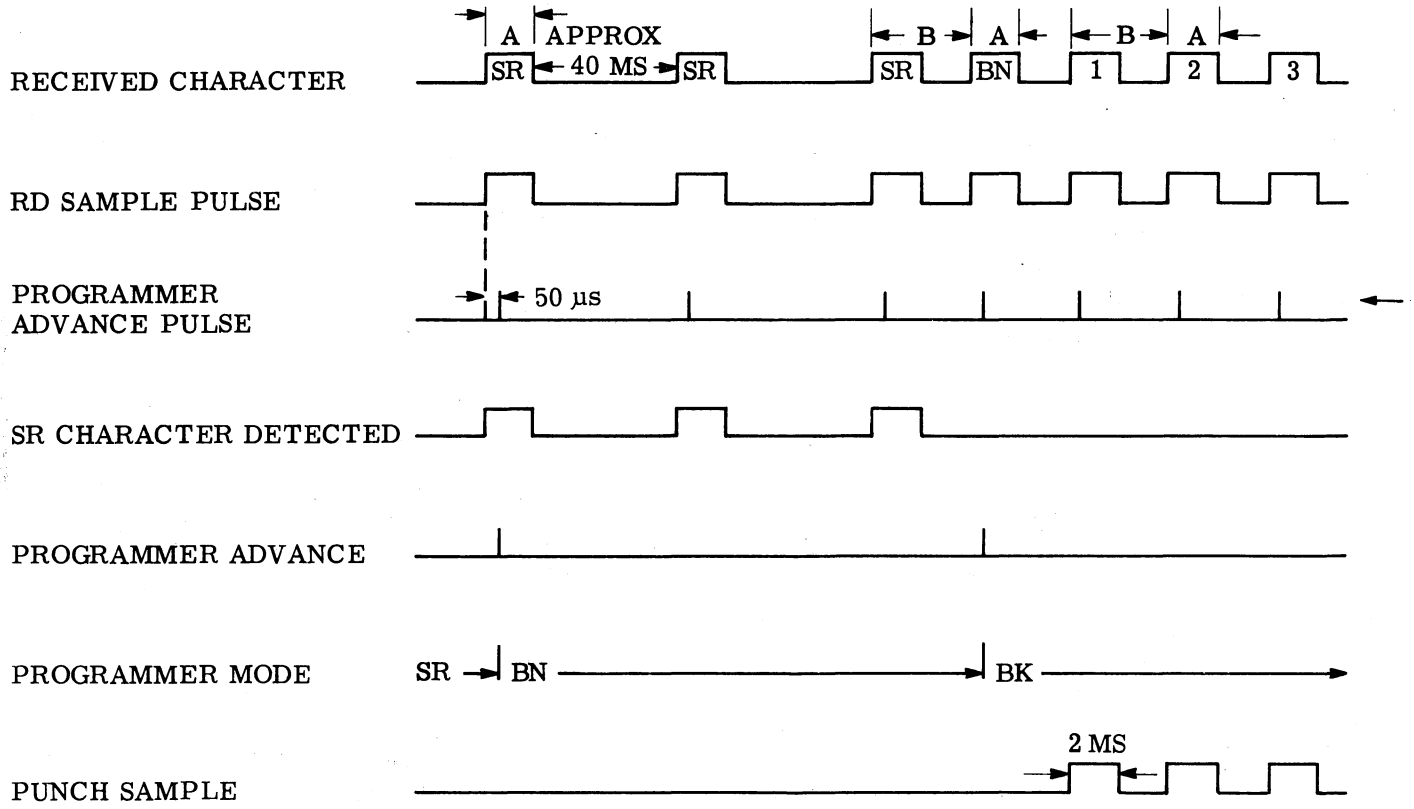


Figure 9 - Receiver EDC Logic



TIMING CHANGES WITH SPEED CHANGES

SPEED	A	B	C	D
1050 WPM	0.953 MS	9.53 MS	9.53 MS	6.0 MS

Figure 10 - SR to BN to BK Timing

The punch primes are derived from the eight data levels from the receiver distributor. A -6 volt dc signal on a lead represents a space for that level so that punch driver level will not be primed. A 0 volt dc signal primes that punch level. The punch primes are gated in the HSEDC receiver control module to provide an all-mark signal for deleting or to provide an all mark except for level 4 spacing for a FIGS insert signal (using 8-level numbering).

5.13 With the punch levels primed, the punch sample pulse goes from the HSEDC receiver control module to the receiver distributor where it causes the punch drivers to shut off the appropriate punch magnets. Each of the 9 magnets of the punch has two leads from the punch drivers. Refer to the appropriate section for a description of punch operation. Basically, the magnets are picked up by a -55 volt dc voltage of about 1.4 ms duration and then held up by a -5 volts dc holding voltage. When a particular level is punching, the voltage is shut off for 1.9 milliseconds.

5.14 When receiving 7 level tape, place the LEVEL SELECTOR switch on the receiver distributor in the 7 level position. This will prevent the 8th level from punching. Similarly, in the 6 level position, the 7th and 8th levels will not punch. In the 5 level position, the 1st, 7th, and 8th levels will not punch. If the switch is not placed in the proper position, the 1st level will punch a space (start signal) and the 7th and 8th levels will be punched as marks (stop signal).

D. Photo Verifier Operation

5.15 Each of the eight data levels and the feed level of the punch has a photo verifier cell which senses a hole that has been punched. The location of the photo verifier is one hole displaced from the punching position. After a character has been punched, the tape feeds and the character just punched will come in position to be read by the photo verifiers.

5.16 The photo verifiers have a common supply voltage of -6 volts dc, which comes from the receiving distributor and is applied to the emitters of the photo verifiers. A voltage of +6 volts dc is applied to each collector individually with 9 leads from the HSEDC receiver control module, which are strapped in the high speed receiver distributor and punch driver module, and then go to the photo verifiers in the punch. With no light falling on an individual photo verifier, the collector will stay at +6 volts dc. With the presence of light on the verifier, it will conduct, causing the collector to go to -6 volts dc. The feed level will always produce an output which is used to check for proper tape feeding.

E. Feed Error Detect

5.17 After each character is punched, the tape will feed and the feed level photo verifier will sense the web of the tape moving. This yields the photo reader feed pulse (see Figure 11) which is delayed 50 microseconds from the 0 voltage crossing of the feed photo verifier output.

5.18 The feed alarm detect is accomplished by using two flip-flops. The punch sample sets the feed alarm prime register and the corresponding photo reader feed pulse resets the register, removing the prime. If the tape doesn't feed and the prime register is not reset, the next punch sample will set the feed alarm register, and the receiver will be stopped in an alarm condition.

F. Check Character Generation

5.19 In the BK mode, the incoming data will be punched, with each character being read by the photo verifier immediately after the tape has fed to the next position. The photo verifier outputs are used to generate the two check characters, CK1 and CK2.

5.20 Check character 1 (CK1) is a horizontal character generated by presenting the output from a particular photo verifier level to the same flip-flop for the duration of the 80 character block. The verifier output is gated by the character set pulse (see Figure 11) which is the output of a 200 microsecond one-shot triggered by the photo reader feed pulse. The flip-flops are reset to the zero state before reading in the first character. Each mark that is detected will change the state of the flip-flop. Thus an even number of marks after 80 characters results in a zero state and an odd number of marks results in a one state. At the end of 80 characters, the states of the 8 flip-flops represents the CK1 character.

5.21 Check character 2 (CK2) is a spiral character generated in a similar manner to CK1. However, after each character has been

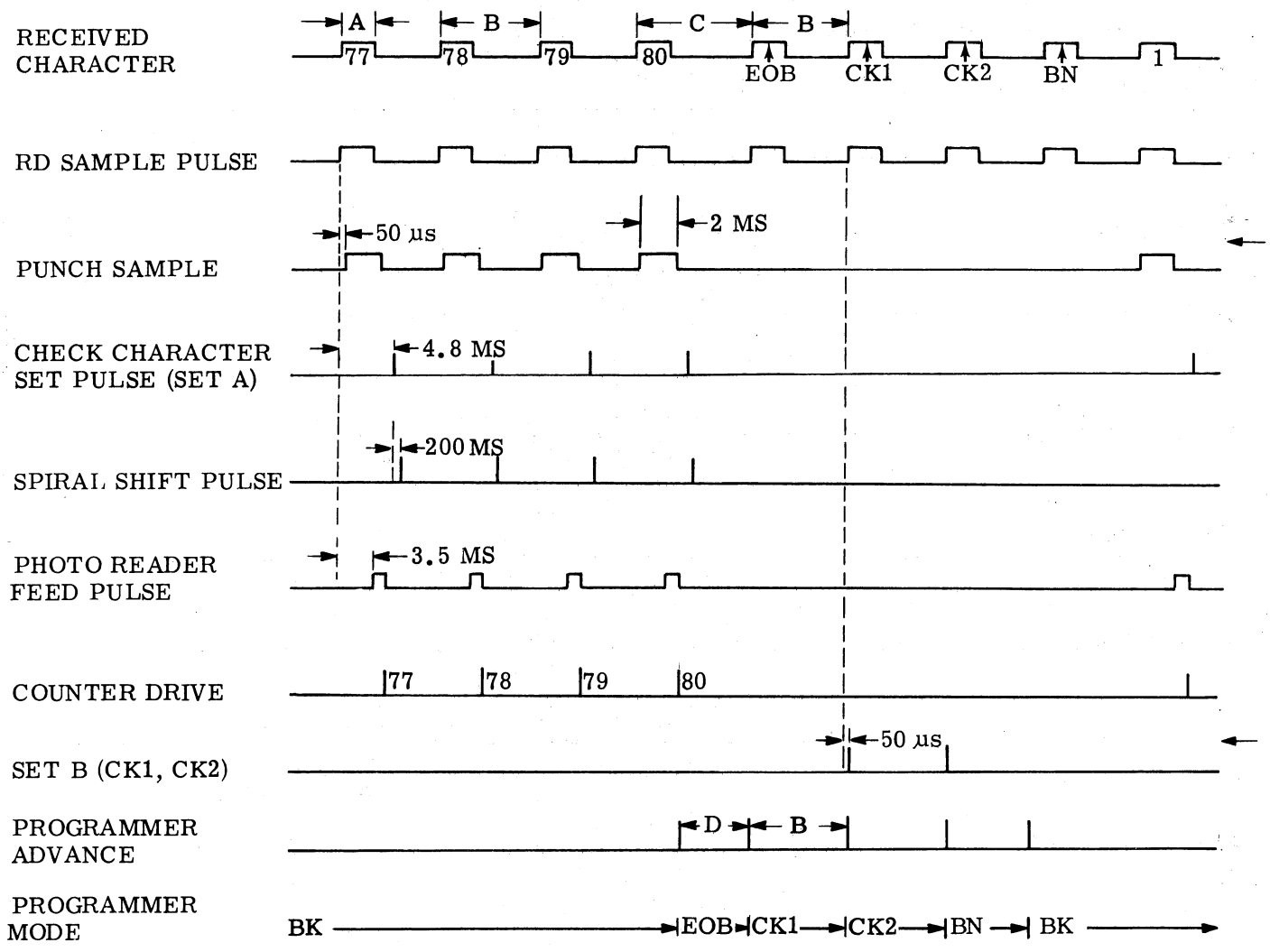


Figure 11 - BK to EOB to CK1 to CK2 to BN Timing

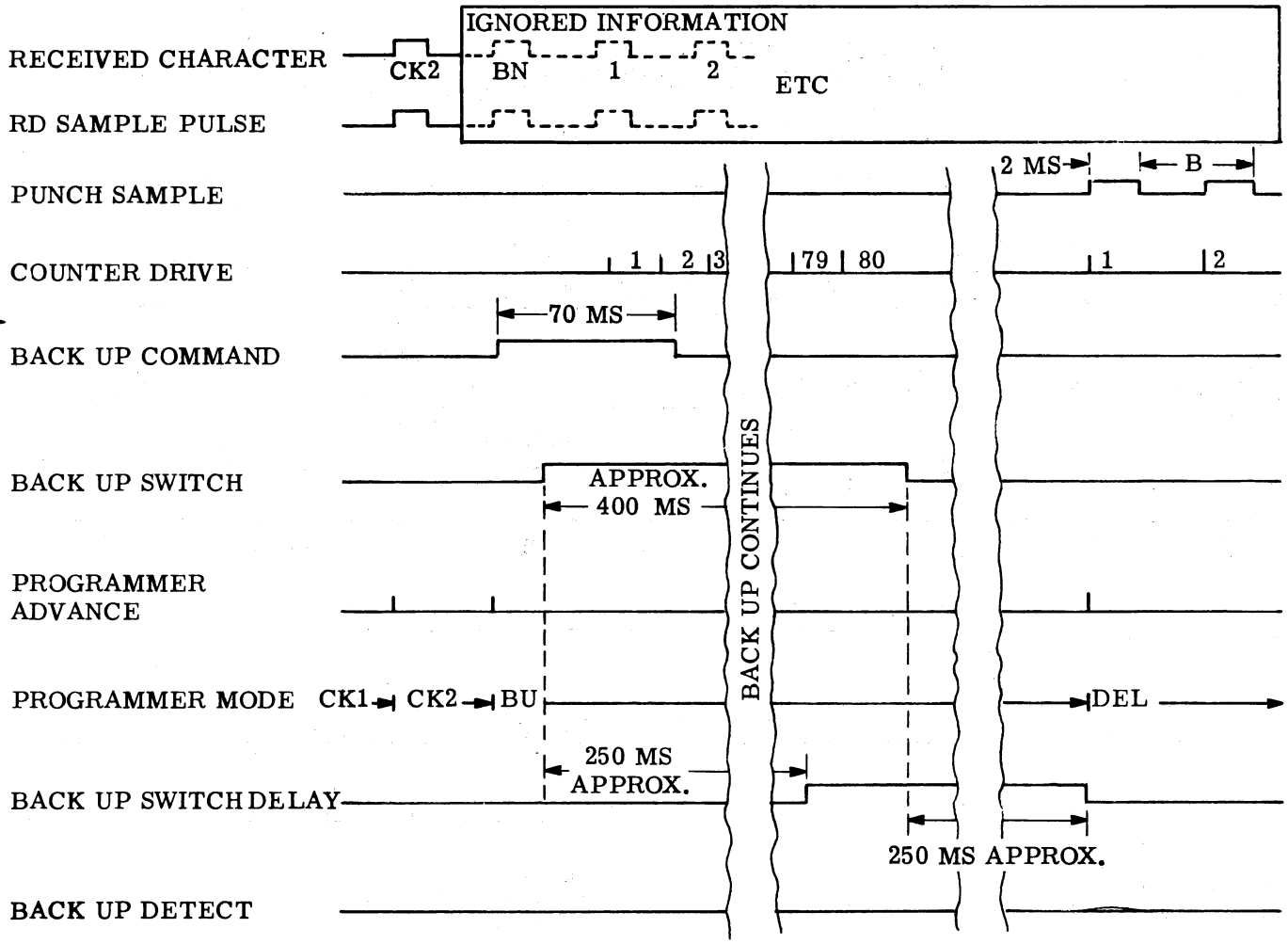


Figure 12 - CK2 to BU to DEL Timing - With Error

read into the flip-flops, the information is transferred to the next higher flip-flop. Thus, a mark in the 2nd level will cause the 3rd level flip-flop to change states and a mark in the 8th level will change the state of level 1, etc. The states of the 8 flip-flops at the end of 80 characters represents the CK2 character.

5.22 In generating the check characters when 7 level data is being received, the 8th level of each character in the 80 character block is always read as a mark. When 6 level tape is being received, the 7th and 8th levels are always read as marks. When 5 level tape is being received, the 7th and 8th levels are always read as marks and the 1st level is always read as a space.

G. Character Counter

5.23 The character counter contains a 10-element ring for counting units and a 9-element ring for counting tens up to 80. When the block is being punched, the character counter counts the photo reader feed pulses until 80 have been received. (If the punch is inhibited because of a block low condition, the RD sample pulses are counted). When the tens counter steps from the 70 to 80 condition, a block complete pulse is generated which causes the programmer to step into the end of block (EOB) mode.

5.24 In the EOB mode, the EOB character is checked by the EOB character control. The EOB character is a fixed 8-level character with a spacing bit in the 1st level and marking bits in the 2nd, 3rd, 4th, 5th, 6th, 7th, and 8th levels of the character. If the EOB character is not detected, an error is recorded, requiring an error correction sequence. In the EOB mode, the last punched character is over the photo verifier so the last character is read into the check character registers. In the EOB mode, there is no inhibit to the programmer advance pulse so the programmer steps into the CK1 mode when the next RD sample pulse occurs.

5.25 In the CK1 mode the incoming data character will be the CK1 that has been generated by the sender. The received CK1 is inverted in form from the CK1 that is locally generated. After reading the incoming CK1 into the horizontal register, all flip-flops should come up in the one state if no error exists. The inverted outputs are sampled and if an error has occurred in any level the flip-flop for that level will be in the zero state, and an error is detected. The CK1 character is inhibited from being read into the CK2 register. Again no inhibits are present for the programmer advance pulse so the programmer steps into the CK2 mode when the next RD sample pulse occurs.

5.26 In the CK2 mode, the incoming CK2 character is read into the CK2 register and it is not shifted because there is no photo reader feed pulse. Error checking is the same as for CK1 of 5.25.

5.27 When in the CK2 mode the next programmer advance pulse will advance the programmer. If no error has been detected the programmer will be returned to the BN mode and transmission will continue. (See Figure 11.) If an error does exist, the programmer will step into the back up (BU) mode. (See Figure 12.)

5.28 In the BU mode, the reverse channel register is reset, shutting off reverse channel. The back-up control is triggered causing a 70 millisecond pulse from a one shot to saturate a power amplifier which provides a circuit to ground for the punch reverse feed magnet. The armature of this magnet is connected to a clutch on the back-up mechanism. Energizing the magnet causes the back-up mechanism to back up the tape exactly 80 characters. The magnet supply is -12 volts dc from the EDC module, strapped in the receiving distributor, and supplied to one side of the magnet coil. The other side of the magnet coil returns to the receiving distributor where it is strapped to go on to the EDC module and the punch reverse feed power amplifier. The photo reader feed pulses are counted while the tape is backing up. At the end of the back-up cycle, the back-up switch on the back-up mechanism opens causing a positive voltage step from -6 volts dc to 0 volt dc to be sent to the EDC module. The -6 volts dc supply comes from the EDC module and is strapped in the receiving distributor and sent on to the back-up switch. The switch return is also strapped in the receiving distributor and goes to the back-up error control of the EDC module. When the 80th character has been counted on back-up, the output of the 80 counter is gated with the BU mode to provide a signal which verifies that the tape has backed up 80 characters. It is then compared with the switch opening pulse. If 80 characters have been counted, a back-up detect pulse (Figure 12) is generated. If 80 characters have not been counted, a back-up error is recorded and the terminal is stopped with the back-up alarm light on. A successful back-up detect causes the programmer to advance to the delete (DEL) mode.

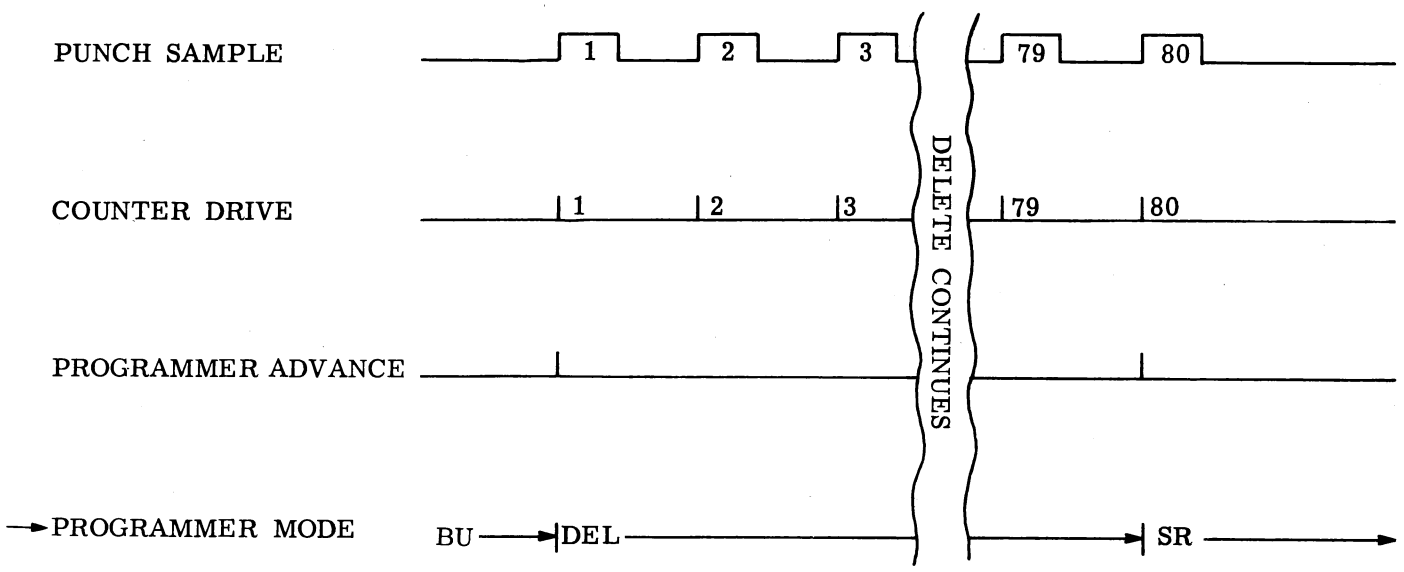


Figure 13 - DEL to SR Timing

5.29 In the DEL mode the incoming RD sample pulses are inhibited and a clock generator is started in the EDC module to provide the gated clock pulses which provide the punch sample pulses (see Figure 13). All punch prime levels are held at 0 volts dc so an all mark character (delete) will be punched. Each punch sample will cause one delete character to be punched. The punch samples are counted by the character counter until 80 characters have been punched. As in the BK mode, programmer advance pulses are inhibited and the block complete pulse (when 80 characters have been punched) advances the programmer to the next mode. In this case the programmer is returned to the SR mode. Transmission can continue only after the sender has completed its back up and again sends SR characters.

NON-EDC OPERATION

5.30 The receiver is capable of operating with the error detection and correction feature disabled so that it can receive from remote terminals without the EDC feature. (At 1050 words per minute, the receiver can receive from any type 2 sender.) Non-EDC operation is selected by pressing the NON-EDC pushbutton on the control panel. When the button is pressed, the terminal will be primed to operate in the non-EDC mode.

5.31 A call is established and the terminal is prepared for data transmission in the manner described in Part 4. The terminal is ready to receive as soon as the NON-EDC pushbutton is pushed. The terminal will begin punching as soon as data is received. The programmer will be locked in the SR mode but a BK mode signal will be generated. This will allow any RD sample pulse to pass through and be transformed into the punch sample pulse. The 8 data leads will be sent straight through without change. As a result, all incoming information will be punched, regardless of content. If the remote sender is an EDC sender and EDC data is being transmitted, all control and check characters will be punched. This method can be used to check whether a sender is generating and sending the correct SR, BNs, block, EOB, and check characters.

5.32 When in the non-EDC mode the feed alarm circuit will be disabled. All EDC functions will be disabled. Reverse channel will be held on so that a remote terminal can be told that the receiver is ready to receive.

STOPPING NON-EDC TRANSMISSIONS

5.33 The reception of data can be stopped as follows:

(a) By pressing the STOP/ALARM-RESET button. This will stop the punch immediately and will shut off reverse channel. Due to propagation time, the sender will have sent more data before detecting reverse channel off. Also, the reader will not back up when in the non-EDC mode. Thus, before restarting transmission, the sending terminal operator must manually back the tape up about 50 characters so no data will be lost. To restart transmission, press the STOP/ALARM-RESET button again.

(b) By pressing the MANUAL button. This will take the terminal out of the non-EDC mode and will place the terminal in the EDC mode. If the remote sender is not sending EDC information, transmission will stop. If the remote terminal is sending EDC information, transmission will continue in the EDC mode of operation.

(c) By pressing the TALK button on the data set. This will instantly stop the punch and will shut off reverse channel. Transmission is re-established by pressing the DATA button on the data set.

STOPPING EDC TRANSMISSIONS

5.34 The receiving terminal can be stopped in three different ways. It can be automatically stopped by the remote terminal; it can be stopped manually by the action of the receiving terminal operator; or it will be stopped automatically if any alarm is present in the receiving terminal.

5.35 The remote terminal can stop the receiver by stopping data transmission. The incomplete block circuit (5.38) will complete the last 80 character block and then that block will be deleted. The receiver will then return to the SR mode, looking for a retransmission of the incomplete block. Transmission will not begin until an SR character is detected. With no transmission being received, carrier detect will be off from the data set and the indicating light SENDER STOPPED will be on. This light being on for several seconds indicates that the operator at the remote terminal wishes to communicate to the receiver operator over the telephone channel. The operator can establish voice communication by lifting the data set handset, pushing the TALK button on the data set and waiting until the remote terminal's operator comes on the line. To re-establish data communication, the operator at the called station places his data set in the data mode by pressing the DATA button. When the operator at the calling station hears a tone on the telephone line, he places his data set in the data mode by depressing the DATA button.

5.36 The receiver operator can manually stop the receiver in two ways. The primary means of manually stopping the receiver is to depress the STOP/ALARM-RESET button. This pulls in the ST and HO relays in the station control and stops the terminal. This essentially inserts an error into the last 80 character block being received and shuts off reverse channel. The remainder of the 80 character block will be punched, then backed up and deleted. When the sender detects reverse channel off, it will back up two blocks. At this point the operator can go to the talk mode by lifting the handset and pushing the TALK button. Data communication can begin again by returning the data set to the data mode. If the receiver was stopped by pressing the STOP/ALARM-RESET button only, transmission can be resumed by pressing the button again.

5.37 The receiver will stop automatically if an alarm condition occurs at the terminal. If a feed alarm is detected, the punch will stop on the character that produced the error. If a back-up alarm occurs, the terminal will be stopped in the BU mode. A low tape condition is merely a warning and does not stop transmission. Only when the tape is completely gone will the feed alarm stop the terminal. In all of these alarm conditions, reverse channel will be shut off and operator intervention is required to correct the alarm condition. The STOP/ALARM-RESET button will light to indicate the alarm condition. In order to start again, the alarm condition must be corrected and the STOP/ALARM-RESET button must be pressed.

INCOMPLETE BLOCK CIRCUIT

5.38 The incomplete block circuit provides a means for finishing the punching of a block when data transmission is stopped, either intentionally or accidentally. Loss of the RD sample pulse allows the recycle timer to set the incomplete block register. This starts the clock generator and inhibits any further RD sample pulses. The clock generator then provides the pulses which yield punch sample pulses and the rest of the block will be punched. The programmer will go through its normal cycle, checking the check characters for errors. An

error has been recorded by the recycle timer so the block that has been punched will be deleted. When the programmer steps into the BU mode, the incomplete block register will be reset and the register will be reset again when stepping from the SR mode into the BN mode. The recycle timer is set to accept the SR rate without turning on. However, any data rate slower than the SR rate will turn it on. During normal transmission the incomplete block register will be reset with each block advance pulse. After an alarm condition, the incomplete block register will be reset when pressing the STOP/ALARM-RESET button. The incomplete block circuit is held off when operating in the non-EDC mode.

FIGURES DETECT CIRCUIT

5.39 When receiving 5 level data, a problem arises from the fact that a delete character corresponds to a letters character of the 5 level code. Thus, if a figures (FIGS) character were present in the block before a delete, the letters character would be detected last because of the delete. Therefore, the HSEDC receiver control module has a circuit for detecting both the figures and the letters characters.

FIGS = levels 2, 3, 5, & 6 marking
LTRS = levels 2, 3, 4, 5, & 6 marking.

5.40 Basically, the circuit has a FIGS detect register for remembering the presence of a FIGS character. If a FIGS character was present at the time of an errored block the FIGS insert register is set. After the errored block is deleted, the programmer steps back into the SR mode. When stepping out of the SR mode, an additional punch sample is generated and the punch primes present the FIGS character so it will then be punched. The FIGS detect register will then be reset when the programmer steps into the BK mode. The insert FIGS register will be reset with the next block advance pulse. The product tape will contain an extra FIGS character after each delete, wherever necessary.

PUNCH TEST MODE

5.41 This circuit provides a means for locally testing the punch and the associated circuitry. Punch test is selected by placing the PUNCH TEST switch in the TEST position. The terminal is locked into the non-EDC mode wherein all incoming data is punched. The spiral check character register becomes the punch test 1st storage. The incoming character is read into the 1st storage as it is being punched. The horizontal check character register becomes the punch test 2nd storage. The character is read into the 2nd storage 2 milliseconds later. When the punched character is stepped it can be read by the photo verifier. The punched character will then be read into the 2nd storage. If the correct character has been punched, all flip-flops of the 2nd storage will be returned to the zero state. Two hundred microseconds later, the 2nd storage will be sampled and if a 1 state exists in any level, a punch test alarm will be recorded and the system will be stopped on the errored character. The PTA indicating light will show the presence of the error. If no error is found the next RD sample pulse will reset the 1st storage and the process of punching and checking will continue. After an error has occurred, the punch test circuit is reset by returning the PUNCH TEST switch to the NORM position.

6. HIGH SPEED RECEIVER DISTRIBUTOR AND PUNCH DRIVER MODULE

GENERAL

6.01 The high speed receiver distributor and punch driver module is located in the lower right-hand section of the receiver cabinet. The module may be pulled forward for servicing. An interior view of the module is shown in Figure 14.

6.02 Diagrams associated with the module, contained in another section, are:

- 7412WD - High speed receiver distributor and punch driver module schematic diagram
- 6405WD - Multivoltage power supply (TP148851) schematic diagram
- 7413WD - High speed receiver distributor and punch driver module actual wiring diagram
- 6406WD - Multivoltage power supply actual diagram

6.03 References in the following circuit descriptions are to the above schematic diagrams.

6.04 The distributor is built around a 10-element shift register consisting of 10 flip-flops designated R0 through R9. R0 is the

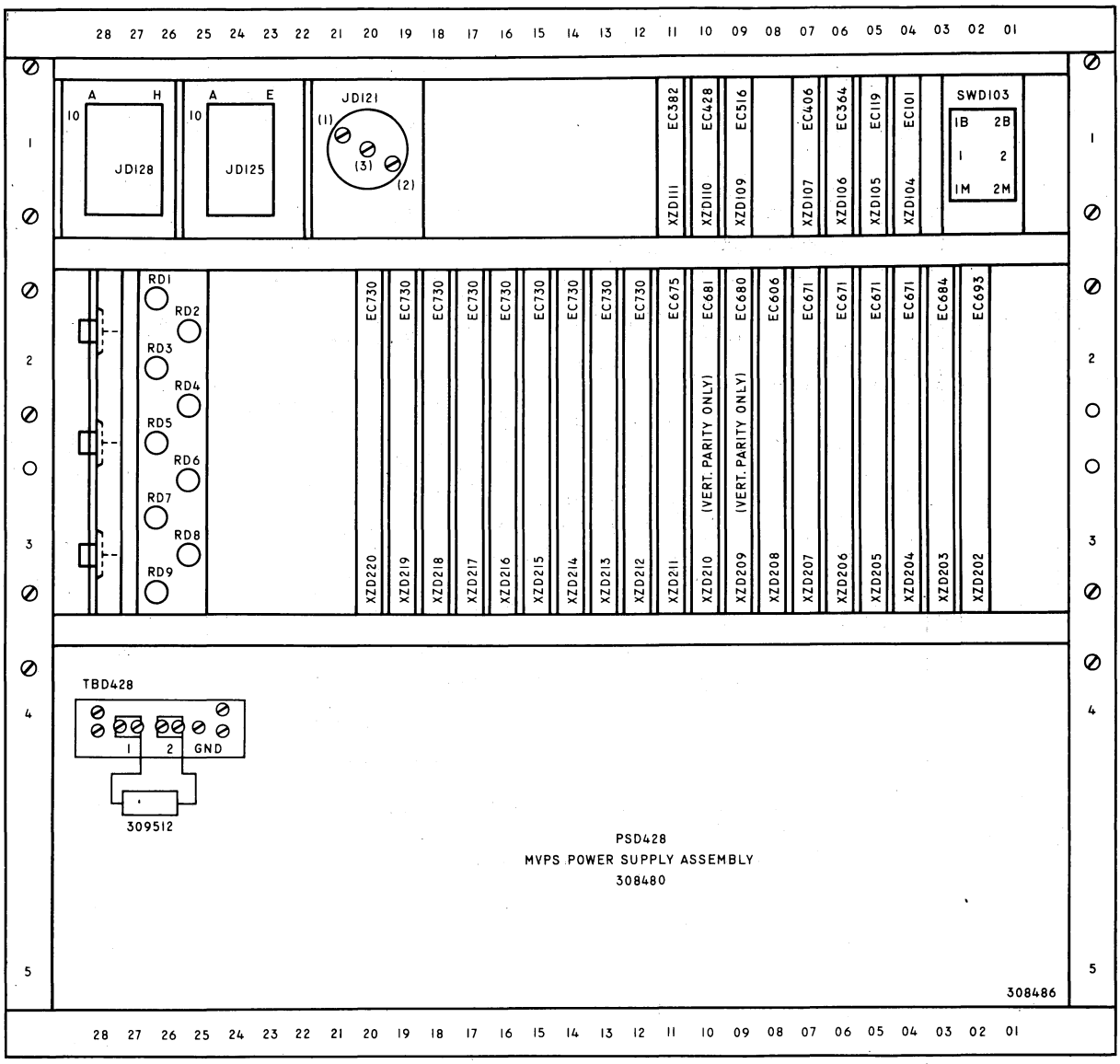


Figure 14 - High Speed Receiver Distributor and Punch Driver, Module D, Left Side View

start element and R9 is the stop element. The shift register has emitter follower outputs. See Figure 15.

6.05 Bit timing must come from an external synchronous clock when operating at speeds other than 1050 Baud. An internal start-stop oscillator is used when operating at 1050 Baud. This start stop oscillator, circuit element ZD107, operates at 2100 Hz driving a frequency divider to obtain a 1050 Hz square wave clock. The external or internal clock provides the timing for the advance pulses and the reset pulses which drive the shift register.

6.06 A character sample appears whenever a character is read into the shift register. A character in sync is defined as a space in the start element and a mark in the stop element. The character sample is inhibited when an out of sync condition exists. The EDC logic uses the RD sample, being the same as the character sample, except it is additionally blinded by the punch blinds.

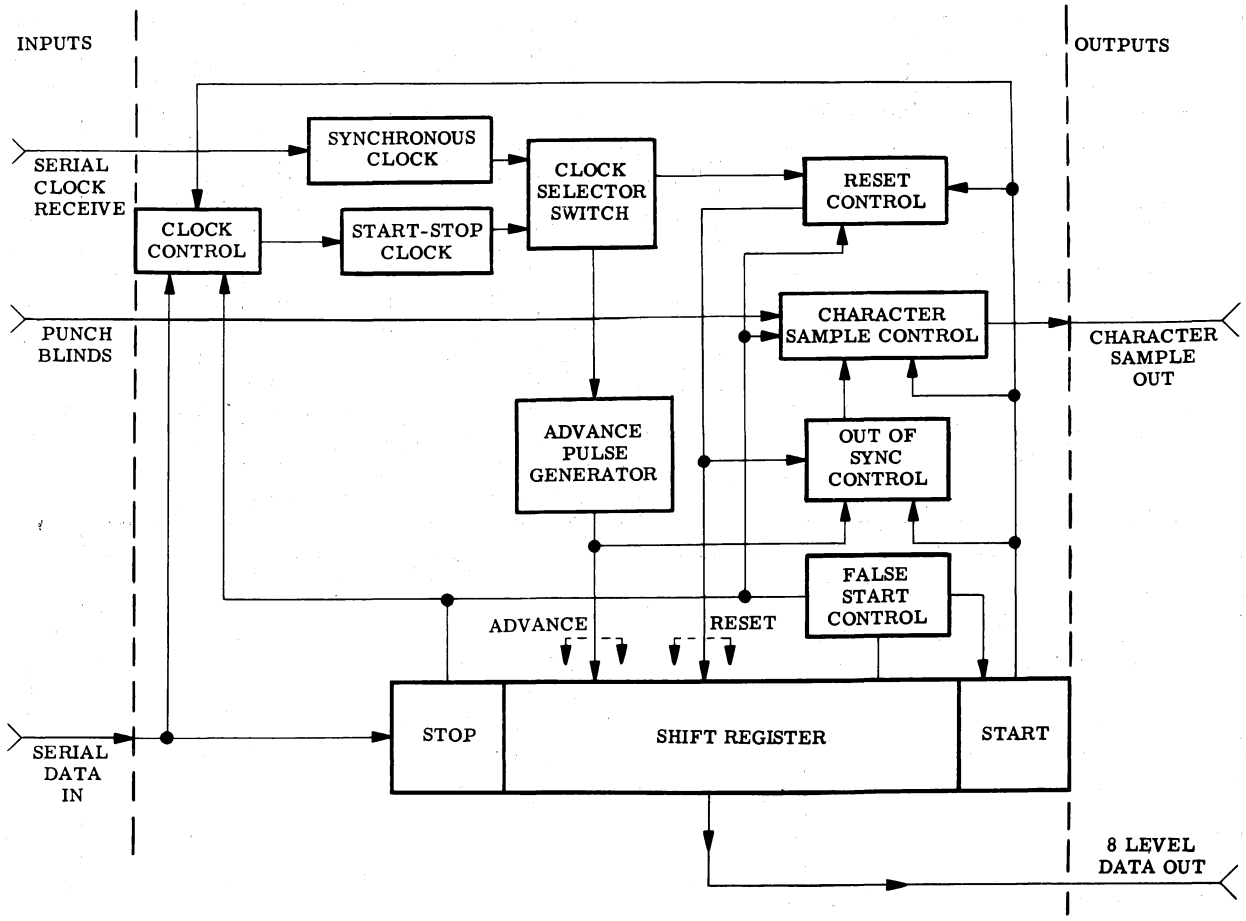


Figure 15 - Block Diagram of Receiver Distributor

6.07 The false start control is used when the distributor is used with its internal start-stop clock. It prevents the distributor from cycling if the start command is shorter than 1/2 bit.

OPERATION WITH ASYNCHRONOUS CLOCK

6.08 Refer to Figure 16 for the logic diagram and Figure 17 for the timing diagram.

6.09 Power on Reset: When power is first turned on, a mark is set into the stop element and a space is set into the start element. The out of sync detector (OSD) is set, preventing a character sample. The clock will be turned off as long as there is mark hold on the line.

6.10 Start: When the data goes spacing, this is the start command for the receiving distributor. The frequency divider (FD) is set and the local oscillator is started. One-half bit

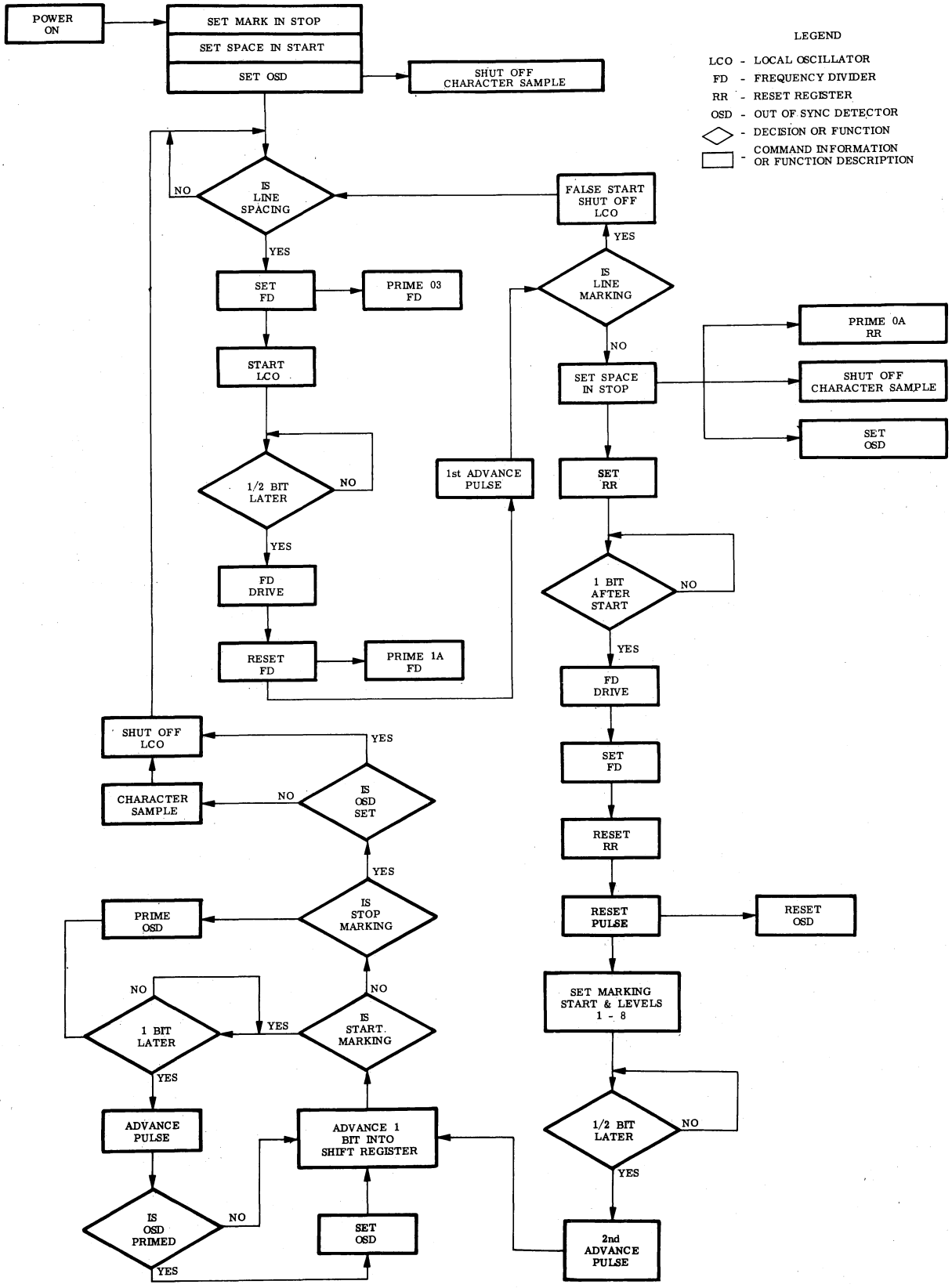


Figure 16 - Receiver Distributor Logic Diagram (Asynchronous Clock)

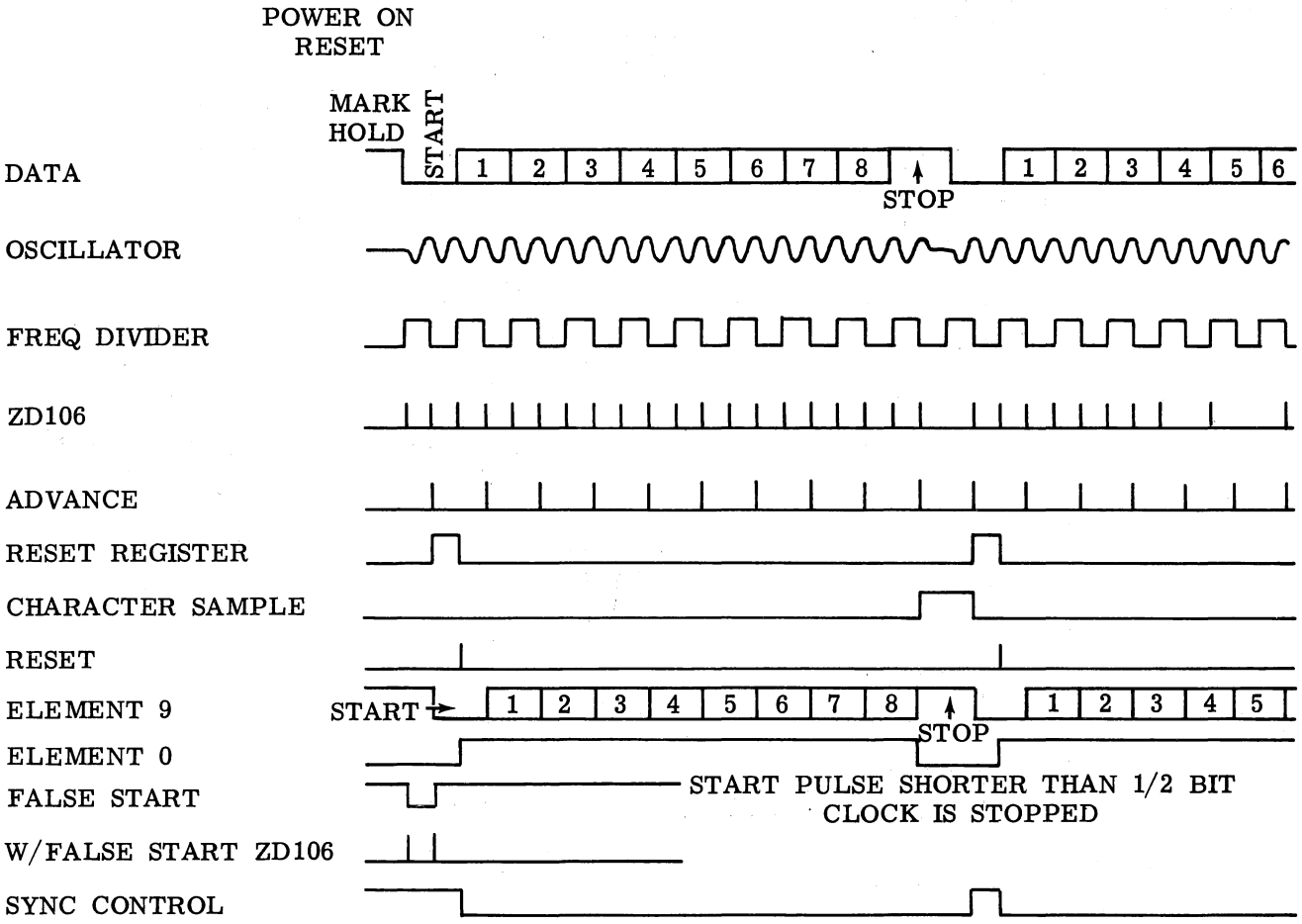


Figure 17 - Receiver Distributor Timing - Asynchronous Clock

later, the oscillator will have completed one cycle and a FD drive pulse will reset the frequency divider. Whenever the FD is reset, an advance pulse will be generated. This first advance pulse will set the space into the stop element.

6.11 Reset: When the stop element goes spacing, the reset register (RR) will be set and the next time the FD is set (1/2 bit later) the RR will be reset. Whenever the RR is reset, a reset pulse will be generated. The reset pulse sets marks into levels 1-8 and the start element. The reset pulse also resets the OSD.

6.12 Reading Character into Shift Register: The advance pulses will now continue at 1 bit intervals, occurring at the midpoint of each incoming data bit. The character will then be shifted into the shift register until there is a space in the start element and a mark in the stop element. This will ordinarily be when the start bit has been shifted all the way through the shift register and the stop bit has just reached the stop element.

6.13 Out of Sync: If the stop element is not marking when the start element goes spacing, and out of sync condition results, the shift register will continue to cycle until a space in the start element coincides with a mark in the stop element. The OSD will be set, which will inhibit the character sample.

6.14 Character Sample: With a space in the start element and a mark in the stop element, a character sample will be presented,

providing the OSD is not set. The oscillator is shut off and will wait for the next start bit. The character sample will last until the next reset pulse occurs. The character to be read out will appear on the distributor outputs for the total duration of the character sample.

6.15 RD Sample: The RD sample is used by the EDC module for its timing. After some gating and shaping, the EDC module presents it to the punch drivers as the punch sample. The RD sample is the same as the character sample except that the punch blinds will inhibit the RD sample.

OPERATION WITH SYNCHRONOUS CLOCK

6.16 Refer to Figure 18 for the logic diagram and to Figure 19 for the timing diagram.

6.17 Power on Reset: When power is first turned on, a mark is set into the stop element and a space into the start element. The out of sync detector (OSD) is set, preventing a character sample. The receive clock comes from the data set, being a square wave with a period of the data bit duration. The negative transition of the receive clock must coincide with the start of each data bit. The receive clock is then inverted for use by the receiving distributor. Now the negative transition of the clock will coincide with the center of each incoming data bit. Each negative transition of the clock produces one advance pulse so the continuous clock produces a continuous stream of advance pulses spaced at 1-bit intervals.

6.18 Start: The shift register will cycle continuously, regardless of the condition on the line. If mark hold is on the line, marks will be continuously advanced into the shift register with the start element being held spacing. The OSD will remain set. When a start bit comes in, the line will go spacing. The next advance pulse will set this space into the stop element. This will set the reset register (RR).

6.19 Reset: The next positive transition of the clock (1/2 bit after the reset register (RR) has been set) the RR will be reset. Whenever the RR is reset, a reset pulse will be generated. The reset pulse sets marks into levels 1-8 and the start element. The OSD is reset.

6.20 Reading Character into Shift Register: The advance pulses will continue at 1-bit intervals, occurring at the midpoint of each incoming data bit. The character will then be shifted into the shift register until there is a space in the start element and a mark in the stop element. This will ordinarily be when the start bit has been shifted all the way through the shift register and the stop bit has just reached the stop element.

6.21 Out of Sync: If the stop element is not marking when the start element goes spacing, an out of sync condition results and the shift register will continue to cycle until a space in the start element coincides with a mark in the stop element. The OSD will be set and will inhibit the character sample.

6.22 Character Sample: With a space in the start element and a mark in the stop element, a character sample will be presented, providing the OSD is not set. The character sample will last for one bit since the next advance pulse will set the OSD. The character to be read out will appear on the distributor output for the total duration of the character sample.

6.23 RD Sample: Refer to 6.15.

CIRCUIT DESCRIPTION

6.24 Power on Reset: When power is first turned on the power on reset (POR) element ZD202C produces a 0 volt dc output on terminals 8, 9, and 10 for a duration of about 300 milliseconds and then the outputs go to -6 volts dc. The output on terminal 8 goes to the inverted output terminal 13 of ZD207 (element RO) to set a space into the start element (0 state). The output of POR on terminal 9 goes to the normal output terminal 12 of ZD204 (element R9) to set a mark into the stop element (1 state). The output of POR on terminal 10 goes to the normal output terminal of the out of sync (OSD) flip-flop ZD204B to set the OSD to the 1 state. This will shut off the RD sample until the first reset pulse is generated.

6.25 Data: Incoming data appears on terminal D1 of connector JD128. Data must conform to system standard signals: mark, 0 volts dc; space, -6 volts dc. The data must be in 10 unit code, 1 start bit (spacing), followed by 8 data bits, and ending with 1 stop bit (marking). The stop signal is 1-bit long in continuous transmission although the stop bit can be any length when running asynchronous and any integral multiple of a bit length when operating synchronous. The incoming data is applied to the

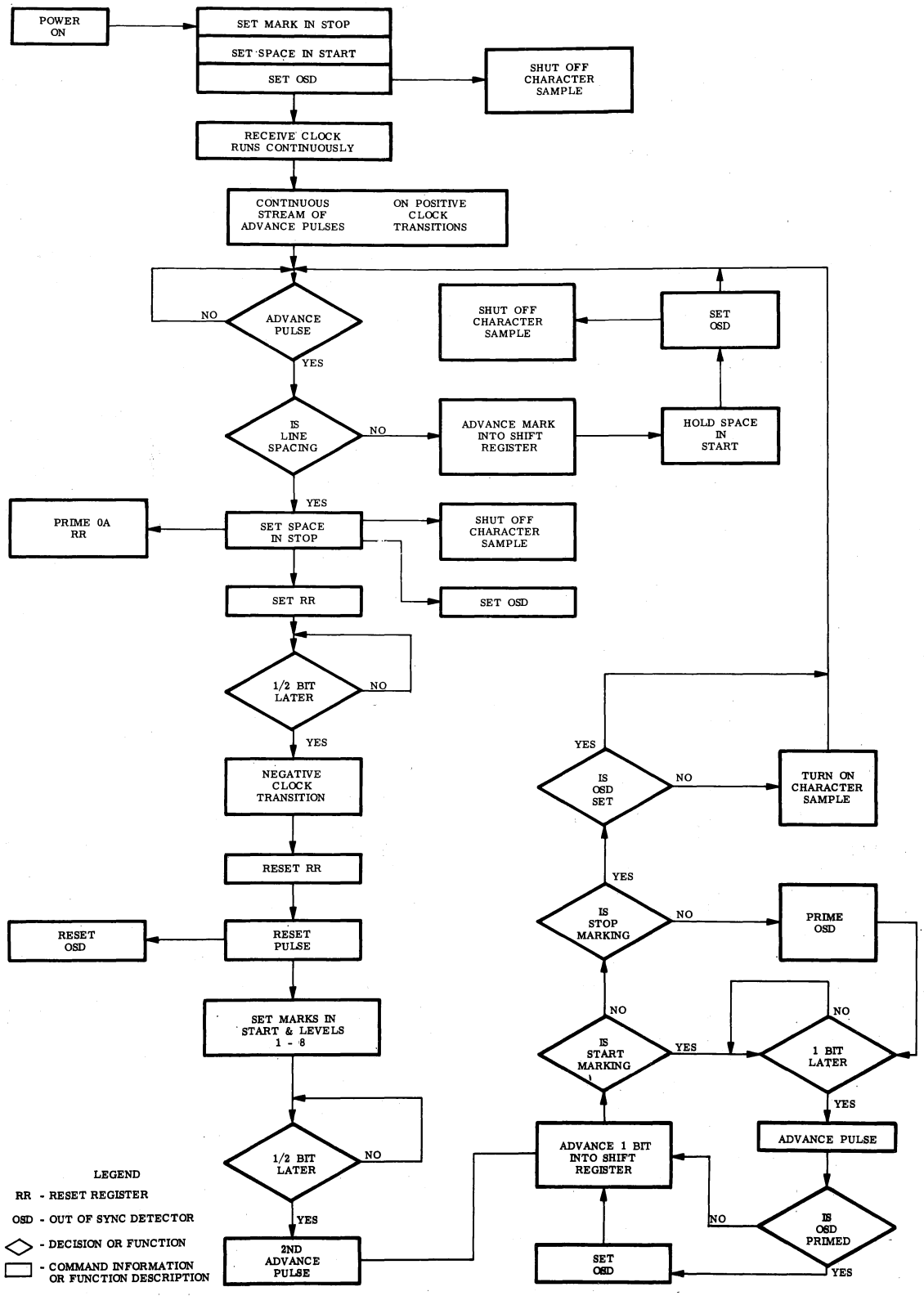


Figure 18 - Receiver Distributor Logic Diagram (Synchronous Clock)

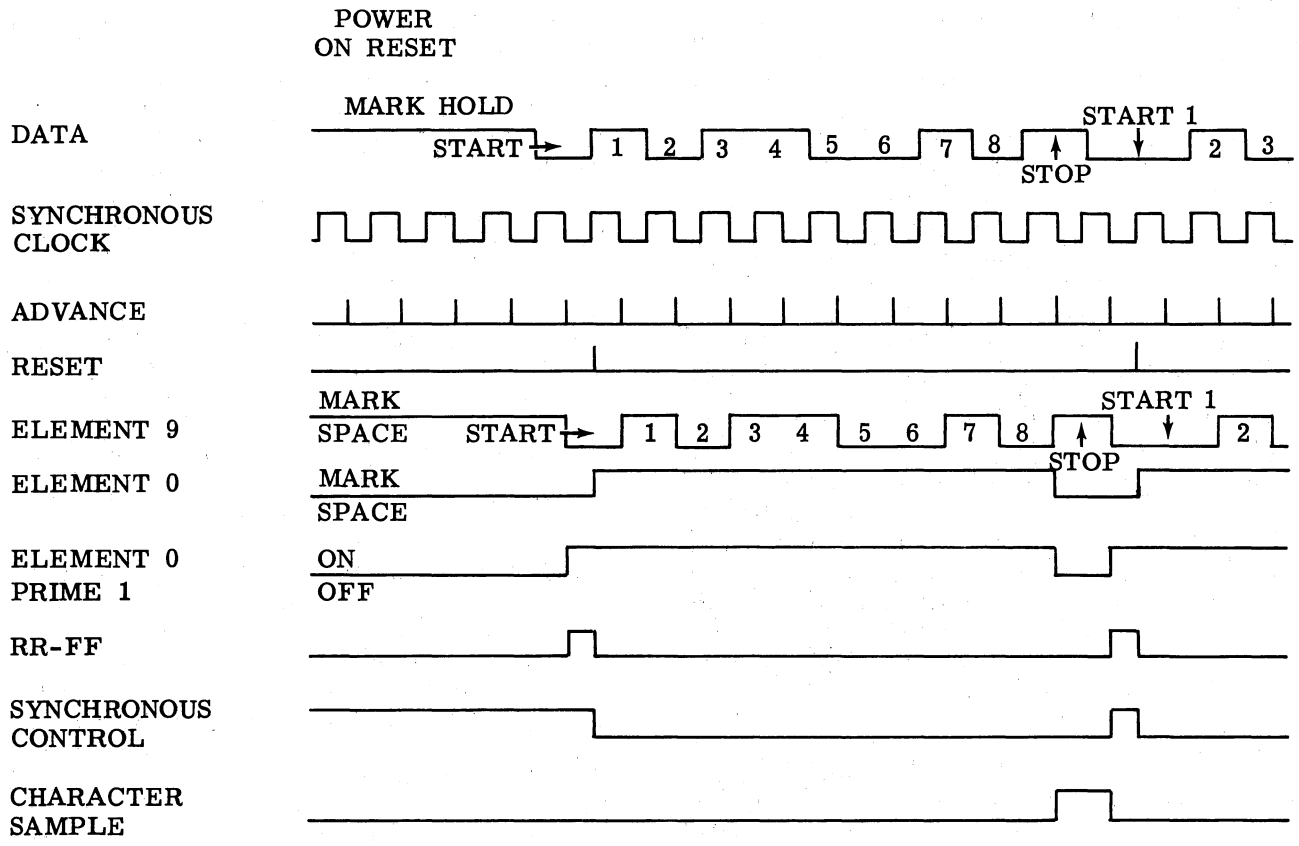


Figure 19 - Receiver Distributor Timing - Synchronous Clock

P1B terminal of flip-flop ZD204 (the stop element) on terminal 32 and is inverted by inverter ZD202D, input terminal 17, output on terminal 13. The inverted data is applied to terminal 30 of ZD204, the POB terminal of the stop element flip-flop. The inverted data is also applied to terminal 6 of OR gate ZD203B. When the data goes spacing, -6 volts dc appears on normal data and 0 volts appears on inverted data. This 0 volt signal passes through OR gate ZD203B, appears at the output terminal 2, and is applied to the local oscillator (LCO) input, terminal H of ZD107, and to the 1A input of the FD flip-flop, terminal C of ZD105.

6.26 Clocks: With 0 volts applied to the input of ZD107, this oscillator will start to operate at a frequency of 2100 Hz. The -6 volt to 0 volt transition to the 1A input of the FD flip-flop will set this flip-flop to the 1 state if it is not already in that state. Each negative transition of the oscillator, whose output is on terminal A of ZD107, will produce an FD drive

pulse on terminal A of ZD106. The FD drive pulse is a positive going pulse, -6 volts dc to 0 volts dc of 10 microsecond duration. The input of ZD106 on which the oscillator output appears is terminal A. Since the FD flip-flop is in the 1 state, 0 volt dc appears on the normal output, terminal L, of ZD105. This is applied to emitter follower ZD202L at input pin 31 and the output (pin 36) is applied to pin C of the signal delay ZD111 which delays the signal 50 microseconds. The output of ZD111, on pin L, is applied to the prime 0B input on terminal A of FD flip-flop ZD105. The next FD drive pulse will appear on terminal D of ZD105, the set OB terminal of the FD flip-flop so the FD flip-flop will be reset to the 0 state. At this point, the normal output of the FD flip-flop represents the internal clock, a square wave output with frequency 1050 Hz. When running synchronous, the serial clock receive from the data set appears on terminal D2 of connector JD128 and then on input terminal 18 of inverter ZD202E. The inverted synchronous clock appears on output terminal 14 of inverter ZD202E. Switch SWD103 is the BAUD switch. The 1050 BAUD clock (internal start-stop) appears on the normally closed side. The output of the clock appears on the common terminal of SWD103. The positive transition of the clock will coincide with the beginning of each data bit and the negative transition will coincide with the middle of each data bit.

6.27 Start Bit Action: At the middle of the first bit, (the start bit) the first negative transition of the clock generates an advance pulse. The clock appears on input terminal 31 of emitter follower ZD202L, and from its output terminal 36 on to input terminal 6 of pulse amplifier ZD202A. The negative clock transition generates a positive going pulse, 10 microseconds wide, on output terminal 1 of ZD202A, which is called the advance pulse. This advance pulse is simultaneously applied to the 0B and 1B terminals of all 10 flip-flops in the shift register; ZD204, terminals 31 and 33; ZD205, terminals 6, 20, 23, 25, 31, and 33; ZD206, terminals 6, 20, 23, 25, 31, and 33; and ZD207, terminals 6, 20, 23, 25, 31, and 33. With a spacing data bit, the first advance pulse will set the stop element ZD204 to the 0 state with inverted output terminal 13 going to 0 volts dc and normal output terminal 12 going to -6 volts dc. The positive step from the inverted output of ZD204 appears on input terminal 18 of OR gate ZD203E, being passed through to output terminal 22 and then to input terminal 25 of emitter follower ZD202K. The same positive transition appears on output terminal 28 of ZD202K, being applied to input terminal 7 of OR gate ZD203B and the 1A input, terminal 8, of reset register (RR) flip-flop ZD204A. This positive transition sets the RR flip-flop since the P1A terminal is permanently primed. The 0 volt level, after the transition holds the oscillator on through OR gate ZD203, primes P0A of RR on terminal 5 of ZD204A, and primes AND gate ZD203F on terminal 19. Since the FD is in the 0 state, 0 volts dc appears on terminal K of ZD105 and is applied to the other input of AND gate ZD203F, terminal 20. With both inputs at 0 volts dc, the output of AND gate ZD203F, terminal 23, will be at 0 volts dc, priming P1B of FD flip-flop ZD105 on terminal J. This allows the FD flip-flop to continue to change states so that the local clock can continue to generate advance pulses. The synchronous clock will continue to oscillate regardless of the condition of the shift register.

6.28 Reset Pulse: The shift register now has the start bit read into the stop element and the clock is continuing. The next positive transition of the clock is applied to the 0A input of RR flip-flop ZD204A (terminal 4) setting it back to the 0 state. The normal output of the RR flip-flop (terminal 1) will go to -6 volts dc, with this negative transition being applied to input terminal 32 of emitter follower ZD202M. This negative transition then appears on output terminal 33 of ZD202M and is applied to input terminal 3 of pulse amplifier ZD202B, where it produces a positive going pulse, 10 microseconds wide, on output terminal 2 of ZD202B. This output pulse is called the reset pulse. It is used to reset the shift register and the out of sync detector. The reset pulse is simultaneously applied to the 1A inputs of shift register elements R0 through R8 (terminals 8, 27, and 34 of ZD205, ZD206 and ZD207). The P1A terminals of all these flip-flops are grounded so they are permanently primed. The reset pulse sets elements R0 through R8 to the 1 state (ie, a mark is set in all levels except the stop element, which has the start bit read into it).

6.29 Shifting a Character into the Register: Each advance pulse will now shift the information appearing on the data lead through the shift register. The normal output of each flip-flop primes the P1B input of the next lower flip-flop (example: R9 primes R8, R8 primes R7, etc.). The inverted output of each flip-flop primes the P0B input of the next lower flip-flop. The advance pulse is applied simultaneously to the 1B and 0B inputs of all the elements.

Element	Flip-flop	Output Terminals Normal	Inverted	Input Terminals P0B	P1B	Advance 0B	1B	Primed by
Stop	ZD204	12	13	30	32	31	33	Data
R8	ZD205	1	2	7	21	6	20	Stop
R7	ZD205	14	17	22	24	23	25	R8
R6	ZD205	12	13	30	32	31	33	R7
R5	ZD206	1	2	7	21	6	20	R6
R4	ZD206	14	17	22	24	23	25	R5
R3	ZD206	12	13	30	32	31	33	R4
R2	ZD207	1	2	7	21	6	20	R3
R1	ZD207	14	17	22	24	23	25	R2
Start	ZD207	12	13	30	32	31	33	R1

6.30 Each advance pulse will cause the information in each level to be shifted to the next lower level because a mark in a level will prime a mark in the next lower level and a space in a level will prime a space in the next lower level. This process of shifting the character through the shift register will continue as long as there are advance pulses. They will always exist when operating with a synchronous clock so the shift register will continue to operate. In the case of start-stop operation, however, the advance pulses will be shut off as soon as a character sample is generated.

6.31 Character Sample and RD Sample: After resetting the shift register, a mark appears in the start element, represented by a 0 volt dc output on terminal 12 of ZD207. This 0 volt dc signal is then applied to input 17 of OR gate ZD203E, being passed through to appear on output terminal 22. Emitter follower ZD202K (input 25, output 28) passes this signal and applies it to input 15 of OR gate ZD203D and to OR gate ZD203B to keep the oscillator going. The 0 volt signal appears on output terminal 21 of ZD203D, is inverted by inverter ZD202H and amplified by emitter follower ZD202J (input 21, output 29). This inverted signal appears on terminal D3 of connector JD128 and is called the character sample.

6.32 In a similar manner the RD sample is generated. The 0 volt signal representing a mark in the start element is applied to input 9 of OR gate ZD203C, appearing on output terminal 3. At this point the signal can be used by the vertical parity accessory, being called the vertical parity sample. The signal is then inverted and amplified in inverter ZD202F and emitter follower ZD202G (input 20, output 26). The signal then appears on terminal D4 of connector JD128. This is called the RD sample and is used by the EDC circuitry for the timing of the entire receiver.

6.33 With a mark in the start element, the RD sample will stay at -6 volts dc. Since the shift register was reset to all marks, the start element will hold a mark for 9 advance pulses. After 9 advance pulses, the start bit will arrive at the start element, setting a space into it. This will allow the RD sample to go to 0 volts dc, provided a mark simultaneously appears in the stop element. If the stop element is spacing, 0 volts dc will appear on input terminal 18 of OR gate ZD203E, which will keep the RD sample at -6 volts dc. Assuming a valid character has been read into the shift register (a space appears in the start element and a mark appears in the stop element) the RD sample will go to 0 volts dc, indicating that a character is ready to be read-out.

6.34 Character Read-Out: The outputs of elements R1 through R8 will now represent the 8 levels of the character to be read-out. The outputs are put through 8 emitter followers before being presented to terminals A1 through A8 of connector JD128, the distributor outputs.

Level	Flip-flop	Emitter Follower ZD208 Output	Input	Output	JD128 Connector
R1	ZD207	14	29, 9	19, 17	A1
R2	ZD207	1	30, 10	33, 13	A2
R3	ZD206	12	31, 11	34, 14	A3
R4	ZD206	14	32, 12	35, 15	A4
R5	ZD206	1	21, 1	20, 18	A5
R6	ZD205	12	22, 2	25, 5	A6
R7	ZD205	14	23, 3	26, 6	A7
R8	ZD205	1	24, 4	27, 7	A8

6.35 0 volts dc represents a mark and -6 volts dc represents a space. The character can be read-out as long as the RD sample is at 0 volts dc. When operating start-stop, the RD sample will last until the next start bit is received. When operating synchronous, the RD sample will last for one bit, and is then turned off by the out of sync detector (OSD).

6.36 Out of Sync: When it takes more than 9 advance pulses to shift a valid character into the shift register, the out of sync detector (OSD) will be set. This will shut off the character sample and the RD sample. With the 9th advance pulse after the reset pulse, the start bit is set into the start element so inverted output terminal 13 of start element ZD207 will go to 0 volts dc. This will be applied to the P1B prime of the OSD flip-flop ZD204B on terminal 24. The next advance pulse will appear on the 1B input of ZD204B (terminal 25) setting the OSD flip-flop to the 1 state, representing an out-of-sync condition. The normal output of OSD, ZD204B, terminal 14, will go to 0 volts dc, being applied to input terminal 16 of OR gate ZD203D and input terminal 10 of OR gate ZD203C. This will keep the character sample and the RD sample at -6 volts dc (off). The out of sync detector will be reset by the next reset pulse, being applied to the 0B input (terminal 23) of the OSD flip-flop. Since the P0B input (terminal 22) is grounded, the reset pulse will reset the OSD back to the 0 state.

6.37 False Start: When the start bit is less than a half-bit long, a false start condition results and the receiving distributor will not operate.

6.38 When operating synchronous, the shift register continues to cycle but a space is held in the start element (P1B is not primed), preventing the distributor from completing its shift. When a valid start bit is received, it will be set into the stop element and the reset pulse will be generated. This sets marks into element R0 through R8 and produces a 0 volt input on terminal 14 of AND gate ZD203A. This will enable this AND gate so that the marks in element 1 (input terminal 12) will appear on output terminal 1 of ZD203A and can be applied to the P1B input, terminal 32, of RO flip-flop ZD207. Now the advance pulses can shift marks into the start element.

6.39 The false start feature is most important when operating with a start-stop clock. It presents the distributor from being started by a start bit that is less than 1/2 bit long. With mark hold on the line and with a space held in the start element all the inputs of OR gate ZD203B will be at -6 volts dc. If a short start bit (less than 1/2-bit long) is received, the local oscillator will start up. Since there is a short start bit, it will not be set into the stop element and the output of OR gate ZD203E will stay at -6 volts dc. This keeps AND gate ZD203A inhibited so that a mark cannot be set into the start element and the oscillator will be shut off. If a mark were set into the start element, the output of OR gate ZD203E would go to 0 volts dc, the clock would be held on and the distributor would operate. With the false start feature, however, the distributor will respond only to start bits longer than 1/2 bit.

6.40 Punch Blinds: The punch blinds are provided for inhibiting RD sample pulses when various accessories are being used. The distributor is allowed to respond to incoming data and to operate, but the RD sample is inhibited. With 0 volts dc on input terminals D6, D7, D8, or D9 of JD128, the corresponding inputs to OR gate ZD203G (terminals 31, 32, 33, or 34) will be held at 0 volts dc. The output of OR gate ZD203G will be 0 volts dc (terminal 36) when any one input is at 0 volts dc. The output of ZD203G is applied to input terminal E of integrated pulse shaper (IPS) ZD104. This will reject 0 volt signals of less than 500 microseconds so that noise will not pass through. The output of IPS (ZD104) on terminal K is then applied to input terminal 11 of OR gate ZD203C which will prevent the RD sample whenever a punch blind is at 0 volts dc. The punch blind will not inhibit the character sample.

6.41 When the punch blind signal is removed, the out of sync detector will be set to the 1 state. When all punch blinds are removed a negative going transition will appear on input terminals A of ZD104, will be inverted, and will appear as a positive transition on output terminal H. This positive transition will appear on the 1A input (terminal 27) of OSD flip-flop ZD204B setting it to the 1 state (since the P1A terminal is permanently primed). Both character sample and RD sample will be turned off and control of them is returned to the distributor.

6.42 Punch Drivers: The punch drivers and punch driver control consists of circuit cards ZD211 through ZD220 and ZD109. Circuit cards ZD212 through ZD220 are EC672 (or EC730) punch driver cards, one for each punch level and one for the feed level. Circuit card

ZD211 is an EC675 punch driver control card. Circuit card ZD109 is an EC516 power pulser, providing letters feedout drive.

6.43 Information to be punched is presented to prime terminal 15 of the respective punch driver card EC672. A 0 volt dc signal primes the driver to punch a hole, and -6 volts dc prevents the punch from producing a hole. The feed level is permanently primed by having terminal 15 grounded. The punch sample from the HSEDC receiver control module passes through IPS card ZD211 to remove noise from the signal and is simultaneously applied to pin 22 of all the driver cards. This sets a flip-flop in each driver to punch the information that has been primed. The OSC in card ZD211 times out 1.9 milliseconds and then resets all the driver cards on pin 30. When punching 5, 6, or 7 level tape, the appropriate levels can be disabled by grounding pin 24 of the level to be disabled. This is accomplished through switch SWD1, the LEVEL SELECTOR switch. To feed out blank tape, pin 30 of ZD211 is grounded which starts the feedout generator. This is applied to pin 3 of the feed level punch driver and the punch will produce feed holes. If an all-marks feedout is desired, a letters drive signal is produced in the HSEDC receiver control module and is applied to pin E3 of connector JD128 and pin E of power pulser ZD109 whose output (pin H) is applied to pin 3 of all 8 punch drivers. A -55 volt dc supply is applied to pins 7 and 36 of each punch driver. A -5 volt dc supply is applied through a diode to pin 28 of each punch driver. The punch coils are driven from terminals 9 and 28 of each punch driver.

6.44 Blank Feed: The BLANK FEED switch (on the horizontal panel of the cabinet) is connected to input terminal E1 of connector JD128, and is functional only when the motor start relay is energized. Pressing the BLANK FEED pushbutton grounds terminal 30 of feedout generator ZD211 and starts the feedout generator. A series of positive going pulses, 35 microseconds wide at a frequency of about 50 Hz. appears on output terminal 28 of ZD211. This is applied to terminal 3 of ZD220 and each pulse will cause the punch to punch a feed hole and step.

6.45 All Feed: When an all-marks character is desired, as when initially testing the punch to see if all levels are punching, the ALL FEED pushbutton must be pressed. This applies to ground terminal E1 of connector JD128, which is applied to terminal 30 of ZD211 to start the feedout generator. The output of the feedout generator goes to pin 3 of ZD220 to cause the feed level to start punching. The output pulses also appear on terminal E2 of connector JD128, called feed drive. The feed drive pulses are gated in the EDC module and reappear on terminal E3 of JD128 as the letters drive when the ALL FEED button is pressed. The letters drive pulses are applied to input terminal E of power pulser ZD109. The power pulser will now produce output pulses, positive going, 25 microseconds wide, to the input terminal 3 of all the 8 level punch driver cards to produce the all-marks character.

6.46 5, 6, or 7 Level Punching: When 5, 6, or 7 level data is being received, the unused punch levels can be disabled by putting the LEVEL SELECTOR switch (SWD1) in the proper position. When in the 7 level position, punch level 8 is disabled. In the 6 level position, levels 7 and 8 are disabled. In the 5 level position, levels 1, 7 and 8 are disabled. When a level is to be disabled, a ground is applied through SWD1 to pin 24 of the appropriate punch driver card (level 1 = ZD212, level 7 = ZD218, level 8 = ZD219) and this holds the flip-flop on that punch driver card in the spacing condition.

6.47 Multivoltage Power Supply: The power supply for the receiving distributor and the punch drivers provides a separate fused -55 volts dc and a common fused -5 volts dc to each punch driver. Fused voltages of +6 vdc, -6 vdc, -12 vdc, and -55 vdc is supplied to the circuit cards.

6.48 The receiver station control obtains its power from this power supply:

Voltage	PD128	Voltage	PD128
+6 volts dc	H4	-55 volts dc	H7
-6 volts dc	H5	signal ground	H2
-12 volts dc	H6	circuit ground	H3

6.49 Ac power is applied to the power supply through connector JD121 as follows:

Terminal	Volts AC
1	115
2	ac common
3	frame ground

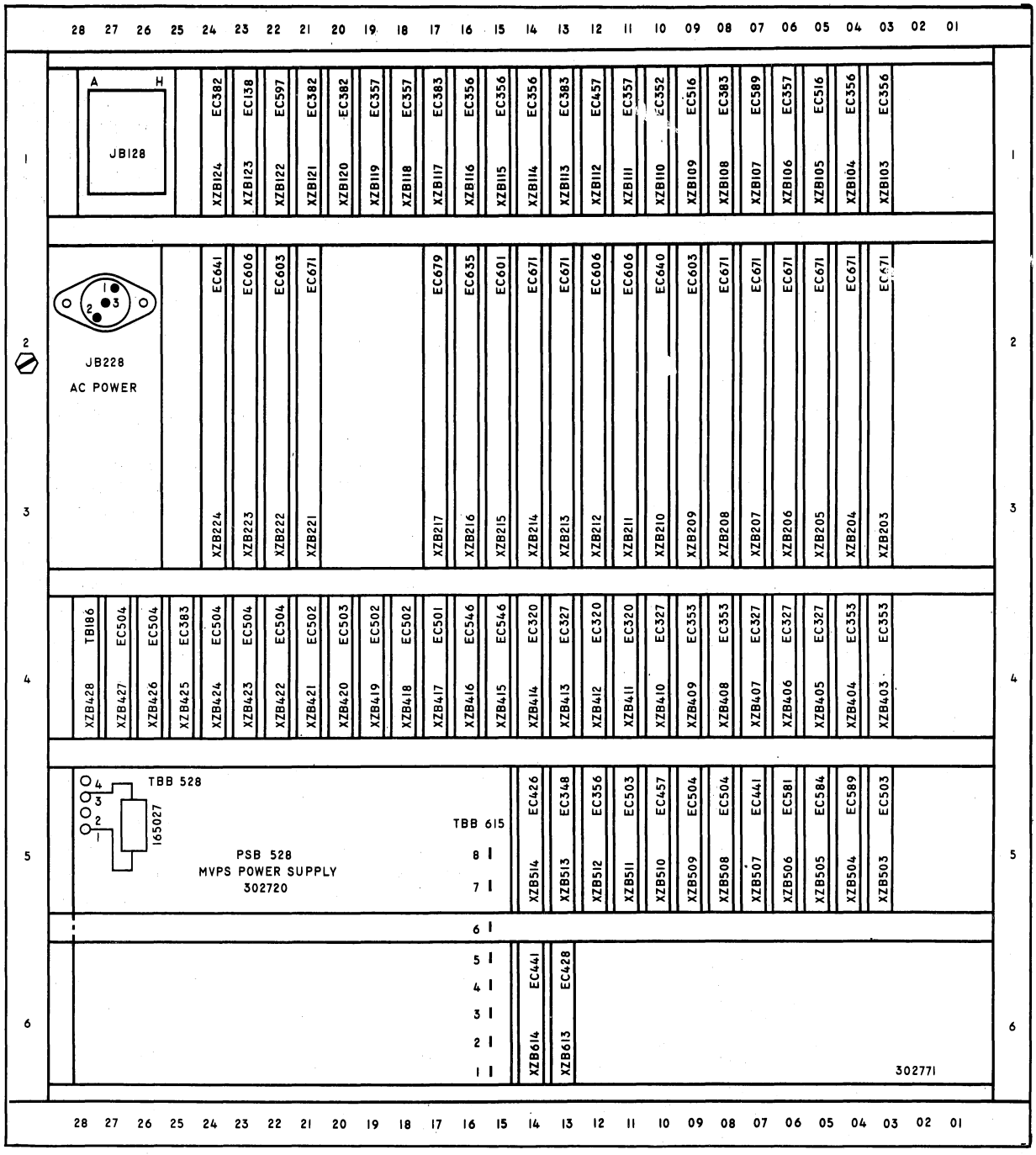


Figure 20 - HSEDC Receiver Control Module B, Left Side View

7. HSEDC RECEIVER CONTROL MODULE

GENERAL

7.01 The HSEDC receiver control module is located in the lower left-hand section of the receiver cabinet. It may be pulled forward for servicing. An interior view of the module is shown in Figure 20.

7.02 The schematic diagrams, contained in another section, are:

7063WD - HSEDC receiver control module
7058WD - Multivoltage power supply (TP302720)

POWER SUPPLY (7058WD)

7.03 The power supply used (TP302720) receives 115 v ac from terminals 1 and 2 of JD228, with terminal 3 being ground. The ac supply is applied to terminals 1 and 3 of terminal board TBB528; terminal 2 is ground. The outputs of the power supply appear at terminal board TBB615. Terminals 1 and 2 supply 1 volt ac for the indicating light filaments. Terminal 3 supplies -12 volts dc. This -12 volts is then put through a four ampere fuse (FB603) from where it is distributed to the module, and returned to terminal 4 of the power supply. The power supply then uses the -12 volts dc to produce -6 volts dc on terminal 5. -6 volts dc is not fused again before being sent to the module. +6 volts dc appears at terminal 6 and is fused with a one ampere fuse (FB602) before being distributed to the module. Terminal 8 supplies +50 volts dc. This then goes through a 1/2 ampere fuse (FB601) and is supplied to the plates of the indicating lamp assemblies. Terminal 7 of the power supply is a common ground for all of the power supply voltages. All of the power supply voltages are wired to connector JB128; some are used externally and some are there only for references: 1 volt ac appears on terminals A8 and B8 of JB128; -12 volts dc appears on terminal B7; -6 volts dc appears on terminal A4; +6 volts dc appears on terminal B3; +50 volts dc appears on terminal A3. Filter card ZB613 is used to filter noise from +6 volts dc (pin R), -6 volts dc (pin P), and -12 volts dc (pin M).

7.04 Circuit ground appears on terminal B6. In addition, frame ground appears on terminal B5 of JB128. Circuit ground and frame ground are tied together externally in the receiver wire field.

RECEIVER PROGRAMMER

7.05 The receiver programmer is the heart of the HSEDC receiver control module. It performs the basic function of selecting and directing the actions of the module and consists of several ring elements connected together. Each ring element is assigned a name. The ring elements used in the receiver programmer are: sender ready, abbreviated SR, location ZB405A; block number, abbreviated BN, location ZB406A; block, abbreviated BK, location ZB405D; the next ring element is end of block, abbreviated EOB, location ZB405B. Following EOB comes check character 1, CK1, location ZB406C and check character 2, CK2, location ZB406D. After CK2, comes back up, abbreviated BU, location ZB406B. The final element is delete, abbreviated DEL, location ZB406C.

7.06 When the terminal is first turned on, the programmer will reset itself to the SR mode. The programmer is then advanced by programmer advance pulses which come into terminal F of ZB403B, a ring drive element, with the output on N. This will simultaneously be applied to all of the advance elements of the programmer ring. The output of each programmer element is put through a symmetrical emitter follower, element ZB212, before being sent to the rest of the EDC logic. With the programmer in the SR mode, there will be a 0 volt output at terminal H of ZB405A. The output of all the other ring elements will be at -6 volts dc. This output of the SR element is applied to a ring reset element ZB403A on terminal R. It passes through to terminal P, ZB403A and is applied to terminal F of ZB406A. This will prime the next ring element, BN, so that when the next programmer advance pulse comes from the ring drive element ZB403B, the programmer will be advanced from the SR mode into BN mode. In the BN mode the output of terminal H of ZB406A will now go to 0 volts dc, and the output on terminal H of ZB405A will go to -6 volts dc. The output from terminal H of ZB406A is then applied to terminal A of ZB405D priming the BK element so that the next programmer advance pulse will advance the programmer to the block mode. In the block mode, the output of terminal D of ZB405D will go to 0 volts which will prime the EOB element, terminal J of ZB405B. The next programmer advance pulse will advance the programmer to the end of block mode.

7.07 In the EOB mode, the output K of ZB405B will go to 0 volts dc which will prime the next element CK1 on terminal L of ZB405C.

The next programmer advance pulse will advance the programmer to the CK1 mode. This will produce an output of 0 volts dc on terminal M of ZB405C, which will then prime the CK2 element, ZB406D terminal A. With the next programmer advance pulse, the programmer will be advanced to the CK2 mode. The output of CK2 element on terminal D will then go to 0 volts and will prime the back-up element, ZB406B on terminal J. The next programmer advance pulse will advance the programmer into the BU mode. In the BU mode, the output on K of ZB406B goes to 0 volts priming the delete element, ZB406C on terminal L. The next programmer advance pulse advances the programmer into the delete mode. In the delete mode, the output on, terminal M of ZB406C goes to 0 volts dc which is then applied to terminal H of ring reset element, ZB404A. This will produce a 10 microsecond positive pulse on output terminal M of ZB404A which will set the programmer back in the SR mode.

7.08 The above sequence of the programmer is the sequence followed when an error has been detected and must be corrected by going through the back-up and delete cycle and returning to the SR mode. In normal operation when no errors have been detected, the programmer will go directly from the CK2 mode back to the BN mode. This is accomplished by the output of terminal D of ZB406D being applied to terminals 2 and 22 of emitter follower ZB212 with outputs at 5 and 25. Thus, in the CK2 mode an output is applied to terminal H of ring reset element, ZB403A. If no error has occurred, terminal K of ring reset element, ZB403A will be at 0 volts dc. This will produce a 10 microsecond negative pulse on terminal P of ZB403A which is applied to terminal F of ZB406A. This output applied to the BN mode is longer in duration than the output applied to the BU mode element. As a result, the programmer will be set into the BN mode.

CODE LEVEL DISTRIBUTION

7.09 The eight code levels from the receiving distributor appear on terminals D1 through D8 of connector JB128. These eight code levels are then applied to the character recognition matrix and the character distribution gates. The character distribution gates perform the function of properly priming the punch driver primes. The received data is passed through unchanged in the block mode. In the delete mode, all levels are primed so that the delete character will be punched. When the FIGS detect circuit requires a figures character, this character is produced by the gates. The incoming data is applied to the character recognition matrix which is a circuit designed to recognize the 5 fixed control characters (SR, BN1, BN2, BN3, and EOB). The code levels are inverted and applied to the character recognition matrix. The normal data levels 1 through 8 are applied to terminals 26, 25, 24, 23, 20, 19, 18, and 17 respectively of ZB224. These normal data leads are inverted in ZB222 being applied to terminals 2, 5, 11, 14, 22, 25, 15, 20 respectively. The outputs of the inverted signal appear on terminals 4, 7, 9, 12, 24, 27, 16, and 18 respectively of ZB222. These are applied to emitter follower ZB223 on terminals 9, 10, 11, 12, 1, 2, 3, 4 respectively. The outputs of these emitter followers are the inverted data signals which then appear on terminals 17, 13, 14, 15, 18, 5, 6, and 7 respectively of ZB223.

7.10 These inverted signals are then applied to terminals 13, 12, 11, 10, 6, 5, 4, and 3 respectively of ZB224. The normal and inverted signals are then used by the character recognition matrix to determine the validity of the control characters. The 8 data levels are also applied to 8 OR gates; these OR gates are used to prime the punch for punching a delete character or a figs character. The levels 1 through 8 are applied to terminals P, M, H, and D of ZB426 and terminals H, M, D, and P of ZB427 respectively. Terminals N, K, E, and C of ZB426 and terminals E, K, C, and N of ZB427 are the other inputs of the OR gates and are supplied with 0 volts when a delete character is desired. The outputs of these OR gates, levels 1 through 8, appear on terminals S, R, B, and A of ZB426, and terminals B, R, A, and S of ZB427 respectively. The output on A of ZB426, the fourth level, is applied to inhibit gate ZB512A on terminal D. The base input of ZB512A, terminal N, is supplied with 0 volts dc when the fourth level is to be inhibited as in the figs character. The output of ZB512A on terminal K will be always -6 volts dc if there is a FIGS prime condition. The outputs of the OR gates ZB426 and ZB427 and the inhibit gate ZB512A are then applied to connector JB128. These are then the punch driver prime signals from which the punch derives its punching information. Level 1 appears on terminal G1 of JB128, level 2 appears on terminal G2 and so on up to level 8 appearing on terminal G8 of JB128. On all the code levels, a 0 volts potential represents a marking condition and will result in a hole in the paper tape. A -6 volts dc potential represents a space and will result in a no hole condition in the tape. In normal operation, when a block is

being punched, the code levels will go through OR gates ZB426 and ZB427 and inhibit gate ZB512A without being changed and will appear on the punch driver prime levels 1 through 8 of JB128.

7.11 When a delete is desired, the delete mode condition will appear on terminal C of ZB424 represented by a 0 volt potential. This will appear on the output of ZB424C and at the inputs of all the OR gates ZB426 and ZB427. Thus the outputs of these gates will all be 0 volts and an all-mark character will be obtained. When a FIGS character is desired, the FIGS prime lead will go to 0 volts dc. This 0 volts is applied to terminal 29 of emitter follower ZB223A, whose output, terminal 19, is applied to terminal D of ZB424C and again all the levels will be primed for marks. However, as previously described, inhibit gate ZB512A will now be inhibited because base input terminal N will have 0 volts dc on it and level 4 will be prevented from punching.

CHARACTER RECOGNITION MATRIX

7.12 The character recognition matrix ZB224, EC641, is a special recognition diode matrix which contains five AND gates arranged to detect 5 of the 256 possible characters in an 8 level code. These are the 5 control characters that are used in the system (sender to receiver). The first character is the SR character with levels 1, 5, 6, and 7 marking. The EOB character is levels 2, 3, 4, 5, 6, 7, and 8 marking. Block number 1 (BN1) has levels 1, 3, 6, and 8 markings. Block number 2 (BN2) has levels 2, 4, 5, and 7 marking. Block number 3 (BN3) has levels 1, 2, 7, and 8 marking. When one of these characters appears at the input terminals of the character recognition matrix, a 0 volt potential will appear at the corresponding output terminal of the character recognition matrix. If the SR character is detected, 0 volts dc will appear at terminal 7 at ZB224, and the other outputs will stay at -6 volts dc. If the EOB character is detected, a 0 volt output will appear on terminal 35 of ZB224. If the block no. 1 character is recognized, terminal 15 of ZB224 will go to 0 volts. If the block number 2 is detected, terminal 21 of ZB224 will be at 0 volts dc. If block number 3 is detected, terminal 28 of ZB224 will be at 0 volts dc.

7.13 Element ZB428 contains three diodes which allow the block numbers to be detected only when the programmer is in the BN mode. When the programmer is in the BN mode, 0 volts dc will appear on terminal K of ZB428 and the corresponding 0 volts output of terminal 15, 21, or 28 of ZB224 will be allowed to pass. If the programmer is not in the BN mode, terminal K of ZB428 at -6 volts dc and any 0 volts potential on terminal P, R, and S of ZB428 will be clamped to -6 volts dc and no output of BN detected will appear.

RD SAMPLE PULSE

7.14 The RD sample pulse appears at terminal B2 of JB128. It is positive-going (-6 volts dc to 0 volts dc) and is one-bit wide. It is at 0 volts for the total duration of the bit. It appears on the input terminal of the EDC module when a character is available in the receiving distributor. The RD sample pulse provides the timing for the EDC circuitry. The punch sample which drives the punch is derived from the RD sample. The RD sample pulse is applied to terminal C of ZB120 and appears on terminal L of ZB120, delayed 50 microseconds. This delayed RD sample is then applied to inverter ZB106C on terminal C, the output of ZB106C appears on terminal A. The inverted sample pulse is then applied to terminal F of pulse amplifier ZB113A. The output of this pulse amplifier is a positive-going pulse, 10 microseconds wide, and will appear 50 microseconds after the lead edge of the RD sample pulse. This 50 micro-second-delayed sample is then applied to terminal D of inhibit gate ZB114A. This gate will be inhibited only during the delete cycle and in the case of an incomplete block so the delayed sample pulse will ordinarily appear on terminal K of ZB114A. It is then applied to terminal E of OR gate ZB422A and passes on through, appearing on terminal B of ZB422A. It is then inverted in ZB111B (input terminal E and output terminal D), and again inverted in ZB111C, (input terminal C and output terminal A). Inverters ZB111B and ZB111C serve to regenerate and shape the pulse. At this point the pulse is a positive-going pulse, 10 microseconds wide, delayed 50 microseconds from the beginning of the RD sample pulse and is called the programmer advance pulse.

7.15 There are two modes when the punch must be enabled: the block mode, and the delete mode. In these two modes, 0 volts dc appears on terminal A of AND gate ZB420C, enabling the delayed sample pulse to be passed to emitter follower ZB211F input terminal 22. The output of ZB211F on terminal 25 is called the gated clock. A gated clock is applied to terminal C of inhibit gate ZB115D, which is

only inhibited when the BN is low; so ordinarily the gated clock will appear on output terminal J of ZB115D and applied to terminal L of one shot ZB112. The output of this one shot on terminal J is called the punch sample and appears on terminal C4 of connector JB128. The punch sample is a positive-going pulse, from -6 volts to 0 volts dc, two milliseconds wide, occurring 50 microseconds after the leading edge of the RD sample pulse. The punch sample is the command to punch the character that is on the punch driver primes of the EDC module.

7.16 The second delayed clock is also derived from the RD sample pulse and is used to sample for check character errors, by the FIGS detect circuit, and to shut off reverse channel when the block high condition exists. The output of the ZB106C is an inverted RD sample pulse, delayed 50 microseconds. This appears on terminal C of signal delay ZB121 where the signal is delayed an additional 50 microseconds and appears on terminal L of ZB121. The output is then applied to terminal H of pulse amplifier ZB113B. The output of ZB113B on terminal D will be a positive-going transition -6 volts dc to 0 volts dc, 10 microseconds wide occurring 100 microseconds after the start of the RD sample pulse and is called the second delayed clock.

PHOTO READER FEED PULSE

7.17 The photo reader feed pulse is used to drive the character counter to maintain proper block lengths and is used by the feed alarm circuit to verify that tape is feeding properly. The photo reader feed pulse is derived from the photo verifier on the feed level. The photo verifier obtains -6 volts dc and +6 volts dc from the EDC module. When the photo verifier has light falling on it, its output will be -6 volts dc. If the photo reader does not have light falling on it, its output will be +6 volts dc. This output will appear on terminal C2 of JB128, it is then applied to terminal 15 of pad circuit ZB217J.

7.18 The purpose of the pad circuit is to decrease the sensitivity of an individual photo cell, so that it may be matched to the electronics. The output of pad circuit ZB217J is on terminal 16 and is applied to terminal 26 of ZB216I. This is an emitter follower whose output is applied to an inhibit gate, also on ZB216I. This inhibit gate is permanently primed, having terminal 27 grounded so the inhibit gate will act as an inverter with the output on terminal 18 of ZB216I being inverted from the input appearing on the terminal C2 of JB218. When a feed hole has been punched and the tape feeds to the next position, a short web of tape will be sensed because there will be a short time when no light will fall on the feed hole detector. This will result in a positive-going pulse from -6 volts dc to +6 volts dc for the duration of the feed time. This positive-going pulse appears on the output terminal 18 of ZB216I as a negative-going pulse. This pulse is then applied to input terminal C of signal delay ZB124 where it is delayed 50 microseconds and appears on terminal L of ZB124. From there it is applied to inverter ZB106D on input terminal P. The output of inverter ZB106D appears on terminal D. This output will be a positive-going pulse of 10 microseconds duration with the 0 volts potential corresponding to the web on the tape. This is called the inverted photo reader feed pulse. One inverted photo reader feed pulse will accompany each successfully punched character. The inverted photo reader feed pulse will occur approximately 3.5 milliseconds after the start of the RD sample pulse (see 7.14).

7.19 One shot ZB122 is driven by the trailing edge of the photo reader feed pulse, a positive-going transition applied to the S1 input, terminal L. The output of ZB122, on terminal J, will be a positive-going pulse, 1 millisecond wide, occurring at the trailing edge of the photo reader feed pulse. The trailing edge of this 1 millisecond pulse will produce a 10 microsecond positive pulse out of pulse amplifier ZB117A on terminal N. This 10 microsecond pulse is called the set A pulse. It occurs approximately 1 millisecond after the photo reader feed pulse. It is used in the spiral check character circuit and in the punch test mode, both of which are described in subsequent paragraphs.

SR TO BN MODE ADVANCE

7.20 The programmer advance pulse is applied to terminal F of ZB420A, an AND gate which will not allow the programmer advance pulse to go through unless the other two inputs are at 0 volts dc. The input E of AND gate ZB420 comes from the SR mode. When in the SR mode, a 0 volts potential will appear at terminal P of inhibit gate ZB512B and if the SR inhibit appearing on terminal M of ZB512B is at -6 volts dc (receiver not alarmed), then a 0 volts potential will appear on output terminal L of ZB512B and on input terminal E of ZB420A. The other input, terminal H of ZB420A, comes from emitter follower ZB211P output terminal 5.

7.21 When an SR character is detected, SR detected will go to 0 volts dc, being applied to input terminal 2 of ZB211P, and being passed on to terminal H of ZB420A. Thus, when the programmer is in the SR mode, and the SR character has been detected, AND gate ZB420A will be enabled and the programmer advance pulse will appear on terminal B of ZB420A. This advance pulse then goes to emitter follower ZB211D, input terminal 32, output terminal 35, and goes to terminal L of OR gate ZB421A. The output of ZB421A is then the programmer advance which advances the programmer from the SR to the BN mode. The programmer advance appears on terminal L of ZB504. This is the S1 terminal of the one shot ZB504. The P1 terminal K of ZB504 is permanently primed, so each programmer advance will produce a 200 microsecond output on the inverted output terminal J of ZB504. This will be a negative-going pulse, 0 volts dc to -6 volts dc, of 200 microseconds duration. The negative transition of this pulse drives the ring drive ZB403B, input terminal F. The output of ZB403B on terminal N is the programmer advance pulse described in 7.05. This pulse will advance the programmer from the SR mode into the BN mode. The programmer advance pulse appears also on input terminal A of inhibit gate ZB114C, but the base input, terminal F of ZB114C, will be at 0 volts when the programmer is in the SR mode and terminal L of ZB418A passes the 0 volts potential on to terminal F of ZB114C. Thus, the output of ZB114C on terminal H will remain at -6 volts dc.

REVERSE CHANNEL CONTROL

7.22 Flip-flop ZB213C controls the reverse channel and when it is in the one state, 0 volts dc appears on terminal N of ZB213C and reverse channel will be turned on. This 0 volts output is applied to the base of inverter ZB222J. The emitter of ZB222J, terminal 30, is permanently grounded so it is acting as an inverter. This inverted output appears on terminal 29 of ZB222J with -6 volts dc corresponding to reverse channel on and 0 volts dc corresponding to reverse channel off. The output of this inverter appearing on terminal B9 of JB128 and is called reverse channel blind. When the terminal steps into the block number mode (BN mode), reverse channel is turned on. A positive transition, -6 volts dc to 0 volts dc, appears on terminal 8 of flip-flop ZB213C, the A1 input, and P1A input terminal 9 is permanently primed so the flip-flop ZB213C set to the one state and reverse channel will be turned on.

7.23 If the block number is high (block high) the P0A terminal 5 will be primed and the second delayed clock, appearing on the 0A input, terminal 4, will shut off reverse channel by resetting the flip-flop ZB213C to the 0 state. Reverse channel will now remain on until an error has been detected. When an error is detected, the programmer will step into the back up (BU) mode. This will present a positive transition to the 0B input of ZB213C, terminal 4. Since the P0B terminal is grounded (terminal 7), the reverse channel register will be reset to the zero state and reverse channel will be turned off. The reverse channel register reset signal will appear on terminal 2 of ZB213C; this will be 0 volts dc when the programmer is in the SR mode, the BU mode or the DEL mode. If any of these three modes are present, the 0 volts potential on terminal 2 of ZB213C will prevent reverse channel from turning on by preventing ZB213C from going to the one state. When the terminal is operating in the non-EDC mode, a 0 volts potential will appear at reverse channel on, which will keep reverse channel turned on.

BLOCK HIGH-LOW CONTROL

7.24 The block number control consists of a block counter, block number comparison gates and a block low register. The block counter consists of a three-element ring consisting of ZB407D, ZB407B, and ZB407C; one of these elements will be in the one state while the other two elements will be in the 0 state. The element in the one state represents the block number. If the ZB407D is in the one state, a 0 volts potential appears at output terminal D and this represents block number one (BN1). If the 0 volts output appears on terminal K of ZB407B, this represents block number 2 (BN2). If the 0 volts output appears on terminal M of ZB407C, this represents block number three (BN3). The block counter is advanced one number for each block advance pulse. The block advance pulse appears on terminal D of inhibit gate ZB115A, which at start up will not be inhibited, so the output K will present the block advance pulse to terminal F of ring driver element ZB404B to drive the block counter ring. One output pulse on terminal N of ZB404B appears for each block advance pulse. This pulse will simultaneously appear on terminals S, R, and N of ZB407.

7.25 The output of each block number drives the next higher block number. For example, the output of BN1 on terminal D drives the BN2 element on terminal J. Similarly, BN2

drives BN3 on terminal L. The output of BN3 drives BN1 on terminal A. When the advance pulse comes in, therefore, the block number will be advanced one number. If block number 3 exists, the block will be advanced to number one. When the block counter is in the block number 1 condition (BN1), a 0 volts output will be presented to terminal 34 of element ZB215. If the block counter is in block number 2 condition, a 0 volts potential will be presented to terminal 35 of ZB215. If the block number 3 condition is present, 0 volts will appear on terminal 36 of ZB215. As data is being received, and the programmer is in the block number mode, block numbers can be detected as described in 7.12. If the block number 1 is detected, 0 volts will appear on terminal 31 of ZB215. If block number 2 is detected, 0 volts will appear on terminal 32 of ZB215, and if block number 3 is detected, 0 volts will appear on terminal 33 of ZB215.

7.26 There are nine two input AND gates on ZB215 which are used for comparison of the incoming block number and the locally generated block number. If block numbers are the same, there will be an output from AND gates K, L, or M which will go through OR gate S, through emitter follower V, and will appear on terminal 3 of ZB215 with a 0 volts potential representing a block number OK condition. If the received block number is lower than the locally generated block number, there will be a 0 volts output on AND gate G, H, or J which will go through OR gate R, through emitter follower U, and will appear on terminal 4 of ZB215, a zero volts dc output representing the block number low condition. If the received block number is higher than the locally generated block number, a 0 volts dc output representing the block number low condition. If the received block number is higher than the locally generated block number, a 0 volts output will appear on AND gate N, P, or Q which will then pass through OR gate T and will appear on output terminal 2 of ZB215, the zero volts dc output representing a block high condition.

7.27 With a block high condition, the terminal shuts reverse channel off immediately before receiving the block. A 0 volts potential (block high) appears on the P0A terminal of the reverse channel register ZB213C on terminal 5. The second delayed clock then comes in on the 0A terminal of flip-flop ZB213C and sets the reverse channel register to the 0 state which shuts reverse channel off.

7.28 If the block number is low, the P1A input, terminal 26, of the block low register flip-flop of ZB213B will be primed. If the block number is not low, the terminal E of inverter ZB118B will be at -6 volts dc and its output on terminal B will be at 0 volts, which will then prime P0A of the block low register, terminal 19 of ZB213B. The block low register will be set by the block low register set pulse produced by the programmer in the following manner. The programmer advance pulse advances the programmer to the BN mode which puts 0 volts on the emitter of inhibit gate ZB114D, terminal C. The output of ZB114D will stay at -6 volts because base input terminal E is at 0 volts. When the next programmer advance (BN to BK) arrives, base input E of ZB114D goes to -6 volts for 200 microseconds, producing a positive-going pulse of 200 microseconds duration on the output of ZB114D, terminal J. This block low register set pulse then simultaneously appears on terminals 27 and 18 of the block low register, setting the flip-flop to the state that has been primed. If the block number is low, the P1A terminal is primed and the flip-flop will be set to the one state.

7.29 If the block number is not low, the P0A is primed and the flip-flop will be set to the 0 state. When the block number is low, therefore, a 0 volts output will appear on output terminal 14 of ZB213B. This 0 volts output will appear on inhibit gate ZB115A on terminal N, which will prevent the block advance pulse from advancing the block number. With a block low condition, a 0 volts signal will appear on base input terminal E of inhibit gate ZB115D which will inhibit the gated clock from producing a punch sample. Therefore, the punch will not punch as long as the block number is low.

7.30 When the block number is low, the inverted output of the block low register, terminal 17 of ZB213B will be at -6 volts. This -6 volts will appear on terminal 35 of error block register ZB213A. The P1A terminal on error block register will not be primed and no errors can be recorded. When the punch is not punching, because of a block low condition, all errors are ignored. The incoming block is not punched and the terminal waits for the next block number which will be OK.

7.31 The normal output of the block low register is applied to terminal F of inhibit gate ZB115C and the inverted output of block low register is applied to terminal M of inhibit gate ZB115B. These two inhibit gates determine

which pulse will be used by the character counter. If the block is being punched; that is, the block number is now low, then the inverted photo reader feed pulses will be counted. If the block number is low, there is an absence of photo reader feed pulses, so the gated clock will be counted. The photo reader feed pulse appears on terminal A of inhibit gate ZB115C and if the block number is not low, the output on H of ZB115C will be the photo reader feed pulses. The gated clock appears on terminal P of ZB115B and if the block is low, the gated clock will appear on output terminal L of ZB115B.

7.32 When the block number is OK, a 0 volts potential will appear on terminal L of OR gate ZB423B. If the block number is low, 0 volts will appear on terminal K of ZB423B. With a block low or a block OK condition, a 0 volts output will appear on terminal R of ZB423B. This is called the error reset prime and is used to reset the error block register so that error may be recorded. The error reset prime appears on P0A input of the error block register terminal 29 of ZB213A. The error block register will then be set 0 by the second delayed clock, which appears on the 0A input of the error block register, terminal 28 of ZB213A.

BLOCK NUMBER TO BLOCK TEXT ADVANCE

7.33 While the programmer is in the BN mode, the programmer advance pulse will be inhibited until a non-SR character is detected. While SR characters are being detected, 0 volts dc appears on terminal E of AND gate ZB511A, being primed in the BN mode by a 0 volts signal on terminal F of ZB511A. Therefore, a 0 volts output will appear on terminal B of ZB511A which will then be amplified by emitter follower ZB211E and will appear on terminal K of OR gate ZB418A. This will appear on terminal F of ZB114C and which will inhibit the output of ZB114C so that the programmer advance pulse cannot pass through to advance the programmer.

7.34 When an SR character is not detected, however, inhibit gate ZB114C will not be inhibited and the programmer advance pulse can appear on output terminal H of ZB114C from where it can then advance the programmer to the BK mode. Any character other than an SR character will advance the programmer to the BK mode. As soon as the programmer is in the BK mode, a 0 volts signal will appear on terminal M of ZB418A, which will hold the base input of ZB114C at 0 volts dc inhibiting further programmer advance pulses from advancing the programmer.

PHOTO READER - DATA LEVELS

7.35 When the terminal is in the BK mode, the gated clock will be present and the punch driver sample pulses will be driving the punch. As the punch is punching, the photo reader will read each character, one character after it has been punched. The output of the photo reader is then used to generate the two check characters. The 8 photo readers are connected to connector JB128, level 1 appearing on terminal F1 on up through level 8 appearing on terminal F8. Level 1 then appears on terminal 35 of pad circuit ZB217, level 2 on terminal 33, level 3 on terminal 31, level 4 of terminal 29, level 5 on terminal 27, level 6 on terminal 21, level 7 on terminal 19, and level 8 on terminal 17.

7.36 As described for the photo reader feed pulse, the output of the photo reader is at -6 volts when light is falling on it, and it goes to +6 volts when there is no light. A mark condition corresponds to -6 volts and a space condition corresponds to a +6 volts. The outputs of the pad circuit are on terminals 36, 34, 32, 30, 28, 22, 20, and 18 respectively of ZB217. These appear on the inputs of ZB216, terminals 23, 22, 17, 19, 20, 34, 28, and 9 respectively. When 7 level tape is being received, a -6 volt potential is permanently applied to the 8 level terminal 9 of ZB216 to hold the 8 level marking. If 6 level tape is being received, a -6 volts is applied to the 7 and 8 levels, terminal 28 and 9 of ZB216. If 5 level tape is being received, a ground is applied to input 23 of ZB216 for level 1 to hold level 1 spacing and levels 7 and 8 will have -6 volts applied. This means that a permanent space is being generated in level 1 and permanent marks are being generated for levels 7 and 8 when 5 level tapes are being received. The 8 inputs of ZB216 go through emitter follower amplifiers and then are applied to the base inputs of 8 inhibit gates (similar to the feed level described above).

7.37 The photo reader outputs are then gated by the character set pulse which is derived from the photo reader feed pulse in the following manner: when the terminal is in the BK mode, 0 volts appears on input terminal K of OR gate ZB422B and when the terminal is in

the EOB mode 0 volts appears on input terminal L of ZB422B. Thus, if the programmer is in the BK mode or the EOB mode, a 0 volts output appears on terminal R of ZB422B which primes P1 of one shot ZB107 on terminal K. The photo reader feed pulse appears on the S1 input of one shot ZB107, terminal L, which then produces a 200 microsecond positive-going pulse on terminal J, the normal output of one shot ZB107. This is called the character set pulse and is applied to input terminal E of power pulser ZB105, which is permanently primed.

7.38 The output on power pulser ZB105 appears on terminal H and is a positive-going pulse, -6 volts to 0 volts dc, of 15 to 35 microsecond duration, occurring 1.05 milliseconds after the photo reader feed pulse (in the BK or EOB mode). This output pulse is then simultaneously applied to the emitters of the 8 inhibit gates of ZB216. All inhibit gates of ZB216 on which a mark appears the -6 volts will allow the character set pulse to pass through. Therefore the output on terminals 13, 12, 11, 10, 8, 36, 35, and 21 of ZB216 will correspond to the marks and spaces of the 8 levels of the characters. 0 volts dc will correspond to a mark and -6 volts dc will correspond to a space. A mark will appear as a positive-going pulse 15 to 35 microseconds long. These 8 level outputs then appear on OR gates ZB508 and ZB509. Levels 1 through 4 appear on terminals E, K, C, and N respectively of ZB508 and levels 5 through 8 appear on terminals E, K, C, and N respectively of ZB509. Levels 1 through 4 will then appear on output terminals B, R, A, and S of ZB508, and will be called the first gated levels 1 through 4. Levels 5 through 8 will then appear on output terminals B, R, A, and S of ZB509 and will be called the first gated levels, 5 through 8.

7.39 The first gated level is then used to generate the horizontal check character. The first gated levels 1 through 4 then appear on input terminals D, C, P, and A of inhibit gate ZB103 and the levels 5 through 8 appear on terminals D, C, P, and A of inhibit gate ZB104. The bases of inhibit gate ZB103, terminals N, E, M, and F, and the bases of inhibit gate ZB104, terminals N, E, M, and F, are connected to the CK1 mode of the programmer. Therefore, the first gated level is allowed to pass through inhibit gates ZB103 and ZB104 in all modes except the CK1 mode. The outputs of these inhibit gates are called the second gated levels and appear on output terminals K, J, L, and H of ZB103 and K, J, L, and H of ZB104 respectively. The second gated level is used to generate the spiral check character.

HORIZONTAL CHECK CHARACTER

7.40 A horizontal check character is generated for each 80 character block that the receiver receives and is generated in the horizontal check character register, ZB206, A, B, C; ZB207, A, B, C; and ZB208, A, B. The horizontal check character, CK1, is one of the two characters used for error detection.

7.41 When the programmer steps into the BK mode, a storage reset pulse is generated by power pulser ZB109. In stepping into the BK mode, a positive transition, -6 volts dc to 0 volts dc appears on terminal E of power pulser ZB109 which is permanently primed so a positive-going pulse, 10 and 35 microseconds wide, will appear on output terminal H of ZB109. This is called the storage reset. The storage reset pulse comes in on the 0A terminal of the 8 horizontal check character register flip-flops. The P0A terminal of these flip-flops are permanently primed so the 8 register levels will be reset to the 0 state. In the 0 state the inverted output will go to 0 volts, which will prime the P1B terminal of all 8 levels. The first gated level is applied simultaneously to the 1B and the 0B terminals of the 8 check character register levels. If a mark appears on a particular level the positive transition on 1B of that level will cause the flip-flop to be set to the 1 state. If a space appears on that level the -6 volts signal will not cause the flip-flop to change states. All those levels that have changed state will now have 0 volts dc on the normal output of the flip-flop, which is connected to the P0B terminal of the same flip-flop. This means that the next incoming mark will set the flip-flop back to the 0 state. It can be seen, thus, that an incoming mark will change the state of the flip-flop, whereas an incoming space will not change the state of the flip-flop. When the 80 character block has been received, the number of marks in a particular level will either be even or odd. If an even number of marks have been encountered in a particular level, that level flip-flop will have been set and re-set an equal number of times so that the state of that flip-flop will be 0. If there has been an odd number of marks on a particular level that flip-flop has been set one more time and it has been re-set, so the final state will be the one state. The horizontal check character is represented by the states of the 8 flip-flops after the 80th character has been read into the horizontal check character register.

SPIRAL CHECK CHARACTER

7.42 The spiral check character is generated in the spiral check character register consisting of ZB203A, B, C, ZB204A, B, C, and ZB205A, and B. The spiral check character, CK2, is the second of the two characters used for error detection. The storage reset pulse is applied to terminals J and K of fan-out ZB110. From there it appears on output terminals N, M, L, E, D, C, B, and A of ZB110. These are connected to the inverted output terminals of the 8 flip-flops of spiral check character register. The storage reset pulse resets all of the registers to the 0 state. The inverted output of each of the 8 flip-flops then primes the P1B terminal of the same flip-flops. The second gated levels come in on terminals 0B and 1B. If a mark occurs on a particular level, it will set that level flip-flop to the one state.

7.43 After the character has been punched and read, the character set pulse appears on terminal F of pulse amplifier ZB108A and is a positive-going pulse of 200 microseconds duration. The trailing edge of the character set pulse occurs 200 microseconds after the set A pulse. This negative-going trailing edge causes a positive-going, 10 microsecond pulse to appear on output terminal N of pulse amplifier ZB108A. This 10 microsecond pulse is called the spiral shift pulse, and it appears on the 1A and the 0A terminals of all 8 flip-flops.

7.44 If a flip-flop has been set to the 1 state its normal output is connected to the P1A terminal of the next higher flip-flop. If the flip-flop has not changed states and is in the 0 state, the inverted output will prime the P0A terminal of the next higher flip-flop. Therefore, the spiral character shift pulse will transfer the one or the 0 condition to the next higher flip-flop. The 1 or 0 in level 8 will be transferred to level 1. Level 1 will be transferred to level 2, etc. The process of reading in a character and shifting it to the next higher flip-flop 200 microseconds later will continue for the 80 characters of the block. The state of 8 flip-flops at the end of the 80 character block will represent the spiral check character.

CHARACTER COUNTER

7.45 The character counter is used to maintain the proper length of the block. To accomplish this, feed holes are counted when punching or backing up the block and punch commands are counted when deleting. When a BN low condition exists, the 80 characters not being punched will be counted by counting the gated clock pulses. The output of the character counter is used to advance the programmer into the EOB mode when an 80 character block has been punched; into the DEL mode when a successful 80 character back up has occurred; and into the SR mode when an 80 character delete is complete. The character counter consists of a 10-element ring for counting units and a 9-element ring for counting 10s up to 80.

7.46 The character counter is reset to 0 using the counter reset pulse derived from the delete mode or the block mode signal. The delete mode signal appears on terminal F of ZB423A; the block mode signal appears on terminal E of ZB423A. When the programmer steps into the BK mode or the DEL mode, a positive transition from -6 volts to 0 volts appears on either terminal E or F of OR gate ZB423A. The same positive transition will appear on the output terminal of ZB423A. This transition is then inverted in ZB106A and again is inverted by ZB106B with the same transition appearing on terminal B of ZB106B. This is called the counter reset. The counter can also be reset by a punch back-up signal, described previously. When the punch has been told to back up the tape, a punch back-up signal will be produced (a positive-going transition from -6 volts dc to 0 volts dc). This signal occurs when the programmer steps into the BU mode. The counter reset signal appears on input terminal C and the punch back up signal appears on input terminal D of OR gate ZB423C. Either output of ZB423C on terminal A will reset the counter.

7.47 This reset signal is then inverted by ZB119C with the output appearing on A, being now a negative-going transition, 0 volts dc to -6 volts dc. It is then applied to terminal H of ring reset ZB409A and terminal H of ring reset ZB408A.

7.48 Both ring reset elements are primed by having terminal K grounded. The output of ring reset ZB408A on terminal P is then applied on terminal F of units counter element ZB410A which sets the units counter to 0. The output of ring reset element ZB409A similarly will reset ZB413A to zero, the zero state of the tens counter. When the block number is not low, inverted photo reader feed pulses will be counted. When the block number is low, the gated clock will be counted.

7.49 In the delete mode, the actual punch commands will be counted. A block number low condition inhibits ZB115C on terminal F while it enables ZB115B on terminal M so that the gated clock will pass through to terminal A of ZB512C. The block number low condition will inhibit the gated clock at ZB115B and will enable the photo reader feed pulses to appear on terminal A of ZB512C. This in turn will be inhibited if the programmer is in the delete mode which would present 0 volts to terminal F of inhibit gate ZB512C. The delete mode signal also appears on AND gate ZB511D on terminal N. This is gated with the inverted punch sample which is on terminal P of ZB511D. When in the delete mode, this punch sample appears on terminal S of ZB511D and goes to emitter follower ZB211G on terminal 23. After amplification it appears on output terminal 26 of ZB211G and then is sent to terminal N of OR gate ZB424D.

7.50 When the programmer is not in the delete mode, the inverted punch sample will not be passed and inhibit gate ZB512C will be enabled so that the gated clock or the photo reader feed pulses can appear on terminal P of OR gate ZB424D. Therefore the output of OR gate ZB424D on terminal S will either be derived from the inverted punch sample, the gated clock, or the photo reader feed pulse depending on the conditions in the receiver. This output goes to input terminal F of ring drive ZB408B.

7.51 The output of ring drive ZB408B on terminal N then drives the units counter. The units drive is a negative-going transition 0 to -6 volts, 10 microseconds wide, one occurring with every negative-going transition to the input of ZB408B. The units counter is primed in such a way that each unit drive pulse will step the counter to the next higher digit. When the units counter is in the 9 position, the output of terminal K of ZB412C goes to ring reset element ZB408A on terminal R and is sent on through to terminal P of ZB408A, and then appears on terminal F of ZB410A, resetting the counter to the 0 state. This output of the 9 position also appears on inverter ZB118C on terminal C, is inverted and appears on output terminal A. From there it is sent to terminal F of ring drive element ZB409B. The output of ring drive element ZB409B, on terminal N, will be a negative-going pulse, 0 volts dc to -6 volts dc, 10 microseconds wide.

7.52 When the unit counter steps from the 9 position to the 0 condition, the output of ring drive element ZB409B will step the tens counter from the 0 state to the 10 state. The tens counter will not be stepped again until the next tens drive has been generated by the unit counter going from 9 back to the 0 position.

EOB CONTROLS

7.53 When the punch has recorded 80 characters, the programmer will step to the EOB mode, by looking at the output of the tens counter. When the tens counter is in the 70 position, the 0 volts output on terminal M of ZB414A will appear on terminal N of ZB420D. This AND gate will be primed when the terminal is not in the back up mode. Therefore, terminal P of inverter ZB119D will be at -6 volts dc and output terminal S of ZB119D and input P of ZB420D will both be at 0 volts dc. The output of AND gate ZB420D will appear on terminal S, which will go to input terminal H of pulse amplifier ZB108B.

7.54 When the counter steps from the 70 position to the 80 position, having read the 80 character block, the voltage on terminal H of ZB108B will go to -6 volts dc. This negative transition will cause a positive-going pulse to appear on output terminal D of ZB108B. This will be a positive-going pulse, -6 volts dc to 0 volts dc 10 microseconds wide and is called the block complete pulse which is then sent to terminal P of OR gate ZB421A. The output of this OR gate on terminal R produces the programmer advance pulse that advances the programmer from the block mode into the end of block mode.

7.55 When the programmer is in the EOB mode, the EOB character will be checked for accuracy by the EOB character control and 0 volts dc appears on terminal D of AND gate ZB419C. This will allow the programmer advance pulse, appearing on terminal C of ZB419C, to pass through the AND gate to appear on terminal A of ZB419C, and on input terminal P of inhibit gate ZB114B. If the EOB character has not been detected, this pulse will be allowed to pass through inhibit gate ZB114B and will appear on output terminal L. From there it will appear on terminal L of OR gate ZB419A and will set the error block register. If the EOB character is successfully detected, a 0 volts signal will appear on terminal M on ZB114B and the programmer advance pulse will be inhibited from setting an error.

ERROR DETECTION (Figure 21)

7.56 The presence or absence of an error is recorded in the error block register. If the error block register flip-flop is in the 1 state, this represents the error condition, and if it is in the 0 state, this represents a no error condition. When the programmer is in the BN mode, a 0 volts dc signal will appear on terminal 32 of ZB213A, priming the P1B terminal. The next programmer advance pulse which appears on the 1B terminal of the error block register (terminal 33 of ZB213A) will set the error block register to the 1 state. If the block number is not high, the error reset prime will be at 0 volts dc on the P0A input terminal 29 and the second delayed clock, which appears on the 0A terminal (terminal 28 of ZB213A) will reset the error block register flip-flop to the 0 state. However, if the BN is high, the prime will not be present and the 1 state will be retained.

7.57 To check the check characters for errors, the eight data bits of CK1 and CK2 are read into the check character registers for comparison with the locally generated checked characters. The normal data bits are presented to the 8 inhibit gates of ZB209 on terminals 3, 6, 10, 13, 23, 26, 17, and 19, level 1 to level 8. These will be inhibited until a set B pulse comes in on terminal N of ZB111A.

7.58 The set B pulse is derived from the RD sample pulse. The first delayed sample pulse appears on terminal C of AND gate ZB418C. This AND gate will be enabled in the CK1 mode or the CK2 mode when 0 volts dc appears on terminals 5 or 7 respectively of OR gate ZB210D. The 0 volts output from terminal 8 of ZB210D enables AND gate ZB418C on terminal D so the first delayed sample will appear on output terminal A of AND gate ZB418C, will be amplified by an emitter follower ZB211N, to become the set B pulse on terminal 18 of ZB211N. This set B pulse is inverted by ZB111A and will present a negative-going pulse on terminal R of ZB111A. This will be amplified by emitter follower ZB211K and will be presented to the base inputs of the 8 inhibit gates of ZB209. The normal data bits will be inhibited until a set B pulse comes in on the bases of the inhibit gates of ZB209. The set B pulse will allow the normal bits to pass through and be presented to the OR gates ZB508 and ZB509 (terminals F, L, D, and P of ZB508, and terminals F, L, D, and P of ZB509 respectively). These then become the first gated levels.

7.59 During the CK1 mode the incoming check character (CK1) is read into the horizontal check character register. If there has been no error the incoming check character will be an inverted character from the one that has been locally generated. When the incoming check character is read into the horizontal check character registers, all of the flip-flops not already in the 1 state will be set to the 1 state. This means that with no error being detected, all of the flip-flops of the horizontal check character register will come up in the 1 state. If any of the levels is an error, that level will come up in a 0 state and the inverted output of that level will then be presented to the OR gate ZB210B. The OR gate ZB210B has eight inputs one for each level so if there is an error in any one level, there will be a 0 volts dc output on terminal 21 of ZB210B. This scheme detects if there has been an error in the check character 1 and the CK1 readout will present a 0 volts signal to terminal 11 of emitter follower ZB211L which will then be presented to terminal H of AND gate ZB418B. Terminal E of ZB418B is at 0 volts dc when the programmer is in the CK1 mode. With both terminals E and H of ZB418B at 0 volts the AND gate is primed so that the second delayed clock, which appears on the terminal F of ZB418B, can pass through and appear on output terminal B of ZB418B. From there it appears on terminal 29 of ZB211A, is amplified and appears on terminal 19. It then goes to OR gate ZB419A on terminal K. A 0 volts dc input to OR gate ZB419A means that there has been an error.

7.60 If there has been a CK1 error, the second delayed clock will appear on the output of ZB419A, terminal R, and will be presented to terminal 34 of ZB213A which is the 1A terminal of the error block register flip-flop. If the block number has not been low, the P1A terminal of the error block register, terminal 35 of ZB213A, will now be primed and the error block register will be set to the 1 state, recording the error.

7.61 While the programmer is in the CK1 mode, the incoming check character is inhibited by inhibit gates ZB103 and ZB104 from being read into the spiral check character registers, preserving the spiral check character that has been locally generated. The next programmer advance pulse advances the programmer into the CK2 mode. The data in the second gated levels now represents the check character 2 and it is read into the spiral check character

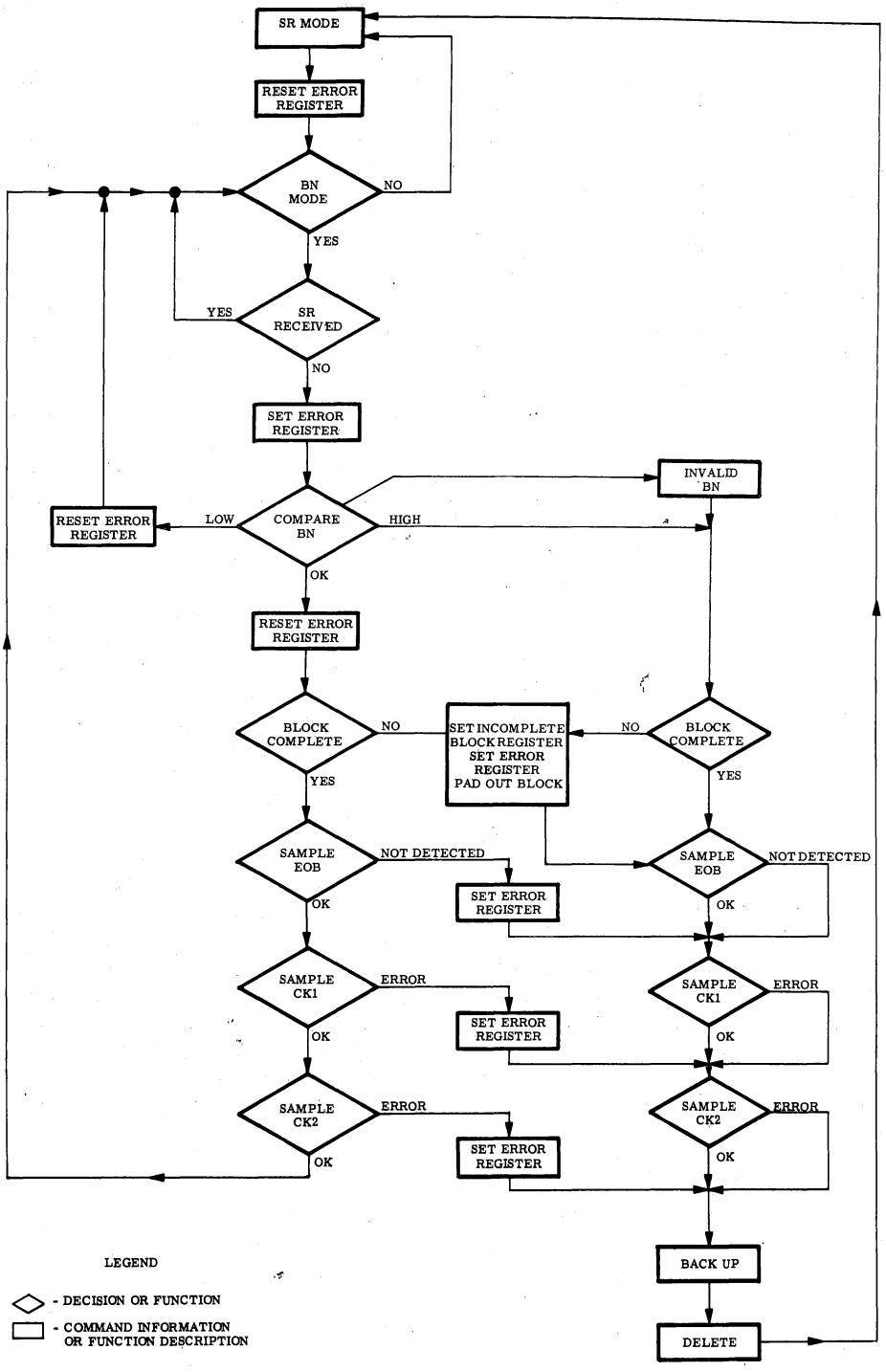


Figure 21 - Error Circuit Logic

registers. The CK2 is inverted from the locally generated one so all of the flip-flops should come up in the 1 state. If any level is in error, the corresponding flip-flop will come up in the 0 state. The inverted output of the flip-flop with an error will be 0 volts dc, which is applied to OR gate ZB210A. The inputs of OR gate ZB210A, terminals 35, 34, 33, 32, 21, 30, 19, and 18, are connected to the inverted outputs of the 8 flip-flops of the spiral check character register and if an error occurs in any one level, a 0 volts output will appear on terminal 29 of ZB210A. This is called the CK2 readout.

7.62 The CK2 readout will then be amplified by emitter follower ZB211M and the 0 volts output will be presented to input terminal H of AND gate ZB419B. Terminal E of ZB419B will be at 0 volts potential when the programmer is in the CK2 mode. With terminals E and H of ZB419B at 0 volts, terminal F is primed so that the second delayed clock, which appears on terminal F of ZB419B, can pass through the AND gate and appear on terminal 33 of ZB211B which, in turn, sends the second delayed clock to terminal P of OR gate ZB419A, from where it will be sent to the error block register to set in the error.

7.63 While the programmer is in the EOB mode, if a valid EOB character is not detected, a positive-going transition will appear on terminal L of ZB419A. From there it will be sent onto the error block register so that an error can be recorded. Finally, if an incomplete block has been detected, a positive-going transition will appear on terminal M of ZB419A and an error will be similarly recorded by the error block register.

ADVANCE FROM EOB TO BU MODE

7.64 When the programmer is in the CK1 mode, the CK2 mode or the EOB mode, there is no 0 volts input to OR gate ZB418A, so that inhibit gate ZB114C will be enabled allowing the programmer advance pulse to advance the programmer. When the programmer is in the CK2 mode and there is no error present, the programmer will be set back into the BN mode, as described in 7.08. If, however, there has been an error, the programmer advance pulse will advance the programmer to the back-up mode.

PUNCH REVERSE FEED

7.65 When the programmer steps to the back up mode, there will be a positive transition applied to terminal L of ZB505, a one shot that is permanently primed by having terminal K grounded. The output of ZB505 will be a positive-going pulse, 70 milliseconds wide, appearing on terminal J, the normal output. This pulse will then appear on terminal H of power amplifier ZB506A. With a 0 volts potential on the input H of power amplifier ZB506A, there will be a circuit to ground from terminal A and pin C3 of connector JB128 so that the punch reverse feed magnet will have a ground. It will operate to trigger the back-up mechanism.

BACK-UP DETECT

7.66 While the programmer is in the back up mode, there will be 0 volts dc on terminal P of OR gate ZB418A. As long as this voltage appears, inhibit gate ZB114C will inhibit programmer advance pulses from advancing the programmer. While the tape is being backed up, the character counter will be counting the photo reader feed pulses. When the 80th count has been obtained, a 0 volts signal will appear on terminal L of AND gate ZB420B. The other input of this AND gate, terminal M, will be at 0 volts because the programmer is in the BU mode. With the two inputs of AND gate ZB420B being at 0 volts, the output of terminal R will be at 0 volts dc which will be presented to terminal N of ZB119A, will be inverted to present -6 volts dc to base input terminal M of inhibit gate ZB116B and will present a 0 volts potential to base input, terminal F, of inhibit gate ZB116C. Thus, if there has been a good back up and 80 characters counted, inhibit gate ZB116B will be enabled and ZB116C will be inhibited.

7.67 When the back-up is complete, the back-up switch on the back-up mechanism will close, and there will be a negative transition appearing on terminal C1 of connector JB128. This negative transition will appear on the input of IPS card ZB123, terminal H. ZB123 will delay this negative transition about 20 milliseconds before applying it to input terminal H of pulse amplifier ZB117B. This negative transition will cause a 10 microsecond positive pulse to appear on terminal D of ZB117B. This pulse will then be applied to inhibit gate ZB116B on terminal P and inhibit gate ZB116C on

terminal A. If there have been 80 characters counted, the pulse will be allowed through ZB116B and there will be a back-up detect signal on terminal L of ZB116B.

7.68 If there have not been 80 characters counted, ZB116B will be inhibited and ZB116C will be enabled so there will be a pulse out of inhibit gate ZB116C on terminal H. This will be presented to back up error register flip-flop on terminal 8 of ZB214C, the 1A input. The P1A terminal of ZB214C is permanently primed by having terminal 9 grounded so the back up error register flip-flop will be set to the 1 state. With the back-up error register in the 1 state, there will be a back-up alarm represented by a 0 volts signal appearing on terminal 1 of ZB214C.

DELETE

7.69 When the back-up has been successfully completed, the back-up detect signal will appear on input terminal M of OR gate ZB421A. The output of ZB421A on terminal R is then the programmer advance pulse that advances the programmer into the DEL mode. In the DEL mode, a 0 volts signal will appear on input terminal S of OR gate ZB418A which will be sent on to inhibit gate ZB114C, terminal F, to inhibit further programmer advance pulses from advancing the programmer. 0 volts dc will now be applied to input terminal D of OR gate ZB417C. Its output on terminal A goes to terminal P of inverter ZB118D where it is converted to a -6 volts dc, which is applied to terminal P of gated oscillator ZB416. A -6 volts signal on terminal P of ZB416 allows the gated oscillator to start oscillating.

7.70 This gated oscillator is called the clock generator: it generates the pulses needed for the punch drive for deleting. The pulses appearing on output terminal A of ZB416 are a stream of positive-going 10 microseconds pulses, the first one occurring approximately 5 milliseconds after the input voltage goes to -6 volts. These pulses are applied to OR gate ZB422A on terminal F and then they are sent on through the normal path to produce the gated clock from which the punch command pulses are generated. The output of OR gate ZB417C is also applied to the base of inhibit gate ZB114A, terminal N. This inhibits the incoming RD sample pulses from producing the gated clock.

7.71 During deletion, all of the punch levels will be primed by 0 volts dc appearing on terminal C of OR gate ZB424C. Its output, terminal A, is applied to all of the punch driver prime levels and 0 volts dc on a punch prime level will produce a mark for that level. Thus, an all marks character will be punched as was described in 7.45.

7.72 The character counter will be reset to 0 and the inverted punch sample pulses counted. Punching of the all marks characters will continue until 80 characters have been counted and a block complete pulse is generated. A block complete pulse is applied to terminal P of OR gate ZB421A and the programmer advance pulse out will advance the programmer back into the SR mode.

ALARMS

A. Feed Alarms (Figure 22)

7.73 The feed alarm circuit checks that the tape has moved after each punch command. If two punch commands are recorded, without an intervening photo reader feed pulse, a feed alarm will be recorded. Feed alarm detection is done by two flip-flops, the feed alarm prime register and the feed alarm register. The feed alarm register, ZB214A, has its P1A and P0A terminals permanently primed by being grounded. The feed alarm register, ZB214B, has its P1B terminal primed by the normal output of the feed alarm prime register. When the receiver is reset, the feed alarm prime register and the feed alarm register will be reset to the 0 state by a 0 volts signal on terminal 13 of ZB214A and terminal 17 of ZB214B. (See 7.77.) The punch sample is applied to terminal P of OR gate ZB423D. It will pass through and appear on terminal S and be applied to terminal 1A of feed alarm prime register ZB214A (terminal 34). ZB214A will be set to the 1 state and the normal output on terminal 12 will go to 0 volts which will be applied to terminal 24 of ZB214B, priming the feed alarm register. The photo reader feed pulse that follows the punch command by about 2.5 milliseconds will then be applied to terminal 28 of ZB214A, which will reset the feed alarm prime register back to the 0 state and will remove the prime from the feed alarm register. If, however, a photo reader feed pulse is not detected and another punch sample is presented to the feed alarm circuit, the feed alarm register will still be primed so that the punch sample will set the feed alarm register

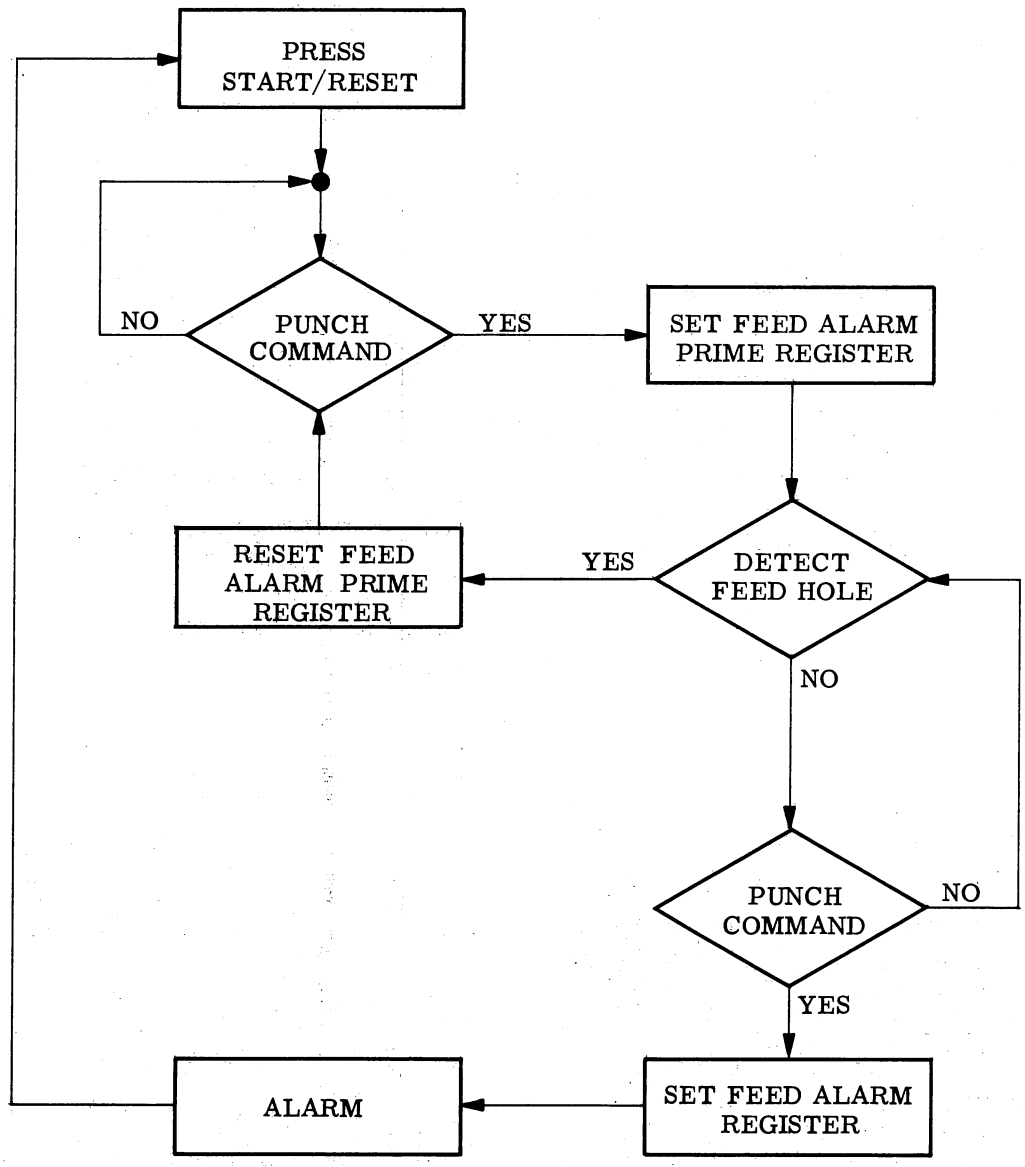


Figure 22 - Feed Alarm Logic

to the 1 state, the punch sample being applied to terminal 25 of ZB214B. The FA indicating light will go ON. With the feed alarm register in the 1 state, a 0 volts output appears on the normal output of ZB214B, terminal 14. This is then applied to OR gate ZB424A, which collects all of the various alarms for the equipment, and presents them as an alarm output. The 0 volts output of ZB424A is then applied to emitter follower ZB211Q on input terminal 3. Its output on terminal 6 is applied to relay driver ZB506B on terminal K and provides a circuit to ground from terminal S as an alarm output.

7.74 This alarm condition will also present 0 volts dc to terminal E of OR gate ZB417B, whose output (terminal B) is presented to terminal 24 of emitter follower ZB211H. The output

of this emitter follower, terminal 27, goes to the programmer and sets it back to the SR mode. As a result, any alarm condition sets the programmer into the SR mode, and stops the receiving terminal.

B. Punch Test Alarm

7.75 When an error has been detected in the punch test mode, 0 volts dc will appear on terminal H of OR gate ZB424A and the preceding described alarm condition will result. The PTA indicating light will go ON.

C. Back-Up Alarm

7.76 As described in 7.68, if the back up is not accurate, the back up alarm condition will be produced and a 0 volt signal will appear on terminal F of ZB424A, so a similar alarm condition will be set up. The BUE indicating light will go ON.

STOP AND RESET

7.77 The stop condition can be initiated by grounding terminal B1 of connector JB128. With an external contact to ground, the receiver will be set into the stop condition. The integrated pulse shaper (IPS) card ZB614 has its input H normally held at -6 volts to through terminal board ZB428. When the contact goes to ground, the output of the IPS, terminal K, will go to 0 volts. The integrated pulse shaper card is set to reject pulses shorter than 500 microseconds, so that noise cannot stop the terminal. The output appears on terminal K of ZB614 (a positive transition from -6 volts dc to 0 volts dc). A 0 volts signal will then be applied on fan out gate ZB503D on terminal S. Its output, on terminal N, is called error hold which is then applied to terminal 12 of the error block register, ZB213A, holding the error condition while the receiver is stopped. This stopped condition also produces the SR inhibit signal which is applied to terminal M of inhibit gate ZB512M. This prevents an SR character from advancing the programmer to the BN mode while the terminal is stopped. The positive transition from ZB614 is also applied to input terminal F of pulse amplifier ZB425A, but no action will occur until it receives a negative-going transition. This transition is also applied to terminal E of inverter ZB119D. Its output on terminal D will then be a negative-going transition from 0 volts dc to -6 volts dc. It is simultaneously applied to inhibit gate ZB209J, terminal 31, and ZB209K, terminal 34, enabling both of these inhibit gates. When the programmer is in the SR mode, a 0 volts signal appears on terminal 33 of ZB209K so 0 volts dc appears on the output terminal 32 of ZB209K. From there, it is applied to terminal H of OR gate ZB417B, producing a stop and reset signal, setting the programmer into the SR mode. The input to inhibit gate ZB209J is called non-EDC stop prime (see 7.89).

7.78 To start and reset the receiver, the ground must be removed from terminal B1 of JB128. This will cause a negative-going transition from the 0 volts dc to -6 volts dc, to appear on terminal H of IPS card ZB614, which will present a negative-going transition to terminal F of pulse amplifier ZB425A. Its output will then be a positive-going pulse, 10 microseconds wide, called the reset pulse. The reset pulse is applied to fan-out gate ZB503B on input terminal R. One output of this gate, terminal K, is applied to terminal 13 of ZB214A setting the feed alarm register to the 0 state. Another output of ZB503B terminal M, is applied to terminal 17 of ZB214B setting the feed alarm register to the 0 state. The third output of this fan-out terminal L is called the back up error reset which is applied to terminal 2 of ZB214C, which will reset the back up error register to the 0 state. The reset pulse will be applied to terminal 4 of ZB205C to reset the punch test alarm register. Finally, the reset pulse will be applied to terminal 6 of ZB208C to reset the incomplete block register to the 0 state.

PROGRAM TEST

7.79 In the program test mode the programmer may be advanced one mode at a time by manually pressing the push button SWB502. To put the receiver in the program test mode, switch SWB501 must be put in the TEST position. This prevents programmer advance pulses from being applied to ZB504 and allows advance pulses to come from the programmer test push button switch SWB502. Pushing SWB502 grounds terminal H of IPS card ZB507, causing a positive transition to appear on output terminal K of ZB507, which will be applied to terminal L of ZB504. Each press of SWB502 will result in one output pulse of 200 microseconds duration, from output terminal J of ZB504. IPS card ZB507 prevents noise pulses shorter than 500 microseconds from producing an output. Each press of the programmer test push button switch will advance the programmer to the next mode.

The programmer will advance from the SR to BN mode to BK mode, EOB mode, CK1 mode, CK2 mode, BU mode, DEL mode, and then back to the SR mode. This program test mode is important to the serviceman to determine if the proper actions are occurring in each mode.

INCOMPLETE BLOCK DETECT

7.80 The incomplete block detect circuit provides a means for completing blocks that are not complete for one reason or other. This may be due to the sender stopping transmission; it may be due to breaks in transmission due to line breaks, etc. The receiver will detect loss of transmission and will complete the 80 characters of the block being received, will record an error, and will delete that block. The first delayed sample, occurring 50 microseconds after the RD sample pulse, will be applied to input terminal L of one-shot ZB510. This will cause a positive output pulse of 2 milliseconds duration to appear on terminal J of ZB510, which will then be applied to input terminal P of gated oscillator ZB415 which is set to start oscillating if there is a lack of pulses being applied to the input terminal or if they are spaced farther apart than 45 milliseconds. This is just slightly longer than the SR rate. With loss of data, there is a lack of RD sample pulses so that pulses will not appear on terminal P of ZB415. This gated oscillator, called the recycle timer, will start oscillating, with its output appearing on terminal A of ZB415 being a series of positive pulses 10 microseconds wide spaced 45 milliseconds apart. The first pulse out, applied to terminal M of OR gate ZB419A, will set an error into the error block register. It is also applied to input terminal 1A of incomplete block register flip-flop ZB208C. This pulse will set the flip-flop to the 1 state because the P1A terminal (terminal 9) is grounded. Terminal 1 of ZB208C will go to 0 volts dc which will then go to OR gate ZB417C on terminal C. The IBK indicating light will go ON. This will cause the gated oscillator ZB416 to start oscillating as described in the delete mode (7.69), and the gated clock will produce punch sample pulses.

7.81 When the 80 characters have been punched, the programmer will step into the EOB mode and the error correction cycle will begin because an error has been recorded. The programmer will then go into the back up mode, into the delete mode, and will return to the SR mode. In the SR mode, the programmer again looks for an SR character. When the programmer detects an SR character and advances into the BN mode, an incomplete block register reset pulse will be produced. The detected SR character will produce a 0 volts dc signal on input terminal C of OR gate ZB422C. The output of ZB422C (terminal A) is called the incomplete block register reset and is applied to terminal 4 of ZB208C which will set the incomplete block register flip-flop back to the 0 state. During normal EDC operation after each successful block has been received, a block advance pulse is generated. This block advance pulse is applied to input terminal D of OR gate ZB422C to produce an incomplete block register reset pulse. The incomplete block register can also be reset by pressing the stop button as described in 7.78.

FIGS INSERT CONTROL (Figure 23)

7.82 When operating in the 5 level mode, the delete character corresponds with the letters character of 5 level Baudot code. This circuit stores the figures command and reinserts it into the tape when there has been a delete while the figures character was up. The circuit consists of two recognition gates which recognize the FIGS or LTRS character, a FIGS detect register which stores the figs command and an insert figs register which primes the figs insert control register, which inserts the figs character when necessary. The AND gate ZB514A is set to recognize the letters character for 5 level Baudot code. The AND gate ZB514B is set to recognize the FIGS character of 5 level Baudot code. This is accomplished by applying the normal bits for levels 2, 3, 5, and 6 to four of the input of these two AND gates. The 4th normal bit is applied to the remaining input terminal of the letters detect gate and the inverted bit 4 is applied to the remaining input terminal of the FIGS detect gate. When a LTRS character is detected, all of the inputs of AND gate ZB514A will be at 0 volts and a 0 volts output will appear on terminal B of ZB514A. When a FIGS character is detected, all of the inputs of AND gate ZB514B will be at 0 volts dc so a 0 volts output will appear on terminal R. When the terminal is in a BK mode, 0 volts will be applied to terminal D of diode ZB428 allowing the 0 volts signal from the figs detect gate to be applied to terminal 26 of FIGS detect register ZB221B. When the second delayed clock is applied to terminal 27 of ZB221B, the FIGS detect register will be set to the 1 state indicating that a FIGS character has been received. The normal output, terminal 14, of ZB221B, will go to 0 volts dc which primes AND gate ZB417A on terminal M.

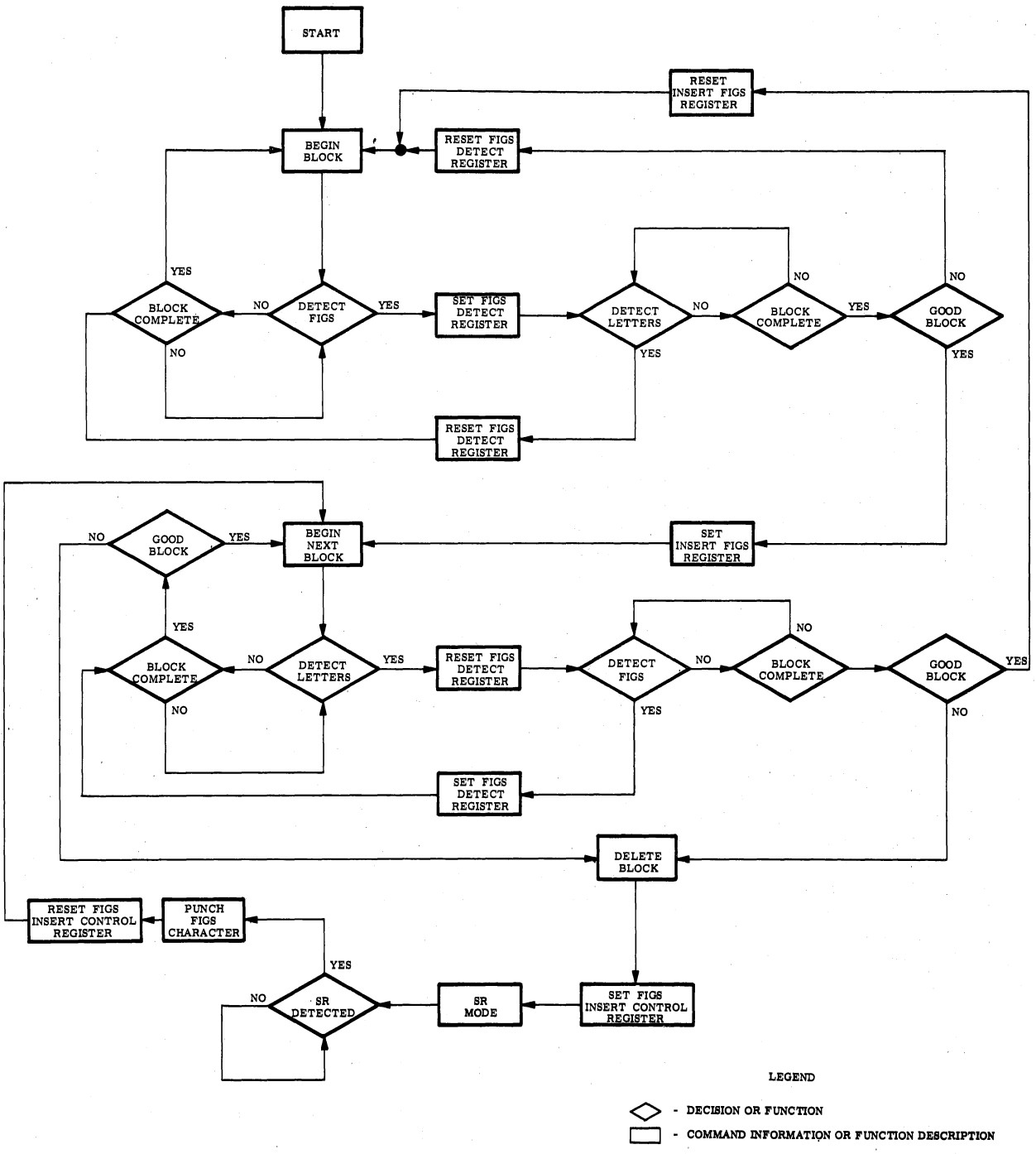


Figure 23 - Figures Insert Logic

7.83 Since the receiver is in the BK mode, terminal K of ZB417A will also be in 0 volts. When a LTRS character is detected, 0 volts will appear on terminal L of ZB417A. Since this AND gate is primed, an output of 0 volts will appear on terminal R of ZB417A. This will prime P0B of the FIGS detect register on terminal 22 of ZB221B and the second delayed clock, applied to terminal 23 of ZB221B, will set the figs detect register back to the 0 state. Therefore, a FIGS character will set the FIGS detect register and a subsequent LTRS character will reset the figs detect register.

7.84 When the figs detect register is in the 1 state, a 0 volts signal will prime P1A of the insert figs register, terminal 9 of ZB221C. When the figs detect register is in the 0 state, a 0 volts signal will prime the P0A of ZB221C on terminal 5. The insert FIGS register will only be set when the programmer goes into the BK mode. Therefore, the insert FIGS register will be set to the 1 state if the FIGS character is up from the preceding block and it will not be set if the LTRS character is up. The insert FIGS register will be set to the 0 state if a block advance pulse comes while the LTRS character is up.

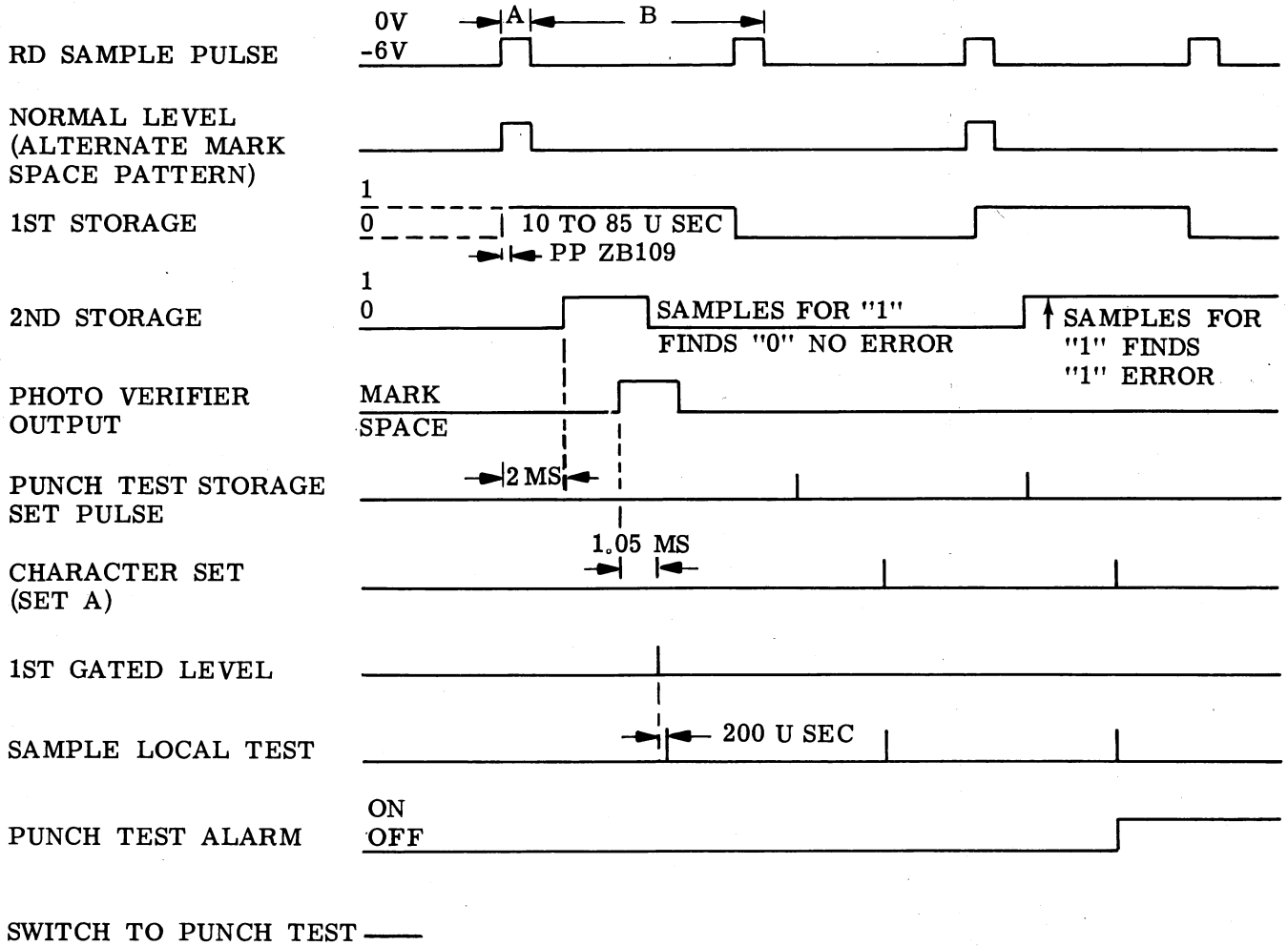
7.85 With the insert FIGS register set to the 1 state, it means that the preceding block had the FIGS character up last. If the next block is deleted, the FIGS character will have to be reinserted. The insert FIGS, represented by 0 volts on terminal 1 of ZB221C, will be presented to input terminal C of AND gate ZB511C. If the next block had an error block and the programmer goes into the DEL mode, a 0 volts signal on terminal D of AND gate ZB511C will cause a 0 volts output on terminal A of ZB511, which will prime P1A of the FIGS insert control register, on terminal 35 of ZB221A. The FIGS insert control register will only be allowed to operate when the receiver is in the 5 level mode. In the 6, 7, or 8 level mode, ground is applied through SWB602 to terminal 18 of ZB221A which will keep this flip-flop in 0 state. If a delete has followed a block that had the FIGS character and the insert FIGS register had been set with 0 volts dc being subsequently applied to terminal 35 of ZB221A, the next block complete pulse, applied to input 1A, terminal 34 of ZB221A, will set the FIGS insert control register to the 1 state, presenting a 0 volts output on terminal 12 of ZB221A called the FIGS prime signal. This is applied to the P0A input, terminal 29 of ZB221A. This FIGS prime signal is applied to emitter terminal L of pulse inhibit ZB513A. This will be inhibited when the terminal is in the SR mode and 0 volts is applied to base terminal S of the ZB513A.

7.86 When the programmer is stepping out of the SR mode into the BN mode, the negative transition on terminal F of ZB513A will cause a positive pulse at output terminal N of ZB513A. The positive transition of this pulse is called the punch command figs insert, and is applied to terminal L of ZB112 from which one punch sample is produced. The figs prime signal is also applied to input terminal 29 of emitter follower ZB223A from which all punch driver levels are primed. This signal is also applied to the base terminal N of inhibit gate ZB512A, which keeps level 4 from being primed. Therefore, the additional character that is punched will be an all-mark character except for level 4, which will be spacing. This will be an extra FIGS character, put into the tape after the 80 character delete.

7.87 When the programmer steps into the BK mode again, a positive-going transition will appear on terminal 28 of ZB221A. Since the P0A terminal is primed, the FIGS insert control register will be reset back to the 0 state. When the register is set, and 0 volts appears on terminal 1 of ZB221C. This 0 volts signal is also applied to the P1B terminal of ZB221C, terminal 24. When the programmer steps into the DEL mode, a positive transition is applied to the 1B input terminal 25 of ZB221B which sets the FIGS detect register to the 1 state. If, however, the LTRS character had been set into the insert FIGS register a 0 volts output would appear on terminal 2 of ZB221C which would prime the P0A input, terminal 19, of ZB221D. If the programmer has stepped into the BU mode, indicating a bad block, the FIGS detect register will be set back to the 0 state by a positive transition appearing on the 0A input, terminal 18, of ZB221B.

INDICATING LIGHTS AND TEST LAMP

7.88 The indicating lights which appear on the front panel of the EDC module are triode indicating lights. The plate of each indicating light is provided with +50 volts dc. The fila-



TIMING

SPEED	A	B
1050 WPM	0.953 MS	9.53 MS

Figure 24 - Punch Test Timing

ments are supplied with 1 volt ac. The grid of each indicating light is provided with the signal that is to be indicated. If a -6 volts signal appears on the grid of the indicating light, the light will be held off. If the grid goes to 0 volts dc, however, the light will illuminate. The test lamp on the bottom row of the indicating lights can be used for testing various points of the module to determine if -6 volts or 0 volts is present. To use the test lamp, attach a test lead to terminal 10 of DSB401. Attach the other end of the test lead to the point to be indicated. When the point being tested is at -6 volts dc, the lamp will be off. If the point being tested goes to ground, the test lamp will illuminate.

NON-EDC

7.89 In the non-EDC mode, the receiver will punch all incoming data and all the EDC circuitry will be disabled. The programmer is locked in the SR mode and reverse channel is held on continuously. When the NON-EDC pushbutton is pressed, a ground will be applied to terminal A2 of JB128. This ground will lock the programmer in the SR mode (SR mode hold). 0 volts dc is applied to terminal F of OR gate ZB417B producing a stop and reset signal to set the programmer into the SR mode and hold it there as long as this ground appears on terminal A2 of JB128. Ground is also applied to terminal

B of fan-out gate ZB503A. Output terminal F of ZB503 will go to 0 volts and will be applied to terminal N of OR gate ZB422D. This will simulate a BK condition so that the punch will be enabled. On terminal E of ZB503A a 0 volts dc signal will be called the pad out inhibit and will be applied to terminal 2 of incomplete block register ZB208C holding this flip-flop in the 0 state so that this circuit is disabled. Thus, the terminal will stop immediately without padding out when transmission is stopped. For each RD sample pulse received, one character will be punched. Reverse channel is held on because terminal H of ZB503A will be at 0 volts dc. This reverse channel on signal will be applied to terminal 1 of reverse channel register ZB213C. It will hold reverse channel on so that a remote sending terminal which is examining for reverse channel will be able to send.

7.90 Ground will also be applied to terminal B of fan-out ZB421B. Output terminal E of ZB421B will go to 0 volts dc and is called feed alarm inhibit. Feed alarm inhibit is then applied to terminal 17 of feed alarm register ZB214B, holding this register in the 0 state so that no feed alarm can be detected. The 0 volt output on terminal F of ZB421B is called BN low reset. This will be applied to terminal 17 of block low register ZB213B, keeping this flip-flop in the 0 state, disabling the BN high-low control. The 0 volt output appearing on terminal H of ZB421B is called non-EDC stop prime, applied to base input terminal 30 of inhibit gate ZB209J. When the terminal is in the stop condition, the 0 volt output on terminal 29 of ZB209J is applied to base input terminal E of inhibit gate ZB116D. This will prevent 0 volts dc from appearing on terminal J of ZB116D, which will keep one-shot ZB112 from being primed; no punch sample can be produced while the STOP button is pressed.

PUNCH TEST (Figure 24)

7.91 When the PUNCH TEST switch SWB601 is placed in the TEST position, the receiver will be placed in the punch test mode. The receiver will be placed in the non-EDC mode (see 7.89 and 7.90) and all incoming data will be punched. Each character is stored and compared to what was punched. When the two do not agree, a punch test alarm (PTA) results and the receiver stops.

7.92 In the punch test mode, ground will be applied to terminal 17 of SWB601 which will place the receiver in the non-EDC mode. As in the EDC mode, the programmer will be locked in the SR mode, reverse channel will be held on, the pad out circuit will be inhibited, the BN circuit will be disabled, and a constant BK signal will be generated. However, the 0 volts output from terminal 67 of SWB601 will be removed so there will be no feed alarm inhibit and the terminal will be able to detect feed errors. The punch test switch will take the output of terminal H of ZB412D (the 80 elements of the counter) and will send it back to ring reset ZB409A on terminal R so that the tens counter will be reset to the 00 state. Thus, the character counter will be continually running and a character count can be made in case of an error.

7.93 Switch SWB601 removes ground from terminal 2 on ZB205C enabling the punch test alarm register and applies the inverted output to the set B enable. Set B enable is then applied to terminal D of AND gate ZB418C, so that the first delayed clock will be enabled to produce the set B pulse. The punch test storage set pulse is derived from the two millisecond output pulse of one shot ZB510. This two millisecond pulse is applied to input terminal H of pulse amplifier ZB425B. On the negative transition of this pulse, a ten microsecond positive-going pulse will appear on output terminal B of ZB425B, producing the punch test storage set, occurring two milliseconds after the first delayed clock. With the PUNCH TEST switch in the TEST position, punch test storage set pulse will be applied to the 1A terminals of the 8 flip-flops of the horizontal check character register (punch test second storage).

7.94 The punch test second storage will be reset to the 0 state when the terminal is switched into the punch test mode. A positive-going transition appearing on terminal 5 SWB601 will reset the register and is called the storage reset. It is applied to the 0A inputs of the punch test press second storage since the P0A terminals are permanently primed. All the flip-flops will be set to the 0 state.

7.95 The first gated levels will still be applied to the 1B and 0B input terminals of the 8 flip-flops of the punch test second storage. The spiral shift pulse is now called the sample local test pulse. The incoming RD sample pulse is called the punch test first storage reset, being applied to input terminal E of power pulser ZB109. This will reset the punch test first storage. The incoming data levels which go to the emitter inputs of inhibit gate ZB209 with each set B pulse, the data appears on the

outputs of ZB209 being called the test levels. The test levels then appear on the emitter input terminals of inhibit gates ZB103 and ZB104 are passed because these gates are enabled, and the second gated levels are produced.

7.96 The second gated levels are then applied to the 0B and 1B inputs of the punch test first storage flip-flops. Each level with a mark will set that flip-flop to the 1 state. The outputs of the punch test first storage are called test primes and are applied to the P1A inputs of the 8 flip-flops of the punch test second storage. The punch test storage set pulse will set those flip-flops of the punch test second storage to the 1 state that have been primed by the test primes (ie, those data levels that are marking).

7.97 When the tape has been punched and moved, the photo verifier output will then appear on inputs 1B and 0B of the punch test second storage. If the incoming character has been punched accurately, the punch test second storage will be reset to the 0 state. If the character has not been punched accurately, one of the levels of the punch test second storage will come up in the 1 state so a 0 volts output will appear on the normal output terminal of that level which will pass through OR gate ZB210C. The resulting 0 volts output on terminal 9 of ZB210C is called the punch test readout. 0 volts dc will appear on punch test readout when a character has not been punched correctly. This 0 volts signal is applied to the P1A input of the punch test alarm control flip-flop, terminal 9 of ZB205C. The sample local test pulse will now come in on the 1A input of the punch test alarm register (terminal 8 of ZB205C) and will set it to the 1 state indicating the alarm condition. Terminal 1 of ZB205C will go to 0 volts dc indicating the alarm and generating the punch test stop signal. It is also applied to input terminal H of OR gate ZB424A to produce the alarm output and the stop and reset condition. Set B enable will be removed (terminal 2 of ZB205C going to -6 volts dc). Punch test stop will also appear on input terminal H of OR gate ZB422A. This will keep the output of OR gate ZB422A, terminal B, at 0 volts which will prevent the gated clock from being produced. No punch commands will be produced so the terminal will be stopped immediately on the character of which a punch error has occurred.

7.98 The punch test second storage is reset to the 0 state only when a correct character has been received. After a punch test alarm has occurred, the punch test second storage can be reset only by returning the PUNCH TEST switch to the NORMAL position and then back to the TEST position.

LETTERS DRIVE

7.99 When the ALL FEED button is pushed to drive all levels of the punch, the letters drive signal is produced in the HSEDC receiver control module. The feed drive signals from the punch driver appear on terminal A7 of connector JB128 and are applied to input N of OR gate ZB423D. This gate produces punch sample pulses to drive the feed alarm circuit. Inverted punch sample pulses are applied to input N of inhibit gate ZB116A. When the ALL FEED button is pressed, ground is applied to terminal E1 of connector JB128 and to input D of inhibit gate ZB116A. For each negative pulse on pin N of ZB116A, there will be a positive output pulse on pin K of ZB116A. These positive pulses represent the letters drive signal which appears on terminal E2 of connector JB128 and is sent to the punch driver to drive the 8 punch levels.

8. RECEIVER STATION CONTROL

GENERAL

8.01 The receiver station control contains five relays, one flasher, and one circuit card. See Figure 25. The schematic diagrams, contained in another section, are:

7406WD - Receiver station control module
7070WD - TP302790 controls assembly

8.02 Refer to the above diagrams when using the following circuit descriptions.

AC POWER DISTRIBUTION

8.03 The ac power comes into the station control assembly on the ac cord supplied. The hot side of the line goes through fuse FH1 which fuses the line at 10 amperes, and goes to terminal 17 on connector JH3. From terminal 17, one lead takes the ac power signal to the POWER ON/OFF switch, SW11. The other side of this switch is returned to terminal 19 on JH3, and connected to terminal 2 on the ac relay. The other side of the ac relay, terminal 7, is connected to the other side of the line. When the switch is pushed to turn power on, two sets of controls from the ac relay send switched ac power to the station control on two leads and to

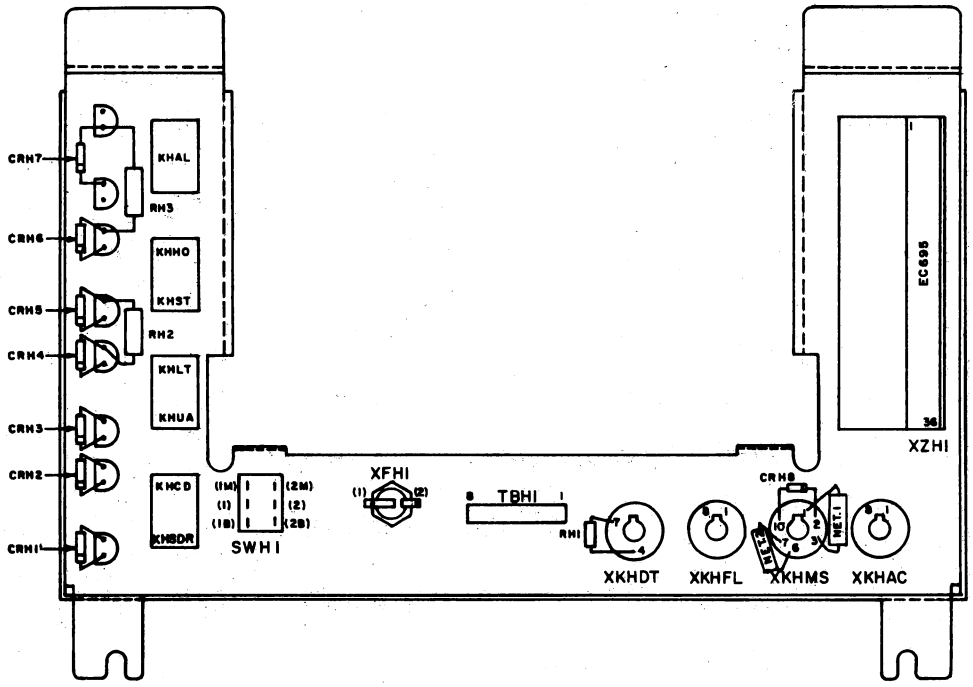


Figure 25 - Receiver Station Control, Module H

terminals 1 and 2 on JH3. The common side of the AC line is not fused.

8.04 The switched ac power is also sent through to the MS (motor start) relay contacts to be distributed to the receiver's motors.

8.05 When ac power comes to the receiving distributor module, it will energize the power supplies in the module to produce dc power. The station control assembly uses +6 volts, -6 volts, -12 volts, -55 volts, signal ground and circuit ground. These voltages come into the station control on pins 44, 45, 46, 47, 42, and 43 respectively of connector JH4. From the station control, -55 volts, signal ground and circuit ground are sent to the controls assembly on pins 15, 22, and 23 of connector JA3.

8.06 When the power ON/OFF switch is pushed ON and circuit ground is established, the ground signal, through pin 12 of connector J1,

will cause the indicator in the POWER switch, DS11, to light.

DATA SET INTERFACE LOGIC

8.07 The station control assembly provides an interface for the data set. The signals to and from the data set are EIA standard interface signals. The station control converts the EIA signals to system neutral signals and it converts system neutral signals to EIA signals. The following table applies to the EIA signals:

Data-Binary State:	One	Zero
Data-Signal Condition:	Marking	Spacing
Paper Tape:	Hole	No Hole
Voltage:	Negative (-3V to -25V)	Positive (+3V to +25V)
Control Function:	Off	On

8.08 In order for the data set to be able to enter the data mode, the DTR (data terminal ready) lead must be on. This lead is normally held on by the output of polar-to-polar amplifier Z1H whose input is held off by the RI (ring indicator) lead. The RI lead comes in on pin 9 of connector JH4 and goes to pin 32 of Z1H. A negative voltage on this lead (-6 volts) will produce a positive voltage (+6 volts) at the output, pin 31, which goes to pin 7 of JH4 to hold the DTR lead on.

8.09 When a call is made at the receiver terminal, the data set will enter the data mode when the operator pushes the DATA button on the data set. If a call comes into the receiver terminal, however, the RI lead will go positive during the ringing cycle, causing the DTR lead to go negative and since the data set will only enter the data mode during the ringing cycle, the data set will never answer. This requires the operator to manually answer the call and manually cause the data set to go to the data mode by pushing the DATA button. Since ringing stops when the call is answered, the DTR lead will be on and the data set will enter the data mode.

8.10 When the data set enters the data mode, the DSR (data set ready) lead will come on (+6 volts). This signal comes in pin 2 of connector JH4 to the input, pin 34, of relay driver Z1G which will send a 0 volt signal to the DSR relay to operate the relay. Diode CR1 across the DSR relay coil is used to prevent voltage spikes when the relay is de-energized. When the DSR relay is not energized, break contact 2 holds a ground signal on pin 5 of OR gate Z1D which blinds the punch by presenting 0 volts to pin 16 of JH4, the punch blind lead.

8.11 The polar receive clock signal comes into the station control on terminal 5 of connector JH4, goes to pin 19 of P/N amplifier Z1B which converts the signal to a neutral signal and sends it from pin 12 of Z1B to terminal 15 of connector JH4. The receive clock signal is used for timing in the terminal.

8.12 The polar receive data signals come into the station control on terminal 1 of connector JH4, goes to pin 18 of P/N converter Z1A which converts the data to a neutral signal, appearing on pin 7 of Z1A and terminal 11 of connector J2. This neutral receive data signal then goes to the receiving distributor for deserializing.

CARRIER DETECT

8.13 The polar carrier detect signal comes into the station control on terminal 3 of connector JH4, goes to pin 20 of P/N connector Z1C which converts it to a neutral signal and sends it from pin 17 of Z1C to pin 4 of OR gate Z1D. The neutral carrier detect signal also goes to pin 6 of relay driver Z1F.

8.14 Relay driver Z1F is used to drive the CD (carrier detect) relay. When the CD relay is de-energized, it means carrier is on and when it is energized, it means carrier is off. Pin 10 of Z1F primes the relay driver to enable it to pull in the CD relay. It requires a 0 volt signal which is obtained through a contact to ground when the DSR (data set ready) relay is energized. When the DSR relay is energized and carrier detect is present, the CD relay will be de-energized. Diode CR2 is used to prevent voltage spikes when the CD relay de-energizes.

8.15 When carrier is lost, it is an indication that the remote sender has stopped transmission. Therefore, normally closed contact 12 of the CD relay is used to control the SENDER STOPPED indicating light. With no carrier present, the CD relay will be de-energized and contact 12 of CD relay will be closed to ground, presenting this ground to terminal 13 of connector JH3 which illuminates the SENDER

STOPPED indicating light. When carrier is present, the CD relay will be de-energized and the SENDER STOPPED light will be turned off.

REVERSE CHANNEL CONTROL

8.16 Reverse channel is used for the receiver to communicate with the remote sender. Reverse channel will be sent by the data set if terminal 4 of connector J2 is held at +6 volts dc. Reverse channel will not be sent if terminal 4 is at -6 volt dc.

8.17 For reverse channel to be turned on all of the inputs of OR gate Z1J must be at -6 volts dc. If any input is at 0 volts dc the output on terminal 22 will be converted to -6 volts dc in N/P converter and terminal 4 of connector JH4 will be held at -6 volts dc, holding reverse channel off. With all inputs of OR gate Z1J at -6 volts dc, the output on terminal 22 will be at -6 volts, will be converted to +6 volts dc and will appear on terminal 4 of JH4 to hold reverse channel on.

8.18 With a stop or alarm condition at the receiver, the ST or HO relays will be energized and contact 4 of ST relay or contact 10 of HO relay will be closed to ground, holding input pin 27 of OR gate Z1J at 0 volts dc, holding reverse channel off.

8.19 With the ST and HO relays de-energized input pin 27 of OR gate Z1J will not be held at 0 volts dc and control of reverse channel is obtained from the EDC module. When the EDC module turns reverse channel on, it presents -6 volts dc to terminal 14 of connector J2 which goes to input pin 16 of OR gate Z1J to hold reverse channel on. To turn reverse channel off the EDC module presents 0 volts dc to this terminal and reverse channel will be held off.

8.20 Terminal 13 of connector JH4 is provided for external control of reverse channel by a receiver accessory.

8.21 Input pin 13 of OR gate Z1J will also hold reverse channel off when the output of OR gate Z1D is at 0 volts dc. This is the case when the data set ready signal is off or when carrier is lost and the TEST OPERATE switch SW1 is in the OPERATE position.

CONTROL LOGIC

A. Alarm Relay

8.22 The EDC module has three possible alarm conditions: feed alarm, back up alarm, and punch test alarm. If any of these alarms occurs, a circuit to ground occurs on terminal 17 of connector JH4. This goes to the 2L pin of the alarm (AL) relay. The 1U pin of the AL relay goes to -55 volts so the relay will be energized.

8.23 Diode CR7 across the coil of the AL relay prevents noise spikes when the relay is de-energized.

B. Low Tape Relay

8.24 The station control LT relay is used to recognize the low tape condition. It is driven by the low tape contact of the tape supply in the receiver. The contact to ground from the low tape switch comes into the station control on terminal 3 of J1 and goes to the LT relay. If there is sufficient tape, the low tape contact will be open and the LT relay will be in the de-energized state. If low tape exists, the low tape contact will be closed to ground and the LT relay will be pulled in. Contact 11 of LT relay closes to ground, latching LT relay in the energized position. This is done because the low tape switch can open and close many times after its first closure so the LT relay will be latched after the first closure. A subsequent alarm caused by installing a new roll of tape will open contact 9 of the AL relay, removing the latch to the LT relay. Diode CR4 prevents noise spike from appearing across the LT relay coil.

C. Low Tape Indicator

8.25 When a low tape condition occurs, contact 12 of the LT relay closes, allowing current to flow through the heating element of the flasher (FL). After a short delay (about 5 seconds), the flasher energizes, opening FL contact 5 to 7. This removes the ground from the FL heater, allowing it to cool off to reclose the circuit. The FL contact is in series with the POWER/LOW TAPE indicating light (terminal 12 of connector JH3) so it will flash on and off when a low tape condition exists.

D. Stop and Hold Relays

8.26 Two relays in the station control assembly, ST (stop) and HO (hold), are provided to stop and alarm the terminal. They are controlled by the STOP-ALARM/RESET button and by a contact from the LT relay. If the relays are de-energized, they will be pulled in when the STOP-ALARM/RESET button is pushed or when an alarm occurs. If they are automatically pulled in by the AL relay, the alarm must be corrected before the ST and HO relays can be reset. To reset the relays, the STOP-ALARM/RESET button must be reset. When the STOP-ALARM/RESET button is pushed or when an alarm occurs, the ST relay will be pulled in which will cause the HO relay to pull in. When they are reset, the ST relay will drop out which will cause the HO relay to drop out.

8.27 The 55-volt bias supply for the ST relay goes through resistor R2 to pin 2L of the ST relay coil. The 55 volt bias supply for the HO relay goes through resistor R3 to pin 2U of the HO relay. The opposite sides of the ST and HO relay coils, 1L and 1U respectively, are connected together and are also connected to a make contact to ground, 6 of the AL relay in parallel with a series combination of make contact 5 of the ST relay and make contact 5 of the DSR relay to ground. A make contact to ground from the STOP-ALARM/RESET button comes into the station control on terminal 7 of connector JH3 and goes through transfer contacts 8 of the HO relay to the 2L and 2U sides of the ST and HO relay coils respectively.

8.28 With no call in progress, the DSR relay will not be pulled in, make contact 5 of that relay will always be open and the ST and DSR contact combination will have no effect on the ST and HO relays. If the STOP-ALARM/RESET button is pushed, a ground signal will momentarily drive pin 2U of the HO relay to ground and this signal, through the HO relay to pin 1L of the ST relay, will pull in the ST relay. However, nothing will hold pin 1L at ground if the STOP-ALARM/RESET button is released and the ST relay will drop out. If the AL relay pulls in, however, make contact 6 of the AL relay will drive pin 1L and pin 1U to ground and both the ST relay and the HO relay will pull in. When the LT relay drops out, it will cause the ST and HO relays to drop out.

8.29 With a call in progress, the DSR relay will be pulled in and make contact 5 from the DSR relay will close to ground. Now, when the STOP-ALARM/RESET button is pushed and the ST relay pulls in, a ground signal from the DSR-ST contact combination will hold ST relay energized even when the button is released. This will also cause the HO relay to pull in. When the HO relay pulls in, transfer contacts 8 from the HO relay will now allow the signal from the STOP-ALARM/RESET button to go to pin 2L of the ST relay. When the RESET button is now pushed, pin 2L of the ST relay will go to ground and the ST relay will drop out. This will open make contact 5 of the ST relay and remove the ground signal from pin 1U of the HO relay. When the RESET button is released, the HO relay will drop out and transfer contacts 8 from the HO relay will switch back and allow the next signal from the STOP-ALARM/RESET button to go to pin 2U of the HO relay. If the relays are energized when the call is dropped, the ST and HO relays will also drop out.

8.30 If the AL relay pulls in at any time, it will cause the ST and HO relays to pull in. They will remain energized even if the AL relay drops out. The STOP-ALARM/RESET button must be reset to drop out the ST and HO relays when a call is in progress.

8.31 Make contact 1 of the ST relay and make contact 12 of the HO relay are connected to terminal 14 of the connector JH3. When either the ST relay on the HO relay or both are energized, a ground signal is applied to lamp DS13 in the STOP-ALARM/RESET button to indicate the alarm.

8.32 Diode CR7 across the HO relay coil and diode CR7 across the ST relay coil are used to prevent voltage spikes when the relays drop out.

E. Motor Start Relay

8.33 Ac power is supplied to the punch motors and the photo verifier lamp through a contact on the motor start (MS) relay. Switched ac power will be presented to the motor when the MS relay is energized and contacts 1 to 3 and 6 to 7 close. The MS relay will be energized when the data set ready relay is energized by a contact to ground through contact 1 of the DSR relay.

8.34 If DSR is not ON the motors and light can be turned ON by pressing the AUX MOTOR START pushbutton. This will present a ground on terminal 3 of connector JH3 which will energize the MS relay.

8.35 Diode CR8 across the coil of the MS relay prevents noise spikes when the relay de-energizes.

8.36 Pressing the AUX MOTOR START button closes a circuit to ground which illuminates the AUX MOTOR START indicating lamp. If the receiver is in the manual mode, indicated by the MANUAL indicator lamp being on, pressing the AUX MOTOR START button will open a contact which will turn the MANUAL indicator lamp off.

FEATURES AND ACCESSORIES

A. General

8.37 Switch SW6 on the controls assembly selects the non-EDC operation for the receiver terminal. When the NON-EDC button is pushed, a contact is closed to ground on the switch. The 0 volt signal comes into the station control assembly on terminal 1 of connector JH3 and goes to terminal 21 of connector JH4 which sends it to the EDC module to put the receiver in the non-EDC mode. When the NON-EDC button is pushed, a second contact on the switch will also close to ground and cause the NON-EDC indicator lamp, DS6, to light.

8.38 Switch SW1, TEST/OPERATE is provided on the station control assembly to operate the unit when the receiver is not connected to a data set. When the switch is thrown to the TEST position a ground signal is applied to the DSR relay coil to operate the DSR relay. Also the switch opens the input to pin 4 of OR gate Z1D so that the carrier detect has no effect on the punch blind.

8.39 When blank tape is desired from the punch, the BLANK FEED switch SW2 is pressed. This provides a contact to ground on terminal 4 of connector JH3. This signal is fed to OR gate Z1L; output is on pin 36 and will be inhibited if the motors are not on by make contact 9 to 11 of the MS relay. When the MS relay is energized, the ground signal will appear on terminal 22 of connector J2 from where it goes to the punch driver to feed out blank tape.

8.40 When all-marking tape is desired, as when checking the operation of the 8-punch levels, the ALL FEED switch, SW1, is pressed. This provides a contact to ground on terminal 6 of connector JH3 and is strapped on to terminal 24 of connector JH4 for use by the punch driver and the HSEDC receiver control module to produce an all-marking tape. It is also fed to pin 30 of OR gate Z1L; output is on pin 36.

8.41 Spare contacts from the DSR, CD, US, ST, HO, AL, and LT relays are available on connector JH4 for external use.

B. Unattended Answering

8.42 There are two types of unattended answering. Option A1 provides unattended answering under control of the UNATTND button on the controls assembly. Option A2 provides unattended answering only when the UNATTND button is pushed and no low tape or alarm condition exists. The options are programmed on terminal board TB1 using TP306087 terminal jumpers.

8.43 When option A1 is chosen, terminals 1 and 2 of TB1 are connected together and terminals 3 and 4 of TB1 are connected together. When the UNATTND button is pushed, a 0-volt signal goes through a break contact on the AUX. MOTOR START switch and passes through a make contact on the UNATTND switch to terminal 2 of connector JH3. From terminal 2 of J1, the signal goes to the coil of the UA relay to energize the relay. The strap between terminals 3 and 4 of terminal board TB1 provides a 0-volt signal which passes through terminal 11 of connector JH3 to the UNATTND button indicator (DS5) and causes it to light. The MANUAL button indicator (DS4) goes off when the UNATTND button is pushed. If the AUX. MOTOR START button is pushed, the 0-volt signal to the UA relay is inhibited and the UA relay is not pulled in. However, both the non-EDC mode and the unattended mode can be chosen simultaneously.

8.44 When the UA relay pulls in, break contact 3 of that relay opens and inhibits the ring indicator signal from coming in and turning off the data-terminal-ready signal. Thus, if a call comes into the receiver terminal, the data-terminal-ready signal is on and the call is answered automatically. The call is dropped when the distant terminal disconnects.

8.45 If option A2 is chosen for unattended answering, terminals 1 and 2 of TB1 are still strapped together to allow the UA relay to pull in when the UNATTND button is pushed.

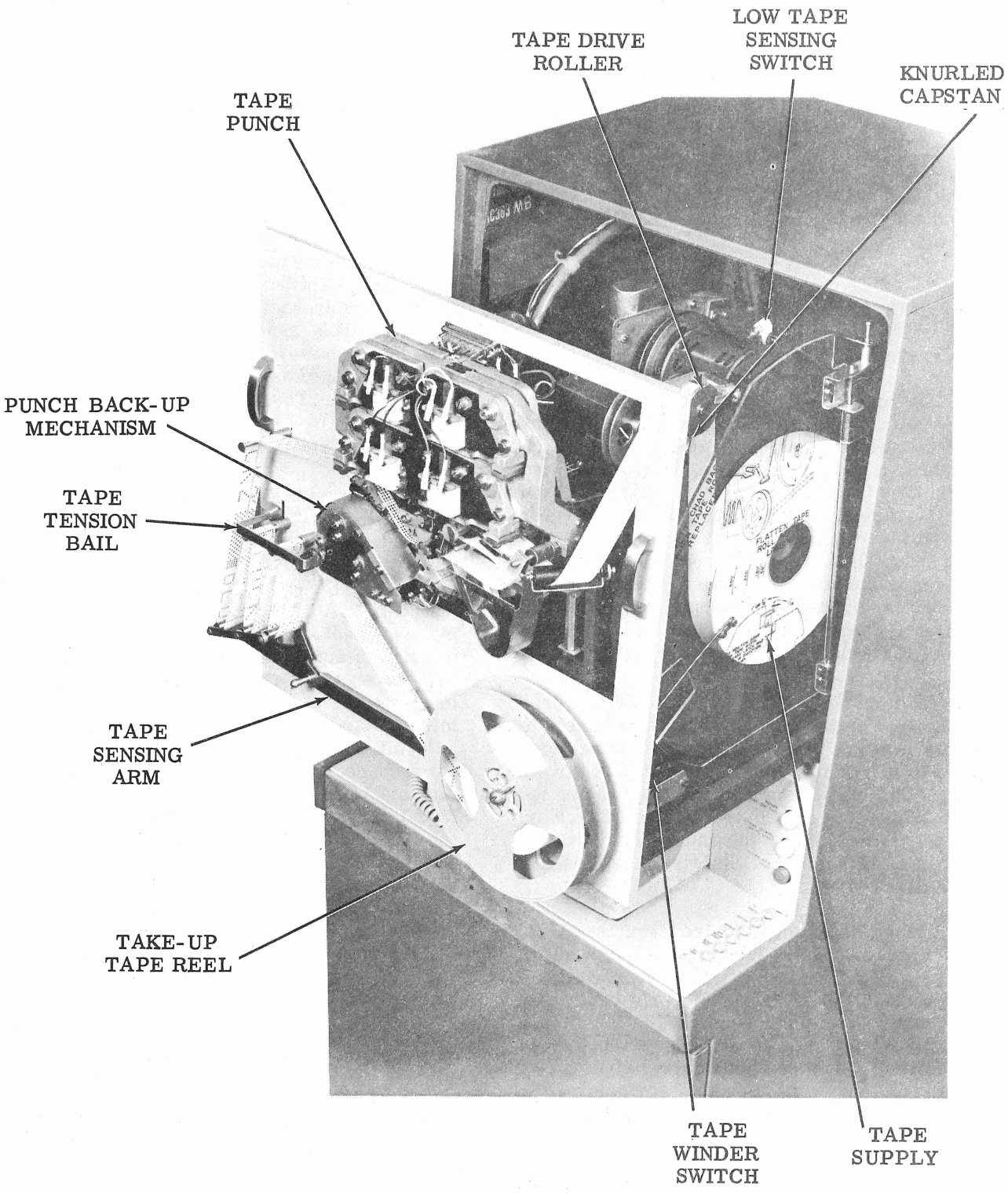


Figure 26 - Punch and Tape Transport Assembly, Right Side View

The strap between terminals 3 and 4 of TB1 is removed and a strap is placed between terminals 4 and 5. This allows the 0-volt signal, which causes the UNATTND indicator to light, to pass through only if the low-tape condition does not exist and the LT relay is not pulled in. If the low-tape condition exists, the UNATTND and FLASH-LOW TAPE indicators both flash. A third jumper is provided with the A2 option which ties terminals 6 and 7 of TB1 together. Break contact 3 of the UA relay inhibits the ring indicator signal, but an alternate path is provided through make contact 9 of the LT relay if the low-tape condition exists and through make contact 5 of the AL relay if an alarm condition exists. Thus, with either condition, the ring indicator signal turns off the data-terminal-ready signal to prevent the receiver from answering automatically. If the low-tape condition does not exist, incoming calls are answered automatically.

C. Disconnect

8.46 The disconnect feature allows an unattended receiver to drop a call if carrier is lost for a time longer than 60 seconds. The disconnect (DT) relay is supplied with -55 volts on pin 3. Pin 2 of the relay, the other side of the heater, goes to ground if the receiver is unattended (contact 5 of UA relay closed) and there is a loss of carrier (contact 8 of CD relay closed). This allows the thermal element of the DT relay to heat. If the conditions persist for 50 seconds, the DT relay energizes and the call is disconnected. This is accomplished by DT relay contacts 5 to 7 closing which presents -6 volts to the DTR terminal. With DTR off, the call is then dropped.

8.47 Disconnect can also be initiated by an accessory by applying ground to terminal 18 of connector JH4.

D. Discrete Calling Generator Accessory

8.48 When equipped with the discrete calling generator accessory, the receiver can call unattended type 4 senders equipped with the discrete calling recognizer accessory. This generator will send out a code which must be recognized by the protected sender before it will send its data.

E. Send/Receive Accessory

8.49 Provision is made in the station control assembly to accept the send/receive cable (TP308514).

9. PUNCH AND TAPE TRANSPORT ASSEMBLY

DESCRIPTION

9.01 The punch and tape transport assembly consists of a tape punch (with back-up mechanism), a light source, and a tape transport assembly which includes the tape supply mechanisms. See Figures 26 and 27.

9.02 The assembly installs in the top section of the receiver cabinet (see Figure 1).

9.03 Refer to the appropriate section for a description of the tape punch and the photoelectric reader.

TAPE HANDLING FACILITIES

A. Tape Supply (Figure 28)

9.04 A fresh 3000 foot roll of tape is placed in the supply container located behind the front panel. The tape roll is placed on the fixed spindle of the container so as to unwind in a clockwise direction. The tape is threaded over the tape drive roller and through the rollers on the punch. When the punch demands tape, the tape pulls the tape drive roller down to engage a continuously rotating capstan, thereby driving the system to feed tape; also, deflection of the drive system is permitted to minimize the shock due to the inertia of the tape supply roll. When a slack condition on the tape occurs, the drive roller is returned to its idle position preventing the system from feeding. The sequence occurs intermittently during punch operation.

B. Tape Winder (Figure 28)

9.05 The tape sensing arm, pivoted on the right lower corner of the front panel, is lifted and latched by the operator for tape threading. The tape arm, in turn, lifts the tension bail to present a clear path for tape entry. Tape coming from the punch is placed between the three posts, on the sensing arm, and the three posts mounted on the front panel, and then secured to the plastic tape reel. When the latch is lifted slightly, the tape sensing arm is released and drops down under its spring tension forming a triple loop of tape. When the punch feeds tape, the tape loops lengthen allowing the sensing arm to move down until a mercury switch (tape winder switch) operates completing

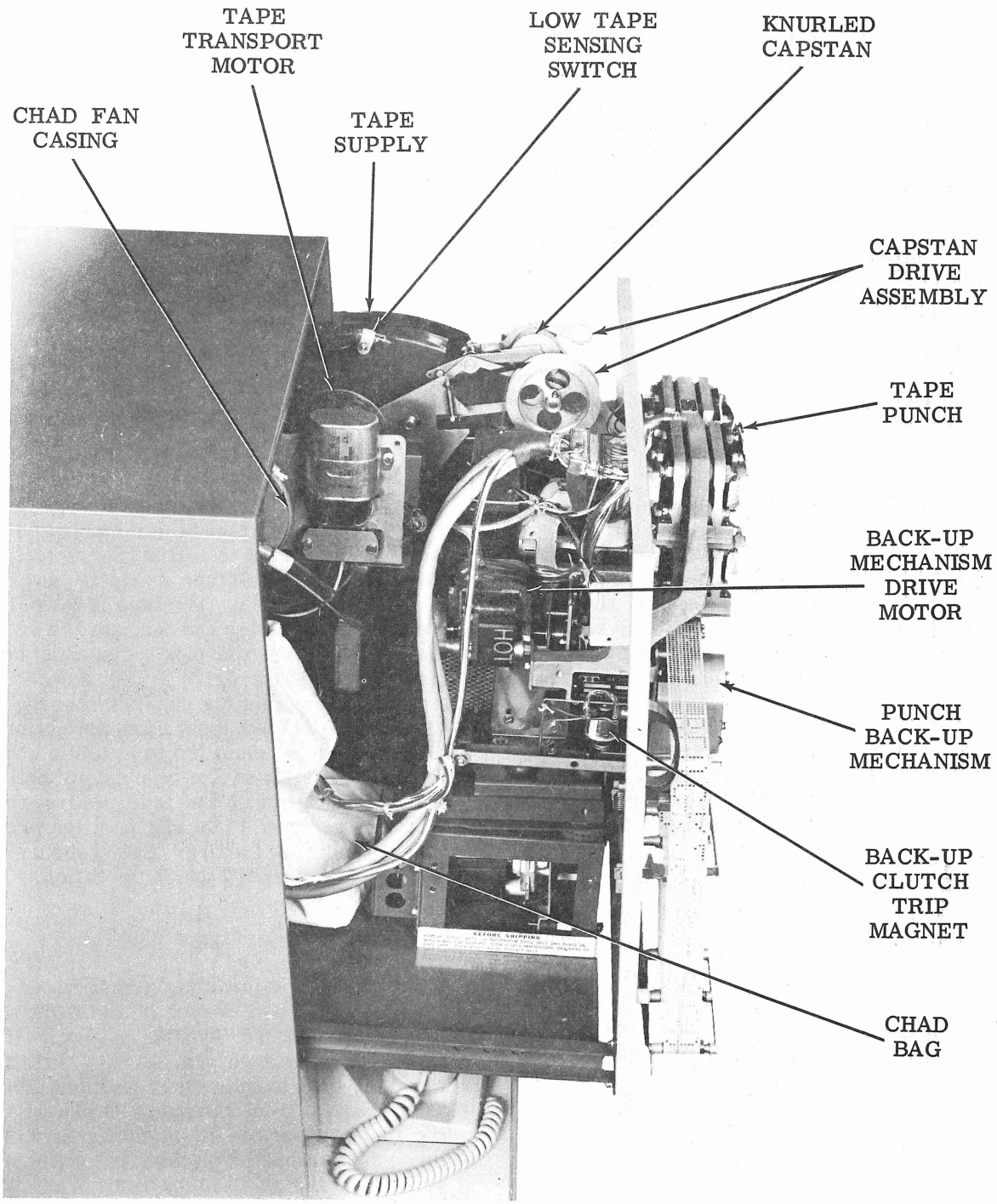


Figure 27 - Punch and Tape Transport Assembly, Left Side View

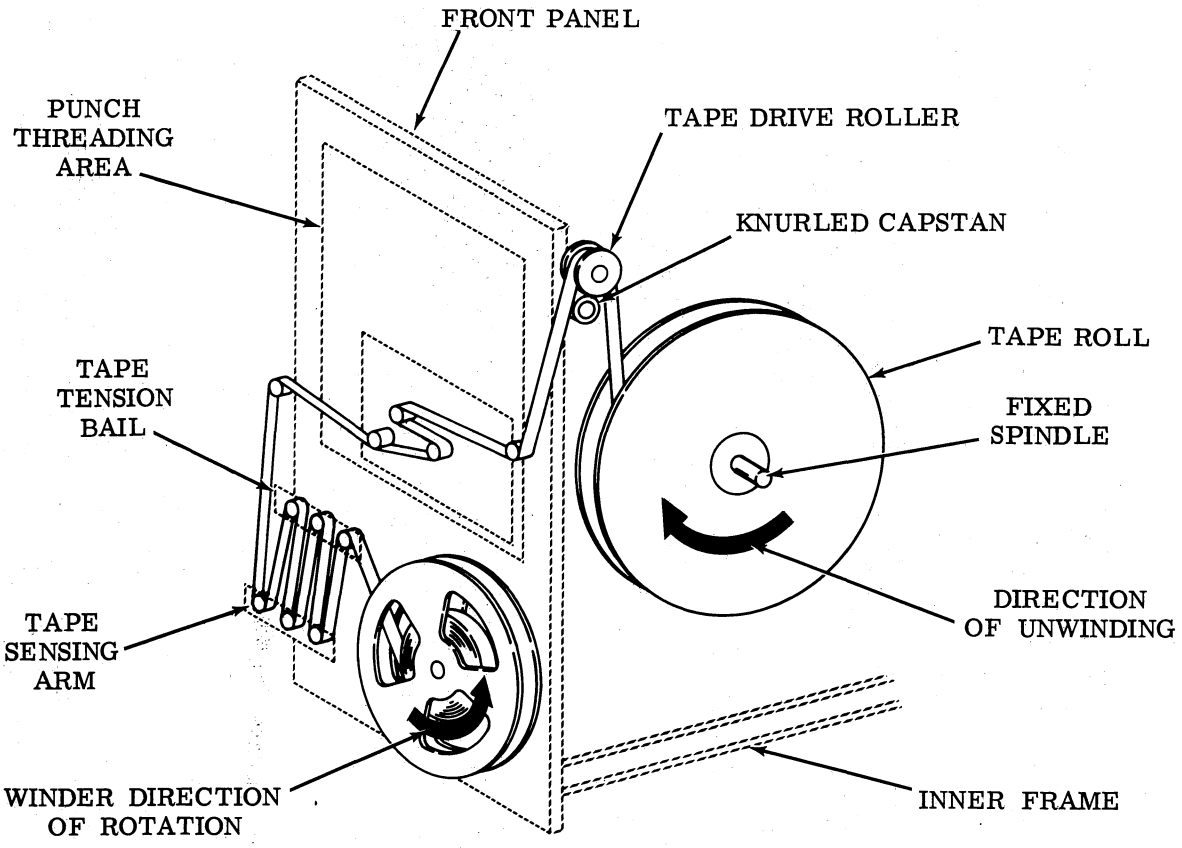


Figure 28 - Path of Tape

the circuit to a shaded pole motor. The winder hub, which is fastened to the motor shaft, accommodates the plastic reel. The motor runs until the tape sensing arm reaches a position such that the tape winder switch opens. The motor then coasts to a stop. When the tape loops enlarge again, the cycle is repeated.

CAUTION: WHEN THE LATCH IS RELEASED, THE TAPE ARM SHOULD BE LOWERED MANUALLY TO PREVENT BREAKING TAPE.

PUNCH BACK-UP MECHANISM

A. Description (Figures 29 and 30)

9.06 The punch back-up mechanism is an electrically-operated device used to retract 80 characters of tape so the punch can overpunch these characters and, in effect, erase them.

9.07 During normal operation of the punch, the forward feedwheel feeds tape to the left while punching occurs in the punch block. The tape passes through the tape guide assembly, without engaging the reverse feedwheel, and is wound on the tape winder.

9.08 When a command to back up is received, the tape guide assembly engages the tape with the reverse feedwheel and disengages the tape from the forward feedwheel. The tape is then fed backwards through the punch block.

9.09 Reverse feeding stops after 80 characters, and the punch feeding and perforating reverts to normal operation.

B. Operation

9.10 Normal Tape Feeding: While the punch is punching tape, the back-up mechanism is not functioning. The back-up mechanism

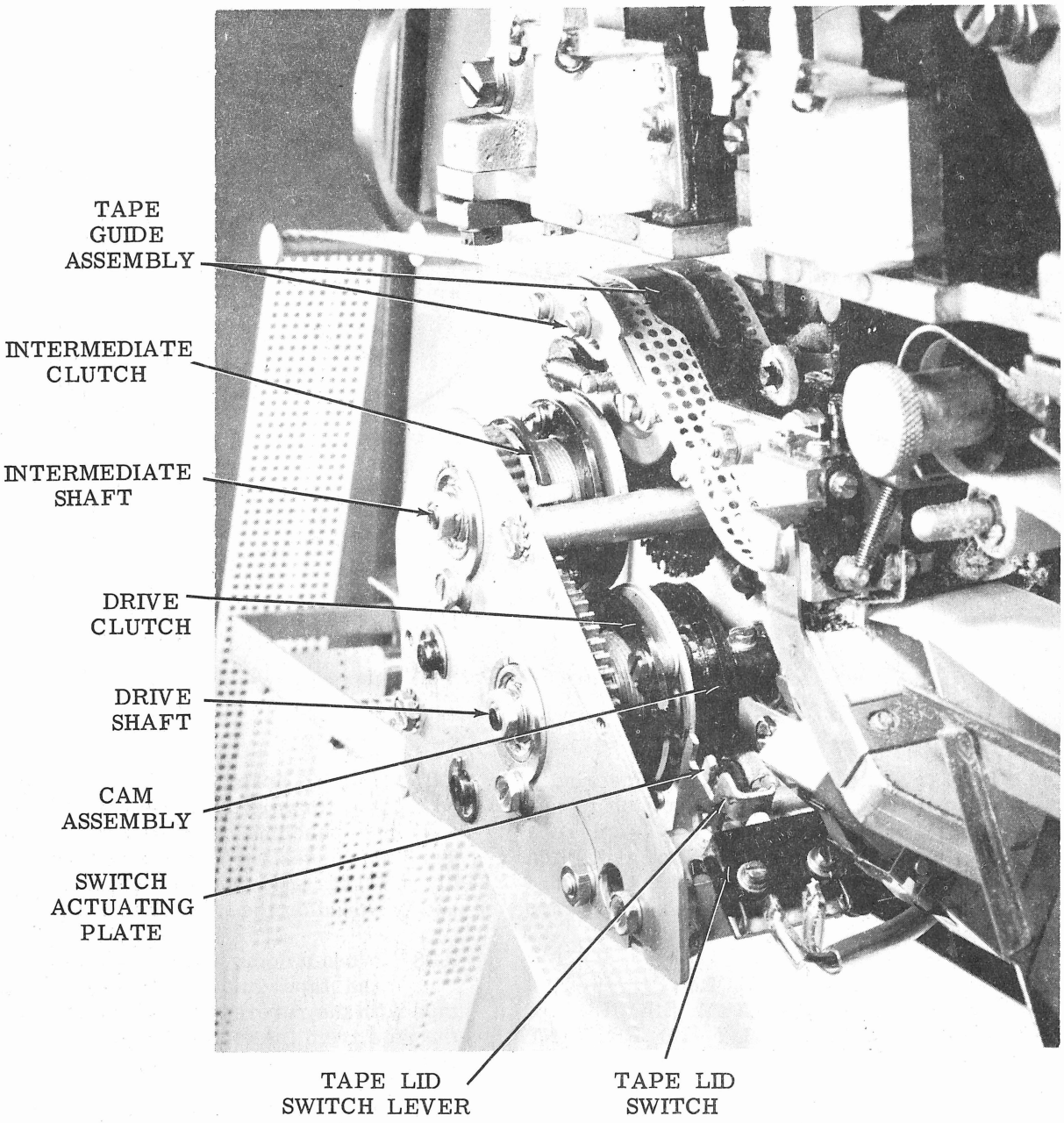


Figure 29 - Punch Back-Up Mechanism, Cover Removed, Right Side View

drive shaft is driven clockwise at about 118 revolutions per minute by a 105-rpm, shaded pole motor (Figure 27) through a timing belt. Since the spring clutches are disengaged, only the gear on the drive shaft and the mating gear or the intermediate shaft rotate. The intermediate shaft is rotating counterclockwise.

9.11 Tape Back Up: When a 6-volt dc, 70-ms pulse is supplied to the clutch trip magnet (Figure 30), the magnet armature is attracted to the core. The armature pulls on the lever attached to the clutch trip shaft causing it to rotate clockwise. The clutch stop lever is rotated away from the clutch disc lug allowing the clutch to engage.

9.12 Engagement of the drive clutch causes the cam assembly (Figure 29) to rotate with the drive shaft. Almost immediately, the tape guide cam follower arm starts to rotate counterclockwise.

9.13 A post on the arm allows the switch lever to be rotated clockwise by a spring. The lever actuates a snap-action switch (tape lid switch) which is wired for normally-closed operation. See Figure 29.

9.14 The follower arm also causes the center of the tape guide assembly to move down and to the left. The tape guide assembly has a torsion spring which tends to bias the assembly to a counterclockwise direction. The tape guide assembly has been resting on the right eccentric stud. As the center of the assembly moves downward to the left, the guide rotates counterclockwise until the left end of the assembly hits the left eccentric stud. At this time the tape in the guide is engaged by the reverse feedwheel. Now the tape is engaged with both feedwheels. Since the center of the assembly is still moving, the tape guide begins to rotate clockwise until the tape guide cam follower arm is on the high part of the cam assembly. At this point the tape is disengaged from the forward feedwheel.

9.15 As the cam assembly rotates further, the cam assembly roller strikes the clutch release lever causing the clutch trip shaft to rotate counterclockwise. The rotation of the clutch stop lever releases the intermediate shaft clutch allowing it to engage. The drum and gear assembly (Figure 30) begins to rotate counterclockwise. The gear causes the reverse feedwheel assembly to rotate clockwise. Rotation of the detent disc (Figure 30) on the reverse feedwheel assembly causes the detent lever to be cammed out to the disc's periphery. The gear ratio between the intermediate shaft and the reverse feedwheel assembly is 2 to 1, so the feedwheel assembly will rotate twice to each rotation of the intermediate shaft. As the detent cutout on the feedwheel detent disc is completing the first rotation, the cam of the drum and gear assembly holds the detent lever out away from disc until the detent cutout is passed. When the detent cutout approaches the second complete revolution, the detent lever is no longer held out by the drum and gear assembly cam. At this point the spring clutch of the intermediate shaft is stopped by its respective stop arm on the trip shaft, and the detent roller of the detent lever drops into the cutout on the detent disc. During rotation of the reverse feedwheel, the tape in the tape guide assembly was fed backwards. Since there are 40 teeth on the reverse feedwheel and it is rotated twice, 80 characters in the tape will have been fed back.

9.16 Shortly after the drum gear assembly is back to its original position, the tape lid cam follower arm starts to move down to the low part of the cam assembly. As it is doing this, a post on the follower arm causes the switch lever to rotate counterclockwise removing the lever away from the switch. At the same time the center of the tape guide assembly is moving upward to the right. The tape guide assembly rotates counterclockwise until its right hand side hits the right eccentric stud. At this point both feedwheels are again engaged with the tape. As the center point moves on the tape guide assembly, it begins to rotate clockwise moving the left end away from the left eccentric stud, thereby disengaging the tape from the reverse feedwheel. The cam follower arm stops rotating when the drive shaft cam completes its revolution and the spring clutch becomes disengaged. The back-up sequence is now complete.

10. RECEIVER CABINET (Figures 1, 2, and 3)

10.01 The receiver cabinet is 20-1/2 inches wide, 54-1/2 inches high, and 24-3/8 inches deep and weighs approximately 40 pounds. Housing facilities for a data set are provided. The lower section is enclosed by a flush mounting door held closed by a magnetic latch; this section is used to mount three electronic modules. The upper section contains mounting facilities for the punch and tape transport assembly. Access to the equipment from the rear is provided by a door which also contains two cooling fans.

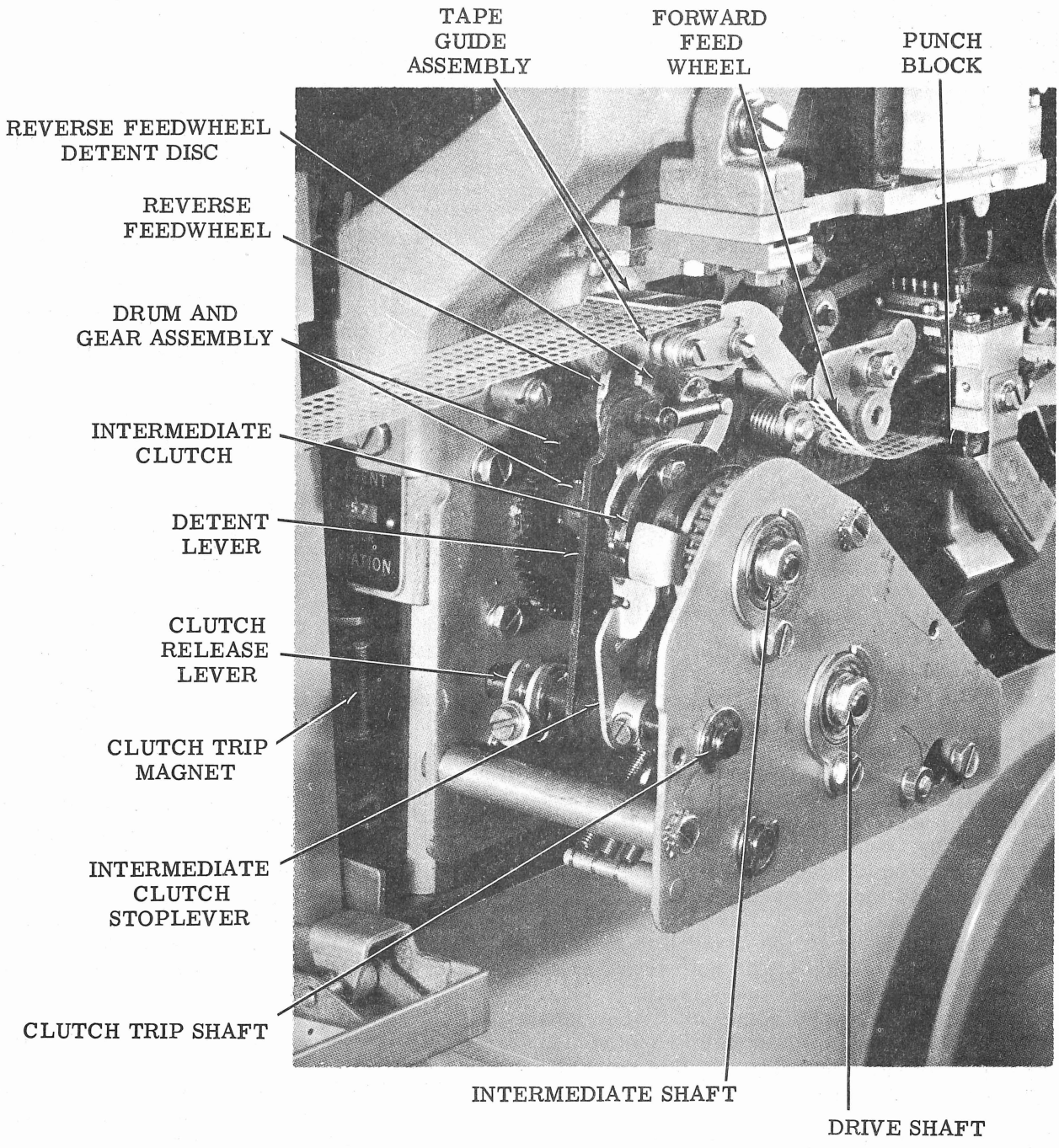


Figure 30 - Punch Back-Up Mechanism Cover Removed, Left Side View

10.02 The punch and tape transport assembly components are mounted on a slide-mounted panel which is 19-3/8 inches wide by 18 inches high.

10.03 The operating controls for the receiver are mounted to the right of the data set on a stationary panel in the center section of the cabinet. The U-shaped receiver station control module is mounted directly behind this panel.

10.04 Electrical connections for the receiver consist of cables extending from the wiring field in the center section of the cabinet through a slot in the rear of the cabinet base.