VERTICAL PARITY DETECTOR (TP308511)

FOR

FIVE TO SEVEN LEVEL OPERATION OF "DATASPEED"* TAPE RECEIVER 4B

CONTENTS PAGE

1. GENERAL

1.01 This section provides description, operation, and installation information for the vertical parity detector (TP308511) used with the Tape Receiver 4B.

1.02 The unit requires no lubrication or adjustment. For maintenance information, refer to the section covering the Tape Receiver 4B trouble shooting.

2. DESCRIPTION

2.01 The vertical parity detector provides for checking the vertical parity of incoming data and for indicating each parity error at the tape receiver, at speeds up to 1200 wpm. The unit is contained on two electronic circuit cards: parity logic card EC680 and parity error indicator EC681. The unit may be installed in either the factory or the field.

2.02 Vertical parity is used for error detection purposes. Parity is accomplished by counting the number of marking bits in each character to determine whether a space or mark bit is to be inserted in the otherwise unused eighth level. Either of two forms may be used: odd parity or even parity. With odd parity, an odd number of marking bits for a character results in the insertion of a space bit in the eighth level of the character; if there is an even number of mark bits a mark is inserted. With even parity, an even number of marking bits results in the insertion of a space bit in the eighth level; if there is an odd number of mark bits a mark is inserted.

2.03 The input to the vertical parity detector consists of 8 levels of parallel data which represent the information to be punched on tape by the tape punch. The input signal to each level is 0 volts for a mark and -6 volts for a space.

2.04 The vertical parity output is 0 volts (parity error) or -6 volts (no parity error).

2.05 The schematic and logic diagrams for the unit (303680 and 303681) are included at the back of this section.

3. OPERATION

GENERAL

3.01 Since the operation of the vertical parity detector unit is related to tape receiver operation, refer to the appropriate section for a description of the various tape receiver modules. Refer also to these wiring diagrams:

(a) Tape Receiver 4B - 7040WD

(b) Receiver Distributor Module - 7412WD

(c) Receiver Control Module - 7063WD

(d) Vertical Parity Inserter - 303680, 303681

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Prepared for American Telephone and Telegraph Company by Teletype Corporation

3.02 When operating without error detection and correction (non EDC), the vertical parity unit provides an output for each parity error and an error character (customer selectable) can be inserted in the place of the wrong character.

3.03 To monitor and check vertical parity, the LEVEL SELECTOR switches on the receiver distributor module and on the receiver control module must be in the identical position. If the vertical parity information is to be included in the product tape, the LEVEL SELECTOR switches must be positioned as follows:

(a) Receiver Control Module - appropriate data level

(b) Receiver Distributor Module - 8 level position

3.04 Incoming serialized data is converted to parallel form by the shift register in the receiver distributor module. The normal outputs of the register, elements ZD204 through ZD207, are then applied to emitter followers ZD208. The output of emitter followers ZD208 are applied to terminals A1 through A8 of connector JD128 for distribution to the receiver control module for gating. The gated signals are then returned to the receiver distributor module for priming their respective punch levels.

3.05 At the same time the eight code levels are applied to the receiver control module, these signals are also applied to vertical parity logic card EC680 (ZD209). The output-input configuration is as follows:

	Output		Input	
Level	Flip-Flop	Pin	Element	Pin
1	ZD207	14	ZD209A	2
2	ZD207	1	ZD209A	3
3	ZD206	12	ZD209B	13
4	ZD206	14	ZD209B	14
5	ZD206	1	ZD209C	23
6	ZD205	12	ZD209C	24
7	ZD205	14	ZD209D	34
8	ZD205	1	ZD209D	35

The output (pin 17) of ZD209G is -6 volts if levels 1 through 8 contain an even number of marking bits or 0 volts for an odd number of marking bits.

3.06 The indication of parity error is accomplished by parity error indicator card EC681 (ZD210) in conjunction with PARITY SELECTOR switch SWD2.

ODD PARITY

3.07 With the PARITY SELECTOR switch in the ODD position, the 0 volt condition is removed from pin 11 of OR gate ZD210B to enable the parity error indicator to be controlled by the parity logic and the inverted punch sample pulse. Pin 11 of ZD210B is an open-circuit at this time and pin 3 of exclusive OR ZD210A is held at a constant -6 volts. If output pin 17 of ZD209 is 0 volts, indicating odd parity (odd number of marking bits), then the output of ZD210A is held at 0 volts. When the inverted punch sample pulse (a 0 to -6 volt, .953 millisecond pulse) appears at pin 5 of OR gate ZD210B, the output of OR gate ZD210B is still held at 0 volts and flip-flop ZD210D is held in the 0 state. The output (pin 9) of emitter follower ZD210E is held at -6 volts, indicating no parity error.

3.08 If output pin 17 of ZD209G is -6 volts, indicating even parity (even number of marking bits), then the output of exclusive OR ZD210A is held at -6 volts. When the inverted punch sample pulse appears at pin 5 of OR gate ZD210B, the output of OR gate ZD210B is changed to -6 volts. After a delay of 15 microseconds through ZD210C, the output of ZD210C is set to 0 volts. This positive transition of -6 volts to 0 volts is then applied to the set 1A point on flip-flop ZD210D. Since the prime PIA is held at ground, the flip-flop sets to the 1 state and the output (pin 9) of emitter follower ZD210E is then held at 0 volts which indicates a parity error. This parity error signal is then applied to terminal E4 of connector JD128 of the receiver distributor module for insertion into the receiver control module for gating and setting the error flip-flop to indicate an error in transmission. At the end of the .953 millisecond inverted punch sample pulse, its positive transition (-6 volts to 0 volts) is again applied to pins 5 and 13 of ZD210. This signal inhibits further parity error sampling at pin 5. At pin 13, the signal is applied to the set 0A point of flip-flop ZD210D to reset the flip-flop to the 0 state and remove the parity error indication of 0 volts from pin 9 of ZD210.

EVEN PARITY

3.09 With the PARITY SELECTOR switch in the EVEN position, the 0-volt condition is removed from pin 11 of OR gate ZD210B to enable the parity error indicator to be controlled by the parity logic and the inverted punch sample pulse. Pin 11 of ZD210B at this time is an open-circuit and pin 3 of exclusive OR ZD210A is held

at ground. If the output pin 17 of ZD209 is -6 volts, indicating even parity (even number of marking bits), the output of ZD210A is held at 0 volts. When the inverted punch sample pulse (a 0 to -6-volt, 2-millisecond pulse) appears at pin 5 of OR gate ZD210B, the output of OR gate ZD210B is still held at 0 volts and flip-flop ZD210D is held in the 0 state. The output (pin 9) of emitter follower ZD210E is held at -6 volts, indicating no parity error.

3.10 If output pin 17 of ZD209G is 0 volts, indicating odd parity (odd number of marking bits), the output of exclusive OR ZD210A is held at -6 volts. When parity error is sampled with the inverted punch sample pulse, the error indication is passed to flip-flop ZD210D to set the flip-flop to the 1 state and give a parity error indication to terminal E4 of JD128 of the receiver distributor module. From terminal E4 of JD128, the signal is passed to the receiver control module for gating and setting the error flip-flop to indicate an error in transmission. At the end of the 0.953-millisecond inverted punch sample pulse, its positive transition (-6 volts to 0 volts) is again applied to pins 5 and 13 of ZD210. This signal inhibits further parity error sampling at pin 5. At pin 13, the signal is applied to the set 0A point of flip-flop ZD210D to reset it to the 0 state and remove the parity error indication of 0 volts from pin 9 of ZD210.

PARITY OFF

3.11 With PARITY SELECTOR switch SWD2 in the OFF position, 0 volts is constantly applied to pin 11 of ZD210 to inhibit any parity error indication.

3.12 While the incoming data is deserialized in the shift register, the inputs to parity logic card ZD209 will vary between 0 and -6 volts. Output pin 17 of ZD209 will also vary between 0 and -6 volts during this deserialization until the entire 10-bit code is contained in the register. At that time, output pin 17 of ZD209 will be either 0 or -6 volts.

3.13 While this shifting into the register is being done, an inverted punch sample signal of 0 volts is applied to pins 5 and 13 of ZD210 to inhibit any error indication due to register shifting and an unstable parity count.

VERTICAL PARITY ERROR REGISTER

3.14 If an error in vertical parity is detected and terminal E4 of JD128 in the receiver distributor module is held at 0 volts for one character length, then the error register in the receiver control module is set.

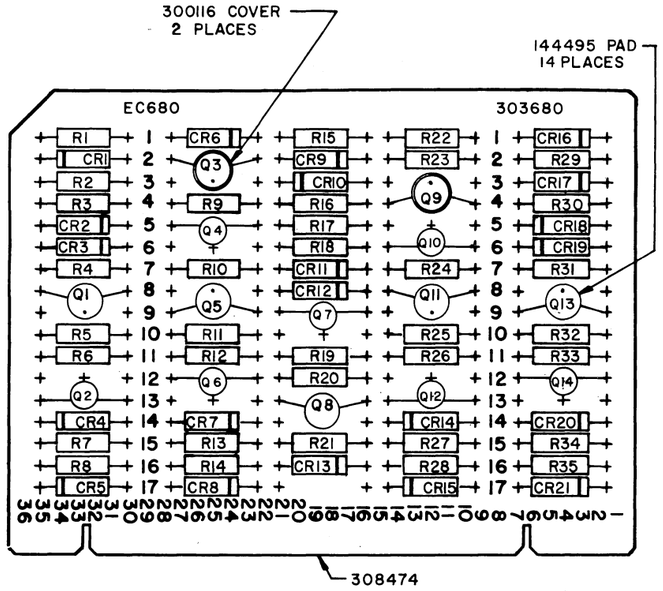
3.15 The 0 volts at terminal E4 of JD128 in the receiver distributor module is applied to terminal A10 of JB128 in the receiver control module and into the errored block control circuit. The input to pin 34 of inverter ZB222K is the punch sample pulse, a -6-volt to 0-volt, 2-millisecond pulse. The output (pin 32 of ZB222K) is applied to input pin E of inhibit gate ZB512D. The vertical parity error signal from terminal A10 of connector JB128 is applied to pin C of inhibit gate ZB512D. The output of this gate (pin J) is inserted into OR gate ZB419A for gating the set pulse for the error register. When an error is present on A10 of JB128 this 0-volt signal is applied to pin C of ZB512D. If this error is present when the punch sample pulse is applied to inverter ZB222K, -6 volts is applied to pin E of ZB512D. The output pin J of inhibit gate ZB512D then goes to 0 volts and this positive transition is gated to the set 1A terminal (terminal 34) to set the error register to the 1 state. Output pin 12 of ZB213A then informs the receiver control module of an error in transmission and to go into the error correction mode.

3.16 Every character that is received and deserialized by the receiver is checked for parity by the vertical parity detector. However, fixed characters, such as SR, BN, and EOB, cannot be passed during any preset parity check because the SR and BN's are both even parity and EOB is always odd parity. Also, check characters CK1 and CK2 cannot be parity controlled because they are determined by the incoming data. Therefore, even though these five fixed characters are checked for parity and may indicate parity error, they are not passed to the error register. This is done because the error prime for errored block control is the punch sample pulse which is not generated because these five characters are not punched. Thus, for EDC operation, only the 80-character block is checked for parity and the five fixed characters are not checked.

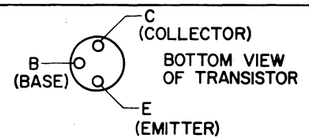
4. INSTALLATION

4.01 The receiver distributor module is prewired to accept the vertical parity detector. To install the unit, simply insert the parity logic card EC680 into position ZD209 and the parity error indicator card EC681 into position ZD210.

PARITY LOGIC



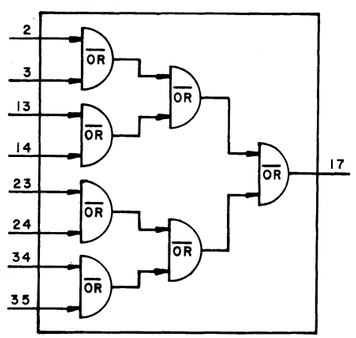
NOTE:
REFER TO 6050WD FOR BASIC MARKING INFORMATION

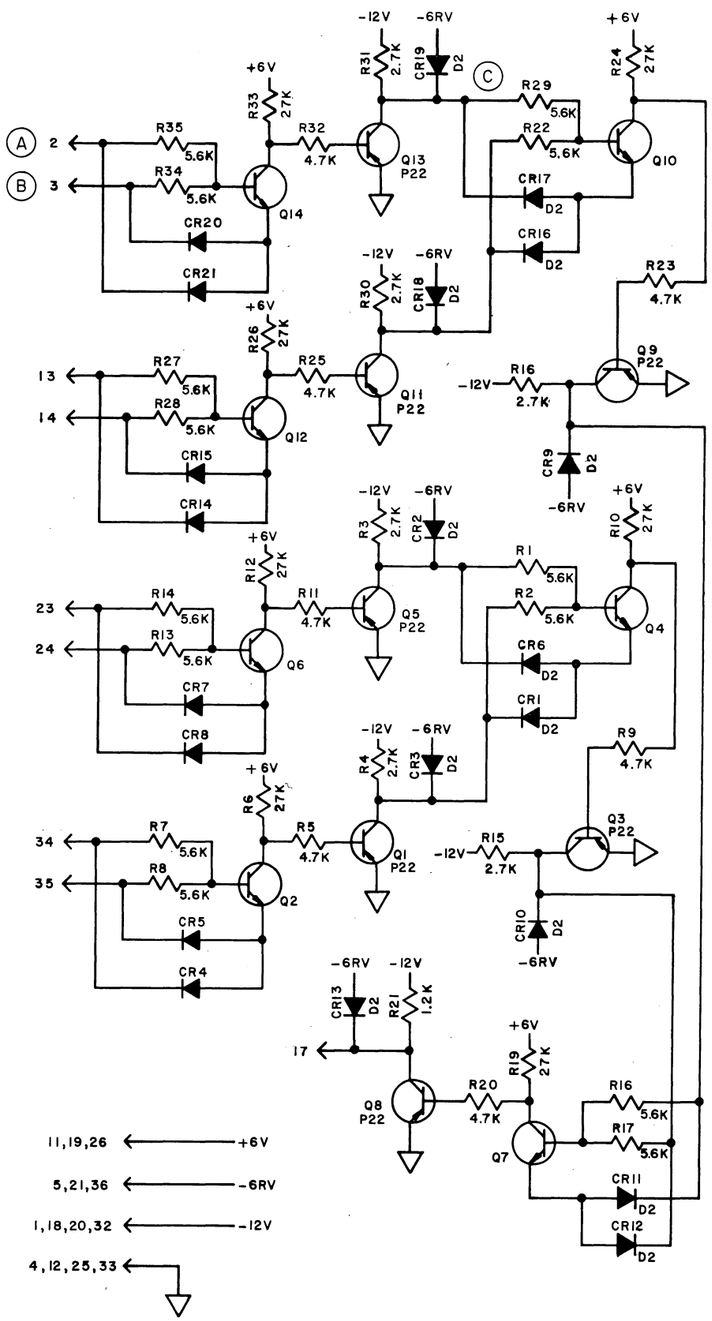


THIS CARD CONTAINS SEVEN EXCLUSIVE "OR" GATES CONNECTED TOGETHER TO FORM A PARITY TREE. A TYPICAL EXCLUSIVE "OR" GATE HAS THE FOLLOWING TRUTH TABLE (SEE TABLE BELOW) WITH INPUTS Ⓐ & Ⓑ BOTH AT 0 VOLTS OR AT -6 VOLTS, TRANSISTOR Q14 IS BIASED "OFF" AND THE COLLECTOR OF Q14 IS CLAMPED AT +6 VOLTS TO BIAS TRANSISTOR Q13 "OFF". THE OUTPUT Ⓒ IS CLAMPED AT -6 VOLTS. WITH INPUT Ⓐ AT 0 VOLTS AND INPUT Ⓑ AT -6 VOLTS OR INPUT Ⓐ AT -6 VOLTS AND INPUT Ⓑ AT 0 VOLTS, TRANSISTOR Q14 IS BIASED "ON". THE COLLECTOR OF Q14 WILL BE CLAMPED AT -6 VOLTS AND BIAS TRANSISTOR Q13 "ON". THE OUTPUT Ⓒ WILL BE CLAMPED AT 0 VOLTS. THE PARITY TREE CIRCUIT CONTAINS EIGHT INPUTS AND ONE OUTPUT. IF AN ODD NUMBER OF INPUTS IS AT 0 VOLTS, THE OUTPUT WILL BE CLAMPED AT 0 VOLTS. IF AN EVEN NUMBER OF INPUTS IS AT 0 VOLTS OR -6 VOLTS, THE OUTPUT WILL BE CLAMPED AT -6VOLTS.

INPUTS Ⓐ	INPUTS Ⓑ	OUTPUT Ⓒ
0 V	0 V	-6 V
-6 V	-6 V	-6 V
0 V	-6 V	0 V
-6 V	0 V	0 V

LOGIC SYMBOL





CIRCUIT BOARD

REF. DESIG.	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
R1-R2	118186	14	RESISTOR, 5,600 OHMS	GATE INPUT
R3-R4	118144	6	RESISTOR, 2,700 OHMS	COLLECTOR LOAD
R5	118146	7	RESISTOR, 4,700 OHMS	BASE INPUT
R6	118187	7	RESISTOR, 27000 OHMS	COLLECTOR LOAD
R7-R8			SAME AS R1	GATE INPUT
R9			SAME AS R5	BASE INPUT
R10			SAME AS R6	COLLECTOR LOAD
R11			SAME AS R5	BASE INPUT
R12			SAME AS R6	COLLECTOR LOAD
R13-R14			SAME AS R1	GATE INPUT
R15-R16			SAME AS R3	COLLECTOR LOAD
R17-R18			SAME AS R1	GATE INPUT
R19			SAME AS R6	COLLECTOR LOAD
R20			SAME AS R5	BASE INPUT
R21	137441	1	RESISTOR, 1,200 OHMS	COLLECTOR LOAD
R22			SAME AS R1	GATE INPUT
R23			SAME AS R5	BASE INPUT
R24			SAME AS R6	COLLECTOR LOAD
R25			SAME AS R5	BASE INPUT
R26			SAME AS R6	COLLECTOR LOAD
R27-R29			SAME AS R1	GATE INPUT
R30-R31			SAME AS R3	COLLECTOR LOAD
R32			SAME AS R5	BASE INPUT
R33			SAME AS R6	COLLECTOR LOAD
R34-R35			SAME AS R1	GATE INPUT
CR1-CR3	177108	13	DIODE, D2	CLAMP
CR4-CR5	181619	8	DIODE, IN482	GATE
CR6			SAME AS CR1	CLAMP
CR7-CR8			SAME AS CR4	GATE
CR9-CR13			SAME AS CR1	CLAMP
CR14-CR15			SAME AS CR4	GATE
CR16-CR19			SAME AS CR1	CLAMP
CR20-CR21			SAME AS CR4	GATE
Q1	177105	7	TRANSISTOR, P22	SWITCH
Q2	300455	7	TRANSISTOR, 2N697	SWITCH
Q3			SAME AS Q1	SWITCH
Q4			SAME AS Q2	SWITCH
Q5			SAME AS Q1	SWITCH
Q6-Q7			SAME AS Q2	SWITCH
Q8-Q9			SAME AS Q1	SWITCH
Q10			SAME AS Q2	SWITCH
Q11			SAME AS Q1	SWITCH
Q12			SAME AS Q2	SWITCH
Q13			SAME AS Q1	SWITCH
Q14			SAME AS Q2	SWITCH
	308474	1	CIRCUIT CARD, ETCHED	
	144495	14	PAD, TRANSISTOR	
	300116	2	COVER, INSULATING	

303680

REVISIONS

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DRAWN M.J.N. CHKD

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TELETYPE CORPORATION

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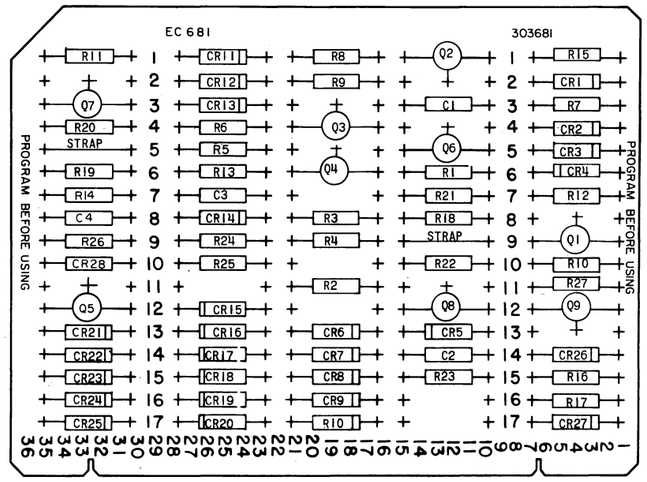
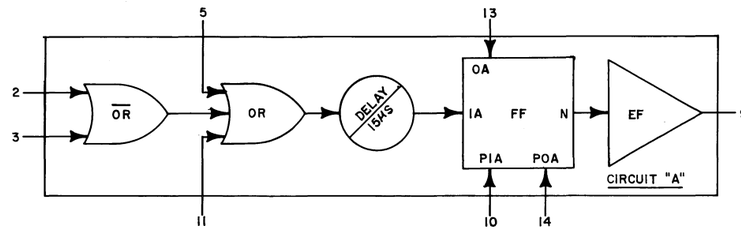
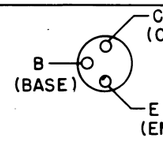


NOTE:
REFER TO 6050WD FOR BASIC MARKING INFORMATION





CIRCUIT BOARD

REF. DESIG.	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
C1, C4	192931	2	CAPACITOR .047	PULSE AMP.
C2–C3	177332	2	CAPACITOR .002	COUPLING
CR1–25	177108	25	DIODE, D2	GATE, CLAMP
CR26–27	177611	2	DIODE, IN682	COUPLING
CR28	178844	1	VARISTOR	BIAS
R1–2	118724	2	RESISTOR 220	BIAS
R3–4	143659	2	RESISTOR 560	BIAS
R5–6	137441	2	RESISTOR 1200	COLLECTOR LOAD
R7–9	129851	3	RESISTOR 3300	BIAS
R10–11	118146	2	RESISTOR 4700	COUPLING
R12–14	143665	3	RESISTOR 5100	LOAD
R15–18	118186	4	RESISTOR 5600	COUPLING
R19	118149	1	RESISTOR 12,000	BIAS
R20	118151	1	RESISTOR 18000	COLLECTOR LOAD
R21–26	118177	6	RESISTOR 22000	BIAS
R27	118187	1	RESISTOR 27000	BIAS
Q1–5	177105	5	TRANSISTOR P22	FLIP-FLOP, AMP.
Q6	193135	1	TRANSISTOR P24	EMITTER FOLLOWER
Q7	177106	1	TRANSISTOR N33	AMPLIFIER
Q8	193134	1	TRANSISTOR N35	EMITTER-FOLLOWER
Q9	177422	1	TRANSISTOR N39	GATE
	308535	1	CIRCUIT CARD ETCHED	
	144495	9	PAD, TRANSISTOR	
	300116	4	HAT, TRANSISTOR	
		2	24 AWG STRAP BARE	

THIS CARD CONTAINS TWO SPECIAL PURPOSE CIRCUITS USED IN TYPE 4 DATASPEED.

CIRCUIT A

THIS CIRCUIT CONSISTS OF AN EXCLUSIVE "OR", AN "OR" GATE, A DELAY INVERTER, A FLIP-FLOP AND A SYMMETRICAL EMITTER FOLLOWER. WITH BOTH INPUTS (2 & 3) AT 0 VOLTS OR -6 VOLTS, TRANSISTORS Q9 AND Q1 ARE BIASED "OFF". THE COLLECTOR OF Q1 WILL BE CLAMPED AT -6 VOLTS. WHEN ONE OF THE INPUTS IS AT 0 VOLTS AND THE OTHER IS AT -6 VOLTS, TRANSISTORS Q9 AND Q1 BIASED "ON" AND THE COLLECTOR OF Q1 WILL BE CLAMPED AT 0 VOLTS. THE COLLECTOR OUTPUT OF THE EXCLUSIVE "OR" IS CONNECTED TO ONE OF THE INPUTS OF THE "OR" GATE. THE OTHER TWO INPUTS ARE 5 AND 11. WITH ALL INPUTS AT -6 VOLTS, THE OUTPUT OF THE "OR" GATE WILL BE CLAMPED AT -6 VOLTS. WHEN ANY ONE OR ALL INPUTS ARE AT 0 VOLTS, THE OUTPUT WILL BE CLAMPED AT 0 VOLTS. THE OUTPUT OF THE "OR" GATE IS CONNECTED TO THE INPUT OF THE DELAY INVERTER AT R15. WITH THE INPUT AT 0 VOLTS, TRANSISTOR Q2 IS BIASED "OFF" AND THE COLLECTOR OF Q2 IS CLAMPED AT -6 VOLTS, WHEN THE INPUT TO THE DELAY INVERTER IS SWITCHED TO -6 VOLTS, THE OUTPUT WILL BE SWITCHED TO 0 VOLTS AFTER A 15 μS DELAY DUE TO THE TIMING CAPACITOR C1.

THE OUTPUT OF THE DELAY INVERTER IS CONNECTED TO THE SET IA INPUT OF THE FLIP-FLOP AT C3. THE PIA INPUT IS AT PIN 10. IN THE STEADY-STATE CONDITION TRANSISTOR Q3 IS "ON" AND TRANSISTOR Q4 IS "OFF". WITH PIA, PIN 10, AT -6 VOLTS, A POSITIVE PULSE AT C3 WILL BE INHIBITED FROM TURNING Q3 "OFF" WITH PIA AT 0 VOLTS, A POSITIVE PULSE AT C3 WILL CAUSE Q3 TO TURN "OFF" AND TRANSISTOR Q4 TO TURN "ON" THE COLLECTOR OF Q4 WILL THEN SWITCH FROM -6 VOLTS TO 0 VOLTS. TO RESET THE FLIP-FLOP, 0 VOLTS MUST BE PRESENT ON POA, PIN 14 AND A POSITIVE PULSE PRESENTED TO SET OA ON PIN 13. THIS WILL CAUSE TRANSISTOR Q4 TO TURN "OFF" AND TRANSISTOR Q3 TO TURN "ON" THE COLLECTOR OF Q4 WILL THEN SWITCH FROM 0 VOLTS TO -6 VOLTS. THE COLLECTOR OUTPUT OF Q4 IS CONNECTED TO THE INPUTS OF THE SYMMETRICAL EMITTER FOLLOWER AT Q6 AND Q8. WITH 0 VOLTS INPUT, THE OUTPUT PIN 9 WILL BE AT 0 VOLTS. WITH -6 VOLTS INPUT, THE OUTPUT WILL BE AT -6 VOLTS.

CIRCUIT B

THIS CIRCUIT CONSISTS OF A TWO-STAGE PULSE AMPLIFIER AND A FAN-OUT GATE. WITH THE INPUT PIN 36 OPEN-CIRCUITED OR AT -6 VOLTS, TRANSISTORS Q7 AND Q5 ARE BIASED "OFF" AND THE COLLECTOR OUTPUT OF Q5 WILL BE CLAMPED AT -6 VOLTS. ALL THE OUTPUTS OF THE FAN-OUT GATE WILL BE CLAMPED AT -6 VOLTS. WITH 0 VOLTS APPLIED TO THE INPUT PIN 36, TRANSISTORS Q7 AND Q5 WILL BE BIASED "ON". THE COLLECTOR OUTPUT OF Q5 WILL SWITCH TO 0 VOLTS, AND ALL THE OUTPUTS OF THE FAN-OUT GATE WILL ALSO SWITCH TO 0 VOLTS. DUE TO THE TIMING CAPACITOR C4, TRANSISTOR Q5 WILL REMAIN "ON" FOR A SHORT PERIOD OF TIME, APPROXIMATELY 25-40 μS, AFTER WHICH TIME Q5 WILL TURN "OFF" AND THE COLLECTOR OUTPUT OF Q5 WILL SWITCH TO -6 VOLTS AND ALL OUTPUTS OF THE FAN-OUT WILL SWITCH TO -6 VOLTS. THE OUTPUT PULSES WILL HAVE A RISE TIME, APPROXIMATELY 5-7 μS, IN DURATION.

THE FAN-OUT GATE MAY BE PROGRAMMED BY REMOVING APPROPRIATE DIODES.

303681

REVISIONS

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PARITY ERROR INDICATOR AND ERROR CHARACTER INSERTER

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DATE 8/1/65

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TELETYPE CORPORATION

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