ELECTRONIC CIRCUITS FOR

"DATASPEED"* PRINTER (RECEIVE-ONLY)

DESCRIPTION AND PRINCIPLES OF OPERATION

1. GENERAL

1.01   This section provides the description and principles of operation for the electronic circuitry found in the "DATASPEED" printer pertaining to the printer operator controls, data set interface, character generator, printer drive, power supply, ink heater and line feed bracket assembly, and the discrete calling generator modification kit. It is being reissued to incorporate recent engineering changes and technical comments not previously included. Since Issue 1 was presented in limited quantity, this is the first general distribution of this section.
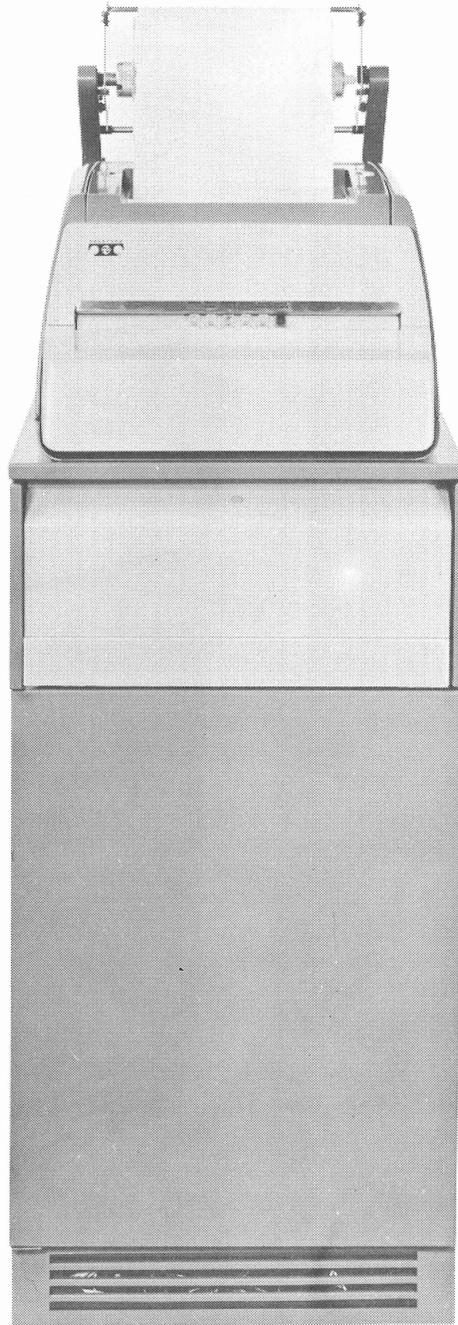
*Trademark and Service Mark of AT&TCo

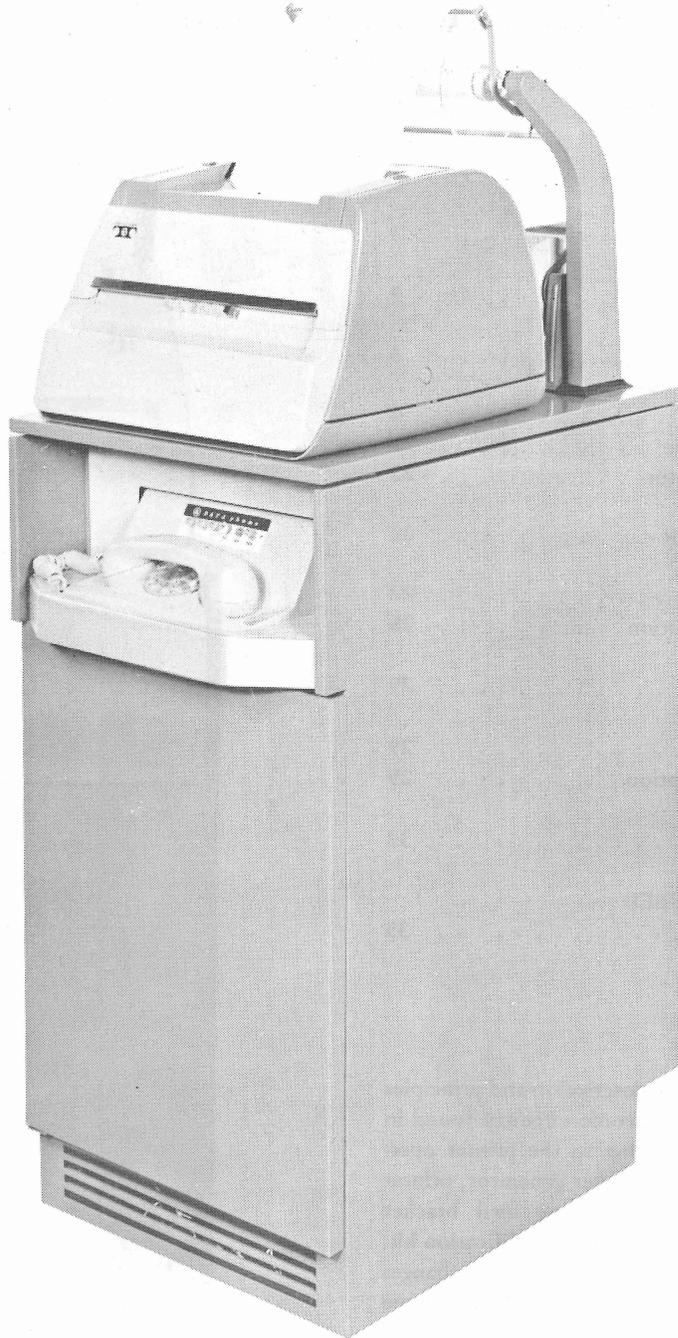Figure 1 - "DATASPEED" Printer Set Without Data Set

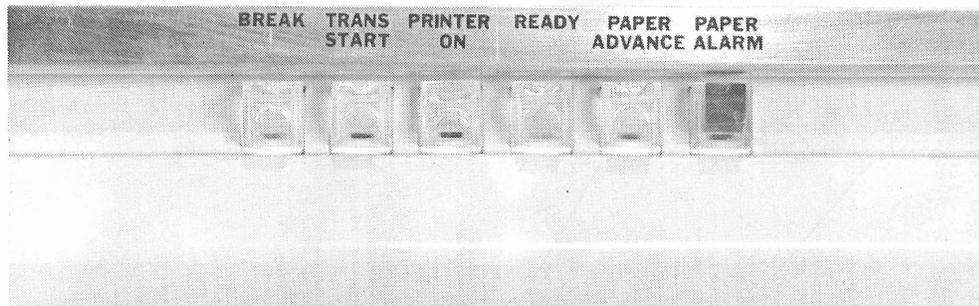Figure 2 - "DATASPEED" Printer Set With Data Set

Figure 3 - Operator Controls (At Front of Cover)

1.02 The "DATASPEED" printer operates from a signal source at 750, 1050, or 1200 words per minute (75, 105, or 120 characters per second) over standard telephone facilities. In order to interface with telephone facilities, it may have its own data set or be connected to an external data set in a "DATASPEED" sender or receiver; the data set is not furnished with the printer in either case. Sets operating at 1050 or 1200 wpm have a serial interface and those operating at 750 wpm a parallel interface.

1.03 The set consists of a cabinet containing the power supply and electronic modules plus space for a data set, with the page recorder and paper transport housed in a separate cover on top (Figures 1 and 2). A paper winder and unwinder are mounted outside the cabinet at the rear. Operator controls are located on a strip at the front of the cover (Figure 3). There are additional controls on the data set and inside the cabinet.

1.04 Power is supplied to the set from a 117 v ac line. High voltage is used in the recorder for printing. As a safety feature, three magnetic reed interlock switches are located inside the cover and one is located at the top center of each door opening to shut off the high voltage when any part of the cover is raised or the front or rear door is opened.

2. COMPONENTS

2.01 Most of the electronic circuits are contained in four modules, each 6 inches wide, 7 inches high, and 19-3/4 inches long, as follows: DAIF serial or parallel interface (may also contain discrete calling generator modification kit), DAG character generator, DAD printer drive, and DAPS power supply. The DAD and DAPS modules and the DAG and DAIF modules are attached to each other vertically when installed in the set so that they are drawn out together (Figure 4). Other circuits are located in the ink heater and line feed bracket assembly that is mounted on the data set shelf (not visible in Figure 4).

2.02 Components are mounted on etched circuit cards of various sizes (except for the power supply), some extending the entire length of the module. Besides discrete components such as resistors, capacitors, and diodes, many cards contain miniature integrated circuits identified by ML numbers. These cards have MC designations while cards with discrete components only have EC designations.

2.03 Integrated circuits used in the modules are of two types: logic circuits (gates and flip-flops) and operational amplifiers (op amps). Logic circuits are digital devices; that is, they respond to and produce as outputs high or low voltage levels or high-to-low or low-to-high transistions only. Op amps are linear devices and respond to a continuous range of voltages. All digital circuits used are compatible with the diode-transistor logic (DTL) family and all linear circuits are "709" type op amps. Schematic wiring diagram symbols and truth tables for the integrated circuits are shown in Figures 5 through 9 and the packages and configurations are shown in Figures 10 and 11.

3. OPERATION

3.01 Reference documents useful for helping to understand the operation of the electronic circuits, see Table A.

3.02 Operation will be described in the order a character would follow from the time its signal appears at the interface until it is printed on the page. The power supply will be covered last. Refer to Figure 12 for a block diagram of electronic operation.

INTERFACE

3.03 The printer is available with either of two interfaces, serial or parallel. Each is housed in the DAIF module. The serial interface (DAIF1) is used for all operation at 1050 and 1200 wpm while the parallel interface (DAIF2)

DAPW PAPER WINDER

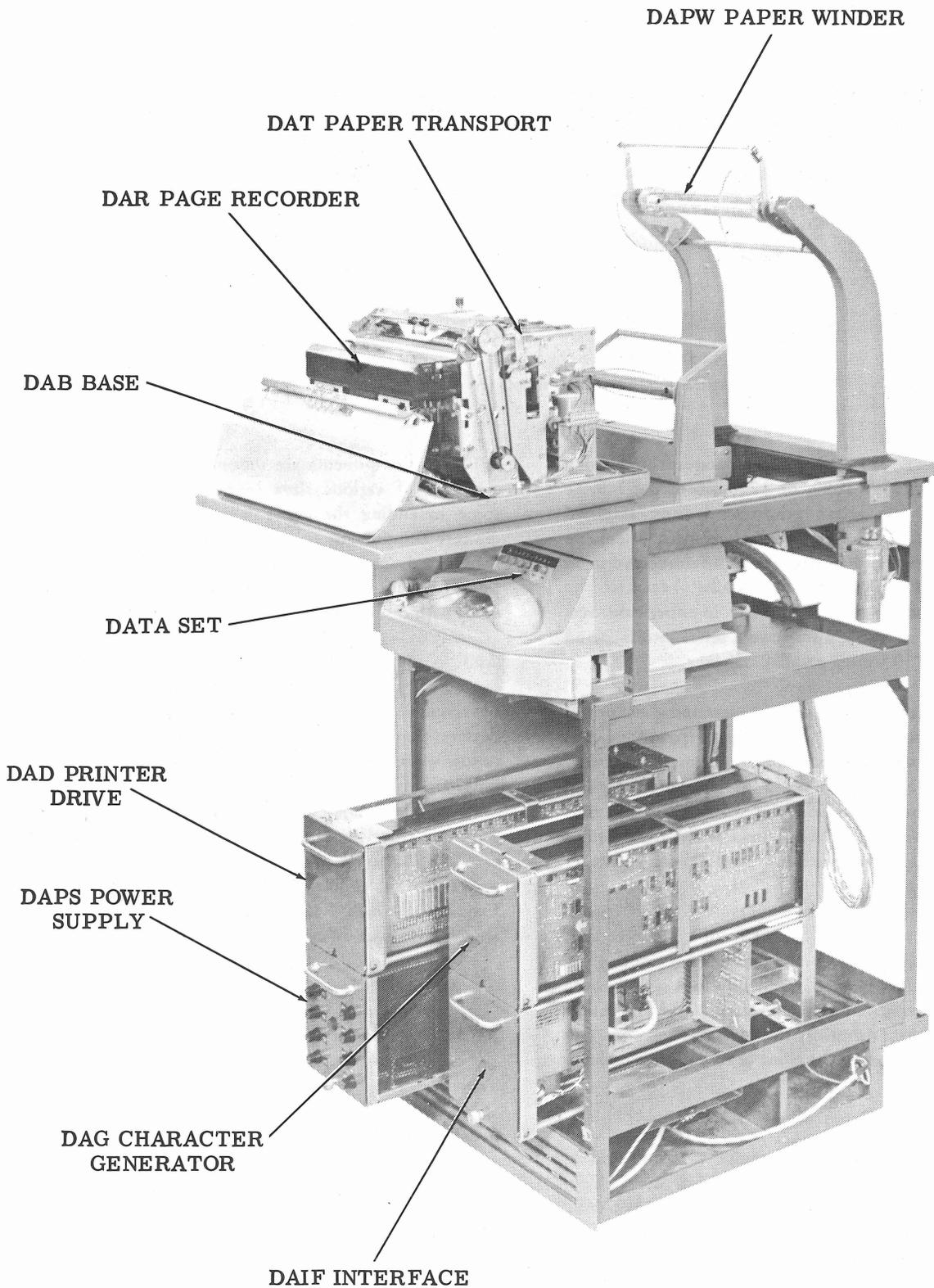DAT PAPER TRANSPORT

DAR PAGE RECORDER

DAB BASE

DATA SET

DAD PRINTER
DRIVE

DAPS POWER
SUPPLY

DAG CHARACTER
GENERATOR

DAIF INTERFACE

Figure 4 - "DATASPEED" Printer Set With Cabinet Panels and Cover Removed
and Upper Slide and Modules Extended

TABLE A

NO.	TITLE	TYPE
8254WD	Receive Only Printer	Schematic WD
8260WD	Receive Only Printer	Timing Diagram
8251/AAA/WD	DAIF1/AAA Serial Interface	Schematic WD
8257/AAA/WD	DAIF1/AAA Serial Interface	Actual WD
8263/AAA/WD	DAIF1/AAA Serial Interface	Reference WD
8268/AAA/WD	DAIF2/AAA Parallel Interface	Schematic WD
8274/AAA/WD	DAIF2/AAA Parallel Interface	Actual WD
8267/AAA/WD	DAIF2/AAA Parallel Interface	Reference WD
TP322130	MC130 Shift Register Card	Complete WD
TP322180-87	MC180-87 Receiver Distributor Control Cards	Complete WD
TP322132	MC132 202C/D Data Set Control RO Card	Complete WD
8256WD	Discrete Calling Generator Mod Kit	Schematic WD
8259WD	Discrete Calling Generator Mod Kit	Actual WD
8277WD	2B Tape Receiver Interface Mod Kit	Schematic WD
8278WD	2A Tape Sender Interface Mod Kit	Schematic WD
8279WD	2A and 2B Interface Mod Kit	Schematic WD
8280WD	5B Tape Receiver Interface Mod Kit	Schematic WD
8272WD	5B Tape Receiver Interface Mod Kit	Actual WD
8281WD	5A Tape Sender Interface Mod Kit	Schematic WD
8271WD	5A Tape Sender Interface Mod Kit	Actual WD
8282WD	5A and 5B Interface Mod Kit	Schematic WD
8273WD	5A and 5B Interface Mod Kit	Actual WD
8252/AAA/WD	DAG2/AAA Character Generator	Schematic WD
TP325365	DAG2/AAA Character Generator	Actual WD
8252/AAB/WD	DAG2/AAB Program Board	Schematic WD
8252/AAC/WD	DAG2/AAC Program Board	Schematic WD
8252/AAE/WD	DAG2/AAE Program Board	Schematic WD
TP322151	MC151 Input Logic Card	Complete WD
TP322150	MC150 Output Logic Card	Complete WD
TP322152	MC152 ASCII Control Logic Card	Complete WD
TP322153	MC153 Baudot Control Logic Card	Complete WD
TP303927	EC927 ASCII Program Board	Complete WD
TP303928	EC928 Baudot Program Board	Complete WD
TP303929	EC929 Output Board Assembly	Complete WD
TP322145	MC145 Spacing Drive (DAD3)	Complete WD
TP322146	MC146 Tracing Drive (DAD3)	Complete WD
TP303925	EC925 Resistor Divider Card	Complete WD
TP303926	EC926 HV Tracing Drive Amplifier Card	Complete WD
8255WD	DAPS5 Power Supply	Schematic WD
8261WD	DAPS5 Power Supply	Actual WD
TP303930	EC930 Line Feed Driver	Complete WD

is used for operation at 750 wpm. Modification kits are necessary to interface with Type 2 and Type 5 "DATA-SPEED" sets and an accessory is available to provide the discrete calling feature. The modification kits are covered in the same part as the appropriate interface but discrete calling, applicable to any interface, is described last by itself.

A. DAIF1 Serial Interface

General

3.04   The DAIF1 interface has only one mode of operation, serial receive only. It provides the station controls and signal conversion necessary to enable data interchange between a signal source such as a 202C or 804A data set or equivalent and elements of the high speed printer. The interface converts data from polar serial start-stop form to neutral parallel (voltage) form. The baud rate is fixed by the interface crystal oscillator frequency.

3.05   Both the printer and the sender are controlled by the interface in either the attended or unattended mode of operation. The interface signals the printer to turn on its motors and enables data to flow only if the printer indicates that it is ready to receive. If the printer cannot receive, the interface will signal the sender that no data should be sent.

3.06   The interface is insensitive to character code and can be wired for 5-, 6-, 7-, or 8-level characters enclosed in a 7, 7.42, 8, 9, or 10-unit frame. Its parallel output can be shifted to handle the 5-level, 10-unit code by means of a jumper clip arrangement so that levels 1 through 5 are received in level positions 2 through 6.

3.07   Power requirements for the interface are as follows:

$+6.0 \pm 0.6$ v dc at 0.500 amp
-12.0 ± 1.2 v dc at 0.150 amp
$+48.0 \pm 6.0$ v dc at 0.200 amp
117.0 ± 10.0 v ac, 60.0 ± 0.5 Hz at 1.0 amp

3.08   Input signals must conform to EIA Standard RS232-B. Output signals to the printer are $+6.0 \pm 0.6$ volts for a mark (or off condition) and 0.0 ± 0.5 volts for a space (or on condition). These signals will have less than 45 percent distortion per bit and 5 percent distortion per character. Output signals to the signal source are $+6.0 \pm 0.6$ volts for a space and -12.0 ± 1.2 volts for a mark.

3.09   There are three options for the DAIF1 interface, excluding variations in receiver distributor control cards for different operating speeds. All are strapping options, as follows:

DU - for operation on a dial-up or switched network
PL   - for operation on a private line or dedicated network and direct interface to a "DATASPEED" Type 2 Sender
Code - for operation with the 5-level code for typesetting.

Physically, the interface consists of three etched circuit cards with integrated circuit and discrete components (in positions ZAU, ZAS, and ZAN) and a NORM./TEST switch (Figure 13).

Controls and Indicators

3.10   The DAIF1 interface has the following controls and indicators on the function strip (Figure 3).

● BREAK (momentary pushbutton) — turns off reverse channel when operated to indicate that a break in transmission is desired. The button lights while it is depressed.

● TRANS START (momentary pushbutton) — starts the discrete calling generator accessory (if present) which sends a discrete code sequence to start an unattended transmitter. The button lights when it is depressed and goes out when the sequence is finished.

● PRINTER ON (indicator and momentary pushbutton) — lights when not operated when the printer has all conditions necessary for printing (a supply of paper and all interlocks closed) and has its motors and high voltage on. The indicator lights when operated only if all interlocks are closed, whether the printer is ready to receive or not.

● READY (indicator and momentary pushbutton) — lights when not operated when the printer has all conditions necessary for printing and the high voltage is capable of turning on or is on. If an overvoltage condition (plate on one or more high voltage tubes too high) should occur, the high voltage will be shut off and the READY lamp will go out. Operating the pushbutton resets the circuit, so the lamp will go on again if the overvoltage condition was temporary. However, the READY lamp always lights while depressed to indicate that it is not burned out.

● PAPER ADVANCE (momentary pushbutton) — feeds out paper and lights button while depressed.

● PAPER ALARM (red indicator) — lights when the paper supply drops below a specified level. The lamp may be tested by depressing the button.
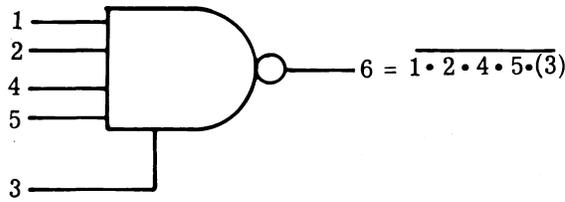
$$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot (3)}$$

NAND Gate (Extendable)

$$4 = 2 \cdot 3 \cdot 5 \cdot 6$$
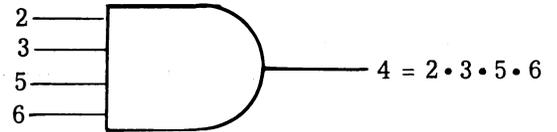
Extender (AND Gate)
(Also shown as four diodes connected together
at outputs)

INPUTS					OUTPUT
1	2	4	5	3	6
1	1	1	1	(1)	0
0	X	X	X	(X)	1
X	0	X	X	(X)	1
X	X	0	X	(X)	1
X	X	X	0	(X)	1
X	X	X	X	(0)	1

INPUTS				OUTPUT
2	3	5	6	4
1	1	1	1	1
0	X	X	X	0
X	0	X	X	0
X	X	0	X	0
X	X	X	0	0

Legend: 1 = High State (More Positive)
         0 = Low State (More Negative)
         X = State of Input Does Not Affect Output

(Output is low when all inputs are high and
high when any or all inputs are low. Input 3
is for extender use only.)

(Output is high when all inputs are high and
low when any or all inputs are low.)

$$6 = \overline{B1 \cdot B2 \cdot B4 \cdot B5 \cdot A2 \cdot A3 \cdot A5 \cdot A6}$$
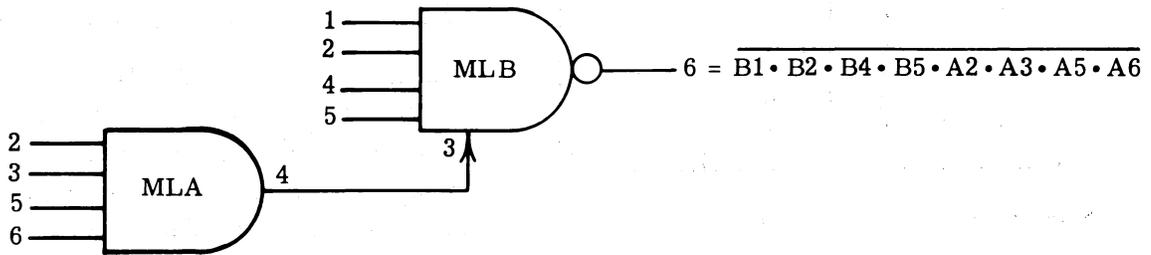
NAND Gate With Extender to Provide 4 Additional Inputs

$$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot 7}$$
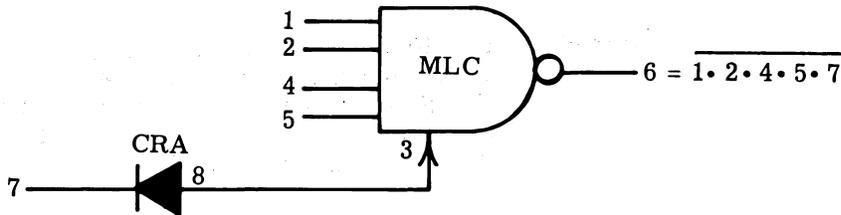
NAND Gate With Diode to Provide Additional Input

Figure 5 - NAND Gates and Extenders — Logic Symbols on
Schematic Wiring Diagrams and Truth Tables
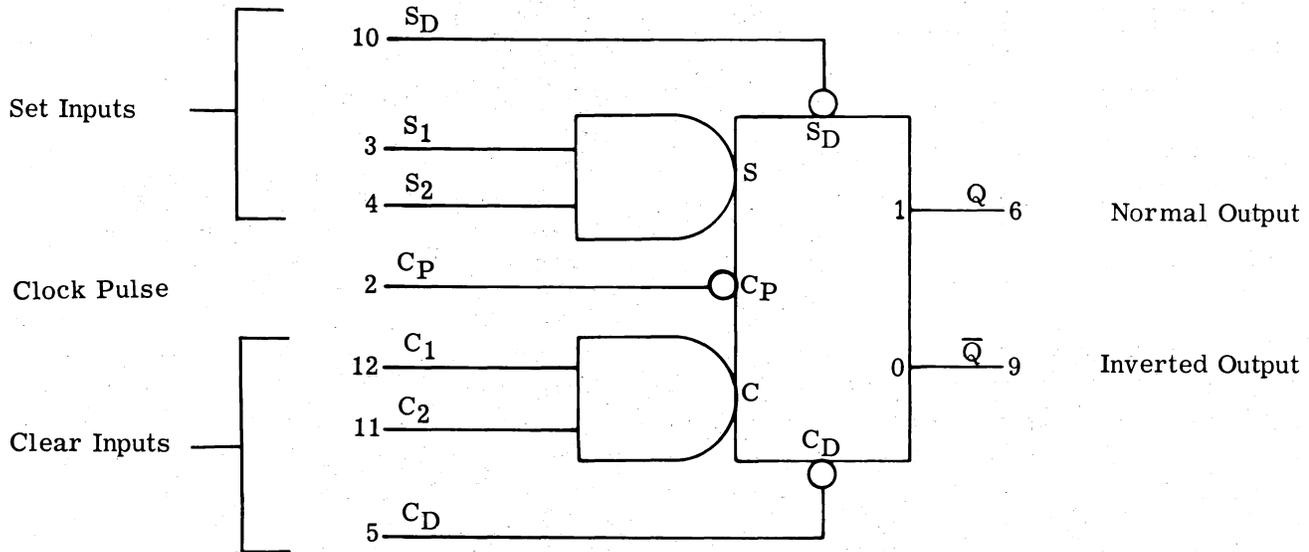
Clocked Flip-Flop

	T_N			T_{N+1}
S_1	S_2	C_1	C_2	Q
0	X	0	X	NC
0	X	X	0	NC
X	0	0	X	NC
X	0	X	0	NC
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

Synchronous Operation Truth Table

(T_{N+1} is the state of the flip-flop after arrival of the Clock Pulse (C_P), not shown.)

S_D	C_D	Q	$\overline{Q}$
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	1	1

Asynchronous Operation Truth Table

(The asynchronous inputs, Direct Set (S_D) and Direct Clear (C_D), override the synchronous inputs, Set 1 and Set 2 (S_1 and S_2) and Clear 1 and Clear 2 (C_1 and C_2); they are independent of all other inputs.)
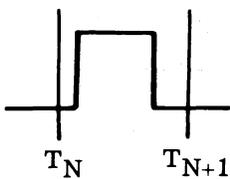

Legend: 1 = High State (More Positive)
0 = Low State (More Negative)
X = State of Input Does Not Affect Output
NC = No Change in State When Clock Pulse Arrives
U = Indeterminate State (1 or 0)

Clock Pulse Waveform

Figure 6 - Clocked Flip-Flop — Synchronous and Asynchronous Operation

Clocked Flip-Flop Connected for J-K Operation
(Q Connected to C_2, $\overline{Q}$ Connected to S_2)

T_N		T_{N+1}
S_1	C_1	Q
0	0	Q_N
1	0	1
0	1	0
1	1	$\overline{Q}_N$

J-K Operation Truth Table
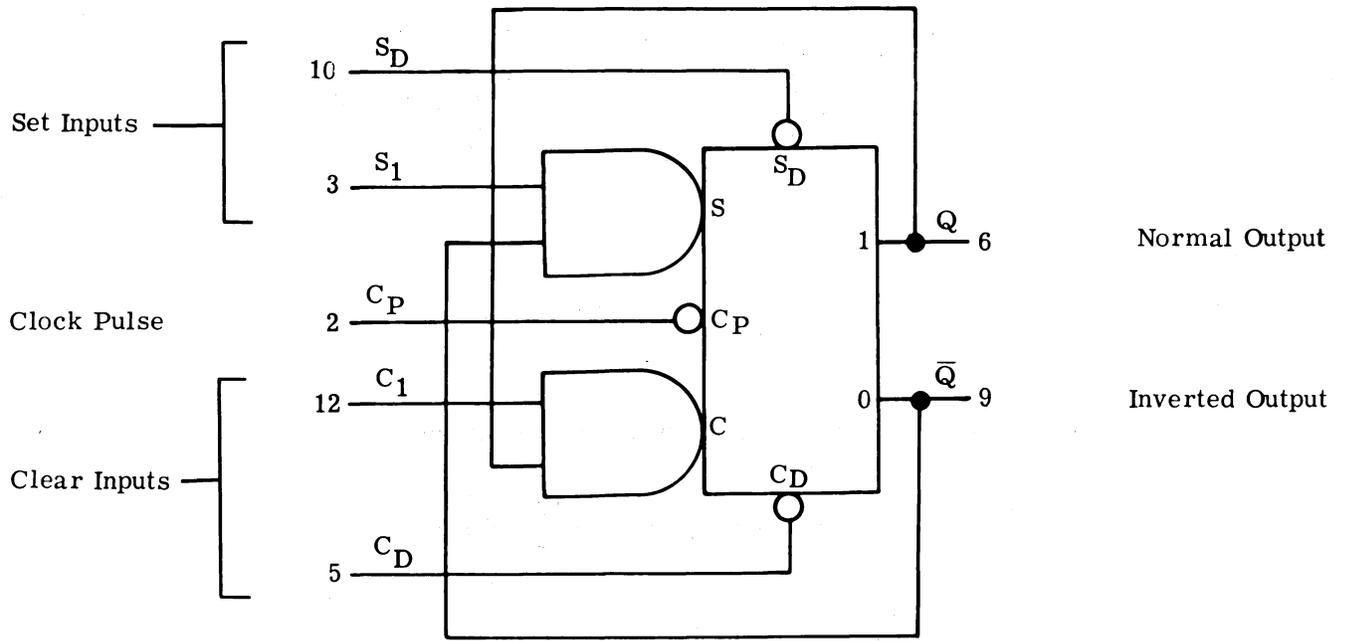
(T_{N+1} is the state of the flip-flop after arrival
of the Clock Pulse (C_P), not shown.)

Legend: 1 = High State (More Positive)
          0 = Low State (More Negative)
          Q_N = State of Q at Time N (No Change in State)
          $\overline{Q}_N$ = Inverse of State of Q at Time N (Change in State)

Clock Pulse Waveform
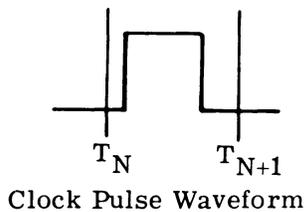
Figure 7 - Clocked Flip-Flop – J-K Operation
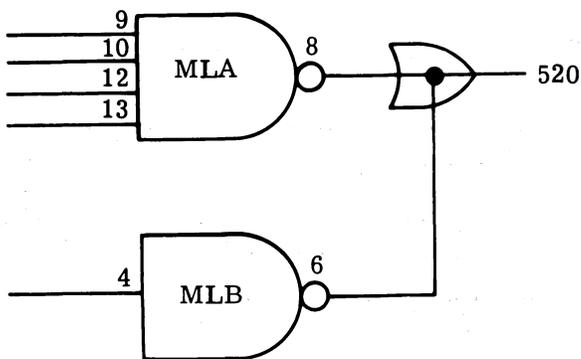
Wired OR Gate (At Interconnection of MLA and MLB)

INPUT		OUTPUT
8	6	520
1	1	1
0	1	0
1	0	0
0	0	0

Legend: 1 = High State (More Positive)
           0 = Low State (More Negative)

(Output is high when all inputs are high and low when any or
all inputs are low, the same as for an integrated circuit
AND gate. When +6 v and 0 v are applied to the same wire,
the 0 v always overrides the +6 v.)

Figure 8 - Wired OR Gate — Logic Symbol and Truth Table
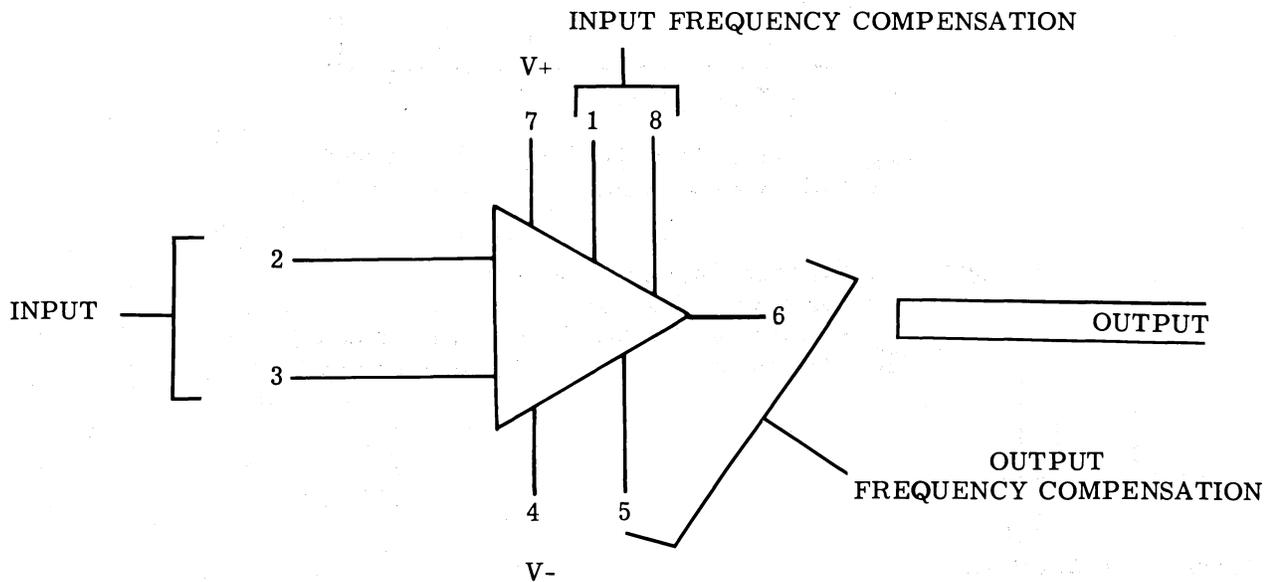
Figure 9 - Operational Amplifier (Op Amp)

REFERENCE END

Note: Numbers refer to terminals on package. Ground is applied to pin 7, +6 v to pin 14.

ML830 - Dual 4-Input NAND Gates (Extendable)
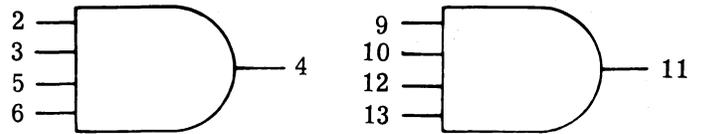
ML833 - Dual 4-Input Extenders

Dual-in-Line Integrated Circuit Package
(Top View)
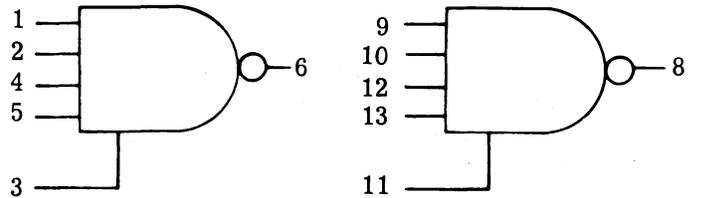
ML844 - Dual 4-Input Power NAND Gates
(Extendable)

ML845 - Clocked Flip-Flop
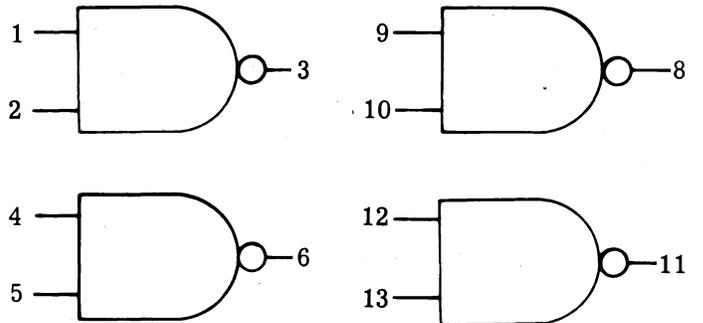
ML846 - Quad 2-Input NAND Gates
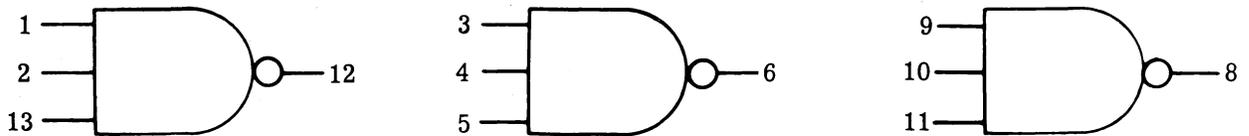
ML862 - Triple 3-Input NAND Gates

Figure 10 - Package and Configurations for Digital Integrated Circuits

REFERENCE TAB
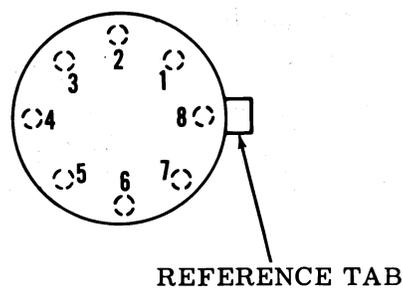
TO-Type Integrated Circuit Package
(Top View)
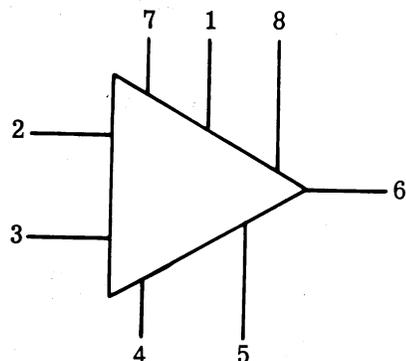
Note: Numbers refer to terminals on package.

Figure 11 - Package and Configuration for Operational Amplifier

The BREAK and TRANS START buttons are not used in private line versions of the DAIF1 interface. In addition to the controls and indicators on the function strip, there are five others located as follows.

● MAIN POWER (toggle switch, located on cabinet frame in front, below DAPS module) — switches all 117 v ac power to cabinet.

● NORM./TEST (slide switch, located on side of DAIF module frame) — allows printer to operate, when in the TEST position, regardless of the condition of the data set.

● Paper jam/paper out alarm (red lighted pushbutton, located on top of the left side frame of the paper transport) — indicates a paper line feed failure. If the paper storage loop is not renewed within 28 or 29 line feed steps (because paper has been allowed to run out or has broken or jammed, or the pre-paper puller motor has failed), the READY light on the control strip will go out, the paper jam/paper out alarm lamp will light, and the printer will become inoperable. (Normally the pre-paper puller motor renews the paper storage loop after 18 line feed steps, resetting the alarm circuit binary ripple counter.) The PAPER ALARM lamp may be lighted also. Depressing the pushbutton after the condition has been corrected resets the printer and extinguishes the red light.

● Override (pull switch, located on lower front of cabinet frame by lower door hinge, in back of front door) — overrides (bypasses) the interlock switches for the front

and rear doors when extended forward, permitting the printer to be turned on manually for servicing when the front door is removed.

● High voltage on (red indicator, located on face plate of DAPS module) — Lights when the high voltage is on. (This indicator is behind the front door and will be visible only when the door is removed and the override switch is operated.)

Operating Procedure

3.11   Dial-up Operation: If the printer data set is equipped with a handset, data calls may be originated manually at either the printer or the remote sender. If this data set is placed in the AUTO mode, data calls originating at the sender will be answered by the unattended data set. Examples of data set and interface operation showing the relationships among the control signals are given in Figures 14 and 15 for manual on-line operation with the printer originating the call and for unattended operation. Manual on-line operation with the sender originating the call, not shown, is similar. Operation may be interrupted by depressing the printer BREAK button, which removes the READY signal to the interface and so shuts off supervisory transmitted data (STD) to the data set. Absence of this signal removes reverse channel to the sender, causing it to stop.

3.12   Private Line Operation: In this type of operation calling is done automatically by a line controller device; no handset is used with the data set. Consequently, the data set is permanently on line and the data set ready, data terminal ready, and ring indicator signals are not used
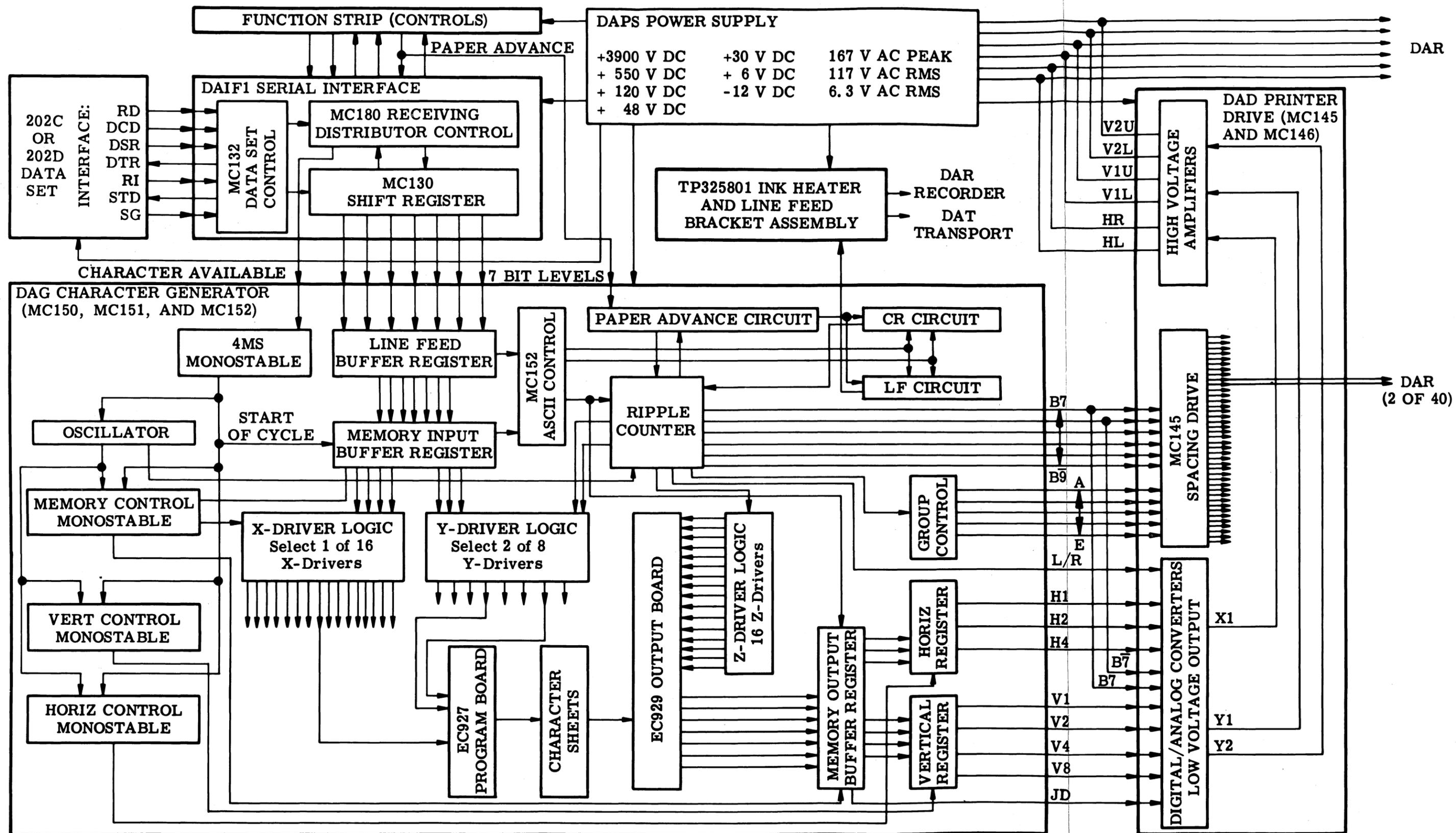
Figure 12 - Block Diagram of "DATASPEED"
Printer Electronic Circuits

POSITION ZAN

POSITION ZAS

POSITION ZAU

NORM./TEST SWITCH
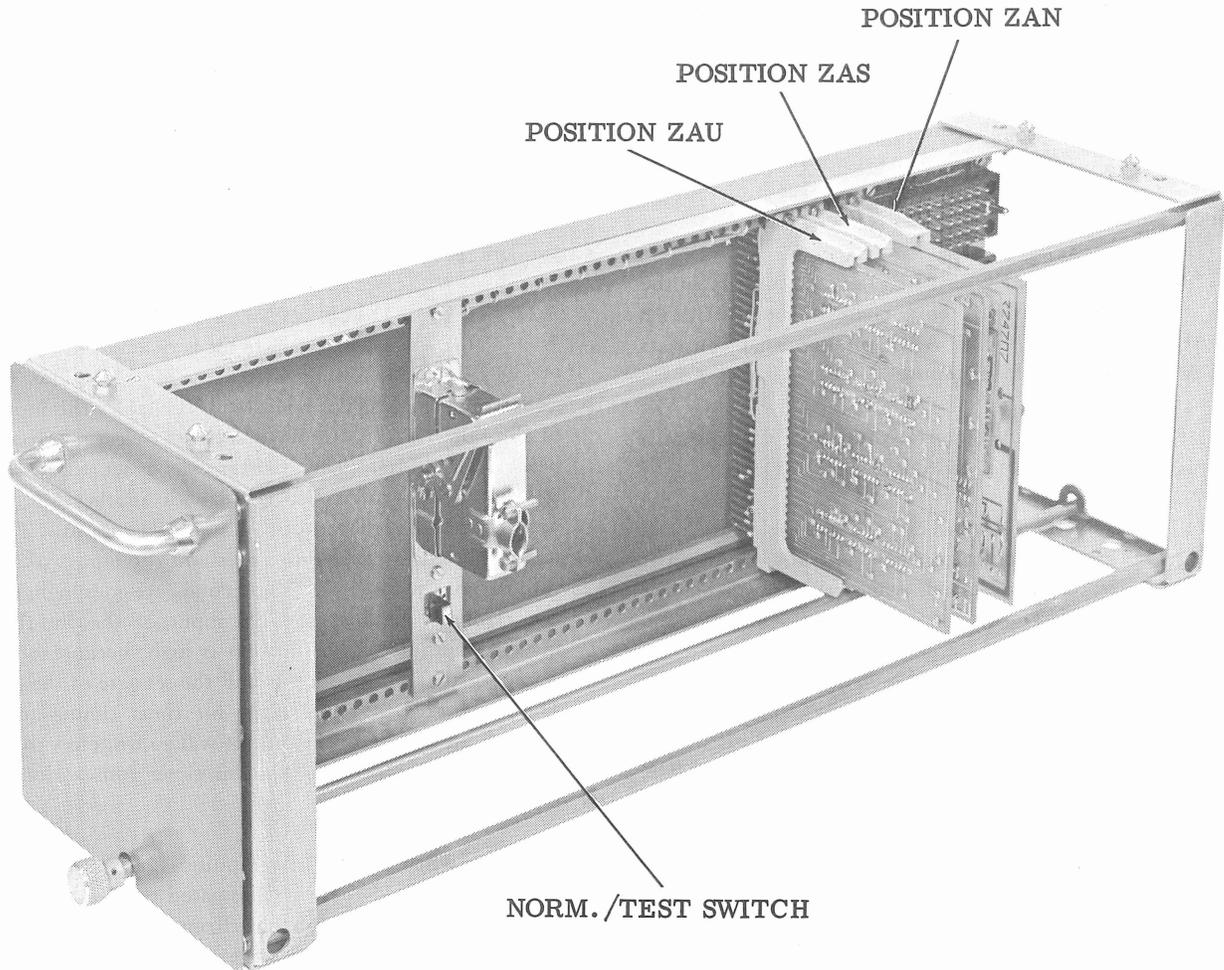
Figure 13 - DAIF1 Interface

and data carrier detector (DCD) is the main control signal. The sender activates the printer by placing carrier on line, causing DCD to come on to the interface. Line feed signals must be suppressed for 500 milliseconds after carrier is turned on to allow the motors to come up to speed. DCD on causes the interface to enable the received data (RD) signals and turn on the private line-receive message (PL-RM) signal to the printer. In response, the printer turns on its motors and high voltage and presents a READY signal to the interface, turning on STD and reverse channel. At the end of the message, carrier is turned off by the sender, causing DCD and PL-RM to go off and shut off the printer. If the printer interlocks are opened before or during a message or paper runs out at the transport, the DISCONNECT signal will go on, shutting PL-RM (and therefore the printer also) off.

Detailed Circuit Description

3.13   Refer to wiring diagrams 8251/AAA/WD (serial interface schematic), 8263/AAA/WD (serial interface master reference), TP322130 (MC130 shift register

card), TP322180-87 (MC180-87 receiver distributor control cards), TP322132 (202C and 202D data set control RO card), and 8260WD (timing diagram). Wiring diagram 8251/AAA/WD is not a complete schematic, but must be supplemented by the master reference wiring diagram (containing notes) and the three individual circuit card drawings (containing the schematics for the circuitry on the cards).

3.14   References to components in this description are abbreviated as follows: XZAN, XZAU, and XZAS refer to the terminals on the cards in positions ZAN, ZAU, and ZAS, respectively, and MLA1, MLA2, etc, refer to specific integrated circuit components. The number following an XZ or ML designation designates an associated terminal or pin. For example, "XZAN-18, MLA2-3, MC132" refers to terminal 18 on card MC132, located in position XZAN, which is connected directly to pin 3 on circuit MLA2. The drawing of card MC132 shows that circuit MLA2 is three three-input NAND gates. All "gates" mentioned in the description are NAND gates unless stated otherwise, and all

references to MC180 apply to cards MC181 through MC187 as well. Refer to Figures 5 through 9 for schematic wiring diagram symbols and truth tables for the integrated circuits.

3.15 Logic signals, unless noted otherwise, are either +6 v (high) or 0 v (low). The on or off condition of a circuit element varies with its function and is defined separately.

3.16 Turn On: The NORM./TEST switch must be in the NORM. position. This enables the RECEIVE MESSAGE lead XZAN-18, MLA2-3, MC132, that connects to the AUTO ON relay driver input.

3.17 The DAIF1/AAA interface turns the data terminal ready (DTR) lead, XZAN-33, on (+6 v) if:

(1) DISCONNECT lead XZAN-32 is high at MLA1-4, MC132. This indicates a general ready condition at the printer, cabinet closed, some paper available for printing.

(2) SELECTABLE lead XZAN-12 is low at MLA1-10, MC132. This signal detects a low paper condition at the paper supply and turns the DTR lead off (-12 v) before the printer answers a new data call. The SELECTABLE lead cannot cause the DTR lead to turn off once a call has been answered.

(3) The disconnect timer output OP-6, MC132 is high (+6 v) at MLA1-5.

3.18 While the data carrier detect (DCD) lead, XZAN-25, MC132, is off (-12 v), it forces MLA1-1 low, disabling receive data (RD) gate (MLA1-12) and the PL-RM gate (MLA3-6). The data set ready (DSR) lead XZAN-27 is also off, forcing MLA2-3 high and holding off the RECEIVE MESSAGE lead, XZAN-18, which keeps the motors and high voltage off. The DSR lead low also forces MLA3-3 high which switches MLA2-6 low, disabling the disconnect timer.

3.19 The DSR on signal (+6 v) initiates the turn on. It switches on the RECEIVE MESSAGE lead (low) at MLA2-3 and also enables MLA3-3, forcing MLA2-6 high and causing the disconnect timer to begin timing out.

3.20 When DCD (XZAN-25) comes on, MLA2-8 goes low, resetting the disconnect timer; this keeps MLA1-5 high and allows DTR, at the collector of Q2 to remain high. With DCD high and ring indicator (RI) at MLA3-10 low, receive data (RD) gate MLA1-2 is enabled.

3.21 Receive Data: the received data bits come into MC132-24, MLA1-13 and each is converted to a high signal — from a mark (-12 v) — or to a low signal — from a space (+6 v) — at the output, MLA1-12. This signal goes to

the RD input of MC130-B29, MLA4-4 and card MC180. The MC180 signal is inverted with respect to the incoming signal and goes to the RD bar input of the shift register, MC130-B31, MLA4-12, and to the bit timer on MC180. When data is not present the RD input, MC132-24, must be kept marking (-12 v) or the bit timer will be free-running. The receive mode (RM) signal, is strapped to ground forcing the RR+ output high and thus enabling all the necessary gates for data reception.

3.22 The RD lead, MC132-24, is normally marking (-12 v), but when a start bit is received it goes spacing (+6 v), forcing the output of RD gate MLA1-12 low. This low signal and a high signal from MC180 enables the input gates of flip-flop MLA4, MC130 to shift in a clear or space on the next clock pulse. (The register was reset to mark.) The MC180 high signal is also gated with another MC180 high signal and forces the output of a NAND gate low. This pulls down the output of another gate and the inputs of a second gate and of the bit timer. The second gate goes high, releasing the clamp it held at the CD input of the flip-flop. The inverted output of the flip-flop is high, because of the CD clamp, enabling a gate input and the set gate of the flip-flop. The low signal also starts the bit timer timing and about one-half bit time later the output will go from low to high for about 10 microseconds. The bit timer runs as long as the input is low.

3.23 When the bit timer pulse is applied to the other input of the gate it is gated through and inverted. The binary does not change from the 0 to the 1 state, however, until the trailing edge of the bit timer pulse nears ground. When this happens, the gate is disabled and the flip-flop clear input is enabled. The next bit timer pulse will not be passed by the gate but the binary will go back to the 0 state on the trailing edge of the pulse. Thus, the next pulse will be enabled to go through the gate. The bit timer pulse rate is therefore twice the bit rate and the first pulse out occurs at the midpoint of the start bit. This is the one-half bit sample delay and is followed by the binary and gate dividing the pulse rate by two to match the bit rate. If the start bit is less than the bit timer rate, the bit timer will be reset before a pulse can be generated.

3.24 The pulses passed by the gate are inverted and applied to the clock pulse buss of the shift register, ZAU, MC130. The CP inputs are pins 2 of the elements MLA4, MLA3, MLA2, MLV2, MLC4, MLC3, MLC2, MLD3, and MLD2. Another gate on MC180 also inverts the pulses and applies them to an additional gate on the same card. Its output is high except when the shift register element 1 outputs (pins 6) are all high. Another input of this gate is high because the output of a gate is forced high when it detects a stop condition. If the shift register has all marks (1) in it (clear condition), the output of the other gate is low and does not pass a register reset pulse (RR), since it is not needed. If there is a character in the shift register, an input of

SENDING STATION   DATA SET   LINE   DATA SET   DAIF1 INTERFACE   PRINTER

NORM./TEST switch in NORM.

Paper not low (SELECTABLE): interlocks closed, paper not out at transport (non-DISCONNECT).

DTR on enables data set to stay in DATA mode when DATA button depressed (later).

SELECTABLE, non-DISCONNECT received causes Data Terminal Ready (DTR) to go on to data set.

SELECTABLE on, DISCONNECT off signals sent to interface.

DTR and Request to Send (RTS) must be on to data set for data to be sent.

Must be in Talk Mode. Operator answers call and talks.

If above conditions are present, operator may place data set in Talk Mode and dial a sender. (Operation is similar if sending station initiates call).

Called station goes to Data Mode first (by depressing DATA button). Data Set Ready (DSR) goes on to sender.

DSR received.

2025 Hz recognition tone sent for 3.5 seconds after 1.5 second delay.

Operator recognizes tone and depresses DATA button. before it ends.

1200 Hz mark tone turned on.

DSR goes on to interface. 1200 Hz mark tone received.

DSR received causes RECEIVE MESSAGE signal to go on to printer. 15-second timer starts.

Printer turns on motors and high voltage. AUTO ON relay operates, so (if BREAK button not depressed) READY signal goes on to interface.

DCD received.

Data Carrier Detector (DCD) comes on after 40 ms.

STD on causes reverse channel (if used by data set) to go on.

READY on causes Supervisory Transmitted Data (STD) to go on to data set.

SRD received.

Reverse channel received causes Supervisory Received Data (SRD) to go on (if used — pause otherwise).

DCD comes on 40 ms after receipt of mark tone carrier. Received Data (RD) unclamped at same time.

DCD received causes 15-second timer to stop; RD signals enabled. Note: if DCD is not received before 15 seconds are up, the timer times out and drops the call as described below.

CTS received. DSR, DCD, SRD, and CTS cause sender to begin transmitting data to data set as Transmitted Data (TD) signal.

Clear to Send (CTS) turned on 200 ms after 1200 Hz tone sent.

Data transmitted (in serial form).

Data received.

Received data converted from serial to parallel form and send to printer.

Data printed.

At end of message, data transmission stops. RTS goes off.

Transmission stops.

DSR, DCD, and CTS removed.

Operator terminates call by depressing TALK button, going off-hook, then on-hook again. This removes data carrier, DSR, DCD, and CTS.

DCD turns off when sending data set disconnected.

DCD off causes 15-second timer to start; RD signals disabled (preventing printer from copying noise).

Data call is dropped when DTR goes off; data set goes on-hook automatically. DSR goes off to interface.

Timer completes 15-second cycle, shutting DTR off to data set.

DSR off causes RECEIVE MESSAGE to go off to printer and resets timer. DTR goes on again if printer paper and interlock conditions are unchanged.

Printer turns off motors and high voltage.

Note: All times shown are approximate. Propagation time, not shown, may vary widely from call to call.

Reverse channel (if used by data set) goes off when STD goes off.

STD goes off to data set when READY goes off.

READY signal goes off to interface.

The printer is now ready to make or receive a new call.

Figure 14 - Manual On-Line (Dial-Up) Operation of DAIF1 Interface, Printer Initiates Call

SENDING STATION	DATA SET	LINE	DATA SET	DAIF1 INTERFACE	PRINTER
			Must be in AUTO mode or have no handset.	NORM./TEST switch in NORM.	Paper not low (SELECTABLE); interlocks closed, paper not out at transport (non-DISCONNECT).
			DTR on enables data set to answer call unattended.	SELECTABLE, non-DISCONNECT received causes Data Terminal Ready (DTR) to go on to data set.	SELECTABLE on, DISCONNECT off signals sent to interface.
DTR and Request to Send (RTS) must be on to data set for data to be sent.	If able to send, operator may place data set in TALK mode and dial receiver.		Data set answers call automatically, causing Data Set Ready (DSR) to go on to interface.	DSR received causes RECEIVE MESSAGE signal to go on to printer. 15-second timer starts.	Printer turns on motors and high voltage.
	Operator recognizes tone and immediately depresses DATA button, placing data set in DATA mode.		2025 Hz recognition tone set for 3.5 seconds after 1.5 second delay.		
SRD received.	Reverse channel received causes Supervisory Received Data (SRD) to go on (if used — pause otherwise).		STD on causes reverse channel (if used by data set) to go on.	READY on causes Supervisory Transmitted Data (STD) to go on to data set.	AUTO ON relay operates, so (if BREAK button not depressed) READY signal goes on to interface.
DSR received.	DSR goes on to sender and 1200 Hz mark tone is sent on line.	1200 Hz mark tone received.			
DCD received.	DCD comes on after 40 ms.		Data Carrier Detector (DCD) comes on 40 ms after receipt of mark tone carrier. Received Data (RD) unclamped at same time.	DCD received causes 15-second timer to stop; RD signals enabled. Note: if DCD is not received before 15 seconds are up, the timer times out and drops the call as described below.	
CTS received. SRD, DSR, DCD, and CTS cause sender to begin transmitting data to data set as Transmitted Data (TD) signal.	Clear to Send (CTS) turned on 200 ms after 1200 Hz tone sent.				
	Data transmitted (in serial form).		Data received.	Received data converted from serial to parallel form and sent to printer.	Data printed.
At end of message, data transmission stops. RTS goes off.	Transmission stops.				
DSR, DCD, and CTS removed.	Operator terminates call by depressing TALK button, going off-hook, then on-hook again. This removes data carrier, DSR, DCD, and CTS.		DCD turns off when sending data set disconnected.	DCD off causes 15-second timer to start; RD signals disabled (preventing printer from copying noise).	
			Data call is dropped when DTR goes off; data set goes on-hook automatically. DSR goes off to interface.	Timer completes 15-second cycle, shutting DTR off to data set.	
				DSR off causes RECEIVE MESSAGE to go off to printer and resets timer. DTR goes on again if printer paper and interlock conditions are unchanged.	Printer turns off motors and high voltage.
			Reverse channel (if used by data set) goes off when STD goes off.	STD goes off to data set when READY goes off.	READY signal goes off to interface.

Note: All times shown are approximate. Propagation time, not shown, may vary widely from call to call.

The printer is now ready to receive a new call.

Figure 15 - Unattended On-Line (Dial-Up) Operation of DAIF1 Interface, Sender Initiates Call

this gate is high and it passes a reset pulse. The reset pulse goes to a dc flip-flop, and clears it (to the 0 condition), ending any character available condition. It also goes to the SD inputs (10) of all shift register elements except MLD2, MC130. When all of the shift register elements have gone to the 1 state or high condition, the inputs of three gates on MC180 are all high, forcing their outputs low and ending the reset pulse. This pulse typically has a 300-nano-second duration.

3.25   The master-slave (synchronous) operation of a clocked flip-flop used as an element of the shift register is as follows: When the clock pulse goes from low to high it disconnects the slave latch from the master latch and sets the set or clear input into the master latch. When the clock pulse goes from high to low again it disables the set and clear inputs to the master latch and transfers what is in the master latch into the slave latch, fixing the register outputs (Figure 6). The clock pusle, MLB3-8, and the reset pulse, MLD3-8, are applied to the clock pulse inputs, pins 2, and the reset (SD) inputs, pins 10, respectively, of the shift register elements simultaneously during the start bit. The clock pulse shifts the start bit into the MLA4, MC130 master flip-flop while the reset pulse is setting all of the shift register slaves to the 1 state. The reset pulse is removed almost 10 microseconds before the clock pulse goes low again and thus shifts the start bit into the MLA4, MC130 slave.

3.26   The first clock pulse causes a mark to be shifted into MLD2 and a space into MLA4. This forces the input of a gate on MC180 high and it will stay that way as long as MLD2 is marking, which is for the next eight clock pulses. When the input goes high it switches the output of a second gate on MC180 low, which keeps the reset gate on this card disabled and sets a dc flip-flop in the 1 state, disabling its output, the register character available signal. The input of a gate on MC180 being high also switches the output of another gate low, keeping the bit timer on.

3.27   During character reception this signal holds the bit timer on. When the start bit, which is a space, is shifted into the MLD2, MC130, flip-flop and a stop bit, which is a mark, is shifted into the MLA4, MC130, flip-flop of the shift register, this MC180 signal goes low. This forces the outputs of two gates high. With a mark on the RD lead, another gate output is high and the output of the wired OR gate at the outputs of it and another gate is high, causing the bit timer to turn off. The binary is clamped to the 0 state at the CD input, pin 5, by one gate. The output of another gate, being high enables the reset gate and one of the dc flip-flop gates — signaling to the character generator that a character is available. At this time the states of the eight shift register flip-flops are sampled simultaneously by the character generator. This condition remains until the next start bit is sampled or a general reset is received.

3.28   When the MC180 gate goes low, signaling that a character is available in the shift register, it forces another gate high and the output of the next gate goes low.

This causes two more gate outputs to go high. The 100-microsecond delay circuit will time out and give an output pulse going from 0 to +2.5 volts — at base 1 of a field-effect transistor (FET) — for about 10 microseconds. This pulse is inverted by a transistor, clearing a dc flip-flop. When a gate output goes low, it prevents a capacitor from charging up again until the dc flip-flop is reset on the removal of the low signal from the other dc flip-flop. A gate inverts the 10-microsecond negative-going pulse from the collector of the transistor, and another gate inverts it again and presents it to the character generator as the character available signal.

3.29   Turn Off: When the DCD lead, XZAN-25, MC132, turns off, it causes MLA2-6 to go high. The disconnect timer times out and forces MLA1-5 low, turning off (-12 v) the DTR lead, XZAN-33. The DCD low disables the RD input, MLA1-13, and assures a high on the RD output — thereby stoping MC130 and MC180 from cycling. When DTR turns off, it will cause the DSR lead XZAN-27, to go low (-12 v). When the DSR goes low, it forces MLA2-11, MC132 high, turning off the RECEIVE MESSAGE lead. The DSR low also resets the disconnect timer by forcing MLA2-6 low.

3.30   With the disconnect timer reset, DTR can once again go high providing the NORM./TEST switch is still in NORM.

B.   DAIF2 Parallel Interface

General

3.31   The DAIF2 interface has only one mode of operation, parallel receive only. It provides the station controls and signal conversion necessary to enable data interchange between a signal source such as a 402D data set or equivalent and elements of the high speed printer. The interface converts data from parallel contact closures or equivalent to neutral parallel (voltage) form. The baud rate is fixed by the sender but may not exceed the data set maximum (750 for a 402D). A 402D data set must be mounted external to the printer cabinet.

3.32   Both the printer and the sender are controlled by the interface in either the attended or unattended mode of operation. The interface signals the printer to turn on its motors and enables data to flow only if the printer indicates that it is ready to receive. If the printer cannot receive, the interface will signal the sender that no data should be sent.

3.33   The interface is insensitive to character code and can be wired for 5-, 6-, 7-, or 8-level characters enclosed in a 7, 7.42, 8, 9, or 10-unit frame. Its output can be shifted to handle the 5-level, 10-unit code by means of a jumper clip arrangement so that levels 1 through 5 are received in level positions 2 through 6.

3.34   Power requirements for the interface are as follows:

6.0 ± 0.6 v dc at 0.125 amp
-12.0 ± 1.2 v dc at 0.050 amp
+48.0 ± 6.0 v dc at 0.200 amp
117.0 +10.0 v ac, 60.0 +0.5 Hz at 1.0 amp

3.35   Input signals for a mark (or on condition) must be ground (0.0 +0.5 volts) capable of sinking 4 milliamps dc resistive, and for a space (or off condition) must be open or very high resistance (100 K ohm or higher) capable of withstanding +6.6 v dc. The timing lead must be on for a minimum of 4 milliseconds and should occur at a time when the data leads are free of transitions. Output signals to the printer are +6.0 +0.6 volts for a mark (or off condition) and 0.0 +0.5 volts for a space (or on condition). The data signals will have the same duration as the incoming timing signal and the output timing signal will be present for about 280 microseconds near the midpoint of the data signals.

3.36   There are three strapping options for the DAIF2 interface, as follows:

DU - for operation on a dial-up or switched network

DU Omitted - for operation on a private line or dedicated network and direct interface to a "DATASPEED" Type 5 Sender or Receiver

Code- for operation with the 5-level code for typesetting.

Physically, the interface consists of an etched circuit card with integrated circuit and discrete components and a NORM./TEST switch.

Controls and Indicators

3.37   Controls and indicators are the same as for the DAIF1 interface (3.10).

C.   Discrete Calling Generator

3.38   The TP325200 discrete calling generator consists of a TP199570 signal generator assembly and a relay bracket assembly, mounted within the DAIF1 or DAIF2 module frame. The signal generator assembly has a 20 rpm 117 v ac motor and clutch, a TP199580 programmable code disc, and a set of stationary sensing brushes. A dual wire spring relay and terminal strip are mounted on the relay bracket. When programmed, the discrete calling generator permits the printer to enable an unattended Type 2 or Type 5 "DATASPEED" Sender equipped with an identically programmed recognizer.

3.39   Depressing the TRANS START pushbutton on the printer function strip (after the PRINTER ON light has come on) operates the discrete calling generator relay, placing the associated data set in the send or answer-back mode and engaging the clutch. This starts the code disc turning and generates the discrete 14-bit code. When the code disc completes one revolution it stops and restores the data set to its original mode.

3.40   The TP325200 discrete calling generator is almost identical to the TP199550 protected unattended transmitter modification kit for Type 2 "DATASPEED" Receivers. It differs from the TP199550 kit in that it mounts in the interface module instead of having its own frame and cabling and uses a positive instead of a negative voltage supply. There is no difference as far as operation with type 2 equipment is concerned. The discrete calling generator is also similar to the TP199784 station identifier for Type 5 "DATASPEED" Receivers. There are packaging and electrical differences but operation with type 5 equipment is identical. Refer to Section 592-808-101 for additional information.

CHARACTER GENERATOR

3.41   The character generator is a memory and logic system which translates incoming codes from the interface into the signals necessary for the printer drive to direct the generation of characters by the recorder. It controls both the tracing of each individual character and the spacing of characters on a line, plus additional functions such as line feed. The character generator is housed in the DAG module (Figure 16).

A.   General

3.42   The character generator receives information input signals (seven for ASCII, five for Baudot) and a start signal from the interface, in parallel form. Together, these signals define a character. Each character is stored for eight milliseconds while the logic selects and processes the appropriate memory subroutine. This processing consists of sequentially interrogating the memory while storing the character until the tracing drive processes it. On completion of the printing of each character the generator locates to the next printing position.

3.43   The character generator has provisions for generating 64 characters, with each character being composed of a maximum of 31 dot positions (Figure 17). Dot positions are defined by up to 31 seven-bit words, which control the actual tracing of the character, and the outputs of seven binaries, used to position characters on a line.

3.44   The memory consists of a matrix of 112 transformer cores together with input and output windings. Two U sections make up a core and establish a closed magnetic circuit. The memory works on transformer action with a primary of one turn and a secondary of eight turns. Information is stored by selectively routing the transformer primaries. These primaries are on 64 flexible plastic etched circuit sheets 0.003 inches thick, one for each character. Each sheet contains two separate conductors, each

CHARACTER SHEET
TABS

PROTECTIVE STRIP
REMOVED

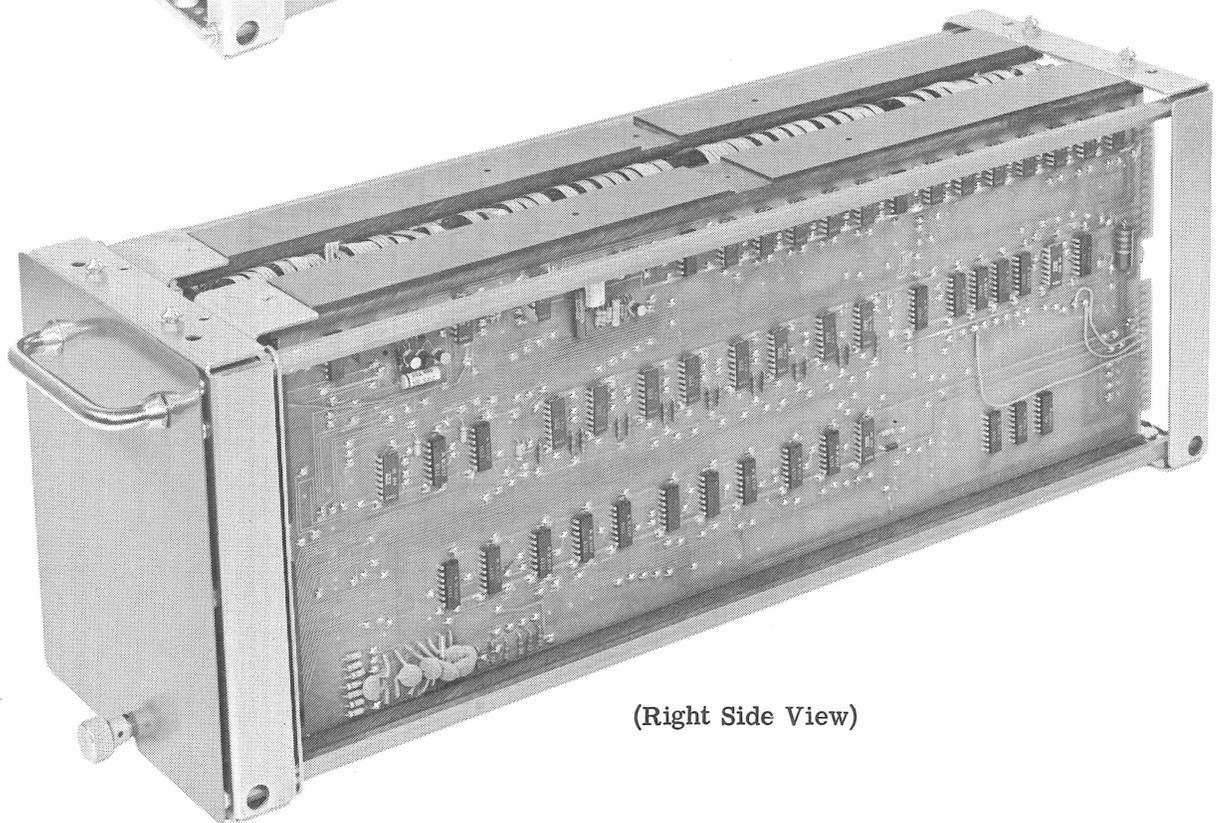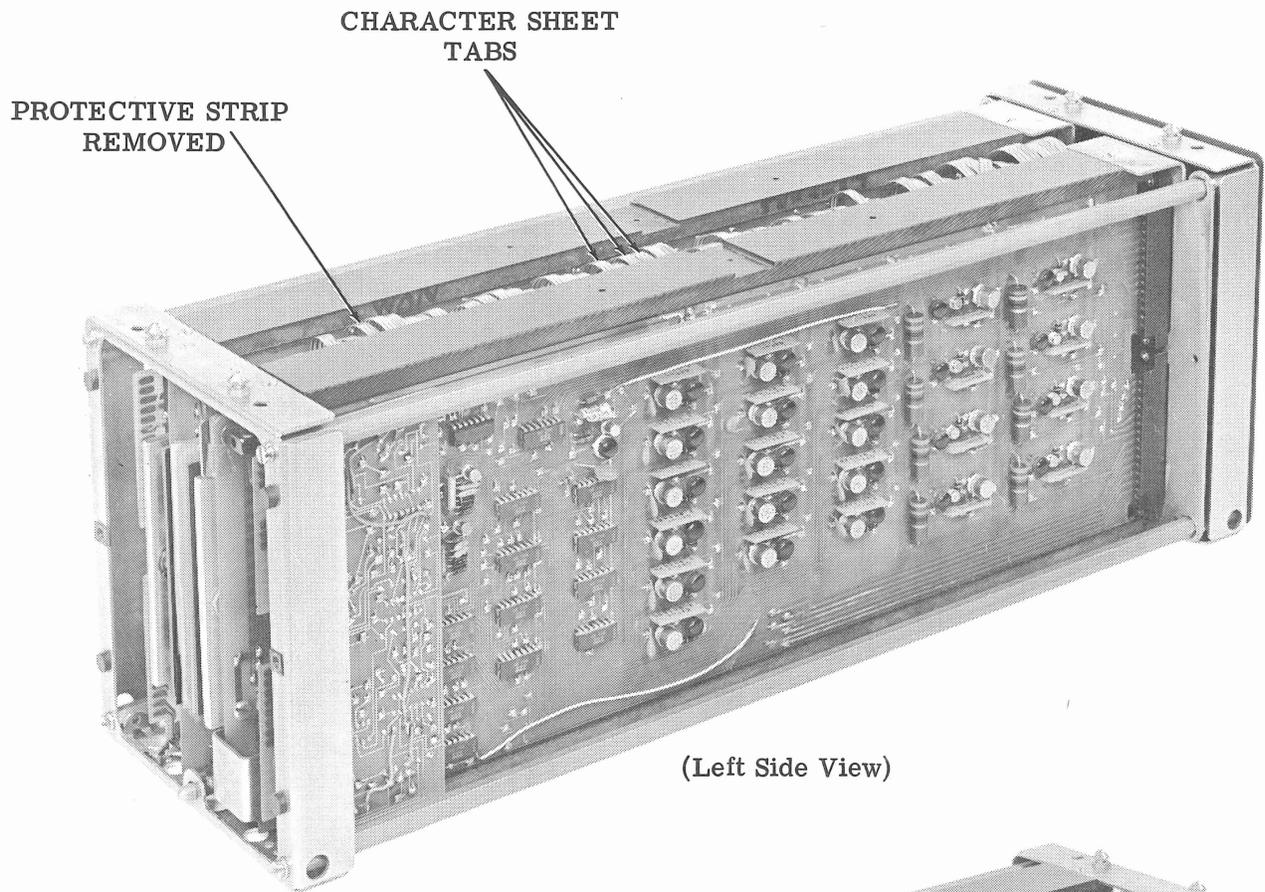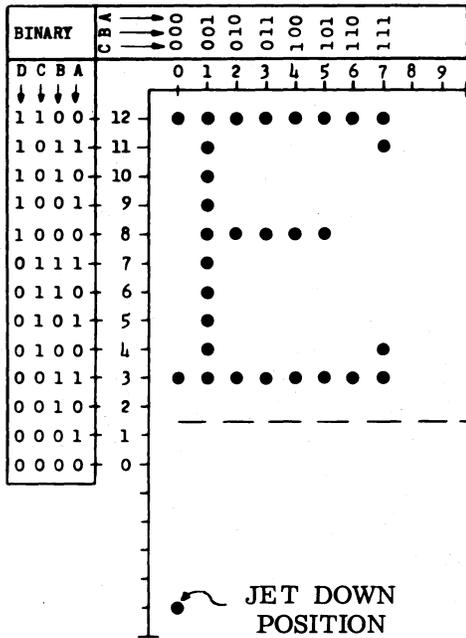(Left Side View)

(Right Side View)

Figure 16 - DAG Character Generator

Note: BINARY A is H1 or V1, BINARY B is H2 or V2, BINARY C is H3 or V3, and BINARY D is V4. The jet down position is controlled by JD and the left-right shift is controlled by L/R.
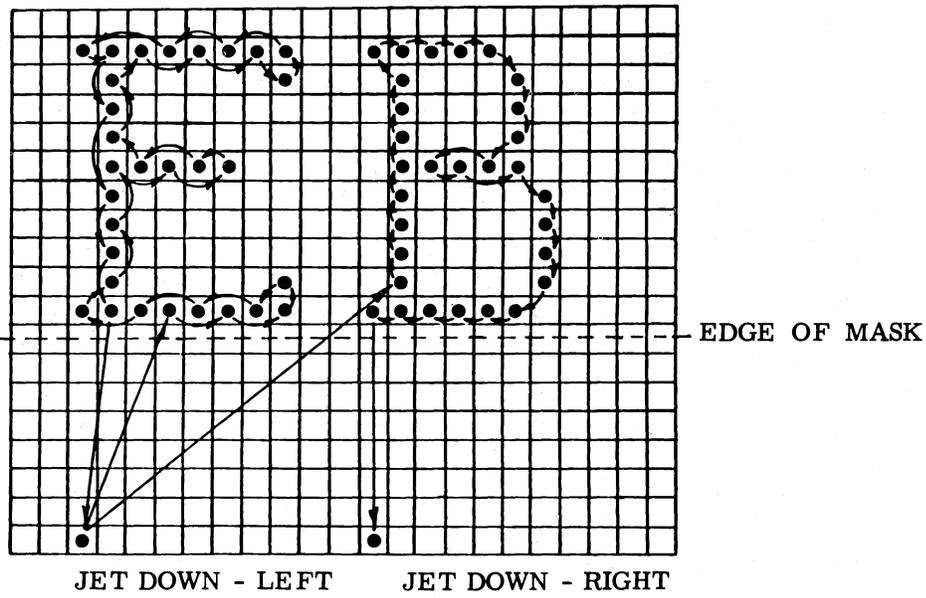
EDGE OF MASK

JET DOWN POSITION

JET DOWN - LEFT   JET DOWN - RIGHT

EDGE OF MASK

Figure 17 - Locating Dots Used to Trace Character Shapes

acting as a primary for half of a character so that the cores are scanned twice per character. In this manner, the number of cores needed to store a character is reduced from 32 times 7, or 224, to 16 times 7, or 112. A separate conductor can be routed around each leg of the U as shown in Figure 18. The secondaries are on an etched circuit card arranged in 16 groups of 7, one for each core. Each group of seven produces the information for two dots of the character (in the form of two seven-bit words).

FIRST HALF

SECOND
HALF
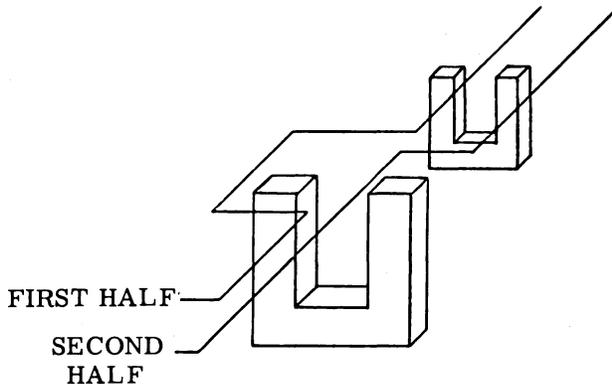
Figure 18 - Conductor Routing Through Transformer Cores

3.45   Depending on which memory program board and character sheets it contains, the memory can store up to 64 characters of ASCII, all of communications Baudot, or all of weather Baudot. The character generator code is dependent upon the code programmed in its memory; individual character sheet part numbers are the same for all characters common to all codes.

3.46   Power requirements for the character generator are as follows:

> 5.3 v - 7.3 v dc
> 41.5 v - 53.0 v dc
> 13 watts maximum power

3.47   There are two independent optional features in the character generator. The time required to feed out one line of paper when the PAPER ADVANCE button is depressed may be reduced from the standard 64 milliseconds to 32 or 16 milliseconds so that paper will be fed out two or four times as fast. Normally, CR initiates carriage return only and LF initiates line feed only, but the character generator may be programmed for simultaneous carriage return and line feed on receipt of CR (for ASCII only) or simultaneous carriage return and line feed on receipt of LF.

B.   Detailed Circuit Description

3.48   The detailed description of this unit is divided into six parts: the line feed buffer and controls; the memory input buffer and controls; the timing signals; the character positioning binaries and associated gates; the memory drivers and controls; circuits peculiar to control functions; and programming for ASCII and Baudot codes.

3.49   Refer to wiring diagrams 8252/AAA/WD (character generator schematic), 8252/AAB/WD (ASCII program board), 8252/AAC/WD (communications Baudot program board), 8252/AAE/WD (weather Baudot program board), TP322151 (MC151 input logic card), TP322150 (MC150 output logic card), TP322152 (MC152 ASCII control logic card), TP322153 (MC153 Baudot control logic card), TP303927 (EC927 ASCII program board) TP303928 (EC928 Baudot program board) TP303929 (EC929 output board assembly), and 8260WD (timing diagram).

3.50   The following discussion is directed toward ASCII operation. Therefore, seven bit input signals defining a character and a start signal must be supplied to the generator from the interface. When a character is ready to be processed, the start signal is received. This signal is referred to as the character available signal and is nominally a low 10-microsecond pulse but can be as short as 1 microsecond or as long as 300 microseconds and still perform properly. These signals are supplied by the interface as described in 3.26 and 3.27.

Line Feed Buffer and Controls

3.51   The low character available signal controls the line feed buffer, shown on sheet 2 of TP322151. It clears register ML2(5) through ML8(5) and simultaneously enables transfer gates ML2(2) through ML8(2) via a high signal generated by inverting gate ML1(13). Because the propagation time of this gate is about 10 nanoseconds, the transfer signal is high longer than the clear signal to the register is low. Utilizing this fact, one signal and one inverting gate are used to both clear and transfer information into the register. The purpose of this register is to supply the line feed mechanism with 12 milliseconds of operating time on receipt of the first line feed signal. The line feed signal is generated by any of three control characters as decoded by three gates, ML1(8), ML2(6), or ML1(6) on card MC152. These control characters are line feed, vertical tab, and form feed, respectively. The line feed signal (which is the result of a wired OR connection of the above gates) drives a line feed network on card MC150 that is described in 3.56(c).

Memory Input Buffer and Controls

3.52   This same low character available signal triggers a four-millisecond monostable network, established by diodes CR1 and CR2 and transistor Q1, by setting a dc

flip-flop ML17 (11, 6) on MC151 that reverse-biases diode CR3, permitting capacitor C1 to charge to the threshold of the network. When this point is reached, transistor Q1 saturates and flip-flop ML17 (11, 6) is reset. The positive-going edge of this four-millisecond signal is sensed by a differentiating network consisting of R7, C3, R8, R9, and Q3 and amplified by an emitter follower consisting of R43 and Q60. This signal, designated start of cycle, is nominally low for four microseconds and is used to clear the memory input buffer register, which consists of ML10(12) through ML16(12) on card MC151. Its transfer gates, ML2(8) through ML8(8), are simultaneously enabled by the inverted start of cycle signal (high) from gate ML1(8). The propagation time on this gate permits the transfer signal (high) to exist longer than the register clear signal (low).

Timing Signals

3.53   The start of cycle signal initiates the internal timing of the character generator. This timing consists of three monostable networks and a unijunction oscillator. There are 32 timing frames within a character interval, each of which defines the operations needed to print one dot. The first frame is initiated by the start of cycle signal, which also starts the above mentioned oscillator. The oscillator initiates the remaining 31 frames. The three monostable networks will be referred to in the following discussion as the memory control monostable, the vertical control monostable, and the horizontal control monostable.

(a)   The memory control monostable consists of ML22(12), ML17(8), CR4, CR5, CR6, C2, R4, R5, R6, and Q2 on card MC151. On receipt of the start of cycle signal (low, on pin 2) or the oscillator signal (low, on pin 1), a dc flip-flop, ML22(12) and ML17(8), is set and diode CR6 is reverse-biased. This permits capacitor C2 to charge via resistor R6 to the threshold of this monostable network, which is established by CR4, CR5 and Q2. When this point is reached, transistor Q2 turns on and flip-flop ML22(12) and ML17(8) is reset. The output signal from this network is a high 10-microsecond pulse. This signal is AND-gated, in effect, with the normal and inverted level 1 signals from the memory input buffer register via NAND gates ML1(3, 6) and inverters ML9(8, 6). Output signals memory register level 1 (MRL#1) and memory register level 1 inverted (MRL#1 bar) are thus always opposite in sign (high, low or low, high). They are supplied to the X-drivers as a sequence of 32 ten-microsecond pulses. The output of the X-drivers is used to read the memory (via program board EC927) as described in 3.55. The memory output buffer register on MC150 is also cleared as soon as the reading of the memory begins. This clear signal is propagated through three gates, ML1(3) or ML1(6), ML17(3) (on MC151), and ML29(8) (on MC150). This propagation delay is necessary to insure that signals in the vertical and horizontal registers (3.53 (b) and (c) are not disturbed by memory output buffer register.

(b)   The vertical control monostable consists of ML3(12), ML4(11), CR7 through CR9, R11, through R13, C2, and Q4, all on MC150. The control and operation of this monostable is identical to the memory control monostable. However, this pulse width is set for 20 microseconds. The output from this monostable enables the vertical register, which consists of ML41(5), ML42(10), ML44(5), and ML45(10), and inhibits its transfer gates, ML41(2), ML42(12), ML44(2) and ML45(12), via inverting gate ML29(3). This condition exists for 20 microseconds, after which these transfer gates and registers behave as simple inverters, sensing the information in the memory output buffer register for the remainder of the 250-microsecond frame.

(c)   The horizontal control monostable consists of ML3(6), ML4(3), CR4 through CR6, R8 through R10, C3, and Q5, all on MC150. Its operation is identical to the monostables described previously except that its output pulse width is 200 microseconds. This signal enables the horizontal register, which consists of ML36(10), ML38(5), and ML39(10), and inhibits its transfer gates ML36(12), ML38(2), and ML39(12), via inverting gate ML29(5). After this 200-microsecond interval, these gates and registers behave as simple inverters, sensing the information in the memory output buffer register, and the Z-driver binaries ML5 through ML8 are stepped, establishing a new word location in the memory.

Character Positioning Binaries

3.54   A ripple counter of seven binaries controls the positioning of characters on a line. These binaries are located on MC150 and designated ML11 through ML17. Their ultimate outputs to the printer drive are five group signals (A, B, C, D, and E) and seven binary signals (L/R, B7, B7 bar, B8, B8 bar, B9, and B9 bar), which together determine all 80 character positions on a line.

(a)   The last three binaries, ML15 through ML17, drive five decoding gates ML33(8), ML34(6), ML34(8), ML35(6) and ML35(8). The outputs of these gates are inverted by gates ML47(6), ML47(8), ML48(6), ML48(8), and ML49(8) and presented to the spacing drive portion of the printer drive as groups E, D, C, B, and A, respectively. They control five intervals on a line which are in turn divided into 16 character positions, determined by the last six binary signals. The five decoding gates are also controlled by a network consisting of gates ML22(6) and ML22(8) on card MC151. These two gates monitor the four-millisecond interval as established by the four-millisecond monostable, the printing interval as established by the oscillator reset gate, and a nonprint or horizontal tab mode as

established by decoders on MC152. Consequently, the five MC150 decoding gates will be inhibited during nonprint characters or intervals.

(b) The inverted output of the first binary, ML11, is coupled to the tracing drive portion of the printer drive via line driver ML30(6) as L/R, and the inverted and normal outputs of the next three binaries, ML12 through ML14, are coupled to the spacing drive portion via line drivers ML31(6), ML30(8), ML32(6), ML31(8), ML33(6), and ML32(8) as B7, B7 bar, B8, B8 bar, B9, and B9 bar, respectively. These last six binary signals determine 16 character positions which, together with the 5 group signals, define the 80-character line. L/R is used by the tracing drive to control the character position – left or right – in which one of the 40 ink jets will print. (B7 and B7 bar are also connected to vertical switches in the tracing drive.)

(c) A nonprint condition inhibits the stepping of the binaries. This print inhibit condition can be generated either by an incoming code that defines a nonprint character (and is decoded on MC152) or the operation of the paper advance network. Should either of these conditons exist, gate ML10(3) is inhibited, and binary ML9 is inhibited from stepping binaries ML11 through ML17. The source of the print inhibit signal is located on MC152 and described in 3.58(a). The paper advance network works in conjunction with these seven binaries and must have control of the binaries at all times. Therefore, should a print inhibit exist the binaries can still operate via an alternate gate ML10(11) that will be enabled when the paper advance network is triggered. This circuit is described in 3.57(a).

Memory Drivers and Controls

3.55   A matrix of 16 X-drivers and 4 pairs of Y-drivers on MC151 allows the selection of any one of the 64 character sheets in the memory. The 16 X-drivers decode bit levels 1 through 4 of the memory input buffer register. The 4 Y-driver pairs decode the last three levels of this register. Therefore, any character information in this register will select only one X-driver and one pair of Y-drivers that in turn will select only one character sheet in the memory. Each Y-driver in conjunction with an X-driver produces the information for 16 dots. Therefore, the Y-driver pair and this X-driver will produce a maximum of 32 dots necessary to print a character. When a Y-driver is enabled, its output rises to +48 volts for half the print cycle (four milliseconds). A binary, ML9 on MC150, produces the controlling signals (B5 and B5M bar) that determine what Y-driver of any Y-driver pair is to be on and for how long. The X-driver is enabled by the input signals and by a sequence of 32 ten-microsecond clock pulses from gate ML9(8) or ML9(6) on MC151, as described in 3.53(a). When an X-driver is enabled, its output is grounded and permits current to flow through one sheet.

3.56   Prior to the time the memory is to be pulsed, the Z-drivers (ML21(6) through ML28(8), MC150) have selected the word position (circuit) on the character sheet that is to be read. By pulsing the memory and then stepping the 16 Z-drivers, the information for 16 dots is sequentially read out. The control of these Z-drivers is a function of four binaries, ML5 through ML8 on MC150. As information for the positioning of each dot is read from the memory (in parallel), it is stored in the memory output buffer register ML45(3), ML44(11), ML42(3), ML41(11), ML39(3), ML38(11), and ML36(3). This information will remain in the register until the memory is pulsed again. It is then selectively applied to another set of registers. The first register stores vertical information. It consists of ML46(6), ML43(8), ML43(6), and ML40(8) and behaves as a register for only 20 microseconds from the time the memory is pulsed. After this interval, this register behaves as inverting gates monitoring the information in the memory output buffer register. Horizontal information is handled identically to vertical information, with one exception. The horizontal register, ML40(6), ML37(8), and ML37(6), behaves as a register for 200 microseconds after the memory is pulsed and as inverters for the remaining 50 microseconds of each character. A jet down signal (JD) is also supplied via NAND gate ML46(8) and diodes CR22 and CR14 – which monitors the outputs of the vertical output buffer register, the inverted vertical control monostable output from ML29(3), and the normal output of binary ML9 – and a register consisting of ML1(8) and ML1(11). These eight signals – V1, V2, V4, and V8 from the vertical register; H1, H2, and H4 from the horizontal register; and JD from ML1(8) and ML1(11) – are supplied to the tracing drive portion of the printer drive, along with L/R, B7, and B7 bar, to control the tracing of each character.

Control Function Circuits

3.57   Three circuits on MC150 control modes other than those associated with the tracing and spacing of characters. They are the paper advance circuit, the carriage return circuit, and the line feed circuit.

(a) The paper advance circuit consists of a dc flip-flop, ML1(6) and ML1(3), which is controlled by the PAPER ADVANCE button on the function strip. When this button is operated, a low signal changes the state of the flip-flop, enabling gate ML10(11) and allowing the character positioning binaries, ML11 through ML17, to step at the character rate as determined by the oscillator and binaries ML5 through ML9. By programming the input (422) of gate ML19(12) to the output of either binary ML12 (416), ML13(412), or ML14 (408), the paper advance will operate at a 16-millisecond, 32-millisecond, or 64-millisecond rate. Since gate ML19(3) is enabled and the oscillator that controls character time enabled by a signal via ML19(3) and ML3(8), binaries ML11 through ML17 will step at

the character rate (8 milliseconds) until the programmed position is located. At this instant, the line feed and carriage return networks are operated via gate ML19(11) and binaries ML11 through ML17 are reset, repeating this operation. The resetting of flip-flop ML1(1) is accomplished by the low signal from line feed driver ML20(6).

(b) A carriage return signal resets the character-positioning binaries to a quiescent state defined as the first character position on a line. The carriage return circuit consists of ML18(8), ML19(6), and ML20(8). Four inputs are capable of triggering this circuit: the carriage return or line feed signal (119), brought in if the character generator is programmed for line feed on receipt of carriage return or carriage return on receipt of line feed; the output of the carriage return decoder, ML2(8) on MC152 (123); the output of the paper advance circuit, via gate ML19(11); and the output of the automatic carriage return and line feed circuit from gate ML2(6), which senses the binary condition (normal outputs of ML11, ML15, and ML17 high) indicating that 82 characters have been received without a carriage return or line feed (two characters are lost when this condition occurs). Any of these signals will set flip-flop ML18(8) and ML19(6) and cause a carriage return by placing a low on the direct set lead, SD (pins 5), of binaries ML11 through ML17. The resetting of this flip-flop and the line feed flip-flop described in the following paragraph is accomplished by the low signal from oscillator Q1 on MC150.

(c) The line feed circuit consists of a dc flip-flop ML18(6) and ML19(8), and gate ML20(6). This circuit can be triggered by: a signal from the line feed decoder, ML1(8), on MC152 (125); the CR or LF signal (119), brought in if the character generator is programmed for line feed on receipt of CR or carriage return on receipt of LF; the output of the automatic CR/LF gate, ML2(6); and the output of the paper advance network via gate ML19(11). The output of this circuit, LF (low), is connected to the ink heater and line feed bracket assembly.

Programming for ASCII and Baudot Code

3.58 ASCII code was assumed throughout the preceding description of the character generator. This required that it contain control card MC152 and program board EC927. In a character generator for Baudot code, these components are replaced by control card MC153 and program board EC928. Operation of these code-sensitive components is as follows.

(a) The ASCII control card, MC152, decodes functions peculiar to ASCII and is used to supply a line feed signal (which also indicates vertical tab and form feed), a carriage return signal, a horizontal tab signal, and a

print inhibit signal — plus two straps to condition the input buffer into the ASCII mode. This board is connected via 45 pin connections (9 groups of 5) to input logic board MC151. Three decoders — line feed (ML1(8)), vertical tab (ML2(6)), and form feed (ML1(6)) — have their outputs connected as a wired OR gate to generate a common line feed signal. These three decoders monitor the outputs of the line feed buffer register and supply the line feed mechanism with four milliseconds of additional operation time. The carriage return decoder can be programmed to be initiated from information supplied to it from the line feed buffer register or the memory input buffer register. This is necessary in order to initiate the carriage return and line feed circuitry simultaneously should the character generator be programmed to have these two operations occur on receipt of a carriage return signal. In ASCII there are 36 nonprinting control characters which have code levels 6 and 7 spacing and one nonprinting character (delete) which has all 7 levels marking. A print inhibit signal must be generated on receipt of any of these characters to prevent the recorder from advancing to the next printing position. Horizontal tab, however, is an exception; it is not now used by the printer, so if it should be received the print inhibit signal must be suppressed so that horizontal tab is converted into space. Also, printing of the character stored in the memory output buffer register when the PAPER ADVANCE button is depressed must be inhibited. All this is accomplished by the print inhibit circuit on MC152: Gate ML3(6) detects horizontal tab and presents it to MC151 (for future use) and to gate ML3(8). The output of ML3(8) is low when levels 6 and 7 are spacing, except when the character received is horizontal tab. Gate ML4(6) inverts the output of ML4(3), whose inputs are the paper advance signal and an input reserved for future use. Gate ML5(6) and diodes CR1, CR2, and CR3 detect the delete character. The outputs of ML3(8), ML4(6), and ML5(6) are connected as a wired OR gate to produce the low print inhibit signal. The program board matrices the X and Y drivers to the appropriate character sheets.

(b) The Baudot control card, MC153, contains gates to decode the following characters: horizontal tab (ML2(6)), line feed (ML2(8)), carriage return (ML1(6)), a letters (ML3(6)) or figures (ML3(8)) shift, and a print inhibit signal generated by these nonprint characters (ML4(8) and ML4(6)). All of these outputs, with the exception of the output for a letters or figures shift and the second line feed decoder, initiate other logic networks already described in 3.57. A signal from decoder ML3(6) (letters shift decoder) will drive the output of flip-flop ML15(6) on MC151 low and the output of flip-flop ML16(6) high. This combination will select the Y-drivers associated with the code field for letters. The detection of a signal from decoder ML3(8)

(figures shift) conditions the above mentioned flip-flops in the opposite states, and the Y-drivers associated with the code field for figures are selected.

PRINTER DRIVE

3.59   The printer drive converts digital electronic signals from the character generator into high voltage analog signals for printing characters with the recorder and for moving paper through the paper transport. The printer drive is housed in the DAD module (Figure 19).

A.   General

3.60   The printer drive receives 11 input signals from the character generator to determine in which column (out of 40) printing will take place: six outputs of a three-stage binary counter and five group signals. It also receives 11 signals to control the tracing of character shapes: four for vertical information, three for horizontal information, one left-right shift, and three vertical amplifier selection inputs. These are all 0 to +6 volt digital signals. An input for control of the power supply is also required.

3.61   Output signals consist of 40 valving signals (+550 v dc) of which only two adjacent ones are energized at any one time, from the spacing drive, and six high voltage analog signals (four vertical, two horizontal), from the tracing drive. Drive signals are independent of the character generator used.

3.62   Power requirements for the printer drive are as follows:

-12.0 v dc	$\pm$1.2 v at 0.25 amp	
+6.0 v dc	$\pm$0.6 v at 0.25 amp	
+6.3 v ac	$\pm$10%	at 1.0 amp
+30 v dc	$\pm$3.0 v at 0.25 amp	
+48 v dc	$\pm$4.8 v at 0.10 amp (front interface)	
+120 v dc	$\pm$10	v limited to 12 ma (3 inputs)
+550 v dc	$\pm$20	v limited to 3 ma
+3800 v dc	$\pm$200	v limited to 5 ma (6 inputs)

3.63   There are no options in the printer drive.

B.   Detailed Circuit Description

3.64   The detailed description of this unit is divided into two independent parts: the spacing drive, MC145, and the tracing drive, MC146.

3.65   Refer to wiring diagrams TP322145 (MC145 spacing drive), TP322146 (MC146 tracing drive) TP303925 (EC925 resistor divider card), 8254WD (printer schematic), and 8260WD (timing diagram).

Spacing Drive

3.66   The spacing drive converts six binary inputs and five group inputs from the character generator into a +550 v dc signal which is applied to the valving electrode of the column to be printed and to the next valving electrode across the line.

3.67   Operation of a typical valving circuit is as described below. Circuit number one is energized by applying a signal of greater than +2.6 volts on pins D313 (group A), D306 (9 bar), D308 (8 bar), and D310 (7 bar). This causes inputs 9, 13, 12, and 10 of ML20 to be at a voltage greater than +2.6 volts. The output, pin 8 of ML20, will go to 0 volts. This will cause reed relay RR40 to be energized through diode CR119. A low output at pin 8 of ML20 will also allow reed relay RR38 to be energized through diode CR114. When RR40 is energized, it couples +550 v dc through current-limiting resistors R79 and R159 to D429. D429 corresponds to valving electrode 1. When RR38 is energized, it couples +550 v dc through current-limiting resistors R75 and R155 to D425, which corresponds to valving electrode 2. The purpose of the current-limiting resistors is to limit the inrush current to the stray capacitance to a safe limit for the reed relay (about 2 ma). When a reed relay is not energized, its output is returned to ground through a high resistance. This resistance gives the stray capacitance a path through which it can discharge. R80 and R160 form this return path for RR40 and R76 and R156 form the path for RR38.

3.68   When pin 8 of ML19 is low, RR38 and RR36 are selected and valving electrodes 2 and 3 are raised to +550 v dc. As the decoding proceeds the selected reed relay and the one ahead of it are always energized at the same time (8260WD, sheet 4). There is a diode connected to the output of each reed relay driver which is returned to ground through a 7-volt zener diode (CR121). Its purpose is to prevent the output of the driver from exceeding +8 v dc because of the inductive kick from the reed relay coil. There is also a pi filter network, made up of C1, C2, and L1, in the +6 v dc supply to the reed relay coils. This is used to filter out any noise from the contacts which may be coupled into the coil.
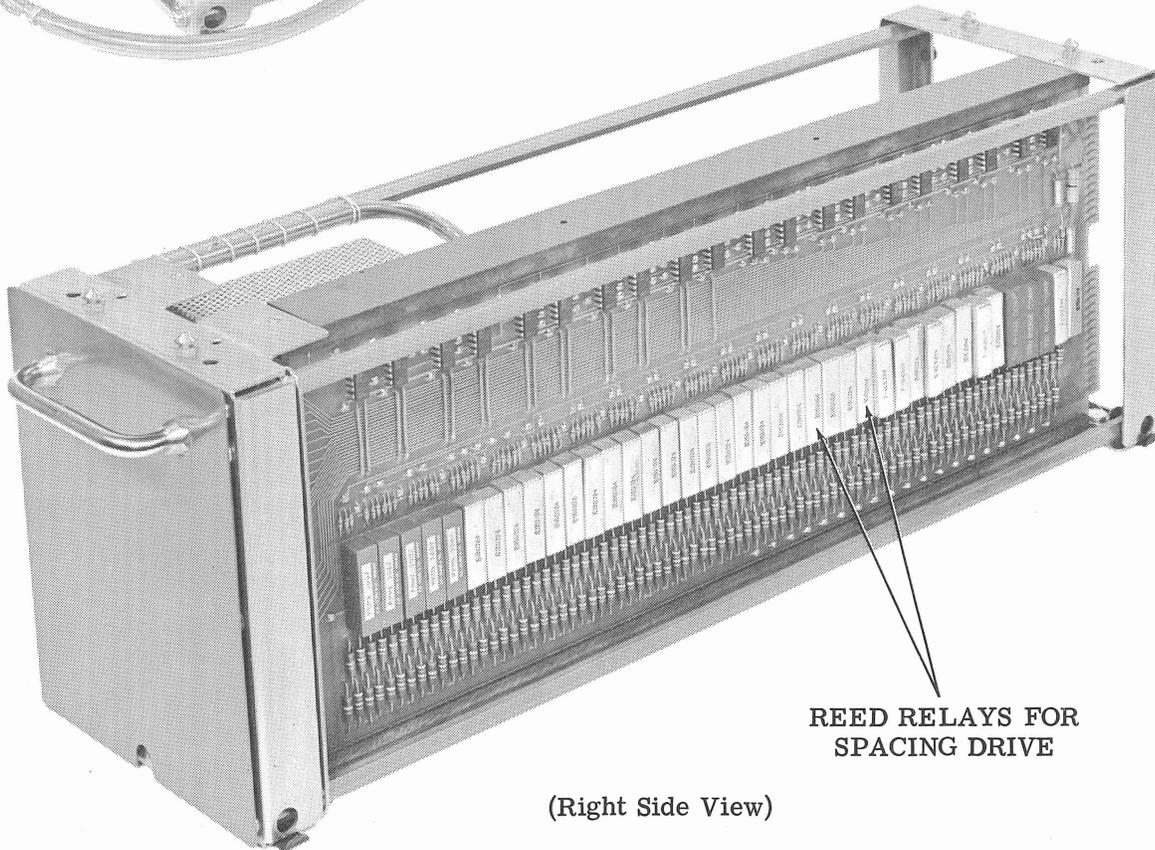
Tracing Drive

3.69   The tracing drive consists of four parts: the digital-to-analog converters, the high voltage amplifiers, the relay driver-over-voltage protection circuit, and two power supplies.

3.70   Digital-to-Analog Converters: Eleven digital signal inputs are used to produce three analog signals (X1, Y1, and Y2) which are used to trace the shape of a character (Figure 17). There are three horizontal binary inputs and one left/right control input (H1, H2, H4, and L/R on pins C229, C227, C225, and C223 respectively) which

PENTRODE TUBES FOR TRACING DRIVE
HIGH VOLTAGE AMPLIFIERS
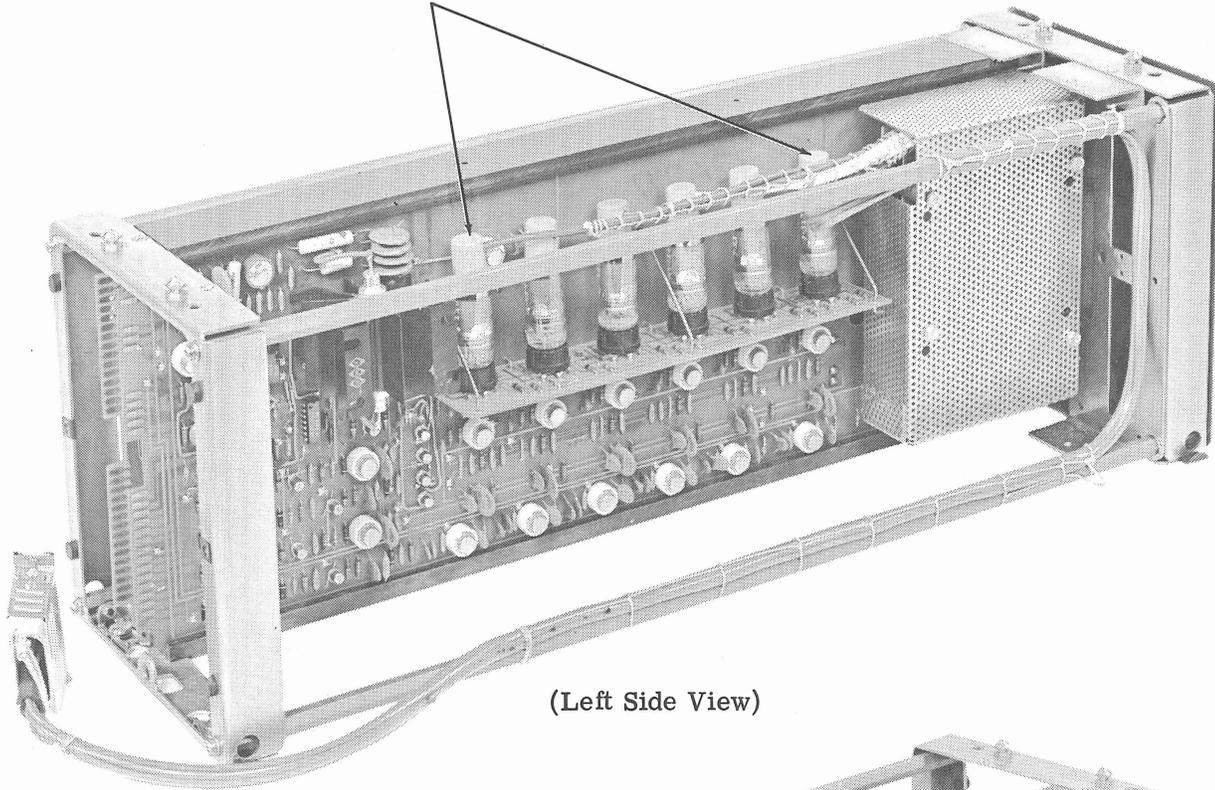
(Left Side View)

REED RELAYS FOR
SPACING DRIVE

(Right Side View)

Figure 19 - DAD Printer Drive

control four NAND gates consisting of Q15, Q16, Q17, and Q18 and associated components. These gates, in conjunction with their collector load resistors (R92, R94, R96, and R98), form digital current sinks weighted according to the binary level they represent; ie, the current sink corresponding to the 1 level is a 0.1 ma sink, the one corresponding to the 4 level is a 0.4 ma sink, and the one corresponding to the L/R level is a 1.05 ma sink. The gates are either on or off as determined by the input signals. The current levels are determined by the collector load resistors and the input voltage to the inverting input of the operational amplifier (OP 17-2). The sum of the currents through these current sinks is the input current to the operational amplifier. In order to maintain a constant differential (0 v) across the two inputs (OP 17-2 and OP 17-3), this input current is matched by a current through the feedback resistor (R100) and level resistor (R104). The output voltage (OP 17-6), then, is proportional to the sum of the current sources, and hence is the analog equivalent of the digital inputs (8260WD, sheet 3).

3.71 The level is determined by the feedback resistor (R100) and level resistor (R104). At this level all of the current sources are off and the output voltage (at OP 17-6) will go to a level such that the voltage at the junction of the feedback and level resistors will maintain the constant differential (0 v) across the two inputs of the operational amplifier. The feedback resistor determines the size of each step. The input resistor (R102) connects the noninverting input of the operational amplifier to a reference voltage. This reference voltage determines the crossover voltage level, which will be between 6.400 and 7.333 volts. The analog output of the horizontal digital-to-analog converter is coupled directly to the horizontal high voltage amplifiers. Each set of deflection electrodes on the recorder is used to print two characters, left and right. In order to do this, there must be a shift in the horizontal deflection voltage between printing levels for a left character and printing levels for a right character. This shift is introduced in the horizontal digital-to-analog converter by a NAND gate controlled by the L/R signal, pin C223, from the character generator. This input is treated in the same manner as changes in the binary inputs, which produce steps in the output voltage.

3.72 There are four vertical binary inputs and three control inputs that control NAND and field-effect transistor (FET) gates respectively (V1, V2, V4, V8, B7, B7 bar, and JD at pins C221, C219, C217, C215, C213, C207, and C222). The vertical digital-to-analog converter is the same as that of the horizontal digital-to-analog converter with one exception: the left-right shift signal (L/R) is replaced by a number 8 binary level that represents a 0.8 ma sink.

3.73 The analog output of operational amplifier OP 16-6 is fed to the inputs of two vertical switches, Q7S and Q9S. The purpose of these switches is to switch the analog signal to one of two sets of vertical high voltage amplifiers and also to introduce the jet down signal. The two

sets of vertical high voltage amplifiers (V1 - V2 and V3 - V4) are connected to alternate sets of vertical deflection electrodes on the recorder through the power supply. Since two valving electrodes are on at one time, it is necessary to switch the vertical analog information from one set of vertical high voltage amplifiers to another during printing. It is also necessary to enable printing by only one set of deflection electrodes at a time. To do this, the ink is deflected down below the mask on the recorder for the nonprinting electrodes. The level needed to cause this is introduced in vertical switches Q8 and Q10 (8260WD, sheet 3). Refer to Section 592-820-110 for details of recorder operation.

3.74 The vertical switches are controlled by a binary output signal, its complement, and the jet down signal (B7, B7 bar, and JD at pins C213, C207, and C222) from the character generator. Each vertical switch is turned on or off by these signals via the FET gages. Each vertical switch is composed of a two-channel FET commutator. For the first vertical switch, one channel is for the digital-to-analog signal Q7, controlled by the normal (B7) control signal, and the other channel is for the jet down signal (JD) Q8, controlled by the inverted (B7 bar) control signal. In the second vertical switch the digital-to-analog channel Q9 is controlled by the inverted (B7 bar) control signal and the JD channel Q10 is controlled by the normal (B7) control signal.

3.75 High Voltage Amplifiers: The high voltage amplifiers are operational amplifiers with a gain of 2200. The high voltage output stage is a tube amplifier stage using a pentode tube. The plate load resistors are located in the high voltage power supply. The output voltage is coupled to a feedback divider network which is accurate to +0.50 percent. For a vertical amplifier the divider output voltage is 1/201 of the input voltage. The output from this divider is connected to the noninverting input of the operational amplifier OP2. A typical amplifier is shown in Figure 20. This operational amplifier has unity gain, in noninverting, and is an impedance transformer. Therefore, the operational amplifier output is equal to the feedback voltage for the high voltage amplifier.

3.76 The input for an inverting high voltage amplifier is applied at A1. The feedback resistor R3 is equal to R1 but effectively, a feedback resistor of 2200 times is present due to the feedback divider network. A reference voltage is applied at A2 to ensure the crossover voltage level of the high voltage deflection output signal. Operational amplifier OP1 is an inverting amplifier with a gain of 2200 and is used to cathode modulate the high voltage output stage. The high voltage output is taken from point A3. An inverting high voltage amplifier is used to drive the vertical lower electrode (the left electrode for the horizontal) on the recorder. (See 8260WD, sheet 2.)

3.77 The input for a noninverting high voltage amplifier is applied at A2. The crossover level of the output is controlled by the crossover level of the input. The

remainder of the circuitry is the same as that for an inverting amplifier. The noninverting high voltage amplifier is used to drive the vertical upper electrode (the right electrode for the horizontal) on the recorder.

3.78   Relay Driver — Overvoltage Protection Circuit: To prevent possible damage to the recorder, the deflection signals at the feedback follower outputs are sensed via an OR gate (CR7 through CR12) for an over-10-volt condition. The sensed levels are tied to the inverting input of differential amplifier OP 13-2. With the noninverting input tied to a 10 volt reference voltage (OP 13-3), the output of the differential amplifier will be high when the inverting input is less than 10 volts. When the inverting input goes higher than 10 volts, the output goes low causing the output (8) of dc flip-flop ML1 to go low. The output of the dc flip-flop is used to control two power drivers. One driver is used to turn off the READY indicating lamp (via CR15). This driver can be controlled by an alternate input signal at C201. The other drive is clamped in the off condition at its input to the output stage (collector of Q2) for overvoltage conditions, causing all motors and high voltage to turn off. This second driver is normally controlled by an input signal (at C209 or C211) from the interface circuitry for automatic turn-on. The outputs (C203 and C205) can sink up to 300 ma and withstand 60 volts. The dc flip-flop is reset from the READY button on the function strip. R60 and C51 are used to insure that the flip-flop output, ML1(8), is high after power turn-on.

3.79   Power Supplied: The low voltage reference supply on MC146 produces the required reference voltages from the +30 v dc and the -12 v dc outputs of the high voltage supply (DAPS). Two voltages, +18 v dc and -6 v dc, are produced from the +30 v dc and -12 v dc inputs respectively. These voltages are zener-regulated at 200 ma. Two voltage-dropping resistors (R89 and R90) are used to drop the voltage from +30 v dc to +18 v dc and from -12.0 v dc to -6 v dc. Zener diodes CR23 and CR24 are used as the regulators. These voltages are the supply voltages for the operational amplifiers.

3.80   By the use of a zener reference diode (CR25) and an operational amplifier (OP15), output reference voltages of +12.000 v dc, +10.000 v dc, +9.500 v dc, +7.000 v dc, +6.750 v dc, +6.200 v dc, and +4.000 v dc are produced. The zener diode provides a reference voltage at the noninverting input of the operational amplifier. It is biased by resistor R105 connected to the output, which is the most stable voltage source available. Part of the output voltage, the amount determined by the variable divider (R106, R107, and R108) at the output, is fed back to the inverting input of operational amplifier OP15. Hence, the output voltage will stabilize at a value at which this feedback voltage equals approximately the zener reference voltage. By adjusting

potentiometer R107, the output can be regulated within +0.5 v and is set so that the output is 12.000 +0.050 volts. A resistor divider network (R109 - R115) produces the remaining reference voltages. The divider current is approximately 10 ma, which is much greater than the load currents, so regulation is not affected by the load currents.

POWER SUPPLY

3.81   The power supply furnishes regulated multivoltage dc outputs for the other modules of the set. Both low and high dc voltages plus three ac voltages are supplied. The power supply is housed in the DAPS module (Figure 21).

3.82   The power supply receives 117 v ac, 60 Hz from the line and transforms, rectifies, and filters it to supply +3900 v dc, +550 v dc, +120 v dc, +48 v dc, +30 v dc, +6 v dc -12 v dc, and 167 v ac peak. It fuses the 117 v ac (nominal) line voltage and supplies it unchanged, and it steps down the line voltage to supply 6.3 v ac rms.

3.83   The two high voltage outputs are supplied to the printer drive module, where +550 v is switched to two adjacent valving electrodes (out of 40) and +3900 v is connected to the plates of the six high voltage amplifiers used in tracing character shapes (the plate load resistors for these amplfiers are located in the power supply). Of the low voltage outputs, +120 v is connected to the screen grids of the high voltage amplifiers in the printer drive; +48 v is connected to the interface (for the control panel and a connection to the printer drive) and the character generator (for the X-drivers, Y-drivers, and Z-drivers); +30 v is connected to the printer drive (to produce +18 v for internal use) and the ink heater and line feed bracket assembly (to drive the paper transport escapement magnet drivers); +6 v is connected to all modules for use of the logic gates; and -12 v is connected to the interface (for the data set and data set control and receive distributor control cards) and the printer drive (to produce -6 v for internal use). The ac voltages have the following uses: 6.3 v ac is used to heat the filaments of the high voltage amplifier tubes, 117 v ac is used for the data set, the paper transport motors, the recorder ink heater, and the discrete calling generator motor (if present), and 167 v ac is presented to an auxiliary power supply which is part of the paper transport to be converted to +10,000 v dc for the platen, +5000 v dc for the recorder mask, and -2500 v dc for a regulator which supplies -1900 v dc to the recorder manifold.

3.84   In addition to the power circuitry the DAPS module also contains the AUTO ON relay and four other relays which indicate that the high voltage is capable of turning on or is on (see 3.10 and 3.11).
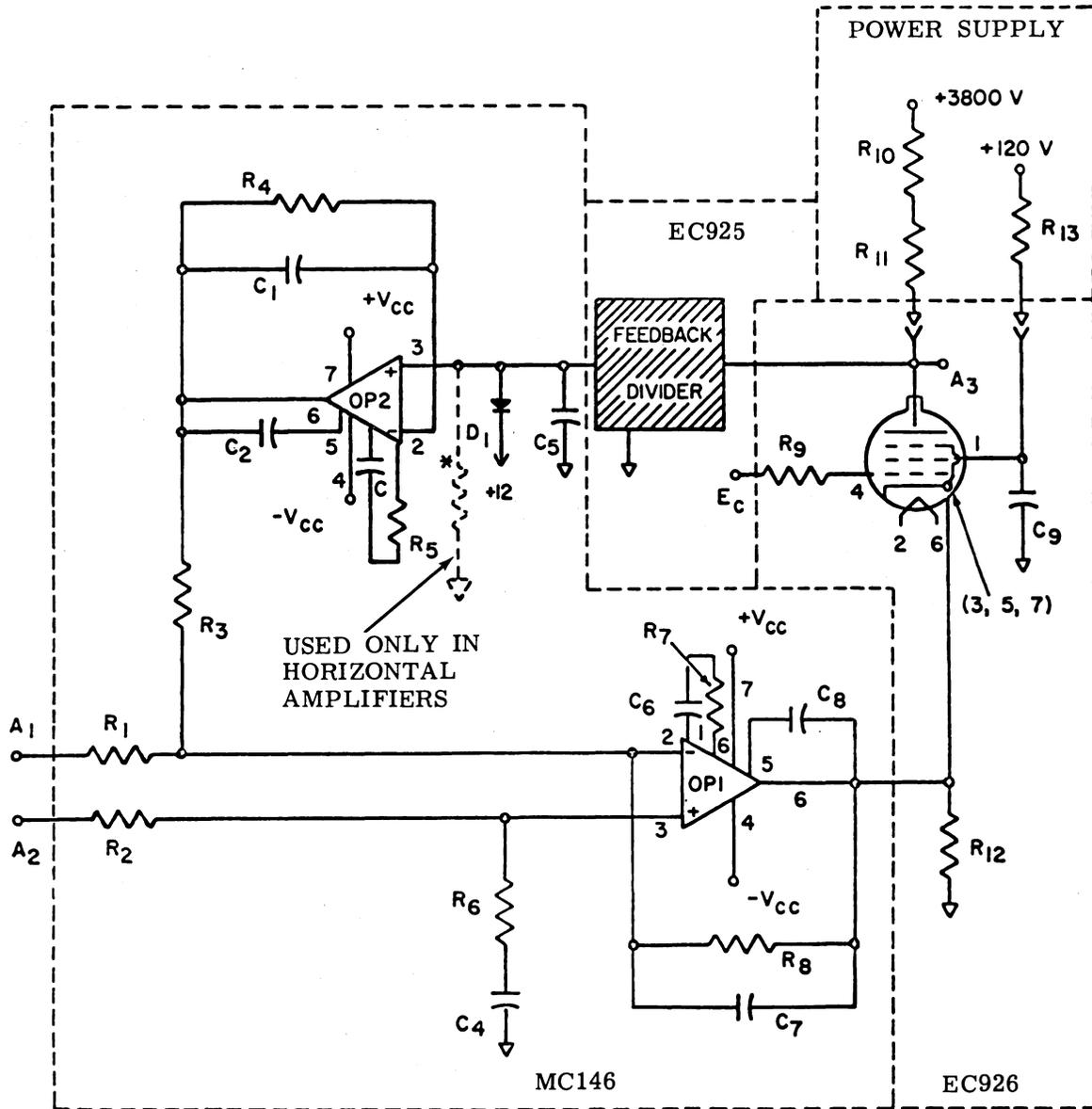
Note: The operational amplifiers in this figure correspond to those in the six high voltage amplifiers as follows:

AMPLIFIER	OP1	OP2
V1U	OP2 (noninverting)	OP1
V1L	OP4 (inverting)	OP3
V2U	OP6 (noninverting)	OP5
V2L	OP8 (inverting)	OP7
HR	OP10 (noninverting)	OP9
HL	OP12 (inverting)	OP11

Figure 20 - Typical High Voltage Amplifiers With Operational Amplifiers for Vertical and Horizontal Deflection Electrodes

HIGH VOLTAGE ON INDICATOR
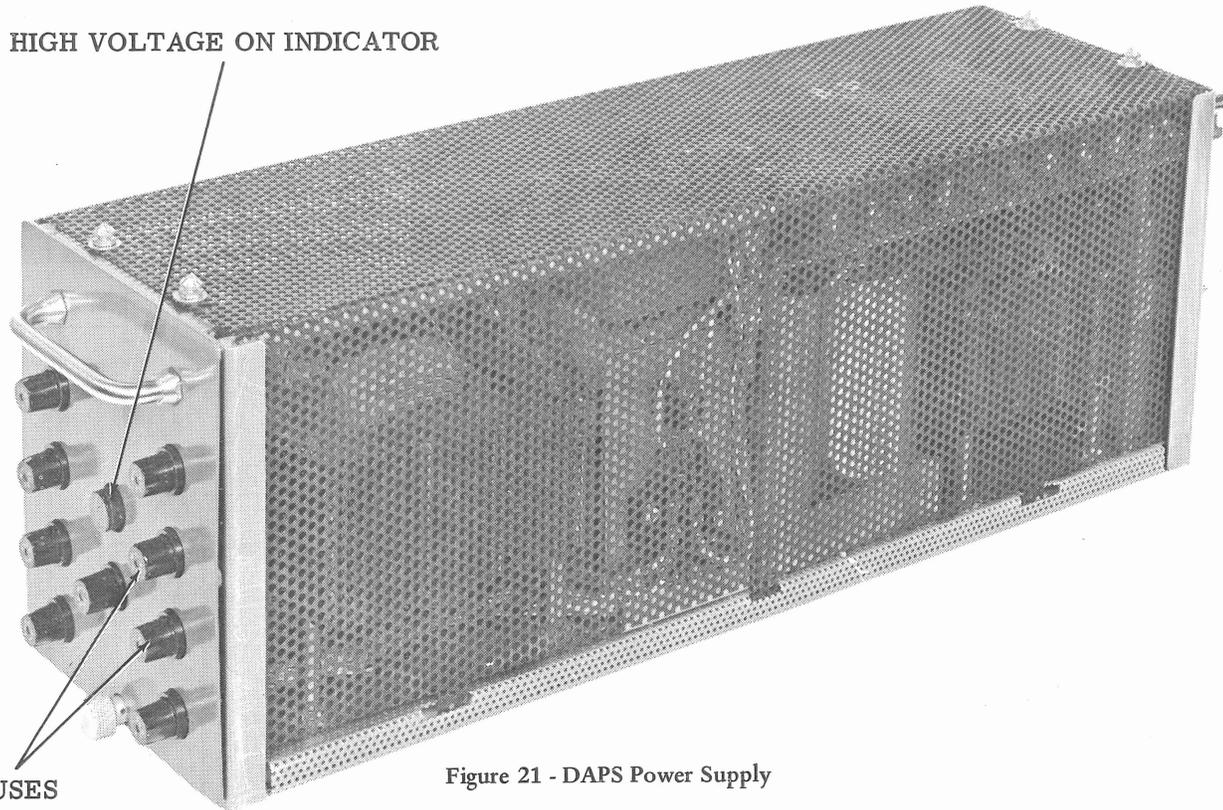
FUSES

Figure 21 - DAPS Power Supply
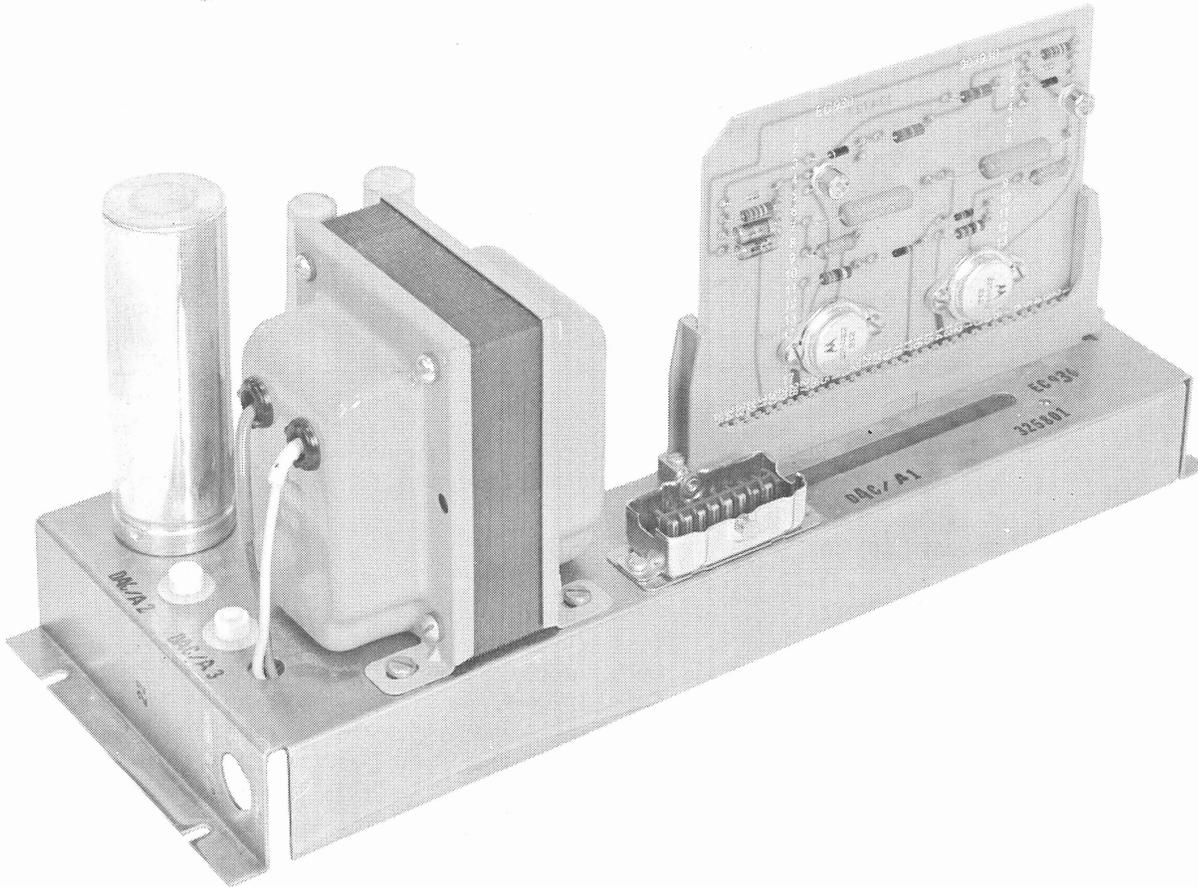
Figure 22 - Ink Heater and Line Feed Bracket Assembly

3.85   Voltage and current ranges are as follows:

+3600   v dc to +4000   v dc at 0   to 30   ma
+530   v dc to +570   v dc at 0.0 to 2.6 ma
+90   v dc to +130   .v dc at 0   to 6   ma
+46.5 v dc to   +53.0 v dc at 0.0 to   1.0 amp
+25   v dc to   +39   v dc at 0.0 to 2.5 amp
+5.3 v dc to   +7.0 v dc at 0.0 to   3.0 amp
-10.5 v dc to   -13.5 v dc at 0.0 to   0.5 amp
164 v ac peak to 171 v ac peak at 0 to 85 ma
105 v ac rms to 130 v ac rms at 0.0 to 0.5 amp
5.8 v ac rms to 7.5 ac rms at 0 to 2 amp

3.86   Nine labeled fuses and red high voltage on indicator lamp are mounted on the module faceplate.

INK HEATER AND LINE FEED BRACKET ASSEMBLY

3.87   The ink heater and line feed bracket assembly (TP325801) has two functions: (a) It supplies current for the recorder ink heater and ink pump, and (b) it contains the paper transport line feed magnet drivers and filter assembly. The assembly is mounted on a bracket 5-1/2 inches wide at the rear of the set and 2 inches wide at the front, 13-1/2 inches deep, and 6 inches high (Figure 22). This bracket is located above the modules to the left of the data set (on the same shelf) and is screwed to the cabinet frame.

3.88   The ink heater and line feed bracket assembly receives +30 v dc for the line feed magnets and 117 v ac for the ink heater. Upon receipt of the +6 v to 0 v transition line feed (LF) signal from the character generator, the assembly switches +30 v to the magnets, permitting the transport to feed one line of paper. (Refer to wiring diagrams TP303930 and 8254WD.) The 117 v ac is continuously transformed to 26 v ac and supplied to the recorder to heat the ink and drive the vibrating ink pump.