HIGH SPEED TAPE RECEIVER WITH RADIO FREQUENCY INTERFERENCE (RFI) SUPPRESSION FOR THE MULTIPLE ADDRESS PROCESSING SYSTEM (MAPS)

DESCRIPTION AND THEORY OF OPERATION

CONTENTS PAGE

1. GENERAL

1.01 This section provides a general description and theory of operation of radio frequency interference (RFI) suppression on the high speed tape receiver. It is used with reference to the standard (MAPS) literature for additional information relating to certain modules and components. Circuitry in this section reflects the new features added to the later models of the master and supplementary senders and rfi suppression. Functional operation of the high speed tape receiver is unchanged.

1.02 The basic purpose of rfi suppression as applied to teletypewriter equipment is to provide shielding to suppress electrical field radiation from 1 kilo hertz to 1 giga hertz. Signal, clock, and electrical power inputs and outputs are the same as described in the standard MAPS sections.

2. DESCRIPTION

2.01 The new parts added to the tape receiver consist of a conduit plate, junction box assembly, screens and frames, capacitors, ground strap, and wiring.

2.02 The conduit plate has three 3/4 inch knockouts for clock and signal cables, and a 3/4 inch opening for ac input conduit connectors. The junction box consists of a six terminal board for ac input connections, six 0.47 microfarad bypass capacitors, and wires to connect to the existing input terminal board.

2.03 Wire screens, and metal frames are attached in back of the plastic windows, providing shielding protection while maintaining visibility of the DRPE punches and tape feeding mechanisms (Figure 1). A ground strap provides a direct ground connection between the conduit plate and cabinet frame.

2.04 Each magnet driver card (Module C) is protected by an 0.02 microfarad capacitor connected across the output to suppress noise in the driver circuits.

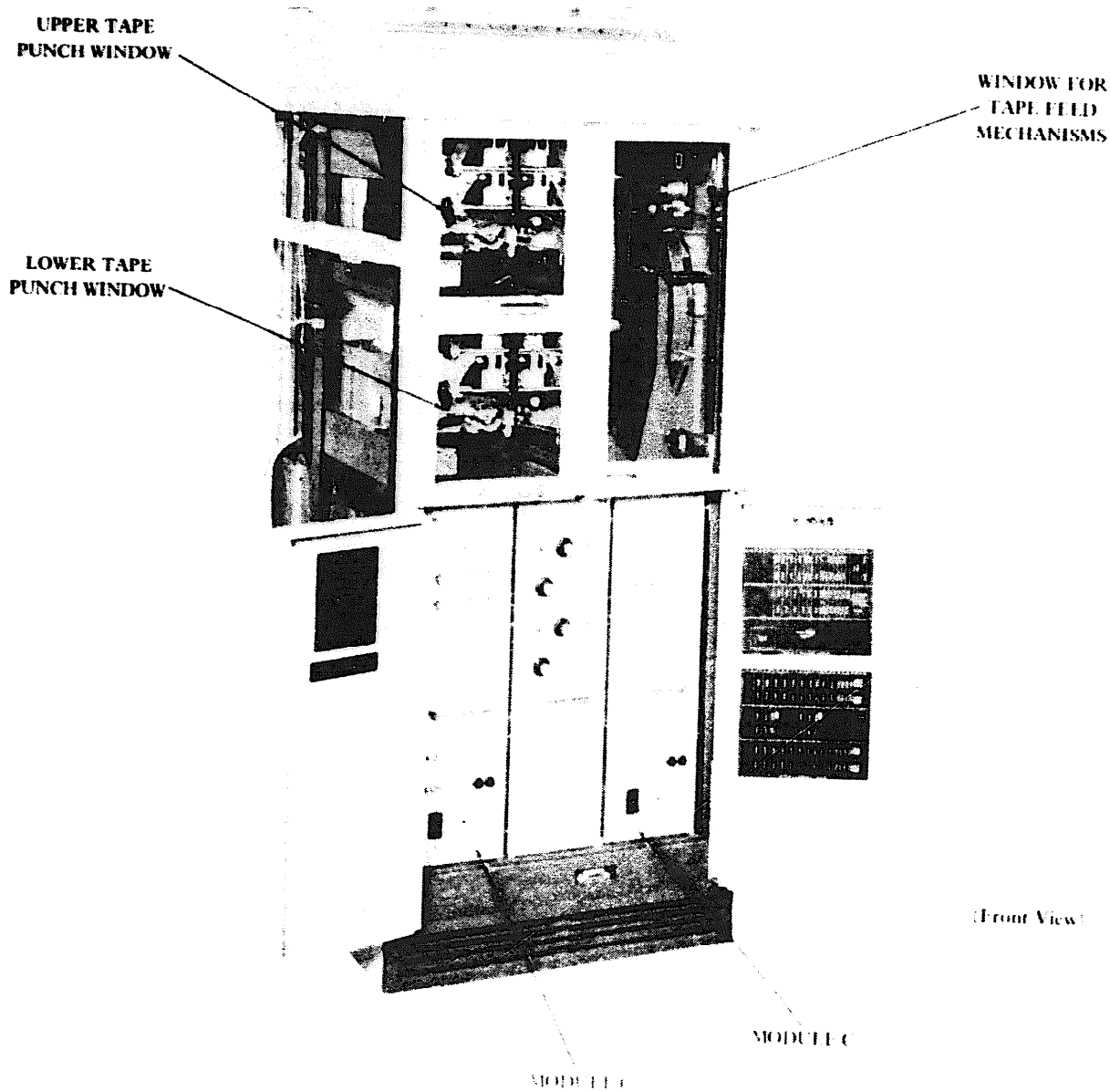


Figure 1 High Speed Tape Receiver

3. THEORY OF OPERATION

GENERAL

3.01 A detailed description of each circuit card is included in the drawing covering the card. The number of the drawing is the same as the part number of the card. The card part number and drawing number is obtained from the EC number of the card by deleting the prefix EC and adding a prefix of 172 for EC300 through EC499, 177 for EC500 through EC599, and 303 for EC600 through EC699. For example, the drawing number for EC359 is 172359, the drawing number for EC690 is 303690. Terminal board cards have the prefix TB, part numbers and drawing numbers for these cards are obtained by deleting TB and adding the prefix 149. For example, the drawing number for TB172 is 149172.

3.02 The equipment voltage levels are of three types:

(a) +6 volts, -6 volts on input and output leads

(b) 0 volt, -6 volts internally

(c) 0 volt, -5 volts on some internal leads, these leads are identified by a shaded corner in the logic symbol from which they originate.

The dc coupled inputs to logic elements are shown as half arrow heads. Full arrow heads are reserved for ac coupled (pulse) inputs.

3.03 The most commonly used logic element is the NOR element, identified by the designation LA within the logic symbol. The output of this element is negative if any input is at 0 volt. The output is 0 volt only if all inputs are negative. A special input to a NOR element, identified by an arrow entering a corner of the symbol, allows the addition of extra logical inputs to the element. The same results can be obtained by connecting two or more elements together to obtain more inputs plus greater load-driving capability.

3.04 The flip-flop element is symbolized by a rectangular box with a diagonal line across the lower half. The operation of this element is similar to that of a standard flip-flop, for example EC671, which contains priming inputs (half arrows) and setting inputs (full arrows). Arrows entering the upper half of the symbol designate prime 1 inputs, and arrows entering the lower half of the symbol designate prime 0 and set 0 signals.

3.05 An arrow entering the center of the symbol implies that the set 1 and set 0 inputs are connected together. If no priming inputs are shown this indicates that the prime 1 input is connected to the inverted output (lower half of symbol). This also indicates the prime 0 input is connected to the normal output (upper half of symbol). A flip-flop connected this way is called a complementing flip-flop or binary counter. Each input pulse reverses the condition of voltages on the normal and inverted outputs.

3.06 A pulse amplifier logic element is identified by a square box with the letters PA and a full arrow head input symbol. This element produces a pulse of approximately 2 microseconds duration whenever the input goes negative. When both inputs to this element are used, a pulse is produced only when both inputs are negative.

3.07 A power amplifier element is shown as a trapezoid symbol with the letters PA. This element has two inputs and can perform the NOR function. It has about three times the load-driving capability of an ordinary NOR (LA) element.

3.08 The delay element is symbolized by a square box with the letters DY. This element can be used as either a one-shot or a free-running multivibrator. Those used as one-shot delay elements have the pulse duration indicated. Those used as free-running multivibrators have the operating frequency indicated.

3.09 The input element translates the input polar signals (+6 volts and -6 volts) to the neutral (0 and -6 volt) signals used internally. The output element translates neutral signals to polar signals. The punch driver elements are described in Section 592-803-100TC.

3.10 The receiver is designed to accept both serial and parallel input signals. Serial signals may be synchronous or start-stop, and may represent 5-, 6-, 7-, or 8-level codes. They may contain from 5 to 16 units (bit times) per character interval. The signals may be received with one or more of the information bits inverted or interchanged in time sequence.

3.11 The CODE LEVEL and UNITS PER CHARACTER INTERVAL switches allow selection of the number of code levels to be used and the number of units per character. A strapping card controls the selection of bit inversion and bit sequence. When more than 9 units are received per character, the units over nine are ignored by the receiver.

3.12 The interconnecting cable between the receiver and its external signal source contains the following leads:

(a) Auxiliary data input (8 leads-parallel)

(b) Auxiliary sample input (parallel)

(c) Data input (serial)

(d) Clock input (serial)

(e) Urgent traffic input

(f) Bit output (8 leads-parallel)

(g) Character available output

(h) Circuit ground, +6 volts and -6 volts

(i) Frame ground

(j) Alarm output (3 leads)

CIRCUIT DESCRIPTION

3.13 A block diagram of the receiver is shown in Figure 2. The counter recognizes character boundaries in incoming serial data by counting the number of units in a character interval. The counter control permits selection of the number of units per character interval and provides for synchronizing the counter with the data. The serial-to-parallel converter stores incoming data bits until a complete character has been received. It includes storage for one character in addition to the character currently being received.

3.14 The punch drive circuits select the data to be punched and control the operation of the punch. The tape handling and alarm logic detect trouble, and alarm conditions, such as low tape, end of tape, tight tape, no tape, and full chad bin. The control panel contains the various controls used by the operator, and the indicators advise the operator as to the condition of the equipment. The reperforator, power supply, and circuits which distribute ac power to the various components of the set are not shown in Figure 2.

3.15 All indicator lamps in the equipment are controlled by relay contacts or by switches. The controlling contacts are shunted by 150 ohm resistors. These resistors allow a small amount of voltage across the lamp filaments keeping them warm but not enough to allow the lamp to light visibly. This decreases the initial surge of current, which increases the life of the lamps and the controlling contacts.

3.16 All relay windings are shunted by diodes which prevent voltage spikes from being generated when the relays are de-energized. The operator control switches are momentary in action, except BUSY OUT and POWER which are alternate action, push on, push off.

PUNCH DRIVER

3.17 The punch driver mechanisms and electrical components are described in detail in Section 592-803-100TC. The operation of the punch driver circuits are described in the following paragraphs. Refer to 7746WD, Sheet 4.

3.18 The input stage of a driver element is through a flip-flop. Pin 15 is a priming input and pin 22 is a setting input. Pin 30 corresponds to the inverted output brought out through a diode. The feed level is controlled by ZC324 so that a feed hole is punched whenever a punch command pulse appears on the common input to pin 22 of all driver cards. A level change occurs on the common pin 30 line when a hole is punched in any level, including the feed level. This level change allows the gated oscillator ZC120 to run.

3.19 The first pulse from ZC120 resets all drivers that were set and turns off its own turn-on signal. The circuit remains in this condition until another set pulse arrives. The four inputs to the punch driver primes are, data received serially, data received in parallel, blank feed out character, and feed out characters programmed into the switches on the front of the driver module. As levels 1 through 8 operate identically, only level 1 will be described in detail.

3.20 The output of ZC316, pin A10 will be 0 volt, conditioning ZC323 to punch the 1-level, if all inputs to the NOR gate are negative. Any positive input to the NOR gate may be viewed as inhibiting punching level 1. The blank feed bus connected to ZC316 pin A6 is negative unless blank feeding is in progress. The character feed bus connected to ZC316 pin A5 through switch SWC5 is negative unless character feeding is in progress. Opening switch SWC5 has the same effect as if ZC316 pin A5 were connected permanently to -6 volts. With the SWC5 switch open the character feed bus is unable to inhibit punching.

3.21 The receive parallel bus is at 0 volt only when parallel data is received. The receive serial bus is at 0 volt only when serial data is received. When the receive serial bus is at 0 volt and the other three feed busses are negative, ZC316 pin A26 is held negative. At this time ZC316 pin B10 is allowed to go positive if the level 1 input from the receiving distributor storage at JC328 pin C8 is negative, indicating a spacing bit. Therefore, punching in level 1 is inhibited. If the input from the receiving distributor storage is positive, ZC316 pin B10 is held negative so that level 1 is permitted to punch. When the receive parallel bus is at 0 volt and the other three feed busses are negative ZC316 pin B10 is held negative.

3.22 The output of ZC316 pin A26 goes to 0 volt if the auxiliary bit one input is negative, or to -6 volts if the input is positive. Therefore, punching is controlled by the auxiliary bit input signals. A pulse from ZC120, pin 7 causes a character to be punched, when pin 9 of this element goes positive. When power is first applied, relays K2 and K3 of ZC418 do not operate immediately because the winding of

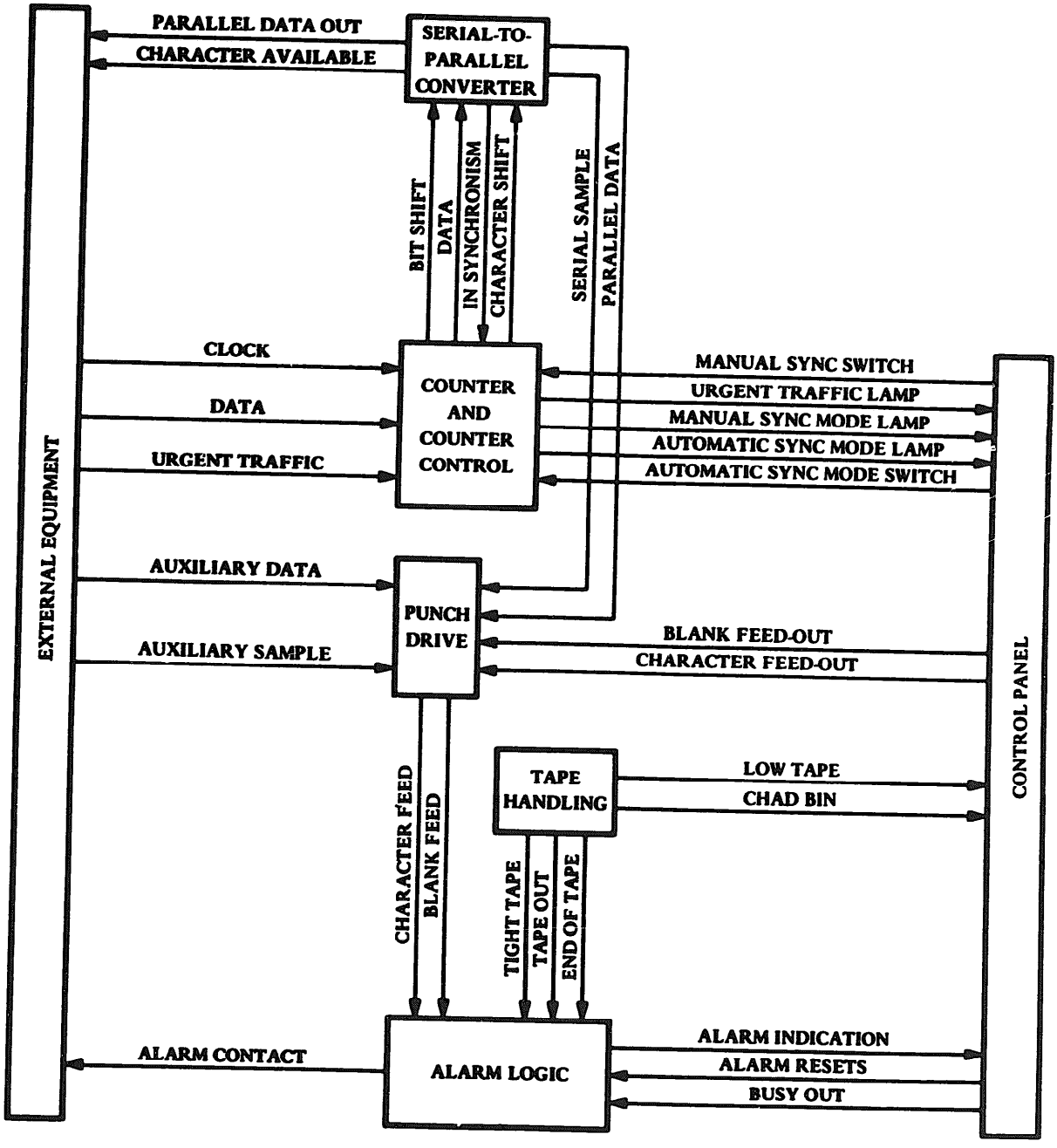


Figure 2 - Block Diagram of Receiver

K2 is connected with an R-C delay network (7746WD, Sheet 3). Relay K3 is then energized through the contact of K2. Before K2 and K3 operates ZC108, pin A12 and ZC112, pin A35 (Sheet 4) are held at 0 volt. Therefore ZC112, pin B27 is negative, pin A9 is at 0 volt, and pin A10 is negative.

3.23 A 0 volt on ZC313 pin A9 holds the blank feed bus negative and 0 volt on ZC313 pin B3 holds the character feed bus negative. With 0 volt on ZC112 pin A14, pin A17 is held negative, holding the receive parallel bus at 0 volt. The 0 volt on ZC112 pin B26 holds pin B28 negative. volt. The 0 volt on ZC1l2 pin B26 holds pin B28 negative, holding the receive serial bus at 0 volt. These conditions hold all punch level inhibit signals off (negative).

3.24 When K2 and K3 are operated ZC108 pin B11 (sheet 3) immediately produces a positive pulse. This acts through diode CR-B of ZC311 to drive ZC120 pin 9 positive, producing a pulse at ZC120 pin 7 punching a delete (rub-out) character. This is done because the punch pins may have partially perforated the tape when power was turned off. This would cause the punch to jam if a delete character were not punched over the partial perforations. Because of the inherent delay in the priming circuits, the delete character will be punched even if the punch prime leads go negative when K2 and K3 operates.

FEEDOUT CIRCUITS

3.25 With no traffic and K2 and K3 operated, ZC12O pin 9 is negative. A circuit consisting of two NOR elements is connected to the BLANK FEED switch (7746WD, Sheet 3). This circuit, sometimes called a latch, is used frequently in connection with switches to eliminate the effects of contact arcing. With the BLANK FEED switch released, a ground at ZC112 pin B23 holds pins A26 and A23 negative. The open at pin A24 allows pin A27 to go to 0 volt, while holding pin A26 negative. If the ground were removed from pin B23, the outputs of the two NOR gates would be unchanged.

3.26 Operating the BLANK FEED switch. grounds pin A24, while holding pin A27 and pin B22 negative. Pin A26 is at 0 volt with pin B23 open. If the ground were removed from pin A24 the state of the circuit would not change. Pin A26 goes to 0 volt as soon as the switch is operated and remains at that voltage, regardless of the contacts arcing, until the switch is released. The latch circuits composed of ZC112, LA-ID and LA-2D are connected to the CHARACTER FEED switch.

3.27 Operating either the CHARACTER FEED switch or the BLANK FEED switch, holds ZC110 pin B34 negative, allowing the multivibrator (MV-A) of ZC313 to run at a frequency of 105 hertz. Square waves from this element appear inverted at ZC307 pin A9, the 1050 wpm lead. At the same time the blank feed or character feed bus goes positive, because of the negative voltages at both inputs of the selected power amplifier element. The blank feed bus or the character feed bus controls priming of the punch drivers as described in 4.18 through 4.24.

3.28 The character feed bus enters ZC112, pin A13 and pin A34 to hold the receive parallel bus and receive serial bus at 8 volt during character feeding. This prevents parallel and serial input data from reaching the punch and interfering with character feeding. Incoming pulses on the 1050 wpm lead enter at ZC112 pin A5 (Sheet 4). Because all other inputs to this element are negative, the 1050 wpm pulses appear inverted at ZC112 pin A10. These pulses drive the punch drive power amplifier of ZC120 and cause the appropriate characters to be punched at a rate of 1050 per second.

3.29 A third character feed circuit is controlled by the CHARACTER FEED toggle switch on the front of the appropriate module C punch driver. This switch is connected to a modified version of the latch circuit described in 4.25. Operating the switch causes ZC112 pin B10 to go negative and pin B9 goes to 0 volt. This 0 volt from pin B9 drives ZC307 pin A10 negative. causing the character feed bus (ZC313 pin B1) to go positive. Negative voltage from pin B10 of ZC112 allows the 240 hertz multivibrator (MV-B) of ZC313 to run, producing pulses on the 2400 wpm lead. These pulses enter ZC112 pin A7 to cause the punch to operate as described previously.

PARALLEL RECEIVING

3.30 After relays K2 and K3 of ZC418 (7746WD, Sheet 3) have operated at the time of power turn-on both inputs to LA-2F of ZC112 are normally negative. This causes ZC112 pin B27 to be at 0 volt and pin 9 to be negative. When parallel data is to be received the auxiliary sample lead goes positive, driving ZC112 pin A9 (the parallel sample lead) positive. This sets flip-flop D-B of ZC311, placing pin B33 at 0 volt. Pin A17 of ZC112 is driven negative, causing the receive parallel) bus to go to 0 volt. At the same time all inputs to LA-IF of ZC112 are negative, causing pin B28 to go to 0 volt and holding the receive serial bus negative.

3.31 Under these conditions (3.30) the punch drivers are primed from the auxiliary bit input leads described previously (3.22). When the auxiliary sample lead

goes negative ZC112 pin A9 goes negative. allowing ZC112 pin A10 to go to 0 volt. The power amplifier ZC120 then emits a pulse which causes the character present on the auxiliary bit leads to be punched. For additional characters the auxiliary sample lead continues to be pulsed. and each negative going transition causes a character to be punched. When no more characters are to be punched the auxiliary sample lead remains negative.

SERIAL RECEIVING

3.32 Serial data is received and converted to parallel circuits to be described later. When a character is assembled and ready for punching, a 0 volt pulse appears at ZC112 pin B7 which was negative. This pulse drives ZC112 pin A10 negative and also resets flip-flop D-B of ZC311. With ZC311 pin B34 at 0 volt and pin B33 negative, the receive parallel bus is held negative and the receive serial bus is held at 0 volt.

3.33 The previous conditions prevent parallel data on the auxiliary bit leads from reaching the punch, and allow data from the serial-to-parallel converter circuits to reach the punch. For example, the first bit of a character received serially is applied to ZC316 pin B6 and appears inverted at pin B10 because the receive parallel bus is negative. If the bit in question is marking ZC316 pin B6 will be at 0 volt, pin B10 will be negative. and pin A10 will be at 0 volt to prime the punch driver.

3.34 At the end of the serial sample pulse (ZC112 pin B7). pin A10 of ZC112 will go positive causing the character for which the drivers are primed to be punched. Further serial sample pulses cause the punching of an additional character at the end of each pulse. When no more characters are to be punched the serial sample pulse lead remains negative.

ALARM CIRCUITS

3.35 The LOW TAPE and END OF TAPE mercury switches are mounted on an arm attached to the tape supply reel holder. The END OF TAPE **switch is** adjusted to close when the tape supply has been used beyond the point at which the LOW TAPE switch operates. The LOW TAPE switch does nothing more than light the LOW TAPE indicator to advise the operator that the tape supply is **used** up. The END OF TAPE switch cuts off the associated equipment that sends messages to the receiver (Figure 3).

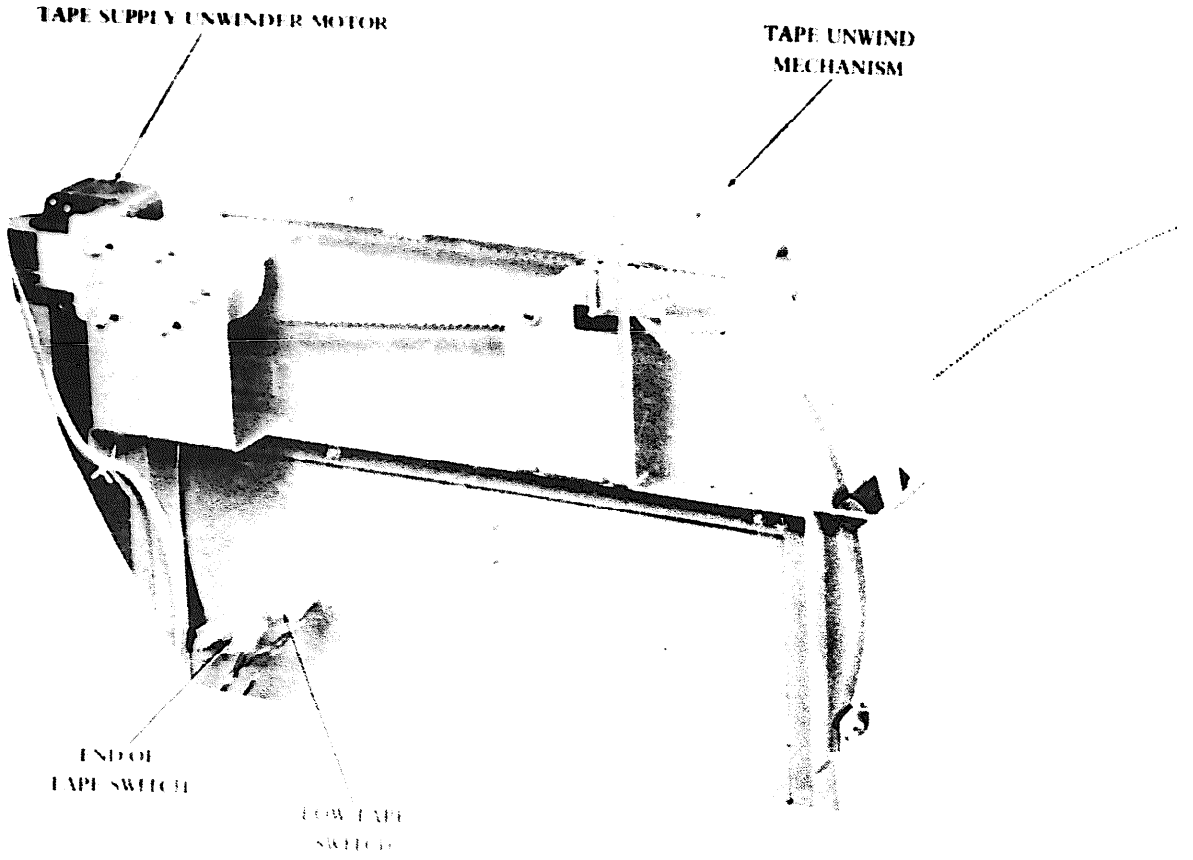
3.36 The **TAPE OUT switch arm is mounted on the** tape feed chute of the punch and closes if there is no tape in the tape path. The TIGHT TAPE contact isactuated by the punch tape supply tension lever when the tape loop in the punch becomes abnormally short. The CHAD BIN switch closes when the chad bin becomes full. as determined by weight (Figure 4). **Like** the LOW TAPE switch. this switch only lights an indicator when it operates.

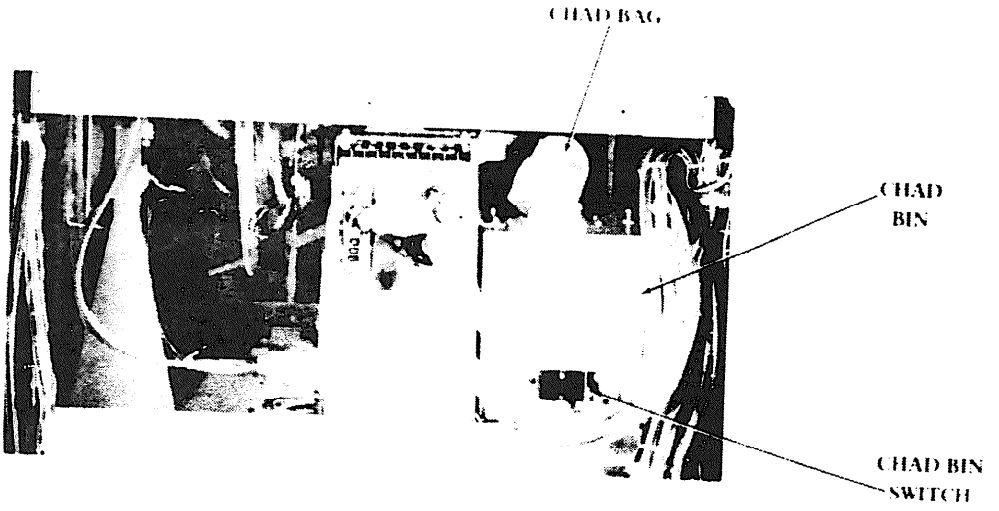
3.37 The NOR elements LA-1A and LA-2A of ZC110 form a latch circuit. When the END OF TAPE switch closes ZC110 pin A9 goes negative and pin A10 goes to 0 volt. Power amplifier PA-ID of ZC108 operates K4 of ZC318 to light the END OF TAPE lamp. An identical latch circuit involving LA-1B and LA-2B of ZC110, PA-2C of ZC108. and K3 of ZC318 controls the TAPE OUT lamp. Both of these latches are reset by pressing the associated END OF TAPE/TAPE OUT indicator switch, which causes ZC110 pins A10 and Al7 to go negative.

3.38 A similar latch using LA-1C and LA-2C of ZC110, PA-1C of ZC108, and K2 of ZC318 lights the TIGHT TAPE lamp when the TIGHT TAPE switch operates. Tape motion is detected by counting punch drive pulses between operations of the tape puller motor on the punch with an eight stage binary counter. The counter is reset each time the tape puller operates. The tape is not feeding properly if the tape puller does not operate before 161 or 162 drive pulses have been counted.

3.39 The counter **consists of flip-flops D-C, D-D,** D-E. **and** D-F **of** ZC311 **and flip-flops D-B.** D-C. D-E. and D-F **of** ZC309. The **counter is reset to zero by applying a positive pulse through diodes on the same cards to the inverted outputs of all the flip-flops except D-D in** ZC311. **When power is first applied the power on level signal at** ZC313 **pin** A31 **holds the reset bus negative. When** K2 and K3 **of** ZC-418 **operates. both inputs to PA-E of** ZC313 arc negative. **causing this element to generate a positive pulse** at **pin** A27. **resetting the counter flip- flops** (7746WD. Sheet 3).

3.40 When the tape **puller** motor **operates,** 60 **hertz ac is** applied to pin B13 of ZC307. This causes 60 hertz pulses at pin All. The NOR elements LA-2B and LA-1C **of** ZC307 form a latch to store tape **puller motor operations, for** the negative transition of the punch **drive pulse. These cycle** the 725 microsecond delay DY-B in ZC108. This resets the above latch and causes PA-E **of** ZC313 **to generate a positive** pulse and reset the counter **flip-flops.**


TAPE SUPPLY UNWINDER MOTOR
TAPE UNWIND
MECHANISM
END OF
TAPE SWITCH


CHAD BAG
CHAD
BIN
CHAD BIN
SWITCH

3.41 This counter reset causes pin A23 of D-D in ZC311 to go to -6 volts. The next drive pulse will place D-D in the set 1 condition. When pin A23 goes to 0 volt flip-flop D-C of ZC311 is set. This action continues down the counter until all flip-flops are set. The first drive pulse sets the counter to a full count of 255. The next drive pulse resets flip-flop D-D of ZC311 so that the counter holds a count of 254. These counts are determined by assigning values to the counter stages from left to right, 1, 2, 4, 8, 16, 32, 64, and 128. The count in the counter is determined by adding the values of all flip-flops that are set. The next drive pulse sets the first flip-flop again.

3.42 When pin A32 of ZC311 goes to 0 volt, flip-flop D-E of ZC311 is reset, so the count is 253. In the same manner the following pulses decrease the count in the counter by one for each pulse. After 160 pulses the counter will contain a count of 96, with flip-flops D-C and D-E of ZC309 set and all others reset. The next drive pulse sets flip-flop D-C of ZC311, and sets flip-flop D-E which sets flip-flop D-F. This sets flip-flop D-B of ZC309 which resets flip-flop D-C, and resets D-C and D-F of ZC309 which sets D-E. This causes all inputs to LA-1B of ZC307 to be negative, allowing pin A17 to go positive.

3.43 The negative edge of the next drive pulse then resets flip-flop D-D of ZC309. This operates relay K1 on ZC418 to light the TAPE FEED indicator. The tape puller motor normally operates more often than every 161 characters (as mentioned in 3.38). The counter is normally reset before a count of 95 is reached and flip-flop D-D of ZC309 is reset. Pressing the indicator associated with the TIGHT TAPE/TAPE FEED switch resets the TIGHT TAPE latch if it was set, or sets the TAPE FEED flip-flop D-D of ZC309, if it was reset.

3.44 This latter action (described in 3.43) starts with the switch in its normal position, ZC307 pin B27 is at 0 volt and pin B9 is negative. When the switch is operated B9 goes positive to set the flip-flop. The time delay associated with the prime input allows the flip-flop to be set even though the prime input goes negative at the same time the set input goes to 0 volt. The NOR elements LA-1E and LA-1F of ZC110 are connected together to form a seven input gate.

3.45 Normally all inputs are negative, allowing pin B28 to go to 0 volt. This holds pin B9 at a negative voltage, causing the power amplifier to operate relay KC119A. A 0 volt signal at any input of the seven input gate will release the relay to indicate an alarm condition to the associated equipment.

3.46 An alarm condition is also indicated if power to the receiver is turned off, since relay KC119A is also released as a result. The inputs to the seven input gate are BLANK FEED, CHARACTER FEED, BUSY OUT (operator switch), END OF TAPE, TAPE OUT, TIGHT TAPE, and TAPE FEED. The BUSY OUT switch is a push-on, push-off operator control, allowing the operator to remove the receiver from service. The indicator lamps for the BUSY OUT, BLANK FEED, and CHARACTER FEED indicator switches are also shown on 7746WD, Sheet 2.

SERIAL-TO-PARALLEL CONVERTER

3.47 Normal and inverted serial data are applied to sections B and C of the CODE LEVEL switch, respectively. If the switch is in the 8-level position, these signals are applied as primes to element D-B of ZD509. The outputs of this element are inverted by elements LA-1A and LA-1B of ZD507 and applied as primes to element D-C of ZD509. Similarly element D-D of ZD509 is primed from the inverted outputs of element D-C, and element D-E primed from the inverted outputs of D-D (7746WD, Sheet 7 and Sheet 8).

3.48 Elements D-B, D-C, D-E, D-F, and D-D of ZD513 are primed from the preceding elements. The group of flip-flops is arranged as a nine element shift register. When the CODE LEVEL switch is set to the 7-level position a ground is applied to pin A7 and pin A13 of ZD507 to allow the output of both LA-1A and LA-1B to go negative. The outputs of these elements, which are the primes of element D-C, ZD509, are connected to the normal and inverted serial leads through sections B and C of the CODE LEVEL switch. One or the other of the serial data leads will be held at 0 volt by the data. Therefore, element D-B of ZD509 is effectively eliminated from the shift register.

3.49 When the CODE LEVEL switch is set to the 6-level position the ground on A7 and A13 of ZD507 is maintained through diode CR-B of ZD507. A ground is applied to pin A24 and pin A31 of ZD507. At the same time the normal and inverted serial data leads are moved to prime D-D of ZD509, which eliminates D-B and D-C from shifting action. In a similar manner element D-D is eliminated from shifting action when the CODE LEVEL switch is in the 5-level position. The number of active elements in the shift register is always one greater than the number of levels indicated by the CODE LEVEL switch setting.

3.50 An additional element is used to hold the start bit in start-stop operation. Each shift register element except the start element primes a storage flip-flop. For example, element D-B of ZD509 primes element D-B of ZD511. In normal operation data is continuously shifted through the shift register without regard to character boundaries. The synchronizing logic (to be described in 3.73 through 3.78), keeps track of character boundaries, and sets the shift register contents into the storage flip-flops when a complete character is properly positioned in the shift register.

3.51 Normal and inverted storage flip-flop outputs enter the patching circuit card ZD517. This card allows the output circuits to be connected to the data storage flip-flops in any order, and with either normal or inverted polarity. The NOR and INV markings on the terminals of ZD517 (TB243) appear to be backwards with respect to the storage flip-flop output. This is done because the signals will be inverted in NOR gates before being presented to the punch driver and output amplifiers. The LEVEL markings on ZD517 correspond to punch levels and have no relation to the order in which bits are received.

3.52 The outputs from ZD517 for levels 2 through 6 pass through inverters to the punch drive logic, after inversion through output elements to the associated equipment. The R-C networks provided in these output leads are used to prevent fast rise time pulses from leaving the receiver, as an RF noise reduction measure.

3.53 The outputs from ZD517 for levels 1, 7, and 8 are passed through NOR gates controlled by the CODE LEVEL switch. For example, level 8 is applied to input B13 of ZD518. Elements LA-2A and LA-2B of this card are connected together to provide signal isolation and increased load driving capability, the outputs of these two elements are identical. With the CODE LEVEL switch in the 8 level position these elements act as a simple inverter. In the 5, 6, or 7 level position a ground is applied to input B12 of these elements, holding the outputs negative.

UNITS COUNTER

3.54 The units counter determines when a complete character is in the shift register by counting clock pulses. To perform this function the units counter must be properly aligned with respect to character boundaries; it must start counting at the first bit of a character and stop at the last bit, and then reset to the starting position (Sheet 6).

3.55 The synchronizing circuits which align the counter with character boundaries will be described in 3.79 through 3.85. For the present discussion it will be assumed that the counter is properly aligned. In the SYNCHRONOUS operation all received bits are data bits. In the START-STOP operation a character is always preceded by a start unit and may or may not be followed by one or more stop units. In either case clock pulses are supplied continuously, so that a stop element must contain an integral number of units.

3.56 The SIGNAL MODE switch selects SYNCHRONOUS or START-STOP operation. The CHAR. SYNC. switch in the OFF position allows reception of characters which always contain a specified number of units. In the ON position the receiver can accept characters having stop elements containing an unspecified number of units. The SIGNAL MODE switch is equipped with a latching circuit. The NOR element ZD303 pin A9 is at 0 volt and pin A11 is negative in the START- STOP position. These conditions are reversed in the SYNCHRONOUS position.

3.57 The counter is composed of flip-flops D-B, D-C, D-D, and D-E of ZD503. In synchronous operation the starting position of the counter is the element D-B, which is reset while the other elements are set. (Sheet 6, the semicircular symbols with the letter D, are additional Prime and set inputs for the flip-flop.)

3.58 The counter is placed in this position by the last character shift pulse. This resets element D-B directly and fires the 100 microsecond one-shot DY-B pulse of ZD305 to pull counter elements D-C, D-D, and D-E into the set condition. In the starting position of the START-STOP operation of the counter all flip-flops are set. With the counter placed in the condition just described, the element D-B is primed to be set rather than reset.

A. Synchronous Operation, 5 Units Per Character

3.59 The output at pin A10 of ZD303 is held negative by the 0 volt input at pin A6. With the synchronous prime signal also negative, the inverted clock pulses are reinverted by LA-1B of ZD303. This causes counter element D-B to be driven by normal clock pulses. The positive-to-negative clock transition occurs in the center of a data bit. The negative-to-positive transition occurs at the time of data transitions. Therefore, the counter is advanced at the time of data transitions.

3.60

3.60 The first clock pulse sets counter element D-B. As pin B34 of this element goes negative pin A26 of ZD303 goes positive to reset element D-C. The next clock pulse resets element D-B. The third clock pulse sets D-B, which sets D-C, and resets D-D. The fourth clock pulse resets D-B. The fifth clock pulse sets D-B which resets D-C. Table A summarizes the action.

TABLE A

FLIP-FLOP OPERATION, 5 UNITS PER CHARACTER

CLOCK PULSE	D-B	D-C	D-D	D-E
0	Reset	Set	Set	Set
1	Set	Reset	Set	Set
2	Reset	Reset	Set	Set
3	Set	Set	Reset	Set
4	Reset	Set	Reset	Set
5	Set	Reset	Reset	Set

3.61 After the fourth clock pulse, and the UNITS PER CHARACTER INTERVAL switch set at 5 (SYNCHRONOUS), all inputs to element LA-1C of ZD303 were negative allowing the output to go to 0 volt. After the fifth clock pulse, pin A27 of ZD303 goes negative. This causes PA-E of ZD305 to emit a pulse, which triggers DY-B of ZD305. These two signals reset the counter to the condition mentioned above for clock pulse 0.

3.62 The pulse from pin A27 of ZD305 is the character shift pulse, and sets the shift register contents into the storage flip-flops. The pulse from DY-B of ZD305 is inverted by element LA-2A of ZD520. The resulting signal goes positive 100 microseconds after the clock pulse which caused the counter to be reset. Pin A21, LA-1F of ZD518 is at 0 volt in synchronous operation (Sheet 8). Therefore, pin B28 of ZD518 is negative and pin B27 of ZD520 is at 0 volt, priming the 2 millisecond one-shot DY-A of ZD305. This is triggered by the character shift pulse.

3.63 The normal output of the one-shot is made available to external equipment. The one-shot output is inverted by LA-1F of ZD520 to form the sample pulse for the punch driver. This pulse enters pin B7 of ZC112 and causes the character in the storage flip-flops to be punched (Sheet 4). The timing diagram in Figure 5 is of the counter operations described in the preceding paragraphs. To relate the description to the figure, the first clock pulse is represented in Figure 5 as the positive going clock transition following the number 1 data pulse, the second clock pulse follows the number 2 data pulse, and so on.

3.64 This mode of operation is the same as described in the previous paragraphs, except that more clock pulses are received before LA-1C of ZD303 detects the completion of a character (Figure 6). Table B shows the various flip-flop states, the first six are the same as those given previously.

C. Start-Stop Operation, 6 Units Per Character, 5-Level

3.65 In this mode of operation the 5 bits of a character are preceded by a start pulse. With the SIGNAL MODE switch in the START-STOP position pin A9 of ZD303 is at 0 volt, pin A11 is negative. This removes the reset prime from counter element D-B, and applies a set prime, so that the starting position of the counter is that in which all flip-flops are set.

3.66 With the CHAR. SYNC. switch in the OFF position, the established synchronous operation proceeds as described in the 5 unit synchronous operation, except for the starting position of the counter and the method of obtaining the punch sample pulse. Table C shows the various counter states.

3.67 As compared with synchronous operation one additional clock pulse is received before the character shift signal is generated and the counter is reset. Referring to 7746WD, Sheet 8, input A21 of LA-1F, ZD518 is negative in START-STOP operation. When the start pulse is in element D-D of ZD513 input A34 of LA-1F, ZD518 goes to 0 volts because of appropriate strapping on ZD517. This causes pin B27 of ZD520 to go to 0 volt, and primes DY-A of ZD305 to generate the sample pulse as before when the character shift pulse arrives. The timing diagram for this mode of operation is shown in Figure 7.

D. Start-Stop Operation, 7 Units Per Character, 5-Level

3.68 If the data information consisted of a start pulse followed by 6 data bits, then operation is the same as described previously. With the exception that this setting of the UNITS PER CHARACTER INTERVAL switch causes the counter to count one additional pulse before generating the character shift signal. An exceptional case is that in which the start pulse is always spacing and the 5 data bits are followed by a stop pulse which is always marking. In this case the CHAR. SYNC. switch may be operated to the ON position, permitting receipt of characters in which the stop pulse may have a duration of an indefinite number of units.

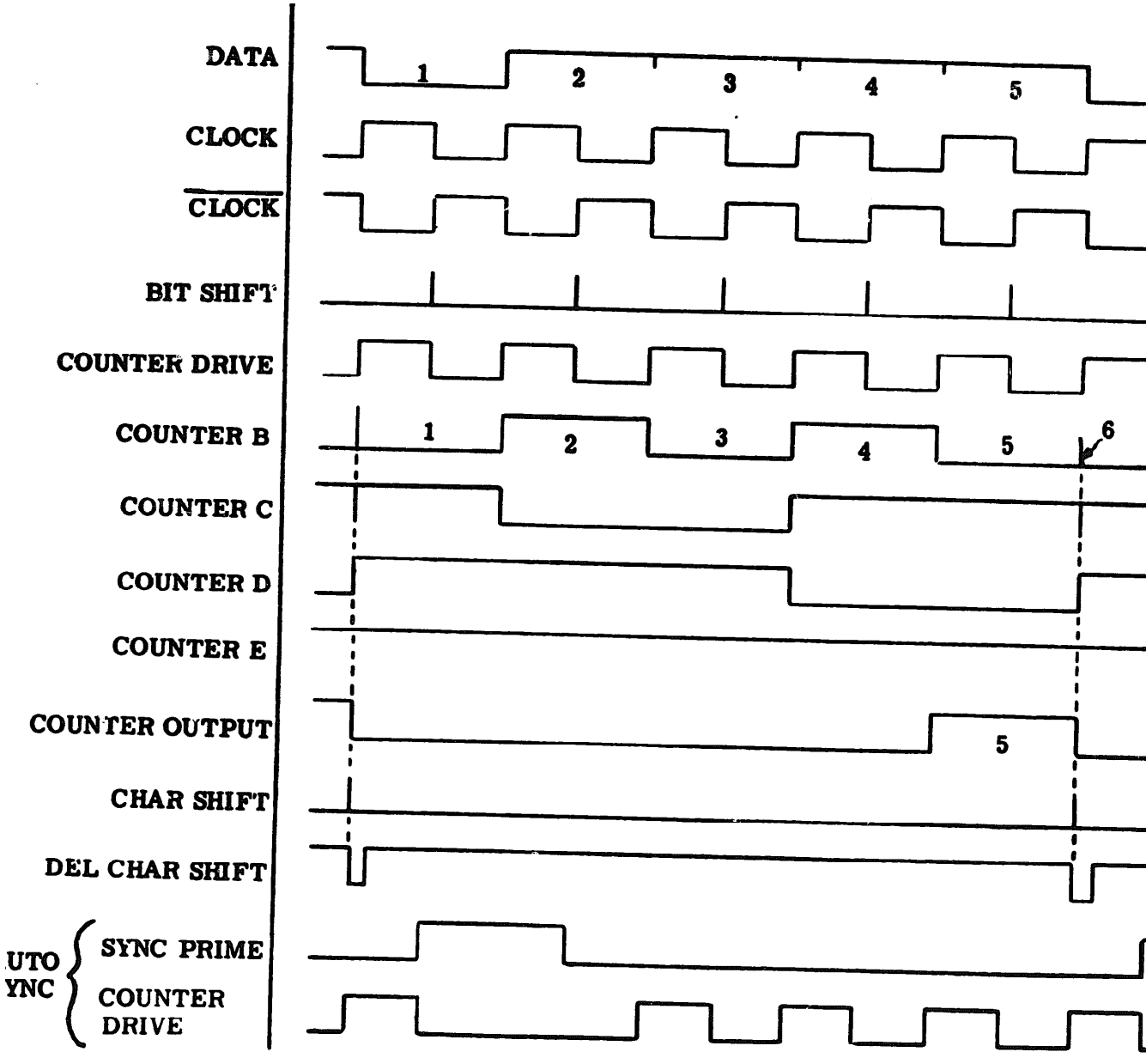


Figure 5- RDL Logic for 5 Unit 5-Level Synchronous operation

TABLE B

FLIP-FLOP OPERATION, 10 UNITS PER CHARACTER

CLOCK PULSE	D-B	D-C	D-D	D-E	REMARKS
0	Reset	Set	Set	Set	
1	Set	Reset	Set	Set	
2	Reset	Reset	Set	Set	
3	Set	Set	Reset	Set	
4	Reset	Set	Reset	Set	
5	Set	Reset	Reset	Set	
6	Reset	Reset	Reset	Set	
7	Set	Set	Set	Reset	
8	Reset	Set	Set	Reset	
9	Set	Reset	Set	Reset	ZD303 pin A27 to 0 volt.
10	Reset	Reset	Set	Reset	Reset to clock pulse 0.

TABLE C

FLIP-FLOP OPERATION, 6 UNITS PER CHARACTER

CLOCK PULSE	D-B	D-C	D-D	D-E	REMARKS
0	Set	Set	Set	Set	
1	Reset	Set	Set	Set	
2	Set	Reset	Set	Set	
3	Reset	Reset	Set	Set	
4	Set	Set	Reset	Set	
5	Reset	Set	Reset	Set	ZD303 pin A27 to 0 volts.
6	Set	Reset	Reset	Set	Reset to clock pulse 0.

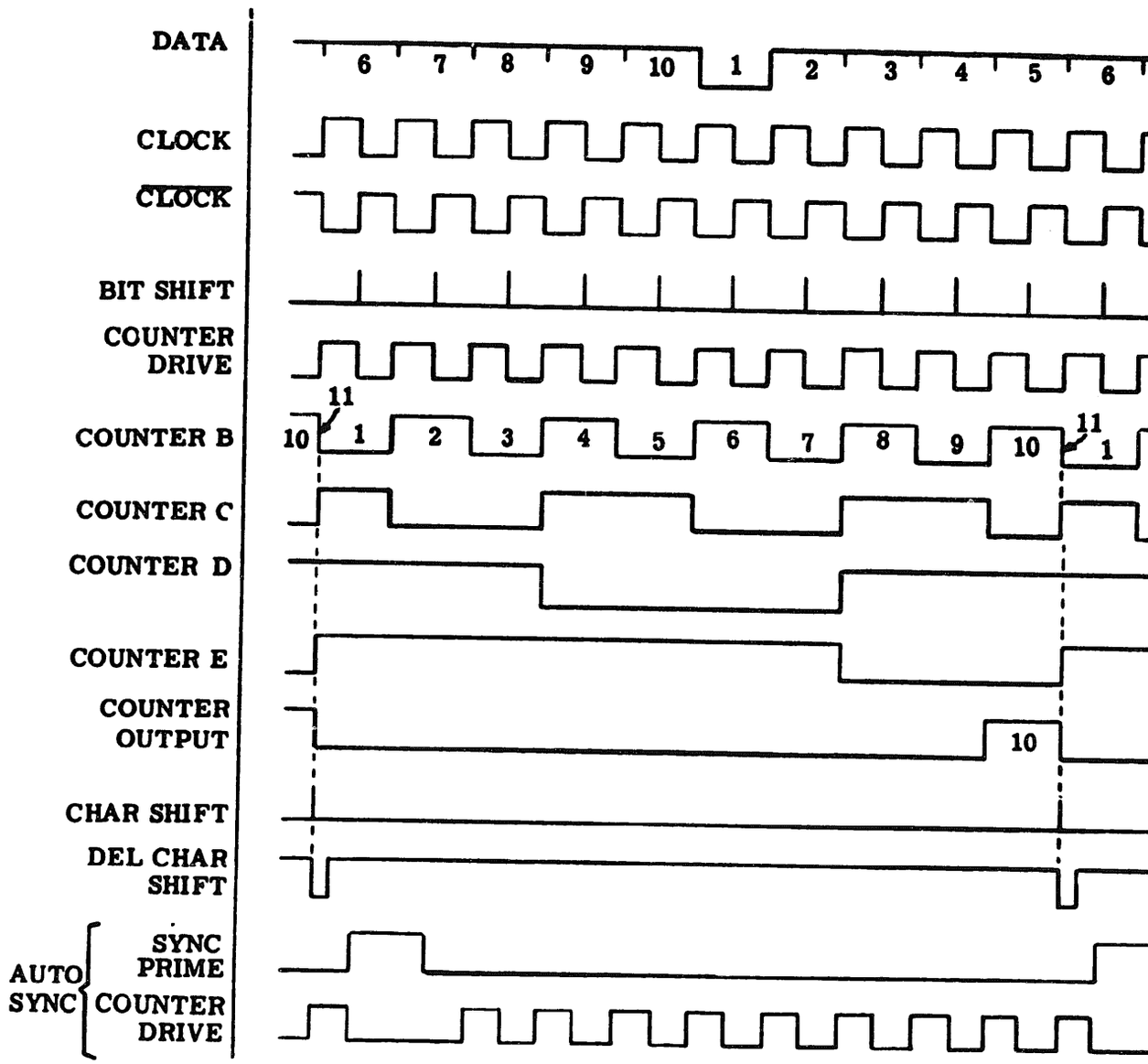


Figure 10 RDL Logic fo 10 Unit 10-Level Synchronous operation

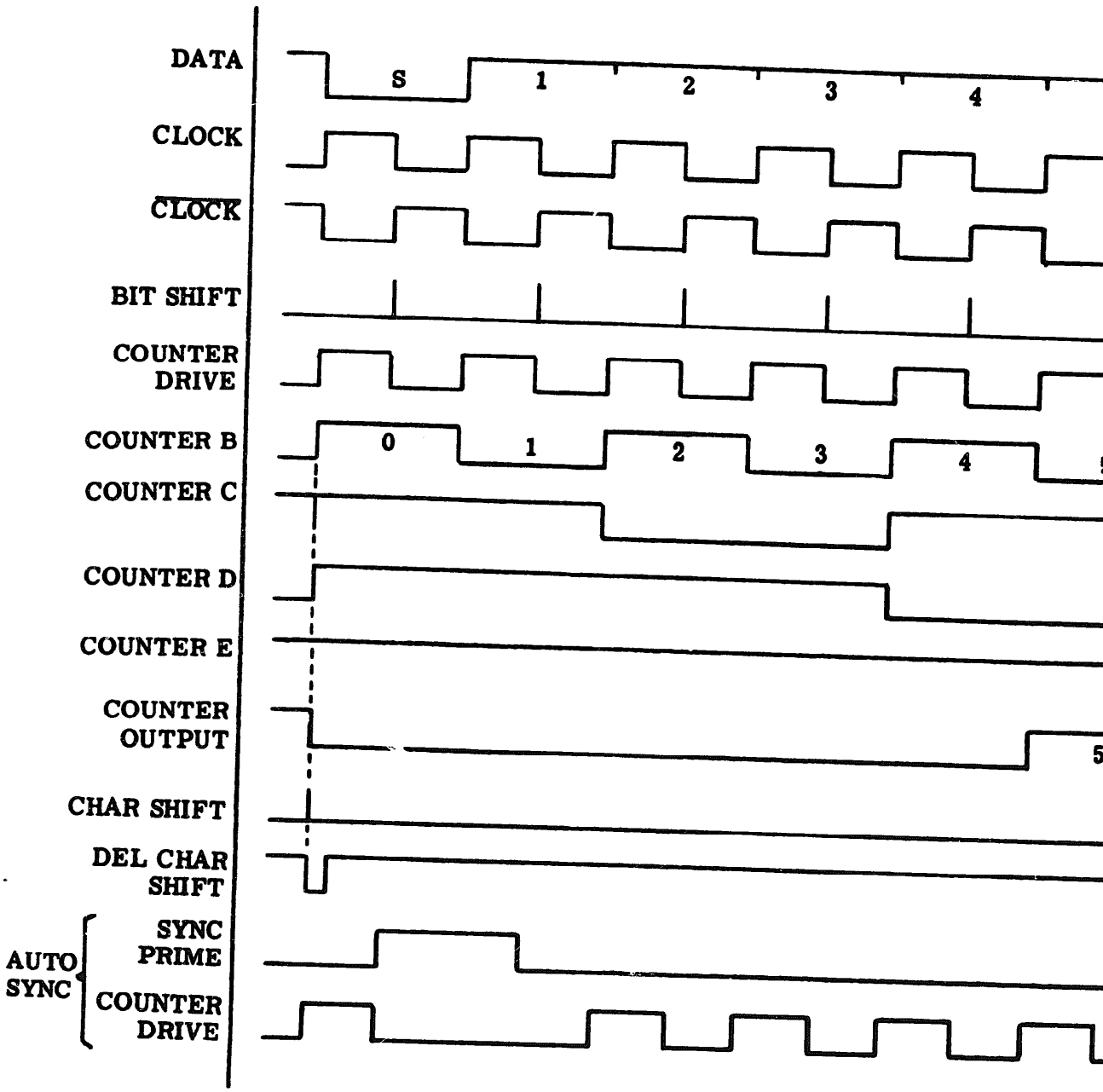


Figure 7 RDL Logic for 6 Unit, 5-Level (Start-Stop)

3.69 In this mode of operation the character synchronous prime signal controls the output of LA-1A, ZD303. When the character synchronous prime signal is 0 volt, pin A10 of ZD303 is negative as before and clock pulses reach the counter. When the character synchronous prime signal is negative pin A10 of ZD303 goes to 0 volt. This holds pin A17 of ZD303 negative at all times so that clock pulses cannot reach the counter. The character synchronous prime signal is controlled by flip-flops D-B and D-C of ZD505. During receipt of a character both of these elements are set, so that the character synchronous prime lead is at 0 volt (Sheet 5).

3.70 When the complete character has been received and transferred into the storage flip-flops, the delayed character shift signal resets element D-B. This occurs 100 miscroseconds after the beginning of the stop pulse. The next bit shift (clock) pulse resets element D-C in the center of the first unit of the stop pulse. With element D-B reset no further clock pulses are counted, so the counter remains in the state corresponding to a number 0 clock pulse.

3.71 No change takes place in the circuit, as long as the incoming data lead remains marking. When the incoming data lead goes spacing, pin A26 of ZD507 goes positive to set element D-B. This allows clock pulses to reach the counter, the first clock pulse also sets element D-C. This element is necessary to delay priming element D-B for one half unit of time, because a slow rise time data input could otherwise cause D-B to be set falsely.

3.72 The timing diagram for this mode of operation is shown in Figure 8. The timing diagram for the 10 unit 5 level start-stop operation is shown in Figure 9, which is the same as that just described except for the different setting of the UNITS PER CHARACTER INTERVAL switch and the greater number of pulses counted.

E. Synchronization

3.73 In the preceding paragraphs it has been assumed that the receiver is properly synchronized, meaning, the counter is reset between characters. It is possible for the receiver not to be synchronized resulting in the character shift pulses not coinciding with character boundaries. This causes each punched character to contain some bits from one data character and some bits from the adjacent character. The circuits to be described perform the function of placing the receiver in synchronism.

3.74 The usual method of synchronizing is suppressing clock pulses from reaching the counter. This is the function of the synchronous prime lead. The 0 volt on this lead holds ZD303 pin A17 negative so that clock pulses are not counted (Sheet 6). A negative voltage on this lead allows the pulses to be counted normally. During synchronizing one clock pulse is deleted during each character interval. This causes the counter to fall behind the data stream. The synchronizing action should stop when the counter falls into the correct position with respect to the data.

3.75 Synchronizm cannot be achieved if any or all of the following conditions are present:

(a) If the UNITS PER CHARACTER INTERVAL switch is not set correctly for the data being received.

(b) If the SIGNAL MODE switch is not set to its proper position.

(c) If the CHAR. SYNC. switch is turned ON when the data stream does not contain proper start-stop pulses.

3.76 With miscellaneous signals being received it is impossible for the receiver to determine whether it is in or out of synchronism. Operating the MANUAL SYNC. indicator switch allows the operator to slip the counter. This process can be repeated until the data being punched appears to be reasonable, as determined by inspecting the tape. The counter slips one position for each operation of the MANUAL SYNC. indicator switch.

3.77 The automatic synchronizing mode causes the receiver to search for a predetermined idle character pattern in the received data. Whenever this character is being received a search for synchronism can be initiated by pressing the AUTOMATIC/MANUAL SYNC MODE indicator switch, unless the receiver is already in synchronism. The AUTOMATIC/MANUAL SYNC MODE switch controls whichever mode is to be used by controlling flip-flop D-D of ZD505. This flip-flop is set for the automatic mode and reset for the manual mode.

3.78 In the automatic mode a negative voltage at pin B22 of ZD505 causes relay K1 of ZD526 to be operated by PA-1D of ZD305. In the manual mode a negative voltage at pin A23 of ZD505 causes PA-2D of ZD305 to operate relay K2 of ZD526. These relays operate the AUTOMATIC SYNC MODE and MANUAL SYNC MODE indicators, respectively. The AUTOMATIC/MANUAL SYNC MODE siwtch operates a latch composed of LA-1D and LA-1E of ZD303. Pin B10 of ZD303 goes to 0 volt when the switch is operated, and pin B34 of ZD303 goes to 0 volt when the switch is released.

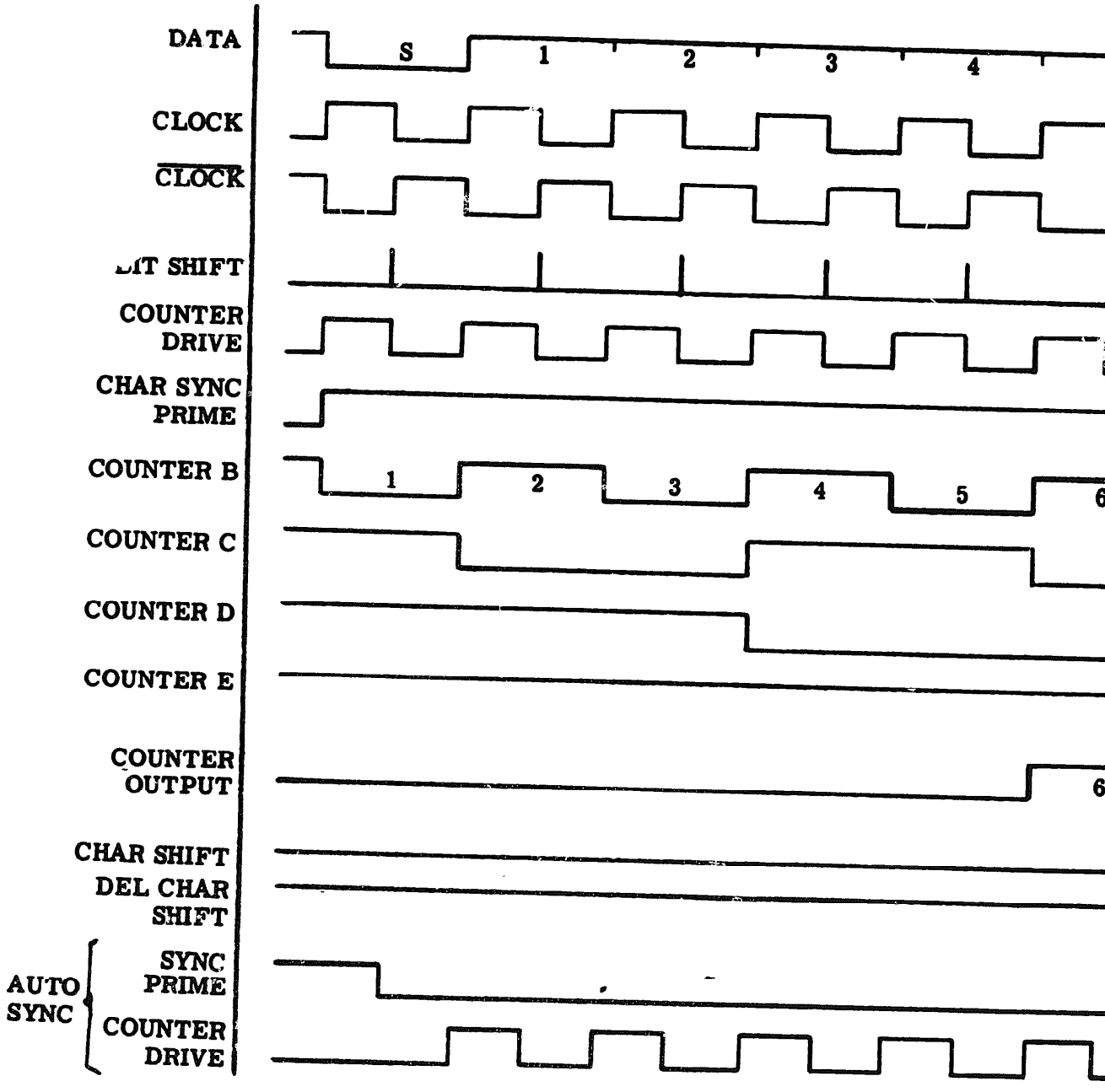


Figure 7 RDL Logic for 7 Unit, 5-Level (Start-Stop)

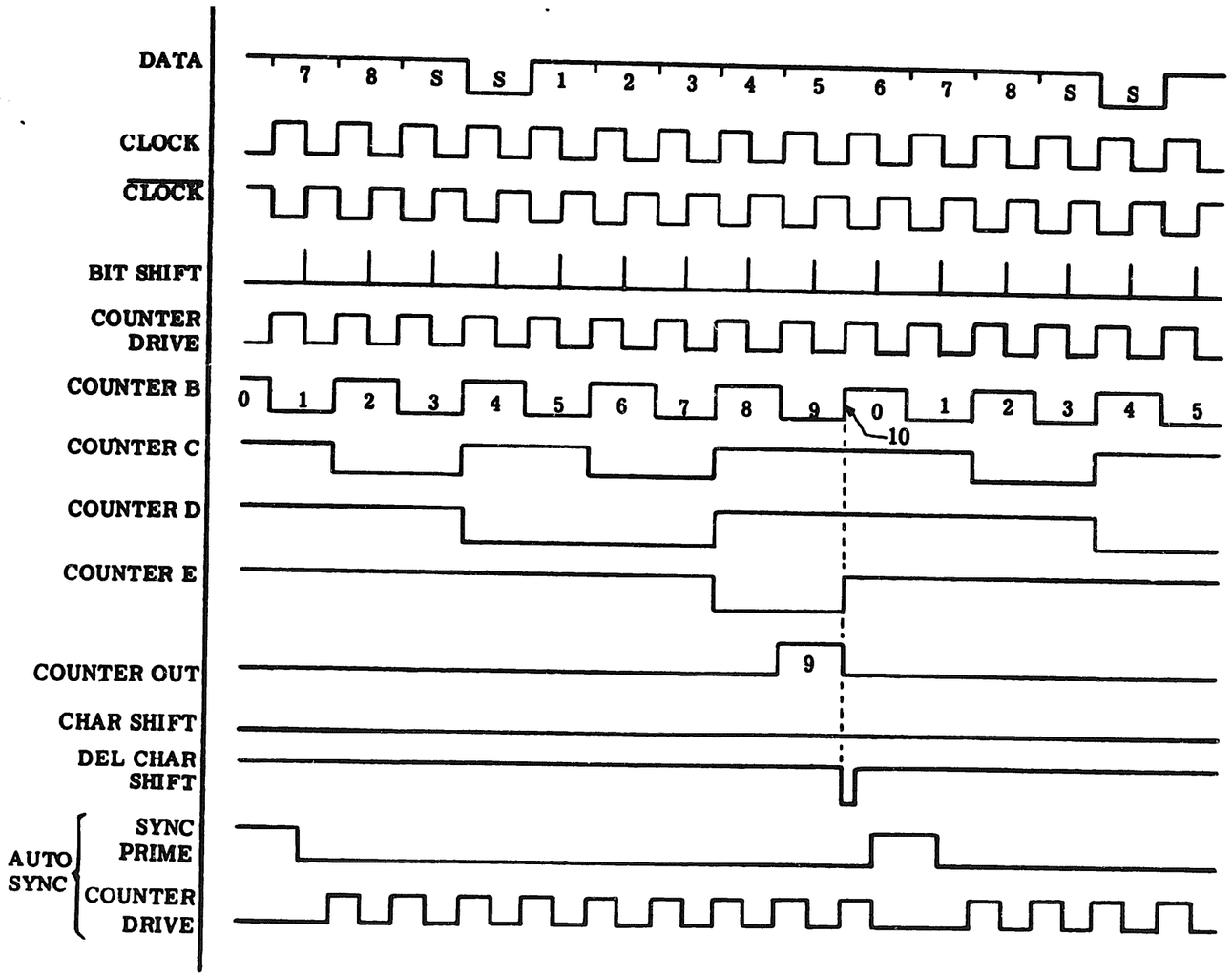


Figure 9 RDL Logic for 10 Unit, 5-Level (Start-Stop)

Automatic Synchronism

3.79 The output of LA-1A, ZD520 is 0 volt when the receiver detects the idle character (Sheet 7). This occurs when all inputs to this NOR element are negative. The outputs of ZD517 indicate negative voltage marking signals. Inputs A7, A6, and B7 of LA-1A are connected to code levels 6, 5, and 4 respectively. Diodes CR-E and CR-F of ZD515 form two additional inputs to the gate for bits 3 and 2, respectively (Sheet 8).

3.80 Elements LA-2C, LA-2D, and LA-2E of ZD520 have their outputs connected in parallel. If any of these gates have both inputs negative, input A5 of LA-1A, ZD520, will be held at 0 volt. Therefore, the in synchronous lead will go to 0 volt, only if levels 2 through 6 after passing through ZD517 are marking, and if each of the gates LA-2C, LA-2D, and LA-2E of ZD520 have at least one input at 0 volt. The latter condition is satisfied if the levels in use, out of group 1, 7, and 8 are marking and the CODE LEVEL switch is set correctly for the number of levels in use. For example, with 7-level operation, the CODE LEVEL switch grounds input B23 of LA-2C so the condition of the eighth level flip-flop is immaterial.

3.81 The elements LA-2D and LA-2E do not have their inputs (B30 and A1) grounded by the CODE LEVEL switch. Therefore, inputs B31 and B1 must be at 0 volt, which is the marking condition, for the in synchronous lead to go to 0 volt. This causes pin A11 of LA-2B, ZD520 to be held negative and prevents flip-flop D-D of ZD505 from being set (Sheet 5). With the preceding conditions available, pin A11 of ZD520 goes to 0 volt to prime flip-flop D-D to be set.

3.82 Operating the AUTOMATIC/MANUAL SYNC MODE switch once, causes B10 of ZD303 to go to 0 volt, setting flip-flop D-D. This primes flip-flop D-E, which is set by the next delayed character shift pulse, at the positive going transition. This causes pin B10 of flip-flop D-E to go to a negative voltage. If the synchronous prime signal is negative pin B27 of LA-2F, ZD507 goes to 0 volt priming flip-flop D-F. The next bit shift pulse sets flip-flop D-F which primes itself to be reset and holds the synchronous prime lead at 0 volt to prevent the next clock pulse from being counted.

3.83 The next bit shift pulse resets element D-F, which then allows clock pulses to reach the counter. When the synchronous prime lead goes negative pin B3 of D-F goes to 0 volt, resetting flip-flop D-E. Therefore, one clock pulse has been inhibited from reaching the counter. If the receiver is still not synchronized, the next delayed character shift sets flip-flop D-E again, causing another pulse to be dropped.

3.84 When synchronism is achieved the in synchronous lead goes to 0 volt on the positive edge of the character shift pulse. This and the inverted character shift, reset flip-flop D-D through the auxiliary input gate. This removes the set prime from flip-flop D-E before the delayed character shift pulse arrives. Therefore, flip-flop D-E is not set and further clock pulses are prevented from reaching the counter by this circuit.

3.85 If synchronism cannot be achieved because there are no characters in the data stream the operator can press the AUTOMATIC/MANUAL SYNC MODE switch again As flip-flop D-D primed itself to be reset, it removed its set prime as it was set, and will reset when the switch is operated. The operator can then try to achieve synchronism with the manual procedure.

Manual Synchronism

3.86 The MANUAL SYNC indicator switch drives a latch composed of LA-1F and LA-2F of ZD303, pin B27 of ZD303 goes to 0 volt when the switch is operated. With flip-flop D-D of ZD505 reset, the auxiliary setting gate of flip-flop D-E is primed. Operating the MANUAL SYNC switch, sets flip-flop D-E, causing a clock pulse to be inhibited from reaching the counter as described previously for automatic synchronizing.

3.87 Because of the ac coupled auxiliary setting gate is is necessary to operate the MANUAL SYNC switch once for each clock pulse to be slipped. Operating this switch the number of times equal to the UNITS PER CHARACTER INTERVAL switch setting, will slip the counter around to its original position. Therefore, to bring the receiver into synchronism, the switch should be operated only the number of times indicated by the UNITS PER CHARACTER INTERVAL switch.

URGENT TRAFFIC

3.88 Urgent traffic, detected by the associated equipment requires immediate operator attention. When urgent traffic is received the associated equipment drives the urgent traffic input lead positive. Inverters LA-1D, and LA-1E of ZD520, insure a sufficiently fast rise time to set flip-flop D-D of ZD515. This causes pin B22 to go to a negative voltage activating PA-2C of ZD305 which operates relay K3 of ZD526. This relay lights the URGENT TRAFFIC indicator (Sheet 5).

3.89 The URGENT TRAFFIC switch drives a latch composed of LA-1B and LA-1C of ZD520. Normally pin A27 is negative and pin A17 is at 0 volt. This primes flip-flop D-D to be reset. Operating the switch causes pin A27 of ZD520 to go to 0 volt, resetting flip-flop D-D and turning off the URGENT TRAFFIC indicator. The time delay, associated with the priming action allows flip-flop D-D to be reset, as the prime input goes negative the reset input goes to 0 volt.

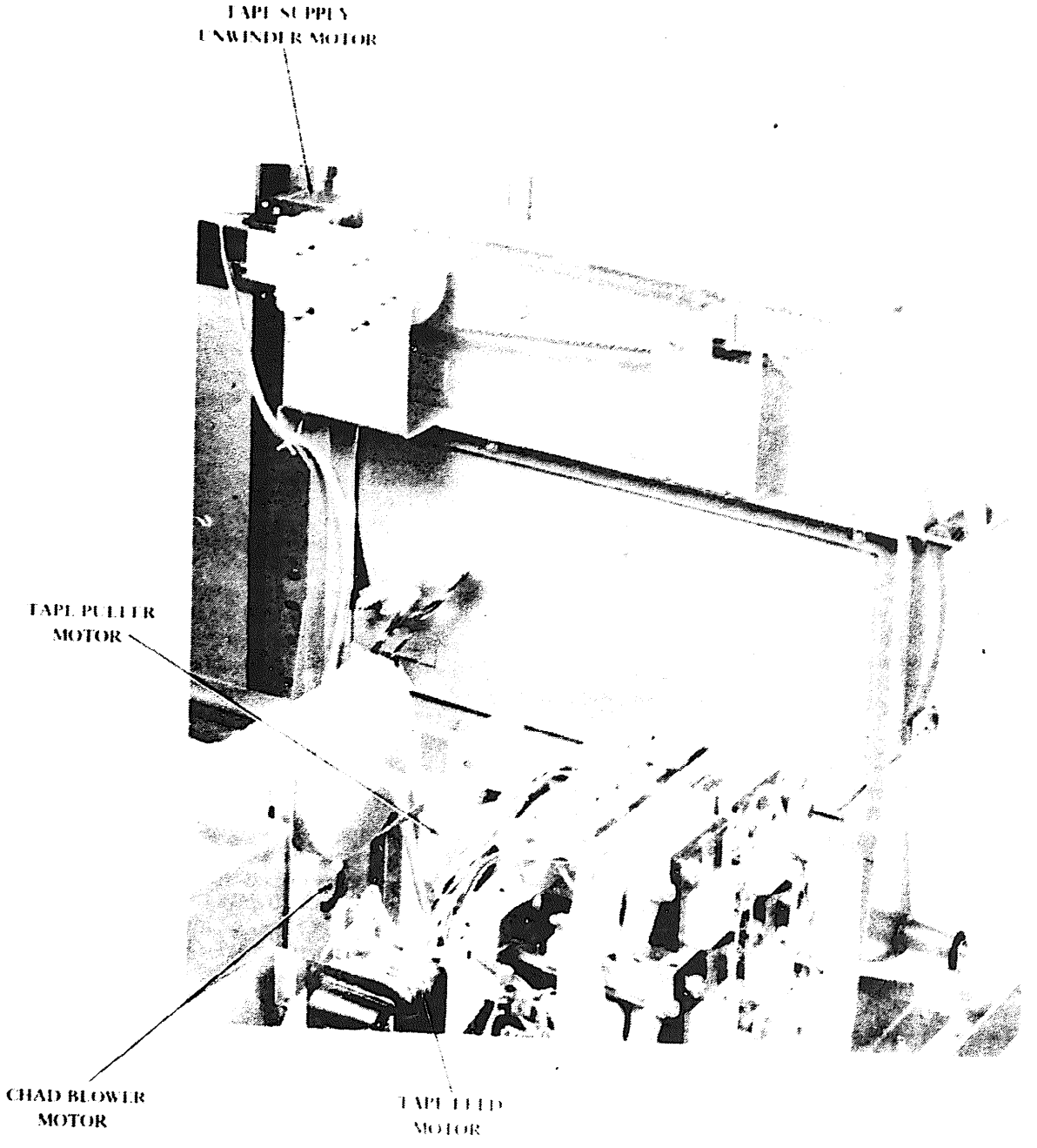


Figure 10 Tape Supply and Chad Blower Mowers

3.90 There are three independent ac input circuits, one for each receiver (upper and lower), and one for the cabinet outlets and fans. Each input is filtered through a 0.47 microfarad bypass capacitor (for rfi purposes) and protected by a 15 ampere circuit breaker. The ac outlets are protected with 5 ampere circuit breakers. Operating either power switch, SW110 or SW210 (upper or lower), activates the three exhaust fans which are protected by a 1 ampere circuit breaker (Figures 2 and 4). The upper reperforator shelf receives its power through the bidirectional silicon switch SST, protected by a 4 ampere circuit breaker (Sheet 9).

3.91 The power supply for the upper receiver is protected by a 5 ampere circuit breaker inside the power supply. The gate circuit for each switch is controlled by a separate pole of the POWER switch, protected by a 1 ampere circuit breaker. A thermal cutout switch removes power to the power supply and reperforator shelf when excessive cabinet temperature is detected. The lower power distribution circuits are similar to those in the upper receiver and will not be described separately.

REPERFORATOR POWER

3.92 Each reperforator shelf includes the following four motors; tape supply unwinder, chad blower, tape puller, and tape feed. The chad blower and tape supply unwinder motors run continuously as long as the POWER switch is on (Figure 10). The tape puller motor is mounted on the tape input side of the punch mechanism. The switch contacts for this motor close when the tape slack in the tape guide loop is used up. This causes the bidirectional silicon switch associated with the tape puller motor to conduct, activating the motor (Sheet 10). The switch contacts for the tape feed motor close whenever the tape feed spring becomes unwound. This causes the bidirectional silicon switch associated with the tape feed motor to conduct, activating the motor.

3.93 The power supply employs a ferroresonant transformer to regulate for line voltage variations. Five separate windings, each with a full-wave rectifier, filter capacitor, and bleeder resistor are used for the outputs of -55 volts, -12 volts, -6 volts, -5 volts, and +6 volts (Sheet 11).

3.94 The -55 volt supply is used by the punch drivers. Each punch driver has a separate 1.7 ampere circuit breaker. The -5 volt supply is used for the punch holding circuits and is protected by a 25 ampere circuit breaker. The -12 volt supply is used by the logic circuits and is protected by a 3.5 ampere circuit breaker. The +6 volt and -6 volt supplies are electronically regulated with the polarity determined by which side is grounded. Except for some resistor values and circuit breakers these two supplies are alike. Due to the fact that both supplies are similar, only one will be described.

3.95 The Q6 emitter follower carries the entire current load of the supply. The base current is supplied through emitter follower Q4. The -12 volt base current comes directly from the power supply through R12. The base current may be diverted from Q4 through Q3 and CR12. The amount of diverted current is controlled by the base current of Q3. This is partly determined by the difference in potential between the CR12 drop and the output voltage at the arm of the variable resistor R16. The voltage across CR12 is a constant 4.7 volts regardless of the current through this diode.

3.96 If the output of the -6 volt supply tends to increase, more current will flow through R17 and the upper portion of R16 into the base of Q3 and through CR12. This will cause an increased current through R12 and Q3, causing the voltage at the collector of Q3 to become more positive. This reduces the base current into Q4, which reduces the base current into Q6. This causes an increased voltage drop across Q6, tending to restore the output of the supply to normal. Similarly, a decrease in output will decrease the base current into Q3, making more base current available to Q4 and therefore to Q6. This reduces the drop across Q6 and tends to increase the output of the supply.