HIGH SPEED SEND-RECEIVE SET FOR SWITCHING SYSTEM NO. 307

ELECTRONIC CIRCUITRY - CALL CONTROL

MODULES A, B, AND G

DESCRIPTION AND PRINCIPLES OF OPERATION

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Prepared for American Telephone and Telegraph Company by Teletype Corporation

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1. GENERAL

1.01 This section provides description and principles of operation for the call control circuitry of the High Speed Send-Receive (HSSR) Set for Switching System No. 307. It is reissued to incorporate the latest engineering changes. Arrows in the margins indicate changes and additions.

1.02 The call control logic is contained in three modules (A, B, and G), the control panel (panel P), and the relay rack (rack S). Briefly, the logic is divided into send, receive, alarm and common logic interface which provide the following:

(a) Control of the HSSR Set when sending.

(b) Control of the HSSR Set when receiving.

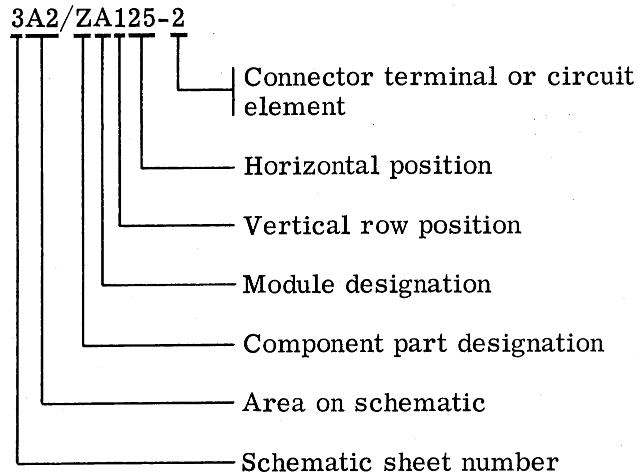
(c) Control signal interfacing between the HSSR Set and the Telephone Equipment Cabinet.

(d) Interfacing with internal circuits of the HSSR Set, ie, character generator, transmission logic, high speed punch logic, and high speed printer logic.

(e) Test switches, indicators, and test points to facilitate trouble shooting and checkout.

(f) An interface which permits connection of Test Set TS-1 in place of the Telephone Equipment Cabinet to simulate control signals between the HSSR Set and the Telephone Equipment Cabinet (TEC).

1.03 The descriptions of circuit operation in this section make reference to the schematic diagrams, which are given in another section. The circuit elements shown on these diagrams (contained in a separate section) are referenced in the text and may be located according to the following system:



1.04 The schematic diagrams for the call control logic are:

Module A - 6545WD, Sheets 1-11
Module B - 6546WD, Sheets 1-9
Module G - 6547WD, Sheets 1-4
Panel P and
Rack S - 6548WD, Sheets 1-6

2. COMPONENTS

GENERAL (Figures 1 through 8)

2.01 The call control logic is contained in the center, or control cabinet, of the HSSR Set (Figure 1) and consists of three modules of electronics (modules A, B, and G) the control panel (panel P) and the relay rack (rack S).

2.02 The modules are supported by the module framework of the cabinet and are removable on extended cables for service. The front panels of each module are equipped with test points, switches, and indicators for maintenance and checkout procedures.

2.03 The control panel, which contains operating controls and indicators, is located at the top of the cabinet. Its associated relay rack is mounted in the cabinet, immediately behind the control panel.

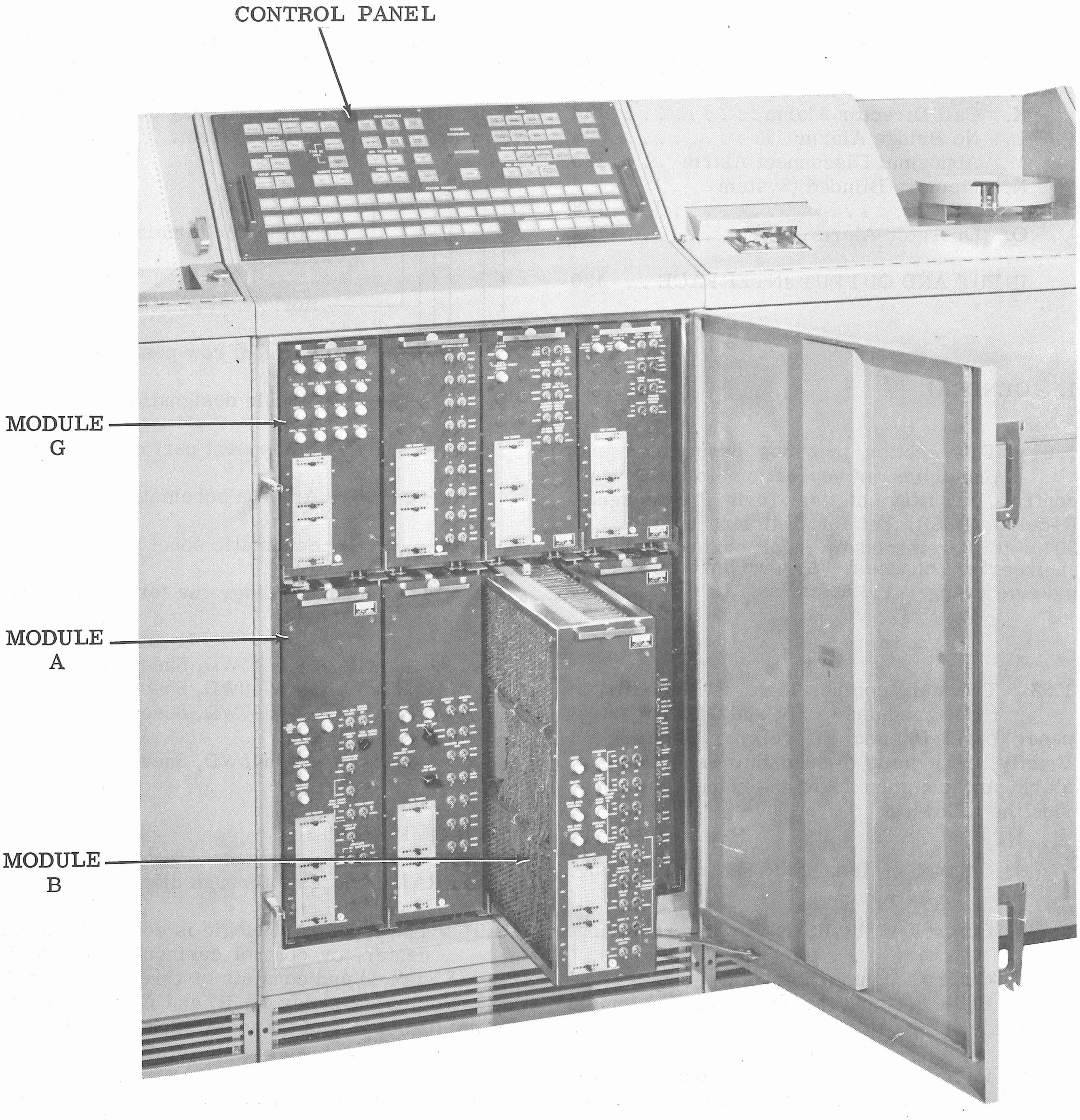


Figure 1 - HSSR Set Control Cabinet, Front View

MODULES (Figures 3 through 8)

2.04 The physical construction of modules A, B, and G is similar. Basically, the rectangular module frame contains two or three banks of connectors into which the etched-circuit cards are inserted. Wiring from the connectors is terminated in a cable assembly which interconnects with the set wiring. The module front panel contains test points, switches, and indicators. A handle is provided for removal of the module from the cabinet.

2.05 The various test points provided by each module appear as encircled numbers on the schematic diagrams.

CONTROL PANEL AND RELAY RACK
(Figures 6 and 8)

2.06 The control panel and relay rack are integral parts of the call control circuitry. The control panel (Figure 6) contains an array of indicator pushbuttons that are used by the operator for setting up the type of call required and for monitoring the progress. All alert conditions are monitored by call control logic and indicated on the control panel. The relay rack (Figure 8) contains plug-in relay circuit cards and wire spring-type relays, which operate in conjunction with the control panel, to control circuits and light the indicator lamps of the operated momentary contact pushbuttons, or to operate indicators for the trouble indicating circuits.

2.07 A brief description of the controls and indicators on the control panel follows:

(a) Transmitting mode controls, located in the upper left corner of the panel, have yellow caps. These controls determine the various send conditions. In an automatic call the operating conditions are preselected and appropriate signals are transmitted to the Telephone Equipment Cabinet and receive station(s) defining the send conditions. In a

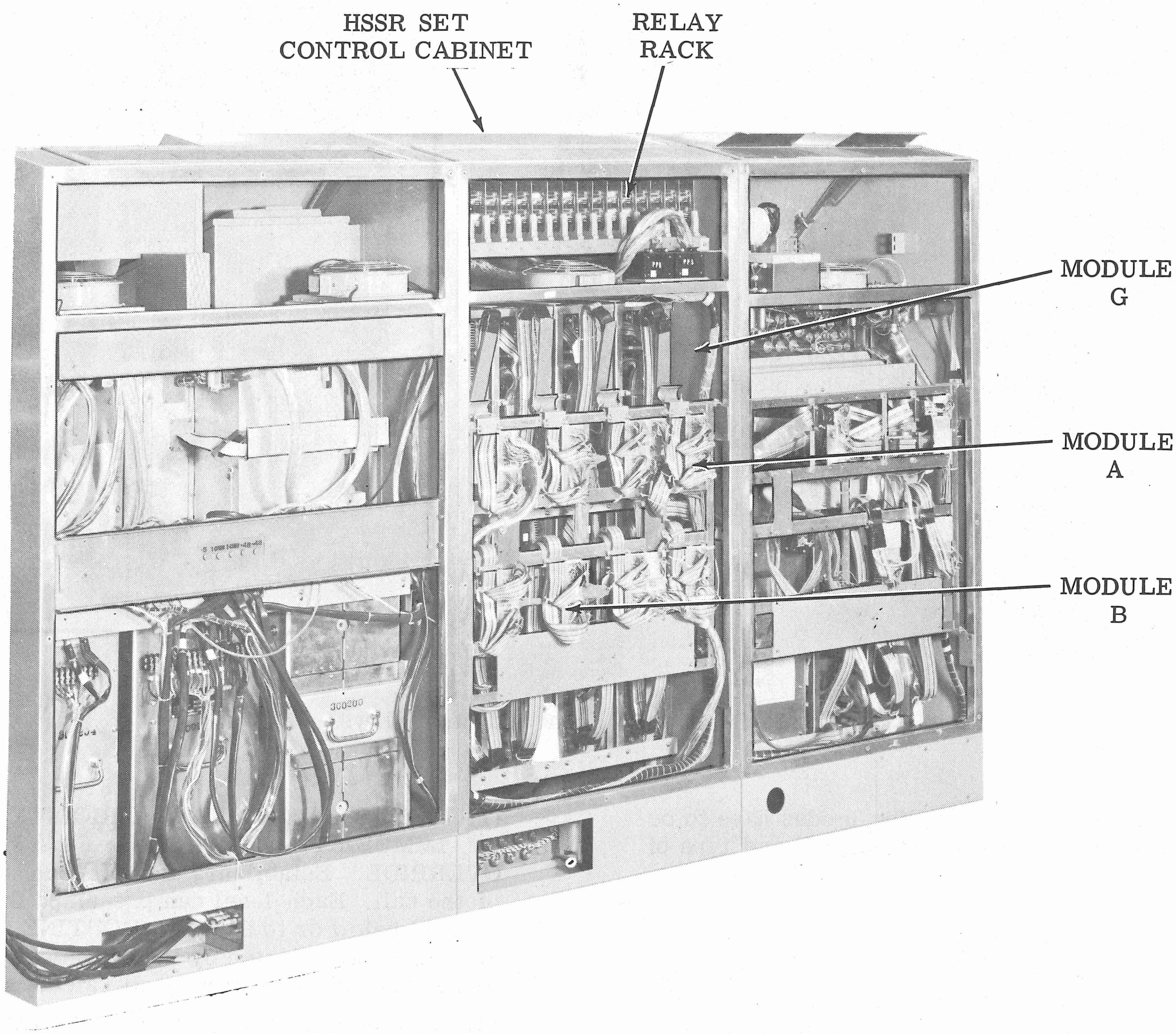


Figure 2 - HSSR Set, Rear View

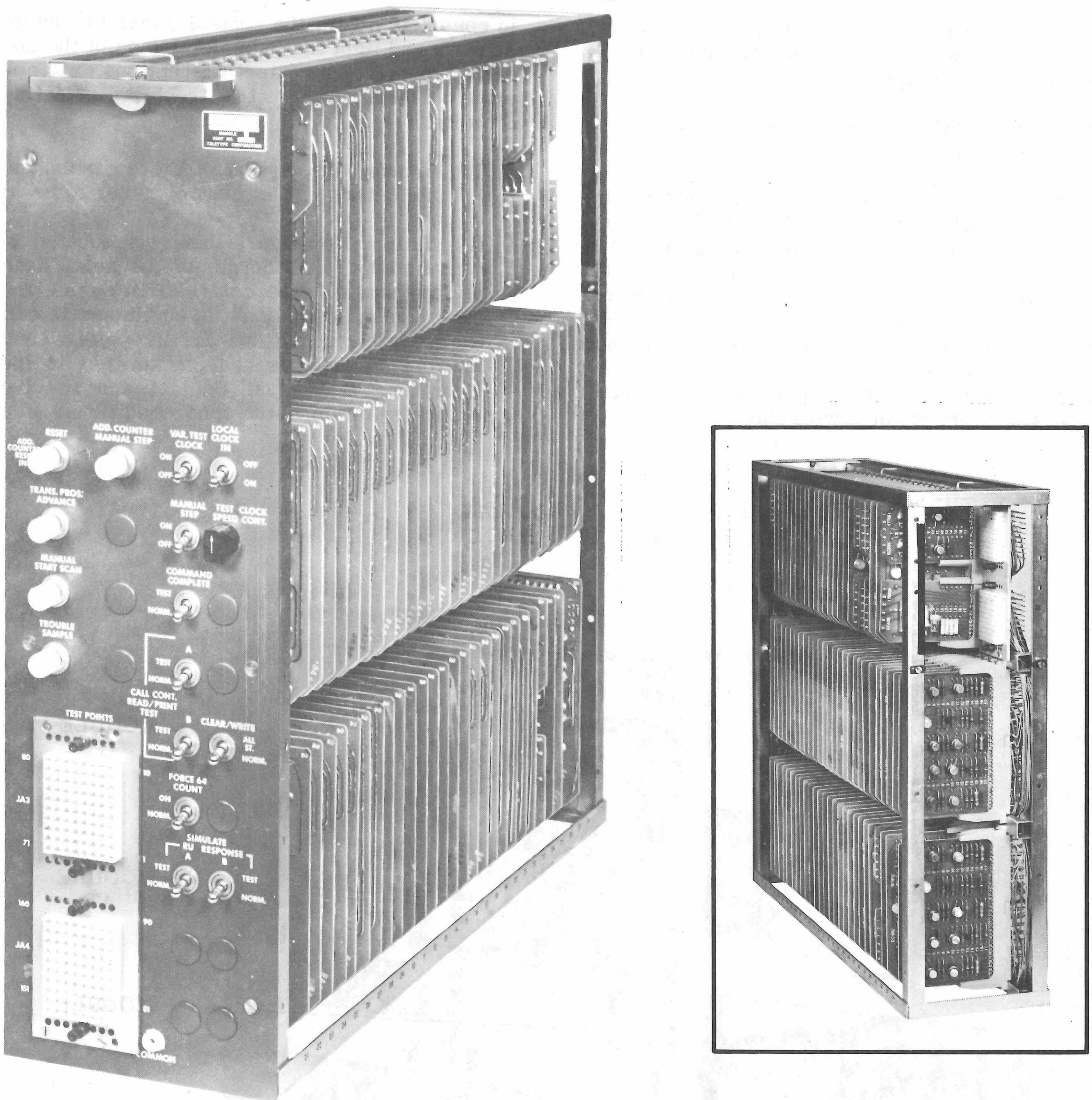


Figure 3 - Module A, Front and Rear Views

manual call like operating modes have to be arranged except for precedence and type of call.

Note: The HSSR Set is programmed to automatically select certain normal modes unless other modes are selected by the operator. The normal modes are: routine precedence, 2400 wpm, ASCII code, error detection, and remote punch off.

(1) Precedence: ROUTINE - PRIORITY - IMMEDIATE - FLASH - FLASH OVERRIDE. Establishes the precedence of the call. Each level can pre-empt the level(s) below or to the left. ROUTINE is automatically selected by the set unless a higher precedence button is operated.

(2) Type of call: BROADCAST - SINGLE - ADDRESS - MULTI-ADDRESS. Depressing the BROADCAST button auto-

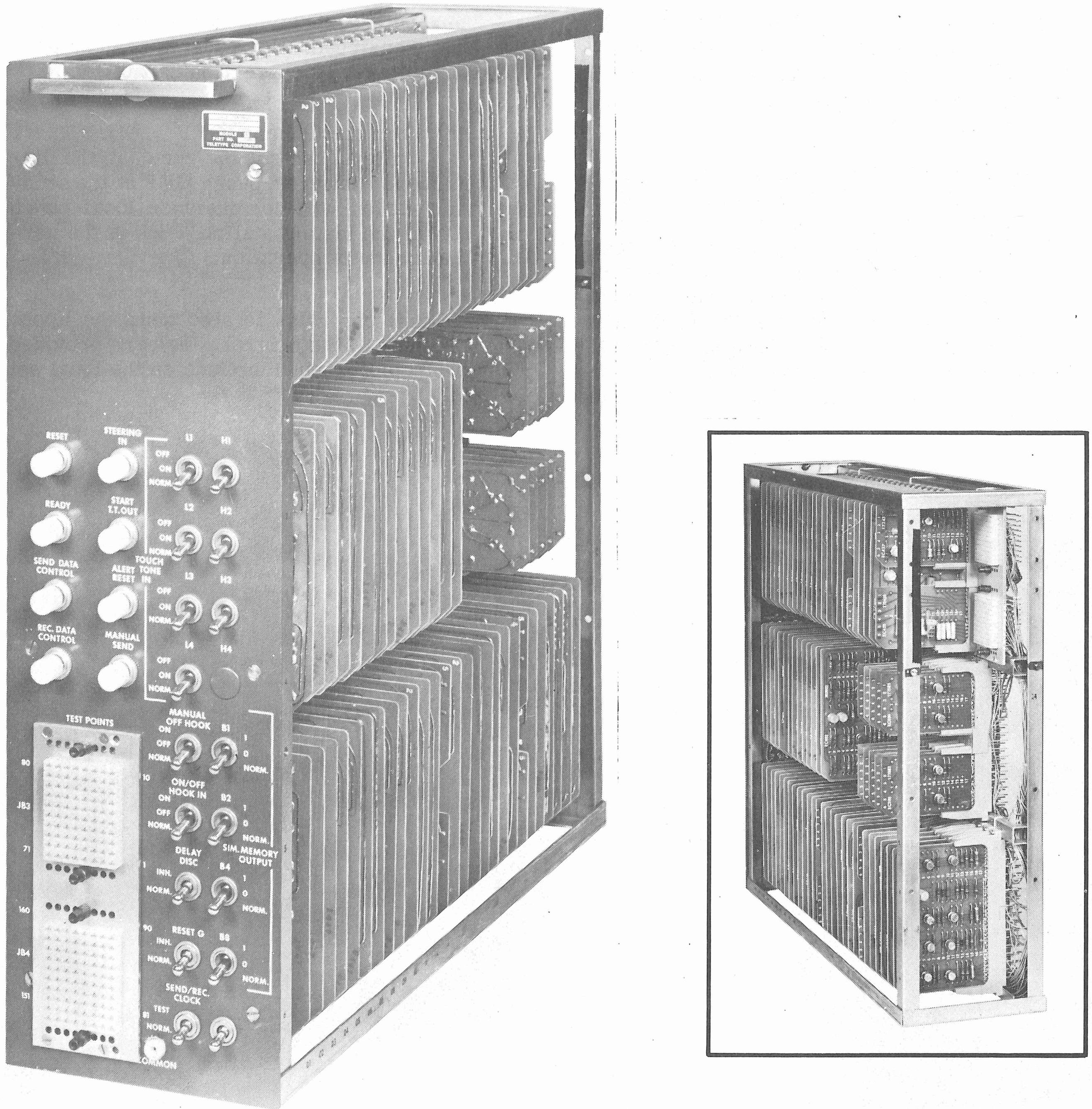


Figure 4 - Module B, Front and Rear Views

matically selects the first fifty stations and permits a message to be transmitted to these stations. All sets are equipped with the BROADCAST button but only selected sets have the capability of using it. The MULTI-ADDRESS lamp lights automatically when a call is originated to two or more stations. The SINGLE ADDRESS indicator lights automatically if a call is originated to a single station. If BROADCAST is depressed neither lamp is lighted. Both lamps are off in the reset condition.

(3) Speed: 2400 - 1200 - 600. Determines the transmission rate of the set in words per minute. 2400 is the normal mode of operation.

(4) Code: ASCII 8-LEVEL, BAUDOT 5-LEVEL. ASCII is selected when 8-level code is used. BAUDOT is selected for 5-level code. ASCII is the normal mode of operation.

(5) Error Control: DETECTION - DETECTION AND CORRECTION. DETECTION is the normal mode of operation. It is automatically selected unless the DETECTION AND CORRECTION button is depressed. This mode may be used on any type of call. The DETECTION AND CORRECTION button activates the error correction circuitry. Correction can be used only on a single address call basis and with a receiving set which is similarly equipped. Not all sets are equipped with the error correction capability.

(6) Remote Punch: OFF - ON. These buttons control the punch at the distant set. However, punch OFF at the sending station will not override local punch ON at the distant station. OFF is the normal mode of operation.

(b) Local controls, located near the upper center of the control panel, are provided to activate certain functions on the local set only.

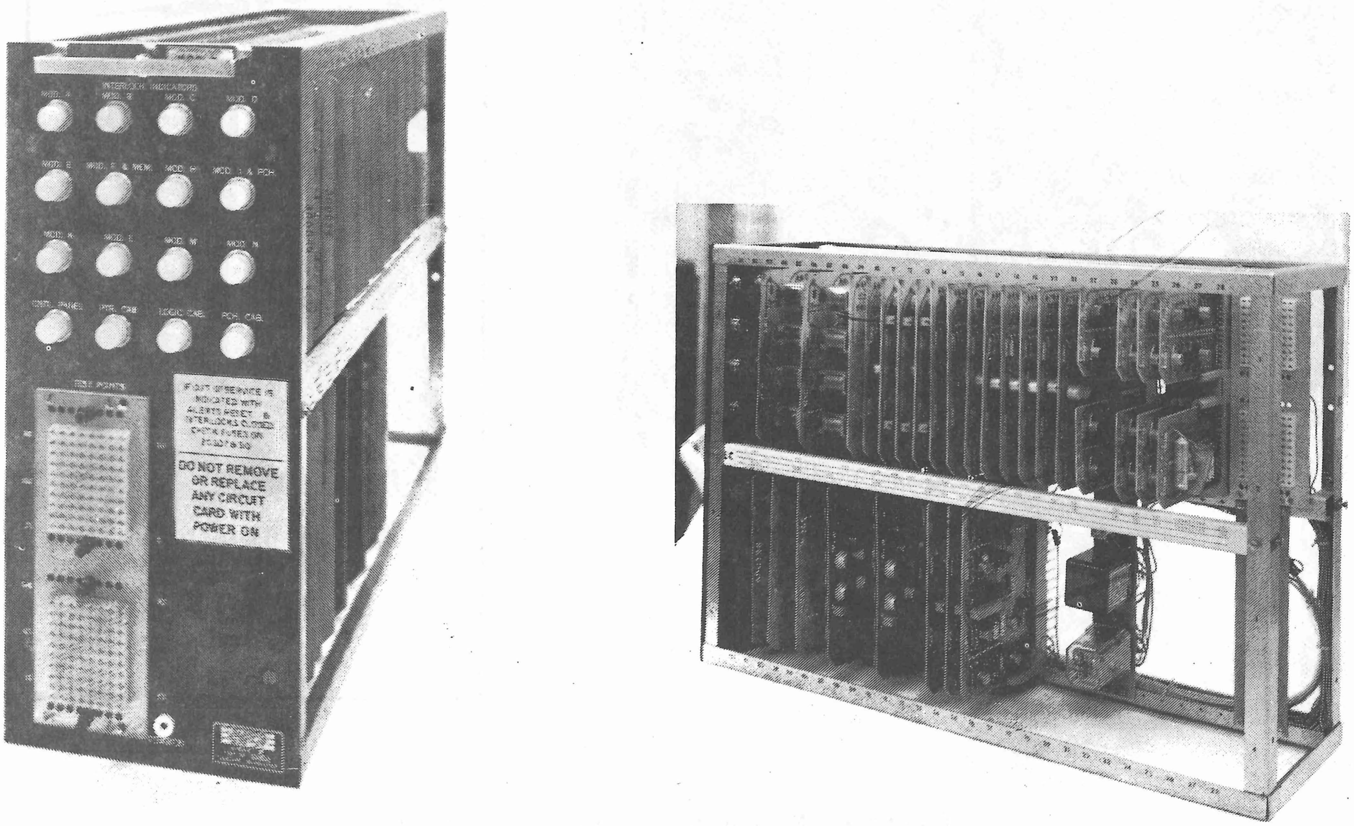


Figure 5 - Module G, Front and Rear Views

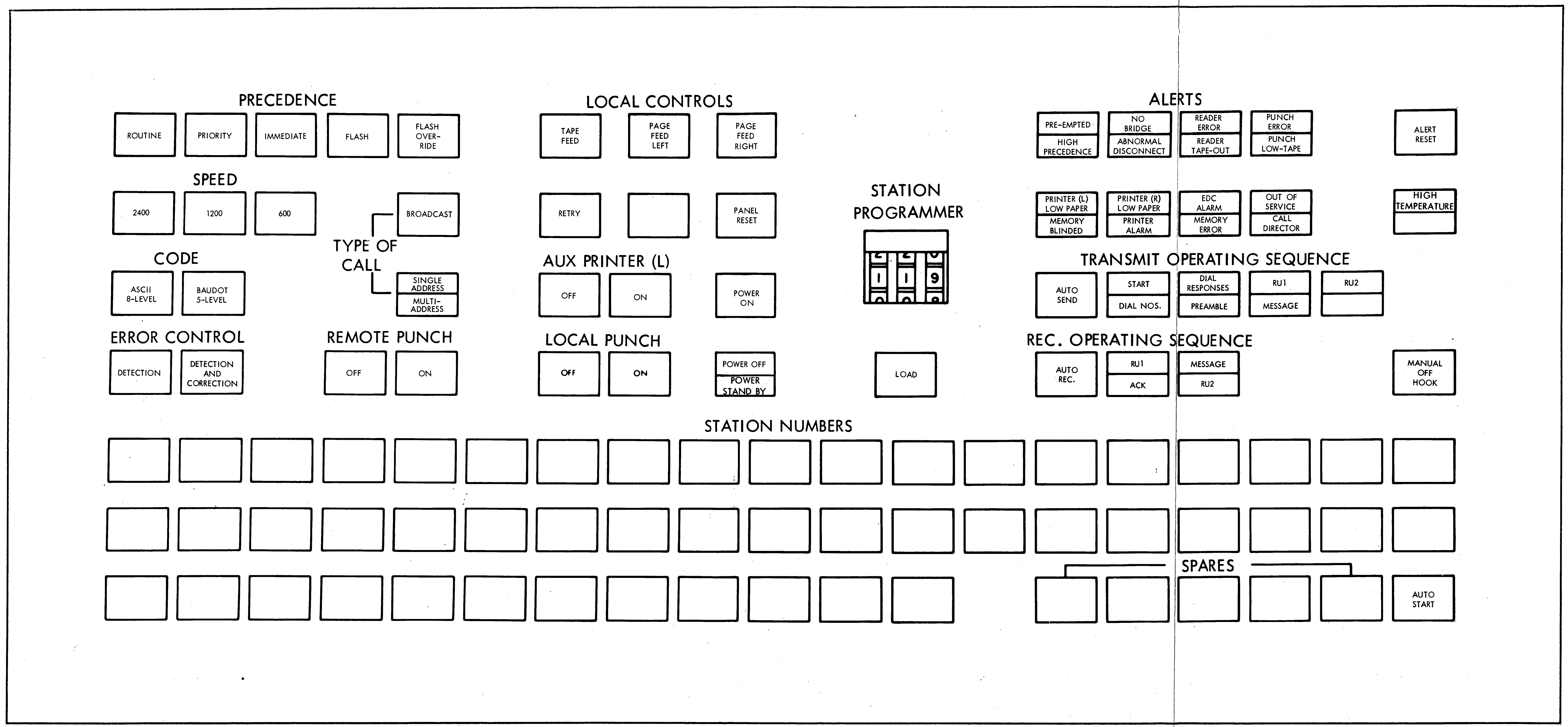


Figure 6 - Control Panel

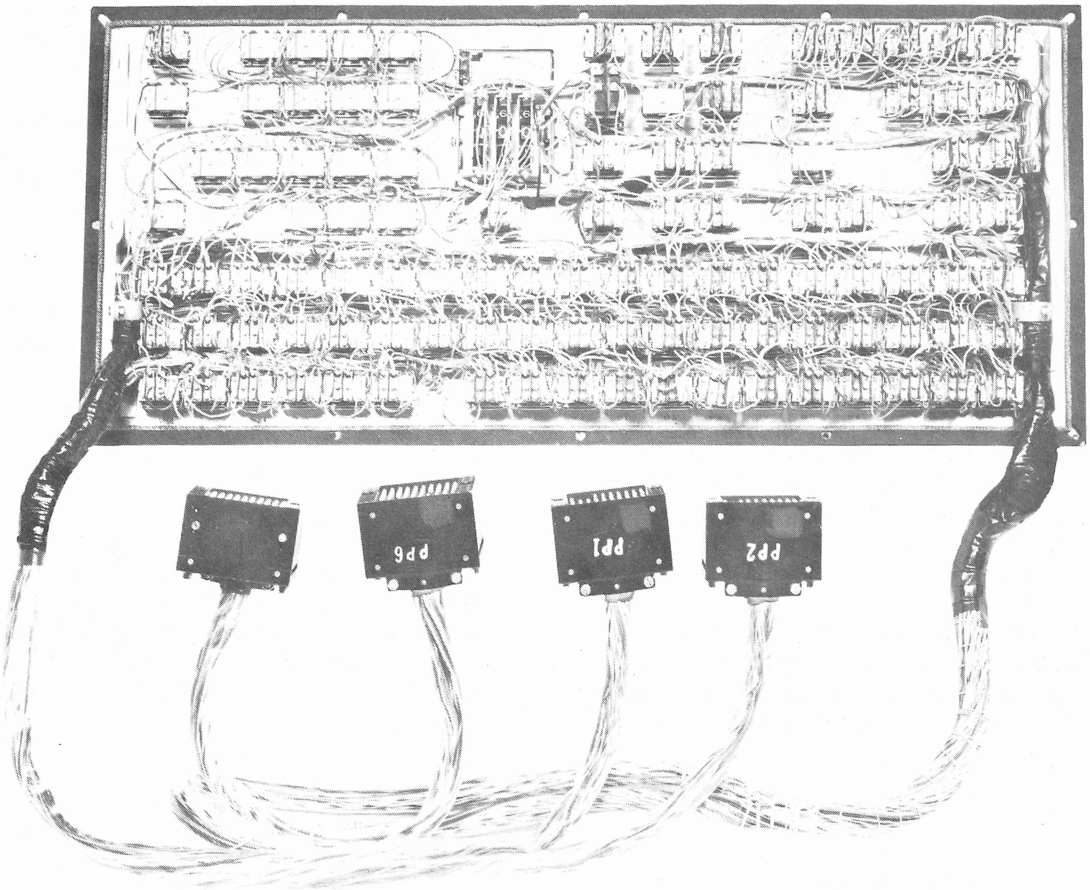


Figure 7 - Control Panel, Rear View

(1) TAPE FEED - Depressing this button causes the local punch to feed-out tape when the unit is idle. The tape is fed out and all levels punched.

(2) PAGE FEED LEFT - Depressing this button causes the left printer to feed out paper.

(3) PAGE FEED RIGHT - Depressing this button causes the right printer to feed out paper.

(4) RETRY - Depressing this button automatically reselects any called station(s) that has not received the message at the completion of a single address, multiple address, or broadcast call.

(5) PANEL RESET - Restores all logic to the reset condition including the control panel but excluding alerts.

(6) AUX PRINTER ON-OFF - Controls the auxiliary (left) printer.

(7) LOCAL PUNCH ON-OFF - Controls the local punch. If the punch has been turned on by the distant station it cannot be turned off by the local OFF button.

(8) POWER ON - Controls power for all components.

(9) POWER OFF POWER STANDBY - Turns power off within HSSR Set. With POWER STANDBY indicator lighted, dc power is applied to HSSR Set.

(c) The STATION PROGRAMMER is used for programming the station number buttons. When originating a call the HSSR Set sends the Electronic Switching System a specific 3-digit number for each station number button that is depressed. By use of the

STATION PROGRAMMER the 3-digit numbers can be added, rearranged, or deleted on the station buttons.

(1) The desired 3-digit number is set up on the programmer by rotating the appropriate wheels until the proper number appears.

(2) Selecting a particular STATION NUMBERS button or group of buttons and depressing the LOAD button loads the number set up on the programmer switch in the memory. When more than one STATION NUMBERS button is selected the programmed numbers are sequentially loaded each time the LOAD button is depressed. SPARE STATION NUMBERS buttons can be readily programmed by the operator; however, the first fifty STATION NUMBERS buttons are programmed by maintenance personnel.

(d) STATION NUMBERS pushbuttons are provided for station selection. Five SPARE buttons are provided for programming infrequently used station numbers. On single address or multiple address calls the desired stations are selected by depressing the appropriate buttons. The selected buttons become illuminated white. If a station is not connected or does not receive complete transmission for any reason that button changes to red. On broadcast calls, the buttons do not light white, but they do light red if related RU acknowledgments are not received. The buttons remain illuminated until the PANEL RESET button is operated.

(e) Automatic Start - AUTO START. When this button is depressed, it activates the HSSR Set and causes a call to be placed automatically. This button is pressed after all transmitting conditions have been selected. It has a yellow cap.

(f) Alerts are lamps provided to indicate that a condition exists that requires the attention of the operator. More than one alert may be illuminated at the same time. They apply only to the local set. These indicators have white caps that turn red when illuminated.

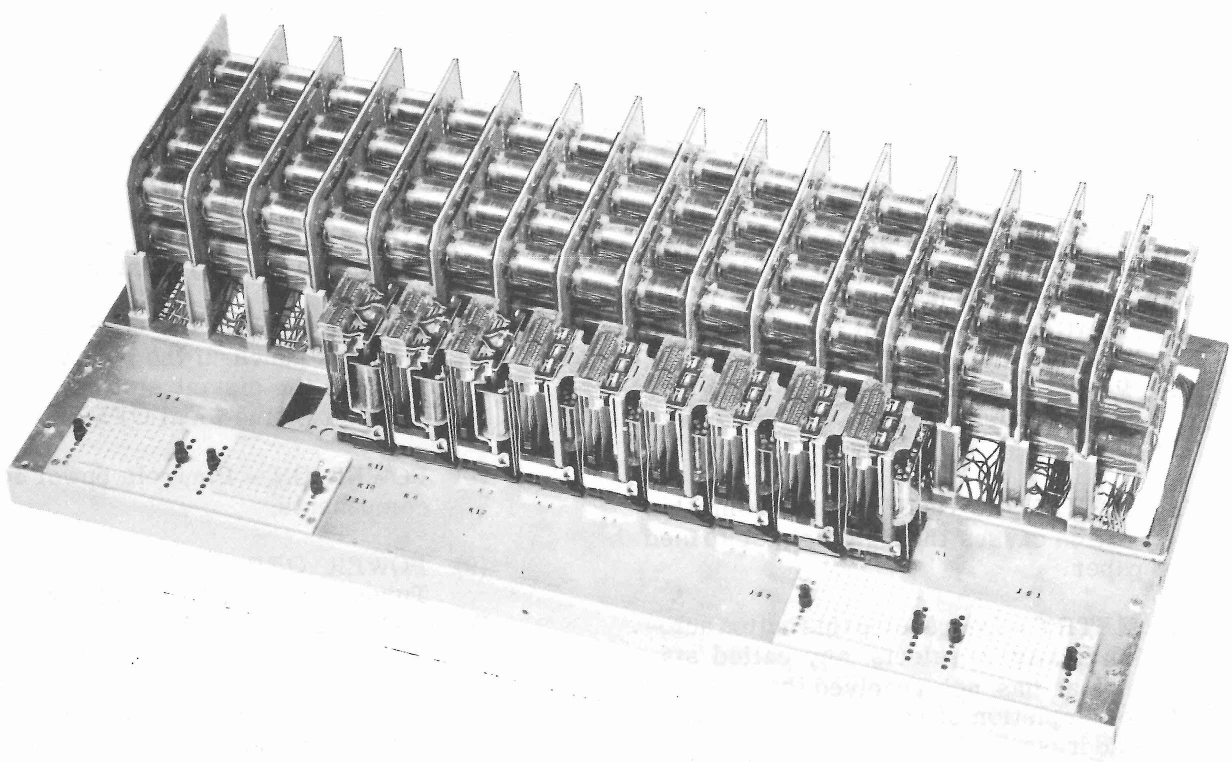


Figure 8 - Relay Rack, Rear View

(1) PRE-EMPTED - Indicates that the call in progress was disconnected because of a higher precedence incoming call.

(2) HIGH PRECEDENCE - Indicates the automatic receipt of a FLASH OVERRIDE or FLASH precedence call.

(3) NO BRIDGE - Indicates that the bridging equipment required for a multiple address call is not available at the switching center.

(4) ABNORMAL DISCONNECT - Indicates an abnormal condition has occurred which caused the HSSR Set to automatically disconnect.

(5) READER ERROR - Indicates improper feeding or sensing of the tape in the reader. When operating in the error correction mode, READER ERROR will cause the set to disconnect (reset).

(6) READER TAPE OUT - Indicates no tape in the reader at the beginning of the transmit sequence. The call will not proceed.

(7) PUNCH ERROR - Indicates that the punch has not properly perforated or a punch feed problem has occurred. In the error correction mode, a punch character error (PUNCH ERROR) will cause the set to disconnect. The occurrence of a punch feed error causes the set to reset.

(8) PUNCH LOW TAPE - Indicates a low tape condition in the punch. If a message is being transmitted or received it will be completed. The set will then automatically be placed out of service until the condition is corrected.

(9) ALERT RESET - Depressing this button restores the alert to normal after the condition has been corrected.

(10) PRINTER (L) LOW PAPER - This lamp indicates a low paper condition in the auxiliary printer. Any message in progress will be completed, and the set will automatically be placed out of service until the condition is corrected.

(11) MEMORY BLINDED - Indicates a failure in the dc supply of the system.

(12) PRINTER (R) LOW PAPER - Indicates a low paper condition in the primary printer. Any message in progress will be completed and then the set will automatically be placed out of service until the condition is corrected.

(13) PRINTER ALARM - Indicates a failure in the printer high voltage supply.

(14) EDC ALARM - This lamp will light only if the set is in the error detection and correction mode. It indicates that the set has failed to correct an error after several tries. The set will reset.

(15) MEMORY ERROR - Indicates a malfunction of the memory in reading stored data. It will cause a disconnect if the set is in the error correction mode or in the process of dialing.

(16) OUT OF SERVICE - Indicates that the set has been placed out of service. It is caused by such conditions as low ink, low paper, low tape, and opening the cabinet doors or leaving set in test condition.

(17) CALL DIRECTOR - Indicates a malfunction in the call director or associated control equipment.

(g) TRANSMIT OPERATING SEQUENCE lamps enable the operator to observe the progress of an outgoing call while it is automatically handled by the set.

(1) AUTO SEND - Indicates automatic call transmission. The indicator lights when the AUTO START button is depressed and remains lighted until the call is completed.

(2) START - Lights when the AUTO START button is depressed. It indicates that the call sequence has begun and extinguishes before the next lamp lights.

(3) DIAL NOS - Indicates that the selected stations are being dialed.

(4) DIAL RESPONSES - When this lamp lights, responses are being received from the ESS indicating the status of the called stations. The responses indicate to the transmitting set whether the called stations are connected, busy, or out

of service, or whether they were dialed correctly (RU order).

(5) PREAMBLE - Indicates the set is transmitting information to the distant stations regarding the transmitting modes.

(6) RU1 - The sending station polls the distant stations digitally by sending the call numbers to verify that they are still connected, and have synchronized, prior to transmitting the message.

(7) MESSAGE - Indicates that the message is being transmitted.

(8) RU2 - This lamp indicates that the sending station again polls the distant stations to determine if they are still connected. This mode is the same as RU1 except it occurs after the message has been transmitted.

(h) REC. OPERATING SEQUENCE lamps enable the operator to observe the progress of an incoming call while it is automatically handled by the set.

(1) AUTO REC. - Indicates receiving a call in the automatic mode. It remains lighted until the call is completed.

(2) RU1 - This lamp indicates that the set has synchronized and is waiting for the transmitting station to query it to see if it is connected.

(3) ACK - Indicates that the set has returned an acknowledgment to the sending set.

(4) MESSAGE - Lights while the message is being received.

(5) RU2 - Indicates that the receiving station is waiting for the transmitting station to question it to see if it is still connected. As soon as the station recognizes its RU, and acknowledges, the RU2 lamp extinguishes and the station disconnects.

(i) MANUAL OFF-HOOK - This lamp indicates that a call is being made manually from the call director associated with the HSSR Set.

3. TECHNICAL DATA

CALL CONTROL INTERFACE WITH CABINET FILTERS

A. Output Signals (Call Control Logic to Filters)

On/Off Hook Out	6 v On, 0 v Off. Indicates HSSR Set is in process of receiving or sending an automatic call.
Send Data Control	-6 v Off, 0 v On. A signal to telephone control to switch out the tone transmitter and switch in the data set (send) on the outgoing line and start synchronizing the data sets and customer equipment at the send station.
Receive Data Control	6 v Off, 0 v On. A signal directing the telephone control to switch out the tone receiver and switch in the data sets on the incoming line and start synchronizing the data set and customer equipment at the receive station.
Tone-Out	6 v Off, 0 v On. Consists of 8 leads in addition to steering lead which terminates at the tone transmitter. A combination of a low (L) and a high (H) representing two dc pairs, along with the steering lead, are necessary to enable the tone transmitter to send 1 of 16 discreet tones. L1 L4 H3 L2 H1 H4 L3 H2 Steering

Information Rate	-6 v Off, 0 v On. Two control leads which the send and receive sets utilize to switch clocks derived in the data set to the appropriate bit rate of 2400, 1200, or 600 bits per second. (a) 1200/2400 bps, -6 v 1200, 0 v 2400 (b) 600 bps; -6 v Off, 0 v 600
DC Precedence	-6 v Off, 0 v On. A group of four leads used to signal the Telephone Equipment Cabinet the level of precedence of an automatically derived call. Flash Override Immediate Flash Priority
Send Data	-6 v Mark, 0 v Space. Lead on which the serial data from the serializer is subsequently presented to the data set.
Operator Alert	-6 v Off, 0 v On. A signal used to control an audible alarm external to the HSSR Set for the purpose of summoning the operator when the incoming call is high precedence or when a station is pre-empted.
Equipment Alarm	-6 v Off, 0 v On. A signal used to control an audible alarm external to the HSSR Set for the purpose of summoning the operator as a result of an equipment failure within HSSR Set.

B. Input Signals (Cabinet Filters to Call Control Logic)

On/Off Hook In	-6 v On-Hook, +6 v Off-Hook. A signal to the HSSR Set indicating a connection to a distant station.
Manual Off-Hook	-6 v On-Hook, +6 v Off-Hook. A signal indicating the telephone handset on the call director external to HSSR Set is off-hook and a voice coordinated call (manual) is in progress.
Manual Send	-6 v Off, +6 v On. A control signal when the send data transfer key is operated on the call director during a voice coordinated call.
Ready	-6 v Off, +6 v On. A signal indicating that the data sets and customer equipment are synchronized and the HSSR Set may start to send or receive data.
Pre-empted	-6 v Off, +6 v On. A signal to the HSSR Set when the set is off-hook and connected to a distant station indicating a higher priority incoming call.
Tone-In	-6 v Off, +6 v On. Consist of 8 leads in addition to a steering lead presented to the HSSR Set indicating combination of tones detected by the tone receiver located in the Telephone Equipment Cabinet. For each discrete tone signal received, a combination of dc pairs, a low (L) and a high (H) along with a steering signal is generated by the receiver and presented to the call control. L1 L4 H3 L2 H1 H4 L3 H2 Steering

Receive Data	-6 v Mark, +6 v Space. Serial data input from the receive portion of the data set.
Send Clock	-6 v to +6 v square wave derived in the data set and occurring at the bit rate specified by the HSSR Set on information rate leads of 2400, 1200, or 600 bits per second.
Rec Clock	Same as above except in phase with the receive data.
Telephone Equipment	-6 v Alarm, +6 v No Alarm. A signal from Telephone Equipment Cabinet indicating trouble condition existing in the equipment.

INTERFACE WITH CHARACTER GENERATOR LOGIC

A. Output Signals

Address Leads	Consist of seven leads on which address information is presented to the character generator logic address register. Signals -6 volts (the 0 condition), 0 volt (the 1 condition).
Memory Load	Twelve leads derived from the station programmer used to load information in memory; -6 volts (0), 0 volt (1).
Read/Restore	A command asking for information at a particular address to be read out of memory and restored; 0 volt - off, -6 volt - read/restore signal.
Clear/Write	A command presented to the character generator logic to facilitate writing new information into the memory at a particular address; 0 volt - off, -6 volts - clear/write signal.
Memory Shift	Negative pulses to character generator logic to shift information stored in output buffer.
Memory Control	A signal indicating call control in EDC logic using the memory; 0 volt - EDC, -6 volts - call control.
System DC OK	Signal from dc monitoring circuit to memory to blind memory inputs if the dc volts drops below a reference level; -6 volts - OK, 0 volt - blind.
Column Advance	Square wave signals presented at a 2 kc rate to column advance the printer.
Auxiliary Printer On/Off	Signal to permit local printer (L) to be turned on; -6 volts - off, 0 volt - on.
Page Feed (R)	A signal from the control panel pushbutton to permit the right page printer to feed out paper at a 100 ms rate.
Page Feed (L)	Same as above except for left printer.

B. Input Signals

4kc Clock	Square wave clock signal which is always present to provide a local clock for the logic.

Command Sample	A 0 to -6 volt signal indicating read/restore or clear/write command has been recognized by the character generator logic.
Memory Output	Four information leads from character generator output buffer representing data read out of memory; 0 volt (0), -6 volts (1).
Memory Parity Error	A signal indicating a memory parity error; 0 volt - error, -6 volts - no error.

INTERFACE WITH TRANSMISSION LOGIC

A. Output Signals (Signals to Transmission Logic)

Send/Receive	-6 volts - receive condition, 0 volt - send condition.
Manual/Automatic	-6 volts - automatic condition, 0 volt - manual condition.
ASCII/Baudot	6 volts - ASCII code, 0 volt - Baudot code.
ED/EDC	6 volts - error detection, 0 volt - error detection and correction mode.
Punch ON/OFF	6 volts - punch off, 0 volt - punch on.
Character Available	A signal to serializer indicating call control character available; 0 volt - no character available, -6 volts - character available.
Parallel Data	Seven leads on which parallel data is presented to the transmission logic serializer for sampling; -6 volts - space, 0 volt - mark.
Send Clock	Square wave (-6 to 0 volt) clock occurring at the 2kc rate, or specified bit rate depending on operating conditions.
Receive Clock	Same as send clock except it is in phase with receive data.
Deserializer Input	Serial data which is gated and subsequently presented to the local deserializer input; -6 volts - space, 0 volt - mark.
Start Message	0 volt - off, -6 volts - start message.
Error Control Tones	Four leads on which error detection and correction answer-back signals (-6 to 0 volt) are presented to the EDC logic representing status of transmitted blocks.
Transmission Logic Reset	A -6 to 0 volt pulse for the purpose of resetting the transmission logic. Character generator logic is reset by the same pulse.

B. Input Signals (Signals from Transmission Logic)

Serial Data	Data from local deserializer, -6 volts - space, 0 volt - mark.
Character Clock	A negative clock (0 to -6 volts) signal, one bit wide, occurring at the character rate.
Delayed Character Clock	Same as above except delayed one bit with reference to the character clock signal.

Receiver in Sync	A signal indicating deserializer is synchronized; 0 volt - not synchronized, -6 volts - synchronized.
Send RU2	A negative signal indicating message has been transmitted and to start the second RU query.
RU Received	A positive pulse from the transmission logic receiver indicating station RU has been detected.
RU1 Mode	A negative signal from the transmission logic receiver indicating it is in the RU1 mode.
Start of Message (SOM)	A negative signal from the transmission logic receiver indicating set has acknowledged.
Receiver Unblind	A negative signal indicating a start of message sequence has been recognized.
Receiver RU2 Mode	A negative signal indicating an end of message sequence has been recognized.
Answer-Back Sample	A negative pulse used to sample EDC answer-back conditions.
Answer-Back Signals	Four leads on which 0 to -6 volt signals are received which represent EDC block status.
Receiver Auto Call Complete	A 0 to -6 volt signal indicating second RU has been detected.
RU Format Alarm	A 0 to -6 volt signal indicating RU was not detected prior to start of message.
Reader Tape Out	0 volt - tape in, -6 volts - tape out.
Reader Verify Error	0 volt - no error, -6 volts - error.
Reader Feed Error	0 volt - no error, -6 volts - error.
EDC Memory Parity Error	0 volt - no error, -6 volts - error.
EDC Alarm	0 volt - no alarm, -6 volts - alarm condition.

INTERFACE WITH PUNCH AND PUNCH LOGIC

A. Output Signals

Tape Feed	A ground signal to feed out tape in the local punch.

B. Input Signals

Low Tape	A negative signal (0 to -6 volts) indicating low tape condition exists.
Punch Feed Error	0 volt - no error, -6 volts - error.
Punch Feed Error	0 volt - no error, -6 volts - error.

INTERFACE WITH PRINTERS (Inputs from Printer Only)

Low Paper (L)	0 volt - paper in, -6 volts - low paper.
Low Paper (R)	0 volt - paper in, -6 volts - low paper.
Printer Alarm	0 volt - ok, -6 volts - no printer high voltage.

INTERFACE WITH TEST SET TS-1

Interface leads to and from Test Set TS-1 which simulate inputs and outputs from the Telephone Equipment Cabinet.

4. GENERAL OPERATION

OVERVIEW

A. Types of Calls (Figure 6)

4.01 The call control logic provides the HSSR Set with the facilities for originating or receiving two types of calls: manual or automatic. Manual calls are single address (point-to-point) and are initiated and concluded under telephone control through facilities provided by the associated Call Director Sets.

4.02 Automatic calls may be single address, multiple address (from 2 to 50 stations), or broadcast (50 stations).

B. Control and Operating Modes (Figure 6)

4.03 The call control logic provides selection of the HSSR Set operating modes, by the operator, when preparing the set for a call. There are two types of operating modes:

(a) Those modes which affect the Telephone Equipment Cabinet (precedence and addressing).

(b) Those modes which affect the sending and receiving HSSR Sets (speed, code, error control, and remote punch condition).

4.04 When the HSSR Set is idle (reset), the control panel indicates the following conditions:

- Precedence - routine
- Speed - 2400 wpm
- Code - ASCII
- Error Control - Error detection
- Remote Punch Condition - Off

The above indications can, of course, be changed manually at the discretion of the operator.

Telephone Equipment Cabinet Control

4.05 Precedence: When originating an automatic call, the operator may choose one of five levels of precedence; routine, priority, immediate, flash, and flash override. The relative precedence information is forwarded to the Telephone Equipment Cabinet via dc precedence leads on which the precedence level signal is presented throughout the call, and by sending a combination of dc signals indicating a particular level of precedence during the start mode.

4.06 Single Address: Originating an automatic call with a single station number button depressed constitutes a single address call. The call control logic automatically determines that the call being originated is a single address (point-to-point) call, and indicates this mode. No information is forwarded to the telephone control.

4.07 Multiple Address: If two or more station number buttons are selected by the set operator, the call control logic automatically determines that the call being originated is a multi-address call and indicates this condition. Pertinent control information is forwarded to the Telephone Equipment Cabinet in the form of dc signals via the tone-out logic, which indicate that a multi-address call is being originated and a dialing bridge is requested.

4.08 Broadcast: The operator may select this mode of operation which is an abbreviated form of a multi-address call. Control signals are forwarded to the Telephone Equipment Cabinet and subsequently the ESS to arrange for this type of call.

Send-Receive Control

4.09 Control Link: Control of the receiving station can be accomplished in either of two ways: Control can be performed automati-

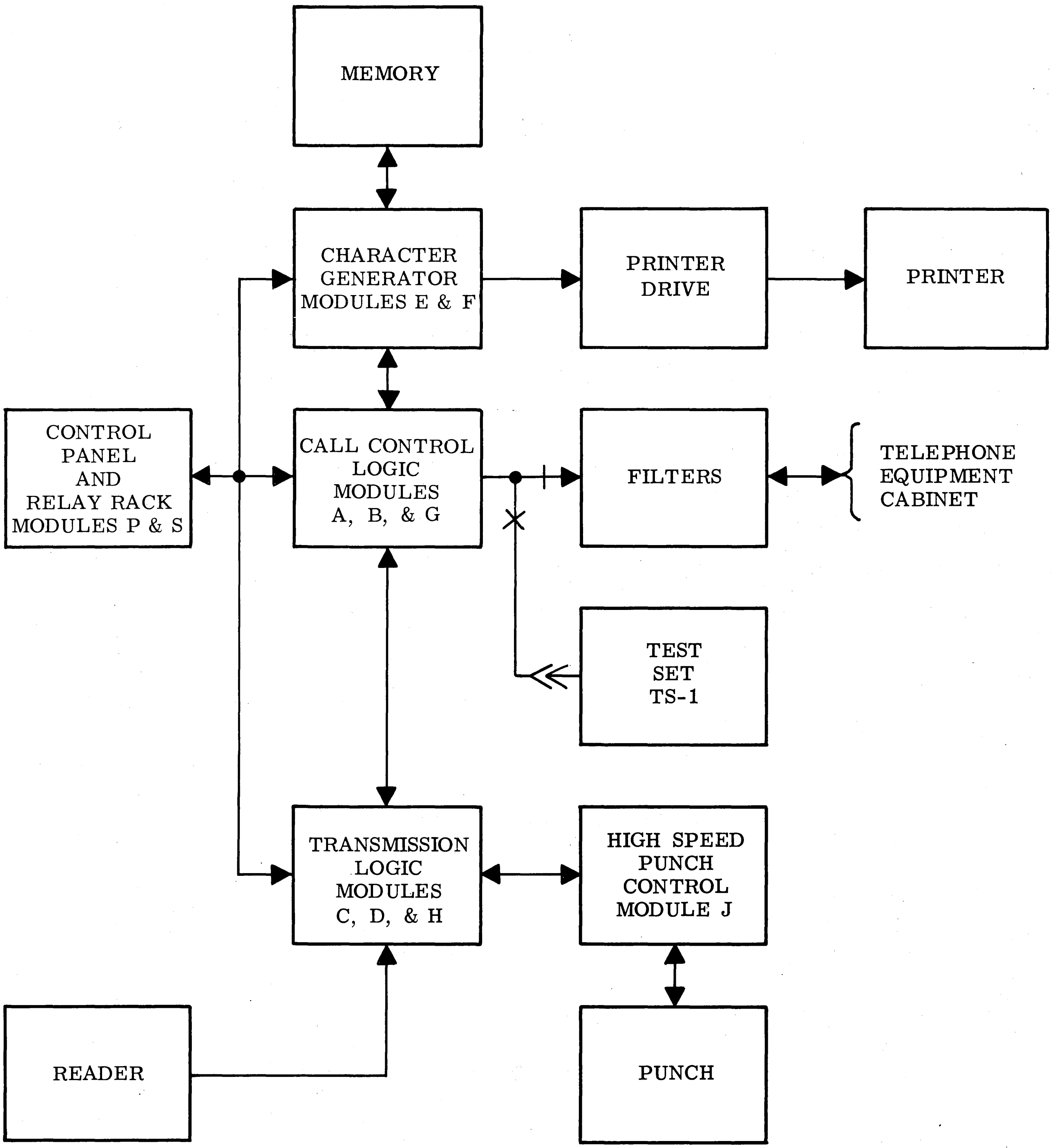


Figure 9 - HSSR Set, Block Diagram

cally through use of control tones which are generated at the sending station and transmitted during the preamble when an automatic call is in progress. The receiving station(s) decodes the information and the proper operating conditions are automatically programmed into the receiving set. Control of the receiving HSSR Set can also be performed manually by the receiving operator in accordance with verbal instructions given by the sending operator via the voice connection (manual).

4.10 Speed: Pertinent speed control information is forwarded to the Telephone Equipment Cabinet and subsequently to the data sets on the information rate leads. Speeds of 2400, 1200, or 600 words per minute are available.

4.11 Code: Messages may be transmitted in either ASCII (8-level) or Baudot (5-level) at the operator's discretion.

4.12 Error Control: Transmissions may be initiated in the error detection (ED) mode or the error detection and correction (EDC) mode. In the error detection mode the transmitted data is checked for errors at the local send station and at the receive station. The page copy is appropriately marked to indicate those lines in which an error is present. When

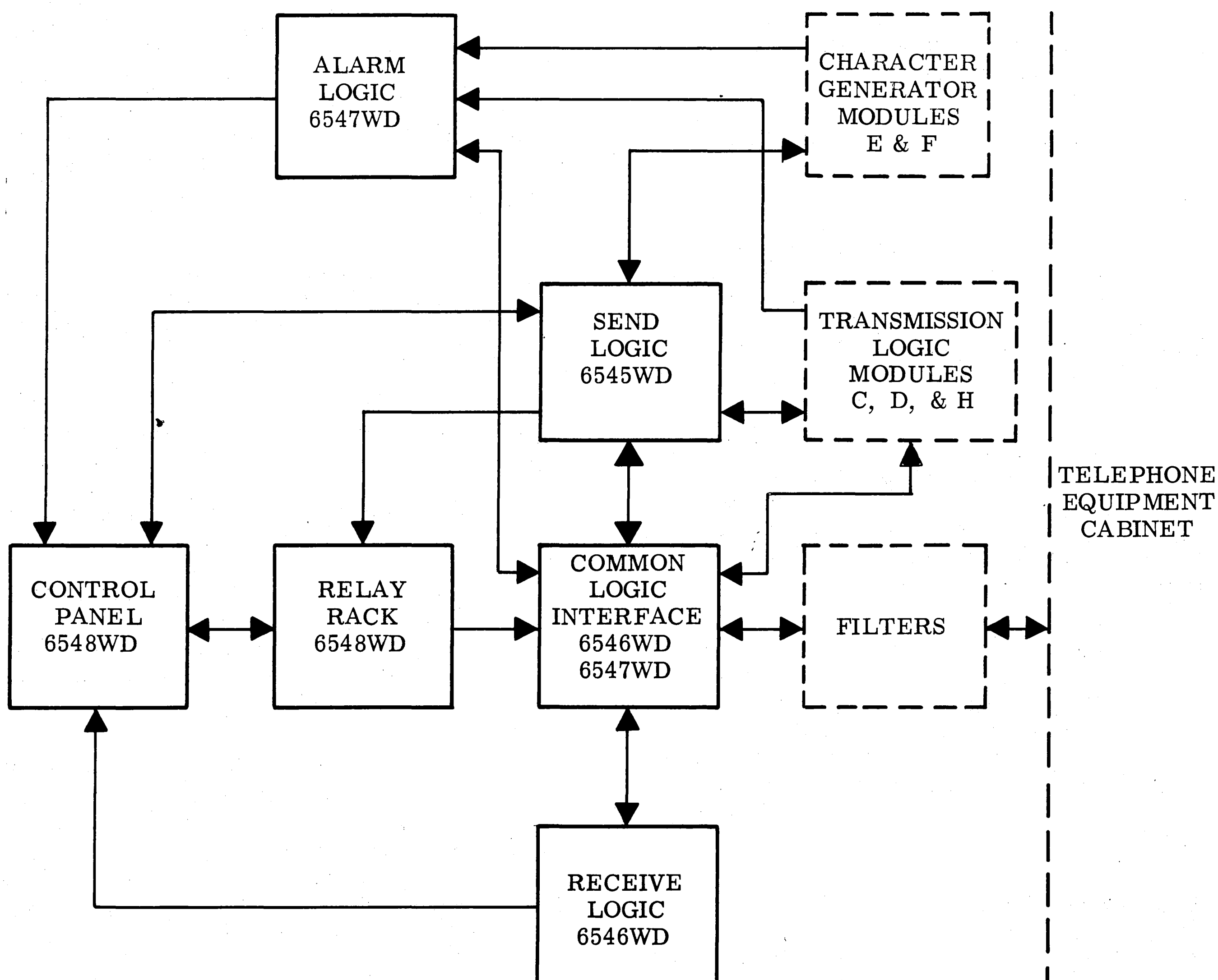


Figure 10 - Call Control Logic, Block Diagram

operating in this mode, transmission is not limited to single address calls.

4.13 When operating in the error detection and correction mode (EDC) data is transmitted in 80-character blocks. Each block is stored and checked. Any errored block is retransmitted. When operated in this mode, transmission is limited to single address calls. If multi-address or broadcast calls are attempted, the HSSR Set will reset and disconnect.

4.14 Remote Punch Condition: At the option of the sending operator the transmitted message may be automatically punched at the receiving HSSR Set. Pressing the REMOTE PUNCH ON button at the sending station will override a LOCAL PUNCH OFF condition at the receiving station. The sending station cannot, however, turn off the receive station punch if it is in the LOCAL PUNCH ON condition.

C. Manual Send (Voice Coordinated) Calls

General

4.15 When the HSSR Set is operated as a sender, the transmission logic (modules C, D, & H) serializer and deserializer are coupled together so that all the data locally generated is deserialized and presented to the monitoring printer.

4.16 Furthermore, when the HSSR Set is operated in the manual mode, the call control circuits regulate the initial phases of the call, and the various operating modes. The transmission logic is in control of the set during the sending of the message.

4.17 In all cases, the operator has complete control of the HSSR Set, and may interrupt a call in progress by resetting the set. Also, the Telephone Equipment Cabinet may forward a pre-empt or an on-hook (disconnect) signal to the call control logic in which case, the HSSR Set will reset and await further instructions.

Sequence (Figure 11)

4.18 The simplest type of call from a logic standpoint is a voice coordinated or manual call in which the HSSR Set operator desiring to send prepares the HSSR Set prior to placing a call to a distant station.

4.19 The manual call is initiated at a Call Director Set external to the HSSR Set, by dialing out a 7-digit number peculiar to the station being called. If the called station is not busy, an off-hook with a ringing signal is received by the Telephone Equipment Cabinet and forwarded to the Call Director Set at the receive station. The receive operator answers this ringing using the telephone handset at the Call Director. Having thus established verbal contact, the sending operator can instruct the receive operator to set up the proper operating modes.

4.20 Next, the operator at the sending station presses the SEND DATA button on the Call Director, and the operator at the receive station presses the RECEIVE DATA button. Both operators then return their handsets to their cradles. This action removes the voice connection and begins the synchronization process between the sending and receiving data sets, and the customer furnished equipment. The completion of the synchronization process causes a signal on the ready lead at the send and receive sets. The send and receive sets respond to this signal as follows:

(a) At the sending station, the ready lead signal unblinds the send clock and the send data leads and also starts a message-start timing circuit.

(b) At the receiving station, the receive clock and receive data lead are unblinded.

(c) The timing circuit at the sending set permits the local transmission logic deserializer to synchronize on delete characters being generated by the set serializer. It requires a minimum of four delete characters to synchronize. When the time out is completed, the reader is started, and the message is transmitted.

4.21 Upon completion of the message, the set operators remove their respective handsets from the cradle and press their DATA TRANSFER key, SEND DATA or RECEIVE DATA, whichever is the case. The ready signal is removed, the clock and data leads are blinded, and voice contact is re-established. The operators agree, by verbal confirmation, that the message was transmitted and received properly and the call is concluded when the handsets are replaced on the cradle resulting in an on-hook (disconnect) condition.

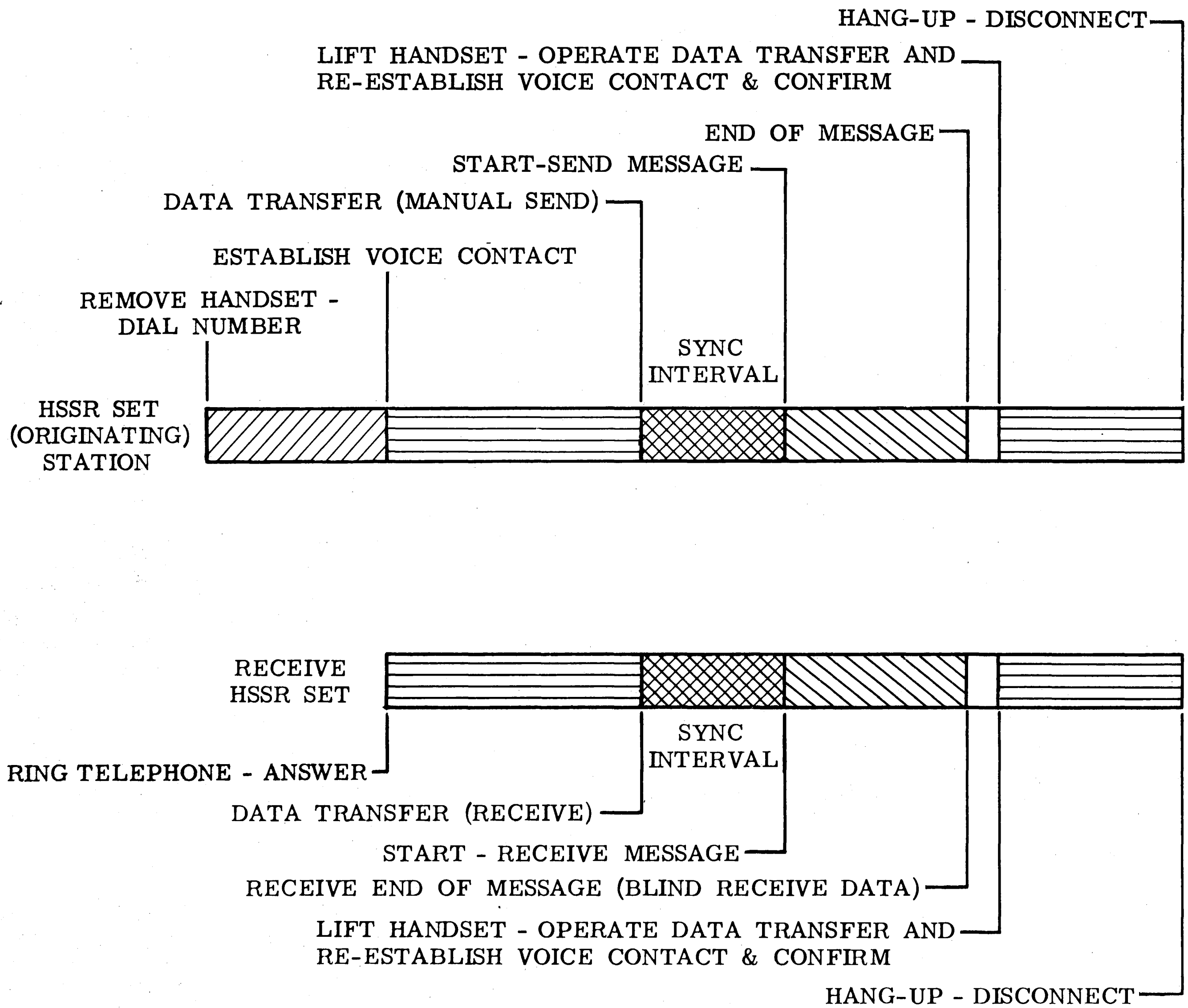


Figure 11 - Manual Call Sequence

D. Automatic Send Calls

General

4.22 Automatic send calls may be single address, multi-address, or broadcast. As in the case of the manual send calls the transmission logic serializer and deserializer are coupled together so that locally generated data is deserialized and presented to the monitoring printer.

4.23 Furthermore when the HSSR Set is operated as an automatic sender the call control logic:

(a) Sends and receives instructions to and from the Telephone Equipment Cabinet.

(b) Sends and receives instructions to and from the connected receiving station.

(c) Relinquishes automatic control of the HSSR Set to the transmission logic; however, it may override this control as a result of certain conditions.

4.24 Again, as in the manual send call, the operator has complete control of the HSSR Set and may interrupt a call in process by resetting the set. Also, the Telephone Equipment

Cabinet may forward a pre-empt or an on-hook (disconnect) signal to the call control, in which case, the HSSR Set will reset and await further instructions.

Sequence

4.25 The operating sequence for single address, multiple address, and broadcast calls appears on Tables 1, 2, and 3 respectively.

4.26 Note that the multi-address call sequence is similar to the single address call except that the HSSR Set polls two or more stations instead of one, during the dial response, RU1, and RU2 modes. The status and number of each station polled is printed-out at the sending set. If the station is not connected or does not acknowledge, a red lamp in the station address pushbutton is lighted, and remains lighted until the panel is reset.

4.27 Note also that a broadcast call differs from a multi-address call in that all 50 stations are selected automatically when the operator presses the BROADCAST button at the control panel. In this type of call, the dial numbers and the dial response modes are bypassed and the 50 station repertory is connected simultaneously by the external electronic switching facility.

E. Automatic Receive Calls

General

4.28 During operation as an automatic receiver, the HSSR Set call control logic performs these functions:

(a) It receives instructions from and sends instructions to the Telephone Equipment Cabinet.

(b) It receives instructions from the sending HSSR Set.

(c) It relinquishes control of the call to the set's transmission logic during reception of the message.

4.29 The instruction signals between the receiving set, sending set, and the Telephone Equipment Cabinet are control tones. The control tones originated by the HSSR Set are dc signals and are converted into tones by apparatus in the Telephone Equipment Cabinet.

Sequence

4.30 Initially, the idle receiving HSSR Set receives an off-hook-in signal from the Telephone Equipment Cabinet. This signal is followed immediately by a tone 9 (high precedence) or a tone 1 (low precedence) signal, which identify the priority of the incoming call.

4.31 The receiving set then sends an off-hook signal to the Telephone Equipment Cabinet to indicate that it has answered the incoming call. The AUTO REC lamp on the control panel is lighted.

4.32 The set then monitors the preamble data which originates at the sending HSSR Set. This data is decoded and used to program the set for the incoming message.

4.33 The last signals received during the preamble mode are dc signals representing a tone 4 (go data). The HSSR Set monitors these signals and responds with a receive data control signal to the Telephone Equipment Cabinet instructing this unit to begin the synchronization process.

4.34 At this point the tone apparatus in the Telephone Equipment Cabinet are switched in. Clock synchronization is then started between data sets.

4.35 When synchronization is completed, the HSSR Set receives the ready signal from the Telephone Equipment Cabinet. The sending HSSR Set generates framing characters (delete) which are subsequently received by the receive set and used for character framing synchronization (sending serializer with receiving deserializer).

4.36 With its deserializer in synchronization with the sending sets serializer, the receiving HSSR Set advances to the RU1 mode. The set is now under control of the transmission logic. When its RU (three-digit station number) is received and detected, the set transmits an acknowledge signal to the sending set and advances to the start of message mode.

4.37 As the set advances from one mode to the next, the corresponding REC. OPERATING SEQUENCE indicators on the control panel are lighted to show the progress of the call. At this time in the sequence, the RU1 lamp is extinguished and the ACK lamp is lighted.

4.38 When the start of message character sequence is received, the monitoring units of the set (high speed punch and printer) are unblinded to permit recording of the message.

4.39 The message data is then received and recorded. The end of message character sequence follows the message data and causes the monitoring units to be blinded. It also advances the set to the RU2 mode.

4.40 When the station RU is received and detected (a final check that this station is still connected), the acknowledge signal is transmitted to the sending set.

4.41 The set's transmission logic generates an automatic call complete signal which resets the logic and disconnects the set. The set, however, is prepared to accept (or originate) another call.

TABLE 1. AUTOMATIC CALL SEQUENCE - SINGLE ADDRESS

Step	Operating Mode Indicators	Signal to Advance Transmitter Program	HSSR Set Operational Events
1.	Set Idle	Auto-Start	On the control panel select operating modes and particular station number to be called. Press the AUTO START button.
2.	Auto-Send	Start Dial	Go off-hook indicating a request for service. Wait for start dial signal from the TEC.
3.	Start	End of Start	A pair of dc signals representing a single tone are transmitted indicating level of precedence selected: Flash Override Tone 13 Flash Tone 14 Immediate Tone 15 Priority Tone 16 A precedence tone is not sent for routine calls.
4.	Dial Numbers		Tone-out (dc signals) a three-digit sequence representing the called station number followed by a punctuation tone, eg, 1, 6, 8*.
5.	Dial Numbers	End of Dial	Tone-out dc signals representing a punctuation tone, tone 12*. Two consecutive punctuation tones to the Telephone Equipment Cabinet indicate end of dialing.
6.	Dial Response		Wait for the response on the tone-in lead indicating status of called stations: Tone 2 - out of service (OS) Tone 5 - reorder (RO) Tone 8 - connected (CO) Tone 11 - busy (BZ) Print out the station number on local printer and record status of station after each call number, eg, 168CO.

*Asterisk indicates punctuation tone.

TABLE 1. AUTOMATIC CALL SEQUENCE - SINGLE ADDRESS (Cont.)

Step	Operating Mode Indicators	Signal to Advance Transmitter Program	HSSR Set Operational Events
7.	Dial Response	Off-Hook-In	If, for some reason, the station is not connected, the station number will be printed along with status. This is also recorded on the control panel, and the HSSR Set is reset. An off-hook-in signal indicates distant station has been connected.
8.	Preamble		Tone-out a series of control signals which are converted to tones in the TEC and forwarded to the distant station so the receiver can automatically set up various operating modes such as speed, code, type of error control, and whether the remote punch should be on. A tone (go data) is sent following the control tones to indicate that the receive set should start synchronizing data sets and external customer equipment.
9.	Preamble	End of Preamble	Send a signal (send data control) to the TEC to initiate synchronization of data sets and external customer equipment.
10.	Preamble	(Receiver in Sync)	A ready signal is received from the TEC indicating synchronization of data sets has been completed and that the HSSR Set may start sending data. The send clock is unblinded along with send data lead.
11.	RU1	End of Scan	Send called station RU query in serial data form (ASCII code) and wait for acknowledgment from the receive station, eg, —LTRS, LTRS, 1, 6, 8, BLK, LTRS, LTRS—. This query is to make sure the receive set has synchronized and the proper station is on the line. When the receive set recognizes its RU, an acknowledge tone (tone 6) is received on the tone-in leads and the send set records this condition by printing out the station number followed by (AK), eg, 168AK. A no acknowledge (NA) is generated locally if the receive set

TABLE 1. AUTOMATIC CALL SEQUENCE - SINGLE ADDRESS (Cont.)

Step	Operating Mode Indicators	Signal to Advance Transmitter Program	HSSR Set Operational Events
11. (Cont.)			does not respond, printing out 168 NA. This condition is indicated by lighting of the red lamp on the control panel associated with the called station number button.
12.	Message	Start RU2	The reader is started and the message is transmitted in ASCII or Baudot code until the tape runs out (tape out). At the end of tape an end of message sequence is generated and the HSSR Set advances to the RU2 mode.
13.	RU2	End of Scan	Query the station once more to determine if the called station has received the message. After the second acknowledgment is received and recorded, the HSSR Set resets and goes on-hook (disconnect).
14.	Set in Idle Condition	Panel Reset	Press the PANEL RESET button to restore the station to the original condition.

TABLE 2. AUTOMATIC CALL SEQUENCE - MULTI-ADDRESS

Step	Operating Mode Indicators	Signal to Advance Transmitter Program	HSSR Set Operational Events
1.	Set Idle	Auto-Start	On the control panel select the operating modes and two or more station numbers to be called. Press the AUTO START button.
2.	Auto-Send	Start Dial	The HSSR Set goes off-hook indicating to the Telephone Equipment Cabinet that a call is to be placed. Wait for a start dial from Telephone Equipment Cabinet.
3.	Start		Tone-out signals indicating level of precedence of this call if a precedence level has been selected. If it is a routine call, a precedence tone is not sent.

TABLE 2. AUTOMATIC CALL SEQUENCE - MULTI-ADDRESS (Cont.)

Step	Operating Mode Indicators	Signal to Advance Transmitter Program	HSSR Set Operational Events
4.	Start	Bridge Available	Tone-out a series of digits followed by a punctuation tone (943*) indicating a request for bridge. Wait for a tone from Telephone Equipment Cabinet indicating: Bridge available - Tone 7 Bridge not available - Tone 0 If a bridge not available signal is received, the HSSR Set goes back on-hook and resets.
5.	Dial Numbers		Tone-out a three-digit sequence representing the selected station's abbreviated number followed by a punctuation tone for each station to be dialed, eg, 168*, 695*.
6.	Dial Numbers	End of Dial	Tone-out a punctuation tone 12*. Two consecutive punctuation tones indicate to the telephone control that the HSSR Set has completed dialing out the station numbers.
7.	The subsequent steps in the multiple address call conform to that of a single address call, except that the HSSR Set polls two or more stations instead of one during the dial response RU1 and RU2 modes. In each case, the station number is printed with its status. If for some reason the station is not connected or does not acknowledge, a red lamp under the related station number pushbutton on the control panel lights and remains on until the operator resets the panel.		

*Asterisk indicates punctuation tone.

TABLE 3. AUTOMATIC CALL SEQUENCE - BROADCAST

Step	Operating Mode Indicator	Signal to Advance Program	HSSR Set Operational Events
1.	Set Idle	Auto-Start	Set up control panel for various operating modes. Select the BROADCAST button. Press the AUTO START button to start automatic sequence.
2.	Auto-Send	Start Dial	The HSSR Set sends an off-hook signal to the Telephone Equipment Cabinet indicating a request for service. Wait for start dial signal.
3.	Start		Tone-out a single tone indicating level of precedence if a precedence level has been selected.

TABLE 3. AUTOMATIC CALL SEQUENCE - BROADCAST (Cont.)

Step	Operating Mode Indicator	Signal to Advance Program	HSSR Set Operational Events
4.	Start		Tone-out the three-digit sequence 996 followed by a punctuation tone indicating a broadcast call is being originated. Wait for an off-hook-in answer from Telephone Equipment Cabinet indicating the fifty stations in the semipermanent repertory are connected. A bridge not available signal at this time indicates the call cannot be placed and the HSSR Set resets.
5.	Preamble		Tone-out the preamble information and go data tone to distant stations.
6.	Preamble	Receiver in Sync	At the end of the preamble signal the TEC is given a signal on the send data control to indicate to the Telephone Equipment Cabinet to switch out the tone generator in the send channel, switch in the data set (send), and start synchronizing the data set and external customer equipment. Wait for a ready signal from the Telephone Equipment Cabinet indicating synchronization has been completed.
7.	RU1	End of Scan	Start polling the 50 stations by sending station RU's and wait for the individual station acknowledgments. Printout station call number and status.
8.	Message	Send RU2	The start of message sequence is sent followed by the originating station number. The reader is then started and the message is sent to all stations that acknowledged during the RU1 mode. When the reader senses an end of tape condition (tape out) the end of message sequence is transmitted.
9.	RU2	End of Scan	Each station which previously acknowledged is polled again as in the RU1 mode. Note: The station RU is not sent until the preceding station has acknowledged or the local no acknowledge time-out circuit has timed-out. Printout the station call number and status.

TABLE 3. AUTOMATIC CALL SEQUENCE - BROADCAST (Cont.)

Step	Operating Mode Indicator	Signal to Advance Program	HSSR Set Operational Events
10.	Idle Condition	Reset Logic	At the end of the station scan an end of scan signal generates a logic reset pulse. The HSSR Set goes on-hook (disconnects) and the logic is reset. The operator may restore the set to the original condition by pressing the PANEL RESET button or he may press the RETRY button and select only that station(s) which did not receive the message. Restore the tape in the reader. An automatic call may be originated again by pressing the AUTO START button.

5. AUTOMATIC CALL LOGIC

GENERAL

5.01 The following paragraphs describe in detail the operation of the call control logic used when the HSSR Set is originating a call. To facilitate explanation, the circuitry is grouped into logic blocks. The function of each block and its relationship to other blocks and external circuitry is covered in a general manner in Par. 5.04.

5.02 Block diagrams, timing diagrams, and charts are included, but reference should be made to the specific schematic diagrams as indicated.

5.03 Figure 12 is a block diagram which shows the logic used to originate an automatic call. The majority of this logic is located in module A; however, the control panel, the relay rack, and certain logic in module B are also used in the automatic call process.

5.04 The basic function of the blocks in Figure 12 are:

(a) Control Panel and Relay Rack: Sets up static conditions and provides a visual record of operating conditions. Includes station number buttons and indicators, operating mode controls, and alarm indicators.

(b) Auto-Start Control: Determines the type of call to be automatically originated and starts the sequence.

(c) Auto-Send Control: Controls the automatic call sequence.

(d) Address Counter Control and Selection Gates: Operates in conjunction with the character generator logic (modules E and F) to retrieve station number and control data information from the memory for use by the call control logic.

(e) Tone-Out Control and Tone-Out Converter: Converts signals to dc outputs (station numbers and control signals) compatible with tone transmitter located in Telephone Equipment Cabinet.

(f) Tone-In: Monitors dc signals received by the tone receiver in Telephone Equipment Cabinet for local control purposes. These include ESS (Electronic Switching System) responses, and answer-back signals from receiving stations.

(g) Response Printout Control and Printout Converter Status Inputs: Operates with the transmission logic (modules C, D, and H) and character generator logic to control printout of station status.

(h) Trouble Encoder and Station Number and Trouble Relays: Operates with the address counter to provide visual indication of stations which do not respond to a call.

(i) On/Off Hook Control: Controls and monitors on/off hook out and in leads to the Telephone Equipment Cabinet (TEC).

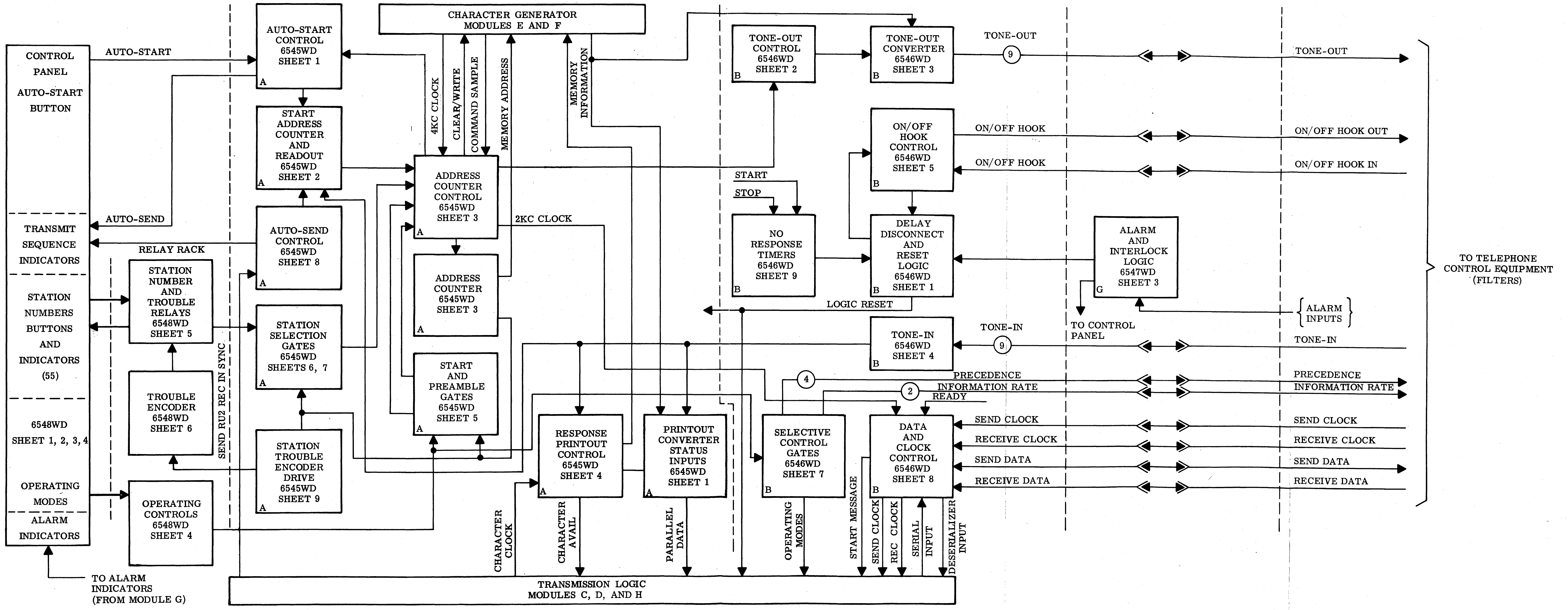


Figure 12 - Automatic Send Logic, Block Diagram

(j) Data and Clock Control: Controls send and receive data leads to the local serializer (module C) and deserializer (module D) and to the Telephone Equipment Cabinet. Controls send and receive clocks from data sets and local clock.

(k) Selective Control Gates: Gates operating control information and forwards it to the Telephone Equipment cabinet and transmission logic.

(l) Delay Disconnect and Reset Logic: Monitors conditions for resetting the HSSR Set.

(m) No Response Timers: Contains timeout circuitry to reset the HSSR Set in the event of a response failure.

(n) Alarm Logic: Monitors alarm and alert conditions and provides a visual record on the control panel.

5.05 During the message mode, the call control logic relinquishes its control of the HSSR Set to the transmission logic. In the start and dial numbers modes, the call control logic provides pertinent information to the ESS. In the preamble mode control information is generated by the call control, converted to tones in the TEC and subsequently forwarded to the receive station(s). Figure 13 is a block diagram of the logic used in this operation.

5.06 In the dial response, RU1, and RU2 modes, the call control logic supplies information necessary for printing out the status of stations as they are polled. Figure 15 is a block diagram of the logic used in this operation. During the status printout process, the memory is time-shared between the call control logic and the character generator logic. The call control requests a readout of the station numbers for printing and the character generator provides the dot information necessary for printing.

TRANSMITTER OPERATING MODE CONTROLS

A. General

5.07 The transmitter operating modes are used to program the call control logic so that pertinent information can subsequently be forwarded to the Telephone Equipment Cabinet, transmission logic, and the distant receive stations during an automatic call.

B. Levels of Precedence (6547WD, Sheet 4 and 6548WD, Sheets 1-4)

5.08 The operator may choose one of four levels of pre-emptive precedence, namely: flash override, flash, immediate, and priority. If no levels of precedence are chosen, the originating call becomes a routine transmission. The HSSR Set is normally reset to the routine condition. Pushbutton switches SP57 through 61 (6548WD, sheet 4) constitute these controls and provide the necessary signals on connector pins PP3-F6 through F10 for actuating the respective relays in the relay rack assembly (module S) which store the selected conditions. Note that the normally closed (NC) contact of each PRECEDENCE switch is in series with another. This series circuit prevents more than one precedence level relay from being selected since the series connections through the NC contact of the ROUTINE switch provides the holding path for the individual precedence relays which are schematically shown on 6548WD, sheet 4. For example, assume the FLASH button is momentarily depressed. A 48 volt signal appears on connector plug PP3-F9 and consequently on receptacle JS3-F9 of the relay rack. The 48 volt signal is applied to input 19 of relay card ZS115 and therefore relay KC is energized. This relay is latched through its NC contact, with 48 volts applied through the NC contact of the ROUTINE switch. If the ROUTINE button or another precedence level button is depressed, this holding path is opened and the flash relay drops.

5.09 When the flash relay is energized, the 48 volt holding signal is fed back to the FLASH button lamps via connector JS3-F9. These lamps, which are two 28 volt bulbs in series, are turned on indicating the FLASH priority button has been selected. The normally open (NO) contact of the flash relay (KC) provides a ground signal on connector JS4-H3 ← which programs the call control logic. This ground signal is applied to module G precedence and mode control logic via JG1-H3 (sheet 4 of 6547WD) where the signal is gated and distributed to do the following:

(a) Provides a dc precedence level (flash) signal to the Telephone Equipment Cabinet.

(b) Provides a negative signal to the start selection gate logic in module A so that during the start mode the flash condition can be toned out.

(c) Provides a signal that is used to turn off the ROUTINE indicator.

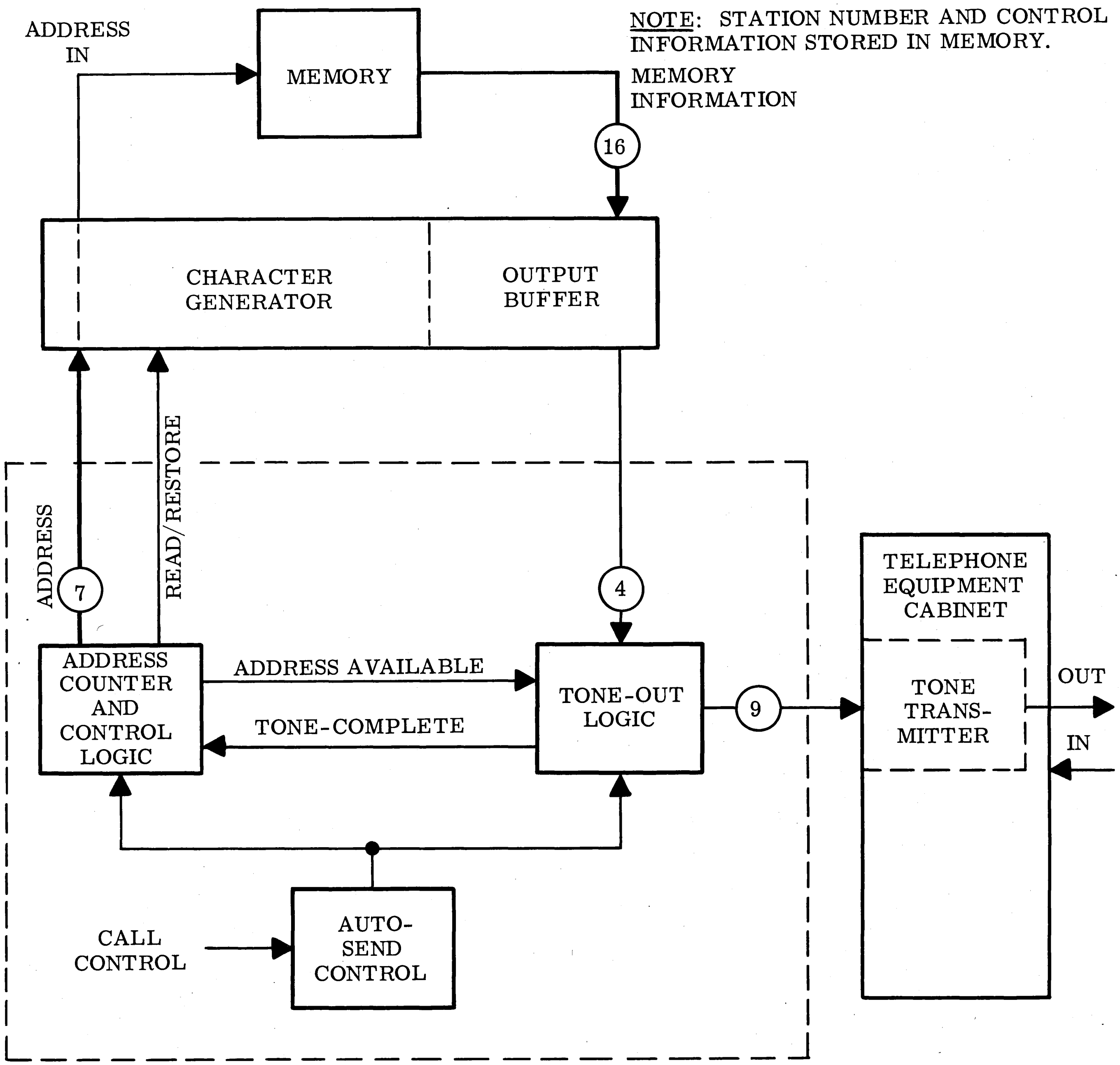


Figure 13 - Tone-Out Logic, Block Diagram

5.10 The ground signal from the relay contact that appears on JG1-H3 drives NOR gate 4A3/ZG118-A and inverter 4B3/ZG119-D. The NOR gate is used to drive a power amplifier 4A4/ZG125-A which in turn drives the ROUTINE indicator lamps. The NOR gate also drives inverter 4A3/ZG119-A which presents a negative routine signal to other logic. In this case, however, a ground signal inhibits NOR gate 4A3/ZG118-A. Therefore, a -6 volt signal is applied to power amplifier 4A4/ZG125 which turns this amplifier off extinguishing the ROUTINE indicator on the control panel. The output of inverter 4A3/ZG119-A goes to ground and this signal is applied to the tone-out control logic to permit the sending of the precedence tone during the start mode. A ground signal on input 14 of inverter 4C3/ZG119-D turns this inverter off. The resulting -6 volt output is applied to selection gate 5A3/ZA303-C via JG1-E3, blinding the gate.

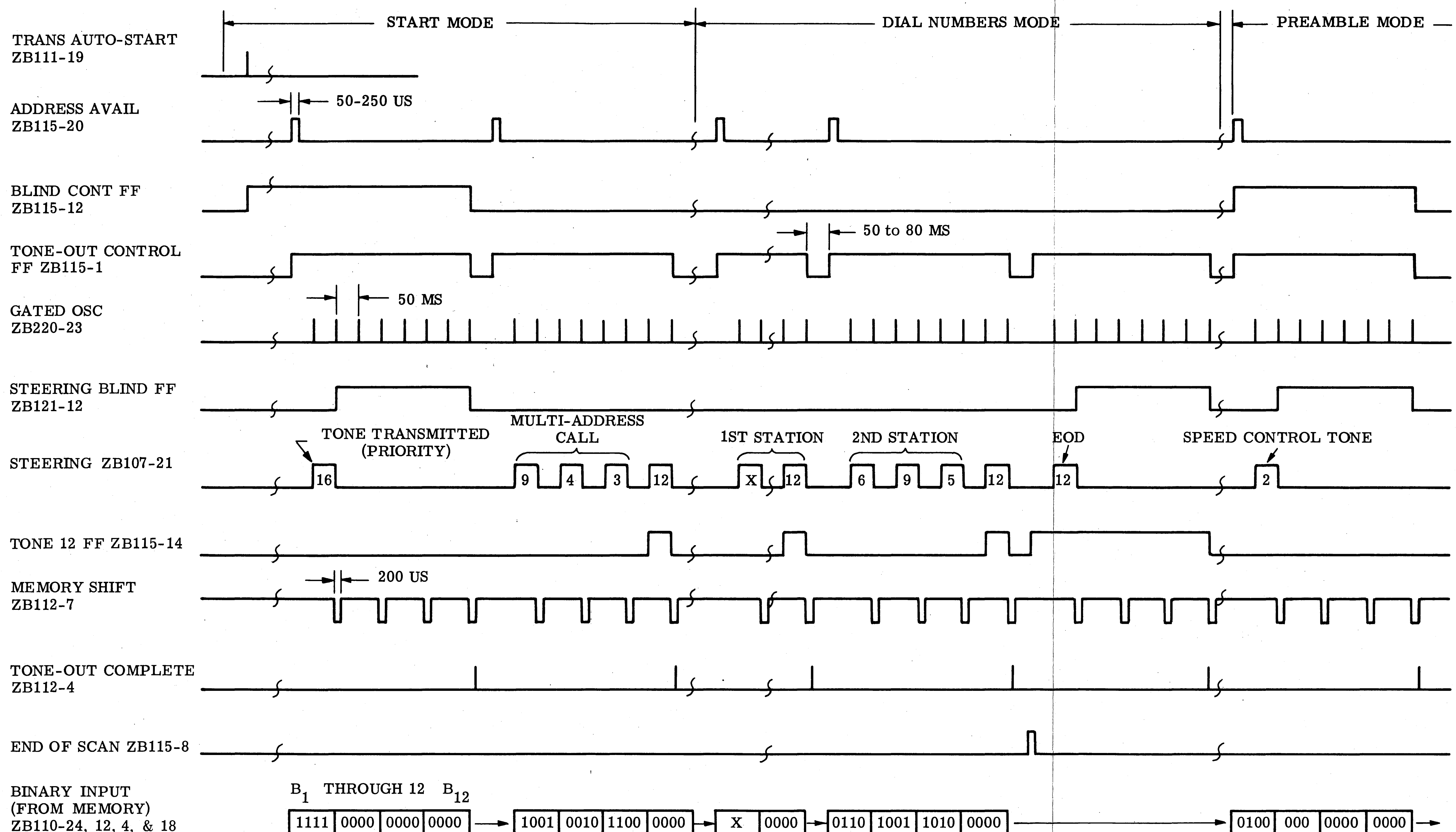


Figure 14 - Tone-Out Logic Timing (Auto-Send Condition)

NOTE: STATION NUMBERS ARE STORED IN MEMORY.

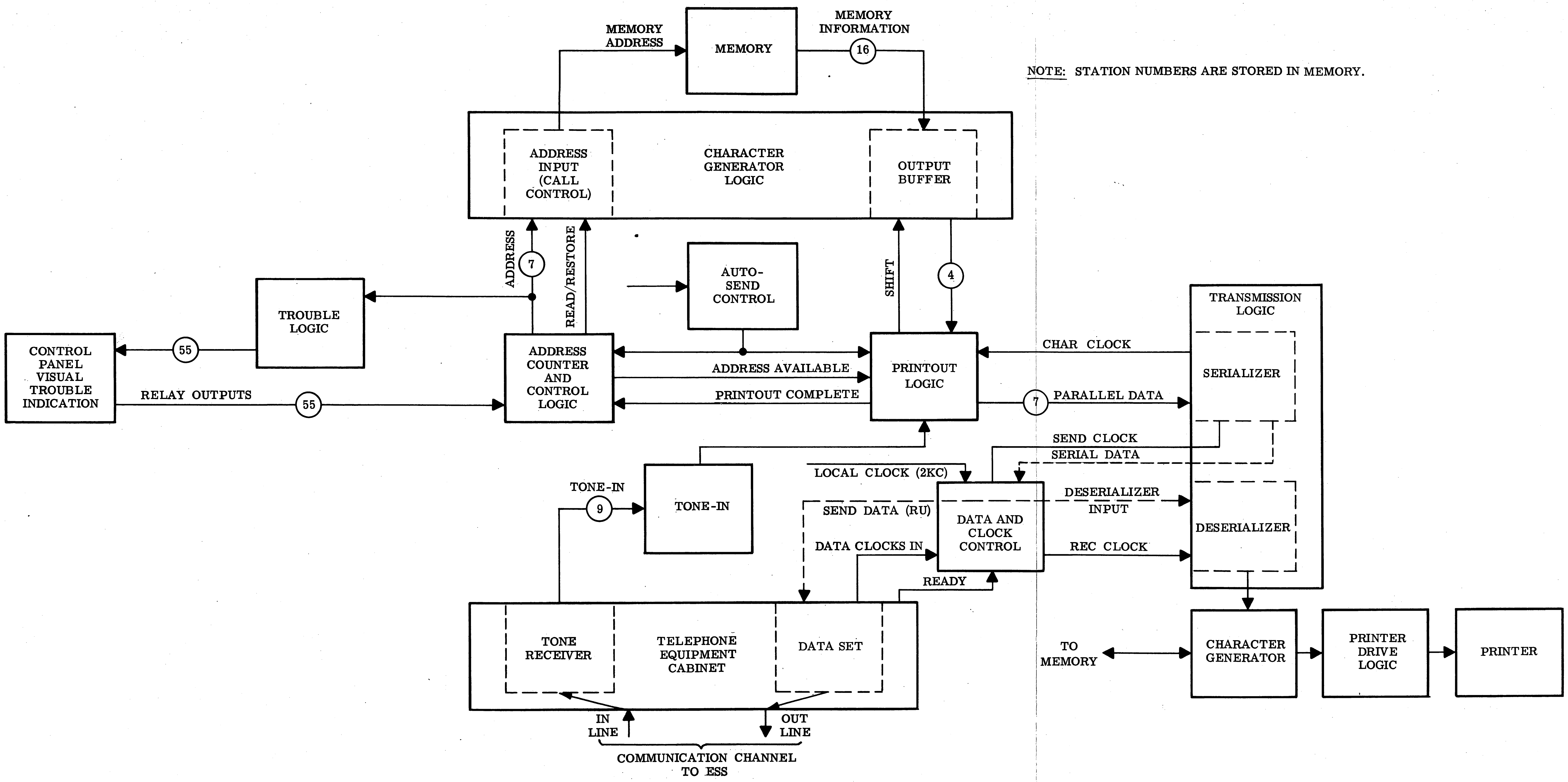


Figure 15 - Status Printout Logic, Block Diagram

During the start mode, this gate is sampled by the address counter and a start sample signal is generated. The end result is that the dc signals representing the flash condition are forwarded to the Telephone Equipment Cabinet where they are converted to tones and sent to the ESS. For a detailed circuit description refer to the respective sections concerning the address counter and tone-out logic.

5.11 Referring back to the precedence logic in module G (sheet 4 of 6547WD), the signals from the precedence relays are gated to present signals on the dc precedence leads which are subsequently forwarded to the Telephone Equipment Cabinet via the filters. These signals appear on JG2-E1 through E4 and are normally at -6 volts. A ground signal on any of these outputs indicates the respective precedence of an automatically derived call. The auto-send signal is used to unblind the NOR gates 4C5/ZG118-B through E. The signal from the precedence mode relay selected can enable the related NOR gate. In the example, the ground signal (FL) from the flash relay through inverter 4C3/ZG119-D applies a negative signal to NOR gate ZG118-D. With the auto-send lead at 0 volts, a negative signal derived from inverter 4C3/ZG119-F appears on input 35 of NOR gate 4C5/ZG118-D thereby enabling this gate and causing a ground signal to appear on the flash precedence lead.

C. Single Address and Multi-Address Indicators

5.12 The SINGLE ADDRESS or MULTI-ADDRESS indicator is lighted automatically after the operator has started the automatic sequence by pressing the AUTO START button. The send logic automatically determines the type of call being originated by the number of station buttons selected. The auto-start control logic, described in a subsequent paragraph, pertains to this function. The respective indicators remain on throughout the call until the logic is reset.

D. Broadcast Control

5.13 When the BROADCAST button is operated, a broadcast relay K12 (sheet 4, 6548WD) in the relay rack is energized thereby programming the call control for a broadcast call. A 48 volt signal from the control panel BROADCAST button is applied to this relay. The relay is energized and latches through its 1M contact. Also, the two lamps under the BROADCAST button are lighted to indicate that this particular mode was selected.

5.14 The normally closed contact, 2B, of relay K12 opens a ground path to logic in module A via pin JS4-F8 unblinding the start selection gate 5B6/ZA303-G. This generates a start sample signal when the address counter samples this gate and permits the three-digit sequence (996) representing a broadcast call to be toned-out. Also, it blinds gates in the auto-start control logic via inverter 1E4/ZA508-K. This overrides the single and multi-address conditions and unblinds NOR gate 1F6/ZA315-B to permit the off-hook signal-in to advance the auto-send control. It unblinds NOR gate 8B7/ZA316-G to permit the auto-send control sequence programmer to bypass the dial numbers and dial response modes.

5.15 Through normally closed contact 3B, the broadcast relay opens a ground path within the relay rack to the first 50 normally closed station select relay contacts which are used to select the individual station selection gates. This action automatically unblinds the first 50 station selection gates resulting in the generation of a station sample signal for each gate as they are sampled by the address counter. These 50 station gates represent those station numbers contained in the semipermanent repertory. The station select indicator lamps are not lighted in the broadcast condition. Refer to Figure 16 which depicts the normally closed broadcast contact and the circuits it controls. The broadcast relay is reset by the PANEL RESET or the RETRY circuit.

E. Speed Control

5.16 These controls are represented by pushbuttons SP62 through SP64 on sheet 4 of 6548WD and present signals on PP3-H1 to H3. The outputs from the 1200 or 600 SPEED pushbuttons apply a 48 volt signal to the appropriate speed control relay, KE or KF on circuit card 4D6/ZS115. The holding path for the individual relays is through the normally closed contact of the 2400 SPEED pushbutton. Only one speed can be selected at a time. When the PANEL RESET button is depressed, the set is reset to the 2400 speed condition.

5.17 The outputs from the NO contacts of the 1200 or 600 relays (KE or KF) apply ground signals via JS4-H5 or H6 to the selective control gate logic in module B (sheet 7 of 6546WD). In module B the signals are gated and subsequently presented to preamble selection gates (sheet 5 of 6545WD), and also to the Telephone Equipment Cabinet. The former outputs permit a preamble sample to be generated when the address counter samples the respective speed gate that is unblinded so that the proper speed control tone can be transmitted to the receive station(s). The latter output permits the Telephone Equipment Cabinet to switch and present the send and receive clocks to the HSSR Set at the specified clock rate. The ground signals from the speed control relays are also applied to control logic in module G which overrides the 2400 speed condition. This logic is shown on sheet 4 of 6547WD.

5.18 Assume the 1200 speed control relay KE is selected. A ground signal is applied to JG1-H5 and NOR gate 4F2/ZG118-F is blinded. The output of this NOR gate goes to -6 volts turning off the power amplifier 4F3/ZG121 which is used to drive two lamps under the 2400 SPEED pushbutton. These lamps are extinguished. Also, the output of the NOR gate drives inverter 4F3/ZG119-K turning this inverter on, and its output goes to ground which blinds the 2400 speed gate 5F2/ZA304-A (in the preamble selection gate logic, sheet 5 of 6545WD).

5.19 At the same time, the 1200 speed preamble selection gate (module A) 5F2/ZA304-B is unblinded from a signal derived from the selective control gate logic in module B (sheet 7 of 6546WD). The ground signal from the NO contact of the 1200 speed relay appears on JB1-H1. This signal is applied to inverter 7A2/ZB315-A and also NOR gate 7B4/ZB311-B. The inverter goes to -6 volts, applying this signal to NOR gate 7B2/ZB311-A and pin JB1-G3. The negative signal on pin JB1-G3 is applied to the preamble selection gate logic.

5.20 In the selective control gate logic, the speed control leads to the Telephone Equipment Cabinet via filters which are subsequently programmed. The switching, in this case, takes place when the HSSR Set goes off-hook and is in the auto-send condition. In the same logic, the input lead defined as receive auto off-hook is used to control a bank of NOR gates 7C4/ZA311-A to F which are used to gate the various operating modes set up on the control panel. This input remains at -6 volts and only switches to ground when the set goes to the automatic receive condition at which time the ground signal blinds the NOR gates 7C4/ZA311-A to F, overriding the various signals from the operating mode relays (control panel modes) and allowing the signals from the receiver control logic to program the set and speed control leads. The receiver control logic is described in Part 6.

5.21 In the auto-send condition, the auto receive off-hook signal is -6 volts and the negative signal from inverter 7B2/ZB315-A (1200 speed) enables NOR gate 7B4/ZB311-A while the ground signal from the 1200 relay contact blinds NOR gate 7B4/ZB311-B. The ground signal from NOR gate 7B4/ZB311-A is applied to two output NOR gates 7B8/ZB313-A and B. Therefore, outputs on connector pins JB1, A8 and A9 are both at -6 volts. These signals are applied to the Telephone Equipment Cabinet as a request to switch to the 1200 bit/sec send and receive clocks. Note that NOR gates 7B8/ZB313-A and B are unblinded as soon as the positive auto off-hook or manual off-hook signals are received on inputs to gate 7A5/ZB313-C. Also, note that the negative receiver auto off-hook signal is used to blind a set of speed control NOR gates via inverter 7F4/ZB314-K located at the bottom of the sheet so that the outputs of these gates are all at -6 volts when the set is not in the auto-receive condition.

5.22 Assume that the 2400 speed condition (reset condition) exists. No relays are associated with the 2400 speed and the absence of the 1200 and 600 speed ground signal from these respective speed control relays indicates the 2400 wpm condition. In this case, inverters 7B2/ZB315-A and B outputs are 0 volt blinding NOR gates 7B4/ZB311-A and C. The 2400 NOR gate 7B4/ZB311-B is enabled and a 0 volt signal is presented to 7B8/ZB313-A. The output on JB-A9 goes to -6 volts; however, 7B8/ZB313-B is enabled and a 0 volt signal appears on JB1-A8 requesting the 2400 bit/sec clock. Following is a truth table for the speed control outputs to the Telephone Equipment Cabinets requesting the various speeds.

Speed Bits/Sec	Speed Control Outputs JB1-A8	JB1-A9
2400	0 v	-6 v
1200	-6 v	-6 v
600	-6 v	0 v

5.23 As stated previously, the outputs from the speed control relay contacts drive logic in module G. Refer to sheet 4 of 6547WD. With 2400 speed selected, NOR gate 4F3/ZG118-F is enabled since both inputs to the gate are negative. Consequently, output of the power amplifier 4F3/ZG121 is 0 volt turning on the 2400 SPEED indicator lamps on the control panel. The output of inverter 4F3/ZG119-K goes negative and this signal is applied to the preamble selection gate logic via JG1-E10 to NOR gate 5F2/ZA304-A which prepared this gate for sampling by the address counter in the preamble mode.

F. Code, Error Control, and Remote Punch On/Off Controls

5.24 These operating mode controls are combined and discussed together in the following paragraphs since their associated logic is similar. Control signals are forwarded to the transmission logic to program this logic for operation in the message mode. As stated previously, the operator can select one of two types of transmission codes, ASCII (8-level) or Baudot (5-level); one of two types of error control, detection (ED) or detection and correction (EDC); and remote punch ON or OFF. The HSSR Set resets to the ASCII, ED and REMOTE PUNCH OFF modes. These controls are lighted pushbuttons shown schematically on sheet 4 of 6548WD as switches SP66 through SP70. Under normal reset conditions, the indicator lamps are driven by power amplifiers located in module C (sheet 8 of 6528WD).

5.25 For each of the following operating modes - Baudot, EDC and REMOTE PUNCH ON - there is a relay which can be selected. These relays are also shown on sheet 4 of 6548WD and represent relays KG and KH on card 4F6/ZS115 and relay KA of circuit card 4F6/ZS116 in the relay rack. They are energized by their respective pushbuttons and latched in the same manner as the speed control relays previously described. The corresponding contact outputs appear on JS4-H7, H8 and H9 and provide signals to the operating mode indicator circuits located in module C in order to extinguish the alternate mode indicators. The contact outputs, with the exception of the REMOTE PUNCH ON, are also applied to the selective control gate logic via pins JB1-H3 and H4 in similar fashion as the control speed leads. See sheet 7 of 6546WD. Here the mode signals are gated in order to provide operating mode signals to the transmission logic so that the logic can be programmed. The operating mode signals to the transmission logic are -6 volts for the ASCII, ED, and LOCAL PUNCH ON conditions and ground for the Baudot, EDC, and LOCAL PUNCH OFF modes.

5.26 Assume the EDC operating mode is selected. A ground signal appears on JB1-H4 and inverter 7D2/ZB315-D is turned off. A negative signal from the inverter enables NOR gate 7D4/ZB311-E since input 9 is also negative. The ground signal from this NOR gate is applied to NOR gate 7D6/ZB312-B which blinds this gate (-6 volts on output) and consequently a positive signal from inverter 7D8/ZB315-H is presented to the transmission logic to indicate the EDC mode has been selected. This signal is also presented to the alarm logic in module G, inverter 3E7/ZG115-J, to monitor certain alarm conditions.

5.27 In the selective control logic, the Baudot and the local punch on signals follow similar paths. The local punch on/off is a local control and only the punch off condition is overridden by a punch on signal from the receiver control logic through NOR gate 7E6/ZB312-C. In this logic, for all conditions except the auto-receive condition, the operating modes as set up on the control panel are reflected to the transmission logic.

5.28 The signals from the Baudot, EDC and remote punch on relays are also applied to the preamble selection gate logic (sheet 5 of 6545WD) to blind the ASCII, ED and remote punch off selection gates and unblind the Baudot, EDC and remote punch on gates so that during the preamble mode the control information representing these selected modes can be transmitted to the receive station(s).

5.29 Referring to operating mode relay circuitry (sheet 4 of 6548WD), note that the EDC mode relay KA is interlocked with module H and cannot be selected unless this module (EDC) is connected to the HSSR Set. Without module H the signal from the EDC pushbutton is disabled (JH1-E10 and JH2-E10 are open).

G. Station Number Buttons and Station Select and Trouble Relays

5.30 There are 55 STATION NUMBERS buttons on the control panel. Each of the first 50 buttons contain a three-digit number which represents a call number of a distant station. The last five STATION NUMBERS buttons are SPARES and are not related to specific numbers unless the operator has programmed in such numbers. The three-digit station numbers are stored in the set's random access memory in binary form and utilized when originating an automatic call. The HSSR Set is capable of dialing all 55 stations if all the buttons have been selected. The five SPARES permit a call to be made to stations not appearing on the regular dialing repertory and are readily changeable by programming in new numbers from the program switch.

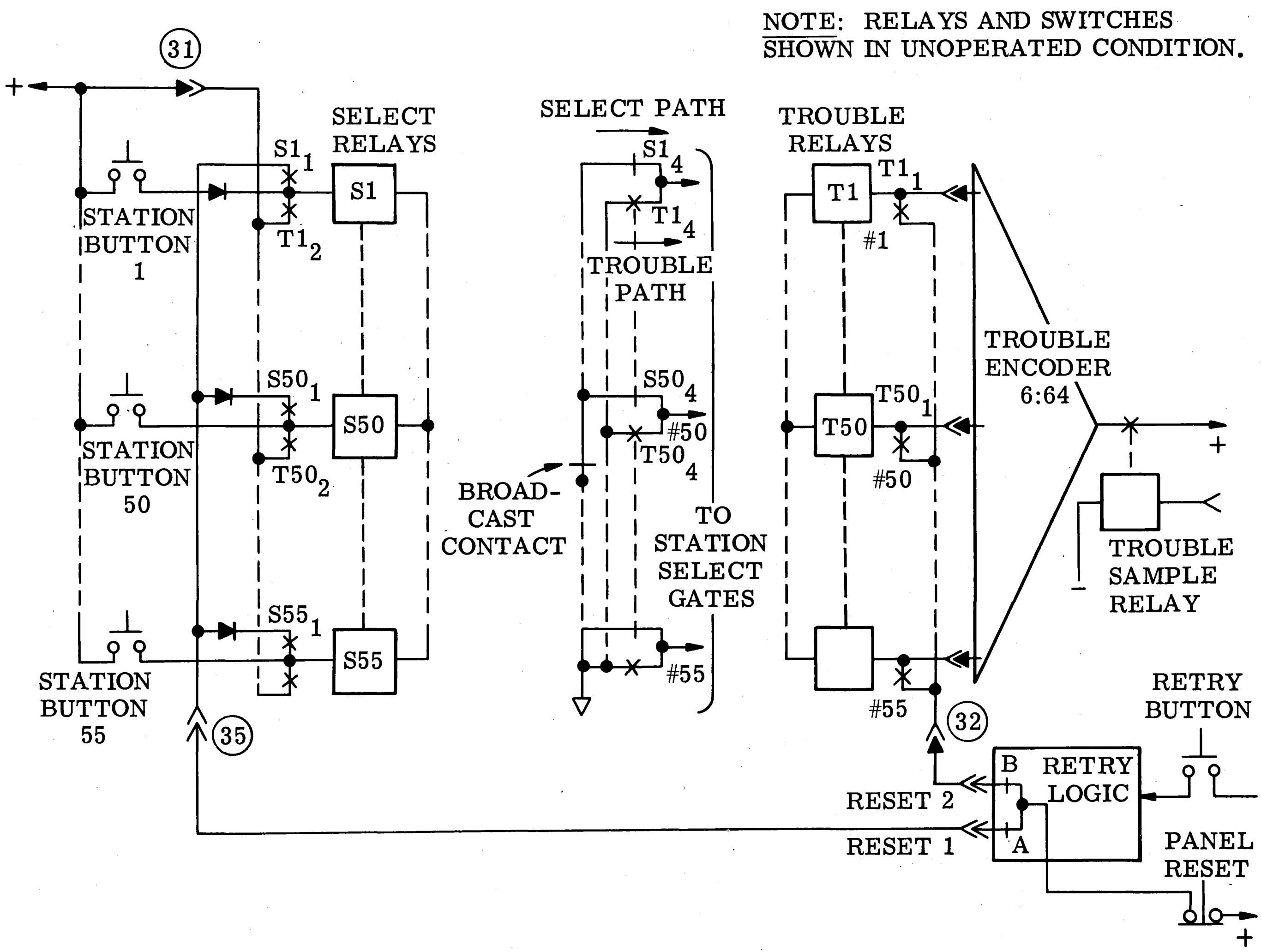


Figure 16 - Retry Logic, Block Diagram

5.31 Each STATION NUMBERS button has an associated station select (S) relay and a station trouble (T) relay which are located on circuit cards mounted in the relay rack (module S) directly behind the control panel assembly. The STATION NUMBERS buttons and relay logic are shown on sheets 3 and 5 of 6548WD. The majority of interconnection between the respective relays is done on circuit card EC634. Since this logic represents 55 parallel circuits a composite block diagram of the station select and trouble logic is illustrated in Figure 16.

5.32 When a STATION NUMBERS button is depressed, a corresponding station select relay is energized and latched and remains in this condition until the operator presses the PANEL RESET or RETRY button. An energized station select relay does the following:

(a) It completes a circuit path to the related STATION NUMBERS button lamps (white) thus presenting a visual indication that the station number has been selected.

(b) It opens a circuit path to a corresponding station selection gate in the call control logic. This gate is sampled by an address counter and represents the address in the memory where the digital information representing the station number is stored.

(1) For example, assume STATION NUMBERS button 1 is associated with memory address 1 where call number 168 is stored in binary form as illustrated below:

Memory Bits	1 2 3 4	5 6 7 8	9 10 11 12	13 14 15 16
Binary Data	1 0 0 0	0 1 1 0	0 0 0 1	0 1 1 1 ←
Decimal	1	6	8	Not Used

(2) STATION NUMBERS button 2 represents address 2 where station number ZYZ is stored, and so on up to button 55. Since the memory is controlled by the character generator logic (modules E and F), the address, along with a read/restore command is presented to the character generator logic so that the information can be read out of the memory and subsequently utilized by the call control logic for dialing out the station numbers and printing the respective station status.

(c) If a station is not connected or does not respond to its RU, the corresponding station trouble relay is energized by a sample signal from the trouble encoder. This logic is described in detail in Par. 5.87. See 6545WD, sheet 9. The station trouble relay performs the following functions:

(1) It closes a circuit path to the related station select gate, blinding the gate and preventing this address from being generated throughout the remainder of the call.

(2) It completes a circuit path to the station select relay which prevents this relay from being reset when the RETRY button on the control panel is depressed. Therefore, the particular station in trouble remains in the select condition. This eliminates the necessity of the operator having to reselect each station which did not respond prior to originating another call.

(3) It opens the circuit to the station select lamps, extinguishing these lamps, and simultaneously completing a circuit path to a pair of lamps (red) under the STATION NUMBERS button to provide a visual indication of the station not responding.

(d) The station trouble relay remains energized throughout the call until the operator presses the RETRY or PANEL RESET button.

H. Retry Logic (Figures 16 and 17)

5.33 As mentioned in the preceding description, the retry logic permits the operator to reselect all the stations that were in trouble on the previous call and to reset those that receive the message so the call can be placed again. The logic consists essentially of relays arranged to permit sequential resetting of the station select and trouble relays. These reset busses are defined as reset 1 and 2. The logic is activated by pressing the RETRY button. Referring to Figure 19, inputs 35 and 32 on relay circuit cards ZS101 to ZS114 (EC634) are resets 1 and 2 respectively.

5.34 In Figure 16, assume station no. 1 and station no. 50 are selected and station no. 1 did not respond. Originally, the station relays are latched through their respective contacts, $S1_1$. A voltage is applied through a normally closed relay contact in the retry logic arbitrarily defined as A. The trouble relay, T1, is energized by a sample pulse from the trouble sample relay's normally open contact and directed by the trouble encoder logic to trouble relay T1. The relay is latched through its contact $T1_1$. A voltage is applied to this set of contacts from a normally closed relay contact arbitrarily defined as B in the retry logic (reset 2 buss). With T1 energized, contact $T1_2$ is closed which completes a path via card pin 31 to a positive voltage. When the RETRY button is momentarily depressed, the A contact is opened. The voltage applied to contacts $S1_1$, $S50_1$ .... $S55_1$ is interrupted and relay S50 de-energizes; however, relay S1 remains energized since $T1_2$ is closed. When the RETRY button is released, contact A closes and after an interval of time, contact B opens (reset 2) which interrupts the latching path of trouble relay T1. Relay T1 is restored to its normal condition and another call can be made to station 1.

5.35 The relays comprising the retry logic are shown on sheet 1 of schematic 6548WD and consist of wire-spring type relays K10, K11 and KF. The latter relay is located on circuit card 1D5/ZS116. Refer to Figure 17 which is a timing diagram of this logic. When the RETRY button is depressed, a 48 volt signal appears on connector pin JS2-H1 which energizes relay K10. The normally closed contacts forming the reset 1 buss are opened and the station relays are reset. Simultaneously, K10-1M closes energizing relay KF. When relay KF is energized the normally open contact to K11 is closed, however, K10-1B is open at this time. When the RETRY button is released, K10 de-energizes, its 1B contact closes energizing relay K11 and an interval of time later depending upon the relay pick-up time K11-8B is opened,

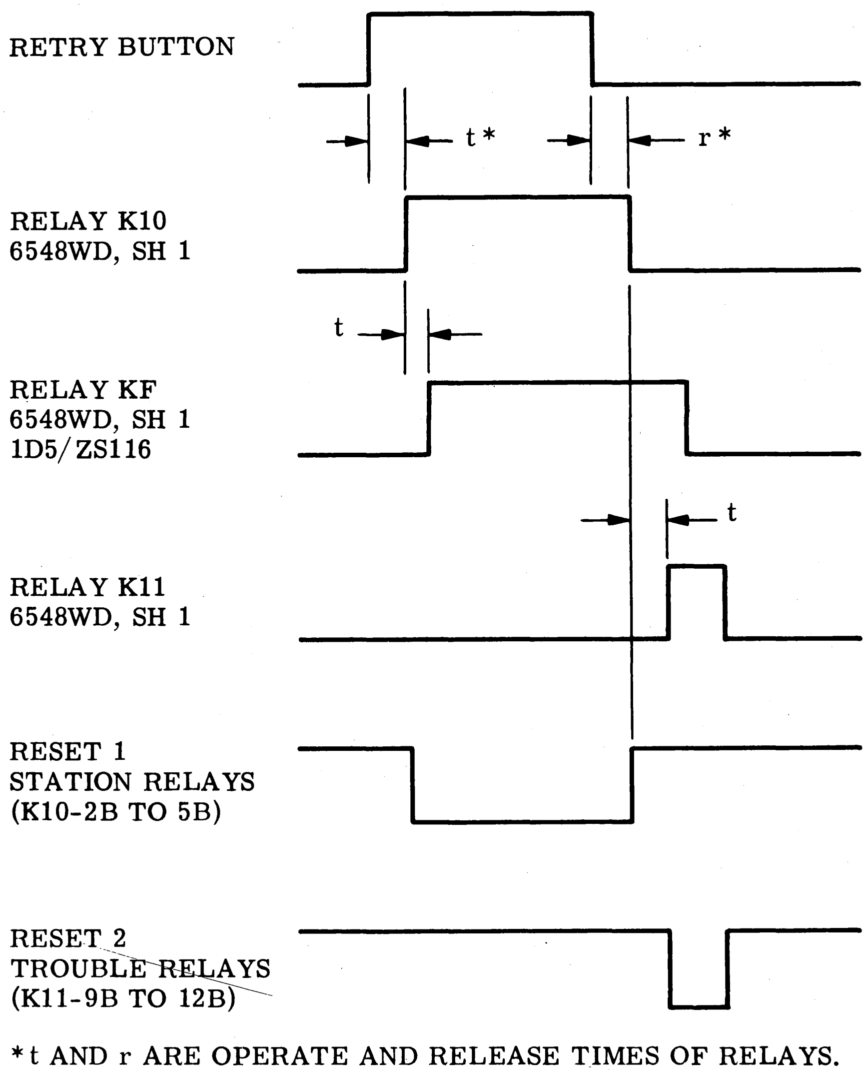


Figure 17 - Retry Logic Timing

therefore dropping relay KF. Simultaneously, normally closed relay contacts associated with K11 are opened breaking the reset 2 buss. The current on this buss is interrupted and all the energized trouble relays drop. Relay KF in turn opens the current path to relay K11 via pins 13 and 14 of circuit card 1D5/ZS116 and relay K11 is de-energized restoring the circuit to its original condition. Several NC contacts of relays K10 and K11 are used to open reset busses 1 and 2 respectively in order to minimize the breaking load on each contact.

AUTO-START CONTROL

A. General (Figures 12 and 18)

5.36 The auto-start control logic consists of a binary stage and various gates which control the start of an automatic call.

5.37 The logic is triggered when the AUTO START button on the control panel is pressed. A preliminary scan is then initiated by the auto-start control logic to determine whether the call is a single address, or a multi-address call. The auto-start control logic operates in conjunction with the address counter and address counter control circuits. The address counter presents signals to the auto-start control logic each time it detects a selected station number button during the preliminary scan. If only one button is selected the call is a single address call. Two or more signals indicate a multi-address call. When a broadcast call is originated, the single and multi-address conditions are overridden.

5.38 At the completion of the preliminary scan (end of scan), the auto-start control generates a transmitter auto-start signal which initiates the auto-start sequence.

B. Auto-Start Control Detailed Description (Figure 18 and 6545WD, Sheet 1)

5.39 Pressing the AUTO START button on the control panel breaks the ground path to pin 9 of NOR gate 1B4/ZA318-E. With the auto-start blind (pin 8) at -6 volts and flip-flop 1B6/ZA323-A in the set 0 state (pin 12 at -6 volts) the NOR gate output will shift from -6 to 0 volt. This positive signal is presented to delays ZA324-A and B connected in tandem. The first delay filters and reshapes the signal from the auto start signal delaying it 800 microseconds. The -6 to 0 volt delayed signal is presented to NOR gate 1B5/ZA518-B. The NOR gate, along with inverter 1C8/ZA520-K are connected to perform an OR function. When the NOR gate is inhibited, the output goes to -6 volts. This signal is presented to inverter 1C8/ZA520-34 resulting in a positive start reset output. The signal appears on connector JA2-F2 and is subsequently presented to the delay disconnect logic in module B (sheet 1 of 6546WD, OR gate 1F7/ZB511-C) and a logic reset pulse is generated by power pulser 1F8/ZB527-B resetting all the digital logic.

5.40 The output of the 800-microsecond signal delay 1B4/ZA324-A also drives the 400-microsecond delay 1B5/ZA324-B. After a logic reset, a positive signal is presented to the set 1B input of flip-flop 1B6/ZA323-A. The normal (N) output of the flip-flop goes to ground, and this signal is applied to NOR gate 1B4/ZA318-E which blinds this gate to any input from the AUTO START button. The input of this NOR gate is blinded to prevent resetting the logic if the operator should accidentally press the AUTO START button.

5.41 The normal output of flip-flop 1B6/ZA323-A also primes flip-flop 1B6/ZA323-B on the P1B input and provides a preliminary scan signal to the start address control logic OR gate 2C5/ZA327-A (sheet 2 of 6545WD).

5.42 The address counter is started and the preliminary scan begun. The counter, driven by a 2kc clock scans the entire complement of selection gates in approximately 32 milliseconds. When the counter samples a selected gate a 250-microsecond positive pulse appears on the station count lead. This positive pulse is coupled through inhibit gate 1C4/ZA320-C, driving flip-flop 1C5/ZA322-A to the set 1 state. The next positive transition on the output of this gate will shift the flip-flop to the set 0 state.

5.43 Assume that a single address call has been initiated. During the preliminary scan, one positive pulse will be returned on the station count lead. Flip-flop 1C5/ZA322-A will be driven to the set 1 state providing a -6 volts (inverted output) to NOR gate 1D5/ZA318-A. Pin 13 of the NOR gate is also at -6 volts, since the broadcast condition had not been selected. Pin 15 of the NOR gate, however, is at ground potential and the NOR gate output remains at -6 volts.

5.44 The next signal received by the auto-start control logic is an end of scan signal, a positive pulse occurring when the address

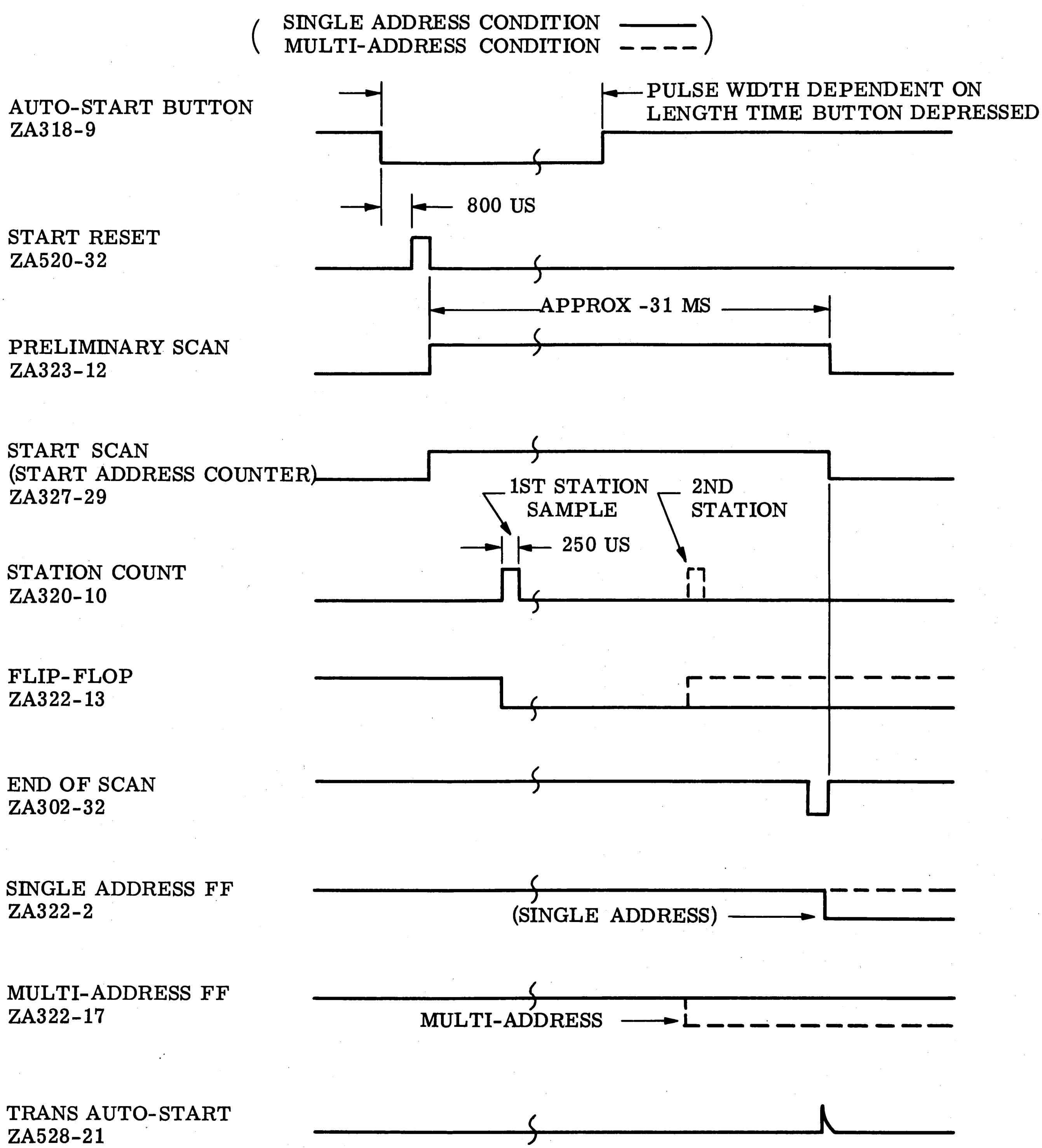


Figure 18 - Auto-Start Control Timing

counter reaches count 62. The end of scan signal does the following:

(a) It resets the preliminary scan flip-flop 1B6/ZA323-A. Flip-flop 1B6/ZA323-B ← which in turn generates a transmitter auto-start pulse is set to the 1 state through power pulser 1C7/ZA528-B. Note that the P1B signal is removed from the auto-start flip-flop at the same time the set 1 pulse is applied.

(b) It sets flip-flop 1C6/ZA322-C to the 1 condition via its 1B input. The prime 1B of this flip-flop is at 0 volts at this time since it is primed by the inverted output of flip-flop 1C6/ZA322-B.

5.45 When flip-flop 1C6/ZA322-C is set to the 1 condition by the end of scan pulse, NOR gate 1D5/ZA318-A is enabled. The NOR gate output shifts to 0 volt to provide the following functions:

(a) It drives power amplifier 1D6/ZA125-A ← turning on the SINGLE ADDRESS lamp on the control panel.

(b) It applies a ground signal to NOR gate 1D7/ZA318-D blinding this gate to prevent a start reset pulse from being generated if the EDC (error detection and correction) mode had been selected.

(c) It drives inverter 1D6/ZA320-A. The three NOR gates, 1E6/ZA315-C, D, and B form an OR gate driving inverter 1F7/ZA319-J. If any one of the NOR gates are enabled, the inverter output goes to -6 volts.

5.46 As previously described (Par. 5.39), the auto-start pulse triggers the control logic taking the HSSR Set off-hook to the Telephone Equipment Cabinet requesting service. This is accomplished by applying the transmit auto-start pulse to the auto-start flip-flop 5D7/ZB517-B in the on/off hook control logic (sheet 5 of 6546WD). The start information is subsequently toned-out to the Telephone Equipment Cabinet after which an end of start is received as the address counter samples the start selection NOR gate 5B6/ZA303-A (sheet 5 of 6545WD). The end of scan signal is a negative pulse from inverter 5C7/ZA302-A in the start selection gate logic which enables NOR gate 1E6/ZA315-C in the auto-start control. The inverter 1F7/ZA319-J presents the negative dial numbers signal to the auto-send control logic NOR gate 8F3/ZA315-E which enables this gate and advances the auto-send control to the dial numbers position.

5.47 In the following description assume that a multi-address call is being originated:

(a) During the origination of a multi-address call, two or more station count pulses are received and consequently flip-flop 1C5/ZA322-A is switched to the set 1 condition by the first pulse and set 0 condition by the second pulse. When the flip-flop goes back to the 0 state, the multi-address flip-flop 1C6/ZA322-B is set to the set 1 state by the positive transition on the set 1B input. The multi-address flip-flop in turn removes the prime from the P1B input of flip-flop 1C6/ZA322-C. Thus, receipt of an end of scan signal will not set this flip-flop to the set 1 condition and the single address NOR gate 1D5/ZA318-A is blinded.

(b) The multi-address flip-flop when triggered enables NOR gate 1E5/ZA318-B. Its output goes to ground and does the following:

(1) It drives power amplifier 1E6/ZA125-B, which in turn provides a -28 to 0 volt signal to turn on the MULTI-ADDRESS indicator on the control panel.

(2) It drives inverter 1E6/ZA320-B which, in turn, unblinds NOR gate 1F6/ZA315-D and the start selection gate 5C5/ZA303-F. The latter NOR gate is sampled by the address counter when the set is in the start mode to signal the ESS for a dialing bridge.

(3) It also unblinds gates in the no response timer logic (sheet 9 of 6546WD).

(c) After the request for bridge (3-digit sequence 943) is toned-out, the next signal received by the auto-send control logic is the bridge available signal from the ESS via the TEC on JA2-F2. This is a 0 to -6 volt signal from the tone-in logic (sheet 4 of 6546WD). This signal enables NOR gate 1F6/ZA315-D and ground appears on its output which drives inverter 1F7/ZA319-J. Consequently, a dial number signal is presented to the auto-send control logic that advances the programmer to the dial numbers condition.

5.48 The following description of the auto-start control considers the condition for a broadcast call. The events which occur are similar to those occurring when a multi-address call is originated; however, in this case NOR gates 1E5/ZA318-A and B are blinded. This is accomplished when the BROADCAST button is depressed, thereby selecting the broadcast relay located in the relay rack. The normally closed contact of the broadcast relay is opened and permits the input to inverter 1E4/ZA508-K to go to -6 volts; consequently, the output of this inverter goes to ground and this signal is applied to pins 13 and 5 of NOR gate 1E5/ZA318-A and B, respectively. The output from the broadcast contact also unblinds NOR gate 1F6/ZA315-B and NOR gate 5B6/ZA303-G in the selection gate logic (6545WD, sheet 3). The latter gate is utilized during the start mode to signal the ESS that a broadcast call is being originated. The control signals consist of a 3-digit sequence 996 which is dialed-out in dc form by the tone-out logic.

5.49 After the start information has been transmitted, the next signal received by the auto-start control is an inverted off-hook from the on/off hook control logic (sheet 5 of 6546WD) which enables NOR gate 1F6/ZA315-B and thereby generating a negative dial number signal. This signal is presented to the auto-send control logic to advance the program counter to the preamble mode. Refer to the description of the auto-send control logic (Par. 5.104).

START ADDRESS COUNTER AND READOUT (6545WD, Sheet 2)

A. General (Figure 12)

5.50 This logic, contained in module A, has two distinct control functions: to start the address counter and to facilitate printing out the station numbers when loading or performing certain off-line tests. The logic also contains some circuitry which generates a reset pulse under certain conditions.

Start Address Counter Control Logic

5.51 This logic accepts inputs from various sources within the call control logic and gates them directly or indirectly in order to provide a start scan signal to the address counter control for the purpose of starting the address counter. The indirect gating is done through a delay start scan circuit to provide the proper timing.

Readout Control Logic

5.52 This logic provides a means of printing out the three-digit station numbers when these numbers are loaded in the memory from the STATION PROGRAMMER switch on the control panel.

5.53 Under certain test conditions it provides a means whereby any or all station numbers (55 maximum) stored in the memory can be read-out and subsequently printed on the local page copy by the printer.

Reset Logic

5.54 This logic (6545WD, sheet 2) is used to generate two signals, reset A and no stations connected, which in turn generate a logic reset pulse for resetting the HSSR Set when the set is in the automatic send condition. The reset is generated so that the set will go on-hook immediately and not go through the remaining call sequences if the following conditions exist:

(a) If an attempt is made to originate a multi-address or broadcast call and the EDC mode has been selected.

(b) If no station(s) is connected.

(c) If no connected stations acknowledge during the RU1 and RU2 querying.

(d) If an auto call complete signal is received from the call control auto-send control logic.

B. Start Address Counter Control Detailed Description (6545WD, Sheet 2)

5.55 When the HSSR Set is used to originate an automatic call, the address counter is used during the following modes:

(a) Preliminary Scan

(b) Start

(c) Dial Numbers

(d) Preamble Mode

(e) RU1 Mode

(f) RU2 Mode

5.56 In the above modes a positive start scan signal derived from OR gate 2C5/ZA327-A is presented to the start scan flip-flop, 3C4/ZA109-C in the address counter control logic (6545WD, sheet 3). A positive transition applied to the set 1B input of this flip-flop sets it to the 1 condition. The OR gate 2C5/ZA327-A gates the various signals in order to provide the positive start scan signal to the address counter control logic.

(a) At the beginning of the preliminary scan phase, a positive signal derived from flip-flop 1B6/ZA323-A is applied to OR gate 2C5/ZA327-A, pin 35. The result is a positive (-6 to 0 volts) start scan signal which remains in this condition for approximately 31 milliseconds until the end of scan signal from the station selection gate resets the flip-flop 1B6/ZA323-A. The start scan flip-flop 3B4/ZA109-C in the address counter control logic is triggered by the positive transition from flip-flop 1B6/ZA323-A.

(b) When the auto-send control (sheet 8 of 6545WD) advances to the start mode a 100-microsecond positive pulse (program step pulse) is generated by signal delay 8B3/ZA325-A. This pulse, is applied to the set 1B input of flip-flop 2C3/ZA525-A, triggering this flip-flop to the set 1 condition. At this time, the P1B input is at 0 volts priming the flip-flop. This is accomplished through inverter 2C2/ZA520-B which is driven by a signal defined as RU1. The RU1 signal is derived from the auto-send control logic, NOR gate 8C5/ZA317-E. (Refer to 6545WD, sheet 8.) Since the auto-send control is not in the RU1 mode, the output of the NOR gate is -6 volts at this time. This signal is inverted to prime the flip-flop 2C3/ZA525-A.

(c) When the flip-flop 2C3/ZA525-A is triggered, a 0 volt signal is applied to the gated oscillator 2C4/ZA624. The gated oscillator starts timing-out to its adjusted value, and approximately 300 milliseconds later a positive pulse of 10 to 20 microseconds in duration is generated. This pulse is applied to the OR gate 2C5/ZA327-A and a start scan signal is generated in order to start the address counter so that pertinent start information can be toned-out to the Telephone Equipment Cabinet. After each bit of control information has been toned-out, which takes about 400 milliseconds, a tone complete signal is received from the tone control logic in module B (6546WD, sheet 2). This signal is a positive pulse, 10 to 20 microseconds in duration, derived from power pulser 2B8/ZB112-A in the tone-out control logic and applied to the start address counter logic via pin JA2-F10. Thus, a positive start scan pulse is again applied to the address counter control to advance the counter to the next address containing pertinent information to be toned-out. The cycle is repeated until all the start information has been transmitted.

(d) When the auto-send control advances to the dial numbers mode a program step pulse is generated again and the delay start scan circuit is triggered (flip-flop 2C3/ZA525-A). The operation is similar to that previously described for the start mode except in this case, station call numbers are toned-out to the ESS. At the end of scan (all selected stations dialed) the tone complete signal is inhibited which prevents the address counter from starting. Instead, the end of scan signal advances the auto-send control logic to the dial response mode. The positive dial response signal from the auto-send control is applied to signal delay 2F6/ZA124-B. Approximately 400 milliseconds later a positive start scan pulse from power pulser 2D6/ZA328-A is applied to the address counter control circuitry. The address counter is allowed to step to the first selected station address. The logic is prepared to print out the first station status as soon as the response is received from the ESS. Note that the P1B input to the delay start scan flip-flop is -6 volts when the set is in the dial number mode thereby preventing the program step pulse from triggering the delay start scan flip-flop when the set advances to the dial response mode.

(e) When the set is in the dial response mode, the punctuation tone, represented by tone 12, is utilized to generate a start scan signal. The tone 12 signal is generated by the ESS between each answer-back response tone and is presented to the tone-in logic in module B (sheet 4 of 6546WD). In this logic, the signal is converted to a positive pulse, 800 microseconds in duration, which appears as an output on NOR gate 4F7/ZB304-D. The positive pulse is applied to OR gate 2C5/ZA327-A via connector pin JA2-F9 generating a positive start scan signal 800 microseconds in duration. The address counter is advanced to the next selected station address to permit printout of the next station response. The cycle is repeated for each station number originally dialed.

(f) As the auto-send control advances to the preamble mode, a transmit program step pulse is generated again and the preamble control information is toned-out. The tone complete signals are generated and presented as start scan signals in a manner similar to that done in the start or dial numbers mode.

(g) At the end of the preamble mode, the auto-send control advances to the RU1 mode, generating a program step pulse. The program step pulse triggers flip-flop 2C3/ZA525-A. Simultaneously, the 0 volt priming signal on the P1B input of this flip-flop is removed, since the auto-send control is advanced to the RU1 mode placing a 0 volt signal on the RU1 lead. The flip-flop 2C3/ZA525-A is now primed on the P1A input. This signal is applied by inverter 2B3/ZA508-F which in turn is driven by NOR gate 2B2/ZA526-A. With the set in the RU1 or RU2 modes, leads RU1 and RU2 are 0 volts priming the flip-flop on the P1A input. Meanwhile, the 400-millisecond gated oscillator 2B4/ZA624 is timing-out, after which a start scan pulse is generated. When switching to the RU1 mode, the send and receive data clocks are unblinded and the transmission logic local and distant station(s) deserializers (module D) have to synchronize.

(h) A minimum of 4 delete characters are required to synchronize the deserializers. The delay start scan circuit permits the distant receiver to synchronize prior to sending the first station RU query. Also, since the individual acknowledgment response tones are 50 milliseconds in duration, it prevents overlapping of timing. In other words, the next station RU sequence is not transmitted until the previous station(s) acknowledge tone has dissipated. In the RU1 and RU2 modes, the flip-flop 3B3/ZA525-A is triggered by the positive printout complete signal on the set 1A input. This signal is derived from the response printout control logic flip-flop 10C2/ZA514-A and is a positive signal from the inverted output of the flip-flop when it is reset. Refer to 6545WD, sheet 10. Thus, 400 milliseconds later, a start scan signal starts the address counter, the counter steps to the next selected station gate, and that station RU is subsequently transmitted. The cycle is repeated until all of the connected stations have been polled.

C. Readout Control Detailed Description (6545WD, Sheet 2)

5.57 Readout during loading the three-digit station number in the memory takes place as follows:

(a) As previously described, the station number loading sequence is started when the output of the LOAD button triggers the clear/write flip-flop 3E6/ZA108-C in the address counter control logic, to the set 1 condition. The positive signal from the clear/write flip-flop is applied to the set 1A of the readout flip-flop 2D3/ZA525-B. This flip-flop then goes to the set 1 condition and a 200-microsecond positive pulse appears at inhibit gate 2E5/ZA520-F which is used to drive NOR 2E6/ZA526-B. The output of the NOR gate goes negative for 200 microseconds which in turn drives inverter 2E7/ZA520-C, resulting in a positive pulse called readout reset. This pulse is subsequently received by the reset logic in module B (OR gate 1F7/ZB511-C) and the transmission logic is reset. A readout (send mode) signal derived from the signal delay 2D4/ZA523-A is presented to flip-flop 8D2/ZB307-A in the data and clock control logic in module B (6546WD, sheet 8). The flip-flop is triggered and instructs the transmission logic to transfer to the send mode. It also unblinds the local clock and data leads and permits the local transmission logic serializer and deserializer to synchronize to facilitate printing-out the information that was loaded in the memory. When the deserializer is synchronized, a receiver in sync signal is received by the readout control logic control. The signal, a negative transition which drives inverter 2E6/ZA507-H, remains negative as long as the receiver is synchronized. Inverter 2E6/ZA507-H drives signal delay 2E5/ZA523-B and inhibit gate 2E5/ZA520-G. The combination of these two circuit elements are used to generate a 400-microsecond positive pulse which is inverted by 2E4/ZA520-D and enables NOR gate 2E3/ZA526-C by presenting a negative signal of 400 microseconds duration on input 29 of the NOR gate. Input 28 of the NOR gate is negative at this time since flip-flop 2D3/ZA525-B is in the set 1 condition. A positive pulse, 400 microseconds in duration, appears on the output of NOR gate 2E3/ZA526-C. This pulse drives the start 1 flip-flop 10D3/ZA514-C in the response printout control logic which in turn activates the printout control logic. Refer to 6545WD, sheets 9 and 10.

(b) In order to printout the correct information, a read/restore command must be presented to the memory control logic so that the information just read in the memory can be extracted and presented to the printout logic for subsequent printing on the page copy. This is accomplished by using the receiver in sync signal (inverted) which sets the address available flip-flop 3D4/ZA108-B in the address counter control logic to the 1 condition via the 1A input thus presenting a read/restore command to the character generator (memory control) logic. See 6545WD, sheet 3. The P1A input of the address available flip-flop 3D4/ZA108-A is primed by the readout flip-flop at this time.

(c) When the printout sequence is completed, the response printout control logic generates a printout reset pulse. This signal is a 10 to 20 microsecond positive pulse from power pulser 10C4/ZA528-A which is used to reset the readout flip-flop, the signal passing through switch SA-17 (CALL CONT READ/PRINT switch), to the set 0A input of the readout flip-flop. The address counter remains at the count selected until the LOAD button is depressed again whereby the cycle is initiated for the next selected STATION NUMBERS button or it may be reset to count 63 by pressing the PANEL RESET button.

(d) The following is a summary of the station numbered loading sequence:

(1) Set up number to be read in memory

(2) Select STATION NUMBERS button(s)

(3) Press LOAD button

(4) Counter advances to selected condition

(5) Present clear/write command to character generator logic

(6) Synchronize local transmitter and receive logic

(7) Present read/restore command to character generator logic

(8) Printout information read in

D. Off-Line Digit Sequence Test

5.58 The following is a detailed description of an off-line test in which all 55 three-digit sequences can be checked by printing the numbers on the page copy.

5.59 To perform this test, the SEND/REC CLOCK switch on module B, and the PRINTER CONTROL switch on module N must be in the TEST position. Test switches on module A labeled CALL CONT. READ/PRINT TEST A and B must be switched to the TEST condition. Switch A applies a ground signal to the P1B input readout flip-flop 2D4/ZA525-B. Switch B disables the reset input to the readout flip-flop and switches this signal to the start scan OR gate 2C5/ZA327-A, input 34. The next step is to select any or all STATION NUMBERS buttons for the test. To activate the logic, depress the TRANS PROG ADVANCE button on module A. A positive pulse is applied to the delay start scan flip-flop 2B3/ZA525-A and the flip-flop goes to the set 1 condition by virtue of setting its collector. The gated oscillator 2B4/ZA624 starts to time-out and after 400 milliseconds a pulse is applied to OR gate 2C5/ZA327-A. The start scan flip-flop is triggered and the address counter is started. The gated oscillator in this case acts as a filter for the MANUAL START SCAN button.

5.60 The counter stops at the first selected station number and an address available (-6 to 0 volts) is presented to the set 1B input of the readout flip-flop 2D3/ZA525-B. At the same time, a read/restore command is presented to the memory control, as described in Par. 5.57. The transmission logic receives a readout reset pulse and a readout and send mode signal, the local clock (2kc) and data leads are unblinded, and the serializer and deserializer are arranged for back-to-back transmission. The transmission logic starts to synchronize and when the receiver in sync signal is received, it is coupled through inverter 2E7/ZA507-H, signal delay 2E5/ZA523-B, and inhibit gate 2E5/ZA520-G. The latter two circuit elements form a 400-microsecond positive pulse from the receiver in sync signal. This pulse is applied to inverter 2E4/ZA520-D and subsequently a negative pulse appears on NOR gate 2E3/ZA526-C. The NOR gate is enabled, its output goes to ground, and a start printout signal is generated and presented to the response printout logic or gate 10B3/ZA327-B (6545WD, sheet 10). The response printout logic is activated and the information (3-digit station number) in the character generator output buffer (module F) is sampled and printed on the page copy.

5.61 When printout is completed, a printout reset pulse derived from the printout control power pulser 10C4/ZA528-A is applied to input 35 of OR gate 2C5/ZA327-A and a start scan signal results which starts the address counter. The address counter stops at the next selected station address whereby a second read/restore command is presented to the memory control, and the events described above are repeated. Note that the readout flip-flop 2E4/

ZA525-B is not reset when printout is completed since switch SA-17 is in the TEST position disabling the 0A reset. Therefore, when the second address available signal is applied to the set 1B input of the readout flip-flop, it is not triggered because it is already in the set 1 condition; consequently, a readout reset pulse is not generated and the readout send mode signal remains positive which is the send condition. The NOR gate 2F3/ZA526-E is enabled when the address available signal, which is positive is inverted by inverter 2E3/ZA520-H. Inputs 9 and 10 of NOR gate 2F3/ZA526-E are also negative at this time. A start printout signal is presented again to the response printout control and the information stored in the memory and related to the second address button selected is printed on the page copy.

5.62 When all of the desired information has been printed-out and the test is complete, the switches A and B are restored to their normal operating positions and the logic is reset.

E. Reset Logic Detailed Description

5.63 Two NOR gates, 2A4/ZA526-F and G, 6545WD, sheet 2, form an EDC reset pulse if an attempt is made to originate a multi-address or broadcast call with the EDC mode selected. The pulse is generated as follows:

(a) If MULTI-ADDRESS or BROADCAST are selected, NOR gate 2A4/ZA326-G is blinded. The positive trans auto-start signal, is inverted by NOR gate 2A3/ZA506-F. This negative signal enables NOR gate 2A5/ZA526-F, and its output goes to ground. The ground signal is presented to NOR gate 2B6/ZA318-F and subsequently to NOR gate 2B7/ZA318-G which inverts the pulse. The result is a positive signal called reset A. The positive pulse on reset A is presented to module B via JA2-G8 to the delay disconnect logic, OR gate 1D7/ZB511-A, resulting in a logic reset pulse that resets the HSSR Set.

(b) If the EDC mode button was not selected, NOR gate 2A4/ZA526-F is blinded and no EDC reset pulse is generated. Conversely, if MULTI-ADDRESS or BROADCAST were not selected, then an EDC call can be originated.

5.64 During an automatic call when the HSSR Set is in the RU2 mode, and the end of scan signal is presented to the auto-send control logic, an auto-call complete pulse is generated (a 250 us positive pulse). This positive pulse is applied to NOR gate 2B6/ZA318-F which blinds the gate, and its output goes to -6 volts for the duration of the pulse. NOR gate 2B6/ZA318-G inverts this negative signal and generates a positive pulse on the reset A lead. The HSSR Set logic is reset.

5.65 The combined circuits of signal delay 2F6/ZA124-B, no response flip-flop 2F7/ZA525-C, and NOR gate 2F8/ZA526-D generate a reset signal (no stations connected) if the following conditions exist: No called station(s) is connected during the dial response mode, and no called station(s) responds to its respective RU's when in the RU1 or RU2 mode. (Refer to 6545WD, sheet 2.)

(a) After the HSSR Set has completed dialing the selected numbers, the auto-send control advances to the dial response mode and a positive signal (-6 to 0 volt) is presented to signal delay 2F6/ZA124-B which delays the set 1 signal to the no response flip-flop 2F7/ZA525-C by 400 microseconds. The no response flip-flop is set to the 1 condition, its inverted output goes to -6 volts and NOR gate 2F8/ZA526-D is unblinded. The first connected (CO) response received from the tone-in logic resets this flip-flop and NOR gate 2F8/ZA526-D is blinded. If no connected signals are received before the end of scan signal is generated by the address counter, the end of scan signal (0 to -6 volts) will enable gate 2F7/ZA526-D and a 250-microsecond positive pulse is applied to NOR gate 1C7/ZA518-B. A start reset pulse is then generated resetting the logic.

(b) The same events take place when the auto-send control advances to the RU1 or RU2 mode. A positive signal, -6 to 0 volt, on leads defined as RU1 and/or RU2 is applied to NOR gate 2B3/ZA526-A. Its output goes to -6 volts and drives inverter 2B3/ZA508-F. The output of inverter 2B3/ZA508-F goes to 0 volt and this transition is applied to the set 1B input of the no response flip-flop 2F7/ZA525-C. The flip-flop is set to the 1 condition and NOR gate 2F8/ZA526-D is unblinded.

(c) The first acknowledge (ACK) received from a called station resets the no response flip-flop, blinds the NOR gate 2F8/ZA526-D, and the no reset pulse is generated when end of scan signal (negative) is applied to input 35 of NOR gate 2F8/ZA526-D. If no stations have acknowledged prior to the end of scan signal, a no stations connected signal is generated when NOR gate 2F8/ZA526-D is enabled by the end of scan pulse. As a result, the HSSR Set is reset (disconnected).

ADDRESS COUNTER CONTROL LOGIC (6545WD, Sheet 3 and Figure 19)

A. General

5.66 This logic is used primarily in the automatic send condition and certain off-line operations to perform the following functions:

(a) It controls the starting and stopping of the address counter by controlling the counter drive pulses presented to the counter.

(b) It gates the outputs from the start, preamble and station selection gates with outputs from the auto-send control logic in order to present read/restore commands to the character generator logic.

(c) It generates station count pulses during the preliminary scan phase.

(d) It controls the starting and stopping of the address counter and presents clear/write commands to the character generator logic during the off-line operation of loading the station numbers in the memory.

(e) It accepts a command sample signal from the character generator logic indicating that this logic has recognized the read/restore or clear/write commands and that appropriate action has been taken.

(f) It provides a local 2kc clock used for local transmission in the auto-send condition or for test purposes and also to drive the address counter. This clock is derived from a 4kc clock in the character generator logic.

(g) It also provides a means of switching out the 2kc clock and instead generate a variable test clock which can be varied between 100cps to 2.5cps. This clock permits slowing down certain events when performing off-line tests.

B. Address Counter Control Detailed Description (Figures 19 and 20)

5.67 As stated previously, the address counter control logic has two clock sources, a 2kc square wave clock and a variable test clock. The 2kc clock is derived from a 4kc clock originating in the character generator logic (modules E and F) and presented to the address counter control on connector pin JA2-B1 (6545WD, sheet 3). The 4kc clock provides a square signal 125 microseconds on (0 volt) and 125 microseconds off (-6 volts), which is applied to inverter 3B3/ZA105-B. The output of the inverter drives the clock divider flip-flop 3B4/ZA108-A. This flip-flop is arranged in the circuit as a binary stage which essentially divides the incoming clock rate in half to a 2kc square wave clock. The normal (N) output of the clock divider flip-flop drives three circuits: inverter 3A8/ZA105-A, signal delay 3B5/ZA103-A, and the set 1B input of the address available flip-flop 3D4/ZA108-B. The inverter 3A8/ZA105-A provides a local 2kc clock signal to external logic for test purposes and also to the data and clock control logic in module B (inverter 8F1/ZB314-D). This clock is used for local transmission at 2000 wpm prior to switching to the send and receive clocks derived from the data sets in the Telephone Equipment Cabinet.

5.68 The output inverter 3A8/ZA105-A also provides clock pulses to NOR gate 10E3/ZA518-G in the response printout control logic (6545WD, sheet 10). In this logic the clock pulses are gated for the purpose of column advancing the local printer. Refer to description of response printout control logic (Par. 5.112).

5.69 In the address counter control, the signal delay, 3B5/ZA103-A, delays the clock signals from the clock divider flip-flop 100 microseconds and in turn drives the set 1B input of the counter drive control flip-flop 3B6/ZA109-B and NOR gate 3B6/ZA107-F. The flip-flop provides the proper timing for unblinding NOR gate 3B6/ZA107-F for allowing a delayed clock pulse to pass through. It is triggered on a positive transition of the clock signal and a negative transition of the clock enables NOR gate 3B6/ZA105-K. The output of the NOR gate, along with the signal delay 3B6/ZA104-B, provides square wave counter drive pulses to the first stage of the address counter, flip-flop 4C1/ZA110-A. The address counter steps on each positive transition of a counter drive pulse. As a result, the start, station, and preamble sample signals used to prime the P1B input of the address available flip-flop 3D4/ZA108-B, are 125 microseconds out of phase with the normal clock pulse. Therefore sampling of the 1B input flip-flop occurs at the midpoint of the prime signal delivered to the character generator logic by the address counter.

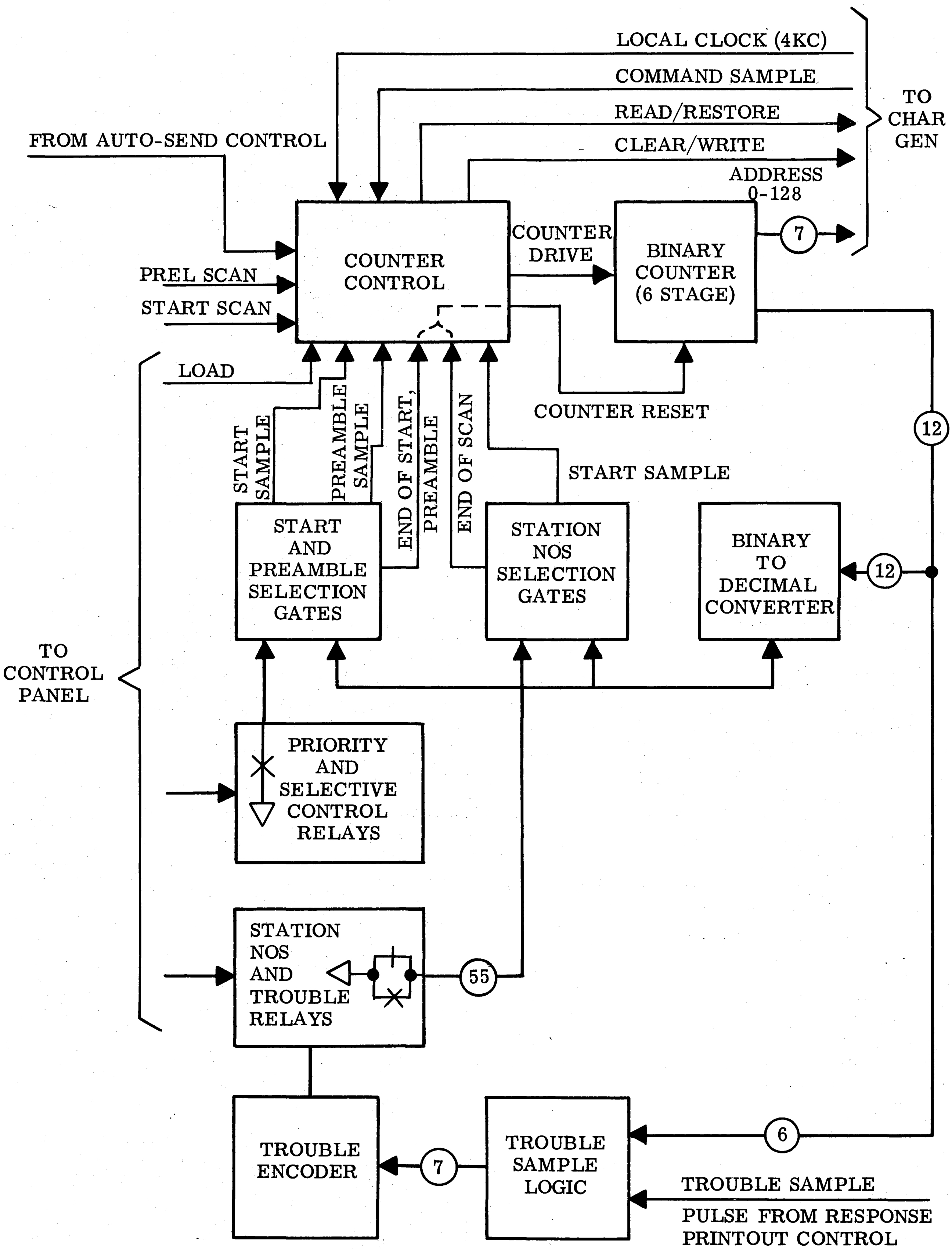


Figure 19 - Address Counter Control, Block Diagram

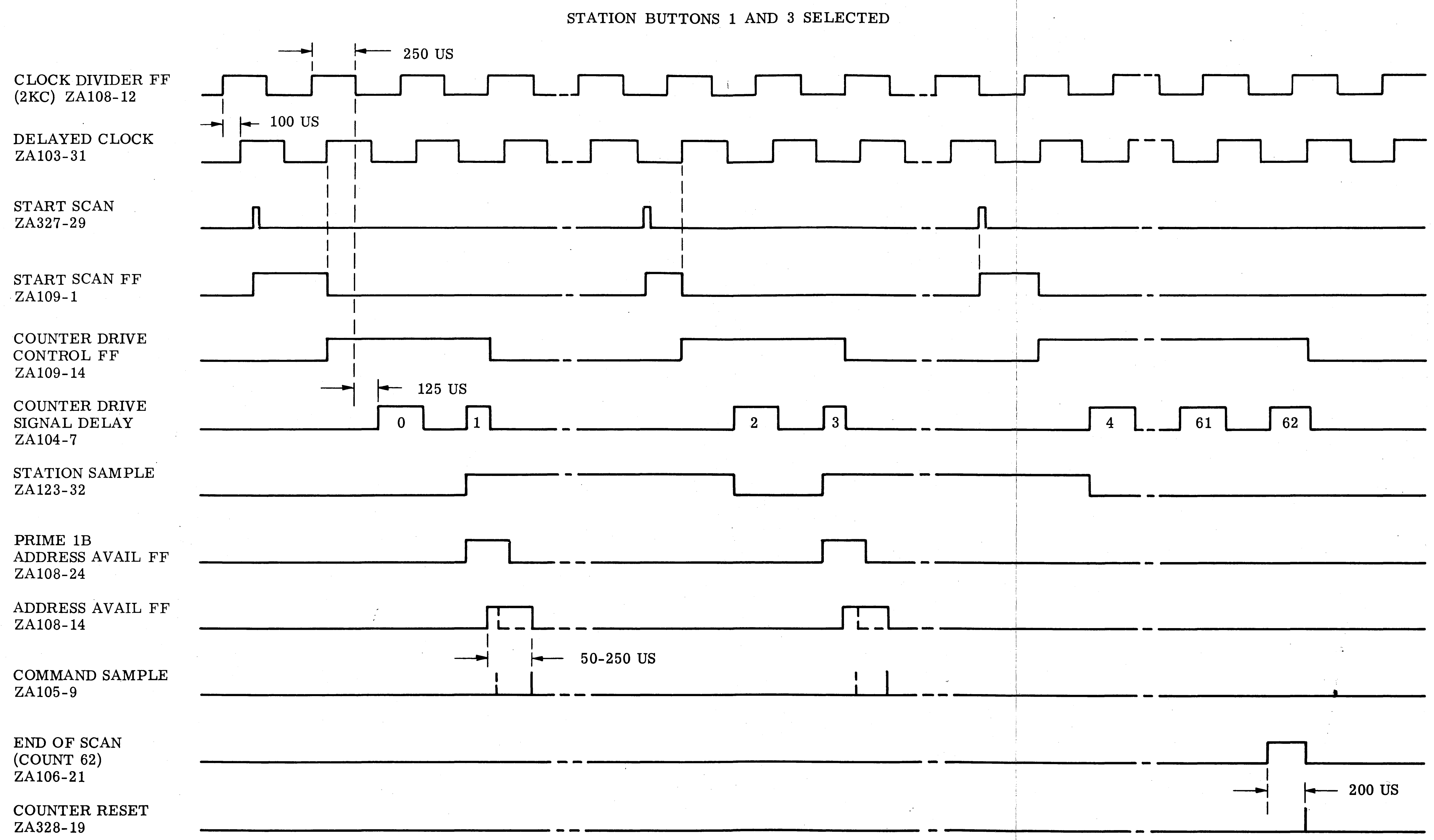


Figure 20 - Address Counter Control Timing

5.70 The following paragraphs describe the address counter control operation in detail when the HSSR Set is used to originate an automatic call. Refer to Figure 20 which is a timing diagram of the address counter control logic. In the example, station buttons 1 and 3 have been selected and these conditions are shown.

(a) The first signal that the address counter control logic receives is a positive start scan signal derived from the start address counter control OR gate 2C5/ZA327-A which initiates the preliminary scan phase. The positive transition of this signal is applied to the set 1B input of the start scan flip-flop 3B4/ZA109-C, setting this flip-flop to the 1 state. The normal (N) output of the start scan flip-flop primes the P1B input of the counter drive control flip-flop 3B5/ZA109-B. The first positive transition from the 100-microsecond signal delay 3B5/ZA103-A (delayed clock signal), received on the set 1B input of the counter drive control flip-flop will set it to the 1 state removing the blind signal from NOR gate 3B6/ZA107-F (counter drive gate). Input 32 of the NOR is also at -6 volts at this time. When the output of the 100-microsecond signal delay goes negative, the NOR gate 3B6/ZA107-F is enabled, its output goes to ground. For each negative clock signal applied to the input of the NOR gate, a positive signal appears on its output. With two station number buttons selected the address counter enables the two station selection gates 6C2/ZA305-C and ZA305-E, which are station gates 1 and 3 respectively, during the preliminary scan phase.

(b) Initially, all flip-flops in the address counter control are in the set 0 state. When originating an automatic call, the address counter is utilized during the preliminary scan phase, the start, dial numbers preamble, RU1 and RU2 modes. During these operating conditions, the address counter is sampling gates at a 2kc rate as it is stepped by the counter drive pulses. The selected outputs of the various gates are start sample, station sample, and preamble sample. These outputs are gated in the address counter control with outputs from the auto-send control logic (6545WD, sheet 8).

(c) Therefore, during a specific operating mode, a particular gate is enabled which primes the P1B input of the address available flip-flop 3E4/ZA108-B. This flip-flop is set to the 1 state when the first positive transition is received on the set 1B input from the clock divider flip-flop. As a result, the address counter stops counting and a read/restore or a clear/write command is presented to the character generator logic (modules E and F) and information is retrieved or written in the memory at the particular address presented to the character generator logic. As a result, two positive signals appear on the station sample lead, input 22 of inverter 3E2/ZA105-E. The output of the inverter goes to -6 volts enabling NOR gate 3C8/ZA107-G and two positive transitions 250 microseconds in duration appear on the output of this gate. These signals are the station count pulses and are presented to the auto-start control logic to determine the type of call being originated. Refer to description of auto-start control logic (Par. 5.36). Input 4 of NOR gate 3C8/ZA107-G is at -6 volts during the preliminary scan phase. This input, defined as inhibit station count, is derived from the preliminary scan flip-flop 1B6/ZA323-A in the auto-start control logic. At the end of the preliminary scan (end of scan) this flip-flop is reset to the 0 condition and the inhibit station count input goes to 0 volt inhibiting the station count pulses.

(d) The negative end of scan signal from the station selection gate inverter 7E8/ZA302-K enables NOR gate 3F4/ZA106-E. Its output goes to ground. This signal is applied to signal delay 3F4/ZA103-B and 200 microseconds later the positive transition drives power pulser 3F5/ZA328-B. The result is a positive pulse approximately 15 microseconds in duration which resets the counter drive flip-flop 3C5/ZA109-B, inhibiting counter drive pulses. It also applies a counter reset to the address counter flip-flops via their set 1A inputs. Thus, the address counter is reset to count 63. Note that only during the start and preamble modes are the respective NOR gates 3F4/ZA106-D and F unblinded to permit end of start and end of preamble signals to generate a counter reset pulse. Although it is not shown schematically, the output of the power pulser 3F5/ZA328-B is isolated from the logic reset buss by a diode. Therefore, a pulse generated by this power pulser does not cause a logic reset but resets the logic confined to the address counter control.

(e) The next signal to actuate the address counter control logic is a start scan signal, generated when the auto-send control logic advances to the start mode. The 64-

count flip-flop 4C8/ZA109-A has been set to the 1 condition when the transmitter auto-start pulse was generated by the auto-start logic. Therefore, the input defined as 64I is at -6 volts which unblinds NOR gates 3F4/ZA106-D and F. However, since the auto-send control is in the start mode (not in the preamble mode), the preamble (N) signal is -6 volts also. The end of start pulse (negative) occurs at a binary count of 71; the end of preamble signal occurs at a binary count of 82. When NOR gate 3F4/ZA106-D is unblinded, the end of start signal (since it comes first) causes a signal that resets the counter logic. Also, when in the start mode, the auto-send control logic provides a -6 volt signal derived from inverter 8E3/ZA319-A defined as start. This negative signal unblinds NOR gate 3E3/ZA106-A and allows a positive start sample, through inverter 3E2/ZA105-D, and a negative delayed clock pulse from inverter 3B7/ZA105-K, to enable this gate.

(f) In the example used in Figure 20, two station buttons have been selected making it a multi-address call. The three-digit sequence 943 (request for bridge) must be toned-out to the Telephone Equipment Cabinet during the start mode. Assume the call is routine and therefore no priority tones have to be toned-out. The information representing 943 is stored in the memory at address 69. Upon receiving the start scan signal the counter drive gate, NOR gate 3B6/ZA107-F, is unblinded in a similar manner as when the preliminary scan phase is initiated. Counter drive pulses are applied to the address counter. When a count of 69 is reached (64 + 5), a positive start sample appears on input 14 of inverter 3D2/ZA105-D. The output of the inverter goes to -6 volts which in turn unblinds NOR gate 3D3/ZA106-A. This NOR is enabled by the inverted counter drive pulse and therefore the P1B input of the address available flip-flop is primed (0 volt). The first positive transition of the normal clock signal is applied to the set 1B input of the address available flip-flop therefore setting this flip-flop to the 1 condition. The positive transition (normal output) from the address available does the following:

(1) It resets the counter drive control flip-flop 3C5/ZA109-B to the 0 condition and blinds the NOR gate 3B6/ZA107-F which inhibits the counter drive pulses.

(2) It presents a positive address available signal to the tone-out control flip-flop 2B2/ZB115-C.

(3) It enables NOR gate 3D7/ZA107-D.

(g) When NOR gate 3D7/ZA107-D is enabled, the positive signal from this gate drives inverter 3D8/ZA105-G. The output of the inverter goes to -6 volts and this negative signal (read/restore) is presented to the character generator logic via connector pin JA2-A8. This signal remains negative until the character generator responds with a negative command sample signal via connector pin JA2-A10. This signal is applied to inverter 3D2/ZA105-C and essentially means that the character generator logic has sampled the read/restore command and the information in memory address 69 has been placed in the character generator output buffer for subsequent sampling by the call control logic. The command sample is received approximately 50 to 250 microseconds after the read/restore command was presented to the character generator logic. The positive signal from inverter 3D2/ZA105-C is used to reset the address available flip-flop 3D4/ZA108-B via the set 0B input. The negative read/restore command is consequently removed since NOR gate 3D7/ZA107-D is blinded, its output going to -6 volts.

(h) At this time the information appearing in the character generator output register, the three-digit sequence 943, is toned-out to the Telephone Equipment Cabinet. Upon completion, a tone-out complete generates another start scan signal and counter driver pulses are again applied to the address counter. The next signal received by the address counter control is the end of start signal which is derived from inverter 5C7/ZA302-A in the start selection gate logic (6545WD, sheet 5). This negative signal occurs when the address counter reaches a count of 71, therefore enabling NOR gate 3F4/ZA106-21. Its output goes to ground and 200 microseconds later a counter reset pulse is generated which resets the address counter to count 63. The 64-count flip-flop 4C8/ZA109-A, is set to the 0 condition along with the counter drive control flip-flop 3C5/ZA109-B. The latter flip-flop, when reset, removes the counter drive pulse signal.

(i) The next start scan signal is generated when the auto-send control programmer advances to the dial numbers mode. The sequence of events that occurs in the address counter control logic are similar to those described above when the set was in the start mode. However, in this case, the station sample signal is monitored by the logic and a different set of addresses (0 through 63) are presented to the character generator logic representing the memory address where the station numbers are stored so that this information can be dialed. With the auto-send control in the dial numbers mode, a 0 volt dial numbers signal is presented to NOR gate 3F2/ZA106-G which blinds this gate. Its output goes to -6 volts and NOR gate 3E3/ZA106-B is unblinded. Therefore, a positive station sample signal (address 1 for button no. 1) accompanied by a negative clock signal enables NOR gate 3E3/ZA106-B and an address available together with a read/restore signal is generated. The counter is stopped and station no. 1 call numbers are toned-out. Note that when the auto-send control is in the dial response, RU1, or RU2 modes, the same NOR gate 3F2/ZA106-G is blinded; therefore NOR gate 3E3/ZA106-B is enabled every time a positive station sample signal is presented to inverter 3E2/ZA105-E. Also, the negative end of scan signal, which is count 62, is presented to NOR gate 3F4/ZA106-E to generate a counter reset pulse. Though the negative end of start and end of preamble signals occur first (counts 7 and 18) these signals are prevented from generating a counter reset pulse since NOR gates 3F4/ZA106-D and F are blinded during the previously described operating modes.

(j) During the preamble mode NOR gate 3E3/ZA106-C is sampled by a positive preamble sample signal accompanied by a negative clock signal on input 28. The same events as previously described transpire and the preamble information is subsequently read out of the memory and toned-out.

C. Logic for Loading Station Numbers (Figure 21)

5.71 One of the off-line operations is the loading of the station numbers in the memory. The address counter control is activated by the LOAD button and generates the clear/write command for loading the information. Refer to Figure 21 which is a block diagram of logic involved in loading the station numbers. Figure 22 is the timing diagram of a loading cycle.

5.72 First, the three-digit number to be loaded in the memory is set up on the STATION PROGRAMMER switch located on the control panel. The load cycle is initiated when the operator depresses LOAD on the control panel. This action operates a set of transfer contacts associated with the LOAD button. The common is connected to ground. The normally closed (NC) contact opens and the normally open (NO) contact closes, resulting in signals being applied to the address counter control logic on connector pins JA1-H10 and H9 respectively. The signals are subsequently presented to two inverters arranged as a dc flip-flop which eliminate signal breaks caused by contact bounce. When the NC contact opens, it removes the ground signal being applied to the output of inverter 3E6/ZA320-G and also the input to inverter 3E6/ZA320-F. Simultaneously, the NO contact closes and applies a ground signal to the output of the first inverter 3E6/ZA320-F and the input to the second inverter 3E6/ZA320-G thereby turning the second inverter off. Its output goes to -6 volts feeding back to the input of the first inverter. For example, if the NO contact should bounce open, by regenerative action, the first inverter will hold the second inverter off and the result is a clean signal on the output of the second inverter, 3E6/ZA320-G with no breaks due to contact bounce.

5.73 When the LOAD button is released, a positive signal appears on the output of inverter 3E6/ZA320-G which is applied to the set 1B input of the clear/write flip-flop 3E6/ZA108-C. The P1B input of the clear/write flip-flop is at 0 volt only if the HSSR Set is on-hook. This prevents the operator from loading the memory while a call is in progress. However, with the P1B input of the clear/write flip-flop at 0 volt, the positive transition occurring when the LOAD button is released sets this flip-flop to the 1 condition. The normal output of the clear/write flip-flop goes to 0 volt and this signal is presented to the start address counter control, input 33 of OR gate 2C5/ZA327-A, which results in a start scan signal. The start-scan flip-flop 3C4/ZA109-C is subsequently triggered and the counter drive gate is unblinded. The normal output of the clear/write flip-flop also blinds NOR gate 3D7/ZA107-D, and its output remains at -6 volts. Therefore, inverter 3D8/ZA105-G holds a

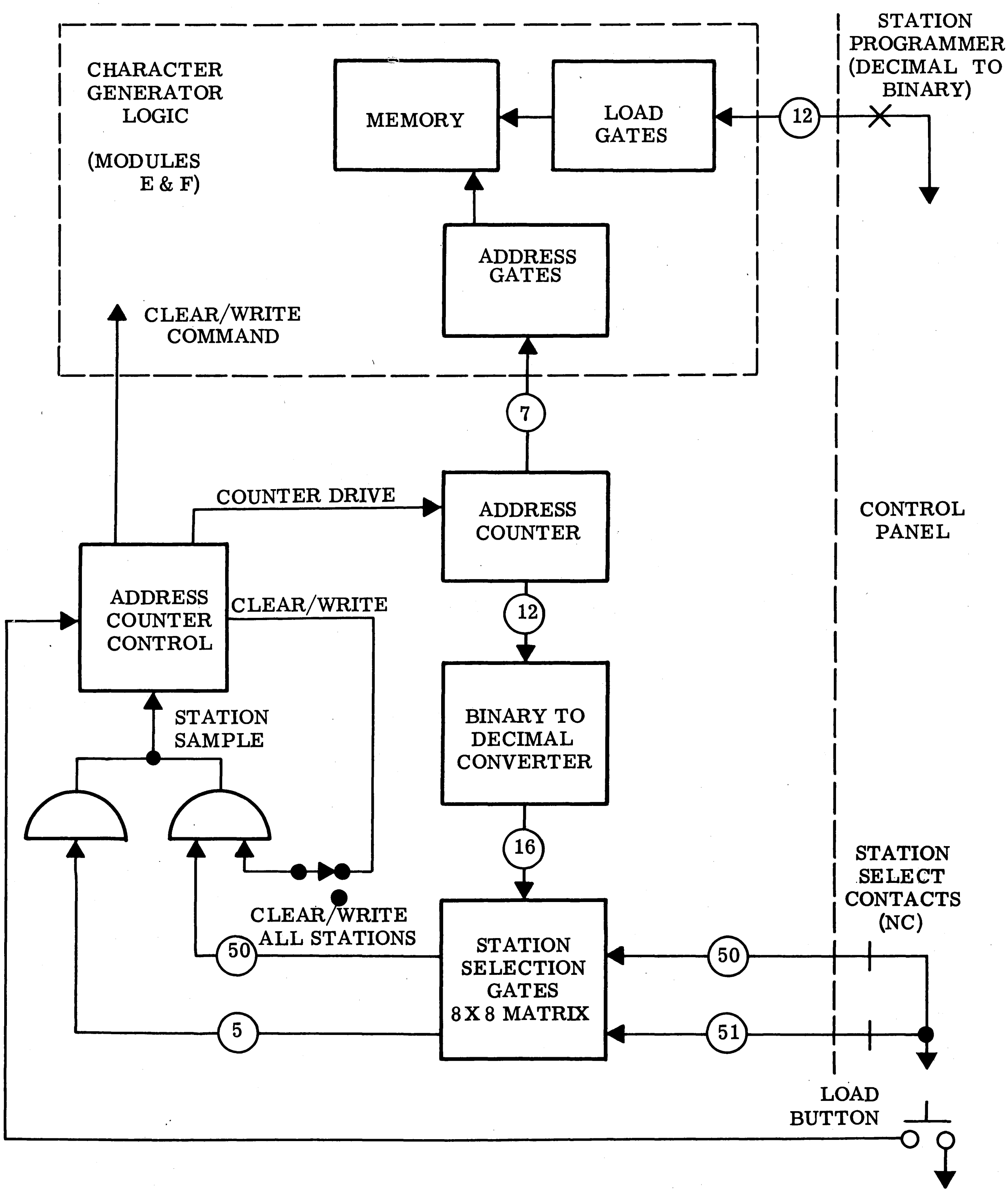
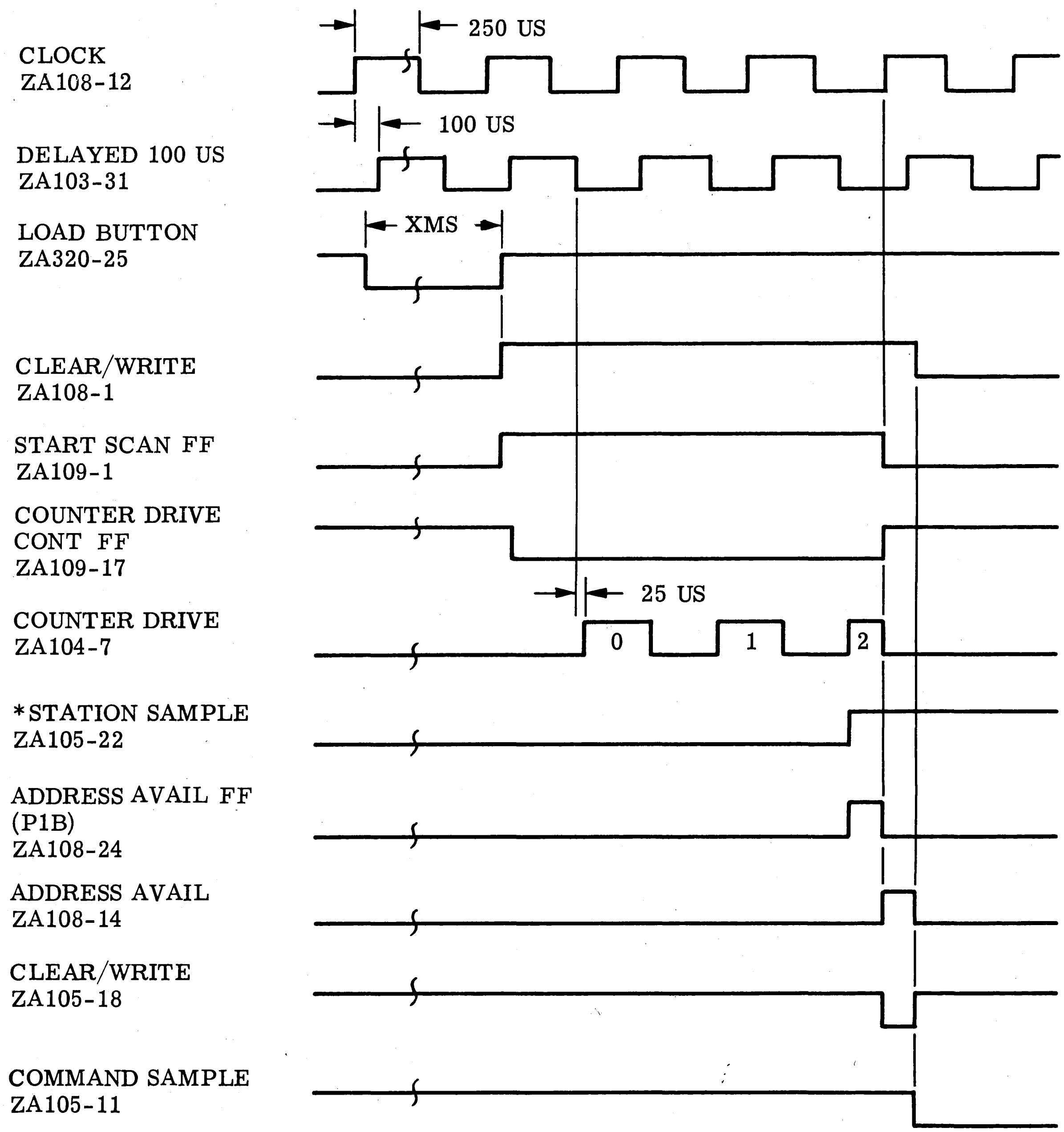


Figure 21 - Station Number Loading Logic, Block Diagram



* NOTE: STATION SAMPLE REMAINS POSITIVE UNTIL COUNTER IS RESTARTED (LOAD BUTTON PRESSED AGAIN) OR RESET.

Figure 22 - Station Number Loading Logic Timing (Station Button 2 Selected)

ground signal on the read/restore lead preventing a read/restore command from being presented to the memory control simultaneously with a clear/write command. The inverted output of the clear/write flip-flop goes to -6 volts unblinding NOR gates 3E7/ZA107-C and 3D3/ZA318-C. Meanwhile, the address counter is being stepped and when it samples a station number gate related to a particular station number selected (station 2 is selected to illustrate timing) for the purpose of loading a number, a positive station sample signal is received and applied to inverter 3E2/ZA105-E. The output of the inverter drives NOR gates 3E3/ZA106-B and 3D3/ZA315-C, the former NOR gate is blinded at this time. Therefore, NOR gate 3D3/ZA315-C is enabled when input 28 goes negative which is the inverted counter drive signals and the address available flip-flop is subsequently primed on the P1B input. The address available flip-flop is triggered to the set 1 condition by the first positive transition appearing on the set 1B input from the clock divider flip-flop.

5.74 When the address available flip-flop is set to the 1 state, NOR gate 3E7/ZA107-C is enabled, its output goes to ground and this signal is applied to inverter 3E8/ZA105-H. This results in a negative (0 to -6 volts) clear/write signal being presented to the character generator logic via connector pin JA2-A9. Simultaneously, the address available flip-flop blinds the counter drive NOR gate 3B6/ZA107-F, removing the counter drive pulses by holding the input, pin 33, of the NOR gate at ground; its output remains at -6 volts. The address available flip-flop resets the counter drive control flip-flop to the 0 state.

5.75 A negative command sample signal is received from the (memory control) character generator logic approximately 50 to 250 microseconds after the clear/write command is presented and the binary information representing the three-digit number appearing on the STATION PROGRAMMER switch is loaded in the memory. Refer to the appropriate section for a detailed description of character generator operation. The command sample signal is applied to inverter 3D2/ZA105-C through the normally closed COMMAND COMPLETE switch. This results in a positive output signal from the inverter which resets the address available flip-flop thus removing the ground signal being applied to input 33 of the counter drive NOR gate 3B6/ZA107-F. The inverted command sample signal is also used to reset the clear/write flip-flop to the 0 condition restoring the circuit to its original state.

5.76 Each time the LOAD button is depressed a load cycle is initiated and a clear/write command is presented, provided a station selection gate is enabled, and one three-number address is loaded in the memory. If no STATION NUMBERS buttons are selected, the address counter advances to count 62 and an end of scan signal is generated. Then, 200 milliseconds later the counter is stopped and the control logic is reset. A summary of the loading sequences is as follows:

(a) Select STATION NUMBER button to be loaded. (See Figure 6.)

(b) Arrange STATION PROGRAMMER switch on control panel to the desired three-digit number.

(c) Momentarily press the LOAD button.

(d) Clear/write flip-flop is triggered and address counter starts.

(e) Address available signal generated, counter stops, clear/write command presented to memory control logic.

(f) Information is written in the memory.

(g) Repeat cycle or reset.

<u>Note</u>: If more than one station number is to be loaded, the desired buttons can be selected and only the STATION PROGRAMMER need be changed after each number is loaded.

D. Logic for the Elimination of the Polling of Unused Station Buttons.

5.77 The purpose of this logic is to eliminate the polling of unused station select buttons, in the RU modes during a broadcast transmission.

5.78 The logic consists of two NOR gates, 3D5/ZA313-C and 3D6/ZA305-B, and one INHIBIT gate, 3D5/ZA302-J.

5.79 The unused station button must be programmed with 999 (an invalid CDC) for this logic to function properly.

5.80 As explained before, when each station select button is scanned, it will generate a station sample signal which will cause the address available F/F 3D4/ZA108-B to go set 1. The inverted output of the address available F/F will cause a read/restore command to be sent to the memory so the CDC may be loaded into the tone-out logic of the B module.

5.81 If the first digit from the memory is a nine (invalid CDC), a 0 V from NOR gate 3B4/ZB106-19 is sent to NOR gate 3D5/ZA313-30, insuring a -6 V at output pin 20. This -6 V is fed directly to 3D6/ZA305-6. Pin 7 of ZA305 will be a -6 V during the RU1 and RU2 modes. Approximately 100 microseconds later, a -6 V command sample signal is applied to 3D6/ZA305-5 causing its output pin 19 to go to 0 V. This 0 V is applied to the 1A lead of the start scan F/F 3C3/ZA109-C. The P1A lead of that F/F is a 0 V during a broadcast call; thus, the F/F goes to set 1 starting the scan for the next station select button. Thus, when a 9 is detected as the first digit of a CDC, it will not be printed and the scan will go to the next button.

5.82 When a valid CDC (first digit other than a 9) is detected, -6 V will be applied to 3D5/ZA313-28, -29, -30, causing output pin 20 to go to 0 V. This 0 V is applied to 10D1/ZA514-25. 10D1/ZA514-24 is at a 0 V during broadcast call; thus, the start 2 F/F, ZA514B, will go set 1 allowing the CDC to be transmitted and printed.

5.83 During the single or multi-address call, the address available signal will be sent to the start 2 F/F via INHIBIT gate 3D5/ZA302-J, which is blinded on its pin 31 during a broadcast call.

E. Address Counter Control Test Features

5.84 Test Clock: With the VAR. TEST CLOCK switch 3A1/SA3 in the ON position, the gated oscillator 3A2/ZA102 will free run and generate narrow positive pulses 10 to 20 microseconds in duration occurring at a specific repetition rate depending on the setting of the speed control potentiometer located on the module front panel. To switch the VAR. TEST CLOCK in the circuit, the 4kc clock must be switched out. This accomplished by LOCAL CLOCK ON/OFF switch 3B3/SA4. With the clock switch in the OFF position, the 4kc clock is removed and the test clock pulses are applied to the clock divider flip-flop.

5.85 Manual Step: The manual step signal originates from the MANUAL STEP pushbutton 3B1/SA2 located on the module A front panel. A set of transfer contacts drives two inverters arranged as a dc flip-flop previously described. The output of inverter 3B3/ZA116-J is applied to a MANUAL STEP switch, 3B3/SA7. With the MANUAL STEP switch in the ON position and the VAR. TEST CLOCK switch in the OFF position, the clock divider flip-flop 3B4/ZA108-A is manually triggered, and the address counter is stepped manually and a local clock is manually presented.

5.86 Manual Start Scan: This pushbutton (2C1/SA9) provides a method for manually starting the address counter. The MANUAL START SCAN button, when operated, applies a positive signal (-12 to 0 volts) to start scan flip-flop 2C3/ZA525-A placing it in the set 1 condition. Approximately 400 ms later a positive start scan pulse is applied to the address counter control.

5.87 Command Complete: This switch (3D2/SA11) simulates the command sample signal received from the memory control and the logic can be tested without applying an external command sample signal. When the COMMAND COMPLETE switch is in the TEST position, the command sample signal from the character generator logic is disabled and the output of the 200-microsecond signal delay 3D5/ZA104-A is applied to inverter 3D2/ZA105-C. Each time the address available flip-flop is set to the 1 condition, its inverted output is delayed 200 microseconds and applied to inverter 3D2/ZA105-C. This results in a delayed positive signal which is fed back to the set 0B input of the address available flip-flop 3D4/ZA108-B and resets this flip-flop and the clear/write flip-flop if the latter circuit was triggered.

ADDRESS COUNTER AND SELECTION GATES

A. General (Figure 23)

5.88 Since the address counter and selection gate logic are closely related, the combined logic is described in the following paragraphs. The call control address counter is shown on sheet 4 of 6545WD. The selection gate logic which is divided into start and preamble and station selection gates is shown on sheets 5, 6 and 7 of 6545WD.

(a) The address counter is a 7-stage counter driven by the counter drive pulses derived from the address counter control logic (6545WD, sheet 3). The seventh stage is externally controlled by the call control logic. The counter drives a binary to decimal converter and the converter, in turn, drives the selection gate logic which is arranged in an 8 by 8 matrix. The address counter also presents an address to the character generator logic (memory control) in terms of a binary number. This address, when accompanied by a read/restore or clear/write command to the character generator, will read out or load information into the memory. Refer to the appropriate section for description of character generator logic and memory loading operation. The address counter and related logic are shown in Figure 23.

(b) The address counter also drives the trouble encoder logic, described in Par. 5.94.

(c) During the auto-send condition the address counter is activated when the HSSR Set is in the following operating modes.

(1) Preliminary scan - samples the station selection gates to determine the number of stations selected.

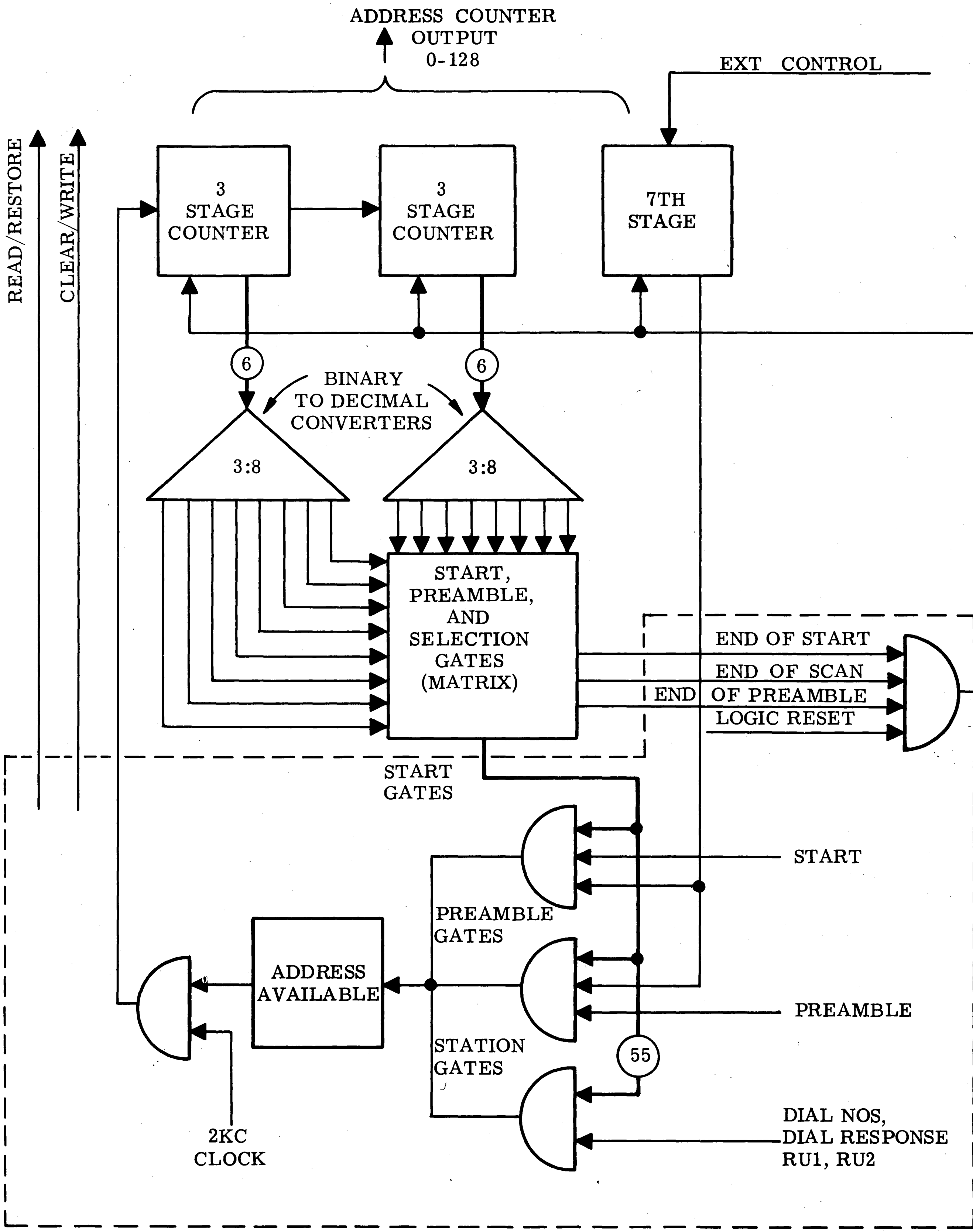


Figure 23 - Address Counter and Related Logic, Block Diagram

(2) Start mode - samples start selection gates so that control information can be read out of the memory, converted, and toned-out.

(3) Dial numbers mode - samples station selection gates so that the binary information representing the station numbers can be retrieved from the memory, converted, and toned-out.

(4) Dial response mode - samples station selection gates again. The information representing the station numbers is read out of the memory, converted, and subsequently printed out on the page copy as the station number along with the response from the ESS.

(5) Preamble mode - samples the preamble selection gates so that information can be read out of the memory, converted, and toned-out as control tones to the distant receive stations.

(6) RU1, RU2, mode - operation is the same as the dial response mode with one exception. The three-digit sequence is transmitted and the send station waits for the response from the distant station.

(d) The address counter is also activated when the station numbers are loaded. This procedure was described in Par. 5.76.

(e) The address counter is controlled by the address counter control logic previously described (Par. 5.67). Under normal operating conditions the counter is stepped at a 2kc rate. It presents address counts 0 to 127 to the character generator logic and by controlling the seventh stage the counts can be shifted from between 0 and 63 to counts between 64 and 127. The station numbers are stored between counts 0 and 55. The various control information is stored in address counts greater than 64. See Table 4 which lists the call control addresses and associated control information stored in the memory.

(f) The 16 outputs of the decimal converters are used to sample 1 of 64 selection gates. One set of binary to decimal converters has outputs for the first 8 counts (0 to 7). The second set of converters has outputs ranging between 8 and 56. The outputs of the converters has outputs defined as: 0, 1, 2, 3, 4, 5, 6, 7, 0', 8, 16, 24, 32, 40, 48, and 56. For example, a count of 25 is represented by outputs on leads 1 and 24.

(g) As stated previously, the station selection gates are arranged to form an 8 by 8 matrix which is logically illustrated in Figure 24.

(h) In Figure 24, each dot in the matrix represents a three-input NOR gate. Two of the inputs originate at the binary to decimal converters. The third input originates from a set of station select and trouble contacts as shown. For example, if STATION NUMBERS button 25 is selected, the normally closed contact S25 is open and the NOR gate is unblinded. As the address counter steps, each gate is sampled as indicated in the Figure 24. When a count of 25 is reached this particular NOR gate is enabled and its output goes to ground as shown in Figure 24. The output of NOR gates are OR'd together so that a single output called the station sample is generated. This signal is forwarded to the address counter control and an address available signal is generated along with a read/restore command to the character generator logic. Therefore, for each selected station number, a station sample pulse results when the address counter samples the respective gate. Since only 55 station buttons are on the control panel, there are 55 station select gates. At the count of 62 a gate is sampled and a signal is generated called end of scan. This signal is used to control other logic and is also used to reset the address counter to the count of 63.

(i) The start and preamble selection gates are arranged as the station selection gates and are shown on sheet 5 of 6545WD. The gates at the top of the schematic comprise the start selection gates which are sampled by the address counter during the start mode. Two of the inputs to these gates are derived from the address counter decimal converter and the third input is derived from logic which represents selected conditions for the originating call such as level of priority and whether the call is a multi-address or broadcast. The respective binary information is stored in the memory at address counts greater than 64. The data is read out of the memory, converted, and subsequently toned-out as control tones to the Telephone Equipment Cabinet. Refer to Table

4 which lists the address counts used during the start and preamble modes and the corresponding binary information stored in the memory along with its control function. If the originating call is routine (no priority) and a single address call, none of the start gates will be enabled and the only signal generated is the end of start signal.

(j) Each time the address counter samples a start selection gate which is not blinded, a start sample signal is generated; however, an address available signal is only generated, from the start sample, in the address counter control if the set is in the start mode. Also, during the start mode, the seventh stage of address counter is in the 1 condition, making

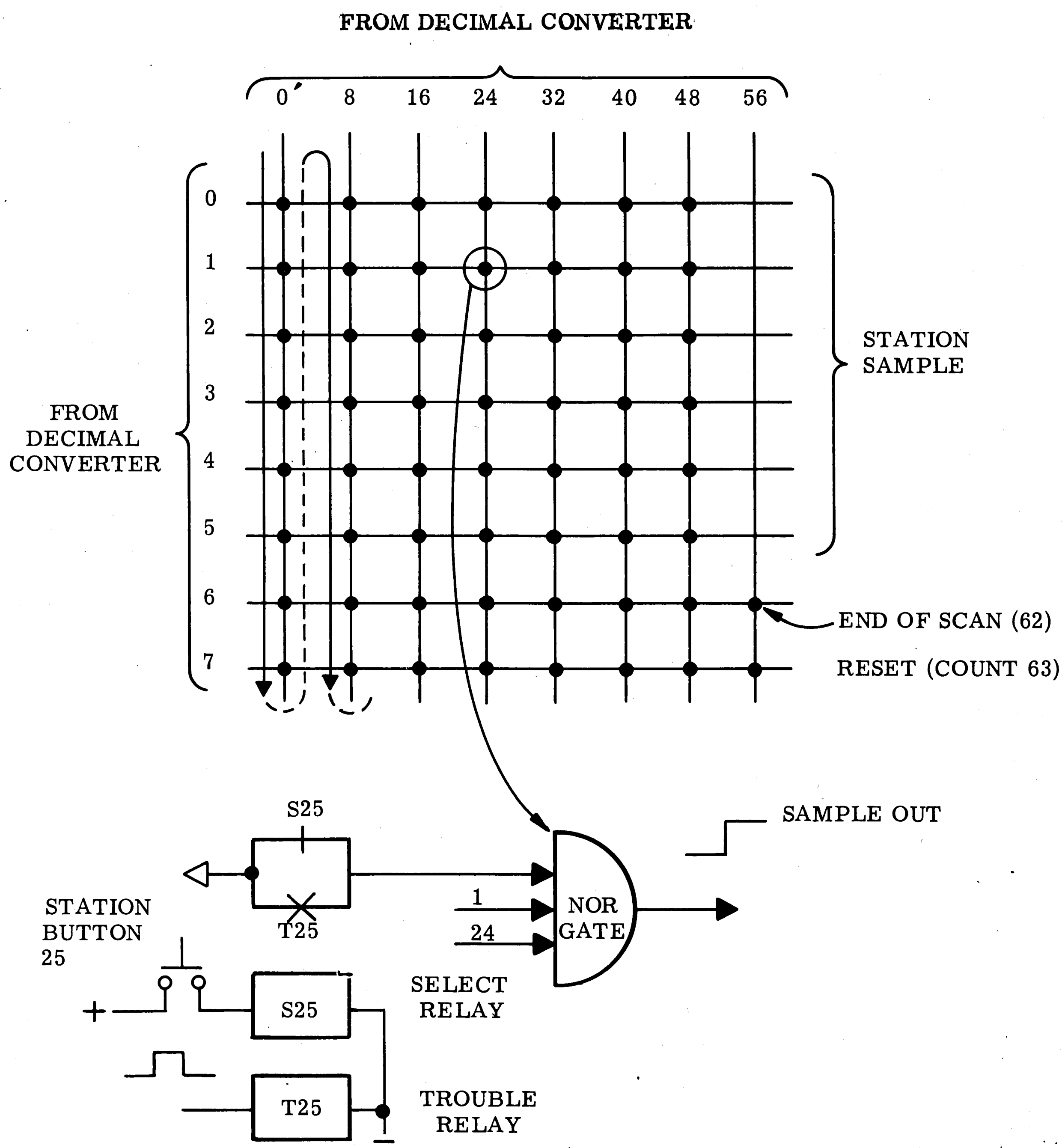


Figure 24 - Station Selection Gate Matrix, Functional Diagram

addresses presented to the character generator logic 64 or greater.

5.89 The preamble selection gates (bottom of 6545WD, sheet 5) are sampled during the preamble mode. Four basic pieces of control information are toned to the receive station(s) during the preamble mode: speed, code, type of error control, punch on/off and a go data tone. The signals from these selected gates produce a preamble sample signal which is presented to the address counter control and an address available signal is subsequently generated. Also during the preamble mode the seventh stage of binary counter is in the 1 state and the addresses presented to the character generator range between counts 64 and 127. The last preamble gate sampled is used to generate an end of preamble signal. This signal is presented to the address counter control and the address counter is reset. The end of preamble signal is also used to reset the no-response timers and to trigger the send data control circuit.

B. Start Mode (Figure 23 and 6545WD, Sheet 4)

5.90 The following description describes the operation of the address counter and associated logic during the start mode. In this description it is assumed that a flash call is being originated.

(a) After the completion of the preliminary scan a transmitter auto-start pulse is generated in the auto-start control logic. This pulse is used to set the seventh stage of the address counter 4B8/ZA109-A thus applying a 0 volt signal on lead (64) to the character generator logic. This automatically makes all address counts presented to the character generator 64 or greater and the flip-flop will remain in this state until the counter is reset.

(b) The address counter is started when a delay start dial signal is received from the Telephone Equipment Cabinet so that

TABLE 4 - ADDRESSES AND BINARY INFORMATION

	Memory Address	Address (Binary Equivalent) 1	2	4	8	16	32	64	Memory Information (Bits) b1	b2	b3	b4	b5	b6	b7	b8	b9	b10	b11	b12	Control Function	Conversion Tone Out Digits
START MODE	65	1	0	0	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	Flash Override	13
	66	0	1	0	0	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	Flash	14
	67	1	1	0	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	Immediate	15
	68	0	0	1	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	Priority	16
	69	1	0	1	0	0	0	1	1	0	0	1	0	0	1	0	1	1	0	0	Multi-Address	943
	70	0	1	1	0	0	0	1	1	0	0	1	1	0	0	1	0	1	1	0	Broadcast	996
	71	1	1	1	0	0	0	1	← Not Used →												End of Start	-
PREAMBLE MODE	72	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	2400 *	0
	73	1	0	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1200	2
	74	0	1	0	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	600	3
	75	1	1	0	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	Baudot	8
	76	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	ASCII *	0
	77	1	0	1	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	EDC	6
	78	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	ED *	0
	79	1	1	1	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	Punch On	9
	80	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	Punch Off *	0
	81	1	0	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	Go Data	4
	82	0	1	0	0	1	0	1	← Not Used →												End of Preamble	-

*Indicates normal reset conditions.

pertinent start information, such as level of priority and type of call being originated, can be toned-out.

(c) In this case a flash call is being originated and the input on JA1-F8 is at -6 volts. This signal is derived from inverter 4C3/ZG119-D in the precedence and mode control logic (6547WD, sheet 4).

(d) When the address counter has received three counter drive pulses, which actually represents a binary count of 2, flip-flops 4C2/ZA110-B and 4C8/ZA109-A are in the set 1 condition. The binary count is 0 1 0 0 0 0 1 which is address count 66. At this particular count, emitter followers 4F2/ZA117-C and 4F5/ZA117-J outputs are -6 volts. Two negative outputs defined as (0') and (2) enable the start NOR gate 5B3/ZA303-C which results in a 0 volt signal on the output. The output of this gate is combined with three other NOR gates so that if one or more is enabled a 0 volt signal results which in turn blinds NOR gate 5C7/ZA305-A. The output of NOR gate 5C7/ZA305-A goes to -6 volts which in turn is applied to inverter 5D7/ZA302-B. The output of this inverter goes to 0 volt and the start sample signal is generated. This output remains at 0 volt until the counter is restarted. The positive start sample signal is presented to the address counter control which results in an address available signal, the counter drive pulses are removed and a read/restore command is presented to the character generator logic. The data stored in memory address 66 is read-out and the information defined as memory output is forwarded to the tone-out control by the character generator logic. The data is subsequently converted and toned-out as tone 14 representing a flash call.

(e) A tone-out complete signal starts the address counter again and, if a single address call is originated, the next start selection gate enabled is NOR gate 5C7/ZA303-A. This gate is sampled at count of 7 which is actually address count 71 (64 + 7). At this time the inverted output of the seventh stage of the address counter (64I) unblinds this gate, and at count 71 its output goes to ground. This signal is applied to inverter 5C7/ZA302-A and a 0 to -6 volt signal (end of start) is generated and applied to the address counter control and other logic. The end of start signal results in a counter reset pulse and therefore the address counter is reset to count of 63. The end of start signal is also used to start a no-response timer, described in a subsequent paragraph.

C. Dial Numbers Mode

5.91 The following is a detailed description of what occurs in the address counter and associated logic when the station selection gates are sampled for toning out the abbreviated three-digit number during the dial numbers mode. It is assumed that station button 25 has been selected, representing the three-digit sequence 695.

(a) After the first stage (4C2/ZA110-A) of the address counter has received 26 drive pulses from the address counter control, flip-flops 4C2/ZA110-A, 4C5/ZA111-A and B are in the set 1 condition. This represents a binary number as follows:

1 0 0 1 1 0 0

$$2^0 + 0^1 + 0^2 + 2^3 + 2^4 + 0^5 + 0^6 = 25$$

Therefore, leads 1, 8, and 16 to the character generator logic (memory control) are at 0 volts, the others are at -6 volts, thus representing the address count 25. In the 0 to 7 binary to decimal converter NOR gate 4D2/ZA114-B is enabled since inputs 5, 6 and 7 are at -6 volts at this time. The output of emitter follower 4F2/ZA117-B is at -6 volts. This output is defined as lead (1). At the same time, NOR gate 4D6/ZA113-E in the 8 to 32 decimal converter is enabled since inputs 8, 9, and 10 are all at -6 volts. Therefore, the output of emitter follower 4F6/ZA117-M goes to -6 volts. This output is lead (24).

(b) Referring to the station select gates (1 to 31) on sheet 6 of 6545WD, the -6 volt signals on output leads 1 and 24 from the address counter are applied to NOR gate 6E5/ZA308-C, inputs 28 and 29 respectively. Input 30 is open circuit since station select relay 25 is energized. With inputs 28 and 29 at -6 volts, NOR gate 6E5/ZA308-C is enabled and its output, pin 20, goes to ground. The 0 volt signal is then applied to NOR gate 6D8/ZA308-A and the output of this gate goes to -6 volts. The -6 volt signal from this gate is then applied to inverter 6D8/ZA302-F which results in a -6 to 0 volt signal appearing on pin 27 of the inverter. Note that the outputs of inverters 6D8/ZA302-E, F and

7D8/ZA302-G, H are connected together to form an OR function. These inverters in turn drive the emitter of inhibit gate 7D6/ZA123-K and a positive station sample signal is subsequently presented to the address counter control logic, inverter 3E2/ZA105-22. This signal remains positive until the counter is restarted by the address counter control. Since the auto-send control is in the dial numbers mode, the address available flip-flop in the address counter control is triggered, the counter drive pulses are blinded, and a read/restore command is presented to the character generator logic. The data representing the 3-digit number is presented to the tone-out converter (6546WD, sheet 3) and converted as illustrated in the block diagram, Figure 25.

(c) A tone-out complete signal restarts the address counter when a count of 62 is reached as represented by the binary count:

0 1 1 1 1 1 0

$$0^0 + 2^1 + 2^2 + 2^3 + 2^4 + 2^5 + 0^6 = 62$$

A -6 volts signal appears on outputs (6) and (56) from the address counter emitter follower 4F4/ZA117-G and R respectively. These outputs drive NOR gate 7E7/ZA312-F in the station selection gates logic which enables this gate and consequently results in a ground signal being applied to the 25-microsecond signal delay 7E8/ZA124-A. The positive delayed signal drives inverter 7E8/ZA302-K. The signal also appears on connector pin JA2-G5. The latter output is applied to the tone-out control logic in order to generate an end of dialing signal. The inverted end of scan signal is used for other control to perform the following functions:

(1) To generate a counter reset pulse.

(2) To set the auto-start flip-flop.

(3) To generate a reset if no stations are connected.

(4) To advance the auto-send control.

(5) To generate a logic reset at the end of an automatically derived call.

(d) When the counter resets to count 63, all the address counter flip-flops are set to the 1 condition except the seventh stage. At count 63, NOR gate 7E7/ZA312-G in the station selection gate logic is enabled, applying a ground signal to power amplifier 7F8/ZA221. The power amplifier output goes to ground and this signal is used to light the COUNTER RESET indicator located on the module A front panel and indicates the counter is in the reset condition. This light is extinguished whenever the address counter is being stepped, and serves as a maintenance guide for determining the condition of the address counter.

D. Preamble Mode

5.92 The following description pertains to operation during the preamble mode when the address counter samples the preamble gates. Six gates are then enabled representing speed, code, error control, punch on/off, go data, and end of preamble. Their respective addresses are listed in Table 4.

(a) When the auto-send control is advanced to the preamble mode, a positive signal is generated which sets flip-flop 4C8/ZA109-A in the address counter to the 1 condition via the set 1A input. This flip-flop unblinds gates 3F4/ZA106-D and F in the address counter control logic and also unblinds the preamble selection NOR gate 7E7/ZA315-A.

(b) The NOR gates at the bottom of sheet 5 of 6545WD comprise the preamble gates: ZA304-A to G, ZA313-E to G and ZA315-A. The outputs of these gates drive NOR gate 5D6/ZA306-A. When a selected gate is sampled, the output of this gate goes from 0 to -6 volts. This negative signal is then applied to inverter 5D7/ZA302-C and a positive preamble sample is generated. This signal is presented to the address counter control logic and remains at 0 volt until the counter is started again by the address counter control. The address counter drive pulses are removed and an address available signal and a read/restore command is generated. The information is read out of the memory, converted, and subsequently toned-out.

(c) After all of the control conditions have been toned-out, NOR gate 5E7/ZA315-A is sampled, representing a count of 82. This gate is enabled, its output goes to ground driving inverter 5E7/ZA302-D. A 0 to -6 volt signal from the inverter defined as end of preamble is forwarded to the address counter control which results in a counter reset pulse. The end of preamble signal is also used to trigger other logic.

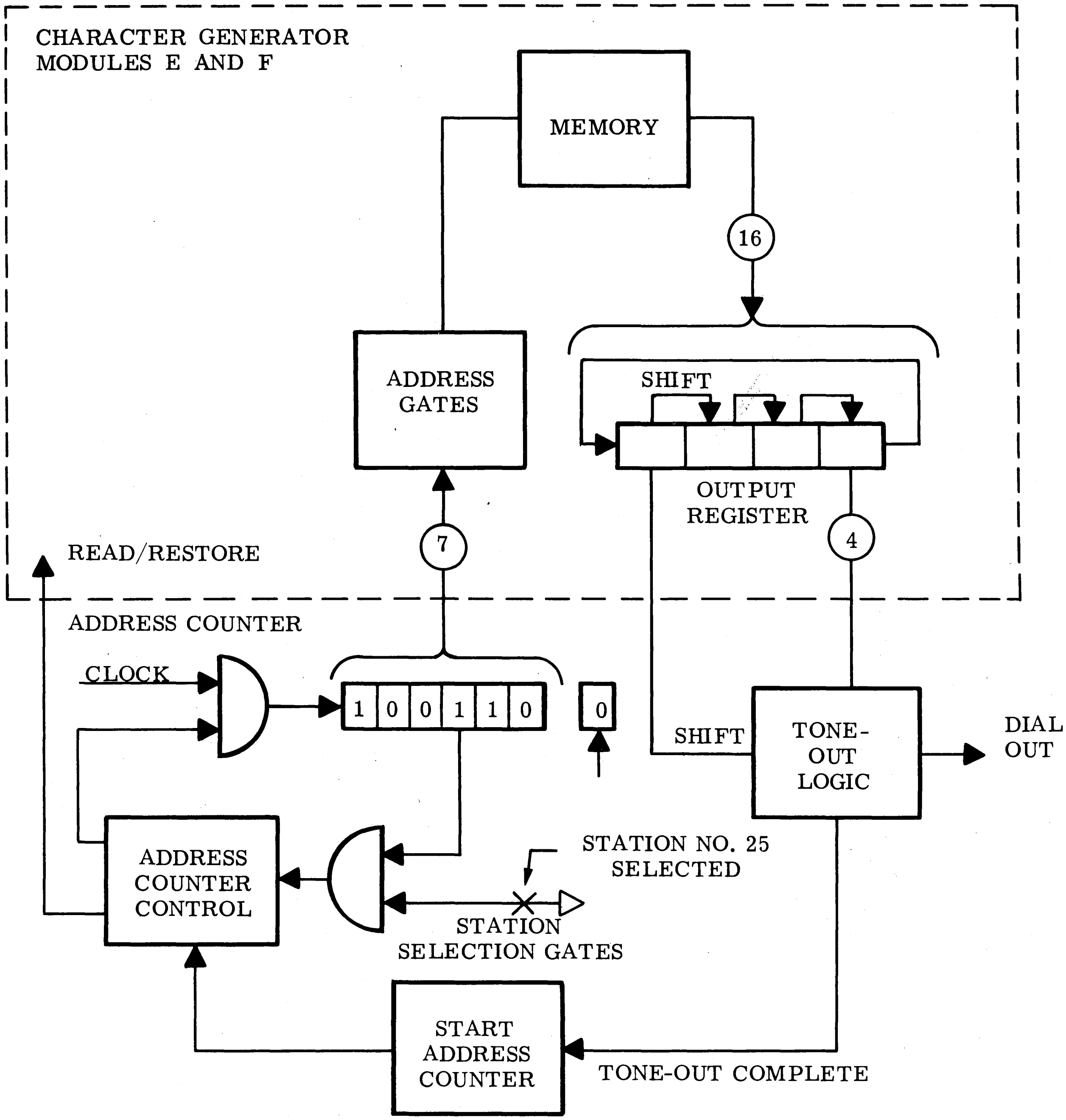


Figure 25 - Dial-Out Logic, Block Diagram

E. Loading of Station Numbers

5.93 The provision made in the logic for loading the station numbers is described in Par. 5.71. The following paragraphs describe how the station selection gates are arranged so that, under normal conditions, only certain station switches can be selected and new station numbers loaded. As stated previously, there are 55 STATION NUMBERS buttons on the control panel representing 55 addresses in the memory where 55 three-digit sequences can be stored. In the first 50 addresses the fixed binary information representing the three-digit number sequences corresponding to those appearing under the STATION NUMBERS buttons are stored. This information can only be changed under certain test conditions. The last five STATION NUMBERS buttons are considered SPARES and are not associated with a fixed repertory. They represent memory addresses 51 through 55. The operator can load any three-digit sequence in memory addresses 51 through 55 using the programmer switch on the control panel. Refer to Figure 21 which is a functional block diagram of the load logic.

(a) The circuit that prevents the operator from loading the first 50 addresses is inhibit gate 7D6/ZA123-K in the station selection gate logic. Refer to schematic 6545WD, sheet 7. The emitter of the gate is driven by the outputs from the first 50 select gates. The base input (34) is driven by the clear/write flip-flop in the address counter control through test switch 7D7/SA18. If, for example, station button 25 is selected and the LOAD button is depressed, the address counter will start and a positive signal will appear on input 33 of inhibit gate 7D6/ZA123-K when the counter reaches a count of 25. This gate is blinded since the normal output of the clear/write flip-flop, 3E6/ZA108-C, drives input 34 of the inhibit gate which is 0 volt at this time; therefore, the gate is inhibited and its output remains at -6 volts and no station sample signal is presented to the address counter control logic. The address counter continues stepping and the no clear/write signal is generated by the address counter control. The counter continues to step until an end of scan signal results in a counter reset pulse applied to the address counter. The output of inhibit gate 7D6/ZA123-K is connected to the output of inverter 7D5/ZA320-K. The latter circuit will go to 0 volt forwarding a station sample signal to the address counter if any of the station select NOR gates 7E4/ZA314-A to G and 7E5/ZA313-B which represent address counts 51 through 55 are enabled. The clear/write flip-flop does not effect a sample signal from inverter 7D5/ZA320-K. The station sample signal remains positive until the LOAD button is depressed again which starts the counter or the counter is reset by pressing the PANEL RESET button.

(b) To facilitate a means of loading the first fifty stations a CLEAR/WRITE switch 7D7/SA18 is located on the front panel of module A. When placed in the ALL ST. (all stations) position, a -6 volt signal is applied to input 34 of inhibit gate 7D6/ZA123-K, opening the gate and disabling the lead from the clear/write flip-flop in the address counter control. Therefore, if any of the first 50 buttons are selected to load numbers and the LOAD button is depressed, the first station selection gate that is enabled will result in a positive station sample signal from the output of inhibit gate 7D6/ZA123-K.

TROUBLE ENCODER DRIVE AND TROUBLE LOGIC (6545WD, Sheet 9)

A. General

5.94 This logic is used during the dial response, RU1, and RU2 modes to direct a trouble sample signal to the appropriate trouble relay, latching up that relay. Latching of the trouble relay will indicate those stations not connected or not responding during the RU1 or RU2 mode by turning the associated STATION NUMBERS button red at the control panel. The trouble relay will also remove this station from subsequent pollings. That is, if a station does not respond during the RU1 mode, it is not polled when the HSSR Set is in the RU2 mode. The station trouble and select relay is described in Par. 5.30. The paragraphs following describe how the trouble relays are latched and the circuitry affected by them.

B. Block Diagram Description

5.95 Figure 26 is a block diagram of the station trouble logic. The address counter is the nucleus of this logic. Its output drives the trouble encoder drive logic. The tone-in logic decodes signals from the Telephone Equipment Cabinet representing the answer-back tones such as station busy, reorder, or out of service. These generate a trouble sample pulse in the dial response mode while the no acknowledge timer generates a trouble sample pulse in RU1 and RU2. The trouble sample pulse is forwarded to the trouble encoder drive logic which in turn is primed by the auto-send control when the set is in the dial response, RU1, or RU2 modes. The trouble sample pulse starts the timing circuit and the input gates are unblinded and signals are subsequently presented to the station trouble encoder, representing the binary input from the address counter.

5.96 The station trouble encoder drive consists basically of power amplifiers and timing circuitry for driving relays in the trouble encoder.

5.97 The trouble encoder is essentially a set of relays (KS1, KS3, KS4, KS5, KS6, KS8) forming a relay tree which is a 6 to 64 binary to decimal converter. A typical relay tree circuit is illustrated in Figure 27 which is arranged to form a 3 to 8 binary to decimal converter. In the figure, a 1 represents a signal which energizes a relay. In the example, a binary count of six is presented to relays A, B, and C resulting in B and C being energized and a sample input signal is directed to output 6.

5.98 Specific relays in the trouble encoder are energized according to the binary input, derived from the address counter. After the relays are energized, a trouble sample signal is forwarded to the station trouble encoder which operates a relay in this logic to generate a sample signal. In the trouble encoder, the sample signal is directed to the station trouble relay related to the address. Therefore, a particular STATION NUMBERS button, and consequently the red trouble lamp, is turned on and the white lamp (selected condition) is turned off under the button. In Figure 24, station button 25 is used as an example. In this case contact S25 would be opened indicating the station button 25 has been selected for dialing. Assuming station 25 is in trouble, a binary count of 25 is then presented on 6 leads to the station trouble encoder and trouble relay (T25) is energized by the sample signal. Therefore, transfer contacts labeled T25 are operated turning on the red lamp under the station button 25 and turning off the white select lamp. The trouble relay also blinds the station selection gate. Other circuits are controlled by the trouble relays as previously described.

5.99 Printout of the station status takes place simultaneously with the operations described above. The address counter remains at a particular count until it is restarted by the address counter.

C. Trouble Encoder Drive Logic

5.100 The following is a detailed description of the trouble encoder drive logic. It is assumed that the station related to button 25 on the control panel is busy and the HSSR Set is in the dial response mode.

5.101 Referring to the trouble encoder drive logic (sheet 9 of 6545WD), input 13 of NOR gate 9B2/ZA119-A is at 0 volt. This signal is derived from the auto-send control indicating the dial response mode. Therefore, the output of this gate is at -6 volts which drives inverter 9C2/ZA320-H. The output of the inverter is used to prime flip-flop 9C2/ZA118-A via the prime 1B input. Initially, all flip-flops are in the set 0 state. In all cases, whether the set is in the dial response or RU modes, the inputs from the address counter are present prior

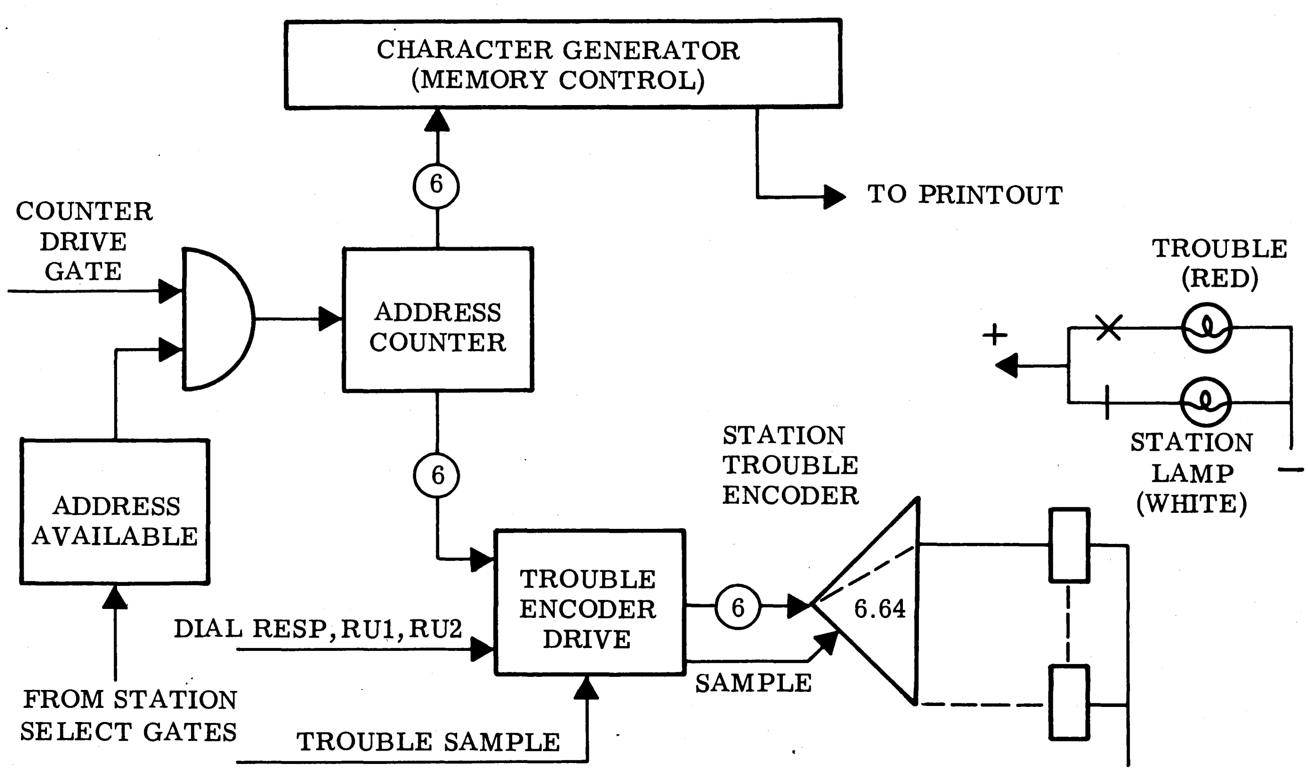
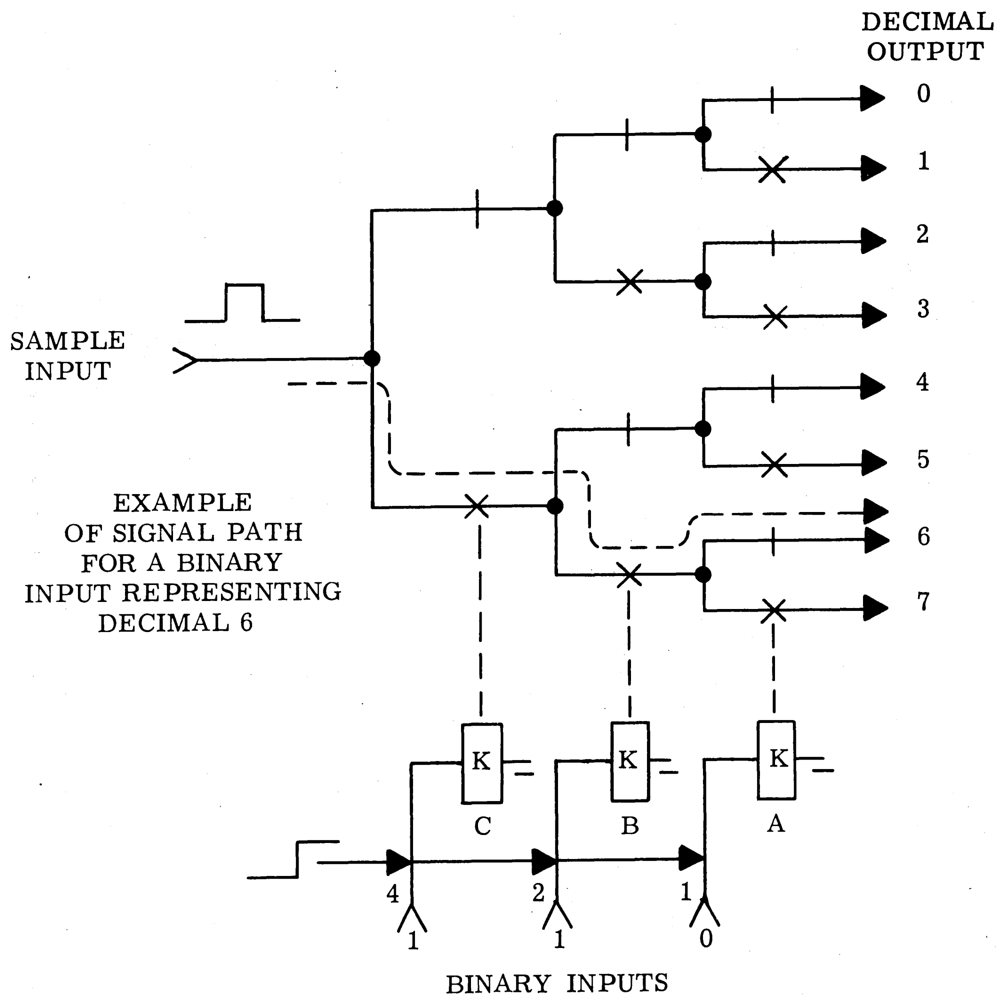


Figure 26 - Station Trouble Logic, Block Diagram



NOTE: A 1 IS DEFINED AS AN ENERGIZED RELAY.

TRUTH TABLE

A	B	C	OUTPUT ON
0	0	0	0
1	0	0	1
0	1	0	2
1	1	0	3
0	0	1	4
1	0	1	5
0	1	1	6
1	1	1	7

EXAMPLE → (0 1 1 6)

Figure 27 - Typical Relay Tree (3:8 Binary to Decimal Converter), Functional Diagram

to the trouble sample pulse. Figure 28 shows the timing of the trouble logic during the dial response mode.

5.102 The inputs defined as 1, 2, 4, 8, 16, and 32 come from the inverted side of the address counter binary stages. A 0 to -6 volt signal on these leads accompanied by a -6 volt signal from inverters 9C3/ZA116-E and F will enable the respective NOR gates 9D4/ZA119-B to G.

5.103 Since the station associated with address counter 25 is busy, leads 1, 8, and 16 from the address counter are at -6 volts. The remaining leads are at 0 volt. An 800-microsecond positive trouble sample pulse is generated upon receipt of a busy tone from the Telephone Equipment Cabinet on the tone-in leads. The BZ signal from the tone logic (module B) is presented to NOR gate 10F1/ZA517-A (6545WD, sheet 10) and passed on to the trouble encoder logic as a trouble sample pulse. Note that in the printout control logic, NOR gate 10F1/ZA517-A is also used for gating the out of service (OS), reorder (RO), and no acknowledge conditions. The trouble sample pulse (-6 to 0 volts, 800 microseconds in duration) is applied to the set 1A input of flip-flop 9C2/ZA118-A which sets it to the 1 condition since it is primed at this time. Its normal output goes to 0 volt and this signal is applied to inverters 9C3/ZA116-E and F, which enable NOR gates 9C4/ZA119-C, D and G. The normal output of the flip-flop applies a ground signal to the gated oscillator 9B4/ZA122 and 30 milliseconds later a positive pulse (10 to 20 microseconds) appears at the output of the gated oscillator which is used to trigger flip-flop 9B5/ZA118-B.

5.104 At this time the outputs of NOR gates 9D4/ZA119-C, D and G go to ground since the input from address counter defined as 32 is at 0 volts. The output of inverter 9D3/ZA123-A is at -6 volts which unblinds inhibit gates 9B6/ZA123-B, D, F, and H. However, only inhibit gates 9B6/ZA123-B, D, and H are enabled since their respective emitters are at 0 volt (these being signals derived from NOR gates 9D4/ZA119-C, D, and G respectively). Therefore 0 volt signals are applied to the power amplifiers 9D6/ZA220-A and B and 9F6/ZA221-A. The outputs of these power amplifiers go from -28 volts to 0 volt and the signals via JA1-H1, H4, and H5 are presented to the trouble encoder logic. As a result, relays K1, K5, and K6 in the trouble encoder are energized. See sheet 6 of 6548WD. Therefore, relay contacts K8-1B, K6-1M, K5-AM, K4-4B, K3-7B, and K2-8M are closed. Relay K9 is momentarily energized by the sample signal. Relay contact K9-8M is closed, thus completing a circuit path from 48 volts to the trouble relay (station 25) located on circuit card 5F3/ZS107, input on pin 7. A trouble relay on this card is energized and latched and the trouble lamp under station button 25 is lighted.

5.105 The sample signal which drives relay K9 also originates in the trouble encoder drive and is delayed to make sure the corresponding relays which direct the sample signal to proper trouble relay are properly energized. Referring to the trouble encoder drive logic (6545WD, sheet 9), when flip-flop 9C2/ZA118-A applies a ground signal to a gated oscillator 9B4/ZA122, 30 milliseconds later a positive pulse is generated by the oscillator which sets flip-flop 9B5/ZA118-B to the 1 condition. The normal output of this flip-flop drives a second gated oscillator 9B6/ZA222. The 0 volt signal starts the oscillator and 30 milliseconds later a positive pulse is generated.

5.106 The normal output of flip-flop 9B5/ZA118-B remains positive for 30 milliseconds and drives power amplifier 9C6/ZA120. Consequently, the output of the power amplifier goes from -28 to 0 volt for 30 milliseconds and energizes the sample relay K9 in the trouble encoder, generating a 48 volt sample signal approximately 30 milliseconds in duration.

5.107 The output of gated oscillator 9B6/ZA222 is used to reset both flip-flops in this logic to the 0 state, and the NOR gates are blinded. The outputs of the power amplifiers go to -28 volts and the relays in the trouble encoder logic are de-energized.

5.108 The same operations occur when the HSSR Set is in the RU1 or RU2 mode. The overall timing is shown in Figure 28.

5.109 Inhibits in the trouble encoder drive serve to reverse the outputs. This reversal occurs on the count of 32 energizing trouble sample relay K8. The +48 volt sample signal from K9-8M is directed through relay contact K8-1M to station trouble relays 33 to 55. With the trouble encoder drive at a count of 32 plus, lead (32) is at -6 volts and the output of inverter 9D3/ZA123-A is ground. If, for example, the (1) lead from the address counter is -6 volts which enables NOR gate 9F4/ZA119-G, inhibit gate 9F5/ZA123-H is blinded and relay K1 is not energized since the output on JA1-H1 remains at -28 volts; however, relay K6 is en-

(DIAL RESPONSE MODE - TWO CONSECUTIVE STATIONS IN TROUBLE)

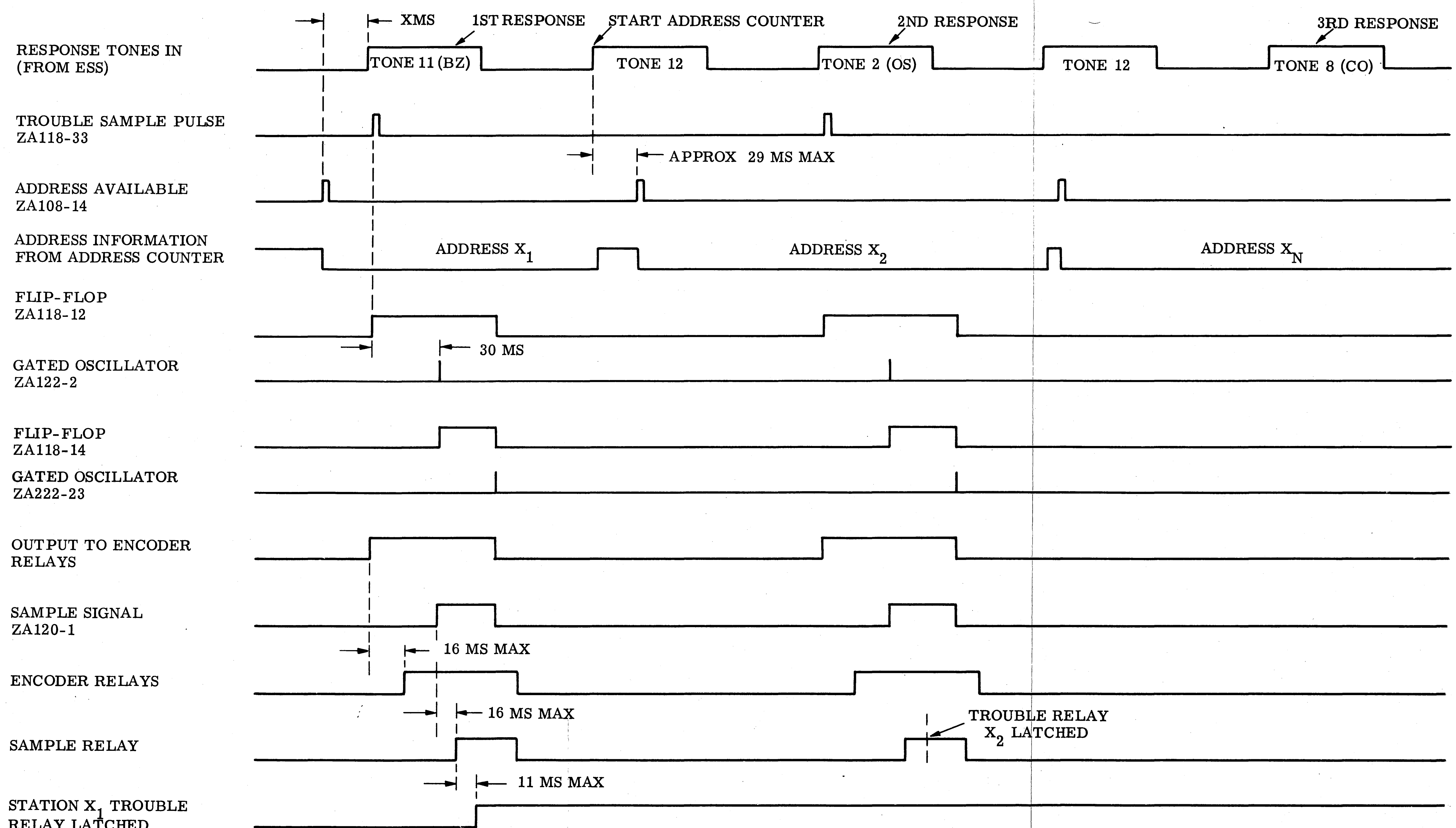


Figure 28 - Trouble Encoder Drive Logic Timing

ergized since the power amplifier 9D6/ZA220-A is turned on as a result of inhibit gate 9D6/ZA123-C being enabled. The inputs from the address counter can be traced to show that (1) goes to (16), (2) goes to (8), (4) goes to (4), (8) goes to (2), and (16) goes to (1).

5.110 Test pushbutton TROUBLE SAMPLE (9C2/SA13) is provided on module A for testing the trouble encoder drive logic, the trouble encoder relays, and the station trouble relays. In a test, the address counter is made to count to the desired address. When flip-flop 9C2/ZA118-A is primed and the TROUBLE SAMPLE button depressed, the operations previously described will occur.

AUTO-SEND CONTROL (6545WD, Sheet 8)

A. General (Figure 12)

5.111 The auto-send control is basically a program counter which controls and indicates the transmitting sequences automatically. The logic consists of a three-stage binary counter which drives a binary to decimal converter (3 to 8) thus providing seven discrete operating modes and a reset (idle) condition.

Normal Sequence

5.112 The normal automatic sequences are as follows:

(a) Reset: Idle condition - automatic send control waits for a negative delay start-dial, 400 microseconds in duration, from module B, and advances the program to the start mode.

(b) Start: Tone-out to Telephone Equipment Cabinet priority and type of call 943 - multi-address, 996 - broadcast. A negative dial numbers signal advances the program.

(c) Dial Numbers: Tone-out all station numbers selected on the control panel. A negative 200-microsecond end of scan signal advances the program counter.

(d) Dial Responses: The dialed stations status are received from the ESS via the tone-in logic. Their respective status is recorded on the control panel and printer page copy. A negative off-hook-in signal advances the program counter to the preamble mode.

(e) Preamble: Tone-out control tones to the receive stations in order to prepare unit. Energize send data control lead. A negative receiver sync complete signal advances program to the RU1 mode.

(f) RU1: Poll all connected stations by sending their respective call numbers via the send data lead and wait for an acknowledge response via the tone-in logic. If a station does not respond, record this condition on the control panel and print station and status on the printer page copy. A negative 200-microsecond end of scan signal advances the auto-send control program counter.

(g) Message: Transmission logic is in control. Start of message and message heading is sent. High speed reader is started and message is transmitted. A negative send RU2 signal derived in the transmission logic advances the auto-send control.

(h) RU2: Poll stations again as in the RU1 mode to determine the status of stations after the message has been transmitted. A 200-microsecond end of scan is gated to generate an auto-call complete signal and the HSSR Set is reset and the set goes to the on-hook (idle) condition.

Broadcast Sequence

5.113 The auto-send sequence varies from the normal sequence during a broadcast call when the sequence advances from the start to the preamble mode, by-passing the dial numbers and dial response modes.

B. Auto-Send Control Detailed Description

5.114 General: The auto-send control logic is located in module A and is schematically shown on sheet 8 of 6545WD. The following is a detailed description of this logic.

5.115 Binary Counter: The binary counter consists of three flip-flops (8B5/ZA321-A, B, and C) which count from 0 to 7 and sequentially control the events previously enumerated during the sending of an automatic call. The flip-flop outputs drive 8 NOR gates (8C4/ZA317-A to G, and 8C2/ZA316-F) arranged in the circuit to form a binary to decimal converter. As the counter advances, only one NOR gate in the converter is enabled representing a specific count. The outputs of these NOR gates, in turn, present various control signals to other logic to prime circuits within the call control.

The outputs of the 8 NOR gates also drive 8 inverters (8E4/ZA319-A to H) and for any given count, only one inverter output is at -6 volts. The remaining inverter outputs are at 0 volt. Therefore, only one of the NOR gates located at the bottom of 6545WD, sheet 8 is unblinded and is enabled upon receipt of a negative (0 to -6 volts) signal on the second input to respective gate. The outputs of the lower gates, specifically NOR gates 8F3/ZA315-E, F, and G, and 8F5/ZA316-A, B, C, and E, are connected together to drive OR gate 8F4/ZA327-E. The output of this gate is fed back to 100-microsecond signal delay 8B3/ZA325-A. The output of the siganl delay in turn drives the first stage of the binary counter. When a particular gate at the bottom of 6545WD, sheet 8, is unblinded and the proper control signal is received, enabling the gate, a delayed positive signal is applied to the first binary stage and the counter is stepped to the next count. The gate is then blinded and the signal is removed. Initially, the auto-send control logic is in the reset condition (count 0).

5.116 Single or Multi-Address Calls: When a single or multi-address call is originated the sequence is as follows:

(a) The auto-start control generates a transmitter auto-start pulse and the HSSR Set goes off-hook. In the auto-send control all flip-flops are set 0 (since the binary counter is in the reset condition). NOR gate 8C2/ZA316-F is enabled since all inputs to this gate are at -6 volts at this time. This represents a count of 0. The 0 volt output of this gate is applied to inverter 8E2/ZA319-H holding it off and unblinding NOR gate 8F2/ZA316-E.

(b) The first signal that the HSSR Set receives after the set goes off-hook is a delay start dial signal (200-millisecond $\pm$50 milliseconds off) from the Telephone Equipment Cabinet. This signal is reshaped in module B (refer to sheet 1 of 6546WD) and a negative delay start dial signal 400 microseconds in duration is received on pin JA2-F8 and is presented to NOR gate 8F2/ZA316-E. This gate is enabled and a -6 to 0 volt signal is applied to OR gate 8F4/ZA327-E. The output of the OR gate goes positive and a positive signal is applied to 100-microsecond signal delay 8B3/ZA325-A. The positive delayed output of the signal delay drives the first counter stage 8B4/ZA321-A and the counter advances to a count of 1, inhibiting NOR gate 8C2/ZA316-F. As a result, NOR gate 8F2/ZA316-E is inhibited and the positive signal is removed from the input of the signal delay. The result is a 100-microsecond positive pulse appearing on the input of the signal delay every time the program counter is advanced. Each time a 100-microsecond pulse is generated, the delayed signal is applied to the start address counter logic at delay start scan flip-flop 2C3/ZA525-A.

(c) At the count of 1, which is the start mode, NOR gate 8C3/ZA317-A is enabled providing a positive priming signal to logic in module B. This signal is also used to drive a power amplifier in module B (9B3/ZB325-A) which in turn drives the start transmitter sequence indicator on the control panel to indicate the set is in the start mode. The inverted output is used to unblind the appropriate gates in the address counter control logic and also to unblind NOR gate 8F2/ZA315-E to prepare this gate for the next signal (a negative dial numbers signal 200 microseconds in duration originating in the auto-start control). The NOR gate 8F2/ZA315-E is enabled and a 100-microsecond positive signal is generated again. The binary counter then is advanced to count 2. At the count of 2 NOR gate 8F3/ZA315-F is primed, the transmitter sequence indicates dial numbers mode, and when the address counter reaches the end of scan, the auto-send control steps to the dial response mode. The address counter is started and stops at the first selected station number address and waits for the station status response via the tone-in logic. The auto-send control is advanced each time the appropriate control signal is received.

(d) These signals are applied to NOR gates 8F3/ZA315-E, F, G, and 8F5/ZA136-A, B, C, D, and E.

(e) NOR gate 8F6/ZA316-D is primed at a count of 7 (when the set is in the RU2 mode). After all the stations have been polled in the RU2 mode, an end of scan signal is generated when the address counter samples the associated selection gate 7E7/ZA312-F. This negative end of scan signal, which is 200 microseconds in duration, is applied to NOR gate 8F6/ZA316-D which enables this gate. A positive signal defined as auto-call complete is generated and applied to NOR gate 2B6/ZA318-F, located in the start address counter control logic (6545WD, sheet 2). A reset A pulse is presented to the delay disconnect logic located in module B via connector pin JA2-G8. Approximately 500 milliseconds later a logic reset pulse is applied to all logic and the HSSR Set goes back on-hook and the automatic call is completed.

5.117 Broadcast Calls: If a broadcast call is originated, the auto-send control logic is arranged so that certain operating modes are by-passed. This is accomplished by inhibit gate 8A5/ZA320-D, inverter 8B7/ZA319-K, and NOR gate 8B7/ZA316-G.

(a) When the HSSR Set is used to originate a single or multi-address call, inhibit gate 8A5/ZA320-D is normally enabled when the second counter stage, flip-flop 8B5/ZA321-B is in the set 0 condition. This counter element is being primed on P1B through this inhibit gate. Input 14 to the inhibit is at -6 volts since NOR gate 8B7/ZA316-G is blinded by a ground signal from the NC contacts of the broadcast relay located in the relay rack. Therefore, the binary counter counts in the normal manner.

(b) However, in a broadcast call, the transmitting sequence advances from the start to the preamble mode. This is accomplished by unblinding NOR gate 8B7/ZA316-G. The ground signal from the NC contact of the broadcast relay is removed from this gate since the broadcast relay is energized.

(c) In this case the delay start dial signal from the Telephone Equipment Cabinet advances the auto-send control to the start mode and NOR gate 8D3/ZA317-A is enabled. The 0 volt signal from the NOR gate is applied to inverter 8B7/ZA319-K. A -6 volt signal from the inverter is presented to the input of NOR gate 8B7/ZA316-G. Input 2 of the gate (-6 volts) is a signal derived from the normal output of the third stage in the counter. Therefore NOR gate 8B7/ZA316-G is enabled, its output goes to ground to blind inhibit gate 8A5/ZA320-D and at the same time prime the P1A input of the third element of the counter. The output of the inhibit gate goes to -6 volts and the P1B input of the second binary element is no longer primed. The auto-send control is now ready to receive the next signal (dial numbers) from the auto-start control.

(d) The negative dial numbers signal enables NOR gate 8F3/ZA315-E, resulting in a positive signal on the output of OR gate 8F4/ZA327-E. Consequently, a delayed positive pulse from the output of signal delay ZA325-A is applied to the set 1B and 0B inputs of flip-flop 8B4/ZA321-A, resetting this flip-flop to the 0 state. The positive pulse from the signal delay is also presented to the set 1A input of flip-flop 8B6/ZA321-C. Since the P1A input of this flip-flop is at 0 volt, it is set to the 1 state forcing the binary counter to a count of 4. At this count, NOR gate 8C4/ZA317-D is enabled and the auto-send control is in the preamble mode. When flip-flop 8B6/ZA321-C was triggered, its normal output blinded NOR gate 8B7/ZA316-G which removed the prime signal on the P1A input of flip-flop 8B6/ZA321-C. It also enables inhibit gate 8B5/ZA320-D by applying a -6 volt signal to input 14. The auto-send control waits for the next signal (receiver in sync). This signal advances the binary counter to a count of 5 which represents the RU1 mode. When the auto-send control receives the appropriate signals, the counter advances to counts 6, 7, and 0 which are the message, RU2, and reset conditions respectively.

5.118 Test Features: Since the auto-send logic controls several gates in other logic blocks a means is provided to manually advance the sequence counter to the desired operating mode to facilitate testing the call control and other logic. This is accomplished by depressing TRANS PROG. ADVANCE pushbutton (8B2/SA5) located on the module A front panel. The TRANSMIT OPERATING SEQUENCE indicators on the control panel serve as a guide to set up the desired operating mode.

RESPONSE PRINTOUT CONTROL AND PRINTOUT CONVERTER LOGIC (6545WD, Sheets 10 and 11)

A. General

5.119 The response printout control and printout converter logic, located in module A, operates with the character generator and transmission logic to provide the following functions:

(a) It controls the printing of the three-digit station numbers and their respective status in a specified format at the originating station.

(b) It controls the sending of the three-digit number sequences comprising the station RU's from the originating station during the RU1 and RU2 querying. It also controls the printing of these numbers with their respective status on the page copy.

(c) During the off-line loading of a station number, it controls the printing of the station number that was loaded in the memory.

(d) During certain test conditions, the logic controls the printing of the station number repertory to check that the proper station numbers have been loaded in the memory.

B. Block Diagram Description

5.120 The response printout control and printout converter and their important inputs and outputs are illustrated in the block diagram, Figure 29. Figures 30 and 31 show the related logic used in the printout function during the dial response and RU modes.

(a) The response printout control logic consists of a three-stage binary counter used for controlling the sequence of sampling the ASCII converter, a binary to decimal converter, a two-stage binary counter to column space the printer, a timing circuit that is activated in the RU mode, and necessary gates for controlling the logic.

(b) The printout converter consists of a set of status flip-flops (buffers) for storing the individual status conditions throughout the printout cycle and a set of gates arranged to form an ASCII converter.

Incoming Signals

5.121 The main signals to the printout logic (response printout control and converter) and their functions are as follows:

(a) Character Clock - Originates within the transmission logic and is a negative signal one bit wide which coincides with the 9th bit of the serial data transmitted. It provides the proper timing between the transmission logic and the printout logic and is used to advance the printout sequence binary counter for character sampling. The clock signals are present at all times when the set is in the send condition.

(b) 2kc Clock - Derived from the address counter control logic for the purpose of driving the column advance counter and supplying square wave column pulses to the character generator logic.

(c) Tone-In - These signals (800 microseconds wide) are derived from the tone-in logic and indicate the status of the dialed stations. The signals are used to set the status flip-flops in the printout converter and also to activate the printout logic. The various tones indicating station status and the abbreviated character sequences printed on the page copy are listed below.

Tone	Station Status	Status Abbreviated Form
2	Out of Service	OS
5	Reorder	RO
8	Connected	CO
11	Busy	BZ
6	Acknowledge	AK
Local time-out	No Acknowledge	NA

(d) Address Available Signal (INV) - A positive signal derived in the address counter control logic and used to initiate the sending of the station RU.

(e) Memory Information - Four inputs originating from the character generator (memory control) output buffer. The signals actually come from the tone-out converter logic and represent the binary information read out of the memory. In this case, the information represents station number digits. The signals are presented to the printout converter with a negative signal indicating a marking condition and a positive signal indicating spacing condition.

Outgoing Signals

5.122 The main signals from the printout logic are as follows:

(a) Character Available - A negative signal to the transmission logic, from the printout control, requesting that the parallel data from the converter be sampled by the serializer. The character available signal remains negative throughout the printout cycle and when removed the transmission serializer reverts back to sending delete characters.

(b) Parallel Data - Seven parallel signals from the printout character generator are presented to the transmission logic serializer. The signals are defined as levels 1 through 7. A 0 volt signal indicates a

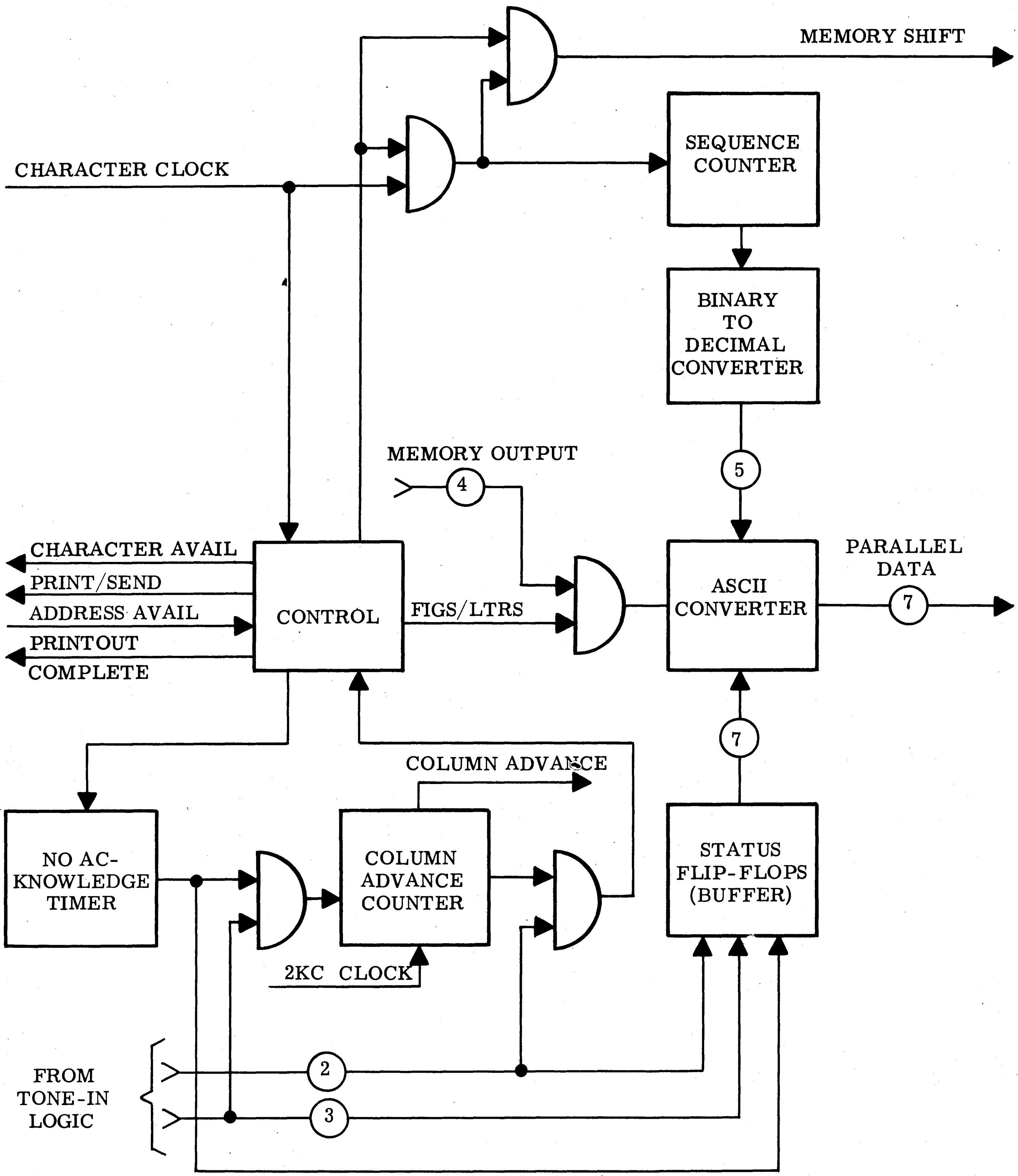


Figure 29 - Printout Control Logic, Block Diagram

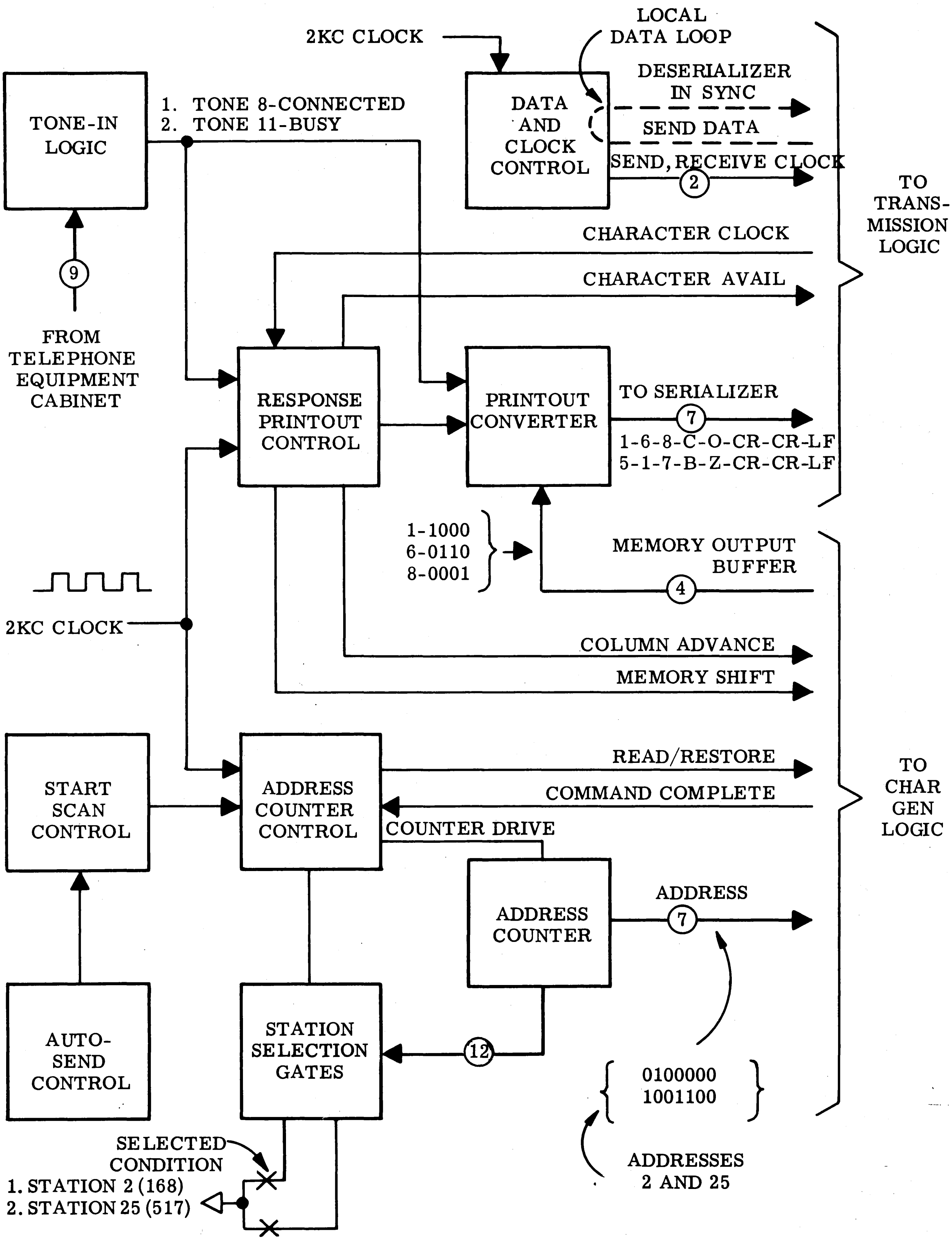


Figure 30 - Station Response Printout Logic, Block Diagram

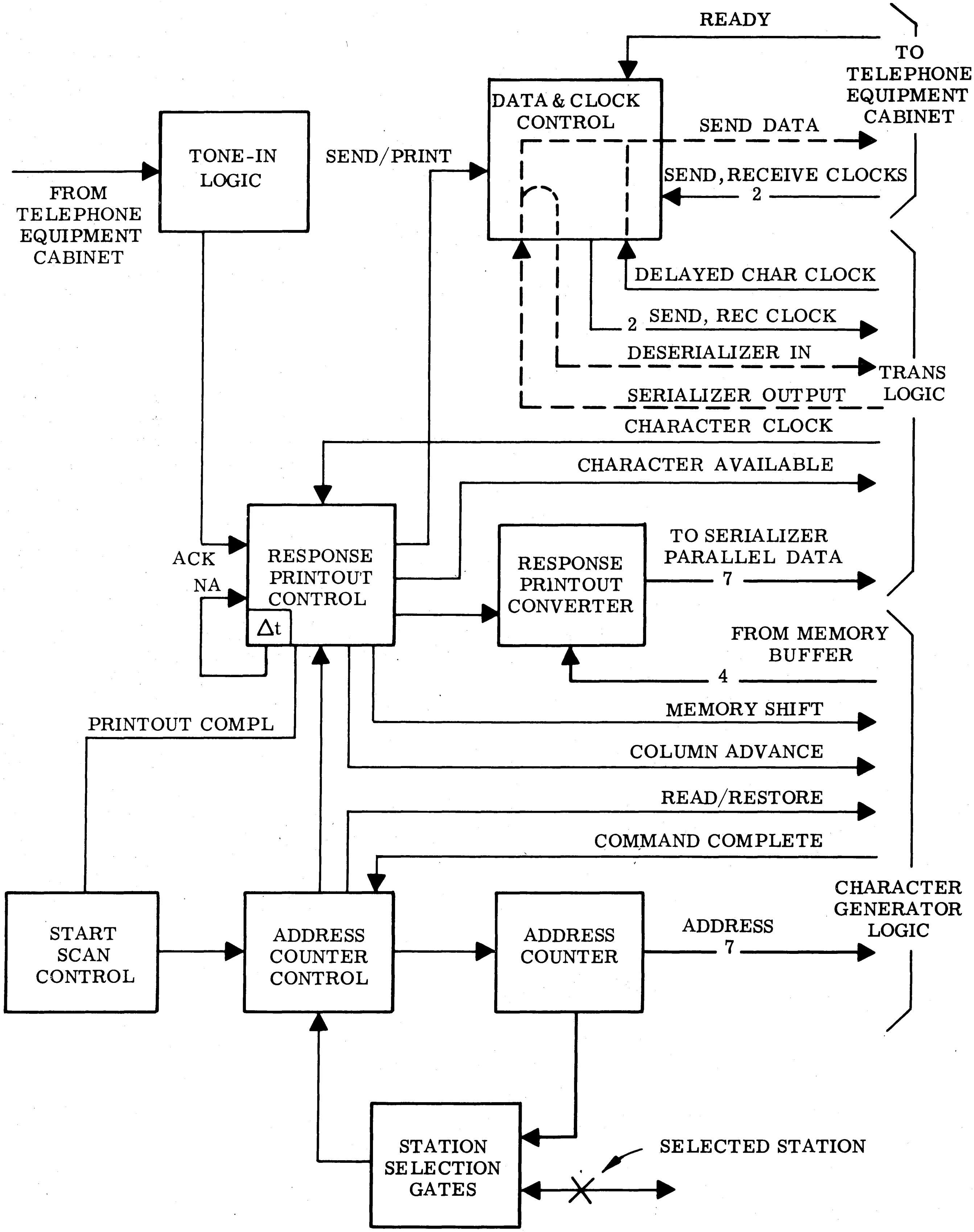


Figure 31 - Dial Response Printout Logic (RU1, RU2 Modes), Block Diagram

marking condition, and a -6 volt signal a spacing condition. These signals are used to prime gates in the transmission logic serializer which are subsequently sampled.

(c) Memory Shift - Negative signals, 100 microseconds in duration, coinciding with sequence counter drive pulses and presented to the character generator logic to shift the character generator output register so that the next set of binary information can be presented to the printout logic. The register is shifted four bits at a time and four shift pulses are presented to the character generator logic.

(d) Column Advance - Square wave signals presented at a 2kc rate to the character generator logic to column space the printer. Four column advance pulses are generated and the printer is column spaced 8 character spaces.

(e) Print/Send - A positive signal to the call control data and clock control logic which blinds the local deserializer input and unblinds the send data output to permit the sending of the station RU.

(f) Trouble Sample Pulse - A positive signal 800 microseconds in duration presented to the call control trouble encoder drive logic and activating this logic.

(g) Printout Complete - A positive signal presented to the start address counter control logic which triggers the delay start scan circuit when in the RU mode so that the address counter can proceed to the next selected station gate after printout has been completed.

Dial Response Mode (Figure 32)

5.123 Overview: The following is a concise explanation of printout logic operation when it is activated during the dial response mode.

(a) After the HSSR Set has dialed the stations automatically, it waits for the ESS to connect the stations and to forward information concerning the dialed staion(s) status. The ESS generates tones representing the station status and delivers this information to the send terminal Telephone Equipment Cabinet when the tone receiver converts the tones to dc levels and presents this information to the HSSR Set on the tone-in leads. The responses for the dialed stations are returned in the same order as the dialing operation, the first response indicating the status of the first station dialed, the second response the status of the second station, and so on. The received tones indicate a station trouble condition or the station connected condition. The respective tone sets the proper status flip-flop in the printout converter and also initiates the printout sequence. If a station trouble tone is received, the printer is column spaced 8 characters from the left-hand margin prior to printing out the station number and status. Thus, the page copy takes this form: all stations connected are printed on the left-hand margin; those stations not connected are printed-out beginning 8 column spaces from the left-hand margin.

(b) During this time, the HSSR Set has advanced to the dial response mode and the address counter has advanced to the first selected station gate. The information comprising the station's call number appears in the character generator output register. The four information bits presented to the printout converter represents the first digit of the 3-digit combination. This information is converted to form an ASCII character and is forwarded to the transmission logic serializer over the parallel data outputs. The serializer samples the data and transmits it via the serial data output lead to the local deserializer. The data is subsequently printed on the page copy at a rate of 2000 wpm. There are 8 characters in the printing format. For example:

.68-C-O-CR-CR-LF

- CR-CR-LF — Fixed Characters - Carriage Return, Carriage Return, Line Feed
- C-O — Status
- 68 — Station No.

(c) The printout is completed in approximately 40 milliseconds at which time the character available signal to the transmission logic is removed and delete characters are transmitted to the local deserializer to maintain synchronization between the serializer and deserializer.

(d) After the response tone (50 milliseconds), a tone 12 is received from the ESS via the Telephone Equipment Cabinet which starts the address counter and advances it to the

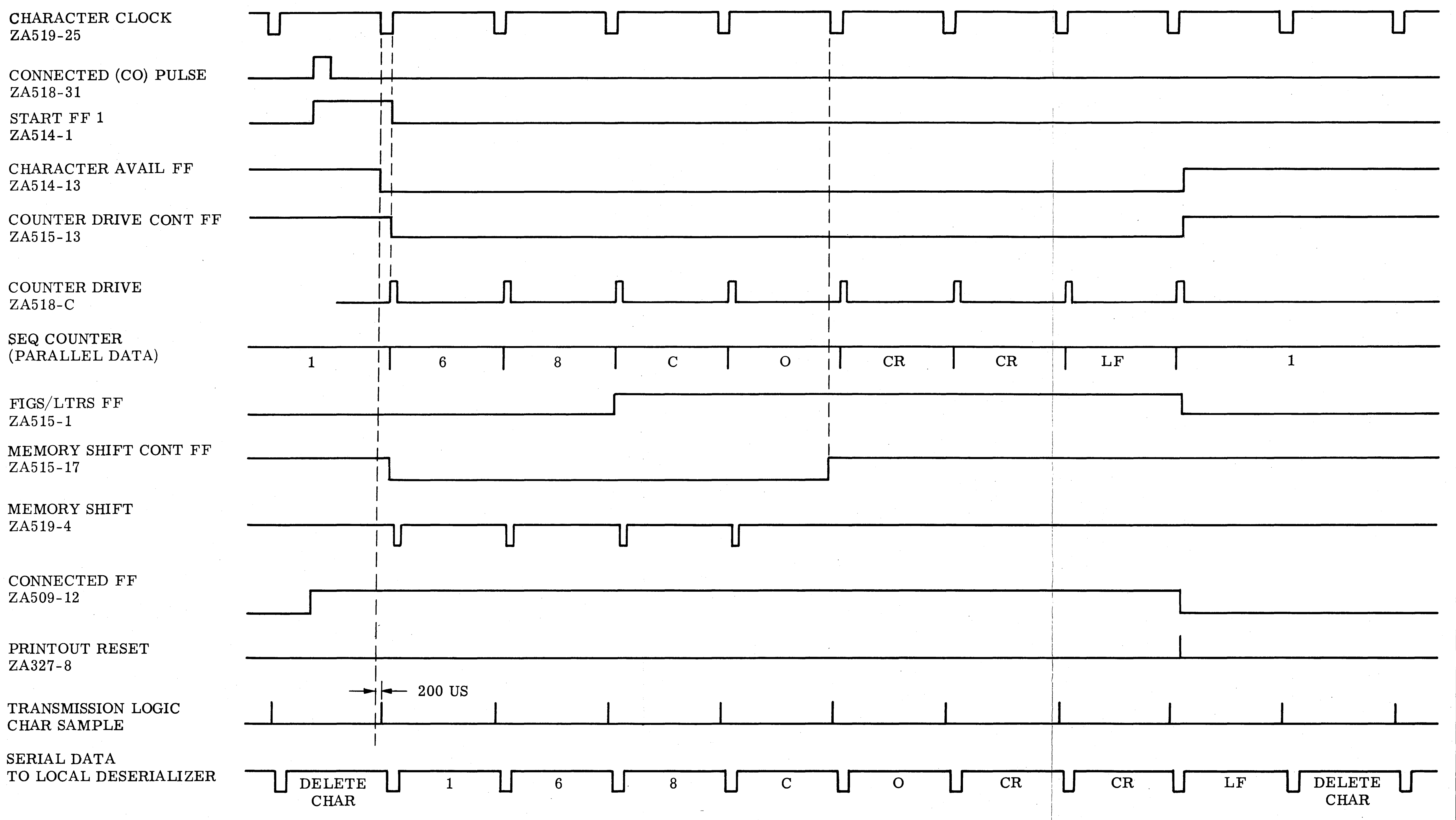


Figure 32 - Printout Control Logic Timing
(Dial Response Mode)

next selected station number gate. It then waits for the response tone indicating the status of this station. When the signal is received via the tone-in leads the cycle is repeated. For each station dialed, a response is received. Figure 32 is the overall timing diagram of printout logic during the dial response mode.

C. Printout Logic - Dial Response Mode

5.124 In the following detailed circuit description of the printout logic it is assumed that the send set is in the dial response mode and that station button 1 has been selected which corresponds to call number 168. The station connected condition is considered first, followed by the busy condition. Figures 33 and 34 are detailed timing diagrams of the printout logic. Refer also to 6545WD, sheets 10 and 11.

Station Connected Sequence

5.125 Initially, all flip-flops in the printout logic are in the set 0 condition. As previously described, when the auto-send control advances to the dial response mode, the delay start scan circuit is triggered and the address counter advances to the first station select gate. At the same time, input 11 of OR gate 11D2/ZA327-C in the printout control logic goes to 0 volts. This signal is derived from the auto-send control. Consequently, a 0 volt signal is applied to the P1A input of the start 1 flip-flop 10D3/ZA514-C.

5.126 The printout logic is started upon receipt of a connected signal from the tone-in logic located in module B. This signal representing the status of station 168 is a positive pulse 800 microseconds in duration appearing on JA2-D6. The positive pulse sets the status flip-flop in the printout converter identified as connected (11B1/ZA509-A) to the 1 condition. All the status flip-flops are primed at this time on the P1A input by the auto-start flip-flop. When the connected flip-flop is triggered, its inverted output goes to -6 volts unblinding NOR gates 11B3/ZA504-B and C and prepares these gates for future sampling by the printout sequence counter when binary counts 3 and 4 are reached. The positive connected signal is also applied to NOR gate 10E2/ZA518-F in the printout control logic. The output of this NOR gate goes negative for the duration of the signal and in turn drives inverter 10E2/ZA519-J. The result is a positive signal coupled through OR gate 10E3/ZA327-B to the set 1A input of the start 1 flip-flop. This flip-flop is triggered to the set 1 condition, priming the P1A input of flip-flop 10B2/ZA514-A.

5.127 In the meantime, the address counter has sampled the first selected gate and an address available signal and a read/restore command have been generated. The data in memory address 1 is read out of the memory and stored in the character generator output register. In this case, digits 1680 are stored in the register comprising 16 bits of information. The digit 0 is not sampled by the call control logic. At this time, four bits of binary information representing digit 1 is applied to NOR gates 11D8/ZA506-B, C, D, and E via inputs on JA2, B9, 8, 7, and 6 respectively. These signals are defined as P1 through P4. They are actually derived from a set of emitter followers in the tone converter logic (sheet 3 of 6546WD) since the tone-out logic utilizes the same inputs from the character generator output register for toning out control and station numbers signals during other operating modes. A 0 volt signal from the emitter followers represents a spacing condition and a -6 volt signal a marking condition. Since the first digit is 1, all inputs to the printout converter (NOR gates) are at 0 volt with the exception of the input on JA2-B6 which is at -6 volts. This signal enables NOR 11D8/ZA506-E gate, presenting a marking signal on level 1 to the transmission logic serializer. This signal remains in this condition until a shift pulse is applied to the character generator output register.

5.128 The first inverted character clock pulse applied to the set 1A input of the character available flip-flop after it has been primed by the start 1 flip-flop triggers this flip-flop to the set condition. A -6 volt signal from the inverted output of the character available flip-flop is presented to the transmission logic indicating a character available. The normal output of this circuit primes flip-flop 10C3/ZA515-A via the P1B input. The delayed character clock will then set flip-flop 10C3/ZA515-A, via the set 1B input, to the 1 state; unblinding NOR gate 10C4/ZA518-C. This action allows the counter drive pulses, formed by the positive transition of the character clock (trailing edge) and signal delay 10A3/ZA521-A, to advance the sequence counter consisting of flip-flops 10C5/ZA511-A to C.

5.129 When the transmission logic receives a character available signal (-6 volts) from the printout control logic, it samples the information on the 7 parallel data leads from the printout converter after a delay of approximately 200 microseconds. This signal is identified as the character sample on timing diagram shown in Figure 32. The input data is subsequently transmitted in serial data form and the signals appear on the serial data lead of the call control data and clock control logic. See sheet 8 of 6546WD. In the data and clock control logic the serial data is directed to the local deserializer. Therefore, the digit 1 is printed on the local page copy.

5.130 The next event that takes place in the printout control logic is to shift the sequence counter to a binary count of 1 and simultaneously shift the character generator output register so the next digit can be sampled by the transmission logic serializer (module C). This is accomplished when the character clock signal goes positive. The inverted character clock signal along with the normal clock signal delayed 100 microseconds by signal delay 10A2/ZA521-A is then applied to NOR gate 10C4/ZA518-C. A 100-microsecond pulse is applied to set 1 and 0 inputs of the first binary stage in the sequence counter 10C5/ZA511-A. The counter advances to a binary count of one and simultaneously the memory shift control flip-flop is triggered to the set 1 condition as inverter 10B6/ZA519-D goes positive. The inverted output of the memory shift control flip-flop goes to -6 volts and this signal combined with a inverted counter drive pulses enabled NOR gate 10B7/ZA518-E. This NOR gate drives inverter 10A8/ZA519-A and a negative memory shift pulse is presented to the character generator via pin JA2-B4. Note that NOR gate 10A7/ZA518-D is blinded at this time. The latter circuit is utilized to present memory shift pulses when the tone-out control logic is activated. The character generator output buffer is shifted and four new bits of information appear on inputs P1 to P4. In this example, digit 6 is presented; therefore inputs P2 and P3 are at -6 volts and P1 and P4 are at 0 volt. These signals enable NOR gates 11D8/ZA506-C and D. Consequently, levels 2 and 3 along with 5 and 6 are marking, representing the digit 6 in ASCII parallel code. The information is sampled 200 microseconds after the next character clock signal. The first counter drive pulse is used to reset the start 1 flip-flop. At a binary count of two the last digit is sampled by the transmission logic.

5.131 The next counter drive pulse advances the printout counter to a count of three which enables NOR gate 10D7/ZA517-B. A 0 volt signal from this gate triggers the figs/ltrs flip-flop 10C8/ZA515-C to the set 1 state. Also, the 0 volt signal is presented on lead X3. The figs/ltrs flip-flop in turn blinds the four NOR gates 11D8/ZA506-B to E accepting the information from the character generator logic and also switches output levels 5 and 6 to the transmission logic to the spacing condition. The 0 volt signal on lead X3 drives two inverters in the printout converter logic, 11B2/ZA508-B and D. These inverters in turn enabled certain NOR gates so that bits indicating alphabetical characters are formed. In this case, the character C, the first character of the abbreviated status condition, is presented. As previously stated, the connected flip-flop is in the set 1 condition; therefore NOR gate 11B3/ZA504-B is enabled. Its output is applied to a set of OR gates arranged to form an ASCII alpha converter. Consequently, inputs 11 and 22 of OR gates 11C6/ZA502-C and B go to ground and the outputs of these respective gates also go to ground. As a result, levels 1 and 2 go to the marking condition. Level 7 is forced in the marking condition by the 0 volt signal on lead X3 which in turn inhibits NOR gate 11A4/ZA507-A. The parallel data representing character C is sampled by the transmission logic, and subsequently transmitted and printed on the page copy.

5.132 When the sequence counter is shifted to a count of four, NOR gate 10D7/ZA517-C is enabled priming the P0B of the memory shift control flip-flop and also applying a 0 volt signal on lead X4. The signal on lead X4 enables NOR gate 11C3/ZA508-C in the converter and the character O is presented on the parallel leads to the serializer in module C.

5.133 The next character clock pulse resets memory shift control flip-flop to the 0 condition prior to the next sequence counter advance pulse; therefore, the character generator output register is shifted only four times. The counter is advanced by each character clock pulse. NOR gates 10E7/ZA517-D, E and F provide 0 volt signals on leads X5, X6, and X7 which are used as drive gates in the printout converter forcing carriage return and line feed characters on the output of the converter.

5.134 When the eighth counter drive pulse is applied to the sequence counter, NOR gate 10D7/ZA517-G is enabled and a positive signal is applied to the P1B input of the memory shift control flip-flop priming this circuit for the next printout cycle. The positive transition is also applied to signal delay 10B3/ZA521-B. Fifty microseconds later the character available flip-flop, 10B2/ZA514-A is reset to the 0 state

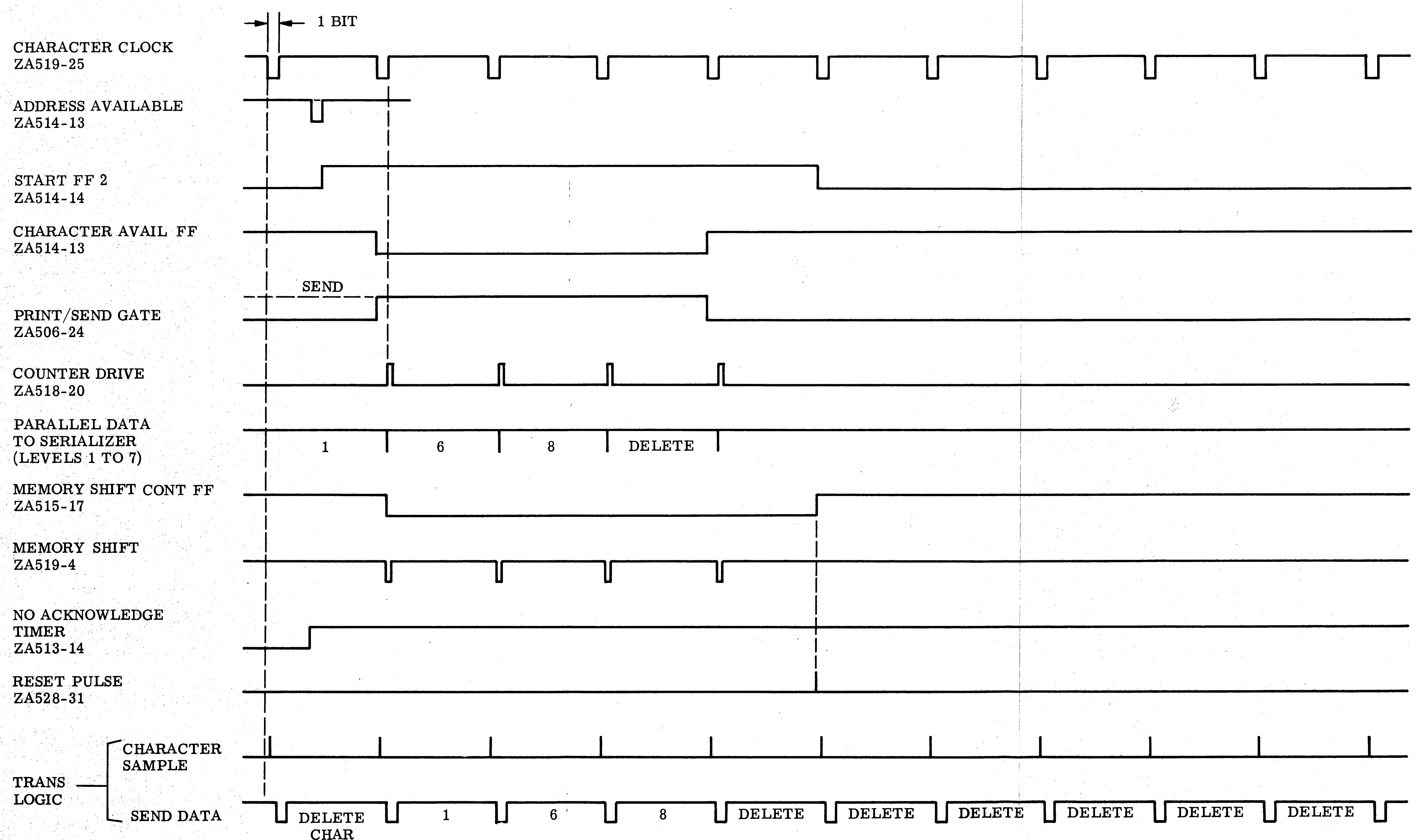


Figure 33 - Printout Control Logic Timing
(Send Station RU)

along with flip-flop 10C3/ZA515-A. The latter flip-flop blinds the NOR gate 10C4/ZA518-C to inhibit the character clock signals from advancing the sequence counter. When the character available signal is removed, 0 volt appears on connector pin JA2-C8 and the transmission logic no longer samples the parallel information presented by the call control printout converter but instead reverts to transmitting delete characters.

5.135 When flip-flop 10C3/ZA515-A is reset, the inverted output goes to 0 volt, driving power pulser 10C4/ZA528-A. A positive pulse is generated by the power pulser which is used to reset all flip-flops in the response printout control and printout converter logic. In this case the connected flip-flop is reset to the 0 condition and the logic is restored to its normal state and waiting for the next response.

Station Busy Printout Sequence (Figure 34)

5.136 The following paragraphs describe a station busy printout sequence.

(a) If a busy tone was received instead of a connected tone for station 168, the events previously described will take place but with a significant difference. Since the busy condition indicates the station is not going to receive the message, the printer must be column-spaced prior to printing out the station call number and its status. Refer to Figure 34 for the column spacing logic timing.

(b) In this case, the 800-microsecond positive BZ pulse is received from the tone-in logic and applied to NOR gate 10F1/ZA517-A. The output of this NOR gate goes negative which drives inverter 10F2/ZA520-A. The inverter output in turn applies a positive trouble sample pulse to the trouble encoder drive logic. This signal also primes flip-flop 10F2/ZA513-A for 800 microseconds via the P1A input. In the meantime, 2kc clock pulses are being applied to the set 1A input of this flip-flop. The first positive pulse that appears on the set 1A input after this flip-flop is primed sets the flip-flop to the 1 condition unblinding NOR gate 10F3/ZA518-G. The NOR gate is enabled when the 2kc clock signal goes negative. Input 2 to the NOR gate is also negative at this time. This results in a positive pulse 250 microseconds in duration on the output of this gate which drives flip-flop 10F4/ZA512-A which is the first element in a two-stage counter. The positive pulses are also used for the purpose of advancing the printer. Each positive pulse, presented to the character generator, column advances the printer two column spaces.

(c) When a count of four is reached, flip-flop output 10F4/ZA512-17 goes to 0 volt which triggers flip-flop 10F5/ZA512-C to the set 1 condition. The positive signal from 10F5/ZA512-1 drives the 200-microsecond signal delay 10E5/ZA522-A and also inhibit gate 10D4/ZA519-K. The inhibit is enabled for 200 microseconds since input 34 remains a -6 volts until the output from signal delay goes positive. The positive pulse from the inhibit gate is applied to OR gate 10E3/ZA327-B and consequently start 1 flip-flop is triggered to the set 1 condition and the printout sequence is started. The positive delayed signal from signal delay also blinds NOR gate 10F3/ZA518-G and resets flip-flop 10E2/ZA513-A to the 0 condition. The last column advance pulse to the character generator logic is 200 microseconds in duration.

(d) The printer is column advanced 8 spaces prior to printing out the station status whereby the printout sequence is the same as that previously described. The printout logic is reset when printout is completed. Fan-out gates ZA326-B and ZA326-C provide isolation and are for collector reset.

D. Printout Logic - RU Modes (Figure 33)

Overview

5.137 The paragraphs following describe what occurs in the printout logic when the HSSR Set is in the RU1 or RU2 operating modes.

(a) During the RU1 or RU2 modes, the operation of the printout logic is significantly different. In this case, the logic is activated twice for each selected station, once for sending the station RU (its three-digit call number) and a second time to print out the respective station's status. The sending and printout occur at the bit rate selected by the operator when the call was originated, namely: 2400, 1200, or 600 bits per second.

(b) The send unit queries the connected stations during the RU1 mode for two purposes. It checks and records all the stations that were originally dialed and connected in order to determine whether the intended receive station units have or have not been properly synchronized. Also, it checks and eliminates those receive stations which are

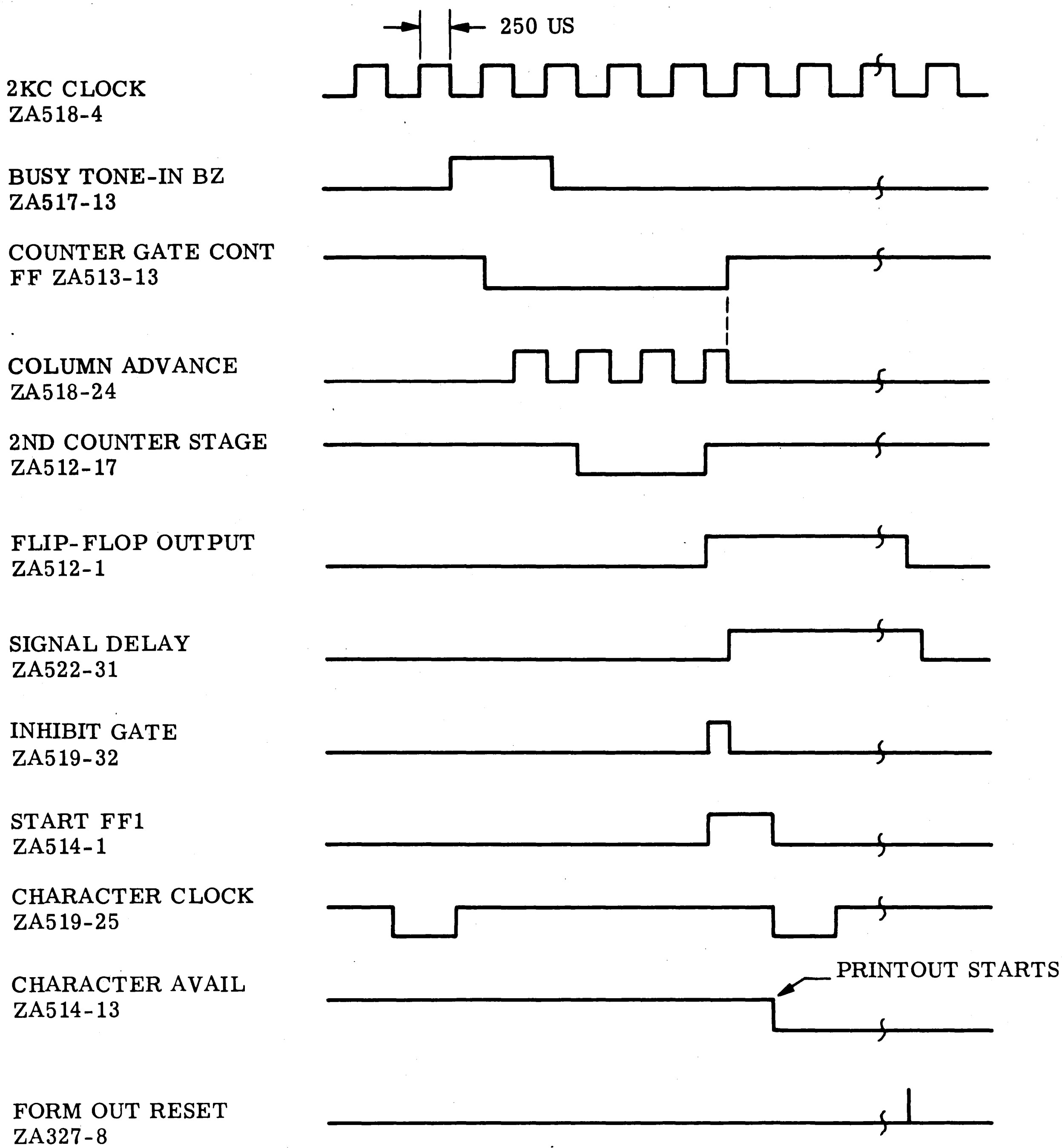


Figure 34 - Printout Control Logic Timing (Column Spacing, Busy, Tone Receiver)

falsely connected. A local timing circuit called the no acknowledge circuit is provided in the printout control logic. Since a receive station that is not synchronized has no means of recognizing its RU and therefore cannot respond to the send station, this timing circuit generates a no acknowledge signal if an acknowledge response is not received within a specified timing interval (500 milliseconds). The timing cycle takes into account transmission delays in sending the station RU and receiving a response from a receive station.

(c) The printout logic is activated by the inverted address available signal from the address counter control. Prior to this signal, the local deserializer is receiving delete characters from the transmission logic serializer via the serial data output. Also, delete characters are being forced on the outgoing line via the send data lead to all the receive stations. The address available inverted signal triggers the printout control logic so that the print/send lead goes to the send condition, thereby blinding the local deserializer and unblinding the send data output. The binary information appearing in the character generator output register (memory information) is sampled and transmitted as the station RU. Simultaneously, the no acknowledge timing circuit in the printout control is started. The three characters comprising the station number (RU) are transmitted, after which the sequence counter is reset. The printout logic waits for an acknowledge signal (tone 6) which is generated at the receive HSSR Set after the station has recognized its RU. When the acknowledge signal is received, the printout logic is triggered again, and the station number, along with its status, is printed out. During this operation the outgoing data line is blinded and delete characters are being forced on line. If the receive station does not recognize its RU, the no acknowledge timing circuit is allowed to time-out, the printer is column-spaced, and the station number followed by its no acknowledge status is printed on the page copy. The printout logic is subsequently reset and a printout complete signal triggers the delay start scan circuit in the address counter control. The address counter proceeds to the next selected station gate and the cycle is repeated. An RU is transmitted to each connected station.

(d) The RU2 query is conducted after the message has been transmitted to determine those stations which did not receive the message. Figure 33 is an overall timing diagram of the printout logic during the RU1 and RU2 modes.

Circuit Description

5.138 The subsequent description considers the events occurring when the HSSR Set is in the RU1 or RU2 mode. Refer to Figure 33 which is timing diagram for sending the RU sequence.

(a) In the RU1 or RU2 modes the start 2 flip-flop is primed along with start 1 flip-flop on the P1A input since the RU1 and RU2 lead from the auto-send control is positive at this time. The printout logic is triggered by a positive address available (INV) signal from the address logic (sheet 3 of 6545WD). This signal occurs when the address available flip-flop, 3D4/ZA108-B, is reset by the positive COMMAND COMPLETE signal from the character generator logic. As a result, the start 2 flip-flop, 10D2/ZA514-B, is set to the 1 state which performs three functions:

(1) It enables inhibit gate 10B1/ZA105-J, thereby priming the P1B input of the character available flip-flop 10B2/ZA514-A.

(2) It unblinds NOR gate 10C1/ZA506-G.

(3) Its normal output goes to 0 volt which triggers flip-flop 10F2/ZA513-B via the set 1B input allowing the 500-millisecond gated oscillator 10F3/ZA524 to start timing out. A no acknowledge signal is generated if the receive station does not respond to its RU prior to the time out.

(b) After the character available flip-flop has been primed, the first inverted character clock signal appearing on the set 1B input of this flip-flop sets it to the 1 state. Thus, a character available signal is presented to the transmission logic. Also, NOR gate 10C1/ZA506-G is enabled presenting a positive send signal to the data and clock control logic in module B. This signal blinds the serial data input to the local deserializer and unblinds the send data lead so that the RU information from the transmission logic serializer can be transmitted on-line to the distant stations. The information from the character generator logic representing the three-digit number is sampled in the same manner as previously described when the printout control was activated in the dial response mode.

(c) When the sequence counter receives its third drive pulse, six of the seven parallel data leads to the serializer are spacing. The seventh level is marking, thus representing the character @ in ASCII code. This fictitious character is not sampled and therefore is not transmitted. Only the first three digits are significant when sending the station RU. At the third count the figs/ltrs flip-flop is set to the 1 condition and at the same time the NOR gate 10A4/ZA518-A is enabled. This NOR gate applies a 0 volt to the P0B input of the character available flip-flop. The next character clock pulse received by the printout control logic resets the character available flip-flop which in turn blinds NOR gate 10C1/ZA506-G and the output of this gate goes to -6 volts removing the send signal. Delete characters are once again transmitted over the send data lead and the local deserializer is unblinded and receives delete characters from the serializer.

(d) At the count of four, the memory shift control flip-flop, 10B5/ZA515-B is primed on the P0B input and the next character clock pulse received resets this flip-flop which in turn applies a -6 to 0 volt signal to the set 0B input of the start 2 flip-flop. The start 2 flip-flop 10D2/ZA514-B is reset to the 0 condition and a positive signal is applied to power pulser 10C4/ZA528-C. A positive pulse, 10 to 20 microseconds in duration, is generated to reset all the printout logic with the exception of the flip-flop controlling the no acknowledge timer. This prepares the logic for the next phase, which is the printing out of the station response.

(e) In the sending of the RU, four memory shift pulses have been delivered to the character generator output register. Each shift pulse is used to shift four bits of information in the register. Since it is a 16 bit register, when the fourth shift pulse is received, the information appearing in the register is identical to the information originally read out of the memory. This data is used again when the station response signal is received.

(f) After the station RU is sent, the printout control logic waits for the acknowledge signal from the tone-in logic, indicating that the receive station has recognized its RU. Assume that the acknowledge signal (AK) is received. An 800-microsecond positive pulse representing tone 6 is received on input 32 of NOR gate 10E2/ZA518-F. This signal is also applied to the acknowledge flip-flop 11F1/ZA510-C placing this status flip-flop in the set 1 condition. The output of the NOR gate 10E2/ZA518-F goes to -6 volts and drives inverter 10E2/ZA519-J. The positive signal from the inverter triggers the start 1 flip-flop and the same sequence of events take place as when a connected tone was received during the dial response mode. This time the printout converter will present the following format to the transmission logic: 1-6-8-A-K-CR-CR-LF.

(g) When the acknowledge signal is received it also resets flip-flop 10F2/ZA513-B on the set 0A input. This flip-flop, which was set to 1 condition to start the 500 millisecond gated oscillator when the station RU was transmitted, is reset to the 0 condition and the gated oscillator is prevented from timing out.

(h) If an acknowledge signal is not received within the 500 millisecond time period, the gated oscillator is allowed to time out and a pulse is generated which sets flip-flop 10F4/ZA513-C to 1 and resets flip-flop 10F2/ZA513-B. The normal output of this flip-flop drives NOR gate 10E1/ZA517-A and the 800-microsecond signal delay 10F5/ZA522-B. The normal output of the flip-flop remains at 0 volt for 800 microseconds until the positive output from the signal delay resets the flip-flop. The 800-microsecond positive signal in turn generates a trouble sample pulse, starts the column spacing counter, and sets 1 the no acknowledge (NA) flip-flop 11E1/ZA510-B in the printout converter. The printer is column-spaced by the character generator logic as a result of receiving column advance pulses from the printout control logic. The characters 168NA are printed on the page copy, column spaced 8 characters over.

(i) At the completion of printout the start 1 flip-flop is set to the 0 condition. The positive transistion from this flip-flop at the beginning of the printout sequence, defined as printout complete, is used to trigger the start scan flip-flop 2C3/ZA525-A. Three hundred milliseconds later the address counter is started and proceeds to the next selected station gate, whereby an address available signal starts the cycle again. Each connected station is polled in the RU1 mode. In the RU2 mode each station that acknowledged in the RU1 mode is queried.

(j) The maximum and minimum time required to send the individual RU's is 66. 4 and 16. 6 milliseconds. The polling of 50 stations at a transmission rate of 600 baud, assuming all stations do not acknowledge, requires a maximum time of approximately 47 seconds.

Test Switches

5.139 To facilitate testing of the HSSR Set in the RU1 or RU2 mode, test switches 10F5/SA21 and 10F7/SA22 (SIMULATE RU RESPONSE) have been included in the logic. These switches are located on the front panel and both must be in the TEST position during a test.

(a) With both switches in the TEST position, acknowledge signals are locally generated in a local test situation. Acknowledge tones are not received, and the only signals generated are no acknowledge signals from the gated oscillator 10F3/ZA524. Thus, for 10 selected stations, 10 RU1's are transmitted resulting in 10 no acknowledge signals.

A reset pulse is generated, since no stations responded, and the set reverts to the idle condition rather than advancing to the message mode to test other automatic sequences.

(b) However, with switches SA21 and SA22 in the TEST position, the ground applied the P1A input of the NA flip-flop 10F4/ZA513-C is removed. Instead, this input is primed by the simulate AK flip-flop. The normal output of the latter flip-flop is coupled to input 32 of NOR gate 10E2/ZA518-F. Therefore, during a test condition, when the set is in the RU1 or RU2 mode, flip-flop 10F2/ZA513-B is set to the 1 condition when an address available pulse is received from the address counter control. Five hundred milliseconds later a pulse from the gated oscillator is applied to flip-flops 10F4/ZA513-C and 10F7/ZA516-A. Flip-flop 10F4/ZA513-C is not triggered. Its P1A input is at -6 volts. However, the simulate AK flip-flop is triggered to the set 1 condition since it is connected as a binary. A positive ACK signal from the normal output of flip-flop 10F7/ZA516-A starts the printout sequence and also triggers the acknowledge flip-flop in the printout converter. At the end of the printing cycle, the simulate AK flip-flop is reset to the 0 condition by a reset pulse from power pulser 10D4/ZA528-C. The printout control logic then waits for the next address available signal.

(c) The signals identified as start printout and readout (send mode) are derived in the readout control logic. See sheet 2 of 6545WD. These signals activate the printout logic.

TONE-OUT LOGIC (6546WD, Sheets 2 and 3)

A. General (Figure 35)

5.140 The tone-out logic used during an automatic call may be divided into two functional blocks: tone-out control and tone-out converter. The tone-out control circuitry controls the tone sequence; the tone-out converter receives binary data from the character generator logic and converts the data into dc signals which are converted into tones by the tone transmitter in the Telephone Equipment Cabinet. This logic is contained in module B.

5.141 The dc output from the tone-out converter consists of two signals: a signal corresponding to one of four possible low-frequency tones and a signal corresponding to one of four possible high-frequency tones. With this arrangement, as shown in the table below, there are 16 different tone combinations available, each associated with a specific digit. The tone transmitter will generate a valid tone only when it receives two signals corresponding to a high-frequency tone and a low-frequency tone and a steering signal which is also generated by this logic.

		Highs			
		H1	H2	H3	H4
Lows -	L1	1	2	3	13
	L2	4	5	6	14
	L3	7	8	9	15
	L4	11	0	12	16

L1-697 cps	H1-1209 cps
L2-852 cps	H2-1336 cps
L3-852 cps	H3-1447 cps
L4-941 cps	H4-1633 cps

Tone Assignment

5.142 The tones corresponding to the digits in the table above are used for control purposes by the call control logic. Digits 0 through 9 are used for dialing the station numbers and, in modes other than dial numbers, for transmitting control information to the receive stations. The tone assignments are as follows:

Tone 0 - 2400 wpm, ASCII code, ED, and remote punch off
Tone 2 - 1200 wpm
Tone 3 - 600 wpm
Tone 4 - Go data
Tone 6 - EDC
Tone 8 - Baudot code
Tone 9 - Remote punch on
Tone 12 - Punctuation tone, separates a set of three-digit sequences
Tone 13 - Precedence, flash override
Tone 14 - Precedence, flash
Tone 15 - Precedence, immediate
Tone 16 - Precedence, priority

5.143 In addition, three-digit tone sequences, are assigned to signal the ESS the type of call being originated: 943, indicating a multi-address call (request for dialing bridge), and 996, indicating a broadcast call. See the timing diagram of the tone-out logic, Figure 36.

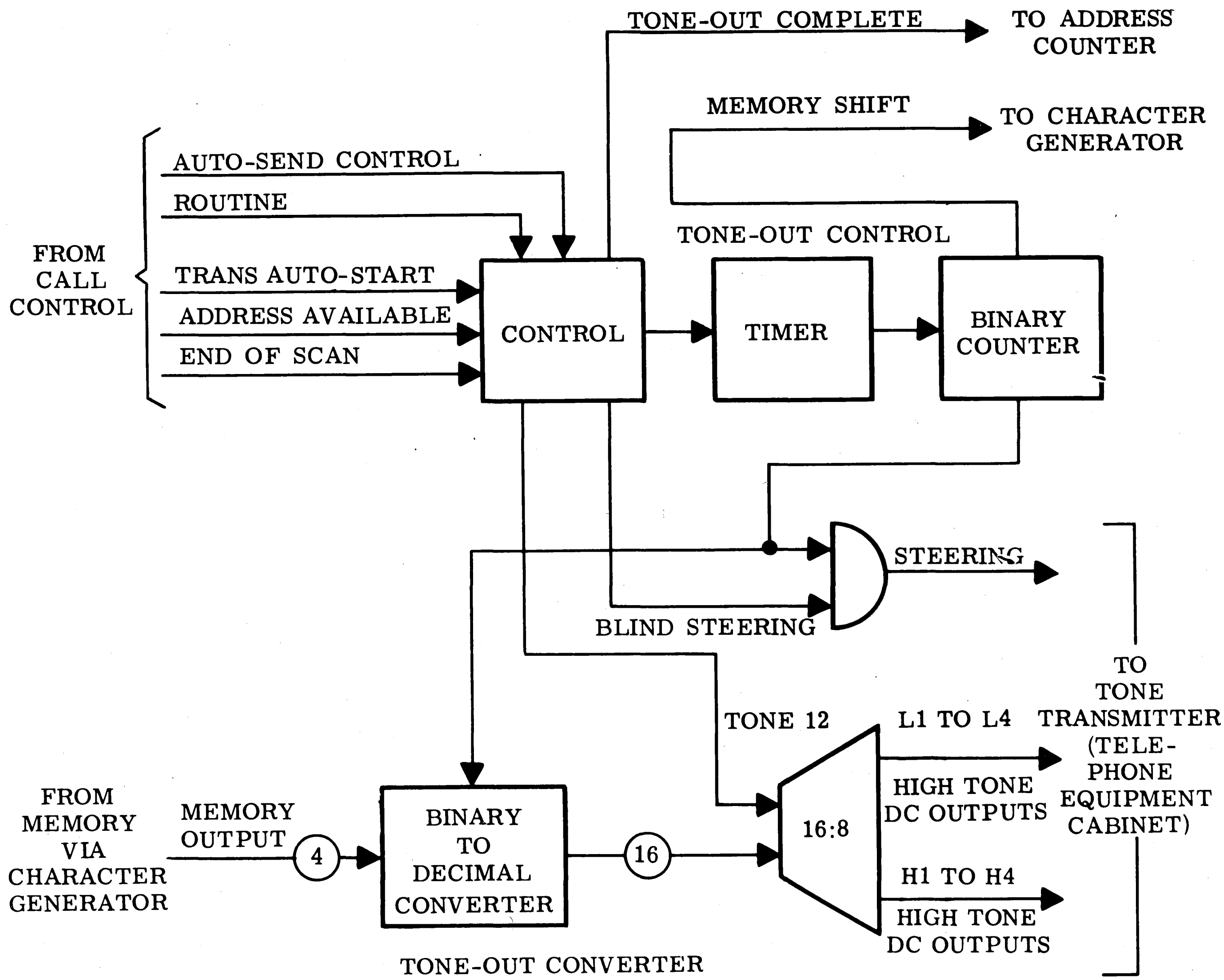


Figure 35 - Send Tone-Out Logic, Block Diagram

5.144 During the sending of an automatic call, the tone-out logic is activated in the start mode to signal the ESS the precedence and type of call being originated. When the set advances to the dial numbers mode, the three-digit sequences followed by a punctuation signal (tone 12) representing the station(s) call numbers are dialed. An end of dialing signal consists of two consecutive punctuation signals. In the preamble mode, single control tones representing various operating modes, as previously described, are transmitted. These signals are subsequently decoded at the receive station(s) in order to automatically program the sets for receiving a message.

5.145 The tone-out control consists basically of a three-stage binary counter which controls the generation of steering signals and the information sampling from the character generator logic. The tone-out converter is basically a binary to decimal (4 to 16) which converts the binary information from the memory to 16 decimal outputs. The decimal outputs are converted to provide a 2 out of 8 signal which represents one low signal and one high signal. The combined logic is illustrated in a simplified block diagram, Figure 35.

5.146 The important signals to the tone-out control logic are as follows:

(a) Start, Dial Numbers and Preamble: These signals originate in the auto-send control logic and prime the send portion of the tone-out control logic, they represent the three modes in which the tone-out logic is used during the auto-send condition.

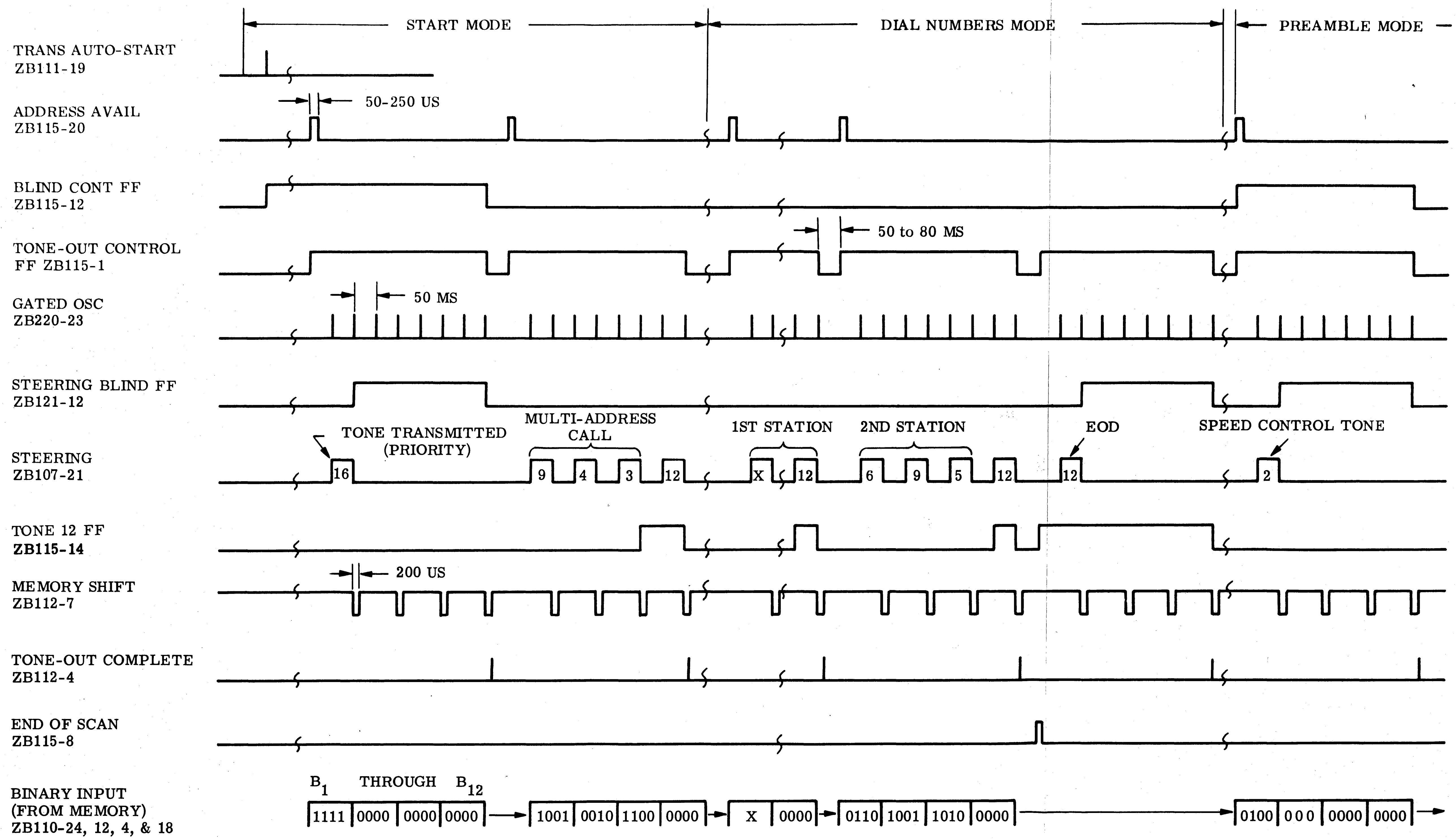


Figure 36 - Tone-Out Logic Timing (Auto-Send Condition)

(b) Routine: This signal primes the blind steering control circuit to permit only one precedence signal to be generated whenever a routine call is not originated.

(c) Transmit Auto-Start: Sets the blind steering control circuit if a precedence call is originated.

(d) Address Available: A signal from the address counter control logic indicating the information requested from the memory is in the character generator output register and ready for sampling by the tone-out logic.

(e) End of Scan: A signal from the address counter logic to generate an extra punctuation tone (tone 12) indicating the end of dialing to the ESS.

(f) Memory Output Buffer: Four leads from the character generator logic on which the memory data is presented to the tone-out converter for conversion to the proper dc levels: -6 volts for the on condition, and 0 volts for the off condition.

5.147 The signals generated by the tone-out logic are as follows:

(a) Steering: A signal, normally 50 milliseconds in duration, sent to the Telephone Equipment Cabinet tone transmitter for sampling the low and high dc signal pairs.

(b) Eight leads to the tone transmitter on which a low and a high dc signal are presented for sampling.

(c) Memory Shift: A signal to the character generator logic instructing it to shift the information in its output register.

(d) Tone-Out Complete: A signal indicating the tone-out sequence has been completed and used to start the address counter.

B. Tone-Out Logic Detailed Description (Figure 35 and 6546WD, Sheets 2 and 3)

Precedence Call

5.148 Initially, all flip-flops in the tone-out logic are in the set 0 condition. An automatic call is originated and a preliminary scan occurs. At the end of this scan a transmitter auto-start pulse is generated in the auto-start control logic and received by the tone-out logic inhibit gate 2D2/ZB111-H. Assume a precedence call is originated. In this case the lead defined as routine is at 0 volts and this signal is applied to inverter 2D1/ZB112-K. Therefore, the inverter output is at -6 volts, priming inhibit gate 2D2/ZB111-H. The positive transmitter auto-start pulse is allowed to pass through the inhibit gate, setting the blind control flip-flop 2C3/ZB115-A to the 1 condition. The normal output of this flip-flop primes the steering blind flip-flop 2C5/ZB121-A via its P1B input.

5.149 When the delay start dial signal is received by the HSSR Set, it advances to the start mode. The tone-out control flip-flop 2B2/ZB115-C is primed on its P1A and P1B input. A 0 volt signal is applied to the input 2 of OR gate 2B1/ZB103-E representing the start mode signal from the auto-send control. The tone-out sequence is started when a positive address available signal is received by the tone-out control logic, setting the tone-out control flip-flop to the 1 state.

5.150 The normal output from the tone-out control flip-flop is applied to gated oscillator 2B3/ZB220. The oscillator, a unijunction timer, starts to time-out. Approximately 50 milliseconds later, a narrow, positive pulse is generated which sets the first flip-flop element 2B4/ZB114-A in the three-stage binary counter to the 1 condition. The inverted output of this flip-flop enables NOR gate 2C8/ZB107-D and a positive steering signal is presented to the Telephone Equipment Cabinet. Input 35 of this NOR gate is negative at this time and NOR gate 2C8/ZB107-E is blinded by the positive signal from inverter 2F2/ZB110-K. The steering signal remains positive (on) for 50 milliseconds during which time the second pulse from the gated oscillator resets flip-flop 2B4/ZB114-A to the 0 condition. During the interval of time when the steering signal is present (0 volts), it is applied to inverter 2D7/ZB111-A and, as a result, NOR gate 2D6/ZB108-C is enabled. Inputs 29 and 30 of the NOR gate are -6 volts at this time representing the send/receive lead (negative) and the normal output of the tone 12 flip-flop, 2D3/ZB115-B, which is in the set 0 state. The 0 volt output from the NOR gate 2D6/ZB108-C is then applied to inverter 2D6/ZB111-B, producing a -6 volt signal on a lead defined as blind. This negative blind signal is presented to the tone-out converter whereby NOR gates 3F4/ZB107-B and C are sampled. In the tone-out converter, one of these gates is enabled, depending upon the input to inverter 3F2/ZB110-H. If the input is 0 volts, NOR gate 3F4/ZB107-B is enabled; if it is at -6 volts, then NOR gate 3F4/ZB107-C is enabled.

5.151 The data sampled by the tone logic comes from the character generator logic output register. This information is stored in the memory and subsequently applied to tone-out converter inverters 3F2/ZB110-E, D, A, and H. During the send condition, all information toned-out is stored in the memory and is presented to the call control logic when a read/restore command is presented to the character generator logic. Refer to the appropriate section of a description of character generator logic operation. The only signal transmitted and not stored in the memory is the tone 12 signal. Actually, sixteen bits of information are read out of the memory and stored in the output register, but only 12 bits are used. Four bits at a time are sampled by the tone-out logic; therefore, decimal combinations 1 to 16 are possible. Referring to the four inputs, a -6 volt signal represents a 1 or marking condition. The table on sheet 3 of 6546WD is a conversion listing for the binary inputs. The input signals applied to the four inverters drive four additional inverters, producing a normal and inverted signal. The first three bits are used to drive a set of NOR gates (3A4/ZB106-A to G), which form a 3 to 8 converter. Only one of these gates is enabled depending upon the status of the first three bits (JB2-D1 to D3). The outputs of these NOR gates drive inverters 3A5/ZB109-A to H. With only one of these inverters negative, two output NOR gates are unblinded. As stated previously, status of the fourth information bit determines which NOR gate, 3F4/ZB107-B or C, is enabled during the steering signal. If the input on JB2-D4 represents decimals 0 through 7, NOR gate 3F4/ZB107-B is enabled. Therefore, inverter 3F5/ZB109-J is -6 volts and this signal is applied to a bank of NOR gates (3A5/ZB105-A to G) and to NOR gate 3E5/ZB104-G. One of these NOR gates is enabled and applies a ground signal to two of eight OR gates wired as a 2 out of 8 converter. As a result, one low and one high signal is presented to the tone transmitter.

5.152 For example, if the signals representing tone 2 are transmitted, NOR gate 3B6/ZB105-C is enabled and the output of OR gates 3A8/ZB102-A and 3D8/ZB103-A go to 0 volts, representing L1 and H2 which is tone 2. Refer to the table sheet 3 of 6546WD. The output signals are present for the duration of the steering signals. As shown in the timing diagram, Figure 36, a precedence tone is transmitted during the start mode. In this case, -6 volts appears on input JB2-D4. NOR gate 3F4/ZB107-C is enabled and signals representing the precedence tone 16 are transmitted.

5.153 When the first steering signal subsides, flip-flop 2B4/ZB114-A is set to 0 by the second pulse generated by gated oscillator 2B3/ZB220. The blind signal returns to 0 volts, blinding the NOR gates in the tone-out converter logic. Also, a negative 200-microsecond memory shift pulse is formed by signal delay 2C2/ZB124-A, NOR gate 2C2/ZB108-D, and inverter 2C1/ZB112-B, instructing the character generator to shift the information in the output register so that new information can be sampled (constituting the second tone under other circumstances). Each time the send portion of the tone control is activated, four memory shift pulses are generated. The first counter stage, set to 0 and representing count two, triggers the second counter element 2B4/ZB114-B and is set to the 1 condition. Its normal output goes to 0 volts and sets the steering blind flip-flop 2D5/ZB121-A to the 1 condition. The normal output of this flip-flop presents a 0 volt signal to input 34 of NOR gate 2C8/ZB107-D, blinding this gate. As a result, no steering signals are generated and the outputs from the tone-out converter are blinded. The steering blind flip-flop remains in this condition until eight pulses have been generated by the gated oscillator 2B3/ZB220, indicating a count of 8. At count 8, the normal outputs of flip-flops 2B4/ZB114-A, B and C go to -6 volts and NOR gate 3A6/ZB107-F is enabled. The 0 volt signal from this gate is delayed 100 microseconds by signal delay 2A6/ZB119-B and presented to the power pulser 2A7/ZB526-A via the OR gate. A narrow pulse is generated resetting all the flip-flops in the tone-out control to the set 0 condition, returning the logic to its original state. The power pulser also enables inhibit gate 2B8/ZB112-A and a positive tone-out complete signal is delivered to the call control start address counter control logic so the address counter can advance to the next selected count. Input 2 of the inhibit gate is -6 volts at all times except during the dial response mode. The purpose of this gate is explained in a subsequent paragraph.

5.154 When the next address available signal triggers the tone-out control flip-flop the cycle is repeated. Since the blind control flip-flop was reset, the steering blind flip-flop is not set to the 1 condition at a count of 2 since its P1B input is at -6 volts. Therefore, four steering signals are generated 50 milliseconds apart and occur each time the first counter element 2B4/ZB114-A is triggered to the set 1 condition. Refer to the timing diagram, Figure 36. The information representing 943 (multi-address) is sampled and signaled out. After the third steering signal, count 6, NOR gate 2C4/

ZB108-A is enabled and the 0 volt signal from this gate is presented to a 50-microsecond signal delay, 2C3/ZB124-B. The delays positive transition sets the tone 12 flip-flop 2D3/ZB115-B to the 1 condition. NOR gate 2D6/ZB108-C is blinded and the output of inverter 2D7/ZB111-B goes to 0 volts, blinding the memory information to the tone-out converter. Therefore, tone 12 is forced on the output. With the tone 12 flip-flop in the set 1 state, the next steering signal enables inhibit gate 2D4/ZB112-D, forcing the output leads L4 and H3 in the tone converter to 0 volts via the tone 12 lead. After each three-digit sequence, a tone 12 signal is transmitted.

Routine Call

5.155 During a routine call no precedence signals are toned-out. Any type of call can be originated on a routine basis. In this case, the routine input to the tone-out control logic is at -6 volts and is applied to inverter 2D1/ZB112-K. The output of this inverter presents a 0 volt signal to the base input of inhibit gate 2D2/ZB111-H. As a result, when the positive transmitter auto-start pulse is applied to input 19 of this gate, the signal is inhibited and the blind control flip-flop is not set to the 1 condition. Consequently, the first address available signal received by the tone-out logic produces four steering signals. Then the bridge request (multi-address) broadcast, or the first station number sequence is dialed-out depending upon the type of call being originated.

5.156 When the HSSR Set advances to the dial numbers mode, input 1 of OR gate 2A1/ZB103-E goes to 0 volts and the tone-out control, blind control, and tone 12 flip-flops are primed again by a 0 volt signal from the output of this OR gate. The tone-out logic is activated again by an address available signal and the first selected station, a three-digit sequence, is automatically dialed out. The station numbers are stored in the memory. Similar events take place as previously described when the logic was activated during the start mode. In the dial numbers mode, four steering signals are always generated since the blind control flip-flop is not set to the 1 state until a positive 250-microsecond end of scan signal is received.

5.157 The positive end of scan signal sets both the blind control flip-flop 2C3/ZB115-A and the tone 12 flip-flop 2D3/ZB115-B to the 1 state. These circuits are set-up to send the end of dialing signal to the ESS (essentially an additional tone 12 after the last station has been dialed). See the timing diagram, Figure 36. With the tone 12 flip-flop in the set 1 state, its output applies a -6 volt signal to inhibit gate 2D4/ZB112-D. The end of scan signal also initiates the tone sequence by triggering the tone-out control flip-flop 2B2/ZB115-C. As a result, a steering signal is generated 50 milliseconds later and the positive signal from the output NOR gate 2C8/ZB107-D (steering signal) is applied to input 13 of inhibit gate 2D4/ZB112-D, generating a 0 volt signal, tone 12 (punctuation). This positive signal is applied to the appropriate OR gates in the tone-out converter so that a low 4, high 3 signal is generated for the duration of the steering signal. At this time the information appearing on the leads from the character generator logic is not sampled since NOR gates 3F4/ZB107-B and C are blinded. This is due to positive signals from emitter followers 3E5/ZB113-E and 3E6/ZB113-F blinding all the output NOR gates and allowing the tone 12 signal to prevail. These output circuits are blinded because the tone 12 flip-flop is in the 1 state and applying a 0 volt signal to NOR gate 2C6/ZB108-C holding it off. This causes the blind circuit to remain positive. After the first steering signal, the steering blind flip-flop 2D5/ZB121-A is triggered to the 1 state since the P1B input to this flip-flop is primed. The gated oscillator 2B3/ZB220 continues to generate pulses. Therefore, the sequence counter continues to advance until a tone-out reset pulse is generated. This occurs when NOR gate 2A6/ZB107-F is enabled. The second tone 12, end of dialing (EOD), should occur a maximum of 82 milliseconds after the previous tone 12.

5.158 The end of scan signal is used also to advance the auto-send control logic from the dial numbers to the dial response mode. A positive signal is applied to input 2 of inhibit gate 2B8/ZB112-A inhibiting the tone-out complete signal after the EOD has been transmitted. This prevents the address counter from being started when dialing is completed. The positive dial response signal is also applied to input 36 of NOR gate 2C2/ZB108-D removing the memory shift pulses.

5.159 The tone-out logic is not activated again until the HSSR Set is in the preamble mode. During this mode, 5 discreet control tones are transmitted to the receive station(s) representing the various operating conditions as previously outlined. The 0 volt preamble signal from the auto-send control logic primes the tone-out control, blind control, and tone 12 flip-flops. It also unblinds inhibit gate 2C2/ZB111-J via inverter 2C2/ZB111-K. Therefore, each time the address available signal sets the tone-out control flip-flop to the 1 state, a -6 to 0 volt signal is applied to the set 1B input of the steering blind flip-flop. One steering signal is generated for every address available as was done when a precedence tone was transmitted in the start mode. The sequence counter continues to count, a tone-out complete pulse is generated, and the logic is reset. In the preamble mode the steering pulses are spaced 350 milliseconds apart. The last control signal toned-out is the go data signal. The tone-out logic then remains idle throughout the rest of the call.

Test Features

5.160 To facilitate testing the tone-out sequence, START T.T. OUT (start tone-out) pushbutton 2B1/SB-6 is provided on module B to trigger the tone-out control flip-flop. The P1A input to this flip-flop must be at 0 volts.

5.161 Switches are provided in the tone-out converter to switch out the four information signals from the character generator logic and to set-up the desired combinations for both the printout converter and the tone-out converter logic. A -6 volt signal represents a mark or 1 condition.

TONE-IN LOGIC (6546WD, Sheet 4)

A. General (Figure 12)

5.162 The tone-in logic, contained in module B, monitors the tone-in leads from the tone receiver in the Telephone Equipment Cabinet and converts these signals to one discreet output signal. The signal is then used by various logic blocks to control the HSSR Set in both the send and receive conditions. Input signals are +6 volts for on and -6 volts for off, approximately 50 milliseconds in duration. In order for the tone-in logic to generate a valid signal, one low and one high input signal must be received with a 50 millisecond steering signal. The latter signal is used for sampling purposes.

5.163 The tone-in logic consists, essentially, of an 8 to 16 converter. A combination of one low and one high signal with a steering signal results in an 800-microsecond positive pulse on the output of one of twelve NOR gates. These gates distribute the signals throughout the logic.

5.164 The various signals from the 12 output NOR gates are gated and used to control and indicate certain conditions within the HSSR Set. In the origination of an automatic, multi-address call, the ESS must answer-back by means of tones whether or not a dialing bridge is available. If a bridge is available, tone 7 is generated and detected, and the pulse from the tone 7 gate is used to advance the auto-send control logic in module A to the dial numbers mode. If a bridge is not available, tone 0 is generated and this signal is used to turn on the no bridge indicator (sheet 5 of 6546WD) and to generate a delay disconnect reset pulse.

5.165 With the HSSR Set in the automatic send condition and in the dial response mode, tones are generated by the ESS indicating the status of the dialed station(s). When the set is in one of the RU modes, and the receive station is polled, an acknowledge signal is generated by the receive station set, converted to a tone, and forwarded to the send set. In each case the signals are sampled within the tone-in converter and forwarded to the printout logic (module A) so the respective station number and status can be printed on the page copy. The tone assignments are as follows:

Tone 2 - Out of service (station does not answer)
Tone 3 - Clear-start over (incorrect format)
Tone 5 - Reorder (wrong number)
Tone 8 - Connected
Tone 11 - Busy
Tone 12 - Punctuation
Tone 6 - Acknowledge (receive station recognized its RU)

5.166 Tone 12 (punctuation) is used to separate each station status signal received from the ESS and to drive the start address counter control logic (6545WD, sheet 2). The signal is essentially a start address counter clock and used to prepare the set for printing-out the next station response.

5.167 In the message mode and with an EDC call in progress, signals are generated at the receive station, converted to tones and transmitted to the send station where they are sampled. These signals are the EDC block answer-back which represent the error or no error conditions of individual blocks of data (80 characters) received by the distant station. The answer-backs are sampled, inverted and presented to the EDC logic (module H) so that appropriate action can be taken. Refer to the appropriate section for a description of error detection and correction logic. The EDC answerbacks are coded as follows:

Tone 0 - Block 0 - OK
Tone 2 - Block 0 - Not OK
Tone 3 - Block 1 - OK
Tone 7 - Block 1 - Not OK

5.168 An idle set can be prepared to receive a call automatically by sending it certain control tones. This phase of operation is discussed in Part 6. The various tone assignments listed on schematic diagram 6546WD, sheet 4.

B. Tone-In Logic Detailed Description (6546WD, Sheet 4)

5.169 To facilitate the explanation it is assumed that tone 2 is received and applied to the tone-in logic. In this case, +6 volt signals 50 milliseconds in duration appear on the low 1 and high 2 inputs and turn off inverters 4C2/ZB305-D and 4F2/ZB305-J. These input signals are accompanied by a +6 volt, 50-millisecond signal to inverter 4A2/ZB305-B. The inverted steering signal is delayed approximately 5 milliseconds by signal delay 4B3/ZB302-A and applied to input 11 of inhibit gate 4B4/ZB305-C. Input 10 of the inhibit gate is positive; therefore its output goes to ground, turning off inverter 4B4/ZB306-C. The negative signal from this inverter is applied to emitter followers 4B5/ZB113-G and H which in turn unblind a set of output NOR gates. Since a low 1 and a high 2 signal are present, outputs of inverters 4C3/ZB305-D and 4F3/ZB305-J are at -6 volts. Therefore, only one NOR gate, 4B6/ZB303-B (tone 2) is enabled. Approximately 800 microseconds later, the output of signal delay 4B3/ZB302-A goes negative removing the signal from inhibit gate 4B4/ZB305-C. The output of inverter 4B4/ZB306-C then goes to 0 volts blinding the output NOR gates and removing the positive signal from NOR gate 4B6/ZB303-B. This produces a positive pulse 800 microseconds in duration on the output of this gate (tone 2), and the signal is applied to other logic for control purposes.

5.170 The four inverters (4B7/ZB306-B, 4C7/ZB306-D, 4D7/ZB306-E, and 4F7/ZB306-F) connected to the outputs of tone 2, 3, 7, and 0 NOR gates provide negative sample signals to the EDC logic in module H. The EDC logic also receives a 50-millisecond inverted steering signal from inverter 4A4/ZB306-A via pin JB2-D5. These signals are used only when the HSSR Set is sending and in the message and EDC modes.

ON/OFF HOOK CONTROL AND DELAY DISCONNECT LOGIC

A. General (Figure 12)

5.171 This logic is used during sending and receiving. The following description applies only to automatic send operation. Automatic receive and manual send operation are covered in Parts 6 and 7, respectively.

5.172 The on/off hook control logic controls the on/off hook out and the send data control leads to the Telephone Equipment Cabinet. It also monitors these signals from the Telephone Equipment Cabinet:

(a) On/off hook in

(b) Manual off-hook

(c) Pre-empted

5.173 The delay disconnect logic gates each of the signals used to generate a reset pulse and to disconnect the set. It is, therefore, closely associated with the on/off hook logic. In addition, this logic monitors the on/off hook in signal. The logic uses an integrator circuit to prevent interruption of the off-hook-in signal during line switching which would cause the set to reset. The integrator prevents this from occurring unless the on-hook signal is present for longer than 500 milliseconds. In that event a logic reset pulse is generated.

B. Detailed Description (6546WD, Sheets 1 and 5)

5.174 Initially, the set is idle (logic reset). Following the depression of the AUTO START button on the control panel and the completion of the preliminary scan, the transmitter auto-start pulse, generated in module A, is applied to the set 1A input of the auto-send flip-flop 5D7/ZB517-D. Because no alarm conditions are present, the on/off hook blind input, which originates in the alarm logic (module G), is at 0 volts, priming the P1A input of the auto-send flip-flop. As a result, the flip-flop is set to the 1 state by the transmitter auto-start pulse and its normal output goes to ground, driving emitter follower 5C7/ZB521-H. The output of the emitter follower drives several circuits:

(a) It drives power amplifier 5B6/ZB324 causing its output to go from -28 volts to ground. This signal turns on the AUTO SEND indicator on the control panel.

(b) It primes the P1A input of the send data control flip-flop 5C8/ZB518-A. This circuit can then be set to the 1 state when it receives an end of preamble signal.

(c) The 0 volt signal from the emitter follower blinds NOR gate 5D5/ZB509-D, preventing tones 1 or 9 from passing through unless the set is reset.

(d) It presents a positive signal to the set 1A input of flip-flop 8D2/ZB307-A in the data and clock control logic (6546WD, sheet 8) setting this flip-flop to the 1 state. This unblinds the deserializer input and connects the local serializer output to the deserializer input to permit local printing. This signal also drives inverter 8E3/ZB314-F which unblinds the local clock (2kc) to the transmission logic.

(e) It provides a positive (-6 to 0 volt) signal on the on/off hook out lead on connector pin JB2-A2 which is subsequently presented to the Telephone Equipment Cabinet via filters. The 0 volt signal from emitter follower 5C7/ZB521-H is applied to NOR gate 5D7/ZB509-C causing the output to go to -6 volts, which enables NOR gate 5D8/ZB510-F therefore generating an off-hook signal. The negative output from NOR gate 5D7/ZB509-C is also applied to inverter 5D8/ZB508-D which results in a 0 volt output from inverter 5C8/ZB508-K blinding the punch feed-out circuitry in the module J and the auto-start gate in module A. This logic prevents feeding-out of tape while the set is off-hook. In addition, it prevents an inadvertent auto-start signal from resetting the logic.

(f) The output of the inverter 5D7/ZB508-D, the auto off-hook signal, goes to 0 volts and is applied to two circuits: power pulser 1E6/ZB528-C in the delay disconnect logic which generates a reset pulse to the transmission logic as soon as the set goes off-hook; and NOR gate 7A5/ZB313-C, in the selective control gate logic (6546WD, sheet 7) which unblinds the speed control leads to the Telephone Equipment Cabinet.

5.175 When the off-hook-out signal has been presented to the Telephone Equipment Cabinet, a delay start dial signal is returned. The HSSR Set then advances to the start mode. The delay start dial is an off-hook-in signal of approximately 150 to 300 milliseconds in duration. This signal is received via pin JB1-A3 from a 800-microsecond signal delay in module G. (See sheet 2 of 6547WD.) When off-hook the signal is 0 volts and is presented to inverter 5F2/ZB507-G. The inverter output goes negative for the duration of the signal. This negative signal is presented to the delay disconnect logic (6546WD, sheet 1) where a delay start dial signal is formed by the trailing edge of the off-hook-in wink when the signal returns to the on-hook condition. The positive signal is applied to inverter 1C4/ZB507-H and 400-microsecond signal delay 1D4/ZB512-B. Both the signal delay and inverter drive NOR gate 1C6/ZB509-A. Inputs 1 and 15 are at -6 volts at this time. Input 1 is the inverted output of the auto-send flip-flop 5D6/ZB517-B and input 15 is controlled by the auto-send control output (6545WD, sheet 8) which is in the count 0 (reset) position.

5.176 The inverted off-hook-in signal is inverted again by inverter 1C4/ZB507-H and this positive signal blinds NOR gate 1C6/ZB509-A. When the off-hook signal goes negative (on-hook) the output of the inverter 1C4/ZB507-H goes to -6 volts immediately. However, the output of the signal delay does not go positive until approximately 400 microseconds later. Therefore, NOR gate 1C6/ZB509-A is enabled during this interval and the positive signal from this gate is applied to inverter 1C6/ZB508-H. A negative delay start dial signal is generated and applied to the auto-send control logic in module A. This signal advances the transmitting sequence to the start mode.

5.177 Inhibit gates 1C5/ZB507-J and K in the delay disconnect logic (6546WD, sheet 1) along with the 400-microsecond signal delay form positive start and stop signals for controlling the delay disconnect flip-flop 1D8/ZB524-C. In the case of the delay start dial signal, a stop signal is formed first, then a start signal. The delay disconnect flip-flop is not triggered at this time since the P1A input is at -6 volts due to a 0 volt signal appearing on the input to inverter 1D4/ZB508-E. Once an off-hook-in is presented to the set, should this signal be removed (on-hook), a 400-microsecond positive start signal will trigger flip-flop 1D8/ZB524-C to the 1 state via the set 1A input. The flip-flop applies a 0 volt signal to gated oscillator 1D8/ZB514 and 500 milliseconds later a positive pulse appears at the output which provides a positive logic reset pulse. The set then goes back on-hook. If, however, the off-hook signal is restored prior to the 500-millisecond signal, the delay disconnect is reset and no reset pulses are generated. This condition is indicated by the dotted waveforms in the timing diagram, Figure 37.

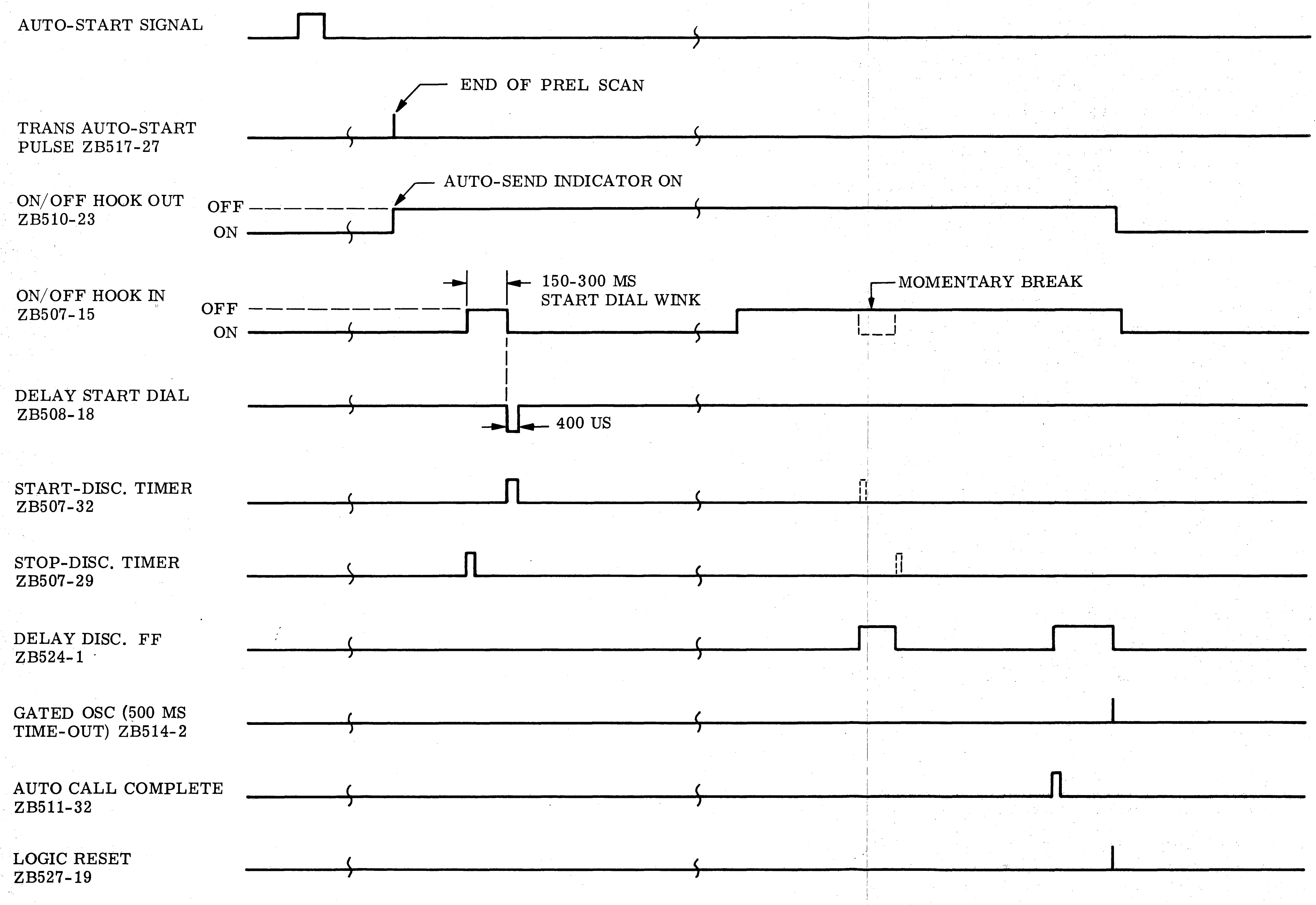


Figure 37 - On/Off Hook Control and Delay Disconnect Logic Timing Diagram

5.178 In the on/off hook control logic (6546WD, sheet 5) during the dial numbers or dial response modes, NOR gate 5E3/ZB509-F is unblinded. The ESS returns an off-hook signal after all station responses have been received by the set. If an off-hook signal is presented during the dialing or prior to the end of scan in the dial response mode, NOR gate 5E3/ZB509-F is enabled producing a positive signal. This signal results in a positive signal from inverter 5E4/ZB508-C which is applied to OR gate 5E5/ZB122-D. The output of the OR gate goes to ground. This positive transition triggers the abnormal disconnect flip-flop 5C5/ZB517-A to the 1 state. The ABNORMAL DISCONNECT indicator on the control panel is turned on via power amplifier 5B5/ZB324. Also, a positive signal is applied to the delay disconnect timer and a logic reset pulse is generated. The 400-microsecond signal delay which drives NOR gate 5E3/ZB509-F prevents NOR gate 5E3/ZB509-E from being enabled since the off-hook-in signal is used to advance the auto-send control in module A to preamble mode. As a result, the auto-send control (6545WD, sheet 8) advances to the preamble mode 100 microseconds after the off-hook-in signal is received. Therefore, NOR gate 5E1/ZB510-A is enabled blinding NOR gate 5E3/ZB509-F before the delayed, inverted off-hook-in signal can enable this gate.

5.179 A no response signal, derived from the no response timers (sheet 9 of 6546WD) is also applied to NOR gate 5E3/ZB509-E and generates an abnormal disconnect when any response failures occur, except no acknowledge in RU1 or RU2.

5.180 During the sending of an automatic call a negative 200-microsecond end of preamble signal is received from the selection gates in module A (inverter 5E7/ZA302-D). This signal is applied to the set 1A input of flip-flop 5C8/ZB518-A triggering it to the 1 state, and a positive send data control signal is forwarded to Telephone Equipment Cabinet. This signal, essentially a go data signal, informs the cabinet to switch out the tone transmitter, switch in the send portion of the data set on the outgoing line, and start the synchronization procedure. The automatic call is terminated when a positive 100-microsecond auto call complete signal is received from module A (sheet 2 of 6545WD) and applied to input 35 of OR gate 1E7/ZB511-A. The delay disconnect flip-flop is triggered to the 1 state, starting the gated oscillator to time-out. After approximately 500 milliseconds, a logic reset pulse is generated to reset the transmission and call control logic. The auto-send flip-flop is reset to 0, removing the off-hook-out signal. The set then is disconnected. Also, if the transmitting set goes on hook as a result of an equipment malfunction at the receive end, a -6 V dc signal is applied to NOR gate 5F3/ZB506-13. This causes a 0 V signal to be applied to the P1A lead of F/F 5F4/ZB518-26. The on-hook signal also causes, after 500 milliseconds, a 0 V delay disconnect signal to be applied to INHIBIT gate 5F3/ZB306-33. This signal is gated thru to set 1A lead of F/F 5F4/ZB518-27. The F/F goes to set 1 state causing the normal output pin 14 to go to 0 V which is applied to OR gate 5E5/ZB122-36. This will cause the abnormal disconnect F/F 5C5/ZB517-A, to go to the set 1 state resulting in an abnormal disconnect indication being shown on the alert section of the control panel. This condition also resets the machine.

5.181 A pre-empt (higher priority) call may arrive during the sending or receiving of a lower priority call. Should this occur, a pre-empt signal is first originated in the ESS and forwarded to the HSSR Set via the Telephone Equipment Cabinet. This signal, +6 volts, is applied to signal delay 2B7/ZG110-B in module G and forwarded to module B via connector JB1-D1. This positive signal is applied to the set 1A input of flip-flop 5C3/ZB516-A, setting it to the 1 state. The flip-flop drives a power amplifier and the PRE-EMPTED indicator on the control panel is lighted. Also the operator alert signal lead is energized controlling an audible alarm within the Telephone Equipment Cabinet. The normal pre-empt signal is applied to OR gate 1E7/ZB511-A and subsequently the delay disconnect flip-flop is triggered. After 500 milliseconds a logic reset pulse is generated and the set is placed on-hook, but ready to be taken off-hook again to receive the incoming higher priority call. The pre-empt signal is removed when the set goes on-hook. The inverted pre-empt signal from inverter 5B2/ZB508-F is applied to the P0B of the delay disconnect flip-flop, holding this input at -6 volts. This prevents the stop signal from resetting the delay disconnect flip-flop when the set goes off-hook.

DATA AND CLOCK CONTROL LOGIC

A. General (Figure 12)

5.182 The data and clock control logic performs the following functions:

(a) In the send condition it connects the local serializer output (module C) to the deserializer input (module D) to facilitate local recording of the transmitted message.

(b) In the send condition and with the set in the data mode, it connects the serial data output from the transmission logic to the send data output. The signals on the send data output are subsequently forwarded to the data set in the Telephone Equipment Cabinet.

(c) In the automatic send condition (RU mode), it alternately blinds the local deserializer input and the outgoing send data lead to permit the sending and printing of the station RU queries.

(d) In the automatic send condition it provides a local clock to the transmission logic. In the automatic or manual send condition it presents the send data clock which is derived in the data sets to the transmission logic.

(e) In the receive condition it unblinds the receive data input to the deserializer and presents the receive clock, derived in the data set, to the transmission logic on the receive clock output lead.

(f) This logic also monitors the ready input. This signal originates in the Telephone Equipment Cabinet and indicates that the synchronization of data sets and other equipment has been completed and that the HSSR Set may start transmitting data.

B. Data and Clock Control Logic **Detailed** Description (6546WD, Sheet 8)

5.183 When the auto-send flip-flop is triggered, its positive signal is applied to the set 1A input flip-flop 8D2/ZB307-A, setting it to the 1 state. The normal output of this flip-flop applies a 0 volt signal to NOR gates 8C7/ZB309-C and 8F5/ZB310-F. The former gate, with 0 volts on input 28, blinds the receive data input. The latter circuit has 0 volts on input 31 which blinds the receive clock input to the transmission logic. The normal output of flip-flop 8D2/ZB307-A drives inverter 8C5/ZB314-B and the -6 volt signal from this inverter unblinds NOR gate 8B7/ZB309-B. Input 7 of this NOR gate is negative at this time and the serial data from the local serializer (on pin JB2-A2) is applied to input 5 of this gate.

5.184 At this time delete characters (all bits marking except the 0 bit) are transmitted locally by the serializer and received by the deserializer. Input 9 of NOR gate 8C7/ZB309-E remains negative during the send condition since NOR gate 8C7/ZB309-C is blinded. The inverted output of flip-flop 8D2/ZB307-A, -6 volts, unblinds NOR gates 8D7/ZB310-A and 8F5/ZB310-E. This allows the send clock from the data set to be applied to both the send and receive clock out leads when the ready signal is received from the Telephone Equipment Cabinet. A positive signal from inverter 8C3/ZB314-E is presented to the transmission logic, indicating the send mode. This signal is also used to indicate the send condition to the tone-out logic (sheet 2 of 6546WD). The auto-send input, a 0 volt signal, turns off inverter 8D3/ZB314-F and the -6 volt signal is applied to NOR gates 8E7/ZB310-B and C. Therefore, the local clock is presented to the transmission logic via the send and receive clock outputs. The ready input, which is off (-6 volts) at this time, is applied to inputs 6 and 29 of the NOR gates, allowing the clock signals (250 microseconds on-off) to pass through.

5.185 The serializer sends delete characters to the local deserializer until station responses are presented to the transmission logic. The serial data signal is represented by -6 volts for space and 0 volts for mark conditions.

5.186 The next signal received by the data and clock control logic is the positive ready signal which indicates that the synchronization procedure of the data sets is completed. The ready signal occurs a maximum of 2 seconds after the send data control is energized; the ready input is normally at a negative voltage. A +6 volt signal from the filter indicating the ready condition is applied to an 800-microsecond signal delay in module G to filter the contact bounce. The positive delayed signal is presented to the set 1A input of flip-flop 8E2/ZB307-B triggering this flip-flop to the 1 state. The normal output of this flip-flop is applied to the emitter of inhibit gate 8E3/ZB306-J priming this gate. The output of the inhibit gate 8E3/ZB306-J goes positive if the ready signal is removed prior to the end of message, generating a ready reset signal. In this case, an abnormal disconnect alarm would be indicated when the set is reset.

5.187 For example, if the set is sending or receiving a message and the handset on the Call Director Set is removed from the cradle (manual off-hook), the ready signal from the Telephone Equipment Cabinet is restored to its normal condition causing a ready reset. The ready signal is coupled to emitter follower 8E2/ZB113-M. The positive signal from the emitter follower drives several circuits. One circuit is the emitter of inhibit gate 8F2/ZB314-H. The delayed ready signal is applied to the base of this gate, forming a 100-microsecond positive pulse, sync reset. This signal is used to generate a transmission logic reset pulse since the local clock to the transmission logic is removed and the send clock from the data set is applied. Approximately 100 microseconds after the sync reset pulse, the send clock from the data set is unblinded, and resynchronization of the deserializer takes place. A negative signal from inverter 8E4/ZB314-G unblinds NOR gates 8D6/ZB310-A, 8F6/ZB310-D, 8B5/ZB309-F and 8C6/ZB309-C. The latter gate is blinded by the normal output of flip-flop 8D2/ZB307-A. The positive output of emitter follower 8E2/ZB113-M blinds NOR gates 8E6/ZB310-B and C, removing the local clock (2kc) from the send and receive clock outputs and simultaneously the send clock, derived in the data set, is delivered over these leads to the transmission logic. With NOR gate 8B5/ZB309-F unblinded, the delayed character clock, derived in the transmission logic, is applied to input 31 of this gate and allowed to pass through. The output drives NOR gate 8B7/ZB309-A which drives the output gate 8B7/ZB309-D. The delayed character clock is in phase with the serial data output which is sending delete characters (all bits marking except for the 0 bit). On the send data output 8B7/ZB309-D, a -6 volt signal is a mark and a 0 volt signal is a space condition. The delete characters are transmitted to the receive sets to allow the distant deserializers to synchronize prior to sending the station RU's. The ready signal also lights a READY indicator on module B front panel.

5.188 When the local deserializer is resynchronized, a receiver in sync signal is generated by the transmission logic, presented to the auto-send control logic in module A and the set is advanced to the RU1 mode. After approximately a 300-millisecond time interval, which allows the distant stations to synchronize, the first station RU is transmitted. The printout control logic is activated. The print/send input, derived from NOR gate 10C1/ZA506-G in the printout control, goes positive at the beginning of sending the station RU. The positive signal blinds NOR gate 8B7/ZB309-A, inhibiting the delayed character clock and preventing this output from overriding the serial data output. The receive stations call number (3-digit sequence) is then transmitted. Refer to Figure 33 which is a timing diagram of this logic. Simultaneously, the print/send output blinds NOR gate 8B7/ZB309-B, blinding the local deserializer while the station RU is transmitted.

5.189 After the RU is transmitted, the print/send signal returns to -6 volts (print condition), forcing the delayed character clock (delete character) to be transmitted on line again and simultaneously unblinding the local deserializer input to allow delete characters to be locally received. The RU response is received, starting the printout logic, and this information is transmitted to the local deserializer resulting in local printout. During the printout, delete characters are transmitted to the distant receive sets to maintain synchronization.

5.190 The set is then advanced to the message mode which causes a positive signal from the auto-send control logic (6545WD, sheet 8) to be applied to emitter follower 9D2/ZB521-22. The output of this emitter follower presents a 0 volt signal to power amplifier 9B6/ZB326. Its output goes from -28 to 0 volts turning on the MESSAGE indicator on the control panel. The positive signal from this emitter follower is also applied to three NOR gates in the data and clock control logic: 8B7/ZB309-A, 8B3/ZB309-G, and 8A7/ZB304-E. The positive signal to NOR gate 8B3/ZB309-G inhibits, making the output go negative. This output signal is applied to the transmission logic via pin JB2-B2 indicating the message condition.

5.191 The HSSR Set is now temporarily controlled by the transmission logic until the end of the message. A positive signal is applied to input 8 of NOR gate 8A7/ZB304-E; the other inputs to the gate at this time are -6 volts. Thus its output goes to -6 volts. This negative signal, referred to as memory control, is presented to the character generator logic during the message mode instructing this logic that the transmission logic may now use the memory.

5.192 The transmission logic uses the memory only in the EDC mode. The positive message signal from the auto-send control blinds NOR gate 8B7/ZB309-A making the output go to -6 volts which removes the delayed character clock signals by applying a -6 volt signal to input 34 of NOR gate 8B7/ZB309-D. The serial data signals, which are presented to input 35, appear on the output of this gate (send data) as inverted signals.

5.193 When a reader tape-out condition is monitored by the transmission logic, the end of message sequence is transmitted and the HSSR Set advanced to the RU2 mode. At this time, the control of the set is restored to the call control logic. The message lead goes negative, causing the memory control lead to go positive allowing the call control logic to use the memory for sending RU's. Delete characters are again transmitted on the line until the first station RU is sent. The sequence of events are the same as those occurring during the RU1 mode. At the end of a call, an auto call complete signal is applied to the delay disconnect logic (6546WD, sheet 1), input 32 of OR gate 1D7/ZB511-A. A reset pulse is generated 500 milliseconds later, restoring the set to the on-hook condition. The ready signal goes negative and flip-flop 8D2/ZB307-A and 8E2/ZB307-B are reset to the 0 state. The send and receive clock outputs go to -6 volts and 0 volts (marking) appears on the deserializer input lead.

C. Test Features

5.194 This logic has two test switches on the front panel of module B for use in testing and trouble shooting. The switches and their functions are:

(a) Send/Receive Unblind Clock: This switch (8D4/SB25), when in the TEST position, unblinds NOR gates 8E7/ZB310-B and C and permits the local clock to pass through these gates to the transmission logic.

(b) Manual Send/Receive: This button (8D1/SB14) when depressed sets flip-flop 8D2/ZB307-A to the 1 condition, simulating the send condition, and connecting the local serializer output to the deserializer input.

NO RESPONSE TIMERS AND TRANSMITTER SEQUENCE INDICATOR DRIVERS

A. General (Figure 12)

5.195 This logic appears schematically on sheet 9 of 6546WD and is located in module B. The transmitter sequence indicator driver logic is strictly dc logic whereby the various outputs from the auto-send control logic located in module A drive the respective emitter followers. The outputs from these emitter followers provide signals to other logic and also drive power amplifiers located at the top of the schematic. The power amplifiers in turn drive specific indicators on the control panel. A ground signal turns an indicator on. As an automatic call progresses only one sequence indicator is on at a time representing the operating mode of the HSSR Set. The AUTO SEND light remains on throughout the call.

5.196 The no response timers consist of two separate timing circuits, a 3.75 second timer and a 26.25 second timer. The latter circuit consists of a three-stage counter driven by a 3.75 second timer which results in a 26.25 second overall time-out. The various time-outs depend on the accuracy of the gated oscillator adjustments.

5.197 The time-outs prevent the set from stopping in a specific operating mode during the automatic-send condition, holding an off-hook-out signal and tying up the line due to some internal or external signal failure. If a failure occurs, a timer is allowed to time-out and a no response signal is generated resetting the set and placing it on-hook. An audible alarm (equipment alarm) is also energized.

5.198 The various time intervals regarding signaling between the HSSR Set and the ESS are listed below. These intervals are monitored by the timing circuits in this logic.

(a) Time between off-hook-out requesting service and the delay start dial return (off-hook-in wink):

Maximum - 2.88 seconds
Average - 0.63 second
Minimum - 0.22 second

(b) Time between dialing out a request for bridge (943) and a bridge available (tone 7) from the Telephone Equipment Cabinet:

Maximum - 1.27 seconds
Average - 0.15 second
Minimum - 0.14 second

(c) Time between the end of dialing signal to ESS (two consecutive tone 12 signals) and the first call progress report (dial response):

Maximum - 26.09 seconds
Average - 5.34 seconds
Minimum - 0.175 second

(d) Time between the last call progress report (dial response) from the Telephone Equipment Cabinet and the off-hook-in (answer):

Maximum - 0.430 second
Average - 0.255 second
Minimum - 0.18 second

(e) Time between the send data control signal out and the ready signal from the Telephone Equipment Cabinet:

Maximum - 2 seconds

(f) A check is made also of the tone-out logic to assure that the dialing out sequence is completed.

B. No Response Timers Detailed Description (6546WD, Sheet 9)

5.199 To check the time interval between an off-hook-out signal and delay start dial return the transmitter auto-start pulse places the set off-hook. The transmitter auto-start pulse is also applied to the set 1A of flip-flop 9E7/ZB524-B setting this flip-flop to the 1 condition. The normal output of the flip-flop goes to ground and the gated oscillator 9E8/ZB622 starts to time-out, continuing as long as flip-flop 9E7/ZB524-B applies a ground signal to its input. Approximately 3.75 seconds later, a pulse is generated by this oscillator and applied to flip-flop 9E7/ZB523-A which is the first element in the three-stage counter. The signal required to stop the counter is a delay start dial signal from the Telephone Equipment Cabinet (off-hook-in wink). The delay start dial signal is a 400-microsecond negative pulse formed in the delay disconnect logic (sheet 1 of schematic 6546WD) and applied to inverter 9F7/ZB519-C. The output of the inverter goes positive resulting in a positive signal applied to power pulser 9F7/ZB527-C. The power pulser generates a narrow pulse to reset the oscillator control flip-flop 9E7/ZB524-B, stopping the gated oscillator from completing its time-out. Also, the counter flip-flop elements are reset by collector reset, the reset pulse being applied to fan-out gate 9F7/ZB123-D. In this case, a positive no response signal is not generated since NOR gate 9D8/ZB520-B is blinded by the reset pulse.

5.200 To facilitate circuit explanation, assume the delay start dial signal is not received. In this case the gated oscillator is allowed to time-out, generating a narrow, positive pulse 15 microseconds in duration. A pulse is, therefore, generated every 3.75 seconds which drives the counter. When seven pulses are generated, 26.25 seconds have elapsed. At that time all the counter flip-flops are in the set 1 condition and their respective inverted (I) outputs are at -6 volts. Therefore, NOR gate 9F8/ZB520-A is enabled, its output goes positive, and this signal is applied to inverter 9D8/ZB519-K. The output of this inverter goes to -6 volts enabling NOR gate 9D8/ZB520-B since input 5 to this gate is also negative. The positive signal from the gate is presented to OR gate 9D8/ZB515-E causing the output of this gate to go positive, generating a signal defined as no response. The positive no response signal is applied to NOR gate 5E3/ZB509-E setting the abnormal disconnect flip-flop 5C5/ZB517-A to the 1 condition. The ABNORMAL DISCONNECT indicator on the control panel is lighted.

5.201 A positive signal from inverter 5E4/ZB508-C is applied to input 20 of the OR gate located in the delay disconnect logic (6546WD, sheet 1), starting the delay disconnect timer. Approximately 500 milliseconds later a logic reset pulse is generated and the set is placed on-hook. The no response signal goes negative when a reset pulse is received by this logic.

5.202 If the call progresses, the delay start dial signal is received, and the tone-out logic (6546WD, sheets 2 and 3) is activated to signal the ESS the priority and type of call being originated. The tone-out flip-flop is set to the 1 state. The positive signal from this flip-flop is applied to OR gate 9E4/ZB515-C and subsequently sets flip-flop 9C8/ZB524-A to the 1 condition. The normal output of this flip-flop controls gated oscillator 9C8/ZB522 starting this circuit to time-out. The timer is reset by a tone-out complete signal from the tone-out logic which normally occurs 400 milliseconds after the tone-out flip-flop is triggered to the 1 state. The tone-out complete signal is a positive pulse derived from inhibit gate 2B8/ZB112-A and applied to input 22 of OR gate 9D7/ZB515-B and subsequently to the set 0A input of flip-flop 9C8/ZB524-A. If the tone-out complete signal is not received, gated oscillator 9C8/ZB522 generates a positive pulse approximately 15 microseconds in duration which is applied to OR gate 9D8/ZB515-E, resulting in a no response pulse. The ABNORMAL DISCONNECT indicator is lighted and the set is reset.

5.203 If a multi-address or a broadcast call is originated, NOR gate 9E2/ZB510-D is unblinded (input 35 goes negative). The negative end of start signal, 200 microseconds in duration, is applied to input 34 of this gate and once again the short period timer is started. In the case of a multi-address call a bridge available signal (tone 7) is required to stop the time-out and also to advance the auto-send control to the dial numbers mode. The positive bridge available signal, 800 microseconds in duration, is applied to inverter 9E5/ZB519-E.

At this time NOR gates 9E5/ZB520-F and G are unblinded since the set is in the start mode. The negative 800-microsecond signal from the inverter is then applied to NOR gate 9E5/ZB520-G, enabling this gate and stopping the timer by resetting the gated oscillator control flip-flop.

5.204 If the broadcast sequence has been dialed-out to the Telephone Equipment Cabinet, an off-hook-in signal should be returned, indicating all stations have been connected. This signal is used to stop the timer once the end of start signal has triggered the timer as described above. The off-hook signal is derived in the on/off hook control logic (6546WD, sheet 5), inverted and forwarded to NOR gate 9E6/ZB520-E. This NOR gate is enabled, its output goes to ground and the positive transition resets the short period timer flip-flop 9C7/ZB524-A via the set 0A input.

5.205 At the end of dialing, a negative 250-microsecond end of scan pulse is presented to NOR gate 9D2/ZB506-G setting flip-flop 9E7/ZB524-B to the 1 state via the set 1B input. The prime 1B input is 0 volts at this time. The long period timer is started and the first dial response should be received within 26.09 seconds. The first dial response starts the printout logic (sheet 10 of 6545WD), generating a positive start print signal, derived from flip-flop 10D3/ZA514-C. This signal remains positive throughout the printout cycle (approximately 40 milliseconds). The positive transition is applied to power pulser 9F7/ZB527-C and the long period timer is reset.

5.206 Because each response is followed by a punctuation tone (tone 12), the long period timer is started again and then reset again by the next positive start print signal. This indicates the second response has been received. In the dial response mode a 250-microsecond end of scan pulse is applied to NOR gate 9D2/ZB506-G and the long period timer is started again. It is subsequently reset by the first start print signal during the RU1 mode. Prior to the above time, the preamble control signals are toned-out and the short timer is started and stopped as each preamble signal (control tones) is transmitted by the tone-out logic. At the completion of this information, a 250-microsecond end of preamble signal is applied to inverter 9F2/ZB519-B and the short period timer is started again. The end of preamble signal is coincident with the send data control signal lead to the Telephone Equipment Cabinet, indicating go data. The end of preamble signal is converted to a positive pulse which is applied to start OR gate 9E4/ZB515-C, starting the short period timer. The maximum allowable time interval allowed between the send data control out and the ready signal from the Telephone Equipment Cabinet is approximately 2 seconds. Therefore, the positive ready signal is used to reset the short period timer. This signal originates in the data and clock control logic (6546WD, sheet 8).

5.207 This logic gates two additional signals which are not related to the no response timers:

(a) The first signal is the no bridge signal, tone 0, which is an 800-microsecond positive pulse occurring during the start mode. The no bridge signal comes from the tone-in logic (6546WD, sheet 4) but is actually derived in the ESS. It is generated if the ESS is not capable of handling a multi-address or broadcast request. The positive signal is inverted by inverter 9F5/ZB519-E and is applied to NOR gate 9E5/ZB520-G which is unblinded at this time. Therefore, a positive pulse is presented to the delay disconnect logic at OR gate 1E7/ZB511-A and no bridge flip-flop 5C5/ZB516-C. This turns on the NO BRIDGE indicator on the control panel and resets the set.

(b) The second signal gated in this logic is the clear-start over signal (tone 3) which resets the set. This signal also originates in the ESS and is presented to the set via the tone-in logic where a positive 800-microsecond pulse is formed. This positive pulse is applied to inhibit gate 9B8/ZB315-F. The base input to this gate is negative during the dial numbers, start, or dial response modes. Therefore, a positive clear-start over signal is presented to the delay disconnect logic, at OR gate 1D7/ZB511-A on input 4 starting the delay disconnect timer. A logic reset pulse is generated 500 milliseconds later and the set is disconnected.

6. AUTOMATIC RECEIVE LOGIC

GENERAL (Figure 38)

6.01 The call control logic used to control an automatic receive call is described in detail in the following paragraphs. Refer to Part 4 for a description of the automatic call sequence.

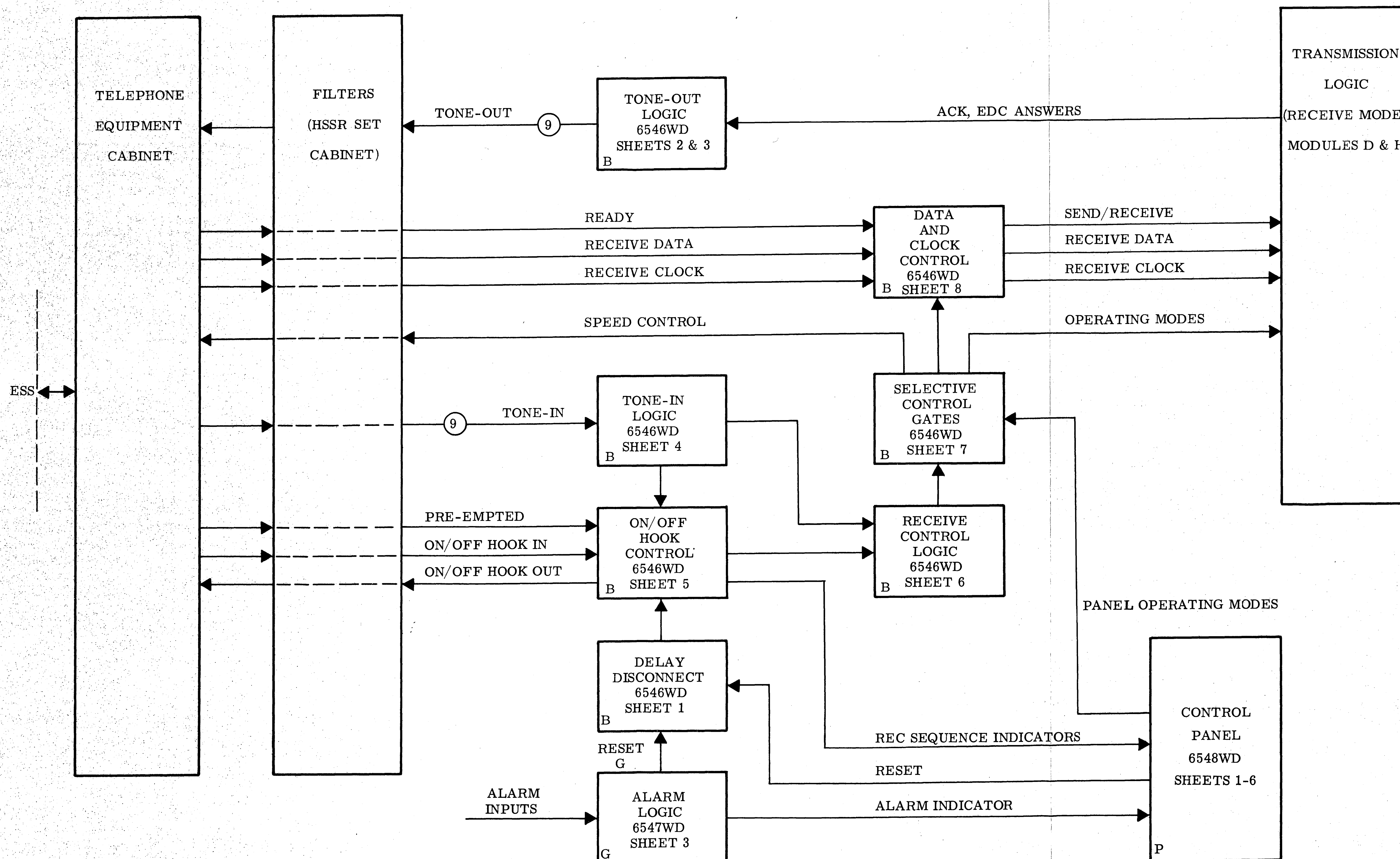


Figure 38 - Automatic Receive Logic, Block Diagram

6.02 As shown in the block diagram, Figure 38, this logic is divided into seven functional blocks which perform the following functions.

(a) On/Off Hook Control: Monitors the on/off-hook-in lead from the Telephone Equipment Cabinet. This signal automatically places the set off-hook. An off-hook-out signal is returned to indicate an answer.

(b) Tone-In Logic: Monitors tones from the ESS (Electronic Switching System) which place the set off-hook, and tones generated by the sending set for setting-up the various operating conditions.

(c) Receive Control: Decodes the dc tone-in signals so that the receive operating conditions may be automatically programmed. It also provides signals which operate the receive operating sequence indicators on the control panel.

(d) Data and Clock Control: Monitors the ready input from the Telephone Equipment Cabinet and controls the receive data and clock which are applied to the transmission logic.

(e) Tone-Out Logic: Originates the acknowledge tone when the receiving set detects its RU query. During the message (EDC) mode, it codes the EDC block answer-back signals which are forwarded as tones to the sending set.

(f) Delay Disconnect Logic: This logic is associated with the on/off hook control logic. It delays disconnecting of the set to permit an acknowledgment of the RU2. It also generates the logic reset pulse.

(g) Selective Control Gates: Gates operating control information and forwards it to the transmission logic and Telephone Equipment Cabinet.

(h) Alarm Logic: Detects certain alarm conditions which prevent the set from answering a call; generates a reset signal during a call sequence.

DETAILED OPERATION

6.03 In the following description of operation refer to the block diagram, Figure 38, and to the specific schematic diagrams as indicated.

6.04 Initially, the HSSR Set is idle. The first signal received is a +6 volt off-hook-in from the ESS via the Telephone Equipment Cabinet and is applied to signal delay 2B7/ZG112-A in the module G. It is then forwarded to inverter 5F1/ZB507-G in the on/off hook control logic (6546WD, sheet 5). The output of this inverter goes to -6 volts and is applied to NOR gate 5D5/ZB509-D through signal delay 5F2/ZB308-B. The set will go to the automatic receive condition if one of two dc signal combinations are received by the tone-in logic, sampled and converted to an 800-microsecond positive pulse and forwarded to the on/off hook control logic. These signals, tone 1 and 9, represent low and high precedence calls, respectively. If a high precedence call is being received, a positive 800-microsecond tone 9 signal is generated by the tone-in logic after sampling the L3 and H3 leads. This signal is presented to input 2 of NOR gate 5D2/ZB508-G in the on/off hook control logic. The output of the NOR gate goes to -6 volts for the duration of the pulse which enables NOR gate 5D5/ZB509-D. The positive signal from this NOR gate is applied to the set 1A input of the auto-receive flip-flop 5D6/ZB517-C. Assume the P1A input to this flip-flop is 0 volts, which is the off-hook blind signal. Therefore, the auto-receive flip-flop is triggered to the 1 state presenting a positive off-hook-out signal to the Telephone Equipment Cabinet indicating to the ESS that the set has answered the incoming call.

6.05. When the positive tone 9 signal is received, flip-flop 5C4/ZB516-B is set to the 1 state, its normal output goes to 0 volts and this signal is applied to two circuits: one turns on the high precedence indicator on the control panel and the other, through NOR gate 5B3/ZB510-B and inverter 5B3/ZB508-A, generates an operator alert which sounds an audible alarm located in the Telephone Equipment Cabinet. In the meantime, the receive auto control is started (sheet 6 of 6546WD). The positive signal from the auto-receive flip-flop is applied to inverters 6D2/ZB507-C and 6E2/ZB507-D. The first inverter output unblinds NOR gates 6B3/ZB505-A, 6F5/ZB506-E and 6F6/ZB506-F. The positive signal from inverter 6E2/ZB507-B is applied to power amplifier 6F3/ZB322 turning on the AUTO REC indicator on the control panel. This indicator remains on throughout the call.

6.06 The steering signal generated when the high precedence tone is received is applied to 200-microsecond signal delay 6B2/ZB525-A and NOR gate 6B3/ZB505-A. The positive steering signal is present for 50 milliseconds. When it returns to -6 volts the signal delay, NOR gate and inverter 6B2/ZB507-E formulate a positive 200-microsecond pulse on the output of NOR gate 6B3/ZB505-A which drives flip-flop 6B4/ZB504-A. This flip-flop, with flip-flops 6B4/ZB504-B and C, form a binary sequence counter. The outputs from the flip-flops drive NOR gates 6C6/ZB505-C to F which provide binary to decimal conversion. Originally, the sequence counter flip-flops are in the set 1 condition; all other flip-flops are initially set 0.

6.07 The first pulse received by the binary sequence counter occurs at the trailing edge of the first steering signal and sets the counter to 0 (count 0). At this time the normal outputs of all the flip-flops are at -6 volts. Therefore, NOR gate 6C6/ZB505-B is enabled providing a 0 volt signal to the P1A inputs of the speed control flip-flops 6B7/ZB502-A and 6C7/ZB502-B. The logic remains idle and waiting for the preamble tones from the send set to set-up the various receive conditions. The first preamble tone received by the tone-in logic sets up the proper speed (bit rate). For example, if the speed is 1200 bps, an 800-microsecond positive pulse, representing tone 2, is applied to set 1A input of flip-flop 6B7/ZB502-A, triggering this flip-flop to the 1 condition. If the speed is 600 bps, tone 3 is received and, as a result, the 600 speed flip-flop is set to the 1 state. If the message is to be received at 2400 bps, tone 0 is received which serves as a buffer tone and no flip-flops are triggered and the 2400 bps condition prevails.

6.08 The 800-microsecond tone signals are generated from the tone-in logic approximately 5 milliseconds after the beginning of a steering signal. When the steering signal associated with the speed control tone goes negative, a 200-microsecond positive pulse is formed again to drive the counter flip-flop 6B4/ZB504-A. The counter is advanced to a binary 1 count and NOR gate 6C6/ZB505-B is blinded. During a count of 1, NOR gate 6C6/ZB505-C is enabled which primes the code flip-flop 6C7/ZB502-C. Approximately 350 milliseconds later the code tone is received. If the set is to be programmed to receive the message in Baudot code, a positive 800-microsecond tone 8 signal is received by the receive control setting flip-flop 6C7/ZB502-C to the 1 condition. If the code is ASCII, tone 0 is received on the tone-in logic; therefore, the code flip-flop is not triggered, representing ASCII code.

6.09 When the steering signal related to the code tone subsides the binary counter is advanced to count 2 and NOR gate 6D6/ZB505-D is enabled, priming the P1A input of the EDC flip-flop 6D7/ZB503-A. The set will accept an EDC call if tone 6 is received. If the receive set is set-up for an ED call, tone 0 is received and the EDC flip-flop remains in the set 0 state. The steering signal goes negative again and the counter is advanced to count 3 by the next step pulse. NOR gate 6D6/ZB505-E is enabled priming flip-flop 6D7/ZB503-B (the remote punch on control flip-flop). If the incoming message is to be punched, tone 9 is received via the tone-in logic to set flip-flop 6D7/ZB503-B to the 1 state forcing the local punch off signal to the on condition. A tone 0 is received if the incoming message does not have to be punched. A punch off request from the send set does not override the local punch on condition. The incoming steering signal subsides and the counter is advanced again to a binary count of 4 and NOR gate 6E6/ZB505-F is enabled. This NOR gate primes the receive data control flip-flop via its P1A input.

6.10 The next tone received is go data, tone 4. The positive transition sets receive data control flip-flop 6E7/ZB503-C to the 1 condition. The normal output of this flip-flop is used to present a signal on the receive data control lead to the Telephone Equipment Cabinet instructing it to switch the tone receiver out of the incoming line, switch in the receive data set, and start the synchronizing process.

6.11 The normal output of flip-flop 6E7/ZB503-C also blinds NOR gate 6B3/ZB505-A. Therefore, when the steering signal related to tone 4 goes negative the counter is not advanced. The positive transition from the normal output of the send data control flip-flop sets gated oscillator control flip-flop 6E7/ZB518-C to the 1 condition, starting the gated oscillator 6E7/ZB614 to time-out. This oscillator is adjusted to a 3.7 to 4 second time-out. The flip-flop control of this oscillator is reset by the receiver in sync signal from the transmission logic if the synchronization procedure is completed within the adjusted time interval. Should the set not receive a ready signal or does not synchronize on the incoming delete characters within the 3.7 second time interval, a receiver not sync reset pulse is generated, the set is reset and goes on-hook.

6.12 With the set programmed, the outputs of the operating mode flip-flops are applied to the selective control gates. See sheet 7 of

6546WD. The positive signal from the receive auto off-hook flip-flop blinds NOR gates 7B4/ ZB311-A to E allowing the signals from the flip-flops in the receive auto control to override the inputs from the control panel. The only input that is not blinded is the local punch on/off signal. This allows the receiving operator to control the local punch on condition. In the auto-send condition, the speed control information is presented to the Telephone Equipment Cabinet through NOR gates 7A8/ZB313-B and 7B8/ZB313-A. The NOR gates 7F7/ZB312-E, F and G are unblinded by the receive auto off-hook signal allowing the receiver control input signals to drive these gates. The Baudot, EDC, and punch on signals are presented to NOR gates 7C6/ZB312-A to C, providing the transmission logic the various operating mode signals. Signals are also presented to the transmission logic informing it that an automatic call is being received. The automatic condition is signified by a -6 volt signal from inverter 5E8/ZB509-B in the on/off hook control logic. The receive condition is identified by a -6 volt signal on the send/receive lead originating in the data and clock control logic (sheet 8 of 6546WD) and presented to the transmission logic on pin JB2-A7.

6.13 Once the Telephone Equipment Cabinet receives the send data control signal, the HSSR Set waits for the ready signal indicating that the synchronization of data sets is completed. The ready signal is applied to the data and clock control logic (6546WD, sheet 8). However, in the receive condition, flip-flop 8D2/ ZB307-A is in the set 0 condition and the auto-send signal is at -6 volts. As a result, the send data and send clock outputs are blinded. The gates controlling local clock 8E7/ZB310-B and C are also blinded since the output of inverter 8D3/ZB314-F is supplying a 0 volt signal.

6.14 A positive ready signal allows inverter output 8E4/ZB314-G to go to -6 volts, unblinding NOR gate 8F7/ZB310-D, and allowing the receive clock pulses to pass through this NOR gate. The receive clock, is derived in the data set, is present at all times and changes to the bit rate requested over the speed control leads as soon as the speed control tone is received from the sender. The receive clock is applied to NOR gate 8F5/ZB310-F. Input 31 to this NOR gate is negative at this time. The -6 volt signal from inverter 8E4/ZB314-G also unblinds NOR gate 8C7/ZB309-C. Input 28 to this NOR gate is at -6 volts since flip-flop 8D2/ ZB307-A is in the set 0 condition.

6.15 With NOR gate 8C7/ZB309-C unblinded, the serial data on the receive data input and applied to inverter 8C7/ZB314 is presented to the local deserializer (module D). These signals (mark is -6 volts and space is 0 volts) correspond to the data being transmitted by the sender. The data signals are received via the data sets, applied to a receive data circuit element 2D4/ZG313 in module G, reshaped and forwarded to the data and clock control logic in module B. Initially, the input data consist of delete characters (all bits marking except the 0 bit). The receive deserializer synchronizes on these characters, requiring a minimum of four characters to synchronize. Refer to the appropriate section for a description of the transmission logic.

6.16 Once the deserializer is synchronized, a negative receiver in sync signal is applied to NOR gate 6D2/ZB506-B in the receive control logic. This signal, accompanied by a negative RU1 mode signal from the transmission logic enables NOR gate 6D2/ZB506-B and places the set in the receive RU1 mode. The receive RU1 sequence indicator on the control panel is lighted by a -28 to 0 volt signal from power amplifier 6F4/ZB322. The positive signal from NOR gate 6D2/ZB506-B resets the time control flip-flop 6E7/ZB518-C to 0, preventing a rec not in sync reset pulse from being generated. Then the set waits for its RU (station call number) to be received.

6.17 The transmission logic has circuitry (module D) to detect the station's three-digit call number (RU) received in serial data form from the send station. When the station RU is detected, a negative start of message (SOM) signal is applied to the call control receive control logic and NOR gate 6F5/ZB506-D enabled. The ACK indicator on the control panel is lighted. The RU1 indicator is extinguished since the negative RU1 mode signal from the transmission logic goes to 0 volts. The set then waits for the start of message sequence. In the meantime, when the transmission logic detects the RU signal, a positive 50-microsecond RU received pulse is generated and presented to signal delay 2E2/ZB118-A in the tone-out logic (module B). This positive signal is delayed 25 microseconds and applied to the set 1A input of flip-flop 2E3/ZB117-C, triggering it to the 1 condition. The normal output of this flip-flop starts the 50-millisecond gated oscillator 2E8/ ZB120 and applies a 0 volt signal to inverter 2C8/ZB110-J through OR gate 2E7/ZB122-A. The output of the inverter goes to -6 volts; this signal enables NOR gate 2C8/ZB107-E. Input 8 to this gate is also negative during the receive condition. The output of NOR gate 2C8/ZB107-E goes to 0 volts generating a steering signal. Simultaneously, the inverted output of flip-flop 2E3/ZB117-C presents a negative signal to inverter 2E4/ZB112-C. The output of the inverter goes to 0 volts and this signal, ACK, is forwarded to the tone-out converter OR gates 3B8/ZB102-B and 3E8/ZB103, forcing the outputs of these gates to 0 volts. Therefore, a low 2 and a high 3 signal accompanied by a steering signal is presented to the tone transmitter in the Telephone Equipment Cabinet where the signals are converted to a tone 6 and transmitted to the send station to indicate an acknowledge condition. After approximately 50 milliseconds, a positive pulse from the gated oscillator resets flip-flop 2E3/ZB117-C to the 0 state removing the steering signal.

6.18 When the transmission logic recognizes the start of message sequence a -6 volt receive unblind signal is presented to NOR gate 6F5/ZB506-E. The gate is then enabled. The MESSAGE indicator is lighted and the ACK indicator is turned off since the SOM signal returns to 0 volts. At this point in the call, the transmission logic unblinds the character generator and punch logic to permit recording of the received message information. The 0 volt output of NOR gate 6F5/ZB506-E drives power amplifier 6F5/ZB422 and primes the P1A input of the abnormal disconnect flip-flop in the on/off hook control logic. If the receive set is inadvertently disconnected (reset) during the message mode, an ABNORMAL DISCONNECT alarm is indicated informing the operator that a complete message was not received. At the end of a message, an end of message (EOM) sequence is transmitted in serial form and is detected by the transmission logic. Upon detection of the EOM the transmission logic presents a negative receiver RU2 mode signal to the receive auto control logic NOR gate 6F6/ZB506-F, enabling this gate. The MESSAGE indicator is turned off since the receive message signal goes to 0 volts, blinding NOR gate 6F5/ZB506-E. The RU2 indicator is lighted by the 0 volt signal from power amplifier 6F6/ZB323. The receive set then waits to detect its RU for the second time in order to send an acknowledge tone to the send station to indicate to the sender that it has received the message. Upon receipt of its RU sequence, the transmission logic samples this information and generates a receive auto call complete signal, a negative pulse applied to the alarm logic in module G (at NOR gate 3B8/ZG117-E). The positive signal from this gate is presented to OR gate 3B7/ZG108-B producing a positive reset G signal which is forwarded to the delay disconnect logic in module B via pin JG1-C9. The signal is presented to input 33 of OR gate 1E7/ZB511-A which sets the delay disconnect flip-flop 1D8/ZB524-C to the 1 state. This starts gated oscillator 1D8/ZB514 to time-out. After approximately 500 milliseconds, a logic reset pulse is generated and the logic is reset. The set goes back on-hook and is prepared to receive or send another call. Simultaneously, when the second RU is detected, a 50-millisecond acknowledge signal is generated in the tone-out logic. The delay disconnect permits this signal to be transmitted to the sending set.

6.19 The operator may disconnect the set at any point in the call by pressing the PANEL RESET button the control panel. During the RU1 mode, should the set not receive its RU prior to receiving the start of message, a negative receive RU format alarm is formed in the transmission logic and applied to NOR gate 3B8/ZG117-F. A positive reset G signal is then applied to the delay disconnect logic resetting the set. As a result, no acknowledge tone is transmitted to the send station and this status is recorded. Should the receive set disconnect during a single address call, the ESS forwards an on-hook signal to the send station causing the send set to reset.

6.20 The following paragraphs describe the operation of the tone-out logic during the reception of an automatic or manual EDC call. This logic generates EDC answer-back signals on commands from the transmission logic. The answer-back signals indicate the status of individual blocks of received message data and originate in the EDC control logic (module H).

6.21 The block answer-back signals (positive) are applied to prime inputs (P1A) of answer-back flip-flops 2F5/ZB116-A, B, C and 2F6/ZB117-A. The sample signal consists of a 200-microsecond negative pulse applied to NOR gate 2F2/ZB108-B. When the set is in the EDC receive condition, inputs 5 and 6 to this gate are at -6 volts, which allows the EDC samples to enable the NOR gate. As a result, the output of NOR gate 2F2/ZB108-B goes positive for 200 microseconds. This signal is delayed 25 microseconds by signal delay 2F3/ZB118-B. The positive signal from the signal delay is applied to the set 1A inputs of the four answer-back flip-flops 2F5/ZB116-A, B, C, and 2F6/ZB117-A. The positive prime signal must be present at least 200 microseconds prior to the positive transition of the sample signal. The block answer signals from the EDC logic (module H)

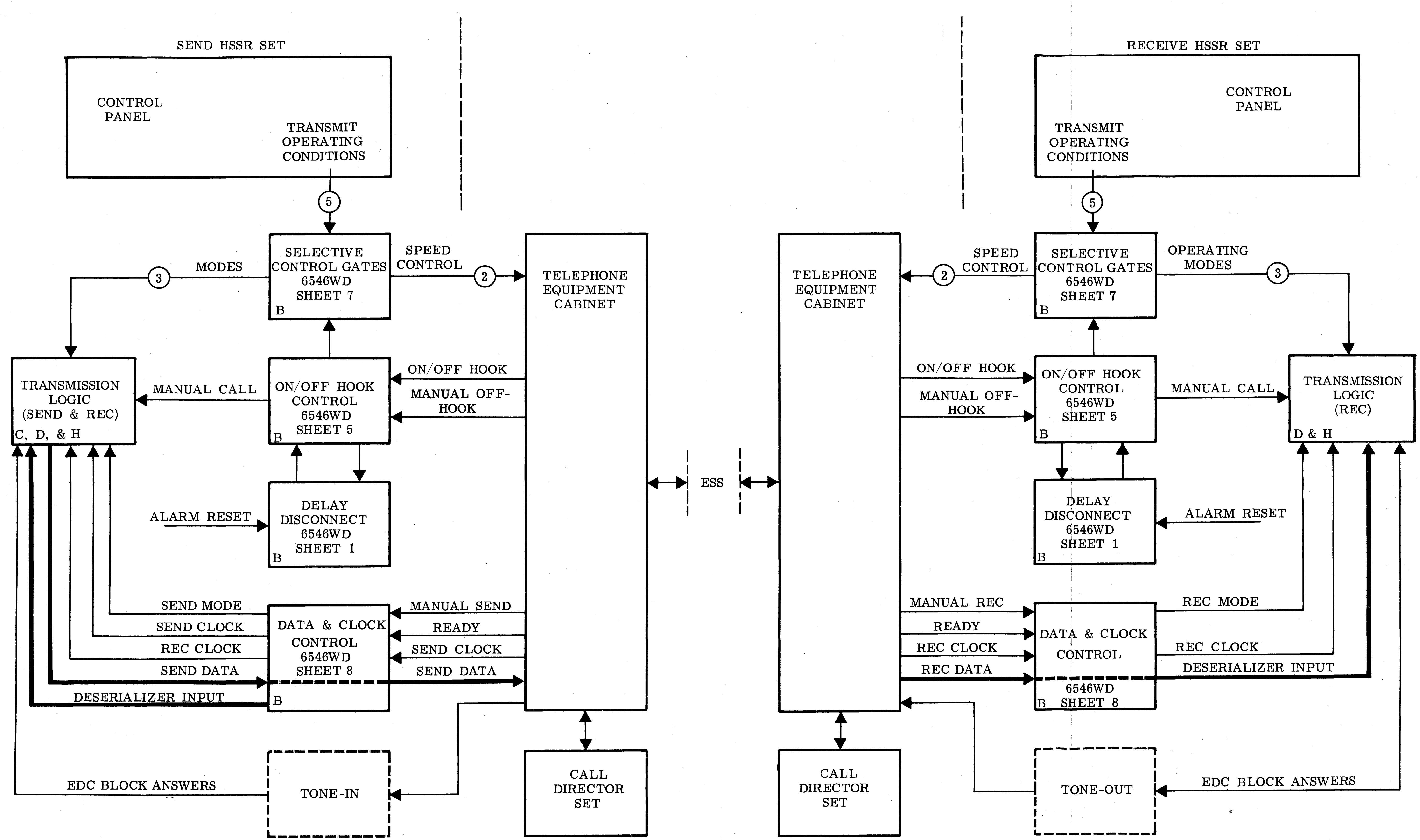


Figure 39 - Manual Call Logic, Block Diagram

appear on connector pins JB2-C1 to C4. The block -0- ok or block -1- ok signal, depending on whether the block is even (block-0) or odd (block-1), is positive throughout the block until an error is detected by the EDC logic. Then the corresponding block ok signal goes to -6 volts and the block not ok goes to 0 volts, priming the respective answer-back flip-flop.

6.22 The EDC sample pulse, generated at the end of each block, sets the answer-back flip-flop which is primed to the 1 state. For example, assume the block -0- ok signal primes flip-flop 2F5/ZB116-A. This flip-flop is set to the 1 state by the positive sample signal. The normal output of this flip-flop goes to 0 volts and this signal is applied to OR gate 2E7/ZB122-A. This causes the 50-millisecond gated oscillator 2E8/ZB120 to start to time-out. Simultaneously, the 0 volt signal from the OR gate forms a steering signal by enabling NOR gate 2C8/ZB107-E. The inverted output of the block -0- ok flip-flop is applied to inverter 2E4/ZB111-C. The output of the inverter goes to 0 volts and is presented to the tone-out converter logic where the dc output signals comprising tone 0 are forced on the outputs of OR gates 3C8/ZB102-C and 3D8/ZB103-A.

6.23 A low 4 and high 2 signal accompanied by a steering signal are presented to the tone transmitter in the Telephone Equipment Cabinet. These signals are converted to a tone representing the digit 0 and transmitted to the send station. At the send station the tone is detected by a tone receiver and presented to the tone-in logic. The signal is decoded by the tone-in logic and forwarded to the send EDC logic so that the required action may be taken. Refer to the appropriate section for a description of transmission logic EDC operation. A positive pulse from gated oscillator 2E8/ZB120 occurs approximately 50 milliseconds later and resets the block -0- ok flip-flop 2F5/ZB116-A, removing the steering and tone signals. The logic remains in this condition until the next answer-back signal is received.

7. MANUAL CALL LOGIC

GENERAL

7.01 The following paragraphs describe in detail the call control logic used by sending and receiving HSSR Sets during manual (voice coordinated) calls. The combined logic is shown in the functional block diagram, Figure 39. Refer also to the manual call sequence chart, Figure 11.

7.02 The manual call logic is much less complex than the logic required for automatic calls. Calls are single address only and require telephone contact between operators before and after the message is transmitted. Telephone facilities are provided by the associated Call Director Sets.

SEND-RECEIVE SEQUENCE

7.03 Initially, the sending set is prepared for transmission by selection of the various operating conditions on the control panel (eg, speed, code, error control, and punch on/off). The high speed reader is loaded with message tape. The transmission logic receives information signals corresponding to the selection of operating conditions (other than speed control) via the selective control gates (6546WD, sheet 7). This occurs in the same manner as when the set is originating an automatic call. The speed control (information rate) data is sent to the Telephone Equipment Cabinet upon receipt of a manual off-hook signal.

7.04 The sending operator then begins the manual call sequence by establishing a voice contact with the receiving station. The telephone handset is removed from its cradle on the Telephone Equipment Cabinet, the number of the station is dialed, and the following events occur:

(a) A 0 volt manual off-hook signal is presented to signal delay 2C7/ZG111-A in the interface logic located in module G. The signal delay filters the input and presents a 0 volt signal to inverter 5F1/ZB507-F in the on/off hook control logic (6546WD, sheet 5). The output of the inverter goes to -6 volts which enables NOR gate 5F8/ZB509-B. As a result, a positive manual signal is sent to the transmission logic on the manual/auto lead. This signal programs the transmission logic for a manual call.

(b) The negative signal from the inverter unblinds inhibit gate 5E5/ZB519-A which applies a signal that triggers the abnormal disconnect flip-flop if the set is placed on-hook by the ESS or if an alarm condition energizes the delay disconnect logic prior to the operator placing the handset on the cradle (manual on-hook). With a 0 volt signal on the output of NOR gate 5F8/ZB509-B, the MANUAL OFF-HOOK indicator on the control panel is lighted by a 0 volt signal from power amplifier 5B8/ZB424. The manual signal also blinds the auto-start signal in module A and inhibits the punch feedout circuit in module J by providing a ground signal to these circuits from inverter 5C8/ZB508-K, thus preventing a call from being automatically originated. The manual signal also disables the tape feed circuit when the set is off-hook. In the manual off-hook condition the Telephone Equipment Cabinet forwards an off-hook-in signal to the set. The 0 volt signal from the manual off-hook gate 5F8/ZB509-B is also applied to NOR gate 7A5/ZB313-C in the selective control gate logic (6546WD, sheet 7). The -6 volt output from NOR gate 7A5/ZB313-C unblinds the speed control gates so that speed control information can be presented to the Telephone Equipment Cabinet.

7.05 After the receive station has been dialed, and if it is not busy, its telephone is rung. The receiving operator answers the telephone and voice contact is established. At the receive station a manual off-hook and an off-hook-in signal are applied to the call control logic to program the set for a manual call. The receiving operator, per verbal instructions, selects the various transmit operating conditions to coincide with the conditions set up at the send station. The respective sets are now prepared for message transmission.

7.06 The voice connection is removed when the send operator depresses the SEND DATA transfer key on the Call Director. This is essentially a go data button. The receiving operator then depresses the RECEIVE DATA transfer key and when the handsets are placed on the cradle the data sets are switched into the corresponding lines and synchronization of these units is then started.

7.07 With the SEND DATA transfer key depressed, a 0 volt manual send signal is presented to signal delay 2B7/ZG112-B via the manual send/receive input. A positive -6 to 0 volt signal from this delay circuit is presented to the set 1B of flip-flop 8D2/ZB307-A and input 1 of NOR gate 8B7/ZB309-A in the data and clock control logic (6546WD, sheet 8). The gate unblinds the send data output, allowing the data from the serializer to pass through NOR gate 8B7/ZB309-D. The 0 volt signal from flip-flop 8D2/ZB307-A connects the local serializer to the deserializer as is done in the auto-send condition. In addition, a positive send signal is presented to the transmission logic from inverter 8C3/ZB314-E, to indicate the send mode of operation.

7.08 When the RECEIVE DATA transfer key is depressed, no signals are forwarded to the set. During the synchronization interval the lamps under the corresponding data transfer keys are flashed at a regular interval. When the synchronization of the data sets and external customer equipment is completed, a ready signal is received by the set from the Telephone Equipment Cabinet. The corresponding data transfer key is lighted indicating that the sets are synchronized. The positive ready signal is detected by the data and clock control logic at the send sets and a sync reset pulse is generated and forwarded to transmission logic. Approximately 100 microseconds later the send clock is presented to this logic via the send and receive clock outputs as is done in the auto-send condition.

7.09 Meanwhile the ready signal is also detected by the receiving set, a sync reset pulse is generated and, 100 microseconds later the receive clock is presented to the transmission logic via the receive clock output lead. The deserializer input is then unblinded, coupling the receive data input to the deserializer.

7.10 When the transmission logic receives a sync reset pulse and the clocks are unblinded, delete characters are transmitted by the sending set to allow the local deserializer and distant receive deserializer to synchronize. At the send station the positive ready signal is applied to input 8 of gated oscillator 8B1/ZB125, starting this circuit to time-out. Approximately 300 milliseconds later, a pulse is applied to the set 1A input of flip-flop 8B2/ZB307-C, setting it to the 1 state. The normal output of this flip-flop is applied to NOR gate 8B3/ZB309-G. Input 2 of this gate is -6 volts; therefore, its output goes to -6 volts instructing the transmission logic to start the message.

7.11 As in the automatic condition, the start of message sequence (SOM) is transmitted prior to the message. When the receive set's transmission logic detects this sequence, the punch and printer units are unblinded. After the start of message sequence, the reader is started and the message is transmitted. The message is recorded by both the send and receive station printers and may be punched at the option of the station operators. At the end of the tape, a reader tape-out signal is detected by the transmission logic and an EOM sequence is transmitted. At the receive station, the EOM is detected, blinding the punch and printer logic. Delete characters are transmitted after the EOM sequence.

7.12 The sending operator removes the handset from the cradle which removes the ready signal. The clock and data leads are blinded. The data transfer key is depressed again thereby going to the voice condition. The receiving operator, noticing the printer has stopped, removes the handset and presses the RECEIVE DATA transfer key. Voice contact is established again between the stations to confirm that the message was transmitted and/or received properly.

7.13 The call is completed when the corresponding handsets are placed on the cradle, removing the manual off-hook and the off-hook-in signals. A 200-micorsecond positive pulse is formed by signal delay 1B4/ZB513-A and inhibit gate 1B4/ZB508-G in the delay disconnect logic (6546WD, sheet 1) starting the delay disconnect timer. A logic reset pulse is generated 500 milliseconds later and the set is prepared to send or receive another call.

8. ALARMS AND ALERTS

GENERAL

8.01 The call control logic monitors the various alarm inputs to provide both a visual indication and an audible alarm to inform the operator that a particular alarm condition exists. The majority of the alarm logic is located in module G and is schematically shown on sheet 3 of 6547WD. Part of the logic is located in module B (sheet 5 of 6546WD) and is concerned with the pre-emptive, high precedence, no bridge, and abnormal disconnect alert signals. A separate output is provided which controls an audible operator alert alarm (in the Telephone Equipment Cabinet) under a pre-empt or high precedence alarm condition. In all cases except the memory parity alarm, the alarm condition is represented by a -6 volt signal.

8.02 An ALERT RESET button is provided to reset the audible alarm. In some cases, the visual indication is removed by pressing the ALERT RESET button. In other instances, such as low tape or low paper, the related alarm indicator is not extinguished until the condition is corrected.

8.03 The following alarm conditions are indicated on the control panel and enable the equipment available alarm to the Telephone Equipment Cabinet. In each case manual reset of alarm condition is necessary.

CONDITION	ALARM INDICATION	REQUIRED ACTION
1. Reader Feed Error (ED) Reader Verify Error (ED) Reader Feed Error (EDC) Reader Verify Error (EDC)	Reader Error Reader Error Reader Error Reader Error	Operator has option to reset unit. Operator has option to reset unit. Reset station - unit is reset. Reset station - go back on-hook, unit is reset.
2. Punch Feed Error (ED) Punch Verify Error (ED) Punch Feed Error (EDC) Punch Verify Error (EDC) Punch Blower Failure (Feed Error)	Punch Error Punch Error Punch Error Punch Error Punch Error	Blind punch on signal - unit is reset. Operator has option to reset the unit. Blind punch on signal - unit is reset. Blind punch on signal - reset unit. Blind punch on signal - reset unit.
3. Printer Low Paper (R) Printer Low Paper (L) (Aux)	Low Paper (R), Low Paper (L) and Out of Service	No reset - will blind off-hook-out until condition is corrected.
4. Printer Alarm (High Voltage On)	Printer Alarm	Unit is reset.
5. Low Tape	Low Tape and Out of Service	Blind off-hook - During a call indicates condition.

CONDITION	ALARM INDICATION	REQUIRED ACTION
6. Out of Service (Interlock)	Out of Service	Reset HSSR Set - Blinds off-hook - will reset unit if it is off-hook.
7. Reader Tape Out	Reader Tape Out	Blinds off-hook - unit is reset. In manual call clock is blinded.
8. Memory Parity	Memory Error	Resets station if it occurs during dialing numbers. During a call indicates alarm condition.
9. EDC Memory Parity (Receiver)	Memory Alarm	During EDC call HSSR Set is reset.
10. EDC Alarm (At Transmitter)	EDC Alarm	Resets the HSSR Set - Manual call stops transmission. Operator has option to restart.
11. Call Director Alarm	Call Director	Blinds off-hook.
12. No Bridge Signal During Start Mode	No Bridge	Resets HSSR Set.
13. Abnormal Disconnect	Abnormal Disconnect	Resets the unit if: (a) No response - time out. (b) Off-hook from block control during dialing. (c) On-hook signal during manual off-hook. (d) On-hook signal during message mode. (e) Ready signal removed prior to EOM sequence.
14. Memory Blinded (System DC Not OK)	Memory Blinded and out of service	Blinds off hook.
15. Cabinet High Temperature	High Temperature	DC power is interrupted.

8.04 The following alert conditions will indicate an alert, and enable the alert lead to Telephone Equipment Cabinet, energizing an audible operator alert.

CONDITION	ALERT INDICATION	REQUIRED ACTION
1. Pre-empted	Pre-empted	Off-On hook (300 millisecond wink) follow by pre-empt signal on lead 31. Resets HSSR Set 500 milliseconds after pre-empt signal.
2. High Precedence Incoming Call	High Precedence	HSSR Set answers automatically.

TYPES OF ALARMS

A. High Speed Reader Errors (6547WD, Sheet 3)

8.05 There are two types of high speed reader errors: feed and/or verify. These error signals are derived in the reader control logic (module C). An error condition is represented by a -6 volt signal applied to inverters 3F5/ZG120-F or G. See 6547WD, sheet 3. The positive transition from the output of one of these inverters sets the reader error flip-flop 3D5/ZG113-A to the 1 state which lights the READER ERROR lamp and energizes the audible equipment alarm. In the ED mode, the reader continues to read the tape.

8.06 During an EDC[4] call, a positive EDC mode signal is presented to inverter 3E7/ZG115-J. The output of the inverter unblinds NOR gate 3D6/ZG116-G. A negative reader error alarm signal in this case not only indicates a reader error, but also generates a reset G signal which is forwarded to the delay disconnect logic in module B, causing the unit to reset.

8.07 Note that once the reader error flip-flop 3D5/ZG113-A (6547WD, sheet 3) is triggered by the set 1 state, a positive signal from the normal output through OR gate 3B5/ZG108-A is applied to the prime 1B input of the equipment alarm flip-flop 3E5/ZG114-A. The equipment alarm flip-flop is set to the 1 state by the first positive transition of the send clock that appears on the set 1B input. This results in a negative signal being applied to the Telephone Equipment Cabinet via a filter, thereby energizing an audible alarm external to the HSSR set.

8.08 The alarm indication is removed by pressing the ALERT RESET button on the control panel. A 0 volt signal from the ALERT RESET button is applied to power pulser 5B1/ZB528-B resulting in a positive pulse from this circuit which is used to reset all alarm flip-flops. In this case the reader error and equipment alarm flip-flops are reset.

B. Punch Errors

8.09 Punch error signals are divided into three categories: feed, verify, and chad blower failure. The latter alarm condition is due to a chad blower failure associated with the punch enclosure and produces a punch feed error condition. The punch feed error alarm is dc coupled to the PUNCH ERROR indicator; therefore, if a blower failure condition exists, the alarm indication cannot be reset. A negative punch verify or punch feed error signal is presented to inverters 3F6/ZG120-H or C respectively which trigger the punch error flip-flop 3C6/ZG113-B to the set 1 condition and light the PUNCH ERROR indicator. See 6547WD, sheet 3.

8.10 If a call is in progress, a reset G signal is generated in a similar manner as described for a reader error condition. The punch feed error signal also drives inverter 3C7/ZG120-B. Its output goes to -6 volts and enables NOR gate 3D7/ZG116-F. As a result a positive reset G signal is generated. The 0 volt output from inverter 3C7/ZG120-B blinds the punch on signal to the transmission logic by grounding the output of NOR gate 7E6/ZB312-C. This connection is made on the wiring field. When punch feed error is detected, the punch is stopped immediately to avoid a tape jam and the HSSR Set is reset.

8.11 If the punch feed error alarm cannot be reset by the ALERT RESET button, a chad blower failure exists. The unit will not go off-hook since the off-hook blind signal is at -6 volts.

C. Printer Low Paper

8.12 The PRINTER (L) LOW PAPER and PRINTER (R) LOW PAPER alarm signals originate in the printers, the (L) indicating the left or auxiliary printer and the (R) indicating the right or primary printer. The LOW PAPER alarm signals are applied to inverters 3F2/ZG115-A and 3F3/ZG115-C. Refer to 6547WD, sheet 3. A -6 volt signal represents a low paper condition. The outputs from the inverters drive the respective LOW PAPER indicators on the control panel. When a low paper signal is present a -6 volt blind off-hook signal from NOR gate 3C1/ZG116-E is forwarded to the on/off hook control logic. See 6546WD, sheet 5. This -6 volt signal removes the primes to the auto off-hook-out flip-flops, inhibiting the off-hook-out signal. If the LOW PAPER alarm condition appears while a call is in progress, the LOW PAPER indicator is lighted and the audible equipment alarm is sounded. The call progresses in the normal manner. The audible alarm signal is stopped when the operator depresses the ALERT RESET button. However, the LOW PAPER indicator remains lighted until a roll of paper is placed in the unit. The operator has the option of resetting the unit during a call.

8.13 Once the HSSR Set is disconnected (on-hook) an automatic call cannot be originated. Also, the set will not answer an incoming automatic call until the low paper condition is corrected.

D. Printer Alarm (6547WD, Sheet 3)

8.14 When the HSSR Set is in the idle condition the high voltage (hv) to the primary (right) and auxiliary (left) printers platen and manifold is removed. Under normal operating conditions the hv is applied to the printers if an off-hook-out or a manual off-hook signal is presented to the printer logic in module L. These signals are gated to operate relays that apply the hv to the respective printers, thus preparing them for recording traffic. To ensure that the hv is on for the primary printer, the ready signal is presented to the printer logic to sample the on condition. Should the hv be off, the ready signal, gated in the printer logic, generates a negative printer alarm signal that is applied to inverter 3F3/ZG115-D in the alarm logic.

8.15 During an automatic condition, the PRINTER alarm is lighted, and 500 milliseconds later a logic reset pulse is generated and the unit disconnects. The alarm light may be extinguished by clearing the trouble that caused the alarm.

8.16 During a manual mode, the PRINTER alarm indicator is actuated in the automatic mode. The alarm light may be extinguished when the trouble that caused the alarm is cleared.

8.17 For a detailed description of the printer control logic refer to the appropriate section.

E. High Speed Punch Low Tape Alarm (6547WD, Sheet 3)

8.18 This alarm signal originates in the punch enclosure from a normally closed low tape contact. At a preadjusted low tape condition (100 to 300 ft) this contact opens and interrupts the ground signal to inverter 3F4/ZG115-E. The inverter applies a ground signal to the power amplifier driving the low tape indicator. A -6 volt blind off-hook prevents the unit from generating an off-hook-out signal to the ESS (as is done for the low paper condition). If the LOW TAPE alarm is actuated during a message, the condition is indicated and the call proceeds in the normal manner. Once the unit is disconnected an out of service condition exists until tape is placed in the unit.

F. Out of Service Interlock Alarms (6579WD, Sheets 2 & 3, and 6547WD, Sheet 1)

8.19 All cabinet doors, modules, and module test switches in the HSSR Set are interlocked. Refer to sheets 2 and 3 of 6579WD for a schematic of this logic. The interlocks from the various modules supply ground signals which operate relays located in module G. See sheet 1 of 6547WD. If the interlock circuit is closed (normal operating conditions), the corresponding relay is operated and an indicator located on the front panel of module G is lighted. In addition, a set of relay contacts are wired in series to provide a ground path on the interlock circuit to input 2 of the out of service gating circuit, NOR gate 2B3/ZG117-G. Referring to the interlock relays (sheet 1 of 6547WD), assume the module A interlock is open (test switch in module A in TEST position). In this case relay KA is de-energized and the lamp identified as module A is extinguished. Also, relay contact KA opens and removes the ground signal to the out of service circuit. Input 3 to NOR gate 2B3/ZG117-G is -6 volts and comes from NOR gate 2B3/ZG109-B, which is blinded by a 0 volt output from NOR gate 2B2/ZG109-C. Input on JG4-F10 is floating unless the test set is plugged into the connector to provide a ground signal. With interlock circuit open, NOR gate 2B3/ZG117-G provides a ground signal to NOR gate 3F4/ZG116-A and OR gate 3B7/ZG108-B. A ground signal is also presented to ZG116-A and ZG108-B when a send data isolator fuse is blown. This is accomplished by a ground being presented to NOR gate 2C4/ZG109-G from the send data isolator card when a fuse is blown. This NOR gate acts as an invertor and presents a -6 volt signal to invertor 2B4/ZG115-K which presents a 0 volt signal to 3F4/ZG116-A and 3B7/ZG108-B. As a result of either of the 0 volt signals being presented to ZG115-K and ZG108-B, the OUT OF SERVICE indicator on the control panel is lighted and a negative blind off-hook signal is presented to the on/off hook control. (See 6546WD, sheet 5.) A logic reset pulse is also generated since the reset G input goes positive, and if a call is in progress the HSSR Set is reset (disconnected).

8.20 Referring to the interlock circuit (6547WD, sheet 2) the NOR gates 2B2/ZG109-A, B and C in conjunction with shorting cards ZG302 and ZG303 are arranged to provide an out of service indication under the following conditions:

(a) If the interlock circuit is open.

(b) If one or both shorting cards are removed when the unit is connected to the Telephone Equipment Cabinet.

(c) If the test set is plugged into module G and the shorting cards are not removed to disable the Telephone Equipment Cabinet interface.

8.21 In each of the above conditions NOR gate 2B3/ZG109-A is enabled since inputs 13 and 15 are negative.

G. High Speed Reader Tape Out Alarm (6547WD, Sheet 3)

8.22 The READER TAPE OUT alarm is actuated if the following conditions exist.

(a) One condition which will initiate an alarm exists when a tape-out signal (-6 volts) is present and an attempt is made to originate an automatic call. The READER TAPE OUT alarm is energized by a signal from the AUTO START button on the control panel. In this case a negative READER TAPE OUT alarm signal that originates in the transmission logic module C is applied to NOR gate 3E1/ZG116-D. The negative signal from the control panel AUTO START button enables the gate and the resulting positive transition sets the reader tape-out flip-flop 3D1/ZG114-C to the 1 condition. The normal output of this flip-flop drives power amplifier 3B1/ZG125, turning on the READER TAPE OUT indicator. The output of the reader tape-out flip-flop also blinds NOR gate 3D1/ZG116-E, removing the prime signal from the auto-send flip-flop 5D6/ZB517-B in the on/off hook control logic. See 6546WD, sheet 5. As a result the transmitter auto-start pulse does not trigger the auto-send flip-flop and no off-hook-out signal is generated. The 0 volt signal from flip-flop 3D1/ZG114-C is applied to signal delay 3A7/ZG111-B through a diode gate which results in a 0 volt reset G signal from this circuit, causing the logic to reset. The alarm is reset when a positive signal from the ALERT RESET button is applied to power pulser 5B2/ZB528-B. A positive pulse from this circuit in turn resets the reader tape-out alarm flip-flop.

(b) In the manual mode, the -6 volt tape-out alarm signal is applied to inverter 3E1/ZG120-A which in turn provides a 0 volt prime signal to the PIA input of the reader tape-out flip-flop 3D1/ZG114-C. See 6547WD, sheet 3. Therefore, this flip-flop is set to the 1 condition by a positive manual send signal generated when the send data transfer key on the Call Director Set is operated. As in the automatic condition, the alarm lamp is turned on and the logic is reset.

8.23 Under normal operating conditions, at the end of a transmission the tape-out alarm is not actuated.

8.24 The tape-out lead is interlocked with the high speed reader cover so that a message cannot be transmitted if the cover is open. With the cover up, a -6 volt tape-out signal is presented to the alarm logic.

H. Memory Parity Alarm (6547WD, Sheet 3)

8.25 The memory parity alarm signal is a positive signal which originates in the character generator logic (modules E and F). This positive signal is applied to the emitter of inhibit gate 3E8/ZG120-E and the set 1A input of the memory error flip-flop 3D8/ZG113-C. The flip-flop 3D8/ZG113-C in turn is set to the 1 state and, consequently, the MEMORY ERROR alarm is lighted. If the memory alarm goes positive during the dial numbers mode, the inhibit gate 3E8/ZG120-E is enabled generating a reset G signal, and the alarm indicator is energized.

I. EDC Memory Parity Alarm (6547WD, Sheet 3)

8.26 The EDC memory parity alarm signal is generated by the transmission logic (module H) when a message is transmitted in the EDC mode. The parity check is made at the receiver and the alarm condition is a negative signal presented to NOR gate 3F7/ZG117-B. The NOR gate inverts the signal, setting flip-flop 3D8/ZG113-C. A positive reset G signal is presented to the delay disconnect logic causing the unit to go back on-hook. In HSSR Sets not equipped with the EDC feature (provided by module H), this lead is held at 0 volts to disable it.

J. EDC Alarm

8.27 The EDC alarm signal originates in the EDC logic (module H) at the send station. It is a -6 volt signal generated if any one of the following conditions are detected:

(a) Excessive (seven) consecutive block reruns. Seven block reruns amount to approximately 4 seconds in time at 2400 wpm.

(b) No EDC block responses received from the distant receive station due to failure in the reverse channel.

(c) Internal logic check on answer-back format (block counters).

8.28 The EDC alarm signal (-6 volts) is presented to NOR gate 3F8/ZG117-D which inverts the signal. Refer to 6547WD, sheet 3. The positive signal from this gate sets flip-flop 3E8/ZG114-B to the 1 state causing the EDC ALARM indicator to light. The normal output of the flip-flop is applied to input 25 of OR gate 3B7/ZG108-B and a positive reset G from signal delay 3A7/ZG111-B is applied to the delay disconnect logic. Approximately 500 milliseconds later the logic is reset and transmission stops. Once the logic is reset, the -6 volt EDC alarm signal returns to 0 volts. The alarm is reset in a similar manner as previously described by pressing the ALERT RESET button. In HSSR Sets not equipped with the EDC feature, this lead is held at 0 volts to disable it.

K. Call Director Alarm (6547WD, Sheet 3)

8.29 An input between the HSSR Set and the Telephone Equipment Cabinet is defined as the call director alarm. A +6 volt signal on this lead is the no alarm condition indicating that the connection to the Telephone Equipment Cabinet is made and that power is on in that cabinet. The alarm condition is represented by a -6 volt signal to the input of inverter 3C8/ZG119-J. The output of the inverter applies a 0 volt signal to power amplifier 3B7/ZG223 which lights the CALL DIRECTOR alarm indicator.

L. No Bridge Alarm (6546WD, Sheet 5)

8.30 The no bridge alarm occurs when the ESS is not capable of handling a multi-address or broadcast call. The signal consists of a tone 0 signal from the ESS which is gated in the on/off hook control logic (6546WD, sheet 5) setting the no bridge flip-flop 5C5/ZB516-C to the 1 condition and lighting the NO BRIDGE indicator. A positive equipment alarm signal from inverter 5A5/ZB306-16 is presented to input 7 of OR gate 3B5/ZG108-A. This actuates the audible equipment alarm. The unit is reset by the no bridge signal and the alarm is reset by pressing the ALERT RESET button.

M. Abnormal Disconnect Alarm (6546WD, Sheet 5)

8.31 The abnormal disconnect alarm is indicated when flip-flop 5C5/ZB517-A is set to the 1 state by a positive signal applied to its set 1A input. This occurs under the conditions outlined in Par. 8.04. The ABNORMAL DISCONNECT indicator is lighted and a positive signal from inverter 5A5/ZB306-G ispresented to the alarm logic in module G as is done for a no bridge condition, to energize the audible equipment alarm.

N. Memory Blinded (System DC OK) (6547WD Sheet 3)

8.32 Module G contains logic which monitors the 48 v dc power supply output (6547WD sheet 1). If the 48 volt input should drop to approximately 45 volts the circuit detects this voltage differential and generates a signal that blinds the memory. Also the memory is blinded if the machine is not in the operate condition. The logic that preforms this function is on sheet 4 of 6547WD and works in connection with the memory blind logic on sheet 1 of 6547WD. The logic mentioned above works together to prevent false triggering and the resulting destruction of the information stored in the memory. The alarm condition is indicated and the unit is prevented from going off-hook. The signal is also used to inhibit the receiver control programmer (module D) from going to the message mode.

8.33 The circuitry consists of two relays, 1F3/KG318 (polar relay) and 1E4/KG418. Two inverters, 1F4/ZG119-H and G, are also included in the logic to eliminate noise due to relay contact bounce. Also included are two NOR gates, 1F6/ZG118-G and 4E6/ZG109-A, and one inhibit gate, 4E7/ZG115-F.

8.34 The memory blind logic consists of two sections. The first is the -48 V dc monitor logic (6547WD, sheet 1). The second is the machine idle/operate logic (6547WD sheet 4). Both sections must be satisfied in order to unblind the memory. In the schematic (6547WD, sheet 1) the circuit is shown in the memory blind condition. Relay 1E3/KG418 is not energized thus providing a ground signal on the output lead JG1-E9 through the NC contact which blinds the memory. A -6 volt signal from inverter 1F5/ZG119-H is applied to inverter 3F2/ZG115-B causing the MEMORY BLINDED indicator to light. Also, a blind off-hook signal (-6 volts) is presented to the on/off hook control (6546WD, sheet 5). The memory blind signal from this logic is removed when the power is turned on and the PANEL RESET button is depressed. The PANEL RESET generates a logic reset and presents a ground signal to relay 1E4/KG418. Relay KG418 is energized and latched through its NO contacts. Contact 3 closes placing 48 volts across pin 8 (relay coil) and the 39-volt zener diode. Relay KG318 is energized. Contact 4 of this relay opens and contact 7 closes. The signal on JG1-E9 then goes to -6 volts (the system dc ok condition). Associated with relay KG318 is a bias winding in series with potentiometer RG318 which is adjusted so that when the input voltage drops to 42 volts, relay KG318 changes state resulting in a memory blind signal on output JG1-E9.

8.35 Although the system dc is ok, the machine must be in the operate condition to unblind the memory. This is accomplished by logic on 6547WD, sheet 4. The HSSR Set is defined to be in the OPERATE state when it is sending or receiving on line, or when internal maintenance functions are being performed, such as, loading the memory.

8.36 NOR gate ZG109-A (6547WD, sheet 4) senses In Sync, Clear/Write, Off Hook, and Man. Off Hook at pins 14, 1, 13, and 15, respectively. If any of the above signals are at 0 V indicating the OPERATE state, -6 V, will appear at ZG109-18. In Sync is derived from REC. IN SYNC appearing at JA2-D3 (6547WD, sheet 2). The In Sync signal is taken from the output of inverter ZA507-H. Thus, it is 0 V when the HSSR Set is synchronized in auto-receive mode of operation.

8.37 The clear/write signal is derived from the memory control circuit (6545WD, sheet 3). A -6 V to 0 V transition appears at ZA107-20 when the memory is conditioned for a clear/write cycle. This transition appears at pin 8 of flip-flop ZA516-C setting it to the "1" state. The 0 V appearing at ZA516-1 is applied to ZG109-1. The flip-flop is reset by the counter reset pulse appearing at pin 4.

8.38 Off hook is actually the on/off hook signal generated in the B module on/off hook control circuit.

8.39 The output of ZG109-A is applied to inhibit gate ZG115-F at pin 26 (6547WD, sheet 4). When SE6, the memory load rotary switch (6553WD, sheet 1) is in the normal position, CRG115 blocks the -28 V applied to lamp XDSE2 and -12 V is applied to ZG115-25 through RG115. In this condition, the output of ZG115-E, pin 27, will be the same as the voltage at ZG115-26.

8.40 If the memory load rotary switch is placed in the load position, 0 V will appear at ZG115-25. When pin 26 is at -6 V, pin 27 will also be at -6 V. However, when pin 26 is at 0 V, pin 27 will be at -6 V. This will cause the memory to be unblinded when the rotary switch is placed in the load position with the set idle.

8.41 The output of ZG115-F, pin 27, is applied to ZG119, pins 16 and 20. The voltage at ZG115-27 is the idle/operate signal.

8.42 The idle/operate signal and the system dc ok signal are combined at pins 16 and 20 of ZG119 in an OR function. A 0 V signal at ZG119-18 is a memory unblind signal.

O. Operator Alerts (6547WD, Sheets 2 and 5, and 6547WD, Sheet 5)

8.43 There are two signals which constitute operator alerts. These signals originate in the ESS and are described below.

(a) Pre-empt: This signal is a positive signal from the Telephone Equipment Cabinet applied to signal delay 2D7/ZG110-B (6547WD, sheet 2). The positive transition from the signal delay is presented to the on/off hook logic (6546WD, sheet 5) setting flip-flop 5C3/ZB516-A to the 1 condition, lighting the PRE-EMPTED indicator on the control panel. The pre-empt signal also triggers the delay disconnect flip-flop 1D8/ZB524-C and 500 milliseconds later the unit is reset and the off-hook-out signal is removed. As soon as the unit disconnects, the pre-empt signal is removed. When the pre-empt flip-flop 5C3/ZB516-A is set to the 1 state, inverter 5A3/ZB508-A presents a 0 volt signal to the filters. This signal defined as operator alert turns on an audible alarm which is distinguishable from the audible equipment alarm. The alarm is reset by pressing the ALERT RESET button.

(b) High Precedence Incoming: An off-hook signal followed by a tone 9 signal turns on the HIGH PRECEDENCE indicator and the audible operator alert signal informing the operator a high precedence call is being received. This is accomplished by setting flip-flop 5C4/ZB516-B in the on/off hook control to the 1 state (6546WD, sheet 5). The alarms are reset by pressing the ALERT RESET button.

INPUT AND OUTPUT INTERFACE

8.44 The input and output interface is shown on 6547WD, sheet 2 (module G). All of the interface leads between the HSSR Set and the Telephone Equipment Cabinet are shown with the exception of the call director alarm lead which interfaces with the alarm logic previously described. Note that all of the leads except the tone-out signal pairs pass through circuit cards ZG302 and ZG303. These circuit cards are used as strapping cards for signals between the interface filters and the call control logic. The tone-out leads are disabled since the steering-out lead is opened and the tone transmitter does not sample the dc tone pairs from the call control logic. Removal of the shorting cards permits a test set to be plugged into module G at JG-4 to facilitate local testing of the HSSR Set.