DATA SET 404A
TRANSMITTER-RECEIVER
THEORY OF OPERATION AND
SUPPLEMENTARY INFORMATION

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1. GENERAL

1.01 This section includes detailed description, operation, and test procedures of Data Set 404A. The information contained in this section supplements the information contained in other sections and is not required for installation, maintenance, or service under normal circumstances.

1.02 This section is reissued to change the designations of the circuit packs to apparatus codes. Because of extensive revision, change arrows have been omitted.

1.03 Data Set 404A is a low-speed, parallel transmission transmitter-receiver which automatically transmits and receives multifrequency signals for dialing and controlling purposes. Figure 1 is a front view of the set and its major components.

1.04 For detailed information on Data Set 404A, refer to SD- and CD-1D055-01.

2. DESCRIPTION

2.01 Data Set 404A is capable of transmitting 2-out-of-8 multifrequency data signals to a TOUCH-TONE Serving Central Office or from station to station over a private switching system.

2.02 Data Set 404A is capable of receiving data signals which are generated by the distant transmitter, and converting these signals into a form suitable for operating the associated equipment. Circuitry for remote testing and installation testing is also provided.

2.03 The transmitting levels are 0, -3, -6, or -9 dBm measured with the transmitting pair terminated in 600 ohms. The data set operates properly with a receiving level of -38 (±2) dBm.

2.04 The telephone line connector, J1, contains the transmit and receive pairs. The input impedance of the line receive pair is 600 ohms. The line transmit and receive pairs connect to external line-switching equipment. In addition, two control interface leads and a Signal Ground (SG) lead are provided. The input impedances of the control interface leads are not less than 3000 ohms, and shunt capacity to signal ground is not

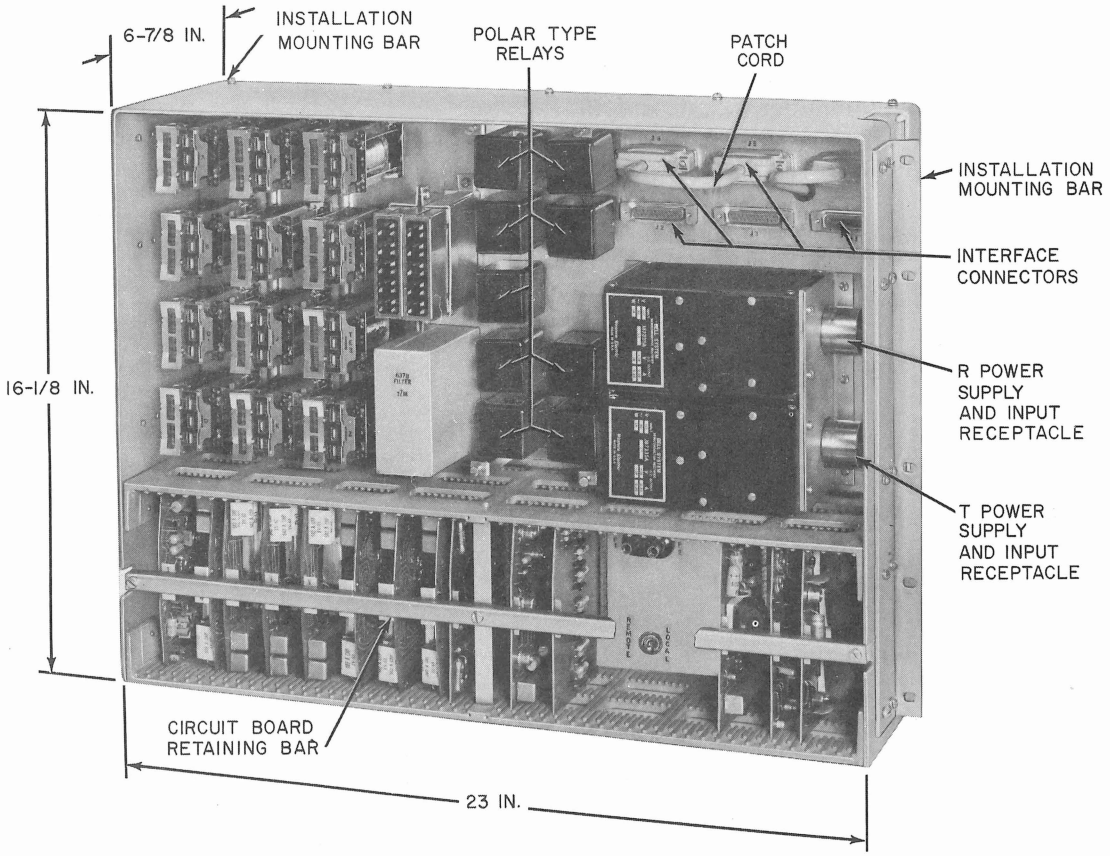

Fig. 1—Data Set 404A, Front View

greater than 2500 $\mu\mu$f. A signal between +3 and +25 volts is recognized as ON; a signal between -3 and -25 volts is recognized as OFF without regard to the rise or fall time of the transition from one state to the other.

2.05 The following control signals are received by the data set from the associated telephone equipment:

(a) ***Request to Send:*** Operation of the Request to Send circuit to an ON condition is interpreted as a signal permitting the data carrier to reach the transmitting telephone line as required by the Send Character (SC) lead.

(b) ***Remote Test:*** The Remote Test (RT) lead allows the customer to place the data set into a condition for testing from a remote Data Test Center. An ON condition requires the data set to go into the test mode. An OFF condition requires a release from the test mode and a return to the normal condition.

2.06 The SG lead is provided in the data set interface to the associated telephone equipment. This lead is common to the ac ground.

2.07 If power fails on either side of the interface, all interface leads are considered to be in the OFF condition at 0 volts. The source impedance of all driving circuits (power OFF) on either side of the interface is not less than 300 ohms with respect to ground.

2.08 A signal level control option is provided to allow insertion of a 10-dB flat loss pad at the data set receiver input. This pad is used to reduce the noise level below receiver sensitivity when the received signal level is expected to exceed -30 dBm. Provision is not made for padding the transmitter signal level below -9 dBm.

2.09 When the Remote Test control interface lead (RT) is turned ON, the data set goes into the test mode. In this condition, the data set:

(a) Disconnects the customer interface (J2) from the data source equipment.

(b) Disconnects the customer interface (J3) from the data sync equipment.

(c) Disconnects the Request to Send lead from the telephone control interface.

(d) Connects the transmit A and B group data leads to the corresponding receive A and B group data leads.

(e) Turns the Request to Send lead ON.

(f) Connects the Send Character (SC) lead to the Character Present (CP) lead.

2.11 The remote Data Test Center can now test the transmitter and receiver completely. By sending a steady tone to operate the C-O channel and by applying both valid and invalid A and B group codes, the test center can test the validity check circuits in the receiver. Both the transmitter frequencies and receiver bandwidths can be checked by sending a steady tone to operate the C-1 channel.

2.12 When used for end-to-end signaling, the data set receiver may be connected to as many as 50 transmitters. The transmitters will be associated in groups of ten by the receiver of the TOUCH-TONE Serving Central Office. Each group of ten input circuits will be monitored for a signal and connected by a mixing pad to the receiving circuit. If a signal is not detected, loss is inserted in the circuit and the noise contribution of the ten circuits is effectively 0. It is to be expected that the following will result from this operation:

(a) If a transmitter is not sending out a tone, the idle circuit noise at the receiver will not be greater than requirement tolerances.

(b) If one transmitter is sending, the signal-to-noise ratio at the receiver will not be greater than 15 dB.

(c) The tone detector of the Serving Central Office will shorten the tone delivered to the receiver by approximately 2 to 10 msec, depending on the input signal-to-noise ratio.

3. THEORY OF OPERATION

3.01 For descriptive purposes, Data Set 404A may be divided into 12 major parts:

A. Power Supply

B. Transmitter Input and Control Circuits

C. Transmitter Oscillators

D. Transmitter Output Amplifier

E. Receiver Input Circuit

F. Receiver AGC Amplifier

G. Band Separation Filter

H. Receiver Channel Amplifiers and Limiters

I. Receiver Detectors

J. Receiver Output Circuit

K. Remote Testing Circuits

L. Installation Testing Circuit

3.02 Data voltage signals greater than +6 volts are accepted in the data set through connector J2 (Fig. 2). These voltages energize one of relays L, M, N, or O, and one of relays P, Q, R, or S, and relay U. The lead on which data is present determines which relay is to be activated. For the purpose of this explanation, assume that the data signal is on lead A1 (terminals 3 and 14 of J2) and that the Send Character (SC) lead is ON.

3.03 A data voltage signal on lead A1 will activate relay L thereby causing contacts 6 and 7 to close. This provides a voltage source which activates relay L'. When relay L' operates, associated contact 12 and 13 provide a ground to terminal 11 of the A group oscillator. The B group oscillator will activate if the data is present on interface leads B1 through B4. The frequencies generated by the A and B group oscillators depend on which relays are applying ground to the oscillators. Therefore, the particular frequencies generated are dependent on the terminals of J2 carrying data.

Note: If two data terminals in the same group are activated together, a data frequency is not generated in that group.

3.04 The data signals generated by the A and B group oscillators are amplified by the transmitter-amplifier. The Send Character (SC) relay (relay U) and the Request to Send lead must be operated before the signals can enter the line circuits.

3.05 The receive pair of the 4-wire private line is connected to terminals 12 and 13 of connector J1. The receiver input circuit consists of a repeat coil and an optional 10-dB loss pad (option W). The signal then passes into the AGC circuit where it is amplified to a fairly uniform level. Feedback control for this AGC action is obtained from the signal in the A group of frequencies. The signal is then separated by the band separation filter into three different frequency components. This filter directs frequency components between 600 Hz and 941 Hz to the A limiter, between 1098 Hz and 1633 Hz to the B limiter, and between 1950 Hz and 2250 Hz to the C limiter.

3.06 The square wave output of each limiter activates detectors which respond to the frequency present in the received data signal. The output of each detector passes through a relay driver. If the detector output signal overcomes the relay driver threshold bias, the corresponding K relay will operate. When the K relay operates, it provides -18 volts to the corresponding A, B, C, D, F, H, J, or K relay. For the purpose of this explanation, assume that the data frequency is such that relays A and F operate. The valid data relay matrix is a series of relays arranged to provide a path through the matrix only when one relay of relays A, B, C, or D and one relay of relays F, H, J, or K is operated. Therefore, the Character Present (CP) lead will be ON only when valid data is being received. Valid data consists of one positive potential from the A group and one positive potential from the B group.

3.07 The diode matrix in the output interface circuit (Fig. 3) applies 0 volts to the output interface whenever data is not present on the line. When data is present, +18 volts are applied through a resistor to the Zener diodes in the output interface circuit. These diodes fire at +6 volts and place a +6 volt signal at output interface terminal J4. The duration of the Output Data and Character Present signals is 40 msec.

A. Power Supply

3.08 There are two power supplies in Data Set 404A. Each power supply converts standard 115-volt 60-Hz ac power into two outputs of +18

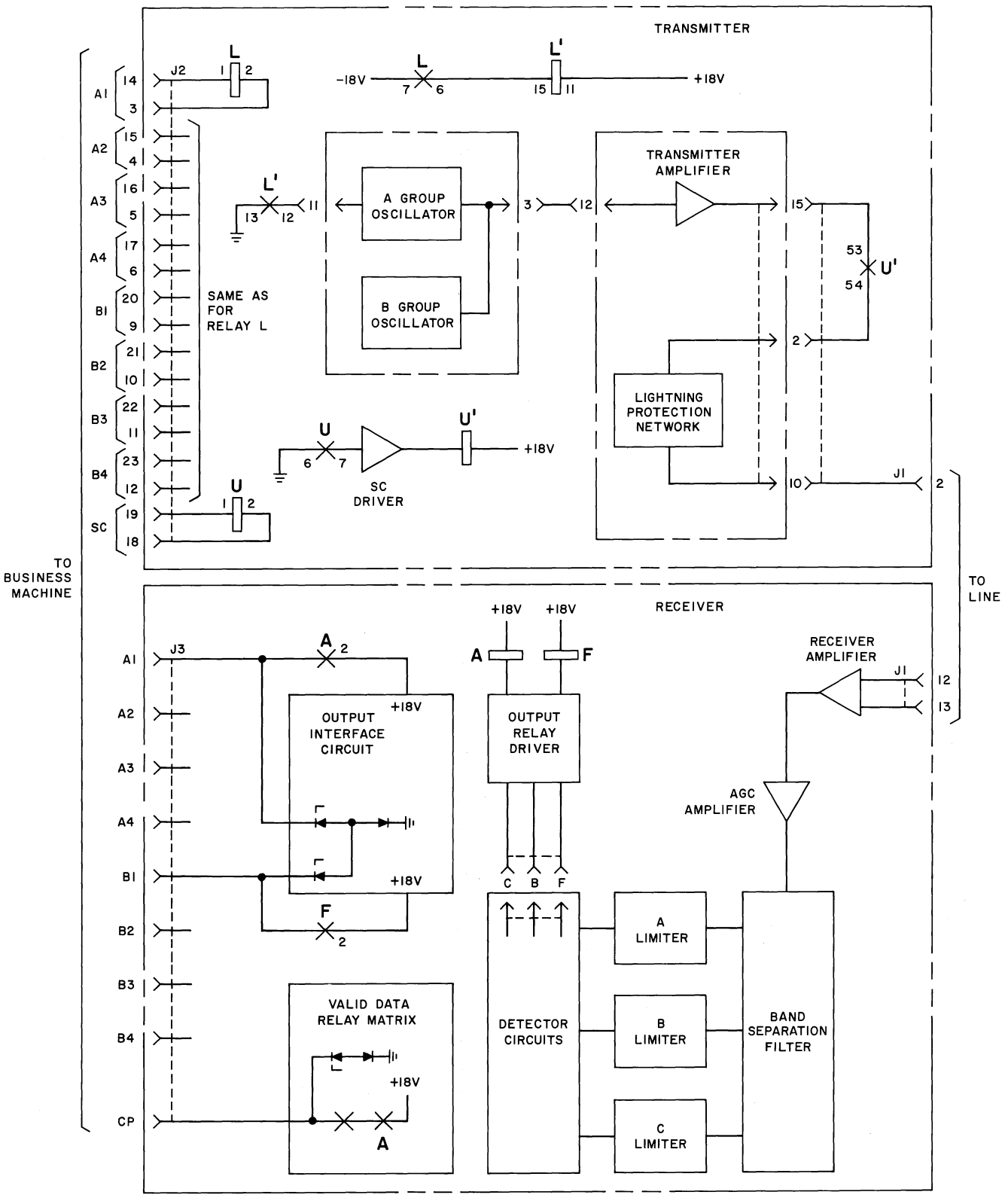

Fig. 2—Data Set 404A, Block Diagram

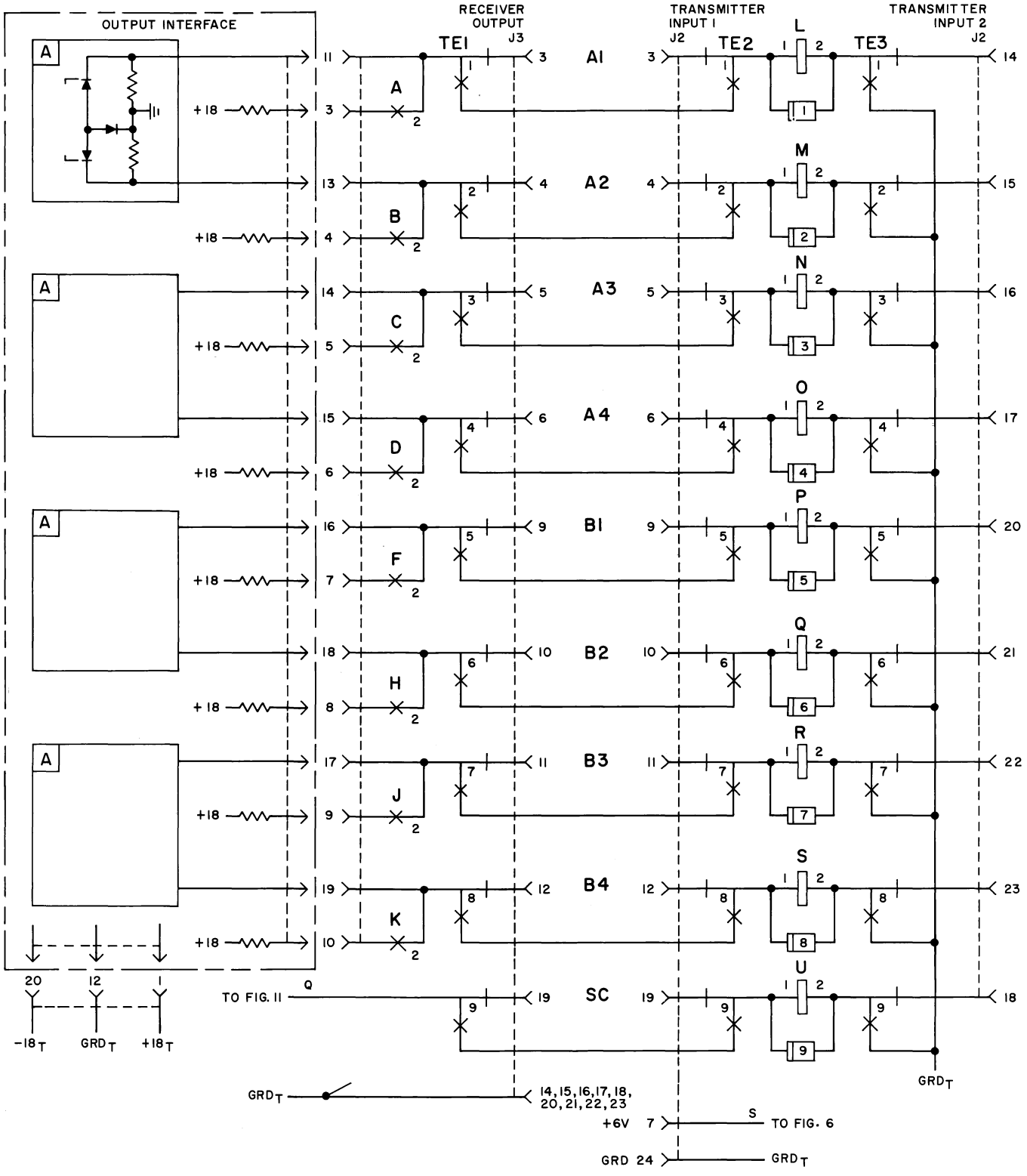

Fig. 3—Interface Diagram

and –18 volts dc. Both power supplies have floating grounds.

B. Transmitter Input and Control Circuits

3.09 Refer to Fig. 4 for the operation of the relay control circuitry. When relay U is operated by voltage on the Send Character (SC) lead, associated contacts 6 and 7 apply ground to the transmitter input circuit. This ground potential activates the SC relay driver through the OR gate. A voltage pulse going to ground also triggers the 50-msec monopulser. This monopulser activates the A group and B group drivers which remain activated for 50 msec. The SC relay driver remains operated for the duration of U relay operation or for a minimum of 50 msec. Activation of the SC relay driver operates the U′ relay. The group driver circuits cannot operate a relay; their only function is to keep an already operated relay in the operated condition.

C. Transmitter Oscillators

3.10 Refer to Fig. 5 for a schematic diagram of the transmitter oscillators. Two oscillators with similar circuitry are provided. The low-frequency oscillator uses transistor Q1 and transformer T1. Bias is provided through winding 9-10 of transformer T1 by the voltage drop across R1 and R4. These resistors are bypassed at signal frequencies by capacitor C2. This bias and R3 fix the emitter current. Alternating current is continuously generated by the oscillating transistors because the collector current is always permitted to flow. When data is not transmitted, two rest frequencies (A0 and B0) are generated and appear at terminal 3. Transformer winding 7-8 is in series with the emitter circuit. Winding 9-10 is connected to the base from the bias supply with a polarity which will cause oscillation.

3.11 The frequency of oscillation is controlled by tuning a tertiary winding. In the absence of data, capacitor C4 sets the oscillator frequency at 600 Hz. When the data source connects ground to circuit board terminals 9, 4, 5, or 11, inductor L1 is shunted across part or all of the tertiary winding, thus setting a frequency of 697, 770, 852, or 941 Hz. Capacitors C6, C7, C8, and C9 substitute for long cabling which is frequently used with this circuit board, thereby assuring that the oscillator will generate the desired frequencies. Varistor RV1 across the base winding limits the amplitude of oscillations at the base of 0.6 volts peak ac. Resistor R2 and capacitor C1 are connected across the base winding to prevent parasitic oscillations. The second oscillator using transistor Q2 operates in exactly the same manner except that the data frequencies are 1098, 1209, 1336, 1477, and 1633 Hz.

D. Transmitter Output Amplifier

3.12 Refer to Fig. 6 for a schematic diagram of the transmitter output amplifier and its associated circuitry. Signals from the transmitter oscillator appear at terminal 12. Resistor R1 and inductor L1 comprise the dc collector supply circuit for transistors Q1 and Q2 in Fig. 5. Resistor R1 is bypassed at signal frequencies by capacitor C2. Inductor L1 and capacitor C1 provide amplitude shaping of the oscillator signal so that signals of different frequencies will have equal amplitudes. The oscillator signal appears at the base of transistor Q1. Base bias for the stage is provided by the voltage divider action of R4, R5, and R6. Capacitor C5 provides decoupling of the power supply ripple. The emitter current is set by R7, R8, R9, and R10. Capacitor C6 bypasses one or more of these resistors at signal frequencies in order to achieve the desired output level as previously described. Resistors R2 and R3 set the collector voltage, and capacitor C3 provides additional decoupling of the power supply ripple. Capacitor C4 prevents dc from appearing at the transmitter telephone line. Varistors RV1 through RV6 provide lightning protection for the transmitter and conduct when more than 3.6 volts are placed across them. The data signal which is less than 3.6 volts does not pass through the varistors. Resistor R14 limits current flow during lightning surges.

3.13 Relay BC is controlled directly by the associated telephone equipment. When the relay is operated, it allows the data signal output of the transmitter oscillator to reach the transmitter telephone line. The relay is operated by transistor Q2 and its associated circuitry shown in Fig. 6. When relay BC is released, diode CR1 prevents generation of large induced voltages. Diode CR2 prevents appearance of voltages greater than –6 on the base of transistor Q2.

E. Receiver Input Circuit

3.14 Refer to Fig. 4 for a schematic diagram of the receiver input circuit. The incoming

signal appears across terminals 20 and 8 (Fig. 4). Varistors RV1, RV2, and RV3 provide lightning protection for the receiver, and limit the surge voltage to 1.8 volts peak. Resistor R13 limits the surge current. Capacitor C4 prevents dc from flowing into transformer T1. The signal is coupled through C4, R13, and transformer T1. T1 matches the impedance of the line with the impedance of the data set. The signal then goes through either option V or option W, and appears at terminal 17 (Fig. 4).

F. Receiver AGC Amplifier

3.15 Refer to Fig. 7 for a schematic diagram of the receiver AGC amplifier. The incoming data signal appears between terminal 15 (Fig. 7) and the -18 volt supply. Resistor R1 terminates the input transformer so that the correct impedance is reflected to the line. Capacitor C1 and resistor R2 couple the signal to the junction of diodes CR1 and CR2. Capacitor C2 couples the signal to the base of transistor Q1. Resistors R3 and R4 set the base bias for transistor Q1. Resistors R7 and R8 limit the emitter current of Q1. Capacitor C7 bypasses resistor R7 at signal frequencies. The collector current for Q1 is furnished through R9 and R13. Power supply ripple and noise are decoupled by capacitor C3. The signal is coupled to the base of Q2 through capacitor C8 and resistor R10. Base bias for Q2 is set by R11 and R12. Emitter current flows through R15 which is bypassed by C9 at signal frequencies. This current also flows through R16 which is bypassed at the higher signal frequencies by capacitor C10. Resistor R14 couples the collector voltage back to the base, thereby lowering the output impedance of the stage and stabilizing the gain. Capacitor C11 at the collector of Q2 couples the amplifier output to the band separation filter input. The low channel output of this filter is fed through C13 and R23 to the base of the return amplifier (transistor Q3). Resistors R22 and R24 furnish base bias for Q3. Resistor R20 stabilizes the gain of the stage. The returned signal is fed through capacitor C6 to the peak-detecting rectifier consisting of diodes CR3 and CR4 and capacitor C5. Resistor R6 feeds the direct current to the gain-regulating diodes CR2 and CR1. Capacitor C4 prevents signal leakage back through the diodes. Resistor R5 prevents distortion of the initial part of the signal by charging capacitor C4 in the steady state.

3.16 The voltage feedback from the output of the band separation filter reduces the amplitude of the signal input, thereby providing automatic gain control. The AGC attack time is determined by the charging rate of C5. Approximately 20 msec are required for adjusting the gain to within 25 percent of its final value. The AGC release time is determined by the discharge time constant of C5 and R6. With a large signal input, the amplifier reaches half of its maximum gain about 300 msec after the signal is removed.

G. Band Separation Filter

3.17 The band separation filter (network 637B) consists of one low-pass, one bandpass, and one high-pass filter with common input terminals. These filters separate the signal into three frequency bands. The common input is fed by the output of the AGC amplifier. The output of the low-pass filter is connected to amplifier stage Q4A and is used to control the AGC amplifier through stage Q3. The bandpass filter is coupled to the amplifier stage Q4B. The output of the high-pass filter feeds amplifier stage Q4C and is used only in connection with the static remote testing of the data set. A valid signal has one frequency component in the low-pass band, and one frequency component in the bandpass band at any given time.

H. Receiver Channel Amplifiers and Limiters

3.18 Refer to Fig. 7 for a schematic diagram of the amplifiers and limiters. The output of the low-pass part of the band separation filter is applied to the base of transistor Q4A through capacitor C14A and resistor R25A. Resistors R26A and R27A furnish base bias for this stage, and R27A stabilizes the gain. The signal is coupled to the next stage by capacitor C15A and resistor R29A. The next stage, transistor Q5A, acts as a limiter to insure that the same amplitude is placed on all detectors. Resistors R30A and R31A furnish base bias. Resistor R33A furnishes emitter current and stabilizes the gain of the limiter. Large positive input voltages cause current to flow to ground through CR5A, and cause Q5A to be cut off. Negative voltages drive Q5A into saturation. For signal amplitudes within the expected range, the resultant limiter output appears as a square wave of approximately 30 volts peak-to-peak amplitude. Capacitor C16 couples the limiter output to its associated detectors. The amplifier-limiter circuits with B and C component designations drive the

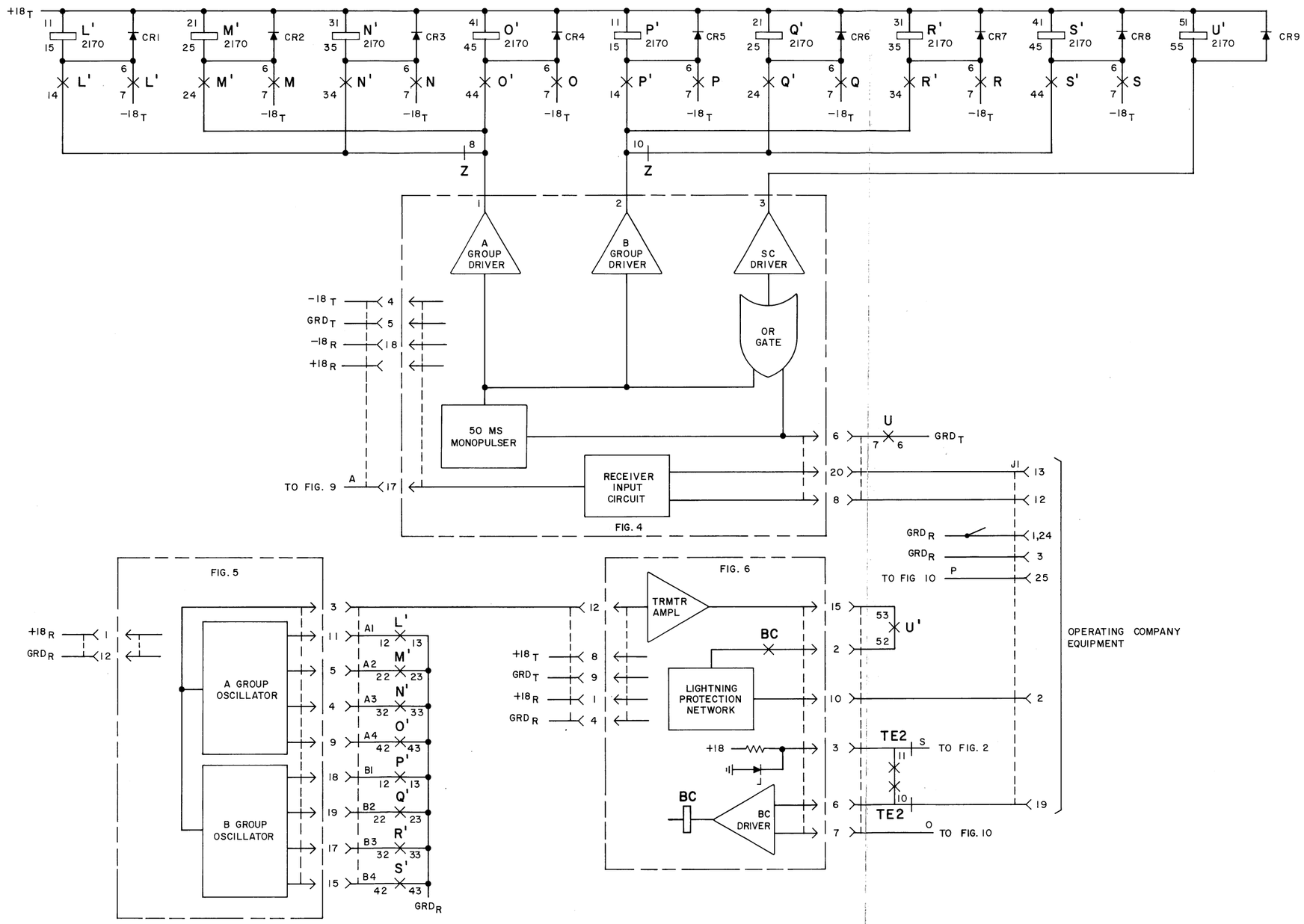

Fig. 4—Transmitter Input and Control Circuits

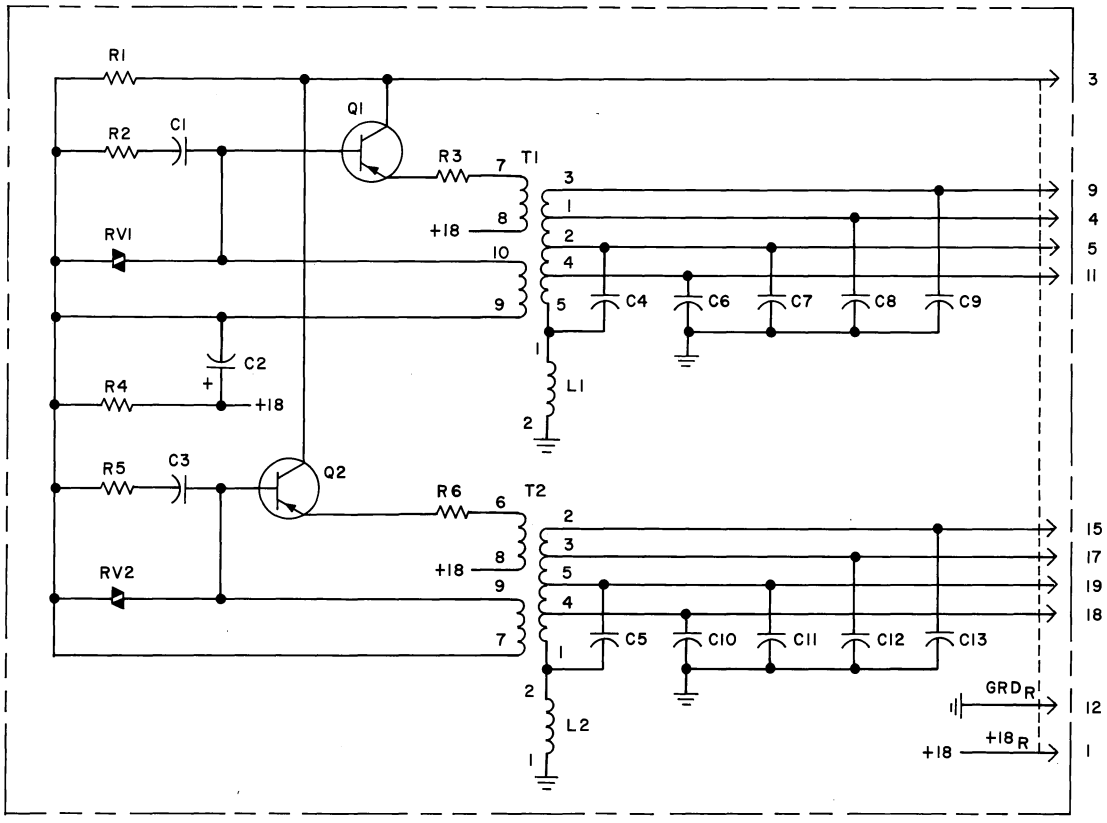

Fig. 5—A and B Group Oscillators

middle- and high-channel detectors, respectively, and operate in a manner similar to the amplifier-limiter previously described.

I. Receiver Detectors

3.19 Transistor Q6 (Fig. 7) acts as an emitter-follower and furnishes a threshold voltage for operation of the detectors. Its base is set by resistors R34 and R35 at 15.6 volts. Capacitor C18 lowers the impedance of the emitter circuit at signal frequencies. Because of the small base-to-emitter voltage drop, terminal 7 (Fig. 7) supplies approximately 15.7 volts to the detectors.

3.20 Refer to Fig. 8 for a schematic diagram of a typical receiver detector. This description of operation is referenced to Fig. 8 only. The operation of the other detectors is similar except that each is sensitive to a different frequency. Refer to Fig. 9 for a functional diagram showing the interconnection of the receiver detectors.

3.21 The emitter circuit of transistor Q1 is powered by +15.7 volts from terminal 15. This terminal connects to the +15.7 volts at terminal 7 (Fig. 7) as described in 3.19. The voltage on tuned circuit Z1 swings above and below +18 volts. When the voltage drops below +15.7 volts, transistor Q1 conducts. The collector current from Q1 charges capacitor C3. During most of this cycle, transistor Q3 is cut off and C3 discharges through resistors R6 and R7. The voltage across C3 is fed through the voltage divider composed of R6 and R7 to the base of transistor Q2. The emitter of Q2 is held at +1.2 volts by the network consisting of RV1, RV2, and R17. When the voltage presented to the base of Q2 goes above +1.2 volts, the transistor conducts, causing current to flow through relay K1A. Connection is made from the A Common to the A1 lead (terminals 18 and 1 of Fig. 8) through relay contacts 2 and 3 of relay K1A. The current in relay K1A causes the voltage at the collector of Q2 to decrease toward +2 volts. This change in voltage is applied to the voltage divider, consisting of R3 and R4, and appears reduced at the terminals of the tuned circuit. This signal feedback aids

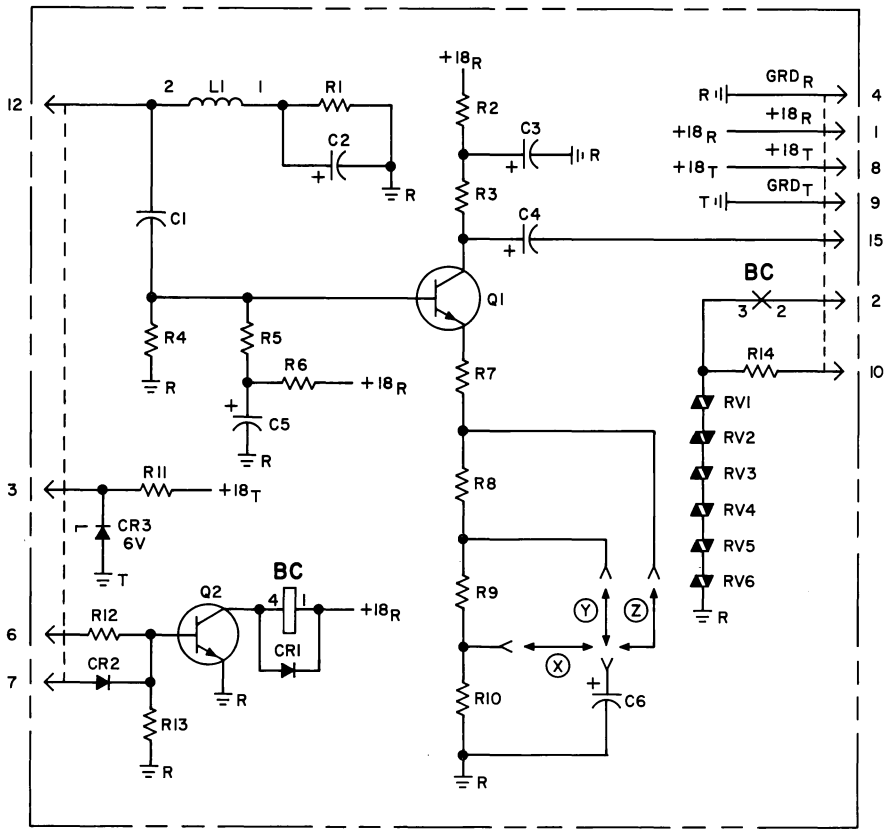

Fig. 6—Transmitter Amplifier and BC Relay

the incoming signal and causes more positive operation of the detector. The feedback signal cannot exceed the detector threshold by itself.

3.22 When the signal ceases, the voltage on the tuned circuit diminishes and no longer exceeds the bias threshold; therefore, Q1 no longer conducts. This allows C3 to discharge completely through R6 and R7. Zero voltage is then presented to Q2, thus causing it to cut off. Without collector current from Q2 in the coil, relay K1A returns to its normal state, breaking contact between the A Common and A1 leads. The collector of Q2 returns to +18 volts, and the bias no longer exists on the tuned circuit.

J. Receiver Output Circuit

3.23 Refer to Fig. 3 and Fig. 10 for schematic diagrams of the receiver output circuit. Assume that a data signal consisting of a 697-Hz component and a 1209-Hz component is present. Due to the relay action described in 3.21, relay K1A (Fig. 8) and relay K1B (Fig. 9) provide a path for -18 volts to terminals 18 and 19 (Fig. 10). The voltages will cause the AND gate to be triggered. The output of the AND gate passes through the integrator and triggers the 40-msec monopulser which operates relay T for 40 msec.

3.24 When relay T operates, a +18 voltage is placed on terminal 1 (Fig. 10). This voltage causes the A and F relays to operate and remain operated for the duration of T relay operation. If relays K1A and K1B open before the T relay releases, the path from -18 volts through contacts in the A and F relays causes these relays to remain operated. When T relay releases, relays A and F open. When relay A is operated, relay B, C, or D cannot operate because break contacts 6 and 8 of the A relay prevent +18 volts from reaching relays B, C, or D. A similar action occurs to prevent relays H, J, and K from operating when relay F is operated.

3.25 When the relays are not operated, a path does not exist between terminals 6 and 11 (Fig. 10). When relays A and F operate, a path

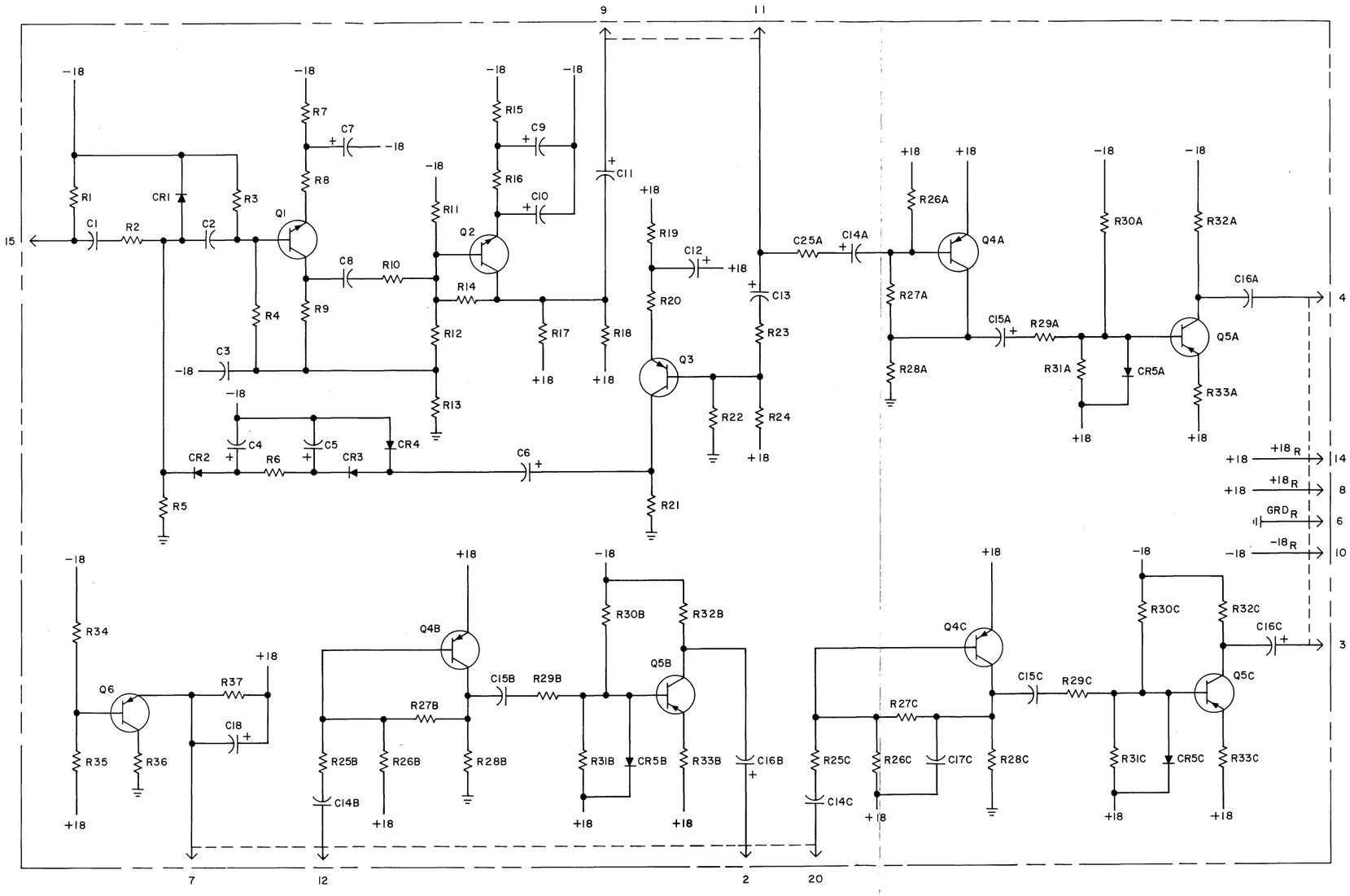

Fig. 7—AGC and Line Limiter

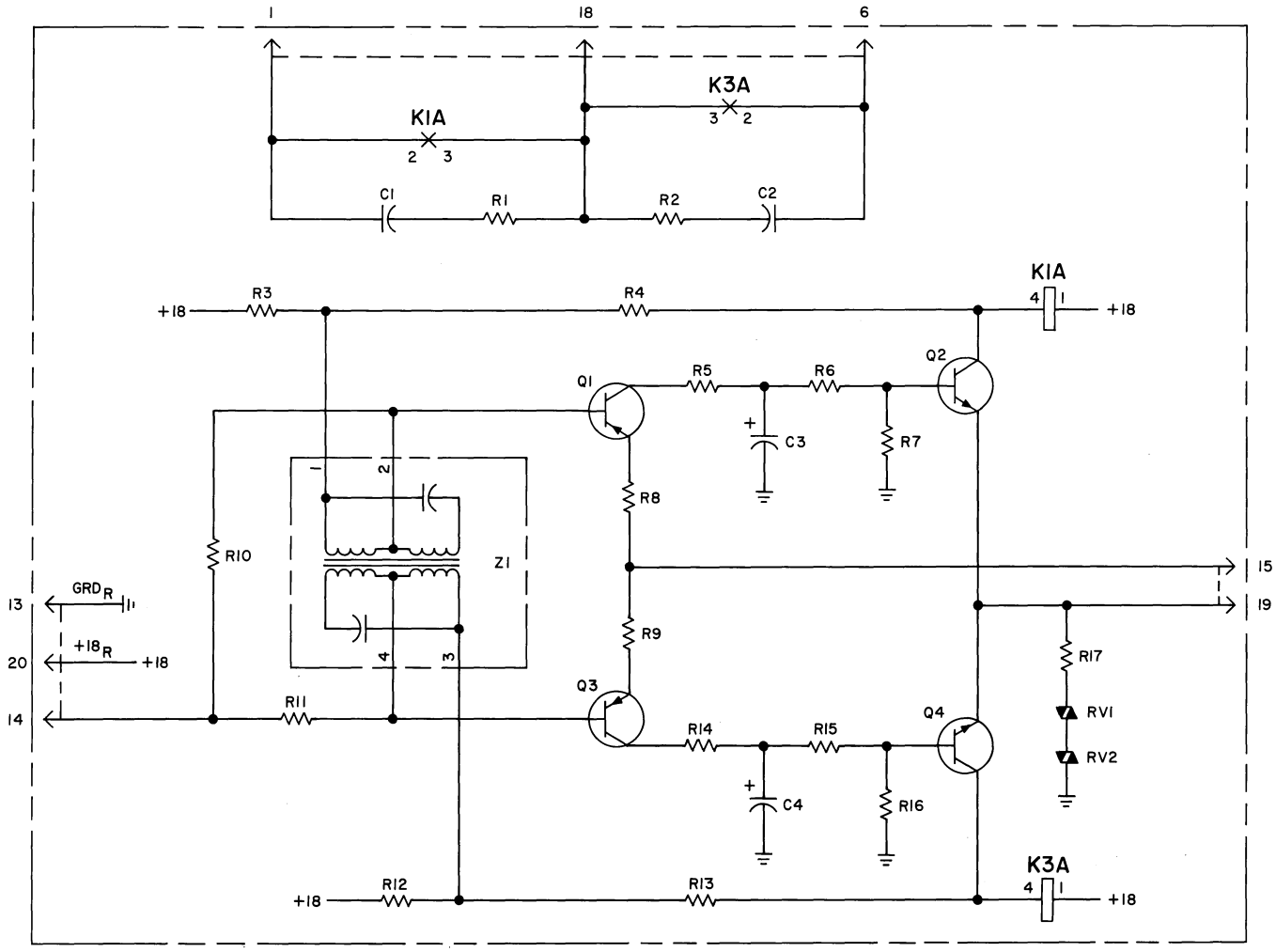

Fig. 8—Detector Circuit

is provided through relay contacts to connect terminals 6 and 11. These terminals connect to the relay matrix as shown in Fig. 10 and explained in 3.06.

3.26 In the quiescent state, voltage is not applied to terminals 11 and 16 (Fig. 2). When relays A and F are operated, current from the +18 volt supply flows through the relay contacts and Zener diodes. When the voltage at the diodes exceeds the reverse breakdown point, a +6 volt potential is placed on terminals 11 and 16 of the output interface circuit. This voltage will be present as long as relays A and F remain operated. Similar operation occurs for relays B, C, and D, or relays H, J, and K.

K. Remote Testing Circuits

3.27 For a schematic diagram of the remote testing circuits, refer to Fig. 2, Fig. 10, and Fig. 11. Transistor Q6, diodes CR5, CR6, and CR7, varistor RV4 and the associated circuit components as shown in Fig. 11 make up the remote test driver which operates relay TE1 (Fig. 10). The interconnection between these circuits and the other circuits is shown in Fig. 10.

3.28 To place the data set in the remote test mode, a +6 voltage is applied to terminal 5 (Fig. 11) through R13 to the base of transistor Q6. This voltage turns on the transistor. Current flows from the +18 volt supply through R15 to terminal 9. As shown in Fig. 10, relay TE1 is

connected from terminal 8 to terminal 9 of the TE relay driver circuit. When transistor Q6 is turned on, relay TE1 operates. Diode CR7 is a current limiter for protecting transistor Q6. To open the TE1 relay, a -6 volt potential is supplied to terminal 5. This turns transistor Q6 off and stops the current from flowing to relay TE1.

3.29 When relay TE1 is operated, the contacts provide a path for -18 volts to operate relays TE2 and TE3. When relay TE2 is operated, a positive voltage appears at terminal 6 (Fig. 6). Refer to 3.13 for operation of the BC relay. Relays TE1 and TE2 disconnect the receiver output and transmitter input from the customer equipment and connect the transmitter input to the receiver output (Fig. 2). Relay TE3 grounds one side of the coil of relays L, M, N, O, P, Q, R, S, and U.

3.30 This procedure allows for remote testing of the data set. When two of relays A, B, C, D, F, H, J, or K are operated, the voltages produced by the relay operation are coupled by TE1 and TE2 to the transmitter input. These voltages operate two corresponding relays of L, M, N, O, P, Q, R, or S, thereby operating the transmitter.

3.31 To place the data set in the static remote test mode, the set must first be placed in the remote test mode. This operates relay TE3 whose contact is in series with relay Z. When a signal containing a 2050-Hz component is received by the data set, relay K1C (Fig. 9) will be operated. This relay operation connects lead M to N (Fig. 10) and places ground on one side of relay Z, thereby causing it to operate. Contact 1 of the Z relay shorts terminals 6 and 11 (Fig. 10), thus bypassing the relay matrix.

3.32 Contact 2 of the Z relay applies +18 volts to terminal 1 (Fig. 11). This bypasses relay T and allows one of relays A, B, C, D, F, H, J, or K to operate whenever a -18 voltage is applied to the other side of this relay. The relay will remain operated as long as this voltage is applied to the coil.

L. Installation Testing Circuit

3.33 Refer to Fig. 12 for a schematic diagram of the installation testing circuit. Resistors R16 and R17 (Fig. 4) form a 10-dB pad for a signal from terminals 2 and 3 on J1 to terminals 12 and 13 on J1. This circuit loops the transmitter telephone line to the receiver telephone line through the 10-dB pad. Switch S1 connects +18 volts to either pin 19 or 25 on J1. In the LOCAL test position, a +18 voltage connects to pin 19 on J1, thus operating the BC relay (3.13). When S1 is in the REMOTE test position, a +18 voltage connects to pin 25 on J1, thus operating the TE relay (3.28). Resistor R18 (Fig. 4) limits current flow from the +18 volt supply during the installation test.

4. TESTING PROCEDURES

4.01 The following test procedures do not cover all the trouble possibilities for Data Set 404A. The tests are designed to verify that the Data Set 404A does meet operating requirements.

4.02 The following test equipment or the equivalent is required:

1—535 Tektronix Oscilloscope

1—Ballantine True RMS Voltmeter Model 320-S1

1—Hewlett Packard 5212A Electronic Counter

1—Hewlett Packard 302A Wave Analyzer

1—General Radio 1450 TB Decade Attenuator

1—KS-14510 Volt-Ohm-Milliammeter

1—Krohn-Hite 440A Oscillator

Note: If a substitute is used, it must have a range of 0.2 to 25 Hz with an amplitude capable of operating a 303H interrupting relay. The relay contact should be closed for half of each cycle of the oscillator and open for the other half.

3—Muirhead D-695-A/100 Oscillators

Note: If substitutes are used, they must cover the frequency range of 500 to 2400 Hz. Each must be calibrated within ±1 Hz over this range.

1—Harrison Labs 800A-2 Twin Low Voltage Power Supply

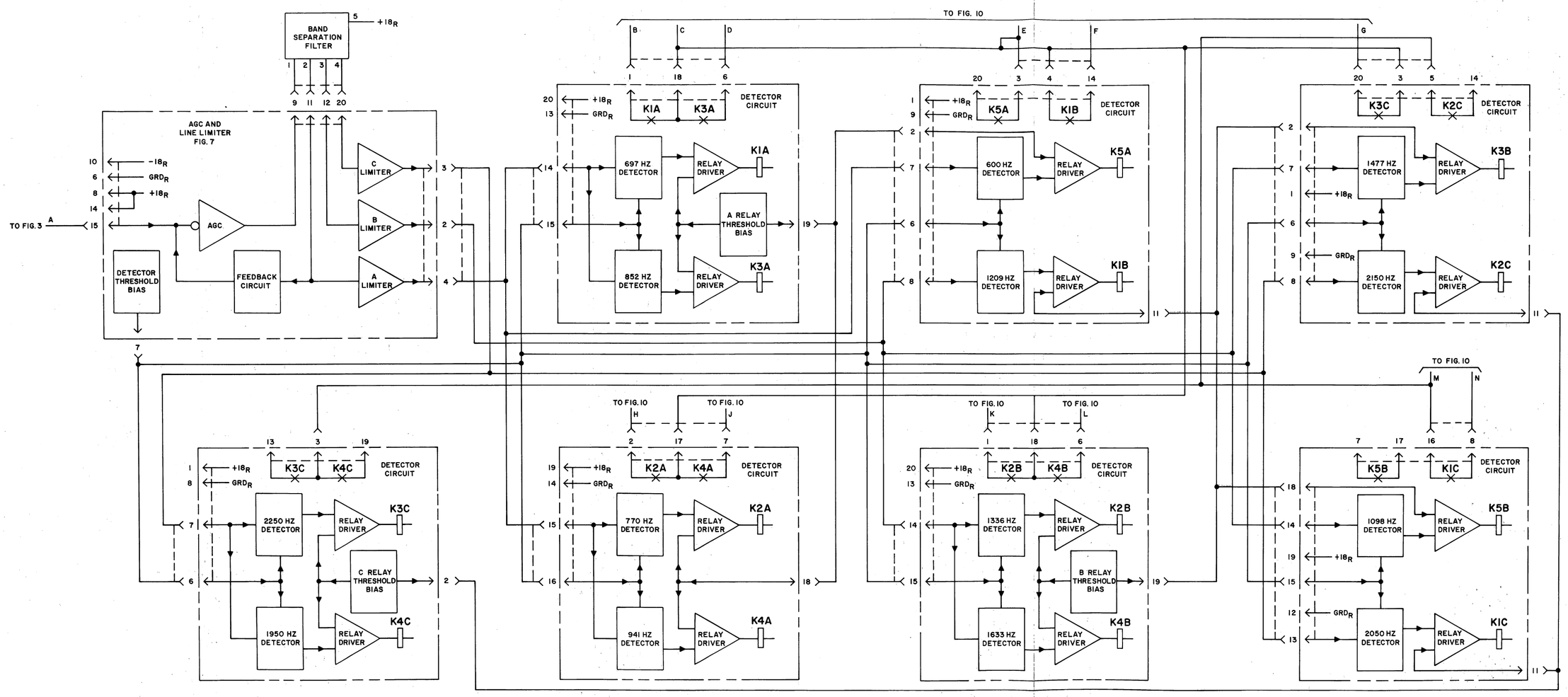

Fig. 9—Interconnections of Detector Circuits

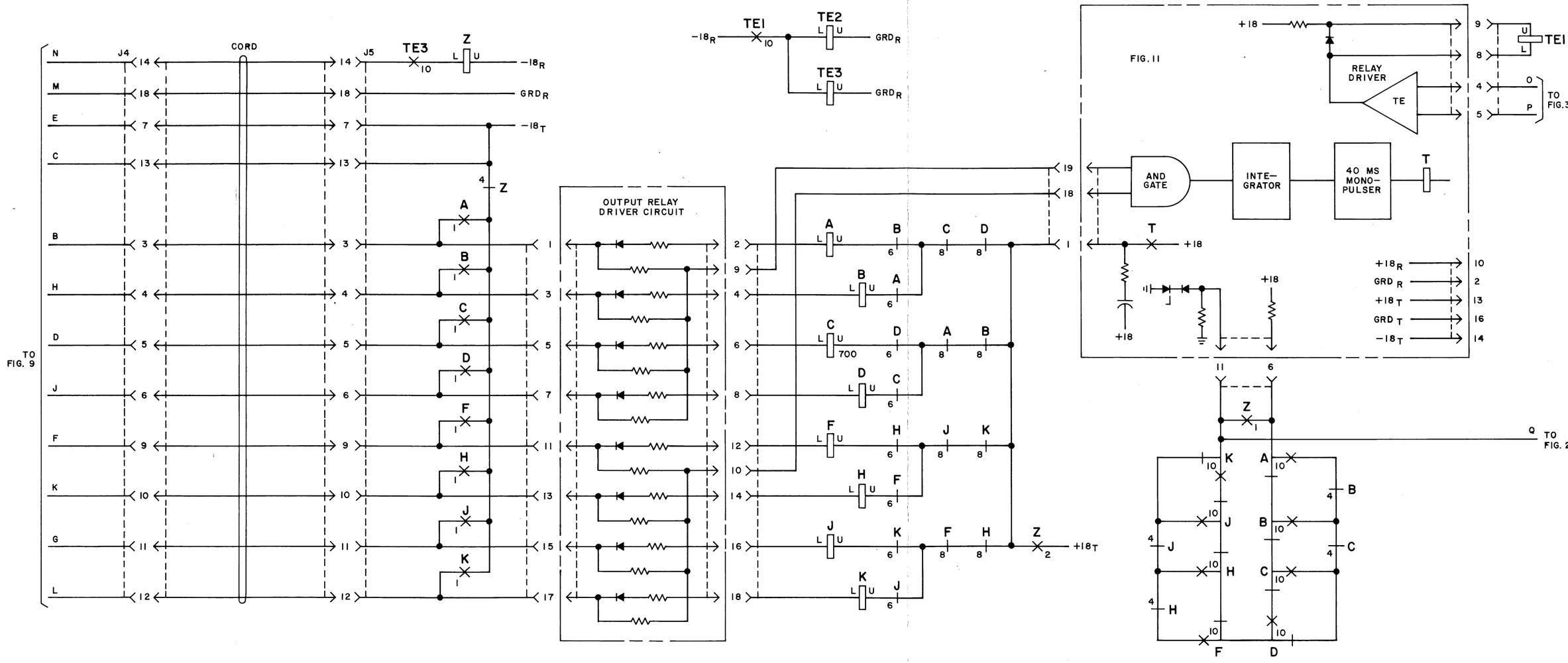

Fig. 10—Relay Interconnections Circuit

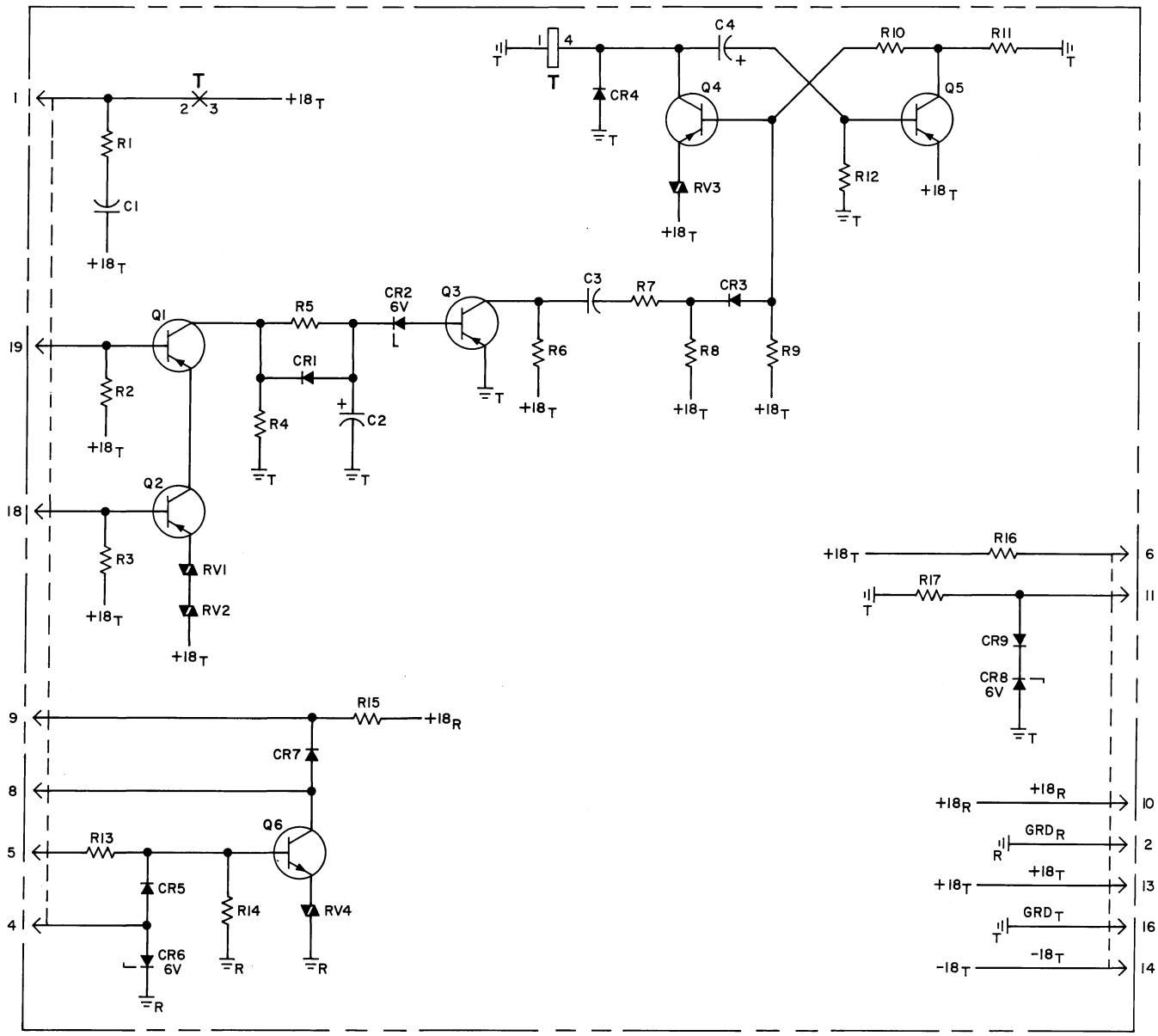

Fig. 11—AND Gate, Output Timer and TE Relay Driver

4.03 The following tests should be performed with power ON unless otherwise stated. Tests are made at the rear of the data set.

Caution: A factory-installed chassis ground strap has been placed between E1 on the chassis and ground (grd R). Before installation testing, verify that this strap is connected. After testing is completed, remove this strap. If the data set requires further testing, or if the data set is tested at a later date, disconnect the ac power at the data set and connect plug P1 to J1. There is a shock hazard in the Data Set 404A when the power is ON and plug P1 is not connected to J1.

A. Power Test

4.04 To check the positive, negative, and ground points, proceed as follows:

(a) Using a voltmeter with a high impedance (greater than 10K ohms) and with a 200

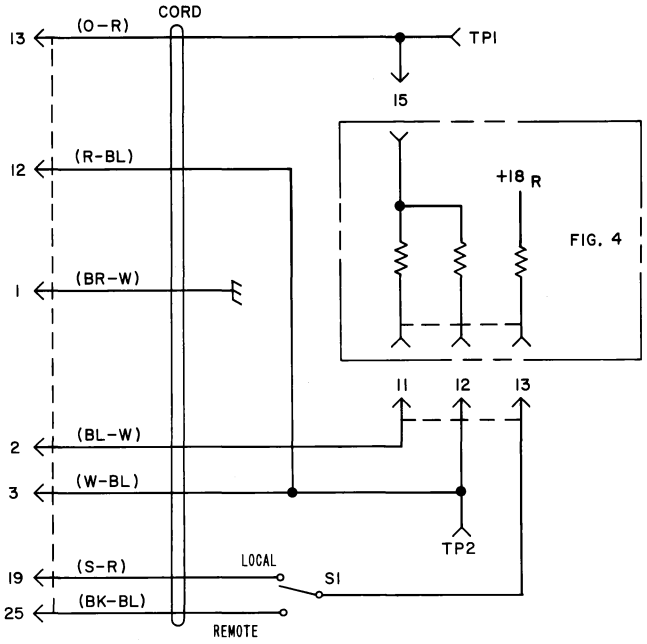

Fig. 12—Installation Testing Circuit

(±5) ohm, 3-watt resistor across the probe, check all plug-in boards. Verify the following conditions:

- GRD$_R$ points must be at the same potential as the G terminal of the R power supply.
- +18$_R$ points must be +18 (±1) volt with respect to GRD$_R$.
- -18$_R$ points must be -18 (±1) volt with respect to GRD$_R$.

(b) Using the same voltmeter as above, but using a 102 (±5) ohm, 3-watt resistor instead of the 200-ohm resistor, check all plug-in boards. Verify the following conditions:

- GRD$_T$ points must be at the potential of the G terminal of the T power supply.
- +18$_T$ points must be +18 (±1) volt with respect to GRD$_T$.
- -18$_T$ points must be -18 (±1) volt with respect to GRD$_T$.

4.05 If the above requirements are not met, remove all plug-in boards and conduct the following tests:

(a) Connect a 102 (±5) ohm, 3-watt resistor from GRD$_R$ to +18$_R$. A voltage reading between these two points should be +18 (±0.5) volts with respect to GRD$_R$.

(b) Connect a 102 (±5) ohm, 3-watt resistor from GRDR to -18R. A voltage reading between these two points should be -18 (±0.5) volts.

(c) Repeat for the T power supply.

B. Transmitter Tests

4.06 With all switches of the circuit open, connect test equipment to the data set as shown in Fig. 13 and Fig. 14. Signals should not be seen on the oscilloscope at this time.

(a) Close S12; oscillations should not be present.

(b) Close S11; oscillations should be present.

(c) Open S12; oscillations should not be present.

(d) Close S5, S8, and S12; a 600-Hz signal should be present.

Note: Tune T1 of CP AS63 (Fig. 5) to 600 (±1) Hz. Check the scope and electronic counter for results.

(e) Close S4; a 941-Hz signal should be present.

Note: Tune L1 of CP AS63 (Fig. 5) to 941 (±1) Hz.

(f) Open S4 and close S3; an 852 (±2) Hz signal should be present.

(g) Open S3 and close S2; a 772 (±2) Hz signal should be present.

(h) Open S2 and close S1; a 697 (±2) Hz signal should be present.

Note: Readjust T1 and L1 of CP AS63 (Fig. 5) in order to bring all frequencies within ±2 Hz of the stated frequencies.

(l) Open S5 and S8 and close S4; a 1098-Hz signal should be present.

Note: Tune T2 of CP AS63 (Fig. 5) to 1098 (±1) Hz.

(j) Close S8; a 1633-Hz signal should be present.

Note: Tune L2 of CP AS63 (Fig. 5) to 1633 (±1) Hz.

(k) Open S8 and close S7; a 1477 (±3) Hz signal should be present.

(l) Open S7 and close S6; a 1336 (±3) Hz signal should be present.

(m) Open S6 and close S5; a 1209 (±3) Hz signal should be present.

Note: Readjust T2 and L2 of CP AS63 (Fig. 5) in order to bring all frequencies within ±3 Hz of stated frequencies.

(n) Open S1 and S4.

(o) Remove the option strap from CP AS61 (Fig. 6).

(p) Operate S1; observe a signal level of -9 (±1) dBm on the voltmeter.

(q) Place the strap for option X on CP AS61 (Fig. 6); observe a level of -6 (±1) dBm.

(r) Place the strap for option Y on CP AS61 (Fig. 6); observe a level of -3 (±1) dBm.

(s) Place the strap for option Z; observe a level of 0 (±1) dBm.

(t) Open S1; set the oscillator to 15 (±1) Hz.

(u) Connect the external trigger of the scope to terminal 1 of the oscillator and sync the scope with the oscillator.

(v) Set the time base to 10 msec/cm.

(w) Close S10; observe a signal duration on the scope for 50 (±5) msec.

(x) Open all switches; return the set to normal.

C. Receiver Detector Tests

4.07 With all switches of the 404A test circuit open, connect the test equipment to the data set as shown in Fig. 13 and Fig. 14.

Note: A regular output indication as seen on the scope is a single interval of +60 (±0.6) volts for each pulse of input signal. This interview must be 40 (±5) msec in duration.

(a) Place straps for option V on CP AS62 (Fig. 4).

(b) Using the scope, measure the voltage at terminals A1, A2, A3, A4, B1, B2, B3, B4, and CP of the 404A test circuit.

Requirement: 0 vdc

(c) Ground the 1000-ohm resistor at the output terminals of oscillator No. 1.

(d) Adjust the output level of oscillator No. 2 to -12 (±1) dBm.

(e) Remove the ground from oscillator No. 1 and ground the 1000-ohm resistor to the output terminals of oscillator No. 2.

(f) Adjust the output level of oscillator No. 1 to -12 (±1) dBm.

(g) Remove the ground from oscillator No. 2 and set the scope in the chopped mode.

(h) Set the scope time base to 10 msec/cm.

(i) Set oscillator No. 1 to the nominal frequency corresponding to detector A1 (Table A).

(j) Set oscillator No. 2 to 1336 (±10) Hz when testing detectors A1 through A4.

(k) Set Krohn-Hite oscillator to 10 (±5) Hz.

(l) Place the A channel probe of the scope to the terminal of the 404A test circuit corresponding with the detector to be tested (Table A).

(m) Place the B channel probe of the scope to terminal 7 of the 404A test circuit.

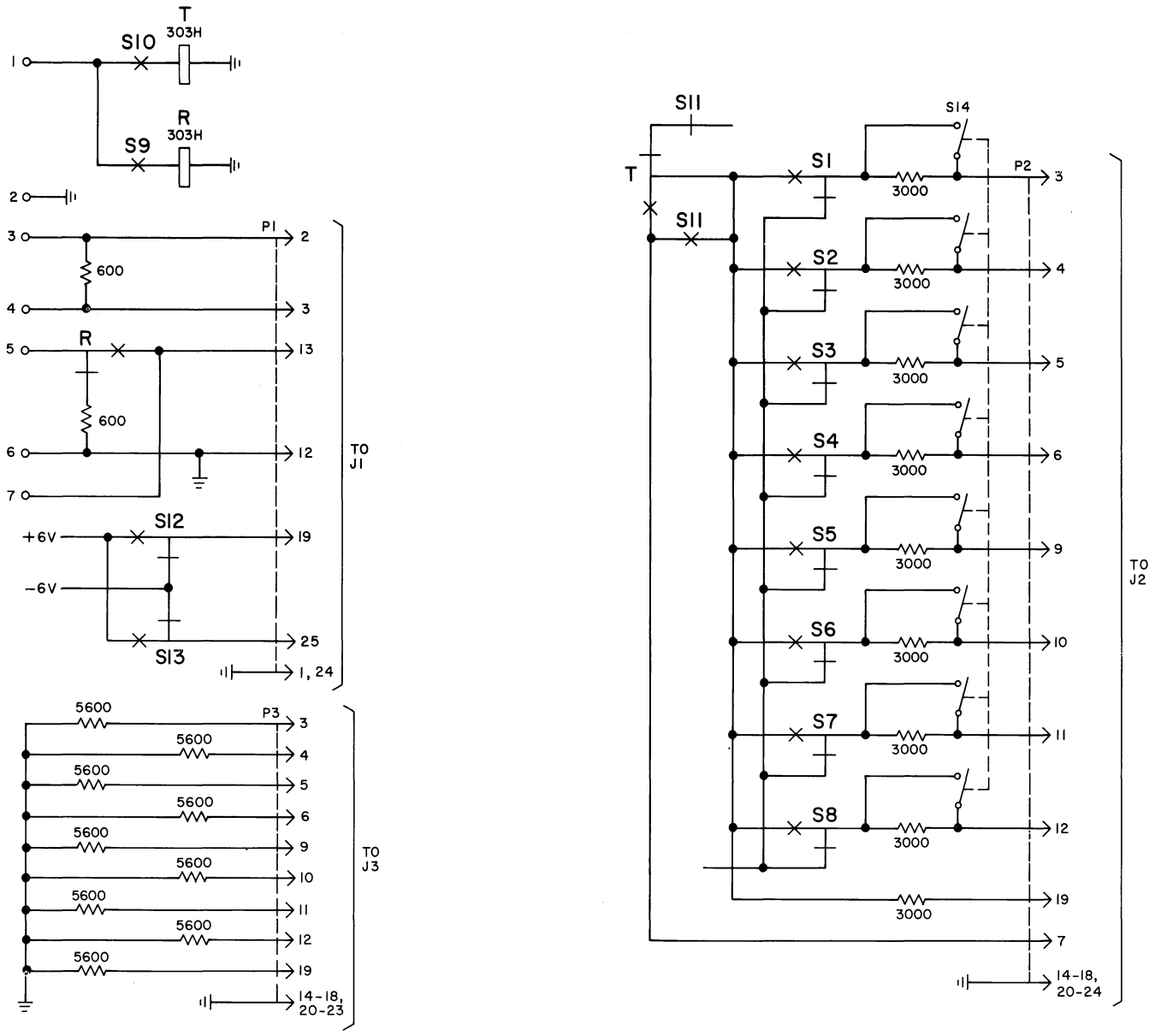

Fig. 13—Data Set 404A, Transmitter-Receiver Test Circuit

(n) Connect the external trigger to terminal 1 of the 404A test circuit.

(o) Sync the scope with the output of the Krohn-Hite oscillator.

(p) Close S14. The time delay between input and output indications must be within 20 to 32 msec. Verify that there are output indications at the CP terminal.

(q) Slowly decrease the frequency of oscillator No. 1 until the regular output indications disappear. Then slowly increase the frequency until regular indications reappear. The frequency at which the regular output first reappears must be within the limits specified under f (LOW) in Table A.

(r) Slowly increase the frequency of oscillator No. 1 from the nominal value until the regular indications disappear. Slowly increase

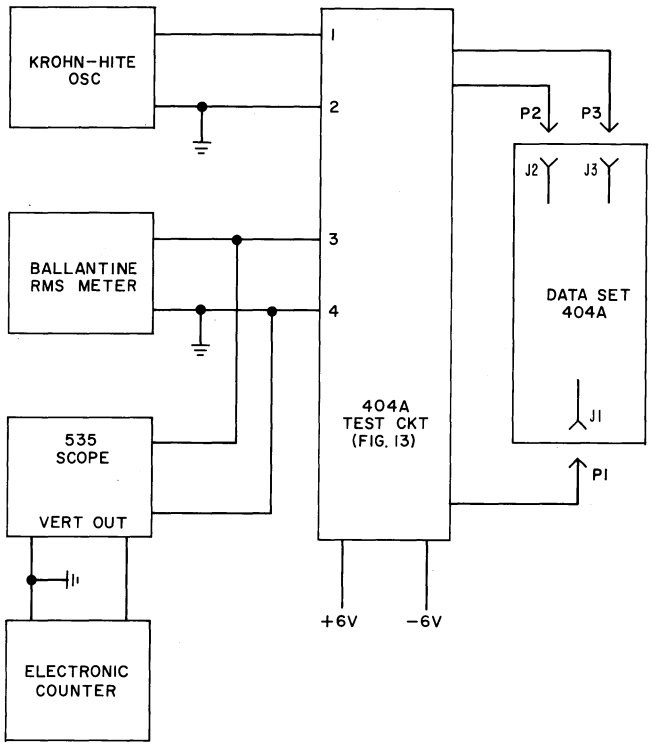

Fig. 14—Transmitter Test Setup

the frequency until regular indications reappear. These frequency limits are given in Table A under f (HIGH).

Note: Repeat steps (i) through (r) for detectors A2, A3, and A4.

(s) Set oscillator No. 2 to 770 (±10) Hz when testing detectors B1 through B4.

Note: Repeat steps (i) through (r) for detectors B1 through B4 at the nominal frequency for each one (Table A).

(t) Set oscillator No. 1 to 770 (±10) Hz.

(u) Set oscillator No. 2 to 1633 (±3) Hz.

(v) Set the Krohn-Hite oscillator to 12 (±0.5) Hz.

(w) Set the scope in such a manner that at least ten output pulses appear on each trace; output pulses should not be missing for at least one trace or for approximately one second.

(x) Restore the circuit to normal unless the following test is to be made.

D. Receiver Sensitivity Tests

4.08 With all switches of the 404A test circuit open, connect test equipment to the data set as shown in Fig. 13 and Fig. 14.

TABLE A

DETECTOR BANDWIDTH SENSITIVITY

DETECTOR	NOMINAL	f (LOW)	f (HIGH)	SENSITIVITY IN DBM
A1	697	657-668	726-737	−38
A2	770	730-741	799-810	−38
A3	852	812-823	881-892	−38
A4	941	901-912	970-981	−38
B1*	1209	≤1176	≥1242	−39
B2*	1336	≤1303	≥1369	−40
B3*	1477	≤1444	≥1510	−40
B4*	1633	≤1666	≥1666	−41

* The upper limit for f (LOW) and the lower limit for f (HIGH) are given explicitly. The difference between the upper and lower operating frequencies measured in this test must be no greater than 88 Hz.

(a) Place straps for option W on CP AS62 (Fig. 4).

(b) Ground the 1000-ohm resistor at the output terminal of oscillator No. 1.

(c) Adjust the signal level of oscillator No. 2 to -38 (±0.5) dBm on the voltmeter.

(d) Remove ground from oscillator No. 1 and ground the 1000-ohm resistor to the output of oscillator No. 2.

(e) Adjust the output of oscillator No. 1 to -40 (±0.5) dBm.

(f) Remove the ground from oscillator No. 2.

(g) Set the Krohn-Hite oscillator to 10 (±0.5) Hz.

(h) Set oscillator No. 1 to the nominal frequency ±1.0 Hz corresponding to detector A1 (Table A).

(i) Set oscillator No. 2 to 1336 (±1.0) Hz when testing detectors A1 through A4.

(j) Close S14. Observe regular indications on the output terminals corresponding to the nominal frequency of the circuit under test.

(k) Open switch S14.

Note: Repeat steps (h) through (k) for detector circuits A2 through A4.

(l) Set oscillator No. 2 to 770 (±1.0) Hz with an output level of -38 (±0.5) dBm when testing detectors B1 through B4.

(m) Repeat steps (j) and (k) for detectors B1 through B4.

(n) Restore the circuit to normal, unless the following test is to be made.

E. Receiver AGC Test

4.09 With all switches of the test circuit open, connect the test equipment to the data set as shown in Fig. 13 and Fig. 14.

(a) Place straps for option V on CP AS62 (Fig. 4).

(b) Adjust oscillator No. 1 to zero output.

(c) Adjust oscillator No. 2 to 770 (±10) Hz with a level of -10 (±1) dBm on the voltmeter.

(d) Set the Krohn-Hite oscillator to 0.3 (±0.05) Hz.

(e) Close switch S14.

(f) Place the scope probe to terminal 1 of the band separation filter (Fig. 9). Observe the time duration from the beginning of the signal until the amplitude drops to 0.45 (±0.05) volts peak-to-peak. This time duration must not be greater than 20 msec.

(g) Set the Krohn-Hite oscillator to 2.5 (±0.1) Hz. Verify that the ratio of the amplitude transient to the steady state is 2.5 (±0.25).

(h) Open Switch S14.

(i) Disconnect the Krohn-Hite oscillator from terminal 1 of the test circuit.

(j) Connect +6 volts to terminal 1 of the test circuit.

(k) Close switch S14.

(l) Connect the Hewlett-Packard wave analyzer to the vertical output terminal of the scope. The second harmonic content of the wave form must be 22 dB or more below the level of the fundamental frequency (770 Hz).

(m) Restore the circuit to normal.

F. Transmitter-Receiver Remote Test

4.10 With all switches of the test circuit open, connect the test equipment to the data set as shown in Fig. 13 and Fig. 15.

(a) Ground the output of oscillators No. 1 and No. 2.

(b) Set the output level of oscillator No. 3 to -10 (±1) dBm as a frequency of 600 (±10) Hz.

(c) Remove the ground from oscillator No. 2 and ground the output of oscillators No. 1 and No. 3.

(d) Set the output level of oscillator No. 2 to -10 (±1) dBm at a frequency of 1555 (±10) Hz.

(e) Remove the ground from oscillator No. 1 and ground the output of oscillators No. 2 and No. 3.

(f) Set the output level of oscillator No. 1 to -10 (±1) dBm at a frequency of 1900 (±10) Hz.

(g) Remove the ground from oscillators No. 2 and No. 3.

(h) Close switches S13 and S14.

(i) Sweep oscillator No. 1 upward in frequency until a steady output is seen on the scope. This frequency must be less than or equal to 2017 Hz.

(j) Continue to sweep oscillator upward in frequency until the indication is no longer seen on the scope.

(k) Sweep the oscillator downward in frequency until the indication reappears on the scope. This frequency must be greater than or equal to 2083 Hz.

Note: The difference between the upper and lower operating frequencies must not be more than 88 Hz.

(l) Repeat steps (a) through (k) substituting the oscillator frequencies shown in Table B. Observe the results on the scope.

(m) Open switch S14.

(n) Remove the +6 volt potential from terminal 1 of the test circuit.

(o) Connect the Krohn-Hite oscillator to terminal 1 of the test circuit. Set the frequency at 5 (±0.5) Hz.

(p) Set oscillator No. 1 at 1950 (±10) Hz.

(q) Set oscillator No. 2 at 941 (±10) Hz.

(r) Close S14; verify that the output signals as seen on the scope have a duration of 50 (±5) msec.

(s) Restore the circuit to normal.

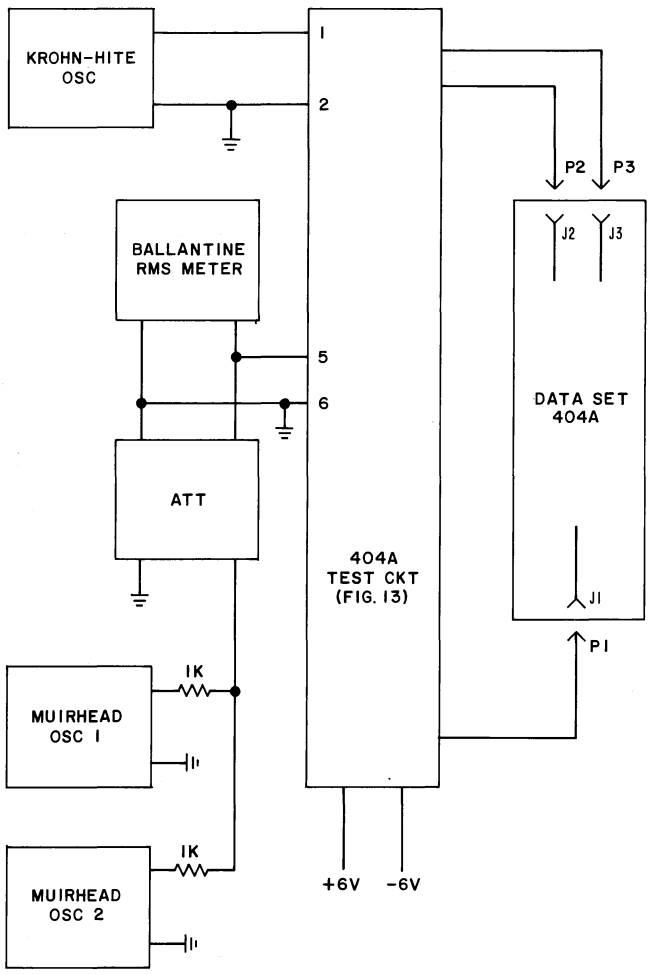

Fig. 15—Receiver Detector Sensitivity and Automatic Gain Control

G. Amplifier Circuit Board Test

4.11 Circuit pack CP AS50 must be removed from the data set in order to perform this test.

(a) Apply +18 (±0.5) volts, -18 (±0.5) volts to the proper terminals of the circuit pack (Fig. 7).

TABLE B

TRANSMITTER OUTPUT FREQUENCY CHECK

OSC 1	OSC 2	OSC 3	WAVE ANALYZER FREQUENCY	
2050*	1555*	697*	697*	1098*
2050*	1555*	770*	770*	1098*
2050*	1555*	852*	852*	1098*
2050*	1555*	941*	941*	1098*
2050*	1209*	600*	600*	1209*
2050*	1336*	600*	600*	1336*
2050*	1477*	600*	600*	1477*
2050*	1633*	600*	600*	1633*

* ±10 Hz

(b) Connect terminals 1, 2, 3, and 4 of a band separation filter to terminals 9, 10, 11, and 12 (Fig. 7), respectively. Connect +18 volts to terminal 5 of this filter.

(c) Place a 10,000-ohm (±1 percent) resistor between the +18 volt supply and each of terminals 2, 3, and 4.

(d) Place a 1210-ohm (±1 percent) resistor between terminals 15 and 10 of CP AS50.

(e) Place a 600-ohm (±1 percent) resistor across the output of a Muirhead oscillator. Set the output level to -6 (±0.2) dBm at 600 (±20) Hz.

(f) Remove the resistor and connect the oscillator to terminals 15 and 10 of CP AS50.

(g) Monitor terminal 9 with a wave analyzer. The fundamental component (600 Hz) should be 155 (±25) millivolts (mv). The second and third harmonic should be at least 20 dB below the fundamental.

(h) Place a 600-ohm (±1 percent) resistor across the output of the oscillator and set the level to -35 (±1) dBm at 600 (±20) Hz. Remove the resistor.

Note: For each level setting, it will be necessary to place the 600-ohm resistor across the output of the oscillator. This resistor must be removed after the level has been set.

(i) Check the rms voltage at terminal 9.

Requirement: 67 (±17) mv

(j) Monitor the level of the fundamental frequency at terminal 4 with the wave analyzer.

Requirement: Not greater than 11.8 volts rms

(k) Reduce the input to -47.5 (±0.5) dBm. Monitor the level of the fundamental frequency at terminal 4.

Requirement: More than 11.2 volts rms

(l) Set the input at -40 (±1.0) dBm at 1350 (±20) Hz. Monitor the level of the fundamental frequency at terminal 2.

Requirement: More than 12.3 volts rms

(m) Reduce the input to -49.5 (±0.5) dBm. Monitor the level of the fundamental frequency at terminal 2.

Requirement: More than 11.7 volts rms

(n) Set the input to -40 (±1.0) dBm at 2250 (±20) Hz. Monitor the level of the fundamental frequency at terminal 3.

Requirement: More than 12.6 volts rms

(o) Set the input to -54.5 (±0.5) dBm. Monitor the level of the fundamental frequency at terminal 3.

Requirement: More than 11.7 volts rms

(p) Measure the voltage at terminal 7.

Requirement: +15.6 (±0.1) volts.

H. Detector Circuit Board Test

4.12 The detector circuit boards must be removed from the data set prior to performing this test. Refer to Table C for the terminal connections to the detector circuit boards. Refer to Fig. 8 and Fig. 9 for a schematic diagram of the detector circuits. Figure 8 shows a typical detector circuit. For detailed schematic diagrams of the detector circuits, refer to SD-1D055-01.

(a) Place two 100A varistors and a 68-ohm resistor in series. Connect one end to ground and the other end to the emitter driver (Z designation in Table C).

(b) Apply +15.6 volts to terminal T.

(c) Set the oscillator to 10 (±1) Hz. Refer to Table D for signal input level and connection to input terminal Q.

(d) Connect a 1.5 volt battery through a 1000-ohm resistor to the input terminals given in Table D.

(e) Set the signal oscillator to the nominal frequency given in Table D.

(f) Slowly decrease the frequency from the nominal value until the regular indications disappear. Slowly retrace until they reappear. The frequency at which the regular indications reappear must be within limits specified in f (LOW) in Table D.

(g) Slowly increase the frequency from the nominal value until the regular indications disappear. Slowly retrace until they reappear. The frequency at which the regular indications reappear must be within limits specified in f (HIGH) in Table D.

(h) The output indication as seen on the scope is a single interval of ground potential for each pulse of input signal. This interval must be between 40 and 60 msec in duration.

(i) The positive going wave front of the output indication should return to +1 volt. The time it takes to return should be 0.5 (±0.2) msec.

(j) Restore to normal.

I. Output Interface Circuit Test

4.13 The circuit board must be removed from the data set in order to perform this test. With the board in the normal operating (vertical) position, the terminals should be counted from the bottom to the top.

TABLE C

VOLTAGE ARRANGEMENT FOR DETECTOR CP

TERMINAL DESIGNATION IN TEST	CIRCUIT BOARD						
	CP AS51	CP AS52	CP AS53	CP AS54	CP AS55	CP AS56	CP AS57
+18V	20	1	1	1	19	20	19
Ground	13	9	9	8	14	13	12
Z (Emitter Drive)		2, 11	2, 11		18		18, 11
T (Threshold)	15	6	6	6	16	15	15

TABLE D

DETECTOR BOARD BANDWIDTH AND LIMITER CHECK

CIRCUIT BOARD CP	BETWEEN OUTPUT TERMINALS	INPUT TERMINAL Q	SIGNAL INPUT LEVEL RMS VOLTS ±0.25 VOLT	OPERATE FREQUENCIES		
				f (LOW)	f (NOMINAL)	f (HIGH)
AS51	18-1	14	12.00	660-667	697	729-736
	18-6	14	12.00	815-822	852	884-891
AS55	17-2	15	12.00	733-740	770	802-809
	17-7	15	12.00	904-911	941	973-980
AS52	3-20	7	12.00	563-570	600	632-639
	4-14	8	12.95	≤1174	1209	≥1244
AS56	18-1	14	12.95	≤1301	1336	≥1371
	18-6	14	12.95	≤1598	1633	≥1668
AS53	20-3	7	12.95	≤1442	1477	≥1512
	5-14	8	13.55	≤2115	2150	≥2185
AS57	17-7	14	12.95	≤1063	1098	≥1133
	16-8	13	13.55	≤2015	2050	≥2085
AS54	3-13	7	13.55	≤2215	2250	≥2285
	3-19	7	13.55	≤1915	1950	≥1985

(a) Connect +18 (±0.5) volts to terminal 1, and terminal 12 to ground.

(b) Connect -18.0 (±0.5) volts to terminal 20.

(c) Using a dc voltmeter, measure the voltage with respect to ground at terminals 11, 13, 14, 15, 16, 17, 18, and 19.

Requirement: 0 volts

(d) Using a dc voltmeter, measure the voltage with respect to ground at terminals 3, 4, 5, 6, 7, 8, 9, and 10.

Requirement: +18 (±0.5) volts

(e) Short terminal 3 to terminal 11. Measure the voltage at terminal 11.

Requirement: +6.0 (±0.6) volts

(f) Remove the short.

(g) Short terminal 4 to terminal 13. Measure the voltage at terminal 13.

Requirement: +6.0 (±0.6) volts

(h) Remove the short.

(i) Short terminal 5 to terminal 14. Measure the voltage at terminal 14.

Requirement: +6.0 (±0.6) volts

(j) Remove the short.

(k) Short terminal 6 to terminal 15. Measure the voltage at terminal 15.

Requirement: +6.0 (±0.6) volts

(l) Remove the short.

(m) Short terminal 7 to terminal 16. Measure the voltage at terminal 16.

Requirement: +6.0 (±0.6) volts

(n) Remove the short.

(o) Short terminal 8 to terminal 18. Measure the voltage at terminal 18.

Requirement: +6.0 (±0.6) volts

(p) Remove the short.

(q) Short terminal 9 to terminal 17. Measure the voltage at terminal 17.

Requirement: +6.0 (±0.6) volts

(r) Remove the short.

(s) Short terminal 10 to terminal 19. Measure the voltage at terminal 19.

Requirement: +6.0 (±0.6) volts

(t) Remove the short. Restore the circuit board to normal.

J. Receiver Output Timer Circuit Board Test (CP AS59)

4.14 The circuit board must be removed from the data set prior to performing this test.

(a) Connect terminal 1 to ground through a 500-ohm 3-watt resistor.

(b) Connect a 20,000-ohm resistor to terminal 19.

(c) Connect a 20,000-ohm resistor to terminal 18.

(d) Connect a 500-ohm resistor between terminal 8 and terminal 9.

(e) Connect +18 (±0.5) volts to terminal 13 and terminal 10.

(f) Connect terminals 2 and 16 to ground.

(g) Connect -18 (±0.5) volts to terminal 14.

(h) Using a voltmeter, measure +18 (±0.5) volts at terminal 6, and 0 volts at terminal 11. Short terminal 6 to terminal 11. Measure +6.0 (±0.6) volts at terminal 6.

(i) Remove the short and connect the scope to terminal 1.

(j) Connect -18 (±0.5) volts through the 20,000-ohm resistor which is connected to pin 19 of CP AS59. An indication should not be seen on the scope.

(k) Remove the -18 volt source which is connected to terminal 19. Connect it to terminal 18 through the 20,000-ohm resistor. An indication should not be seen on the scope.

(l) With the -18 volt source connected to terminal 19, connect -18 (±0.5) volts to terminal 18 through the 20,000-ohm resistor. Observe a single output indication as shown in Fig. 16.

Note: The symbol "To" represents the time at which -18 volts are applied to point A.

(m) Remove the connections from terminals 18 and 19.

(n) Connect -18 (±0.5) volts to terminal 5; measure the voltage at terminals 4, 8, and 9.

Requirement: -6.0 (±0.6) volts at terminal 4

Requirement: +18 (±0.5) volts at terminals 8 and 9

(o) Remove -18 volts from terminal 5.

(p) Connect +6.0 (±0.5) volts to terminal 5; measure the voltage at terminals 4 and 8.

Requirement: 0 volt at terminal 4

Requirement: +1.0 (±0.2) volts at terminal 8

(q) Restore the circuit to normal.

K. Output Relay Driver Circuit Board Test (CP AS60)

4.15 The circuit board must be removed from the data set prior to performing this test.

(a) Set the KS-14510 meter to OHMS X 100. Measure the resistance between terminal 9 and terminals 1, 3, 5, and 7. Measure the

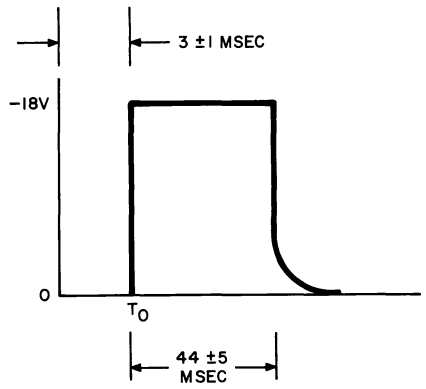

Fig. 16—Receiver Output Indication

resistance between terminal 10 and terminals 11, 13, 15, and 17.

Requirement: 19,600 (±1 percent) ohms

(b) Remove the meter probes and place a ground on terminal 2.

(c) Connect -18 (±0.5) volts through a 220-ohm resistor to terminal 1. Measure the voltage between terminals 2 and 1.

Requirement: -9.0 volts (approximately)

(d) Remove the -18 volt supply from terminal 1 and connect +18.0 (±0.5) volts through the 220-ohm resistor to terminal 1. Measure the voltage between terminals 1 and 2.

Requirement: +18.0 (±0.5) volts

(e) Repeat steps (c) and (d) for terminals as follows:

TERMINAL TO BE GROUNDED	TERMINAL FOR VOLTAGE
4	3
6	5
8	7
12	11
14	13
16	15
18	17

(f) Restore the circuit board to normal.

L. Transmitter Amplifier Circuit Board Test (CP AS61)

4.16 The circuit board must be removed from the data set prior to performing this test. Refer to Fig. 6 for a schematic diagram of the transmitter amplifier board.

(a) Connect the 700-Hz oscillator output between terminal 12 and ground (terminal 4).

(b) Connect a 420A diode (emitter side) from terminal 7 to ground.

(c) Strap terminal 2 to terminal 15. Connect terminal 10 to ground through a 600-ohm resistor.

(d) Connect +18 volts to terminal 1 and 8. Ground terminals 4 and 9.

(e) Connect the strap for option Z as shown in Fig. 6.

(f) Connect -18 volts to terminal 6. Measure the voltage between terminal 17 and ground.

Requirement: -6.0 (±0.6) volts

(g) Set the oscillator to 700 (±10) Hz at a level of 5.2 (±0.1) volts rms.

(h) Place the oscilloscope probes between terminal 15 and ground (terminal 4). A 700-Hz signal should be present. Place the probe between terminal 10 and ground. The signal should not be present.

(i) Remove the -18 volt source from terminal 6.

(j) Strap terminal 3 to terminal 6. Measure the voltage between terminal 17 and ground.

Requirement: 0 volts

(k) Measure the voltage between terminal 6 and ground.

Requirement: +6.0 (±0.6) volts

(l) Place the oscilloscope probes between terminal 10 and ground; a 700-Hz signal should be present.

(m) Connect the strap for option Y as shown in Fig. 6. Measure the signal level between terminal 10 and ground.

Requirement: –3 (±1) dBm

(n) Connect the strap for option X. Measure the signal level between terminal 10 and ground.

Requirement: –6 (±1) dBm

(o) Remove the option straps. Measure the signal level between terminal 10 and ground.

Requirement: –9 (±1) dBm

(p) Remove the strap placed between terminals 2 and 15. Remove the 600-ohm resistor from terminal 10.

(q) Remove the oscillator lead from terminal 12 and connect it to terminal 10.

(r) Set the oscillator level at 4.5 volts rms.

(s) Using the oscilloscope, measure the voltage of the wave form between terminal 2 and ground.

Requirement: 4.0 (±1.0) volts peak

(t) Restore the circuit board to normal.

M. Receiver Input and Transmitter Timer Circuit Board Test (CP AS62)

4.17 The circuit board must be removed from the data set prior to performing this test. Refer to Fig. 4 for a schematic diagram of this circuit board.

(a) Connect –18.0 volts to terminal 4 and connect ground to terminals 5, 8, and 18.

(b) Connect a 1200-ohm resistor between terminal 17 and ground.

(c) Connect straps for option U as shown on Fig. 4.

(d) Connect the oscillator to terminal 20.

(e) Adjust the output of the oscillator to 1000 (±10) Hz at +2.0 dBm. Measure the level between terminal 17 and ground.

Requirement: 1.1 (±0.1) volt rms.

(f) Connect straps for option W. Measure the level between terminal 17 and ground.

Requirement: 0.35 (±0.01) volt rms.

(g) Connect a +18.0 volt source to terminals 1, 2, and 3 through separate 2000-ohm resistors.

(h) Apply ground to terminal 6. A wave form similar to that shown in Fig. 16, should be observed on terminals 1 and 2 each time ground is applied.

(i) Measure the voltage at terminal 3 for the duration of ground application.

Requirement: –17.0 volts

(j) Set the KS-14510 meter to OHMS X 100. Measure the resistance between terminals 16 and 13.

Requirement: 5620 ohms

(k) Set the meter to OHMS X 10. Measure the resistance between terminal 15 and terminals 11 and 12.

Requirement: 287 ohms between terminals 15 and 12

Requirement: 422 ohms between terminals 15 and 11

(l) Restore the circuit board to normal.

N. Transmitter Oscillator Circuit Board Test (CP AS63)

4.18 The circuit board must be removed from the data set prior to performing this test.

(a) Connect a test circuit as shown in Fig. 17.

(b) Connect +18.0 volts to terminal 1 and ground to terminal 12.

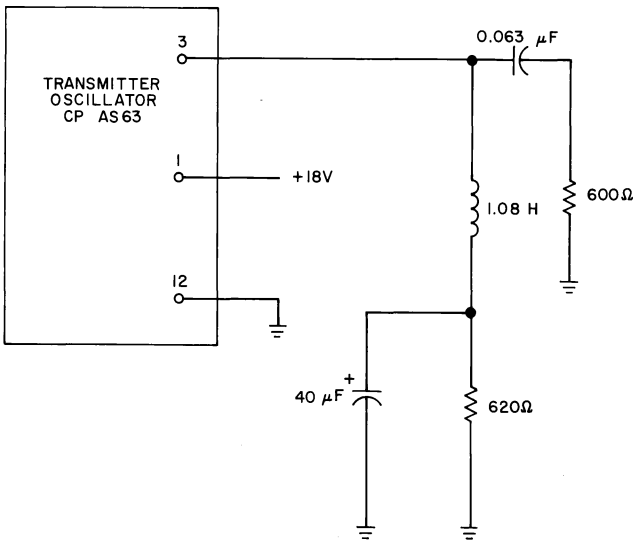

Fig. 17—Transmitter Oscillator Test Setup

(c) Connect a strap from terminal 15 to terminal 18. Observe a single frequency across the 600-ohm resistor.

(d) Connect a 430-ohm resistor between ground and terminal 9. Measure the signal level across the 600-ohm resistor.

Requirement: Equal to or greater than –4 dBm.

(e) Remove the 430-ohm resistor and the strap between terminals 15 and 18.

(f) Connect a strap from terminal 9 to terminal 11. Observe a single frequency across the 600-ohm resistor.

(g) Connect a 100-ohm resistor between terminal 18 and ground. Measure the signal level across the 600-ohm resistor.

Requirement: Equal to or greater than –3 dBm

(h) Restore the circuit board to normal.

5. REFERENCES

5.01 The following is a list of reference information relative to Data Set 404A:

- Data Set 404A Transmitter-Receiver, Identification and Operation (594-021-100)
- Data Set 404A Transmitter-Receiver, Installation and Connection (594-021-200)
- Data Set 404A Transmitter-Receiver, Maintenance (594-021-300)
- Data Set 404A Transmitter-Receiver, Test Procedures (594-021-500)