DATA SETS 403D- AND 403E-TYPES

THEORY OF OPERATION AND SUPPLEMENTARY INFORMATION

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1. GENERAL

SCOPE AND PURPOSE OF PRACTICE

1.01 This practice covers Data Sets (DS) 403D- and 403E-types in greater depth and detail than the description, installation, maintenance, and test (-100, -200, -300, and -500) practices, and is intended to supplement them. Before reading this practice, one should be familiar with the contents of all the other practices in this series, as listed in Part 9. The contents of this practice are not required for normal installation, operation, and maintenance of the subject data sets but should be a valuable aid in the selection of apparatus for specific installations, and in clearing unusual trouble conditions.

1.02 The DS 403D-type is used in multiple set installations, and also as the basic data set in single set installations, where it is referred to as DS 403E-type. In this practice, when referring to both types of data sets in general terms, the term DS 403D/E-type is used. The word "type" has been dropped in subsequent paragraphs; the term "DS 403D/E" refers to DS403D/E-type unless followed by a number to identify a specific data set.

PURPOSE OF DATA SETS 403D/E

1.03 Data Sets 403D/E are data receivers suitable for reception of TOUCH-TONE® signals. These are low-speed voice-frequency 2-out-of-8 parallel *numeric* data signals produced by the TOUCH-TONE telephone and used in both the DDD network and private line service.

1.04 These data sets (except those with the ASCII interface coupler) are well suited for DIVA (**D**igital **I**nquiry, **V**oice **A**nswer) system applications, wherein the customer may call the business machine using a TOUCH-TONE telephone set dial as the input device, and receive a voice answer over the telephone handset (Fig. 1). This answer may consist of machine-generated or prerecorded phrases under control of a computer. Brief examples of applications for DS 403D/E are as follows:

(1) A customer in a department store selects an item he wishes to buy, and presents his credit card to the sales clerk. The clerk checks the prospective buyer's credit rating, using the TOUCH-TONE telephone set as the input device to the credit bureau computer. The computer quickly searches its memory and gives a voice reply to the sales clerk.
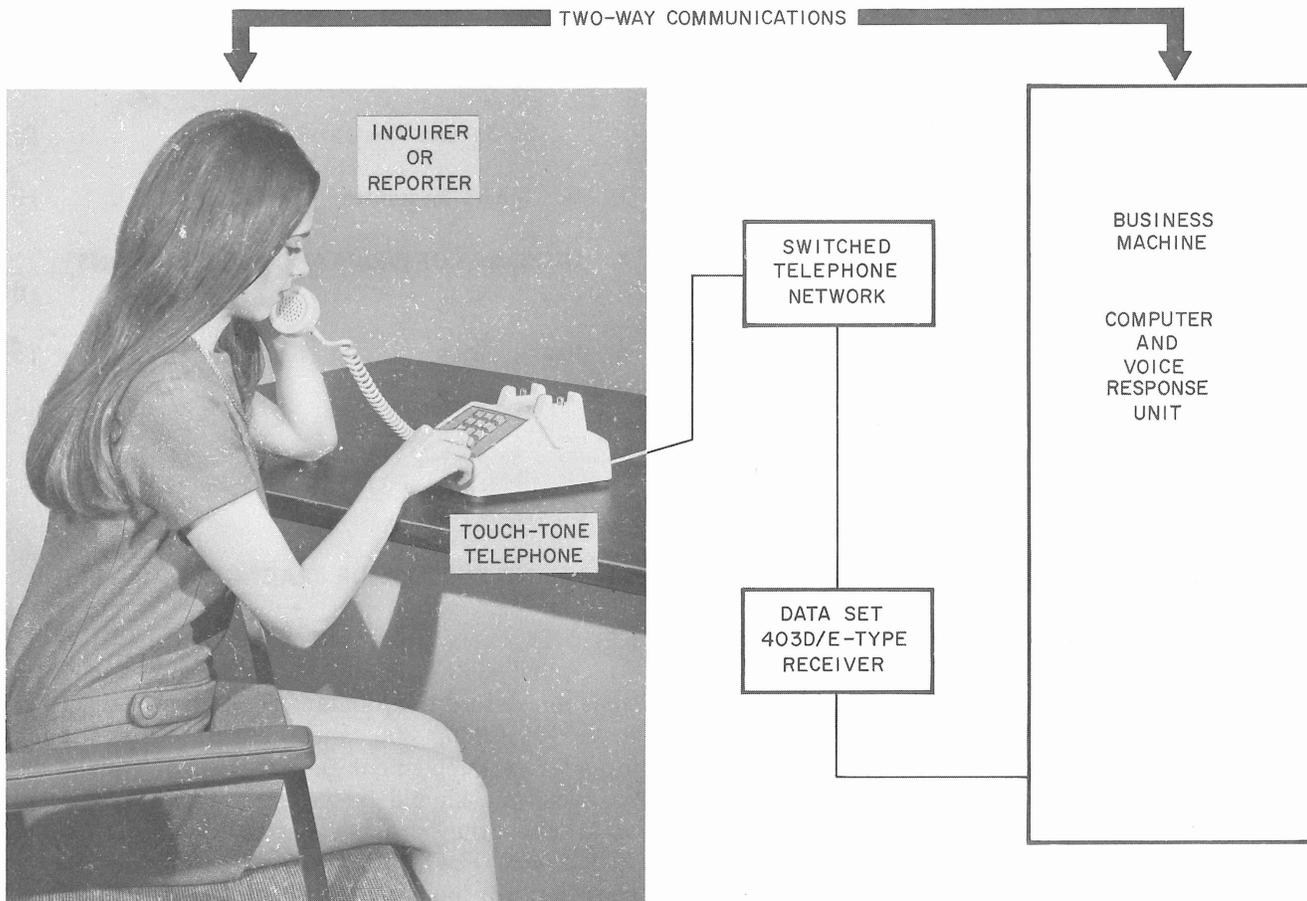
Fig. 1—DIVA—Person-Machine Communications

(2) An individual wishes to find out his current bank balance. Using a scheme similar to that in (1), he inputs to the bank's computer via the TOUCH-TONE dial, and moments later receives his bank balance by means of a voice reply made up of prerecorded phrases under control of the computer.

(3) Another example is data collection using an *exception* reporting scheme, wherein a supervisor determines who is *not* present on a given work day, then reports this to the payroll department computer via the TOUCH-TONE telephone set and the data set. A processor confirms receipt of the information by means of an audible answer-back signal.

(4) Still another application of DS 403D is in a computer-aided grade-school mathematics instruction program. In this application, a console operator calls a student at home after school hours using a CALL-DIRECTOR® telephone set. After a preliminary exchange of verbal information, the operator transfers the student to the computer. This requires the use of the return-to-data feature as described in Part 4. The computer, using a DIVA unit, drills the student in math problems. The student replies by using the TOUCH-TONE telephone dial, while the computer checks the answers, replies "correct" or "try again" via the student's telephone receiver, and keeps a record of the student's progress.

1.05 Note that in each of the aforementioned examples, there is *communication from a person to a machine, and a machine response to the person.* The TOUCH-TONE telephone dial supplies the person-machine interface to enable the person to "talk" to a computer; the telephone handset receiver provides the machine-person interface, permitting the person to receive a verbal reply. The DS 403D/E provides the link from the telephone network to and from the business machine, (a computer in the examples given above). Some other applications of the DS 403D/E are as follows:

- Billing

- Ordering

- Production control

- Payroll

- Inventory

- Room availability

- Airline schedule information

1.06 Three types of interface couplers are provided: CC (contact closure), BCM (binary coded matrix), and ASCII (American National Standard Code for Information Interchange) (Fig. 2). These three interface couplers make the data sets compatible with a large variety of business machines, such as the following:

- IBM 7770 and 7772 Audio Response Units

- RCA 70/510 Voice Response Unit

- CDC 3200 Computer and Cognitronics Voice Unit

- Honeywell Models 200 and 1200 Computers

Note: All of the above are employed in DIVA systems.

1.07 There are presently twelve kinds of DS 403D/E type, six of which are rated MD. The current standard and MD data sets for single and multiple set installations, the three types of interface coupler (15A-type data unit), the power supply, housing, and the USOC codes are given in Table A.

1.08 A data auxiliary set (DAS) is required to supply TALK, TEST, and DATA functions on both single and multiple set installations. The single set station, using DS 403E, requires a DAS 804G for control functions. Multiple set stations, using DS 403D, require a DAS 804K for control functions for each 16 or fewer data lines.

RELAY CONTACT
INTERFACE COUPLER
(15A1 DATA UNIT)

3A-TYPE
DATA MOUNTING

BCM VOLTAGE
INTERFACE COUPLER
(15A2 DATA UNIT)

BASIC RECEIVER

SERIAL ASCII VOLTAGE
INTERFACE COUPLER
(15A3 DATA UNIT)
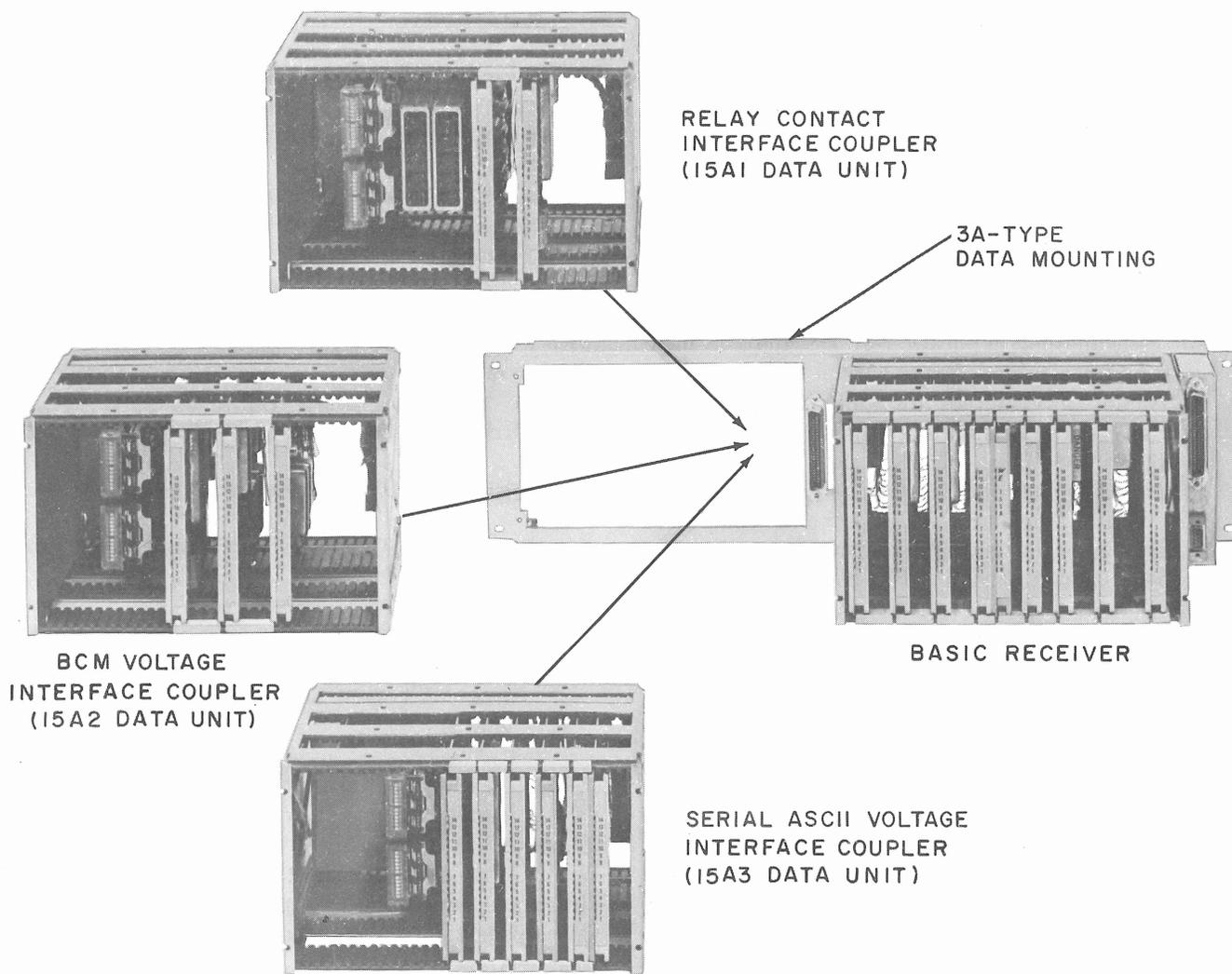
Fig. 2—Data Set 403D/E Basic Receiver and Interface Couplers

TABLE A

DATA SETS 403D- AND E-TYPES
CODING, APPLICATION, AND USOC CODES

DATA STATION DESIGNATION	DATA SET(S) USED	APPLICATION (RECEIVE ONLY)	TYPE OF INTERFACE	DATA UNIT	POWER SUPPLY/ HOUSING	USOC
403D9	403D9	Multi Set	2/8 CC	15A1	31A/ KS-20093	DFA
403D3(MD)	403D3(MD)	Station				
403E5	403D10	Sgl Set			8A/ KS-20018	DCB
403E2(MD)	403D4(MD)	Station				
403D11	403D11	Multi Set	BCM	15A2	31A/ KS-20093	DBB
403D5(MD)	403D5(MD)	Station				
403E6	403D12	Sgl Set			8A/ KS-20018	DCC
403D3(MD)	403D6(MD)	Station				
403D13	403D13	Multi Set	ASCII EIA	15A3	31A/ KS-20093	DAV
403D7(MD)	403D7(MD)	Station				
403E7	403D14	Sgl Set			8A/ KS-20018	DCS
403E4(MD)	403D8(MD)	Station				

Note: Single set stations require a DAS 804G control unit; multiple set stations require a DAS 804K control unit.

FUNCTION OF DATA SETS 403D/E

1.09 Data Set 403E, under control of a DAS 804G, receives and amplifies the incoming data signals, translates them into either parallel contact closure (15A1 data unit), parallel binary coded matrix (15A2 data unit), or serial ASCII (15A3 data unit) signals; these signals are then applied to the business machine (Fig. 3). Voice answer-back from the business machine is provided for in the 15A1 and 15A2 data units, but is not provided for in the 15A3 data unit. Tone answer-back is available under customer control in data sets using the CC and BCM interface couplers; however, it is *not* available in data sets using the ASCII interface coupler. Data Set 403D, under control of a DAS 804K, performs essentially the same functions for a multiple data set receiver (Fig. 4).

THE DATA SIGNAL

1.10 As previously stated, Data Sets 403D/E are designed to receive TOUCH-TONE signals.
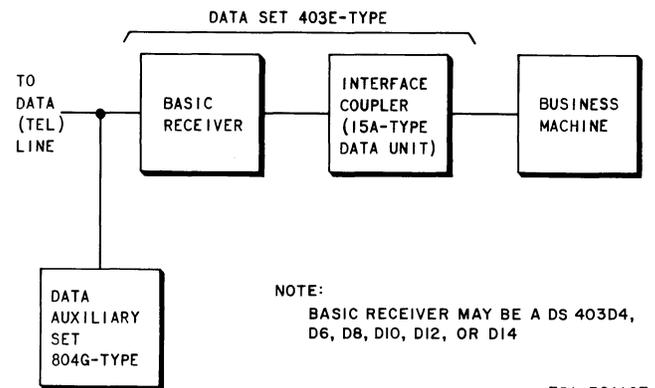
Fig. 3—Data Set 403E-Type Single Set Station—Block Diagram

To provide a basis for understanding the data receivers, a short discussion of the transmitted data signal is given here. The TOUCH-TONE signal is composed of two simultaneous voiceband tones; one from a low group of four frequencies and another from a high group of four frequencies (Fig. 5).

DATA SETS 403D-TYPE

	BASIC RECEIVER	INTERFACE COUPLER (15A-TYPE DATA UNIT)	

TO DATA (TEL) LINES

BASIC RECEIVER

INTERFACE COUPLER (15A-TYPE DATA UNIT)

MULTIPLE-PORT BUSINESS MACHINE OR MULTIPLE BUSINESS MACHINES

BASIC RECEIVER

INTERFACE COUPLER (15A-TYPE DATA UNIT)

BASIC RECEIVER

INTERFACE COUPLER (15A-TYPE DATA UNIT)

DATA AUXILIARY SET 804K-TYPE

NOTE:
BASIC RECEIVER MAY BE A DS 403D3, D5, D7, D9, D11, OR D13.

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Fig. 4—Data Set 403D-Type Multiple Set Station—Block Diagram

HIGH (B) GROUP

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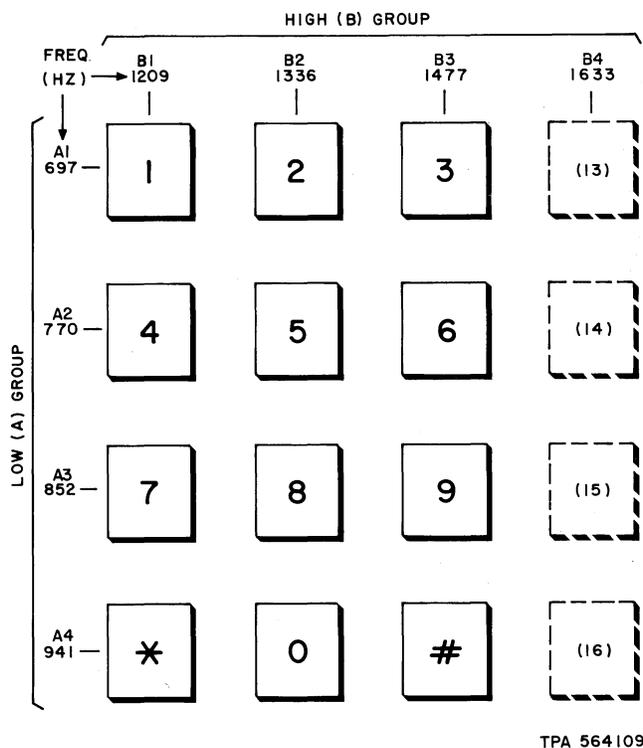
Fig. 5—TOUCH-TONE Dial Frequency Assignments

1.11 Buttons 13 through 16 are not normally present on the TOUCH-TONE telephone, although they are available for special applications and are assigned the B-group frequency of 1633 Hz. This 4-by-4 matrix provides for 16 frequency pairs (characters) using the 8 individual frequencies 2 at a time. The 12-button TOUCH-TONE telephone provides 12 frequency pairs using 7 of the 8 possible frequencies.

1.12 The dual tone for each symbol on the TOUCH-TONE dial is produced so long as the particular button is depressed. For example, if the 8 button is depressed, the 852 Hz of the low (or A) group and the 1336 Hz of the high (or B) group would be generated as long as the 8 button is depressed. The telephone transmitter is muted at this time to prevent talker interference.

1.13 The CC and BCM data sets recognize all 16 of the characters. ASCII data sets recognize only 12 of the 16 characters; they do not recognize a character containing the B4 (1633 Hz) frequency (except for test purposes, as discussed later).

1.14 The TOUCH-TONE frequencies were carefully selected for their nonharmonic relationships and their infrequent occurence in speech, so as to prevent character simulation.

2. DATA SET CHARACTERISTICS

LINE SIGNAL CHARACTERISTICS

2.01 Received signals are all in the voice-frequency range and consist of pairs of tones, one A-group frequency and one B-group frequency, at a rate of up to 10 pairs of tones (10 characters) per second (see 1.10 through 1.14). Line impedance of the data set is either 600 ohms (option X—private line) or 900 ohms (option W—switched network).

2.02 Answer tone and tone answer-back signals can be attenuated before being applied to the data line by option strapping to provide no greater than -12 dBm at the serving central office.

2.03 Voice answer-back is available to customers using the contact closure and BCM interface couplers, but is not presently provided on data sets using the ASCII interface coupler (15A3 data unit). Voice answer-back signals are limited by means of the voice answer-back limiter to ensure that the voice signals applied to the telephone line do not exceed -6 dBm.

INTERFACE SIGNAL CHARACTERISTICS

2.04 Three types of interface coupler are available, as previously mentioned. These interface couplers provide three different kinds of interface signals, permitting the data sets to interface with a wide variety of business machines. Discussion of each type of interface signal follows.

A. 15A1 Data Unit

2.05 The 15A1 data unit provides relay contact closures on eight data leads, which correspond to the four low (A) group and four high (B) group signals produced by the TOUCH-TONE telephone, as discussed in 1.10 through 1.14. For each valid signal received, one A-group contact and one B-group contact is closed. These paired contact closures are presented to the business machine through the interface connector data group leads (Fig. 6). A data carrier detector (DCD) relay contact closure is also presented to the business machine. The

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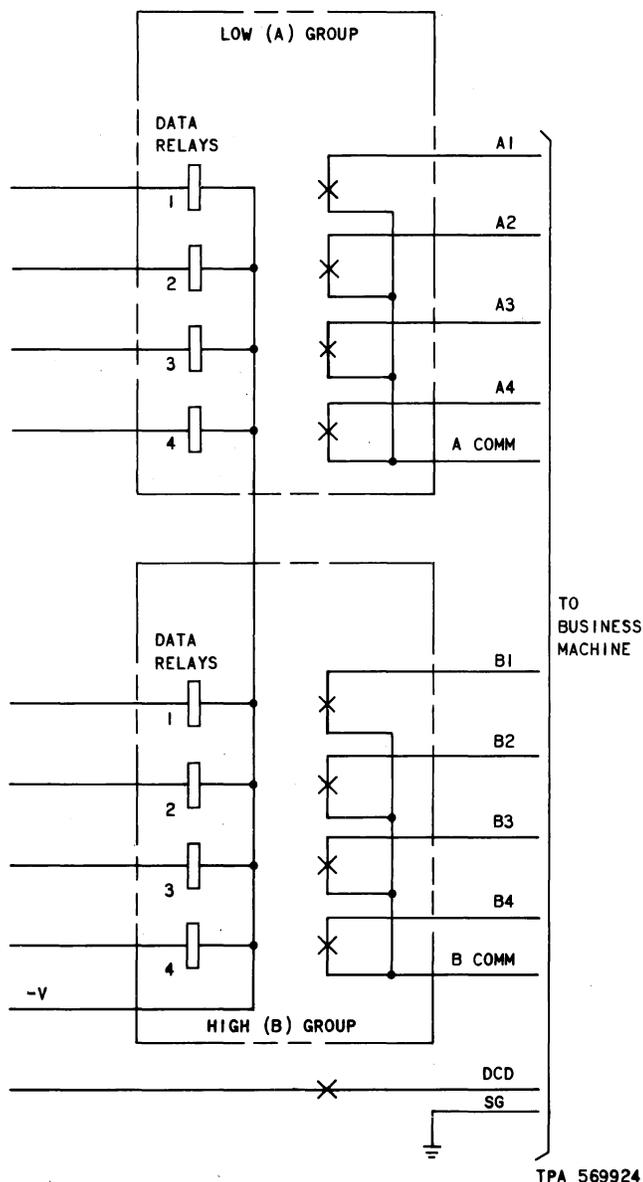
Fig. 6—Parallel Contact Closures Presented to Business Machine

DCD signal is used as a "read" signal by the business machine. The 15A1 data unit is capable of receiving 16 different signals, eg, those produced by a 16-button TOUCH-TONE telephone.

2.06 An answer-back transmitter is provided to permit the customer to signal the transmitting station. The answer-back transmitter is capable of producing three answer-back tones: 1017 Hz, 1785 Hz, and 2025 Hz, depending on whether one or the other or both of two customer interface leads are grounded.

B. 15A2 Data Unit

2.07 The 15A2 data unit provides a parallel 4-level binary coded matrix (BCM) voltage interface signal. Voltages for both data and control functions conform to the Electronic Industries Association (EIA) Standard RS-232-B. TOUCH-TONE type input signals are translated into the BCM code (Fig. 7). Signals are applied to the business machine over four data leads (RD1, RD2, RD3, and RD4) and the DCD lead (Fig. 8). This reduces the number of data leads from nine, as used in the relay contact interface coupler, to five. A positive voltage on a receive data (RD) lead represents a binary 0; a negative voltage represents a binary 1. The 15A2 data unit is also capable of receiving 16 different signals, such as those produced by a 16-button TOUCH-TONE telephone.

2.08 An answer-back tone transmitter is provided to permit the customer to signal the transmitting station. The answer-back transmitter is capable of producing three answer-back tones: 1017 Hz, 1785 Hz, and 2025 Hz, depending on whether one or the other or both of two customer interface leads are grounded.

C. 15A3 Data Unit

2.09 The 15A3 data unit (ASCII interface coupler) accepts parallel A- and B-group frequencies from the basic receiver on eight data leads plus the data carrier detector lead, as do the two other interface couplers. The TOUCH-TONE type signals 0 through 9 are translated to their equivalents in parallel ASCII format. An even parity bit is also generated for each character. In addition, the TOUCH-TONE star (*) and number sign (#) are translated to ASCII characters which are selected by installer option. Also, the second of two successive # provides a 13th character, as selected by installer option. The 15A3 data unit will not respond to the 2-out-of-8 frequencies containing the B4 frequency; therefore the ASCII interface coupler cannot be used with transmitters producing those signals.

2.10 Parallel ASCII characters are next converted from parallel to serial format. The serial clock rate is 110 pulses per second, resulting in a maximum operating speed of 10 characters per second. The serial output is synchronous by bit, but asynchronous by character. Each character is presented to the business machine in the following order (Fig. 9):

HIGH (B) GROUP

		RECEIVE DATA LEADS			
SYMBOL		RDI	RD2	RD3	RD4
I		I	O	I	O
2		I	O	O	I
3		I	O	I	I
4		O	I	I	O
5		O	I	O	I
6		O	I	I	I
7		I	I	I	O
8		I	I	O	I
9		I	I	I	I
O		O	O	O	I
∗		O	O	I	O
#		O	O	I	I
(13)		I	O	O	O
(14)		O	I	O	O
(15)		I	I	O	O
(16)		O	O	O	O

MARK = I = −VOLTAGE
SPACE = O = +VOLTAGE
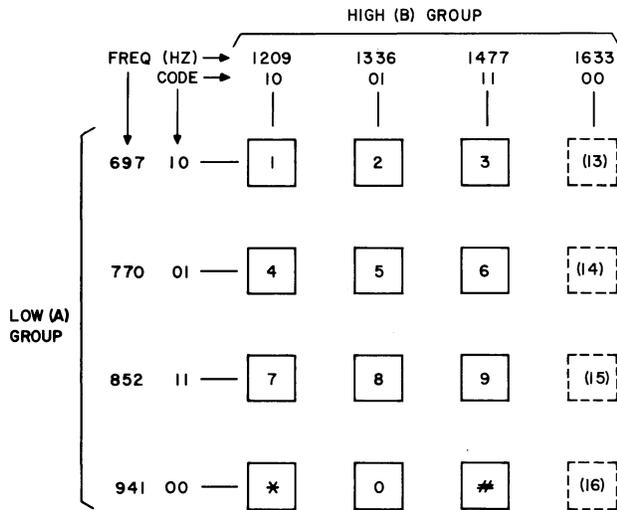
TPA 517542

ARRANGEMENT OF TOUCH−TONE DIAL
SHOWING CODE ASSIGNMENT OF THE
BCM VOLTAGE INTERFACE COUPLER.

BCM CODE TABLE

Fig. 7—Code Assignment and Code Table for 15A2 Data Unit

EIA DRIVERS

FROM BASIC RCVR

AI, A2, A3, A4, BI, B2, B3, B4, DCD

2-OUT-OF-8 TO BCM CONVERTER

RDI, RD2, RD3, RD4, DCD

TO CUSTOMER BUSINESS MACHINE
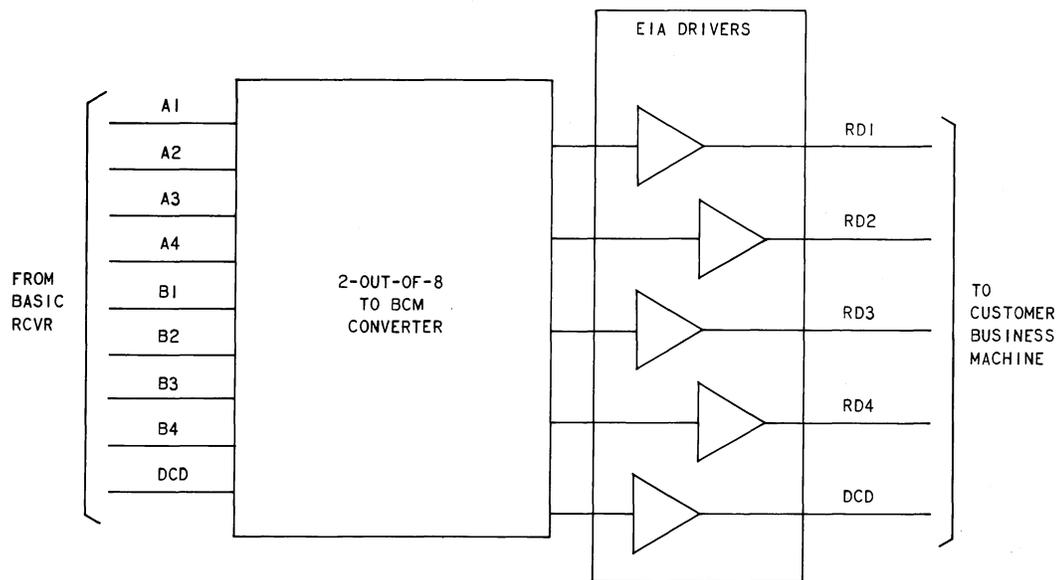
NOTE: BINARY I = −VOLTAGE
BINARY O = +VOLTAGE

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Fig. 8—Parallel BCM Signals Presented to Business Machine
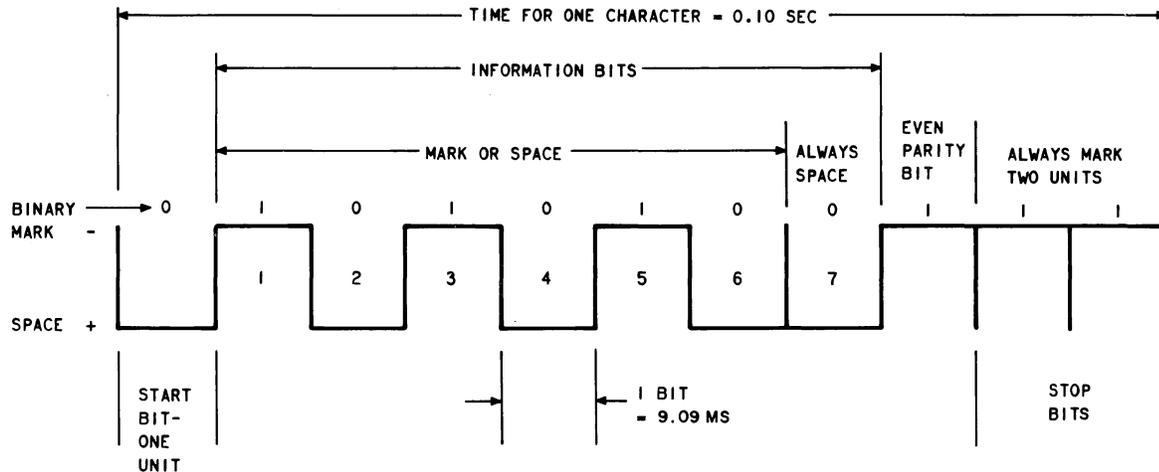
NOTES
1. THIS EXAMPLE ILLUSTRATES THE CONTROL CHARACTER "NAK" OR NEGATIVE
ACKNOWLEDGEMENT. IN THIS CASE THE PARITY BIT IS "1", PROVIDING
AN EVEN NUMBER OF ONES.
2. MARK = -VOLTAGE ; SPACE = +VOLTAGE

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Fig. 9—Serial ASCII Signals Presented to Business Machine

(1) Start bit—spacing—one unit duration

(2) Seven data bits—low order bit first—high order bit (b7) always spacing—one unit duration for each bit.

(3) Even parity bit—one unit duration

(4) Stop bit—marking—two units duration

2.11 The full alphanumeric ASCII code provides 128 characters. Only half this number (64 characters) is used by the ASCII interface coupler, because bit b7 is always a space (Table G). Therefore, no alphabetic information can be received by the 15A3 data unit.

2.12 Signals are presented to the business machine over the received data (RD) lead. Data set ready (DSR), data terminal ready (DTR) and clear to send (CS) leads are also connected to the business machine through the interface connector.

REMOTE TEST CIRCUITRY

2.13 All three interface couplers are provided with remote test circuitry, which permits testing the data station from a data test center. This is accomplished by the TA and TB relays, which transfer the data and control leads away from the customer. When valid test tones are transmitted by the data test center (DTC), tones are returned by the data set to permit checking the following parameters:

● Proper detection of TOUCH-TONE frequencies

● Answer-back tone frequency and level.

After the tests, the data set is returned to normal operation by tones sent by the DTC. See Parts 4 through 7 for further details.

PHYSICAL CHARACTERISTICS

2.14 The basic building blocks of Data Sets 403D/E consist of a basic receiver mounted on a 3A3 data mounting, and any one of three interface couplers (15A1, 15A2, or 15A3 data unit) plugged into the data mounting (Fig. 2). Circuit pack complements of the basic receiver and the interface units are given in Tables B and C, respectively. For further information on physical characteristics of the data set, refer to Section 594-025-100.

TABLE B

CIRCUIT PACK COMPLEMENT OF DATA SET 403D-TYPE BASIC RECEIVERS

DATA SET	CIRCUIT PACK USED							
	CONTROL UNIT	LINE CONTROL	OPTION BOARD	AGC	FILTER	GROUP LIMITERS	CHANNEL DETECTORS	TIMERS, DETECTOR
CURRENT STANDARD 403D9 403D10 403D11 403D12 403D13 403D14	AR462[1] or AR429[2]	AR422	AR461	AR249	755A	AR248	AR246 & AR247	AR245
RATED MD 403D3 403D4 403D5 403D6 403D7 403D8	AR252[1,4] or AR253[2,4]	AR251[4]	AR250[3]					

Notes:
1. For multiple set installation
2. For single set installation
3. Rated A&M only
4. Rated MD

TABLE C

CIRCUIT PACK COMPLEMENT OF 15A-TYPE DATA UNITS

DATA UNIT	CP AR254	CP AR255	CP AR284	CP AR285	CP AR286	CP AR287	CP AR288	CP AR289	CP AR290	CP AR291
15A1	X	X								
15A2		X	X	X						
15A3					X	X	X	X	X	X

A. Data Set 403E Single Set Station

2.15   Data Set 403E consists of a DS 403D and an 8A data unit (power supply) housed in a KS-20018-L1 cabinet. A DAS 804G is required to provide data, talk, and test mode controls for the data station and to provide conventional telephone service. A DAS 801A or 801C Automatic Calling Unit (ACU) may also be provided on an optional basis. Data Set 403E employs one of the six Data Sets 403D listed in Table A for single station use.

For additional information, refer to Section 594-025-100.

B. Data Set 403D Multiple Set Station

2.16   Data Set 403D multiple set station consists of from four to sixteen Data Sets 403D (as listed in Table A), one or two 31A power units, one or two 1B data mountings, and a DAS 804K for control functions. For additional information, refer to Section 594-025-101.

POWER REQUIREMENTS

2.17 All the data set power supplies are designed for operation on 117-volt 60-Hz commercial power supplied by the customer through a 3-wire grounded receptacle. The receptacle should not be under control of a switch. Total line power (60 Hz) may be *estimated* by assuming a maximum of 20 watts per data set, and multiplying by the number of data sets in the station. Power requirements for individual Data Sets 403D/E-type are given in Table D.

OPERATING CONTROLS FOR SINGLE SET STATION

2.18 Data Auxiliary Set 804G is a telephone and control unit which provides normal voice communications, supervisory functions, and switching functions (DATA, TALK, DIAL TONE, and TEST) for Data Sets 403E (Fig. 10). For further details on operation, refer to Section 594-026-200. For further information on DAS 804G, refer to Section 598-048-100.

804G2 AND 804G4

804G1 AND 804G3
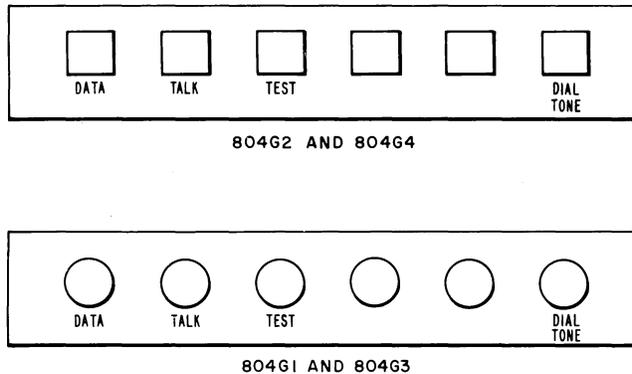
NOTE:
WHEN A GROUND START AUTOMATIC CALLING UNIT IS USED IN CONJUNCTION WITH DAS 804G3 OR DAS 804G4, THE "DIAL TONE" MARKING SHOULD BE STAMPED ON THE KEY STRIP.

Fig. 10—Data Auxiliary Set 804G-Type Pushbuttons

TABLE D

POWER REQUIREMENTS FOR DATA SETS 403D/E TYPE

DATA SET	VOLTAGE SUPPLY	MAXIMUM CURRENT	RIPPLE VOLTAGE	SUGGESTED POWER SOURCE
MULTIPLE DATA SET STATION USE				
403D3, 403D5, 403D9, or 403D11	+18 ±1.0 Vdc - 18 ±1.0 Vdc - 23 ±1.0 Vdc 10 ±1.0 Vac	250 mA 250 mA 200 mA	50 mV PP 20 mV PP 1.0 V PP	31A Power Unit (4 to 16 data sets)
403D7 or 403D13	+18 ±1.0 Vdc - 18 ±1.0 Vdc - 23 ±1.0 Vdc 10 ±1.0 Vac	450 mA 275 mA 200 mA	50 mV PP 50 mV PP 1.0 V PP	31A Power Unit (4 to 8 data sets)
SINGLE DATA SET STATION USE				
403D4 or 403D6	+18 ±1.0 Vdc - 18 ±1.0 Vdc	250 mA 250 mA	50 mV PP 50 mV PP	8A3 or 8A4 Data Unit
403D8 or 403D14	+18 ±1.0 Vdc - 18 ±1.0 Vdc	450 mA 275 mA	50 mV PP 50 mV PP	8A3 Data Unit
403D10 or 403D12	+18 ±1.0 Vdc - 18 ±1.0 Vdc	250 mA 250 mA	50 mV PP 50 mV PP	8A5 Data Unit

OPERATING CONTROLS FOR MULTIPLE SET STATION

2.19 Data Auxiliary Set 804K is a telephone and control unit which provides data, intercept, test, test release, and hold functions for multiple data set stations using Data Set 403D. A field of

48 keys is provided, with associated status-indicating lamps (Fig. 11). Data is applied directly to the data sets without operating any key on DAS 804K. For further information on operation, refer to Section 594-025-101.

L1	L5	L9	L13	T1	T5	T9	T13
L2	L6	L10	L14	T2	T6	T10	T14
L3	L7	L11	L15	T3	T7	T11	T15
L4	L8	L12	L16	T4	T8	T12	T16
UTL	SPARE 1	SPARE 2	SPARE 3				
HOLD	SER						TSTR

NO DESIGNATION UNLESS USED
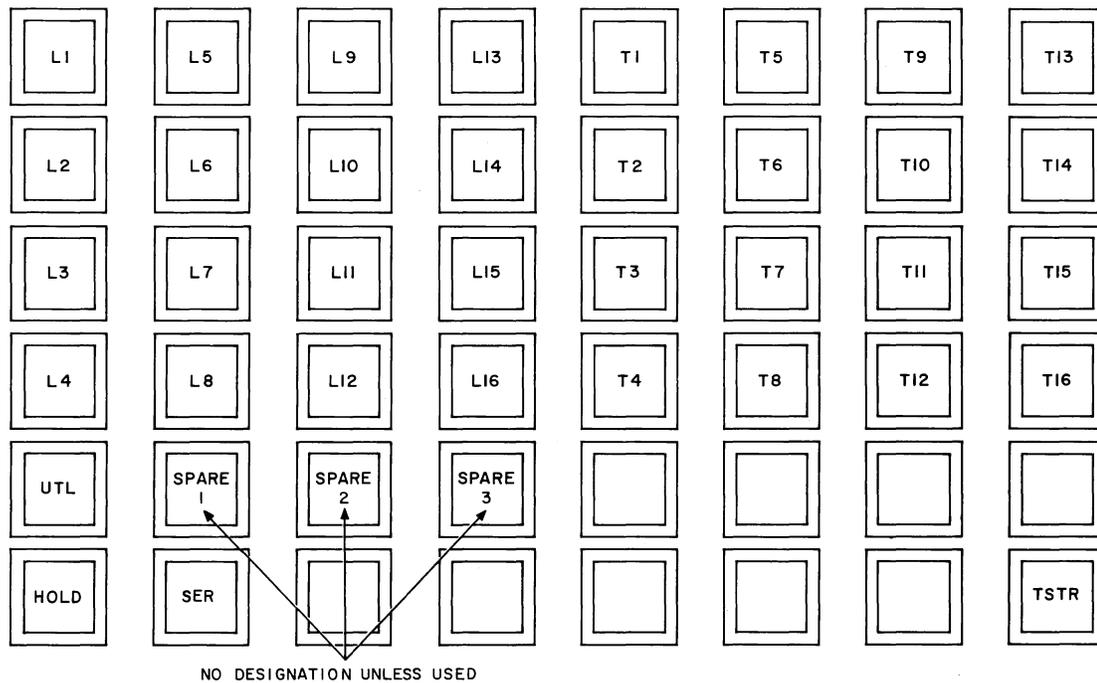
Fig. 11—Data Auxiliary Set 804K-Type—Key Designations

OPTIONS

2.20 The purpose of options is to adapt the data set to specific requirements encountered in a particular installation. The options are applied by strapping specified terminals in the data sets. An example is shown in Fig. 12. Many of the options are similar in function to a single-pole double-throw switch. For example, terminal 6 is strapped to terminal 5 to provide option W; terminal 6 is strapped to terminal 7 to provide option X. Some of the options require more complicated "switching."

2.21 The groups of options are divided into two categories: customer options and Telco options. Customer options are provided to allow the customer to select certain features which meet his needs; Telco options are primarily for the purpose of adapting the data set to match the parameters of the switched network or private line facilities. The available options are summarized in Table E. For additional information on options, refer to Section 590-004-106.
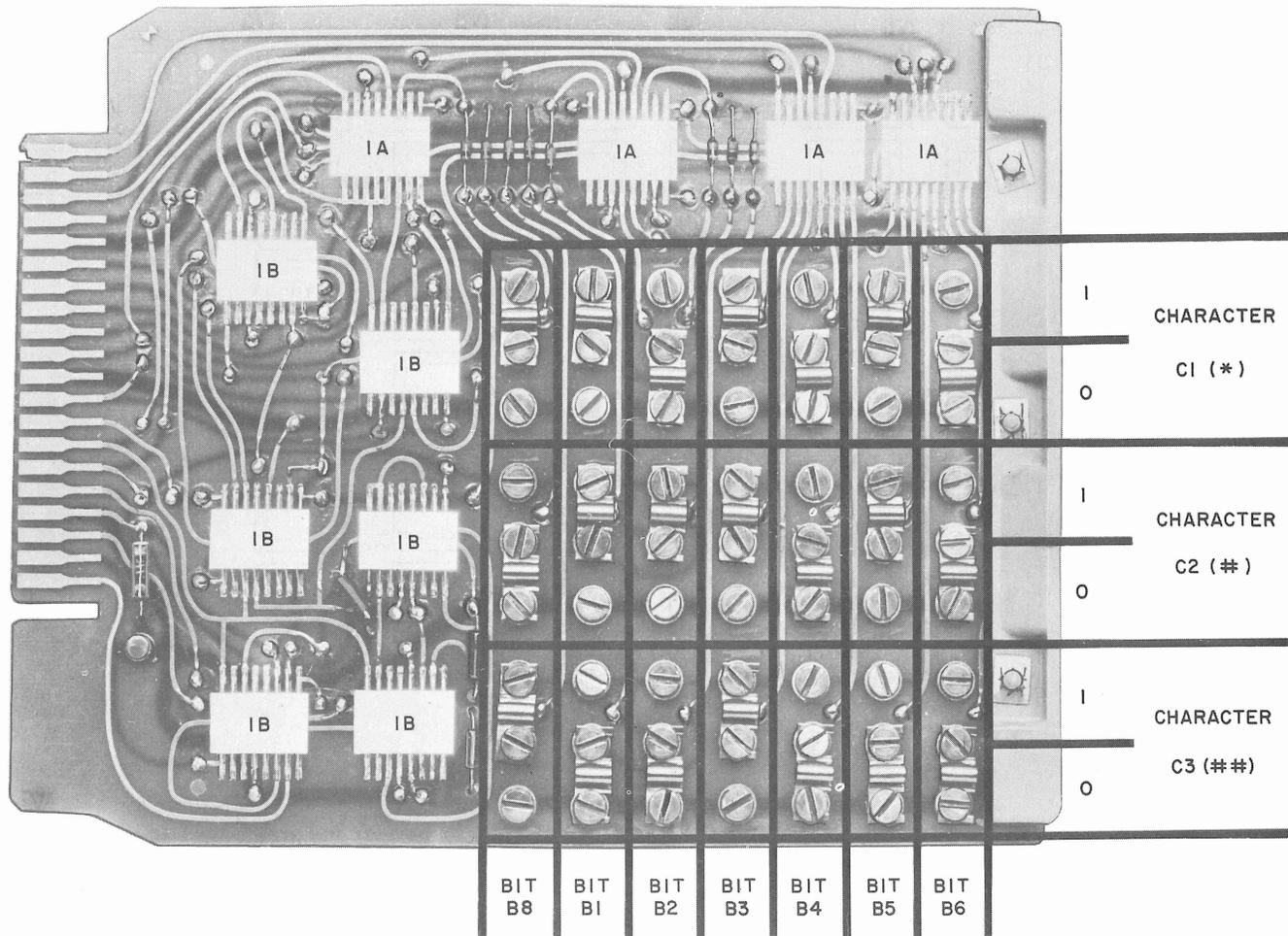
CHAR	B1	B2	B3	B4	B5	B6	B7	B8	FUNCTION
CI (*)	I	O	I	O	I	O	O	I	NAK
C2 (#)	I	I	I	O	I	O	O	O	ETB
C3 (##)	O	O	I	O	O	O	O	I	EOT

NOTE:
FOR EXAMPLE SHOWN AT LEFT, WITH STRAPS POSITIONED AS ILLUSTRATED, THE THREE FUNCTIONS SHOWN WILL RESULT FROM THE STAR (*), NUMBER SIGN (#), AND DOUBLE NUMBER SIGN (# #) AS INPUTS.

Fig. 12—Typical Option Installation on CP AR287

TABLE E

DESCRIPTION OF FEATURES AND OPTIONS FOR DATA SETS 403D- AND 403E-TYPES

FEATURE	OPTION	DESIGNATION		DESCRIPTION	WHERE USED
Answering	Z	Attended		Call answered manually. Manual transfer to data mode if business machine ready.	All 403D- and 403E-types
	Y	Unattended		Call automatically answered in data mode if business machine ready.	
Termination	X	600Ω		Match 600Ω line impedance—principally private line service.	All 403D- and 403E-types
	W	900Ω		Match 900Ω line impedance—principally switched network service.	
Answer-Back Level		Standard Sets	MD Sets	Option chosen at time of installation to make received level of answer-back signal no greater than -12 dBm at serving office. Nominally, data set answer-back signal level with no attenuation is -3 dBm.	All 403D- and 403E-types
	V	-3 dBm	-3 dBm		
	T	-7 dBm	-6 dBm		
	S	-12 dBm	-9 dBm		
6-dB Input Pad	R	In		Normal sensitivity—principally used for TOUCH-TONE or mixed TOUCH-TONE/401-type transmitting stations.	All 403D- and 403E-types
	Q	Out		Increased sensitivity—principally used for 401-type transmitting stations.	
2025-Hz Answer-Tone Duration	N	0.57 Sec		Normal answer-tone timing	All 403D- and 403E-types
	M	1.25 Sec		Answer-tone timing for use with ACU at transmitting station.	
Answer-back	A	Internal		Answer-back circuit in data set used.	All 403D- and 403E-types
	F	External		Customer-provided answer-back generator used.	All 403D types & 403E2,3,5,6

TABLE E (Cont)

FEATURE		OPTION	DESIGNATION		DESCRIPTION	WHERE USED
Line Intercept		E	Attendant Control		Attendant may access data line at any time.	403D3,5,7,9, 11,13
		B	Business Machine Control		Attendant may access data line only when requested by business machine.	403D3,5,9,11
Out-of-Service (Make Busy)		K	Control Circuit OFF	Third Wire Control	Provides means for making data line appear busy by placing ground on third wire (sleeve) or by tip-to-ring short. Line is made busy either by turning control circuit ON or OFF depending on customer equipment. See section entitled Data Sets 403A-, D-, and E-types—Reference Guide (590-004-106) for details.	All 403D-types & 403E5,6,7
		J	Control Circuit ON			403D3,5,9,11 403E5,6
		H	Control Circuit OFF	Tip to Ring Shorted		All 403D and 403E-types
		G	Control Circuit ON			403D3,5,9,11 403E2,3,5,6,
		ZC	Disabled			All 403D- and 403E-types
Private Line Service Without Ringing		ZA	Dry Line (without talk battery)		Allows incoming data calls to be received when ringing signal is not provided. Data set is controlled by DTR interface circuit. Alternate voice service available only with wet line.	All 403D- and 403E-types
		AB	Wet Line (with talk battery)			
Control Function (15A3 Data Unit Only)	Initial ## Character Insertion	XA	Enabled		Provides automatic initial ASCII character for separation of messages.	403D7,13 403E4,7
		XB	Disabled			
	Interdigit Timeout	XC	45 Sec		Permits data set to terminate call after specified period of inactivity.	403D7,13 403E4,7
		XD	15 Sec			
		XE	Disabled			
	∗ Answer-back	XF	Enabled		Provides answer-back tone (2025 Hz) when TOUCH-TONE star (∗) is received.	403D7,13 403E4,7
		XG	Disabled			

TABLE E (Cont)

FEATURE		OPTION	DESIGNATION	DESCRIPTION	WHERE USED
Control Function (15A3 Data Unit only)	# Answer-Back	XH	Enabled	Provides answer-back tone (2025 Hz) when TOUCH-TONE number sign (#) is received.	403D7,13 403E4,7
		XJ	Disabled		
	## Answer Back	ZK	Enabled	Provides answer-back tone (2025 Hz) when second consecutive TOUCH-TONE number sign (##) is received.	403D7, 13 403E4, 7
		ZL	Disabled		

3. DATA SET CAPABILITIES

GENERAL

3.01 Data Sets 403D/E are designed for use on the DDD switched network or private line facilities; therefore, they are subject to the noise, echo, carrier offset, and attenuation inherent in these facilities. Data Sets 403D/E have been designed for reliable operation under these conditions. This part discusses some of the aforementioned network aberrations and the corrective measures provided in the data sets to minimize these difficulties.

ECHOES

3.02 Impedance irregularities, or mismatch, in the telephone transmission plant produce reflections, or echo signals. These echoes are of two types: talker echoes and listener echoes (Fig. 13). **Talker echoes** are produced by a single reflection back to the transmitting station, but cause no difficulty in data transmission; therefore they will not be discussed further here. **Listener echoes** are produced by a double reflection, causing echo signals to appear to be valid signals some time after the valid signals appear. Echo signals that might be encountered on the switched network may have a maximum of 40 milliseconds delay and at a level up to 14 dB below the valid signals. Listener echoes are divided into three types, identified as types I, II, and III.

(a) **Type I Echo:** The type I echo (Fig. 14) appears as a separate data signal and does not overlap the preceding or following valid data signal. A valid data signal has a minimum duration of 40 milliseconds. Since the minimum
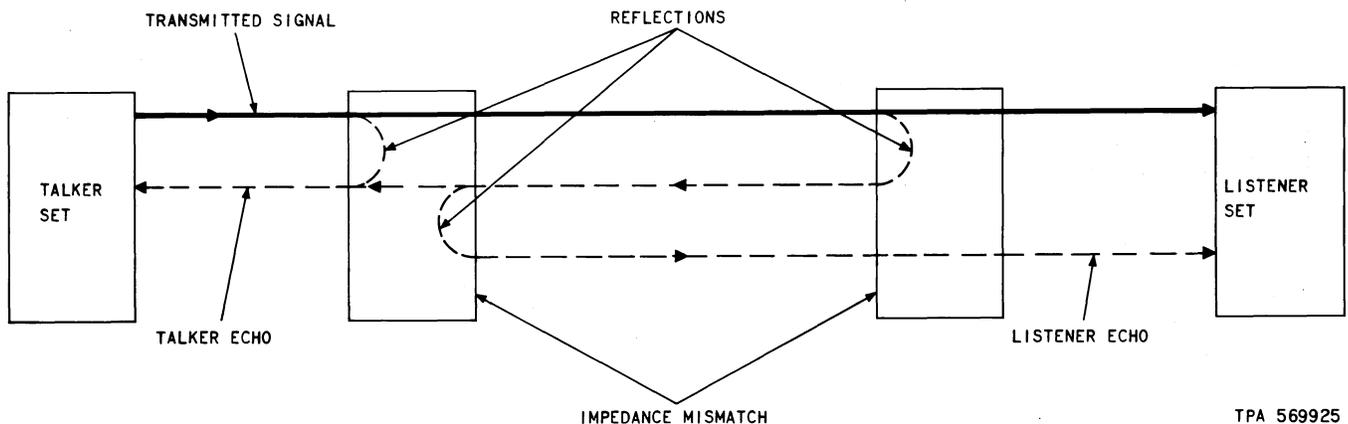

Fig. 13—Echoes on a Transmission Line

TPA 569925

signal duration T_S is 40 milliseconds and the maximum echo delay T_D is 40 milliseconds ($T_S > T_D$), this type of echo will not be encountered and need not be considered further here.

TYPE I

TYPE II

TYPE III

LEGEND:

T_S = SIGNAL DURATION
T_E = ECHO DURATION
T_D = ECHO DELAY
S = SIGNAL AMPLITUDE
E = ECHO AMPLITUDE
T = TIME

TPA 569926

Fig. 14—Types of Listener Echoes

(b) ***Type II Echo:*** The type II echo has a delay of 0 to 40 milliseconds; thus it appears before the valid data signal ends, but disappears before the next valid signal appears. This is the type of echo signal which causes difficulty in data transmission, and for which echo protection is provided.

(c) ***Type III Echo:*** The type III echo appears before the valid signal ends and remains until the next valid signal has started. For type III echoes, the interdigital spacing must be less than the echo duration. Since the interdigital spacing is generally more than 45 milliseconds, this type of echo may also be disregarded.
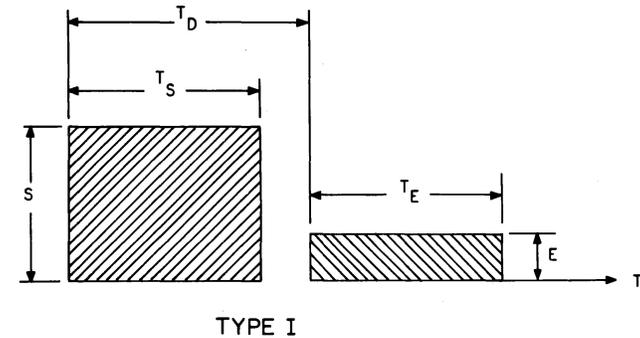
ECHO AND NOISE PROTECTION

3.03 Methods used in the receiver to ignore the presence of noise and type II echo signals are as follows:

(1) Fast AGC (automatic gain control) attack time and slow release

(2) Fixed threshold on input to channel limiters

(3) Channel filter response

(4) Signal timer

(5) Output timer.
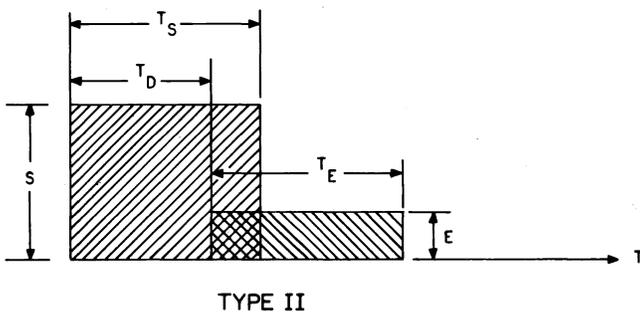
CARRIER OFFSET

3.04 Most medium and long-haul carrier systems use frequency division multiplexing with single sideband suppressed carrier. Because the carrier is not transmitted in these systems, it must be reinserted at the terminating end, resulting in slight differences in carrier frequency. Although carrier systems usually employ a frequency lock arrangement which holds any frequency offset to within ± 1 Hz per facility section, total errors as great as ± 5 Hz can occasionally be encountered in the switched network. To compensate for this and to allow for slight frequency drift with component ageing, the receivers are designed to operate with deviations up to $\pm(0.017\, f_o + 15\, \text{Hz})$ of their designed frequencies. The term f_o refers to the individual TOUCH-TONE frequencies A1 through B4 (Fig. 5). Thus we find that the lowest (A1) frequency has an acceptable range from 670 Hz to 724 Hz; the highest (B4) frequency has a range extending from 1590 to 1676 Hz.
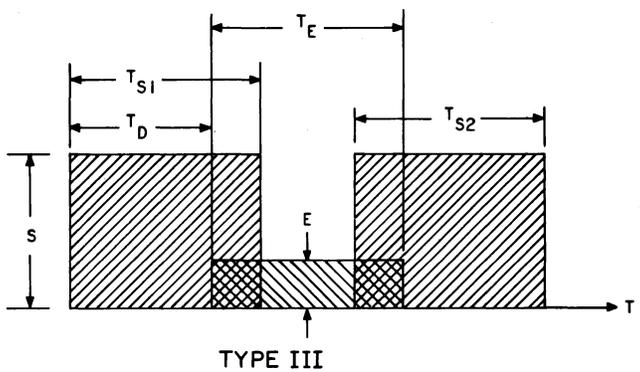
AGC AMPLIFIER CHARACTERISTICS

3.05 The AGC amplifier receives the two-tone data signals through an impedance matching transformer. The amplifier has an input impedance of 600 ohms and a dynamic range of 41 dB; it produces an output voltage of about 0.85 volt RMS over the operating range. The AGC has a fast attack time and a long release time. The long release characteristic of the AGC helps the receiver to disregard echo signals which might cause digit simulation, which would result in false data.

GROUP AMPLIFIER AND LIMITERS

3.06 After the signal passes through the AGC amplifier, the signal is applied to the band separation filter. The filter divides the signal into two groups. The low-group filter rejects the high-group frequencies and passes the remaining low portion of the voice-frequency band. Similarly, the high-group filter rejects the low-group frequencies and passes the remaining high portion of the voice-frequency band (Fig. 15). This method of filtering permits the group limiters to be exposed to as much of the VF spectrum as possible. The respective groups of frequencies are then applied to a group amplifier, threshold circuit, and limiter. Signals greater than the threshold produce a square-wave output of fixed amplitude at frequencies corresponding to the input signal frequencies.

DETECTORS

3.07 Outputs of the two limiters go to two groups of four series-tuned networks, where the individual high and low frequencies are separated into their respective channels. The detectors perform the following functions:

VOICE FREQUENCY SPECTRUM

A-GROUP FREQUENCIES 941 HZ AND BELOW

B-GROUP FREQUENCIES 1209 HZ AND ABOVE
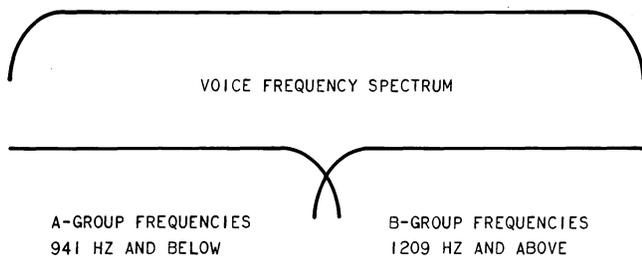
TPA 570096

Fig. 15—High and Low Group Filter Response

• Separate the signals to individual channels

• Verify the presence of two, and only two, signals

• Time input signal duration

• Provide timed output.

After a legitimate signal has been received, the receiver circuitry returns to the idle state in about 6 milliseconds and awaits another signal.

4. THEORY OF OPERATION—BASIC RECEIVER

GENERAL

4.01 This part discusses the theory of operation of the basic receiver in greater detail than other practices in the series, to provide a more thorough understanding of its function. This, in turn, should be of value in the isolation of trouble which has been indicated by loop-back tests from the data test center. The simplified drawings in parts 4 through 7 are provided to show functional relationships only; they are not intended for troubleshooting.

BASIC RECEIVER—FUNCTIONAL DESCRIPTION

4.02 The basic receiver consists of nine functionally related circuit packs (Fig. 16). (Receiver circuit packs for single- and multiple-set use, both MD and current standard, are listed in Table B.) Data signals pass through the DAS 804G control unit or the 1B-type data mounting and are applied to the line control circuit (LCC).

A. Line Control Circuit (LCC) (Fig. 17)

4.03 The LCC contains the following functional circuits:

• Ring Detector

• Line Impedance-Matching Transformer

• Lightning Protection

• 1.1-Second Quiet Interval Timer

• 2025-Hz Answer-tone Oscillator

• 0.57-Second Answer-tone Timer
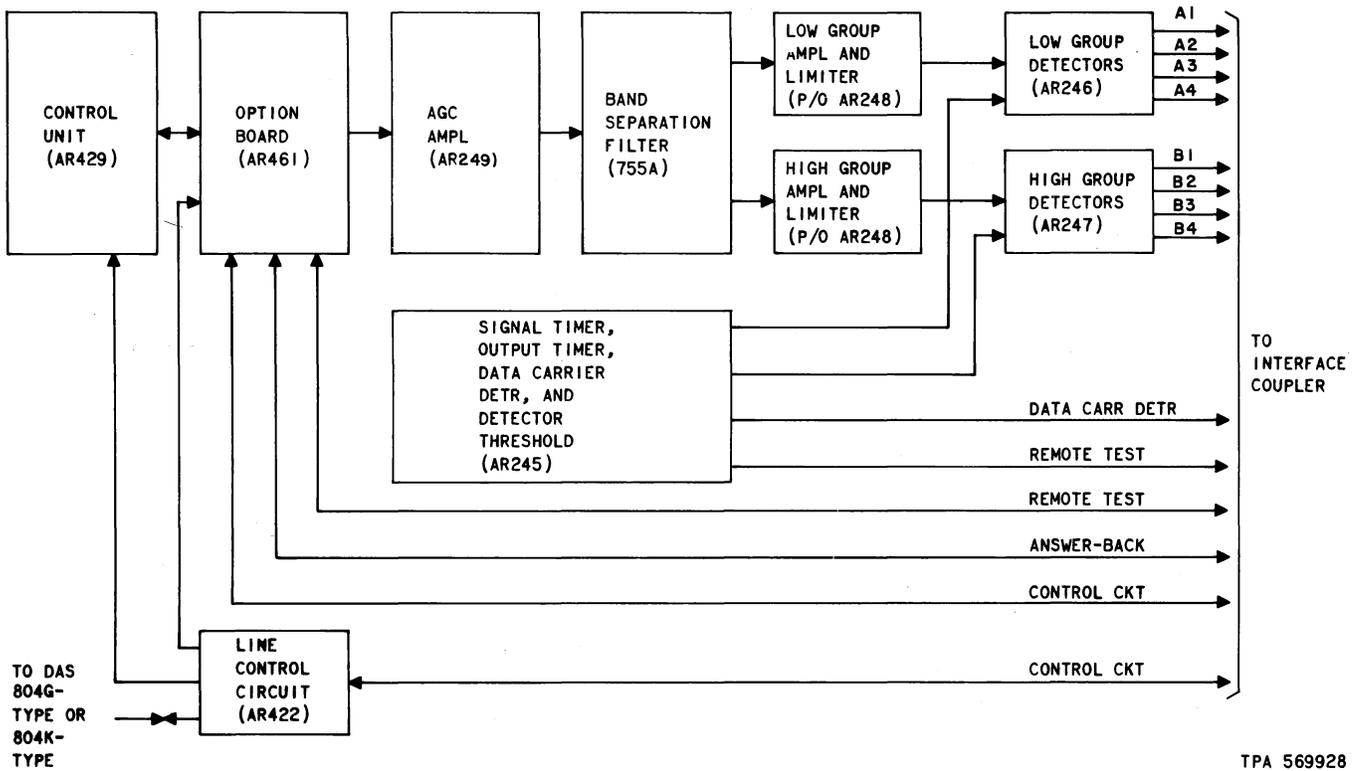
Fig. 16—Basic Receiver—Functional Block Diagram

- Data Set Ready (DSR) Relay Driver

- Line Release

- Attendant Alert Feature

- Out-of-Service Feature

Ring Detector

4.04 When the data set is in the idle state, the ring detector is bridged across the line (DR to DT through K1-1 and K1-2 break relay contacts) (Fig. 17). The circuit into transformer T1 is open because relay K1 is not operated. When a 20-Hz ringing voltage appears on the line, ring relay K4 operates (Fig. 18). Operation of relay K4 indirectly causes relay K5 to operate (Fig. 17). If the customer data terminal relay (DTR) lead is operated, *and* if option Y (auto answer) is strapped across terminal 12 (DTR) and terminal 7 (UA), relay K1 will operate, transferring the line signal from the ring detector to transformer T1 and line holding (H) relay K2, thus tripping the ringing signal. This is known as "line seizure." The dc line current from the central office battery (COB) now flows through the primary of T1 and the H relay, keeping relay K1 operated. Relay K1 remains operated through contacts 2 and 5 of relay K2 after K5 releases. Contact K1-3 operates the DATA lamp in the associated Data Auxiliary Set 804G. If the customer DTR lead is not operated or if power is not applied to the data set, relay K1 will not operate.

Line Matching Transformer

4.05 This transformer provides for impedance matching of either private lines (normally 600 ohms impedance) or DDD lines (normally 900 ohms impedance) with the 600 ohms impedance of the data receiver. The transformer also provides dc isolation for the receiver.

Lightning Protection

4.06 Three varistors are connected across the secondary of transformer T1 to protect against lightning-induced surges on the line. The varistors limit the voltage rise across the transformer secondary to 2.1 volts peak.

1.1-Second Quiet Interval Timer

4.07 Relay K5 is kept operated for about 1.85 seconds. This delay (quiet interval) allows for drop time for a maximum number of tandem links using single frequency (SF) signaling units. This also ensures that relay K1 remains operated to bridge any momentary interruptions in COB, particularly in ESS offices. The LB relay (K5) was not used on CP AR251 (MD).

2025-Hz Answer-Tone Oscillator

4.08 An oscillator is provided to produce a 2025-Hz answer tone to indicate to the calling party that the call has been answered when automatic answer is used at the receiver. Frequency of oscillation is determined by an LC resonant circuit and duration of the answer tone is determined by the answer-tone timer.

0.57-Second Answer-Tone Timer

4.09 This timer is provided to time the duration of operation of the answer-tone oscillator. The oscillator is turned on for 0.50 to 0.65 second (0.57 second nominally) or 1.0 to 1.5 seconds (1.25 seconds nominally) with options N and M, respectively. Option N provides the normal answer-tone duration and option M is used when an automatic calling unit is employed at the transmitting station. Amplitude of oscillation is limited by varistors to 1.3 Vac. The signal level applied to the line is limited by strapping resistors on option board CP AR461 (options S, T, V).

Data Set Ready Relay Driver

4.10 After answer tone is terminated, a 3.0-millisecond delay is introduced before line status (LS) relay K3 operates. When relay K3 operates, it passes a data set ready (DSR) indication to the interface coupler via connector J2-20 and to the customer when the contact closure or BCM interface coupler is used. In the case of the ASCII interface coupler, this signal is used internally in the interface coupler. Another signal, originating at the C relay, provides the DSR indication for the ASCII set. The DSR indication remains until the data call is terminated.

Line Release

4.11 When the customer releases the data terminal ready (DTR) lead (J2-27) in excess of 50 ms, the line control circuit will terminate the call. This is accomplished by dropping connect (C) relay K1, which was operated through the DTR lead. When K1 drops, contact K1-2 opens, dropping the line and the line holding relay K2. When contact K1-4 opens, relay K3 releases. Opening K3-2 contact informs the interface coupler that the call has been terminated. Meanwhile, when relay K1 drops, break contacts K1-1 and K1-2 place the ring detector back across the line in readiness for the next call. The data call may also be terminated by interruption of COB. When the calling party disconnects (hangs up), a battery interruption usually occurs on the data line for a minimum of 10 ms. This interruption is sufficient to drop the H relay, thus terminating the call. When COB interrruption does not occur on the data line for sufficient time to drop the H relay, a time-out period may be used to terminate the call.

Attendant Alert Feature

4.12 On receivers using the contact closure or BCM interface coupler, the customer business machine may send a signal to the associated data auxiliary set to summon an attendant to intercept the call. This is accomplished by the business machine operating the attendant lead (terminal 15 on the customer interface cord). A ground indication is passed from the interface coupler (J2-8) through terminal 32 and contact K3-1 on the LCC. This feature is not available on receivers equipped with the ASCII interface coupler.

Out-of-Service (OOS) Feature

4.13 This feature is provided by either one of two methods: tip-to-ring short or third-wire control. The OOS feature is also arranged by option so that it may be applied by either an ON or an OFF indication from the business machine when used with the contact closure or BCM interface coupler. The tip-to-ring short (Fig. 19) connects the DT lead *across* C relay make contact K1-1 and H relay K2 winding, through option strap G or H and to the DT terminal of transformer T1, then through the primary of T1 to the DR lead. [By placing either Fig. 20 (contact closure interface coupler), Fig. 21 (BCM interface coupler) or Fig. 22 (ASCII interface coupler) adjacent to Fig. 19, the OOS lead may be followed from the business machine to the data line.] The third-wire control scheme places a ground on a third wire back to the CO. Receivers using the ASCII interface coupler are placed out of service by turning the DTR lead OFF (terminal 20 of the interface cord) and with option H or K applied on the option board. In single set installations, the data lamp lights to indicate the out-of-service condition. In multiple set installations, the line lamp winks to indicate the out-of-service condition.
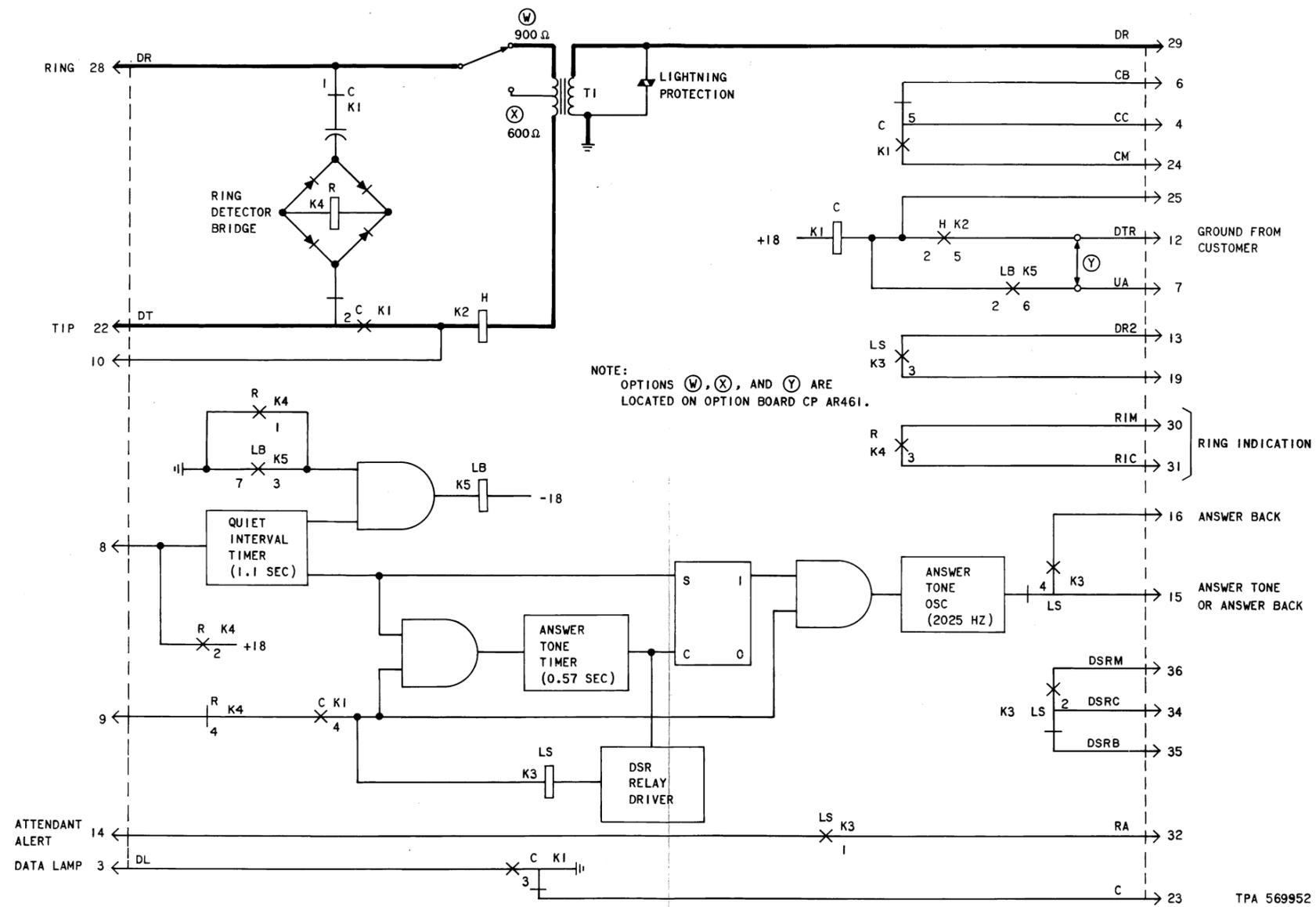
Fig. 17—Line Control Circuit—Functional Diagram
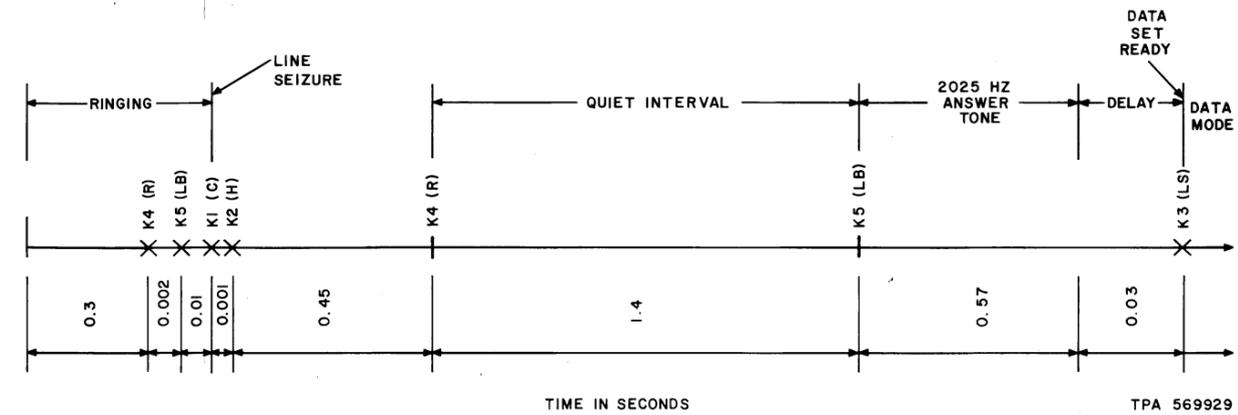
Fig. 18—Contact Sequence Diagram for Line Control Circuit

Fig. 17 and 18

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P/O BASIC RECEIVER

P/O LINE CONTROL CP AR422

P/O OPTION BOARD CP AR461

TIP-TO-RING SHORT

P/O CONTROL CKT CP AR462

P/O OPTION BOARD CP AR461

THIRD WIRE CONTROL
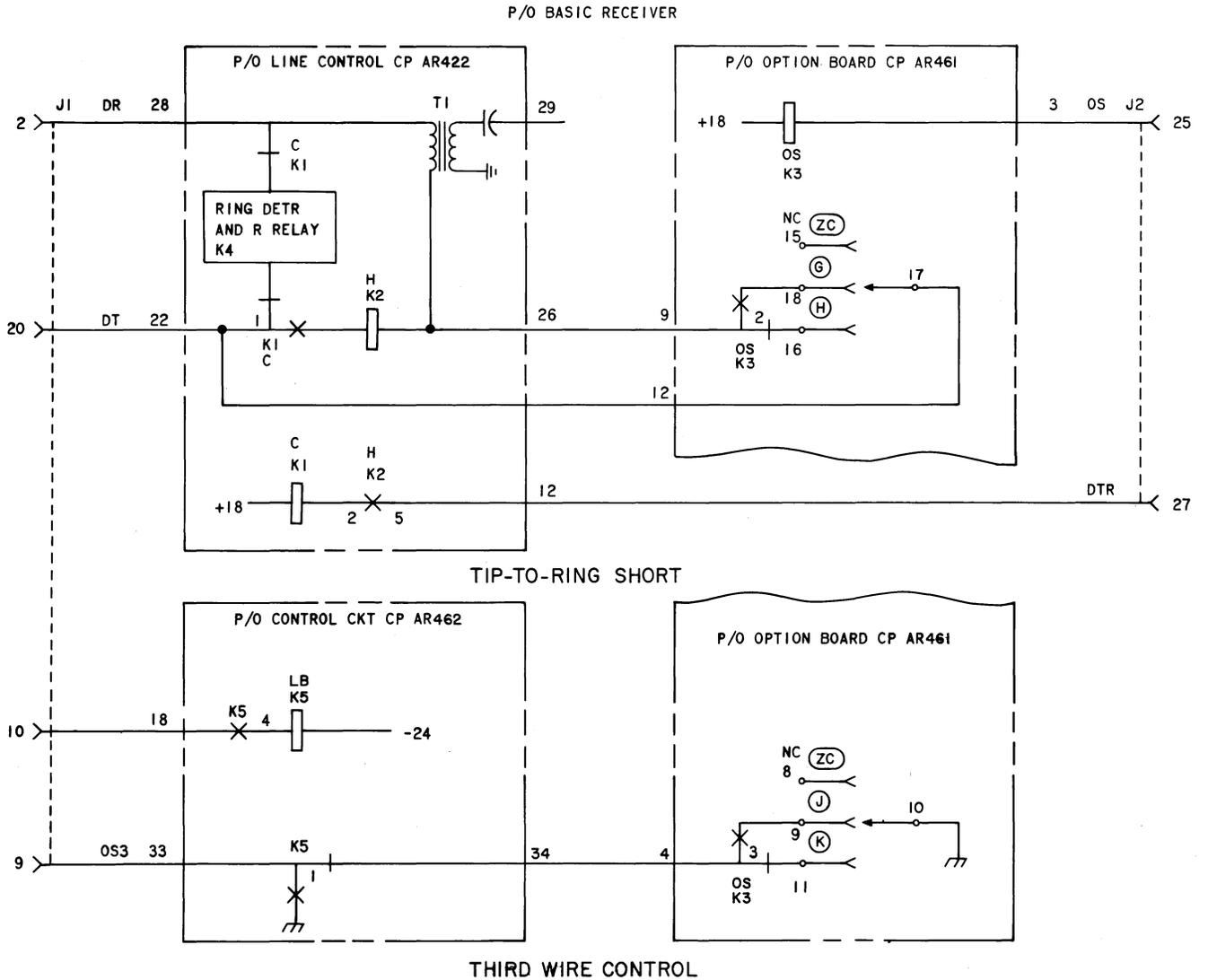
TPA 569930

Fig. 19—Out-of-Service Feature in Basic Receiver—Functional Diagram
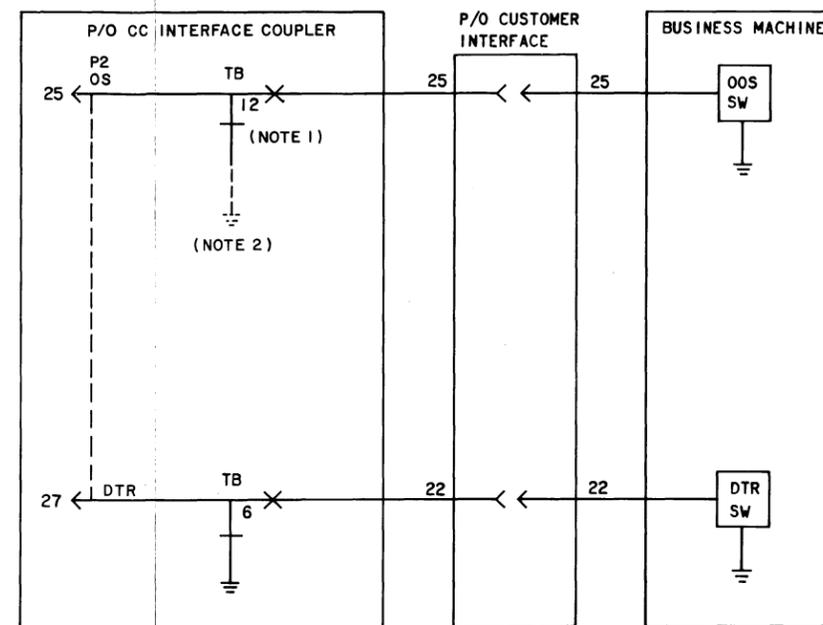
NOTES:
1. TEST RELAY TB IS OPERATED IN DATA MODE.
2. GROUND ORIGINATES IN BASIC RECEIVER AND IS APPLIED TO TB12 VIA OSUG LEAD WHEN OPTION (H) OR (K) IS INCORPORATED.

TPA 569931

Fig. 20—Out-of-Service Feature in Contact Closure Interface Coupler—Functional Diagram
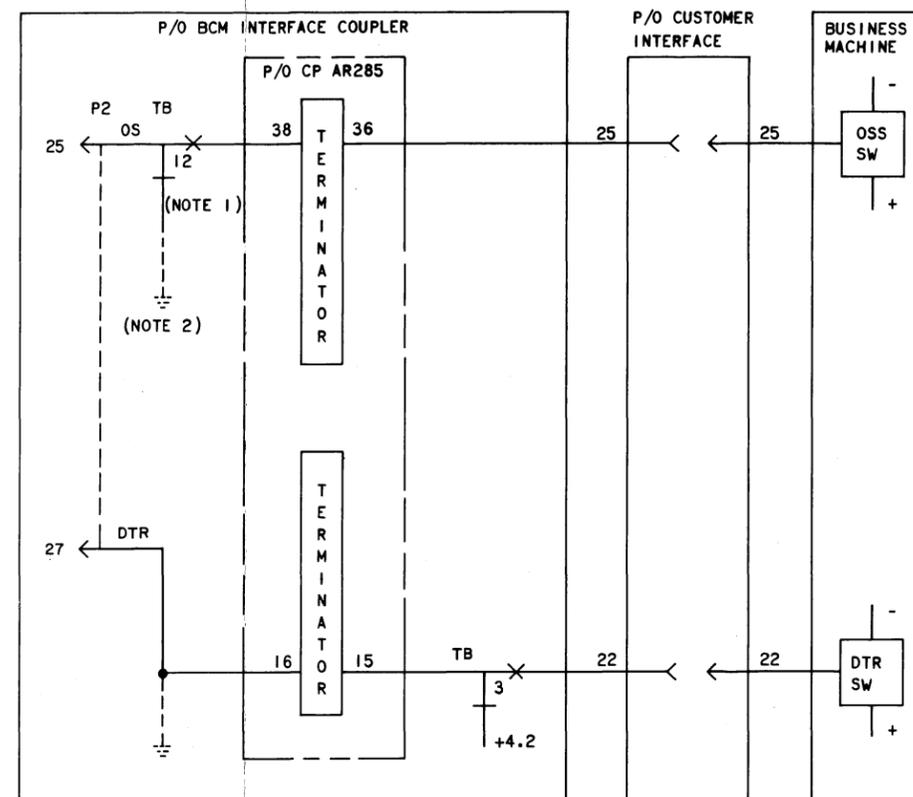
NOTES:
1. TEST RELAY TB IS OPERATED IN DATA MODE.
2. GROUND ORIGINATES IN BASIC RECEIVER AND
   IS APPLIED TO TB12 VIA OSUG LEAD WHEN
   OPTION (H) OR (K) IS INCORPORATED.

TPA 569932

**Fig. 21—Out-of-Service Feature in BCM Interface
Coupler—Functional Diagram**

P/O ASCII INTERFACE COUPLER

P/O CUSTOMER INTERFACE

BUSINESS MACHINE

P/O CONTROL UNIT
CP AR288

ANSBK AND HANGUP CONTROL

DTR-OSS LOGIC

P2
DTR 15

27

(NOTE 2)

+12

10 7 20

TA
(NOTE 1)

20

OOS

DTR
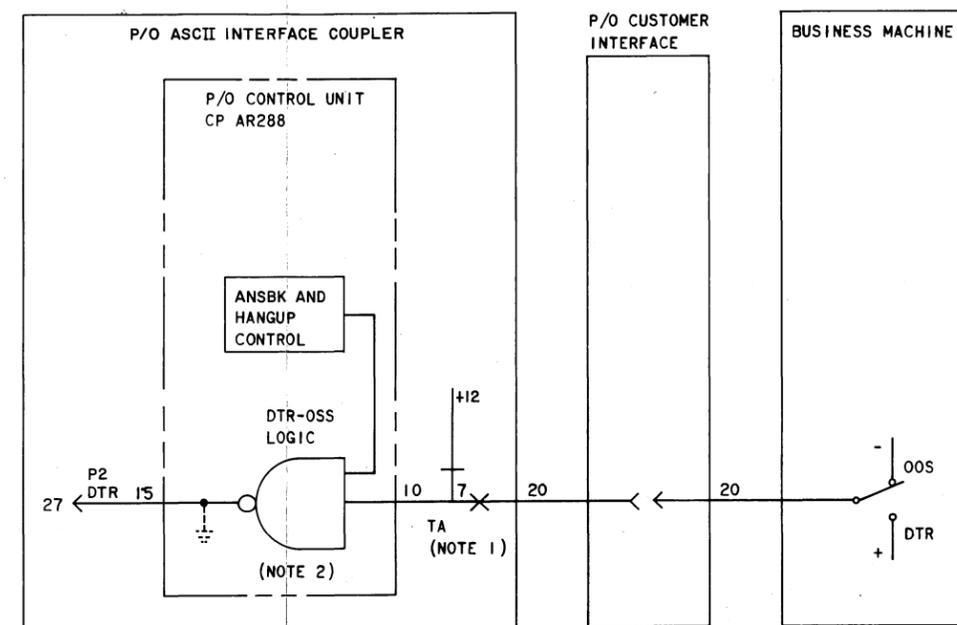
NOTES:
1. TEST RELAY TA IS OPERATED IN DATA MODE.
2. DTR-OSS LOGIC ACTS AS A SWITCH, PLACING
   OPEN OR GROUND ON LEAD 15 OF CP AR288.

TPA 569933

Fig. 22—Out-of-Service Feature in ASCII Interface Coupler—Functional Diagram

B. AGC Amplifier (Fig. 23)

4.14 With the initial ringing-answering phase completed and relay K3 operated to provide the DSR indication, the incoming signal leaves the line control circuit (CP AR422) on lead 29 and enters the option board (CP AR461) on lead 35. The signal then passes through the operated make contact of the data receive (DR) relay K1, and leaves the option board on lead 38. The signal enters the 7-stage AGC amplifier (CP AR249) on lead 3 and is coupled to input transistor Q1 (Fig. 23). The voltage gain of Q1 is nonlinear, varying from 0 dB for strong signals to +6 dB for weak signals. Thus Q1 is the first of three gain-controlled amplifier circuits within the AGC amplifier. The output of Q1 is coupled to a variable loss bridge consisting of transformers T1 and T2, resistors R7 through R10, and diode pair CR1. Bridge loss is controlled to provide a constant voltage out of T2 with a varying input signal level. This variable loss is achieved by changing the current through the diode pair.

4.15 Transformer T2 is capacitor-coupled to transistor Q2. Output from Q2 is capacitor-coupled to Q3, which in turn is capacitor-coupled to transistor Q4. Transistors Q3 and Q4 form a negative feedback voltage amplifier pair, which provides a second gain control. Output from Q4 is capacitor-coupled to Q5; Q5 is in turn capacitor-coupled to transistor Q6, which is the final (output) amplifier for the AGC amplifier. Two outputs are provided through resistors to leads 15 and 16, which in turn go to the band separation filter. Meanwhile, a small portion of the amplifier Q6 output is coupled back through transformer T3 and control amplifier Q7 to control the variable-loss bridge. Resistors R32, R33, and R43 are factory-selected for proper amplifier gain characteristics. The amplifier stage containing Q7 employs a thermistor to compensate for overall amplifier gain characteristics produced by temperature variations. The fast-attack characteristic of the amplifier is provided by varistors RV1 and RV2 in series with capacitor C21. This provides faster AGC action when a sudden increase in input level, such as a tone burst, occurs. Test points are not provided on the AGC amplifier circuit pack.
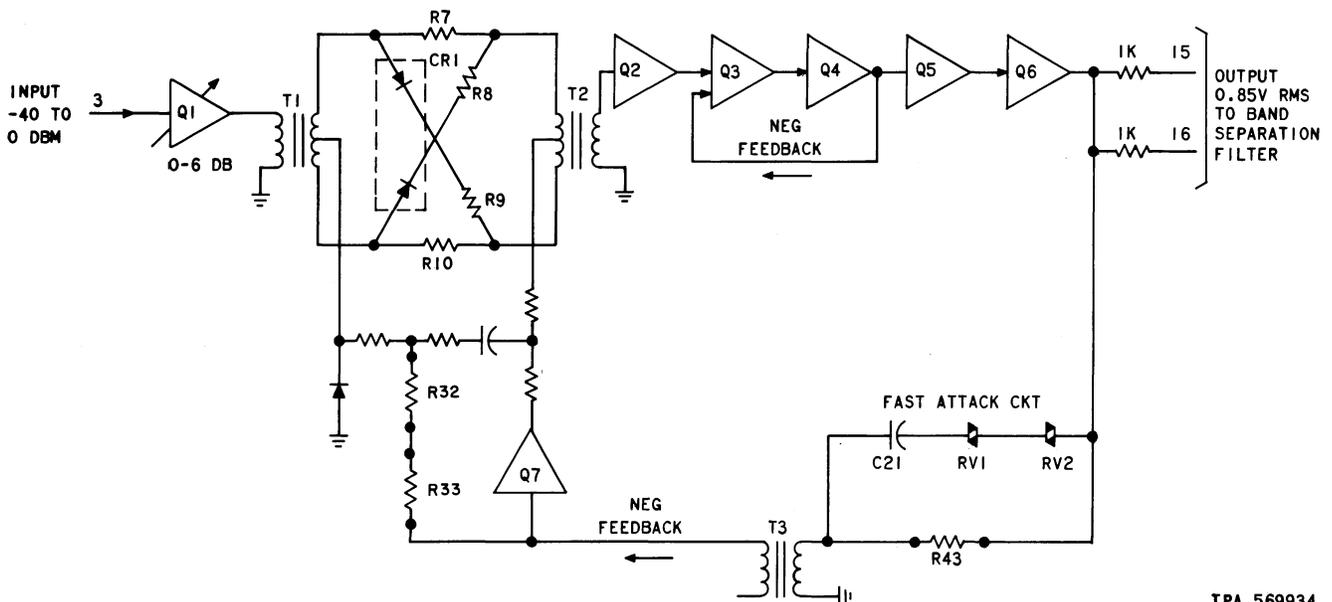
TPA 569934

Fig. 23—AGC Amplifier—Functional Diagram

C. Band Separation Filter (Fig. 24)

4.16 The passive 755A band separation filter separates the voiceband spectrum into a high group and a low group of frequencies (see 3.06). This is accomplished by two separate LC filters,

each in a T configuration. Output of the low frequency group leaves the filter on lead 4 and is applied to lead 3 of the low group limiter. The high group of frequencies leaves the filter on lead 11 and is applied to lead 3 of the high group limiter. Test points are not provided on this filter.
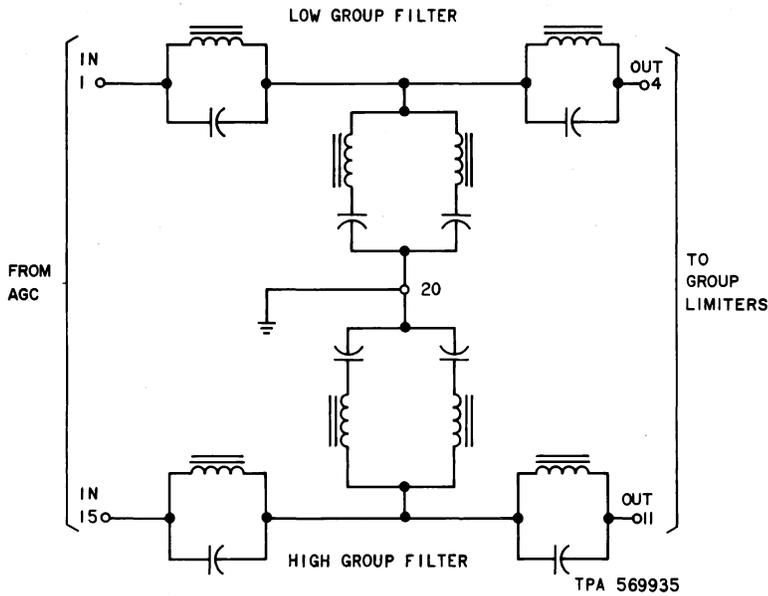
Fig. 24—755A Filter—Schematic

D. Group Amplifiers and Limiters (Fig. 25)

4.17 The low group and high group frequencies from the filter are applied to two similar 4-stage amplifiers, both contained on CP AR248. Since the two amplifiers are so similar, differing only in component markings, first-stage component values, and frequencies passed, this discussion applies equally to both amplifiers.

4.18 The first stage has a 1000-ohm input impedance to match the 1000-ohm output impedance of the 755A filter. Diodes between the first and second stages establish the operating threshold for the amplifiers. The second and third stage limiter amplifiers are controlled by negative feedback from cascaded output stage 4. Amplifier stage 2 operates between cutoff and saturation, causing a square-wave output to be produced. The last stage is composed of cascaded emitter followers, with an output impedance of 10 ohms to match the input of the channel detector that follows. Negative feedback is fed from the output of stage 4 back to the input of the second stage to stabilize limiter sensitivity. Maximum overall gain of the amplifier-limiter is about 20 dBV, producing a square-wave output of approximately 2.65 volts peak-to-peak.
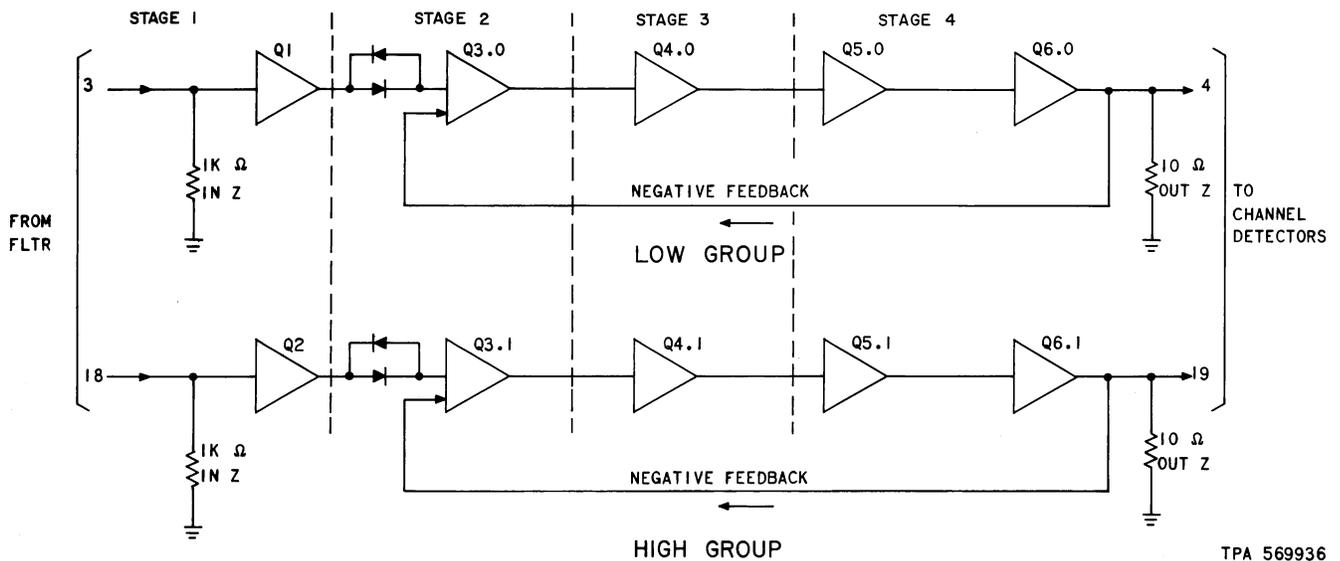
Fig. 25—Group Amplifier and Limiter—Functional Diagram

E. Channel Detectors (Fig. 26)

4.19 Outputs from the high and low group limiters are fed to the inputs of the high and low group channel detectors, respectively. Since the channel detectors are alike except for component values and resonant frequencies, only the low group channel detector will be discussed in detail. The signal is applied to four series-tuned LCR filters, which determine the operating frequency and bandwidth of each channel. Effective Q of the resonant circuit is factory-adjusted by the selection of proper series resistance to establish the required bandwidth. At resonance, only one low group detector is operated. This signal passes to the output OR gate and is added to a similar signal from the high group detector by the AND gate in the timer-detector (CP AR245). The output driver for the particular low group frequency is not enabled until the 23-ms timer in CP AR245 has timed out, thus applying a signal to the output driver in addition to the incoming signal. The timer can only operate when two valid signals—one from the high group and one from the low group—are present. When the output driver operates, one high group and one low group signal are sent to
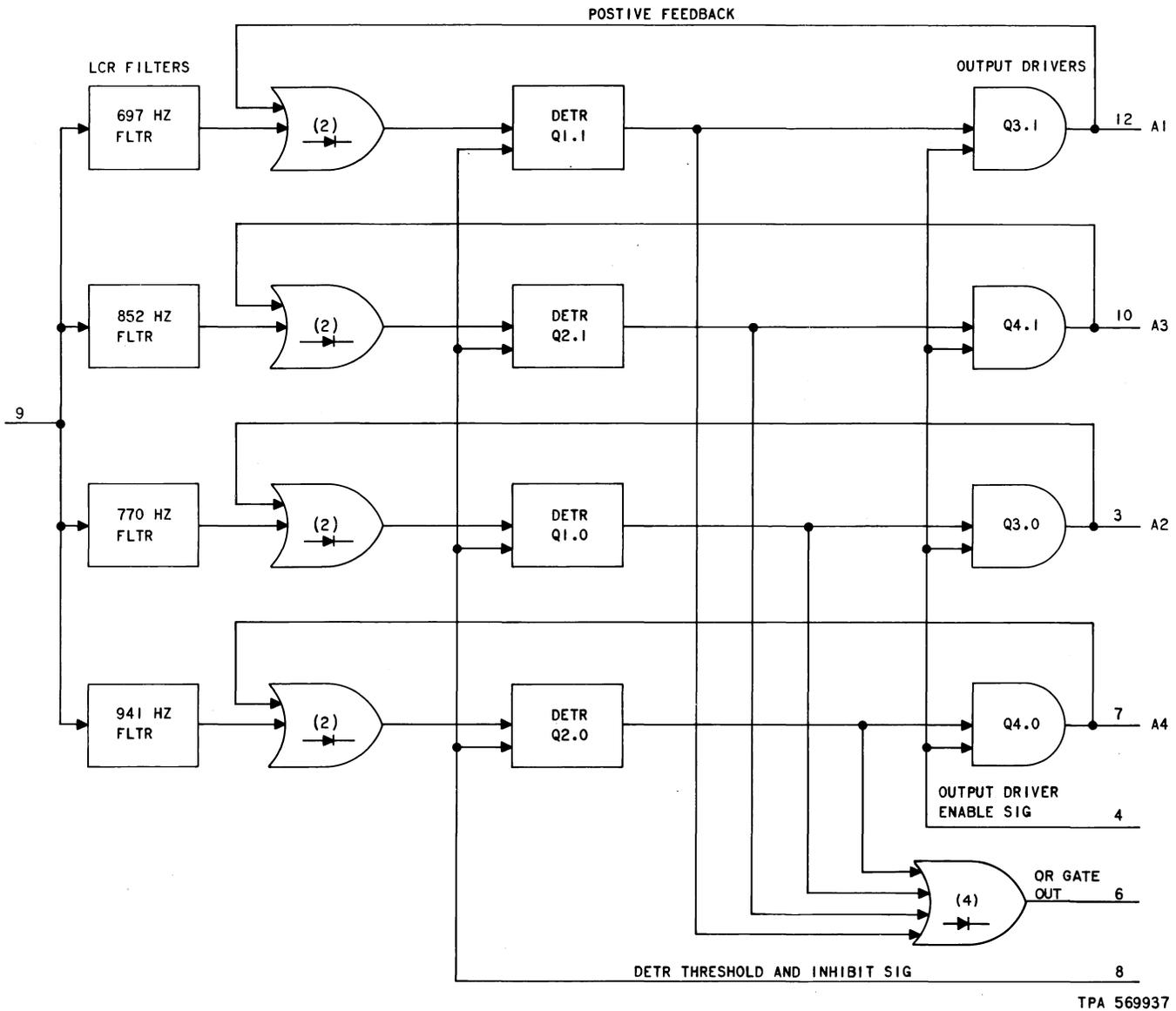
Fig. 26—Low-Group Channel Detector—Logic Diagram

the interface coupler for translation into a form suitable for the customer. Meanwhile, positive feedback is fed back to the OR gate to cause the detector to remain operated, even though the incoming signal may end. The output drivers are turned off by loss of the output driver enable signal, which ends after the 37-ms timer times out. The detector threshold is raised after a valid signal has been received to ensure against false detector operation during the time the output drivers are operated. If the incoming signal ends during the time the output drivers are operated, the receiver starts to recover when the output timer times out (37 ms). The receiver recovers in less than 6 ms and is then ready to accept the next valid signal.

F. Signal Timer, Output Timer, Threshold Circuit, and Data Carrier Detector (Fig. 27)

Signal Timer

4.20 A signal from the 4-input OR gate in the high group channel detector and another from the low group channel detector is applied to transistors Q1 and Q2, which form an AND gate

at the input to CP AR245 (Fig. 27). When two signals are present, an RC timer is started, which times the presence of the incoming signals for a minimum of 23 ms (Fig. 28). This timed signal is fed through amplifier Q3 and to the output timer (Fig. 27). Until the end of this timed period, there is no output from the output drivers in the low group or high group channel detectors (Fig. 26).

Output Timer

4.21 The output timer consists of transistors Q4 and Q5 connected as a monostable multivibrator (Fig. 27). When the signal timer times out, it starts the output timer, which produces a 37-ms enable pulse that is applied to the output drivers in the low group and high group channel detectors. This pulse provides the second of two inputs necessary for operation of two of the output driver AND gates. [The first input has already been applied by the output of one low group and one high group detector (Fig. 26)]. This produces one low group output and one high group output to the interface coupler (A1 or A2 or A3 or A4 *and* B1 or B2 or B3 or B4), with a duration of 37 ms (Fig. 16 and 26).
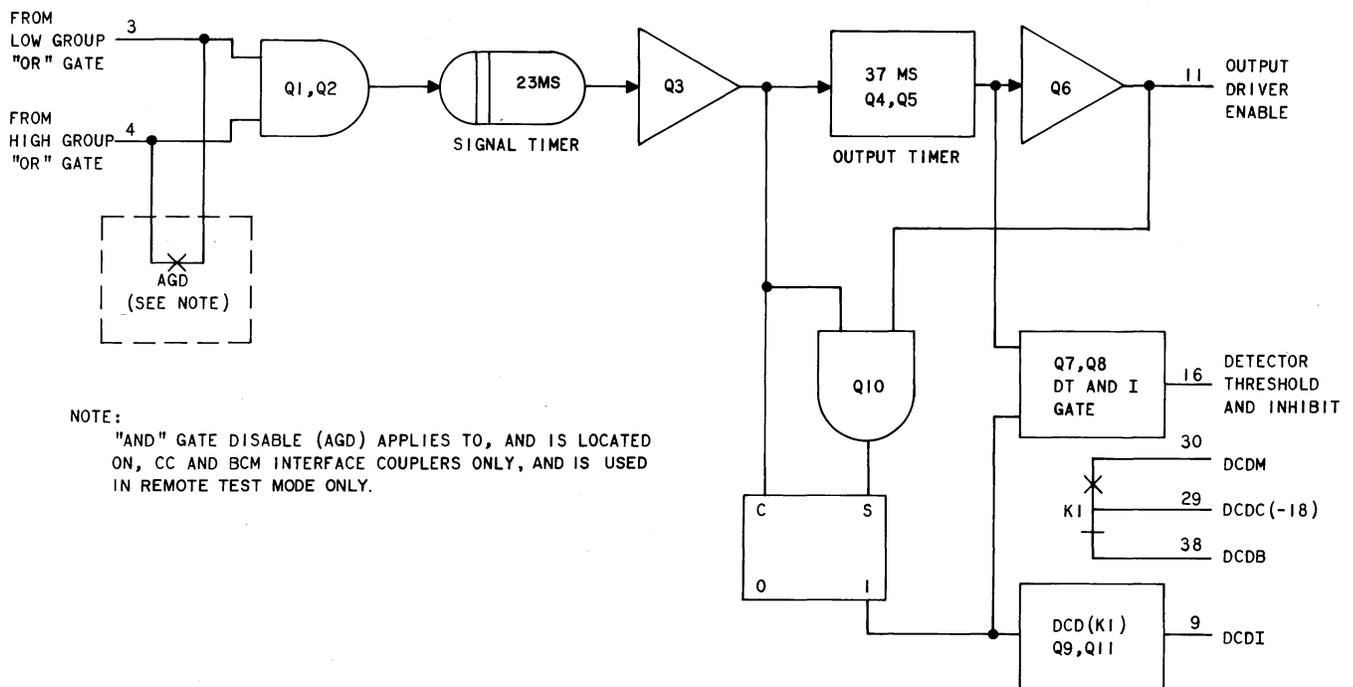
Fig. 27—Signal Timer, Output Timer, Threshold Circuit, and Data Carrier Detector—Logic Diagram

Threshold Circuit

4.22 Normal bias voltage is supplied to the high and low group detectors by transistor Q7 (Fig. 27). When a valid signal is detected, the detector threshold is raised by the action of transistors Q8, Q10, and Q11 to reduce the possibility of false operation by ensuring that the previously operated detector circuits remain locked up.

Data Carrier Detector (DCD)

4.23 With transistors Q3 and Q6 turned on, Q10 and Q11 are operated and in turn operate Q9, which operates DCD relay K1. (The DCD common lead is supplied with −18 volts) (Fig. 27). If the input signal should cease during the timed output interval, the DCD indication remains until the output timer times out (37 ms). After 37 ms, data signals cease but the DCD signal remains as long as an input signal is present (Fig. 28). Operation of the DCD relay is delayed for 2 to 3 ms after operation of the data relays to allow cessation of contact bounce of the reed-type data relays. The mercury-type DCD relay provides a positive timing signal (no bounce) for the business machine to "read" the data present on the data leads. Delay for DCD relay operation is provided by a capacitor on CP AR254 in the CC interface unit, and on CP AR284 on the BCM interface unit; it is connected

to the basic receiver over the DCDI lead (J2-39). The DCDI lead is not present in ASCII interface couplers. The DCD relay information is sent to the customer via the interface coupler when the contact closure or BCM interface unit is used. The DCD information is used internally in the ASCII interface coupler.

G. Mode Control and Key Telephone Control Circuits

> *Note:* There are six possible basic configurations of the DS 403D/E station:

- Single set station with 15A1 Interface Unit (CC)

- Single set station with 15A2 Interface Unit (BCM)

- Single set station with 15A3 Interface Unit (ASCII)

- Multiple set station with 15A1 Interface Unit (CC)

- Multiple set station with 15A2 Interface Unit (BCM)

- Multiple set station with 15A3 Interface Unit (ASCII).

Five functional (abbreviated) drawings are presented in Fig. 30 through 34 with leads arranged so that the two basic receivers and their respective auxiliary sets match with any of the three interface coupler drawings so that the circuits can be readily followed from tip and ring on the left to the customer business machine on the right, thus permitting a simplified presentation of any of the six configurations with a total of five drawings as shown in Fig. 29. Use of the appropriate pair of drawings for your particular station arrangement will facilitate understanding the following discussion.

Single Set Control—Talk Mode—Manual Answer

4.24 When ringing occurs, the handset of DAS 804G is removed and the TALK key depressed. Depressing the TALK key places ground on T relay K1 in the *mode control circuit (MCC)* (Fig. 30). Relay contact K1-1 places a short across the H relay in the *line control circuit (LCC)* so that

Fig. 28—Receiver Signal Timing

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the data set cannot enter the data mode, and also places the apparatus unit across the line. The telephone line is now held by the apparatus unit in DAS 804G.

Single Set Control—Data-to-Talk Transfer

4.25 With the handset of DAS 804G off-hook, depressing the TALK key places ground on relay K1 in the MCC (Fig. 30). Contact K1-1 closes, placing a short access line-holding relay H (K2) in the LCC, which removes the data set from the data mode. Make contact K1-2 opens the circuit to transformer T1. The telephone line is now held by the apparatus unit in DAS 804G. Meanwhile, ground is applied to the TALK lamp through relay contact K1-2 on the MCC, causing the TALK lamp to light. Operation of K1-4 make contact on the MCC resets the circuit in the LCC which generates the 2025-Hz answer tone.

Single Set Control—Data Mode—Manual Answer

4.26 Depressing the nonlocking DATA key removes the short circuit across the H relay (K2) on the LCC (Fig. 30). If the customer DTR lead is turned on, the C relay (K1) will operate through H relay contacts 2 and 5. The C relay transfers the DT lead from the ring detector to the H relay. Telephone line current (COB) now flows through the H relay. The H relay and transformer T1 are now in series from DT to DR. Telephone line current holds the H relay operated. Ground applied through operated relay K1-3 on the MCC to connector J1-11 is used to terminate the test mode, restoring the TA and TB relays in the interface coupler to their normal position for data reception. The TS relay (K2) on the option board (CP AR461) is operated by +18 volts through a dropping resistor. When the data set is placed in data mode, ground applied by the customer operating the DTR lead to terminal 27 of the option board also connects through contacts 2 and 5 of the H relay on the LCC, thus dropping the potential applied to the TS relay sufficiently to cause the TS relay to release. Contacts 2 and 5 of the TS relay are thus open when in the data mode, assuring that the TA and TB relays in the interface coupler remain in proper position for data reception.

4.27 Releasing the DATA key releases the TALK key, which in turn removes the ground from relay K1 in the MCC. When relay K1 is released all contacts return to their normal position. Return

of K1-4 to normal starts the timing cycle on the LCC, and after an appropriate delay, the 2025-Hz answer tone is transmitted. Meanwhile, C relay contact K1-3 in the LCC applies ground to lead J1-27, lighting the DATA lamp. Data may now be received.

Out of Service

4.28 When the customer wishes to place the data set out of service, the appropriate option must have been installed (see 4.13). The OOS indication is sent from the customer through the interface coupler to the OS relay K3 on the option board (CP AR461). The out-of-service indication is then passed through DAS 804G to the CO either as a tip-to-ring short or a third-wire ground.

Attendant Alert

4.29 When the customer business machine wishes to signal an attendant by either visual or audible means, customer interface lead 15 is operated (CC and BCM interface couplers only). This indication is passed through the interface coupler, through the line status (LS) relay K3-1 contact on the LCC, and lead 7 in DAS 804G where it may be used to provide a visual or audible attendant alert. (Refer to Section 598-048-100 for details on attendant alert feature).

Single Set Control—Test Mode

4.30 To simplify procedures for the customer, remote test facilities have been built into the three interface couplers. If the customer reports a suspected case of trouble, a data test center operator calls back and requests the customer to place the data set in test mode by depressing the TEST key on the DAS 804G while the handset is off-hook, and then hang up. With the data set in talk mode and the handset off-hook, when the customer depresses the TEST key, signal ground is applied through J1-13 (AT lead, Fig. 30), through TS relay K2 on the option board and out on lead TM to terminal J2-26, then to the remote test control on CP AR255 in the CC or BCM interface coupler, which operates the TA relay. In the ASCII interface coupler, the TM lead is connected to CP AR290, where the ground passes through a diode, then operates the TB relay. (Remember that the TS relay on CP AR461 is always operated except when in the data mode). Relay contact TA-8 in the CC interface coupler (TA-1 in BCM) transfers

ground away from the TB relay, holding relay TA operated and releasing the TB relay. In the ASCII interface coupler, the TA relay is released by CP AR290. Operation of the TA and TB relays to test mode (TA operated and TB released on CC and BCM interface couplers; TB operated and TA released on ASCII interface couplers) opens all data leads to the customer, and also opens the DSR, DTR, and all answer-back leads to the customer. After the TA relay has operated and the TB relay has released, the TEST key may be released and the handset returned to its cradle, since ground is now applied by make contact TA-8 in the CC interface coupler (TA-1 in the BCM interface coupler; CP AR290 in the ASCII interface coupler). Meanwhile, the TEST lamp is lighted by TA-7 in the CC interface coupler (TA-8 in the BCM interface coupler; TA-4 in the ASCII interface coupler) applying ground to TL lead P2-36 on the interface coupler, and through J1-25 on the basic receiver. Discussion of the remote tests is covered under the respective interface coupler headings.

Multiple Set Control—Data Mode

4.31 Data Auxiliary Set 804K provides hold, talk, and test mode functions and spare, service, and utility line control for multiple set installations using up to 16 Data Sets 403D-type. A 1B data mounting is used as an interconnecting point for data, spare, service, and utility lines with the DAS 804K and with the basic receiver. The 1B data mounting also provides jacks for plugging in a KS-15900 interruptor, up to three 400D key telephone units (KTUs) and a power supply. The interruptor contains motor-driven cams which actuate switches to provide flash and wink indications.

>   *Note:* The *flash* indication is defined as a lamp having an *on* period equal to the *off* period, with a duration of 1 second per cycle. The *wink* indication is a 2-1/2 pulse-per-second signal with an *on* time of 370 milliseconds and an *off* time of 30 milliseconds.

The basic control functions for the multiple set installation from tip-ring to the customer interface cord are shown in Fig. 31 and either 32 (CC), 33 (BCM), or 34 (ASCII). To simplify the drawing, only line 1 is shown in Fig. 31. The other 15 lines operate in a similar manner. For details on the 400D KTU, refer to Section 518-215-125.

4.32 Incoming line 1 tip is connected to J11-26, J1-19 (CT) to terminal 36 of the MCC CP AR462, through operated make contact K7-1 and unoperated break contact K5-2 to terminal 32. From terminal 32, CT connects to terminal 22 of the line control circuit (LCC) CP AR422 and through unoperated break contact K1-2 (C relay) to the ring detector bridge circuit. The opposite corner of the bridge (CR) connects through break contact K1-1 and leaves the LCC on terminal 28. From terminal 28, CR connects to terminal 24 of the MCC then through unoperated break contact K5-3, operated make contact K7-4, and unoperated break contacts K2-2 and K1-3 and out of the MCC on terminal 25 and to J1-1. The CR lead then connects through J1B-1 on the 1B data mounting and leaves on J11-18, where it connects to line 1 ring. [Note that only relay K7 has been operated to this point; K7 is the only relay that is operated on the MCC in the data mode].

4.33 Assume that a call comes in on line 1. In the normal (data) mode, the ringing signal is directed to the ring detector as described in 4.32. Ringing is detected and operates R relay K4. Operation of relay K4 indirectly causes LB relay K5 to operate. If the customer DTR lead is operated and if option Y (auto answer) is installed, ground will be applied through contacts 2 and 6 of the LB relay to C relay K1, causing the C relay to operate. Operation of the C relay transfers the line 1 tip away from the ring detector and to the H relay (K2). Central office battery line current now flows through transformer T1 and the H relay, causing it to operate. The C relay remains operated through make contacts 2 and 5 of the H relay after the LB relay releases. Meanwhile, contact K1-3 transfers ground to lead 3 of the LCC and through K4-1 break contact on the MCC, supplying a steady *on* signal for lamp L1, indicating that a data call is present on line 1. From this point on, the data set functions as in 4.05 through 4.23. If the customer DTR lead is not operated, or if power is not applied to the data set, the C relay will not operate.

Multiple Set Control—Talk Mode

4.34 The talk mode in multiple data stations is entered by various means, depending on the type of data set and the application. For Data Sets 403D3 and 5 (MD), and 403D9 and 11 with

option B installed on the MCC (line intercept under business machine control), the talk mode can only be entered if the attendant lead is turned on by the business machine (lead 15 on the interface cord). The talk mode may be entered from either DAS 804K or a CALL DIRECTOR, if used. The associated line lamp on either or both sets will light steadily when in the data mode. When the attendant lead is operated by the business machine while the data set is in data mode, current will flow through LS relay K3-1 make contact on the LCC, operating relay K4 on the MCC. Contact K4-1 on the MCC transfers from steady ground to the flashing ground lead (provided by the KS-15900 interruptor) on J1B-24 of the 1B data mounting, causing the line lamp to go from steady to flashing. The flashing lamp provides a visual means of summoning an attendant. Also, make contact K4-2 closes, conditioning the circuit for transfer of the telephone line away from the data set and to the DAS 804K and/or the CALL DIRECTOR.

4.35 For Data Sets 403D3, 5, 7, 9, 11, and 13, with option E incorporated, transfer from the data mode to the talk mode can be accomplished regardless of the condition of the attendant lead (not present on ASCII sets). Option E provides continuity from relay K1 winding to MCC terminal 6, which was provided by relay contact K4-2 in the case of business machine control (Fig. 31).

4.36 Lifting the telephone handset and pushing the L1 key on DAS 804K (or the CALL DIRECTOR) places a ground on terminal 6 of the MCC, causing relay K1 to operate. When relay K1 operates, K1-2 make contact closes, causing relay K2 to operate. Operation of K2-3 break contact opens the ground previously applied to K7, causing it to release. This, in turn, transfers line 1 tip away from the data set and to the DAS by the operation of K7-1. Meanwhile, make contact K1-4 bypasses K1-3 and K2-2 break contacts, while release of K7-4 break contact transfers line 1 ring to terminal 22 and over to the DAS. Transfer of line 1 away from MCC terminals 24 and 32 causes the H relay in the LCC to release, returning the data set to the idle state. Relay K3 in the LCC is released, breaking the ground supplied through K3-1 make contact to relay K4 in the MCC. With option B, relay contact K4-2 now opens, but relay K1 remains operated through now-released K7-3 break contact. If the attendant lead is operated, relay K4-1 make contact opens, removing the interrupted ground (flashing signal) from line lamp

L1 on DAS 804K and/or the CALL DIRECTOR. Meanwhile, relay K1-1 make contact provides a steady ground on lead 7 of the MCC, causing L1 to become steady on. The only MCC relays operated in the TALK mode are K1 and K2.

Multiple Set Control—Hold Condition

4.37 Depressing the HOLD key on DAS 804K opens the ground from J9-17 of the data mounting to terminal 6 of the MCC, placing the line in the *hold* condition (Fig. 31). Since line key L1 is not released until the HOLD key is released, continuity between terminals 7 (KT) and 22 (KR) of the MCC is maintained through the apparatus unit of DAS 804K. When ground is removed from terminal 6 of the MCC, relay K1 releases. This causes make contact K1-2 to open; however, K2 does not release immediately because of the slow-release feature provided by capacitor C1 and resistor R3 bridged across relay K2 winding. With relay K1 released, CO line current flows from the tip side of the line to terminal 36 of the MCC, through K7-1 break contact to terminal 7 of the MCC, and out of the basic receiver on J1-21. Current now passes through the data mounting and out on terminal J10-26, through the not-yet-released L1 locking key (the HOLD key is still depressed), and into the network at terminal F; current leaves the network on terminal C, flows through L1 key to terminal J10-1; from J10-1 through the data mounting and out on terminal J1B-3. Next the current enters the MCC on terminal 22, flows through break contact K7-4, through relay K9, resistor R1, break contact K1-4, and to the ring side of the line at terminal J1-1. Relay K9 now operates by current supplied by the CO. Relay make contacts K9-2, 5 close, operating relay K6. Relay K6-1 make contact now closes, providing a low-impedance path across tip and ring (terminals 36 and 25 of the MCC), which effectively shorts the apparatus unit in DAS 804K. The line holding circuit now consists of make contact K6-1, relay winding K9, resistor R1, and break contact K1-4. When relay K6-3 make contact operates, a path to ground is reestablished for relay K2, which keeps relay K2 operated. The transfer sequence just described is sufficiently fast so that relay K2 is held continuously operated by the slow-release feature supplied by C1-R3. Meanwhile, release of K1 transfers terminal 23 of the MCC through operated make contact K1-1 from steady ground to lead 37, which provides interrupted ground for the wink indication to lamp L1 in the DAS. The

wink indication is also applied to the HOLD lamp in the DAS from the 400D KTU in the data mounting through terminal J1-32, to terminal 35 of the MCC, through operated make contact K6-4 to terminal 38 of the MCC, then through the data mounting on terminals J1-26 and J9-14 to the HOLD lamp. The L1 key is released by release of the HOLD key; this disconnects the apparatus unit from tip and ring of the line at J1 terminals 3 and 21. Relays K2, K6, and K9 in the MCC are operated in the hold condition.

Multiple Set Control—Return to Talk Mode from Hold Condition

4.38 Return to the talk mode from the hold condition is accomplished by depressing the L1 key again, which reapplies ground to terminal 6 of the MCC, through break contact K7-3 to relay K1, causing relay K1 to operate. Operation of K1-4 causes relay K9 to release, which releases relay K6. Release of the K6-4 make contact removes the wink indication from the HOLD lamp; operation of relay K1-1 also transfers the L1 lamp from wink to steady ground. With K1 operated, all other circuits return to the condition for talk mode, as described in 4.34.

4.39 Hanging up the handset or depressing another line key on the DAS or CALL DIRECTOR opens the circuit from the apparatus unit in the DAS to terminals 3 and 21 of J1; this also opens the ground circuit on terminal J1-5. All circuits return to the idle state, with only relay K7 on the MCC operated.

Multiple Set Control—Return-to-Data Feature

4.40 It is not presently possible to return to the data mode from the talk mode when using the DAS 804K. If the application of a particular installation requires returning to the data mode from the talk mode, this may be accomplished by using a CALL DIRECTOR that has been modified to provide this feature, and a 1B3 data mounting. In returning to data mode from the talk mode, the objective is to transfer tip and ring away from the apparatus unit and back to terminals 22 and 28 of the LCC with no interruption in line current (interruption of line current would cause the holding relay to drop, thus losing the call). When the DATA key on the CALL DIRECTOR console is depressed, the ground on terminal J1-5 is removed and placed on terminal J1-14, causing relay K1 to

release and relay K8 to operate. The apparatus unit in the CALL DIRECTOR is not immediately removed from the line, since it must hold the line until the LCC can perform this function. The delay in releasing the apparatus unit from the line is accomplished by using the slow-release network C1-R3 connected across relay coil K2 (Fig. 31). When K1 releases, K2 is delayed in releasing by the action of C1 and R3. Since relay K7 is controlled by the K2-3 break contact, it will also be delayed in releasing. Hence, K7-1 and K7-4 will be delayed in disconnecting the apparatus unit from the line. During this delay interval, make contact K8-1 connects MCC terminal 25 to 24, while make contact K8-1 connects MCC terminals 36 and 8. This causes part of the line current to flow through H relay K2 and transformer T1 on the LCC. H relay contacts 2 and 5 energize the C relay which again connects DT (terminal 22 on LCC) to the line. After relay K2 does release, relay K7 operates. The K7-2 break contact now causes relay K8 to release, and break contacts K7-1 and K7-4 release the CALL DIRECTOR apparatus unit from the line. Operation of make contact K8-3 causes the 1.1-second timer on the LCC to reset and the K8-3 break contact starts the timer, causing the 2025-Hz answer tone to be transmitted. After the answer tone, the data set is again ready to receive data.

Multiple Set Control—Entering Test Mode

4.41 The test mode is entered by first taking the handset of the DAS or remote console off-hook and depressing the SER (service line) key. Momentarily depressing the associated nonlocking test key (T1) applies ground to terminal J1-13 through the make contacts of TS relay K2 on the option board and back via the TM lead to relays K3 and K5 in the MCC, causing relays K3 and K5 to operate.

> *Note:* TS relay K2 on the option board is always operated except when in the data mode—see 4.26.

Make contact K5-4 serves as a latch to hold relays K3 and K5 operated through the TSTR break contact after the T1 key is released.

4.42 Relay make contact K3-1 connects the wink ground (J1-8) through terminal 28 of the MCC to terminal P2-37 on the interface coupler; through break contact TA-7, out of the interface

coupler on terminal P2-36 and back through terminal J1B-25 of the data mounting to terminal J9-26, then to test mode lamp T1, causing lamp T1 to wink. Meanwhile, relay contact TA-7 in the CC interface coupler (TA-8 in BCM; TA-4 in ASCII) transfers from wink ground to steady ground, causing lamp T1 to become steady on. Relay make contact K5-1 closes, applying ground to terminal J1-9, which is provided for the third-wire OOS feature.
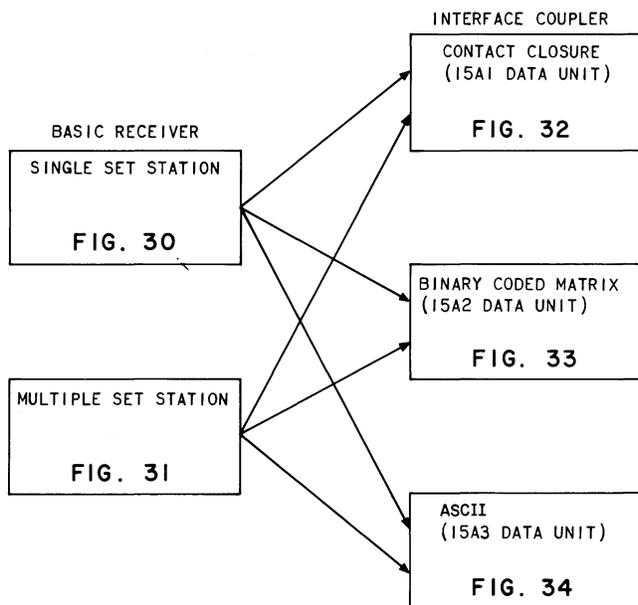
Fig. 29—Drawing Key for Figures 30 Through 34

TPA 570097

4.43 Terminals 22 (DT) and 28 (DR) of the LCC are transferred away from line 1 and to the service line by operation of relay contacts K5-2 and K5-3 respectively. DT leaves the basic receiver via terminal J1-22 (ST), passes through the data mounting, and leaves the data mounting on J11-34. DR leaves the basic receiver via terminal J1-4 (SR), passes through the data mounting, and leaves the data mounting on terminal J11-9.

4.44 Line 1 is placed out of service by terminating the line with resistor R2 through OOS option G or H on the option board (CP AR461) and relay make contact K3-2 on the MCC, which provides an off-hook or busy condition.

Multiple Set Control—Leaving Test Mode

4.45 Depressing the TSTR (test release) key on the DAS 804K transfers ground from terminal J1-10 to terminal J1-28 on the basic receiver. This provides a ground path through terminal 39, CR4, and terminal 29 of the MCC and via the TR1 lead to interface coupler terminal P2-35, then into the remote test control circuit on CP AR255, which initiates transfer of the data set out of the test mode in CC and BCM interface couplers. In ASCII sets the TR1 lead applies ground directly to the TA relay causing it to operate (Fig. 34). Diode CR4 in the MCC provides isolation so that a single TSTR key may be used to serve several data sets (Fig. 31). Momentary removal of ground from terminal J1-10 releases relays K3 and K5, which returns all other relays to their idle state (K7 in the MCC is now operated; all others in the MCC are released). A summary of the relays and their function in the basic receiver is given in Table F.
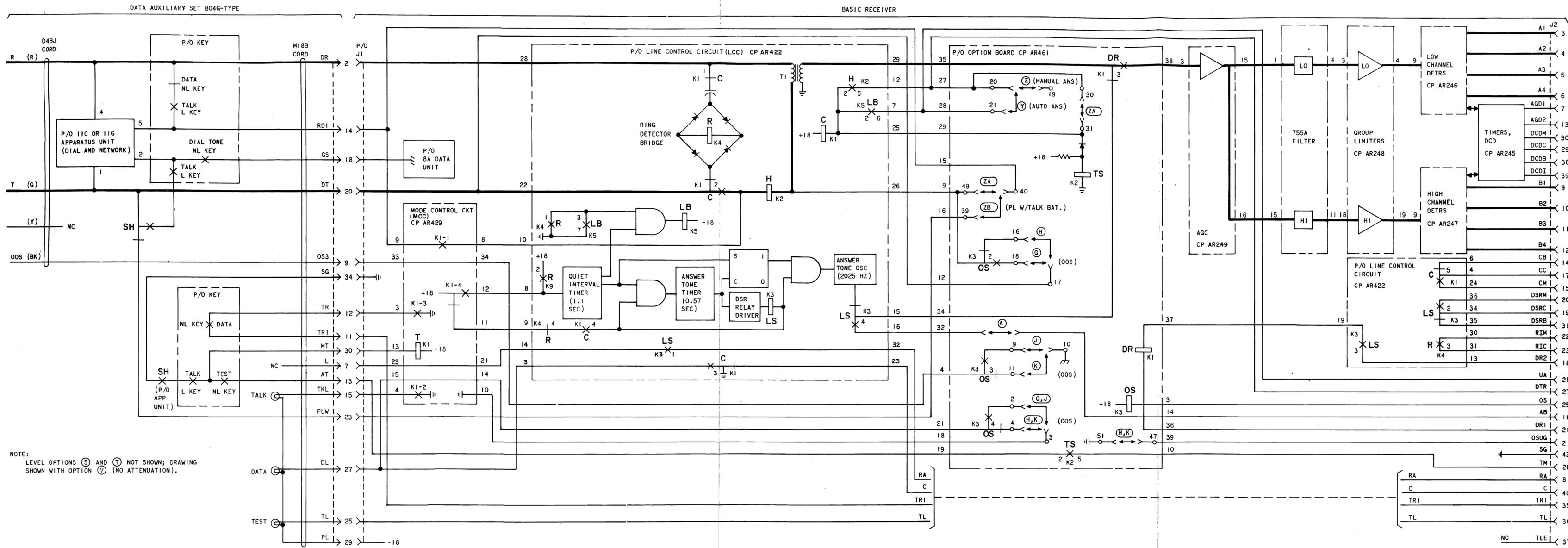
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Fig. 30—Mode Control Circuits for Single Set Use—Functional Diagram

NOTE: LEVEL OPTIONS (S) AND (T) NOT SHOWN; DRAWING SHOWN WITH OPTION (V) (NO ATTENUATION).

BASIC RECEIVER

P/O LINE CONTROL CIRCUIT (LCC)   CP AR422

RING DETECTOR BRIDGE

P/O OPTION BOARD   CP AR461

LOW CHANNEL DETRS   CP AR246

755A FILTER

GROUP LIMITERS   CP AR248

TIMERS, DCD   CP AR245

HIGH CHANNEL DETRS   CP AR247

AGC   CP AR249

P/O LINE CONTROL CIRCUIT (LCC)   CP AR422

QUIET INTERVAL TIMER (1.1 SEC)

ANSWER TONE TIMER (0.57 SEC)

DSR RELAY DRIVER

ANSWER TONE OSC (2025 HZ)

MODE CONTROL CIRCUIT (MCC)   CP AR462

TALK AND HOLD

TEST

DATA

(MANUAL ANS)   (AUTO ANS)

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Fig. 31—Mode Control Circuits for Multiple Set Use—Functional Diagram

NOTES:
1. LEVEL OPTIONS Ⓢ AND Ⓣ NOT SHOWN; DRAWING SHOWN WITH OPTION Ⓥ (NO ATTENUATION).
2. RETURN-TO-DATA LEAD, OPTION Ⓝ IS STANDARD ON 1B3 DATA MOUNTING.

Fig. 32—Contact Closure Interface Coupler—Functional Diagram
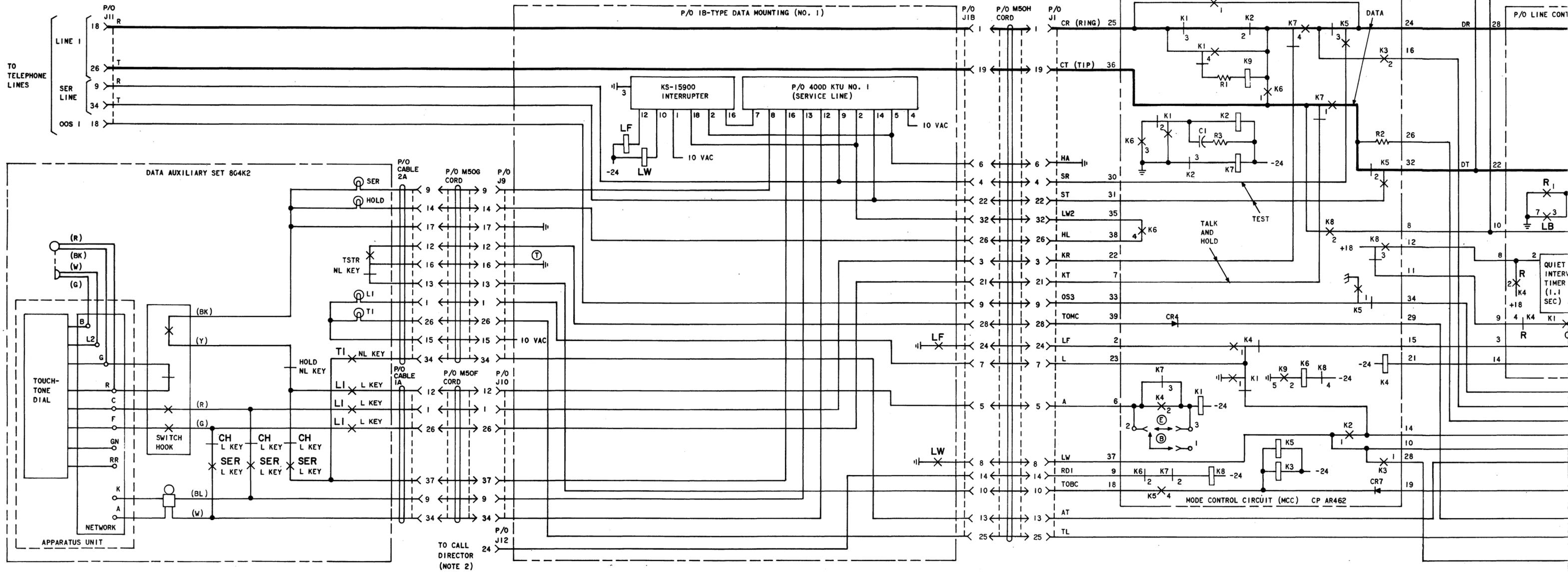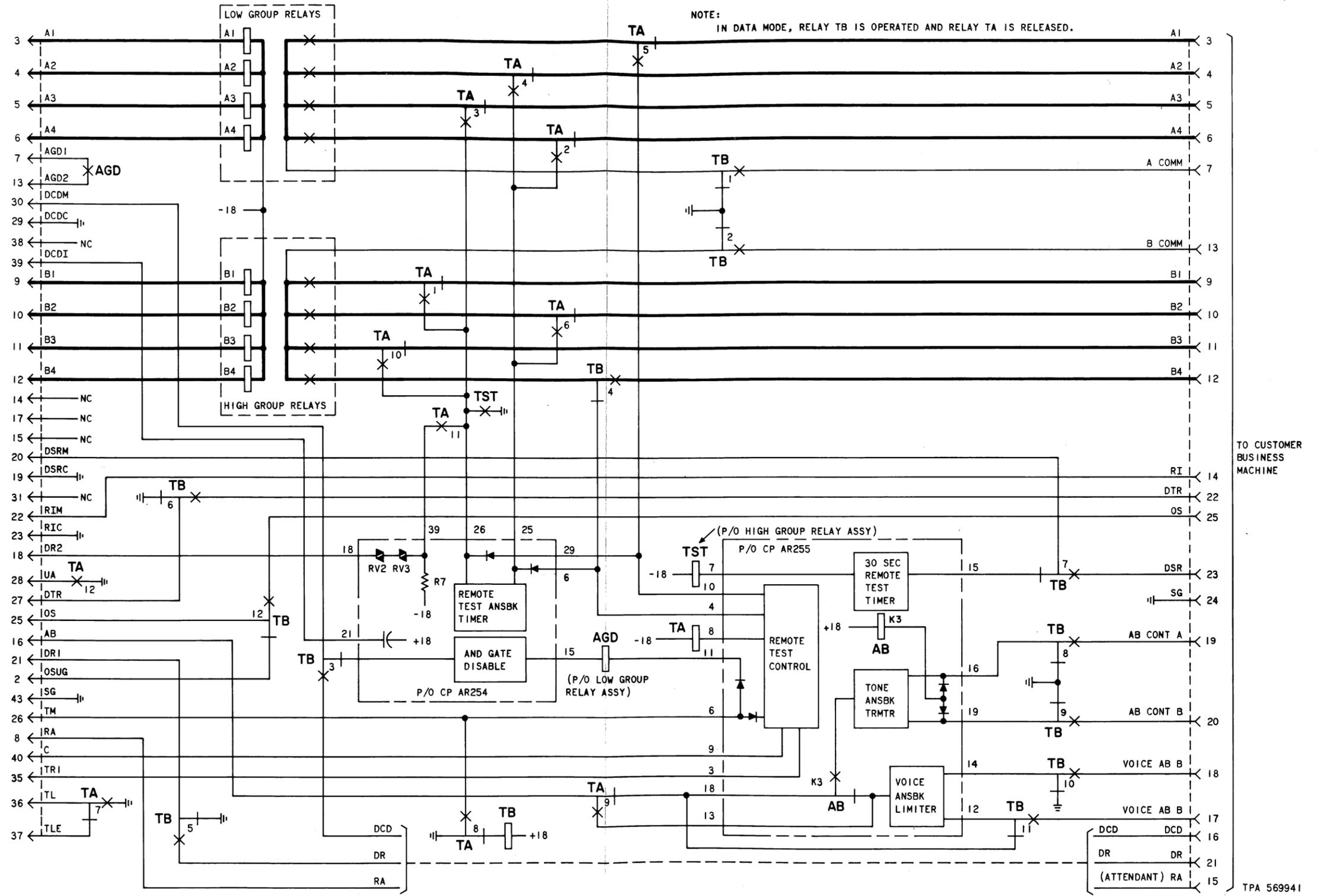
Fig. 33—Binary Coded Matrix Interface Coupler—
Functional Diagram
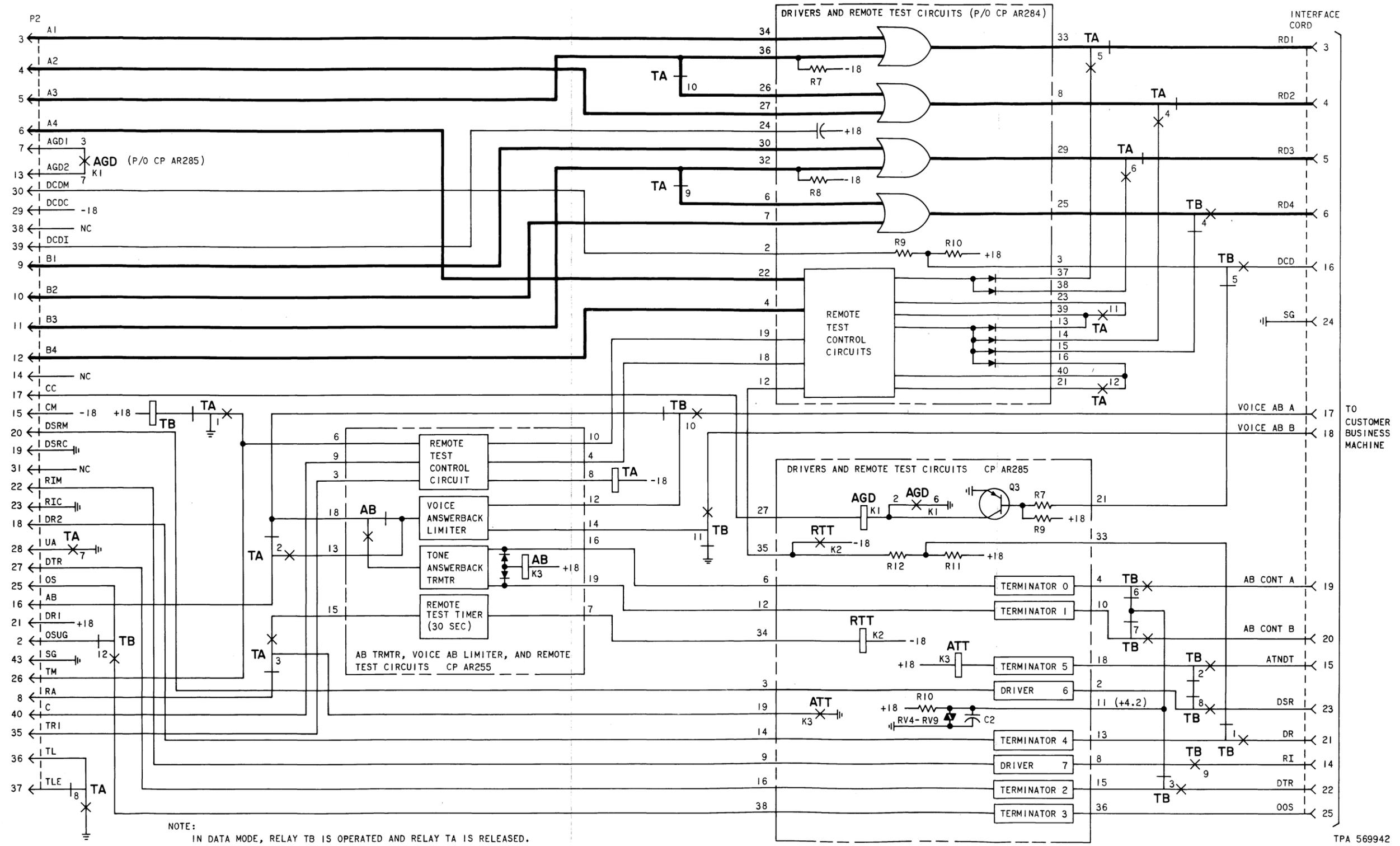
NOTE:
IN DATA MODE, RELAY TB IS OPERATED AND RELAY TA IS RELEASED.

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FORMAT TRANSLATOR CP AR287

PARALLEL-TO-SERIAL CONVERTER CP AR289

OUTPUT CP AR291

P2

CHARACTER RECOGNITION NETWORK

ASCII CHARACTER GENERATION NETWORK

BIT STORAGE REGISTER

COMMUTATOR GATES

OUTPUT GATE

INTERFACE CORD

EIA DRIVER

RD

(1) (2) (3) (4) (5) (6) (7) (8) (9) (0) (*) (#)

LOGIC DRIVER CP AR286

NC
NC
DCDM
DCDC
DCDB
NC
B1
B2
B3
B4
CB
CC
CM
NC
DSRC
DSRB
NC
NC
DR2
UA
DTR
OS
AB
DR1
NC
SG
TM
NC
C
TR1
TL
TLE

A1 A2 A3 A4

B1 B2 B3 B4

DETR
CODING MATRIX

TEST A
CS

REMOTE TEST LOGIC

CLOCK CONTROL AND PULSE COUNTING

GATED CLOCK

REMOTE TEST LOGIC

SG

TO CUSTOMER BUSINESS MACHINE

EIA DRIVER

DSR

30 SEC TIMER

RELAY DRIVER

70 MS TIMER

AB OSC (2025 HZ)

TEST MODE LOGIC AND RELAY DRIVERS

AUXILIARY CP AR290

CONTROL CP AR288

XF XG XH XJ XK XL

ANSBK AND HANG-UP CONTROL

DTR LOGIC

CHARACTER PRESENT DRIVER

VOLTAGE REG

DTR

XD XC XE

TIMEOUT CIRCUIT

PSEUDO-CHARACTER GENERATOR

INITIAL ## (C3) GENERATOR

XA XB

+5 TO ALL IC'S

REGULATOR 166A1

+18R

NOTE:
IN DATA MODE, RELAY TA IS OPERATED AND RELAY TB IS RELEASED.

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Fig. 34—ASCII Interface Coupler—Functional Diagram

TABLE F

RELAY SUMMARY—BASIC RECEIVER

NO.	USED ON CP	DESIGNATION	FUNCTION
K1	AR422	C (Connect)	Interdependent with K2 for holding line connection.
K2	AR422	H (Line Holding)	Holds line connection together with K1.
K3	AR422	LS (Line Status)	Provides "data set ready" indication to business machine after call is answered.
K4	AR422	R (Ring Detr)	Detects ringing on line and initiates automatic answer.
K5	AR422	LB (Line Bridge)	Bridges line before answer tone so that momentary loss of COB will not drop line. Essential when working into ESS offices where such interruptions do occur. This relay is not present on CP AR251 (MD).
K1	AR461	DR (Data Receive)	Transfers data set from receive mode to answer-back mode.
K2	AR461	TS (Test)	Provides test mode for multiple data set installations.
K3	AR461	OS (Out of Service)	Provides busy indication to calling party when business machine is taken out of service, or causes hunting group service (multiple installations) to bypass "busied-out" business machine port.

5. THEORY OF OPERATION—CC INTERFACE COUPLER

5.01 The contact closure interface coupler (15A1 data unit) contains two circuit packs, two AJ81 relays that are used for remote test purposes, and four A-group and four B-group data relays.

A. Data Circuits

5.02 The eight output drivers in the basic receiver (Fig. 26) connect through connectors J2-P2 to the four low-group and four high-group reed relays on the interface coupler (Fig. 32). One side of each of the A-group and the B-group relays is connected through test relay contacts and then to th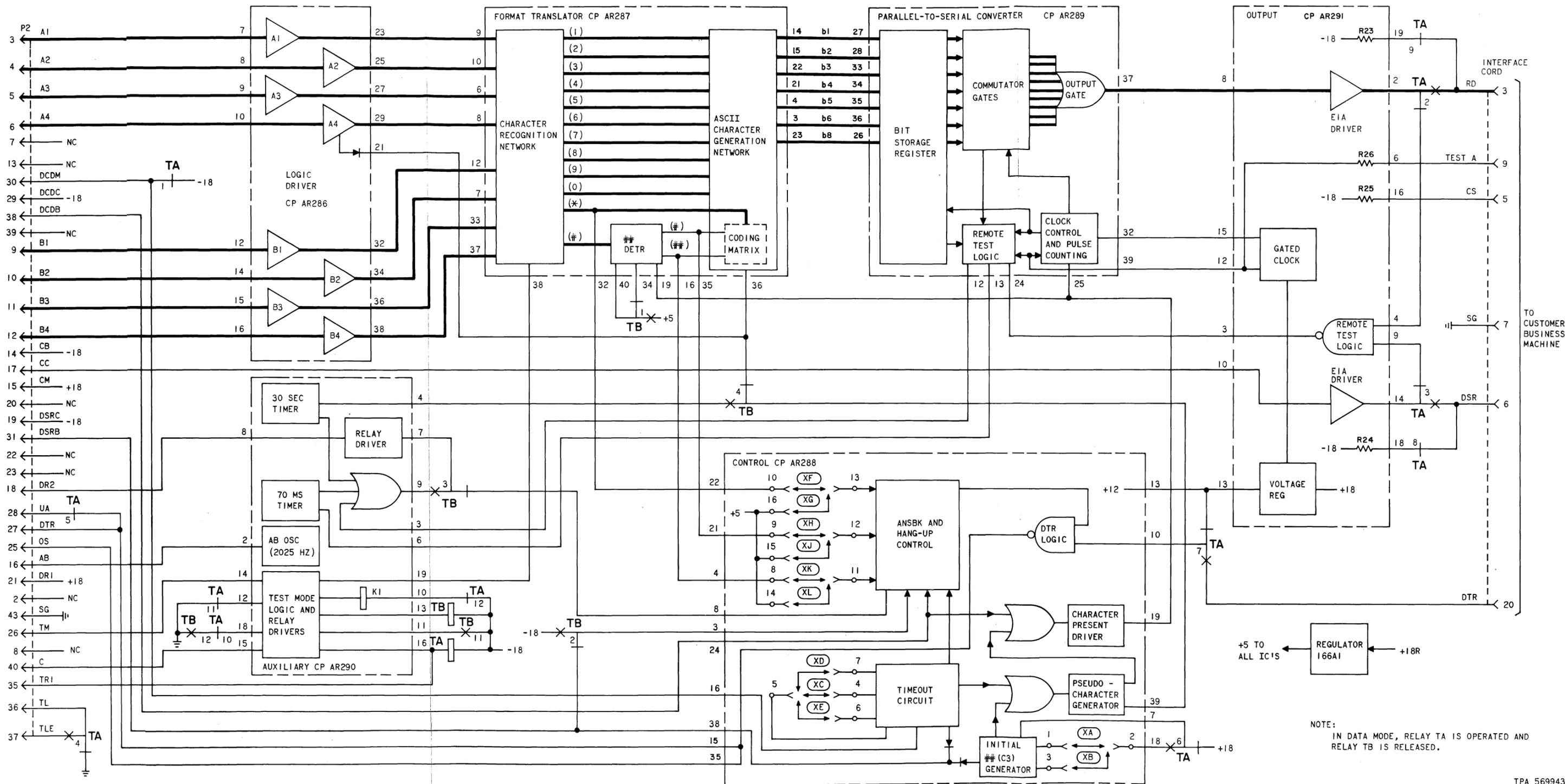e customer interface cord. The opposite sides of all A-group relays are tied together to provide an A common lead; a B common lead is similarly provided. The A and B relay contacts are protected by 185A R-C networks located on CP AR254. A diode is provided across each of the eight data relay windings to provide current surge protection to the output drivers in the basic receiver. (The diodes and R-C networks are not shown on Fig. 32).

> **Note:** In the test mode *only,* relay TA is operated and relay TB is released; in the talk and data modes, relay TB is operated and relay TA is released.

B. Data Carrier Detector

5.03 The data carrier detector (DCD) relay is located on CP AR245 in the basic receiver (Fig. 30 or 31). The common and make contacts of the DCD relay are connected to terminals P2-29 and 30, respectively. The common lead of the DCD relay is connected to signal ground in the interface coupler, while the make contact is connected to the customer business machine through terminal 16 of the interface cord. A ground indication is thus sent to the customer business machine each time the DCD relay operates. (See 4.23).

C. Tone Answer-Back Transmitter (Fig. 35)

5.04 The answer-back transmitter is an oscillator provided to enable the customer to signal the transmitting station at a rate up to 40 baud. The oscillator produces any one of four frequencies, as shown in Fig. 35; however, the 1152-Hz (rest) frequency is not coupled to the data line because AB relay K3 is not operated while the rest frequency is produced. The basic oscillator consists of the circuitry outside of the dashed-line box in Fig. 35, which produces the rest frequency. When the customer grounds either or both leads 19 and 20 of the interface cord (Fig. 32), relays K1 and/or K2 introduce additional capacitance and inductance into the oscillator tuned circuit to change the output frequency (f_o) as shown in Fig. 35. Meanwhile, AB relay K3 operates through the diode OR gate whenever either lead 19 or 20 is grounded by the customer, causing the answer-back tone to be sent out on the data line.

5.05 Transistor Q7 operates as a class A amplifier, providing sufficient gain to sustain operation as an oscillator and also produce a suitable output level. Transformer coupling is used to provide positive feedback from the emitter to the base. The transformer windings are tuned by distributed capacitance. Bias is stabilized by varistors RV8, 9, and 10, and the amplitude of oscillation is limited by varistors RV6 and RV7. Capacitor C13 reduces the gain at higher frequencies to suppress parasitic oscillations.

5.06 The voice answer-back limiter is connected to terminal 18 of CP AR255 unless AB relay

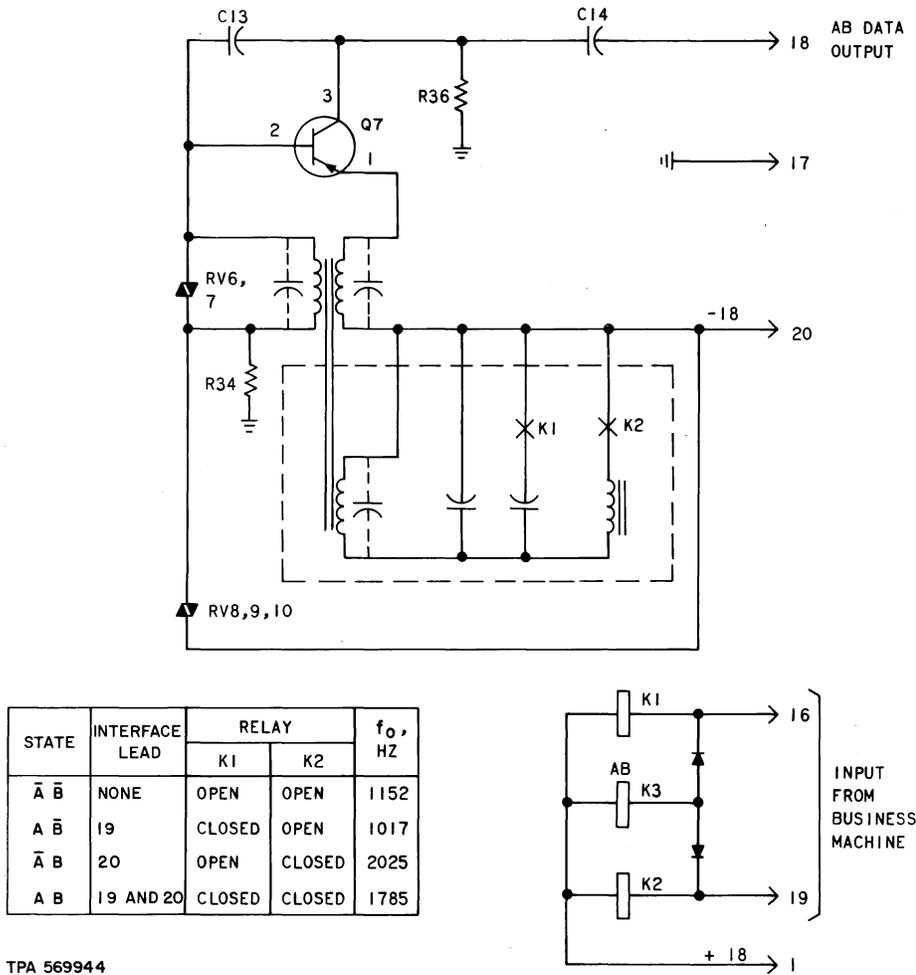| STATE | INTERFACE LEAD | RELAY | | f_o, HZ |
		K1	K2	
Ā B̄	NONE	OPEN	OPEN	1152
A B̄	19	CLOSED	OPEN	1017
Ā B	20	OPEN	CLOSED	2025
A B	19 AND 20	CLOSED	CLOSED	1785

TPA 569944

Fig. 35—Tone Answer-Back Transmitter—Simplified Schematic

K3 is operated (Fig. 32). To enter the answer-back mode, ground must be removed from the DR lead (terminal 21 of the interface cord). This automatically places the voice answer-back limiter in the circuit, provided the data set is strapped for internal answer-back [option A on CP AR250 (MD) or CP AR461 (Fig. 30 or 31)].

D. Voice Answer-Back Limiter (Fig. 36)

5.07 The voice answer-back limiter provides a means for voice response from the customer business machine, such as used in DIVA applications (see Part 1). Recommended input level to the limiter is 0 dBm into 600 ohms impedance. The limiter will accept signals up to +8 dB above the recommended 0-dBm level before peak limiting occurs. The voice answer-back channel is preempted by the data answer-back channel, by virtue of the fact that AB relay K3 operates whenever signals (ground) appear on either lead 19 or 20 of the interface coupler (Fig. 32). When relay K3 is not operated, the voice AB limiter is connected through the K3-3 break contact.

5.08 Voice signals from the customer business machine are applied over a balanced 600-ohm line through leads 17 and 18 of the interface cord, through operated TB-10 and TB-11 make contacts, (the data set is not in the test mode, so relay TB is operated) and to terminals 12 and 14 of CP AR255. Terminals 12 and 14 connect directly to

input transformer T1 of the limiter (Fig. 36). Varistor RV3 begins to limit when the input signal reaches approximately +8 dBm; if the customer input is always below this value, peak limiting is unnecessary, and will not occur. Capacitor C6 couples the signal to the base of transistor Q2. Negative feedback from the collector to the base of Q2 is provided through capacitor C7 and thermistor RT1. Since the impedance of RT1 decreases as the signal level on the collector increases, soft-limiting is provided by RT1 before RV3 begins to limit. Thermistor RT2 provides slow-acting temperature compensation for stabilizing the output level over the operating temperature range of the data station. Blocking capacitor C11 prevents direct current from flowing through thermistor RT2. Resistor R22 provides emitter bias, while resistor R15 provides the collector load. Output of the limiter is coupled through C8 and break contact K3-3 (AB relay), through connector P2-16 to the basic receiver and to the data line. The maximum output level of the limiter is −6 dBm at an impedance of about 600 ohms. The answer-back channel is provided by strapping in option A on option board CP AR461 in the basic receiver (Fig. 30 or 31). The signal then passes through K3-4 make contact on the LCC (CP AR422) and through break contact K1-3 on the option board, then to transformer T1 on the LCC. Transformer T1 matches the 600-ohm AB line to either a 600- or 900-ohm data line (option X or W, respectively, as shown in Fig. 17).
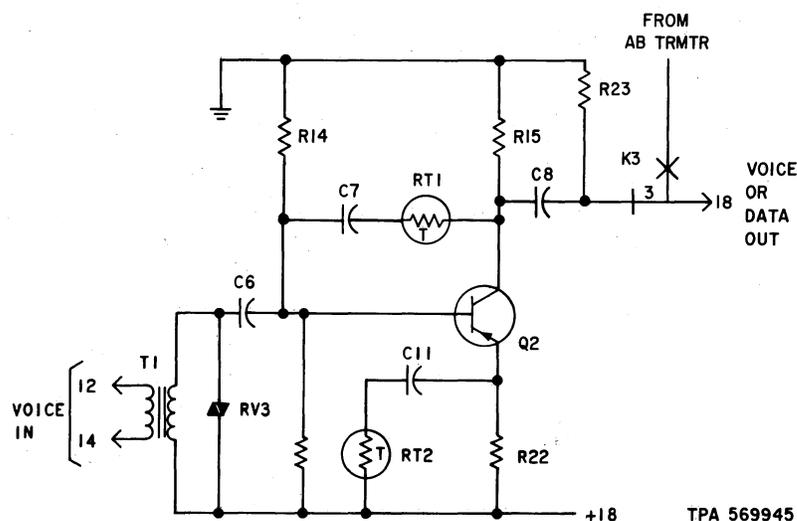

Fig. 36—Voice Answer-Back Limiter—Functional Diagram

E. Remote Test Circuits

5.09 As previously stated, remote test circuits are provided to permit remote testing of the data sets with a minimum amount of effort required by the customer. If the customer reports to the Plant Control Center a data set in trouble, a data test center will call and request the customer to perform the following functions:

(1) Place the data set in test mode.

(2) Hang up.

In case of multiple data set installations, the data set is first transferred to the service line for testing purposes. (Only one data set can be tested at a time). Some of the criteria used in designing the remote test circuit in the data set are as follows:

(1) Simplicity of use by customer.

(2) Test circuitry should be of minimum complexity so that the data circuits are being tested—*not* the test circuitry.

(3) High reliability components used in test circuitry so that the test circuitry will always function properly, thus allowing remote testing to determine condition of data set under test. (Note that TA and TB relays transfer only in test mode.)

5.10 In single set data stations, when requested by the data test center, the customer lifts the handset, depresses the nonlocking TEST key momentarily, then hangs up the handset. Control circuitry involved in entering the test mode is described in 4.30 and shown in Fig. 30 and 32.

5.11 In multiple set data stations, when requested by the data test center, the customer first depresses the SER (service line) key, then momentarily depresses the appropriate nonlocking test key (for example, T5 if data set No. 5 is in trouble) and hangs up the handset. Control circuitry involved in entering the test mode is described in 4.41 through 4.44 and shown in Fig. 31 and 32.

Remote Test Control Circuit (Fig. 37)

5.12 In either single or multiple set data stations, we now have ground applied to the TM lead (P2-26 on interface coupler). This places ground on terminal 6 of the remote test control on CP AR255 (Fig. 32 and 37), causing transistor Q1 emitter current to flow. The base of Q1 is connected to −18 volts through resistors R8, 9, 10, 11, and 13; thus the collector of Q1 goes toward ground when the Q1 emitter is grounded through varistor RV1 and diode CR6, causing the TA relay to operate. RV1 and CR6 provide bias for Q1. The TA relay is locked up by transfer of ground by TA-8 (Fig. 32). The momentary ground supplied by operation of the TEST or T1 key to initiate the test mode is no longer required to keep the data set in test mode. Diode CR3 and resistor R5 provide protection for Q1 when the TA relay is released.

5.13 Test relays TA and TB transfer alternate data relay contacts away from the customer in two groups referred to as *odd test* (OT) and *even test* (ET). Contacts in each group are operated in parallel. The common side of each group of data relays is tied to ground by release of TB1 and TB2 (Fig. 32); the other side of the data contacts in each group is connected through diodes and TA-11 make contact to pin 39 of CP AR254. Pin 39 connects to RV3 and RV2, and passes out of CP AR254 on pin 18, then connects to the DR2 lead (P2-18). The DR2 lead connects to J2-18 through LS-3 make contact to the DR relay on option board CP AR461, then to the DR1 lead J2-21 (Fig. 30 and 31). The DR1 lead is grounded by TB-5 break contact on the interface coupler (Fig. 32). A −18 volts is applied through R7 at the junction of RV3 and TA-11, which operates the DR relay. When any one of the data relays operates in test mode, ground will be applied to the RV3/TA-11 junction, shorting out the −18 volts which operated the DR relay, causing it to drop.

5.14 The data output leads designated A1, A3, B1, and B3 are in the OT group and are transferred to test mode by contacts TA-5, TA-3, TA-1, and TA-10, respectively. Data output leads designated A2, A4, B2, and B4 are in the ET group, and are transferred to the test mode by contacts TA-4, TA-2, TA-6, and TB-4, respectively. The A-group common lead is transferred to ground by TB-1; the B-group common lead is transferred to ground by TB-2. Answer-back control leads A and B are transferred to ground by TB-8 and TB-9, respectively.

5.15 The output from the answer-back transmitter is coupled to the voice answer-back limiter
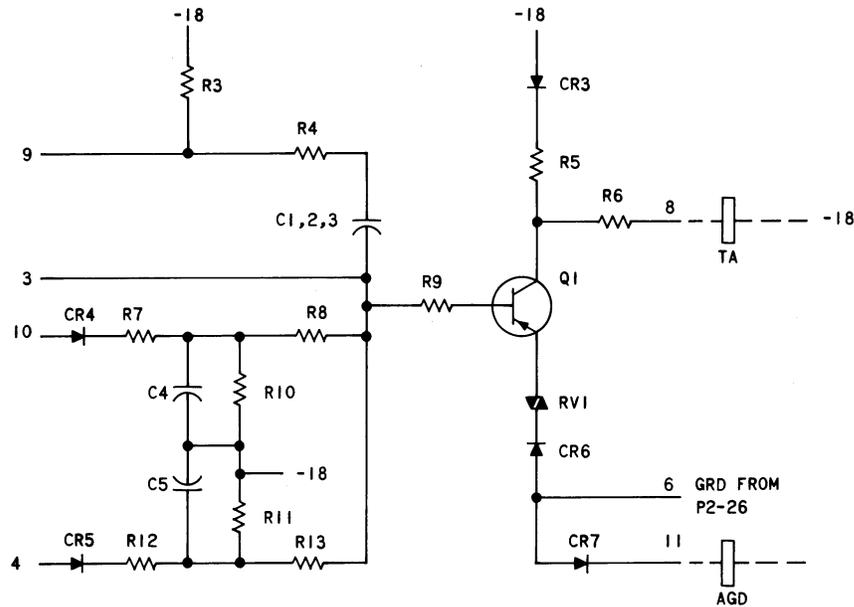
TPA 569946

Fig. 37—Remote Test Control—Simplified Schematic

AB A lead by the TB-11 break contact, while the AB B lead is grounded by the TB-10 break contact. The voice answer-back circuit is now looped around the AB transfer contact through terminal 13 of CP AR255 and TA-9 to the AB lead (P2-16). This provides a means of testing both the tone answer-back transmitter and the voice answer-back limiter.

5.16 Contact TB-7 transfers the data set ready lead from the customer to the 30-second remote test timer at terminal 15 of CP AR255 (Fig. 32). Contact TB-6 transfers the data terminal ready lead away from the customer and to ground; the UA lead (P2-28) is grounded by TA-12. This permits the data set to answer automatically in the test mode, even if the data set is strapped for attended answering (option Z). The OOS lead is transferred away from the customer by TB-12. A ground is thus applied to P2-25 so that the data set will not go out of service with option H or K applied.

30-Second Remote Test Timer (Fig. 38)

5.17 When the data test center calls the data station to test it, the LS relay (K3) on the LCC closes contact DSRM to J2-20 when the data set automatically answers (Fig. 30 or 31). A ground on the DSRM lead, which originates in the CC

interface coupler as DSRC, is now applied through break contact TB-7 to terminal 15 of CP AR255 (Fig. 32). This in turn applies ground to the junction of resistors R27 and R28 in the 30-second remote test timer (Fig. 38). Resistors R26 and R28 form a voltage divider which makes the emitter of transistor Q4 about −12 volts. The base of Q4 is initially at −18 volts, since C12 has not yet charged toward ground; thus Q4 is initially off, as is Q5. Current flow through R31 and R32 holds Q6 on. Varistor RV5 and resistor R33 prevent leakage current from tuning Q6 on. Collector current of Q6 through terminal 7 of CP AR255 operates the TST relay. This places a short through TA-11, through RV3 and RV2, and across the DR relay on CP AR461 (Fig. 30 or 31), permitting the answer-back transmitter to send a 1785-Hz tone out on the data line via the voice answer-back limiter. The data test center (DTC) operator can now measure the frequency and level of the answer-tone, thus assuring himself that the involved portion of the data set is operating properly, and also obtain an indication of line loss. After approximately 30 seconds, C12 will have charged to about 6 volts toward ground through R25 and R27. This reverses the states of transistors Q4, Q5, and Q6, so that insufficient current flows to keep the TST relay operated. When the TST relay releases, the DR relay in CP AR461 (Fig. 30 or

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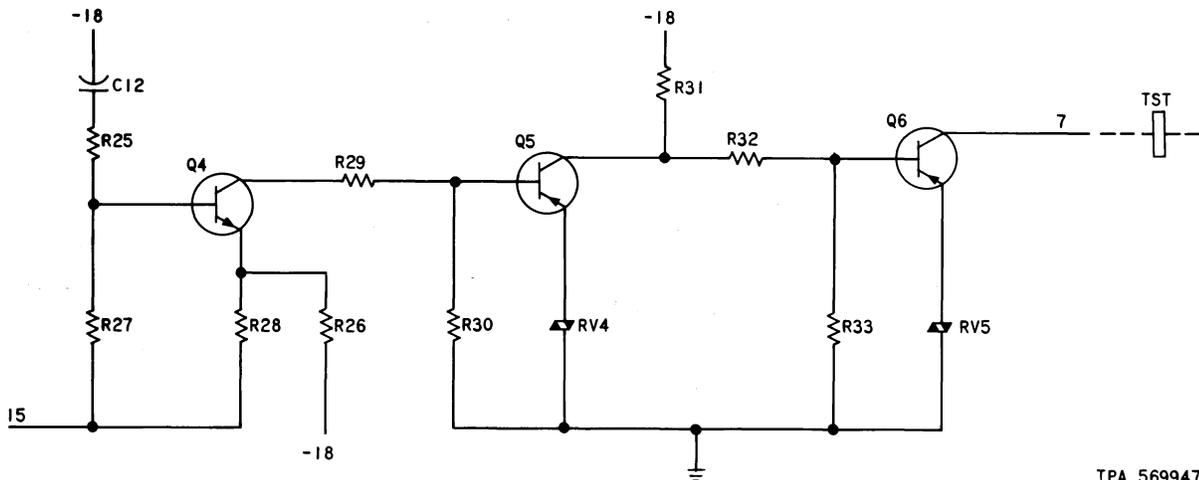
Fig. 38—30-Second Remote Test Timer—Simplified Schematic

31) operates, transferring the data set to the receive mode.

Remote Test Answer-Back Timer (Fig. 39)

5.18 To check the operating frequency ranges of the detectors, the data test center operator transmits steady tones of equal level from two oscillators. The A-group frequency oscillator is set to 697 Hz; the B-group frequency oscillator is set to 1209 Hz. (Remember that two valid frequencies are required to produce an output). The A- and B-group frequencies are first sent individually; no answer tone should be heard by the DTC operator. Both frequencies are then sent simultaneously by the DTC operator. This causes the A1 and B1 data relays to operate, closing a path to ground. This places ground on terminal 39 of CP AR254, which shorts the DR relay. This in turn causes the answer-back transmitter to send a 1785-Hz signal back to the DTC. When the DR relay is released, the input signal is removed from the receiver and the detectors will release after the 37-ms output timer times out (Fig. 27). The time the DR relay is released is controlled by the 37-ms timer plus the charge time of C3 through R5 and R7 on CP AR254 (Fig. 39), and the RC contact protection networks (not shown). For the ET group the disable period of the DR relay is controlled by the 37-ms timer, the contact protection networks, and the charge time of C2 and C3 through R4,
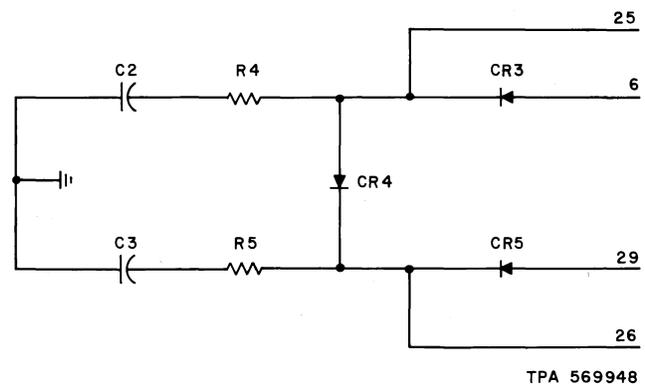
Fig. 39—Remote Test Answer-Back Timer—Schematic

R5, and R7. The OT group causes the 1785-Hz signal to be transmitted for 45 milliseconds and the ET group causes the 1785-Hz signal to be transmitted for 135 ms. Diode CR4 isolates the OT and ET groups. When the DR relay operates again, the input signal causes the detectors to operate again, repeating the process. This cycle continues to repeat until the test tone from the DTC is swept out of the A1 detector operating range. The two different answer-back pulse rates enable the DTC operator to distinguish between adjacent detectors. Resistors R4 and R5 protect the data relay contacts from capacitive surges.

F. AND Gate Disable Circuit (Fig. 40)

5.19 The DCDM lead (P2-30) is transferred away from the customer and to the AND gate disable (AGD) circuit on CP AR254 by release of relay TB-3 when the test relays TA and TB are transferred to test mode (Fig. 32). The AGD circuit is used to disable the AND gate on CP AR245 (Fig. 27). The first DCDM ground indication on P2-30 is coupled to terminal 12 of CP AR254 (Fig. 32 and 40). This ground indication passes through R1 and R2 and turns on transistor Q1. Resistor R3 and varistor RV1 provide proper bias for Q1, while capacitor C1 provides filtering for this lead. Transistor Q1 operates the AGD relay through diode CR7 on CP AR255 (Fig. 37) and to ground through operated TA-8 (Fig. 32). The make contacts of the AGD relay, which are connected to P2-7 and P2-13, short the two inputs together on the AND gate on CP AR245 (Fig. 27). Any input now on either lead will turn off Q1 and Q2 on CP AR245, starting the 23-ms signal timer.

5.20 Detector bandwidth, and to some extent receiver sensitivity, may be tested remotely by sweeping the A- and B-group oscillators at the DTC. When testing the B-group detectors, the A-group oscillator is set at 900 Hz; when testing the A-group detectors, the B-group oscillator is set at 1400 Hz.

TPA 569949
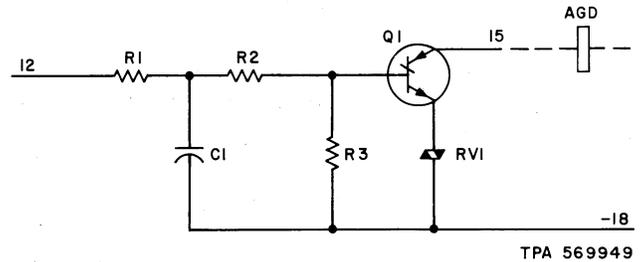
Fig. 40—AND Gate Disable Circuit—Schematic

Note: The data test center operator must be careful to avoid simultaneously sending the A1 and B4 tones until the tests are completed. This combination of tones is used to end the test mode and restore the data set to normal.

G. Ending Test Mode

5.21 Diodes CR3 and CR5 (Fig. 39) prevent any data contacts except A1 and B4 from ending the test mode. When the A1 and B4 signals are received, leads 4 and 10 of CP AR255 are grounded (Fig. 37). This causes Q1 to cut off, releasing the TA relay. This again applies ground to the TB relay at break contact TA-8 (Fig. 32), restoring the data set to data mode.

5.22 The data set can also be returned to data mode at the data station by depressing the DATA key on single data set stations, or the TSTR key on multiple data set stations.

6. THEORY OF OPERATION—BCM INTERFACE COUPLER

6.01 The binary coded matrix (BCM) interface coupler (15A2 data unit) contains three circuit packs, and two AJ81 relays that are used for remote test purposes. This unit has four data output leads instead of the eight data output leads found in the contact closure interface coupler, and uses a special 4-level binary code as previously described in 2.07.

A. Data Circuits (Fig. 41)

6.02 Signals from the eight output drivers in the basic receiver (Fig. 30 or 31) are applied through connectors J2-P2 to four OR gates on CP AR284 (Fig. 33) where the signals are translated from the 2-out-of-8 TOUCH-TONE format to the 4-level binary code that is delivered to the customer business machine. Since the four OR gates are similar in their operation, only the gate supplying output RD1 will be explained in detail.

6.03 A ground indication from either the A1 or A3 detector output driver in the basic receiver applied to terminal 34 or 36 (Fig. 41) will produce a negative output between terminal 33 and signal ground. With a customer business machine load of 3000 ohms, a -7 volt output will be developed at terminal 33 when ground is applied to either input; an open at both inputs produces a $+7$ volt output. The customer business machine load must be between 3000 and 7000 ohms; thus a voltage is always developed that meets the EIA requirement of at least 5 volts, per RS-232-B.
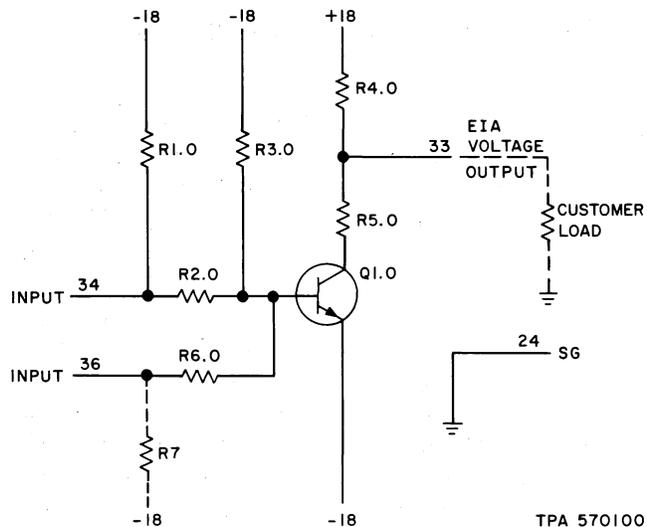
Fig. 41—EIA Voltage Driver—Schematic

6.04 Output RD1 is operated by input A1 or A3; output RD2 is operated by input A2 or A3; output RD3 is operated by input B1 or B3; output RD4 is operated by input B2 or B3 (Fig. 33). Input leads A4 and B4 are connected to leads 22 and 4, respectively, on CP AR284 and are used only for remote testing of the data set, which is discussed in 6.18. Relationships of the TOUCH-TONE input signal and the data outputs and data carrier detector output on leads RD1, RD2, RD3, RD4, and DCD are shown in Fig. 42.
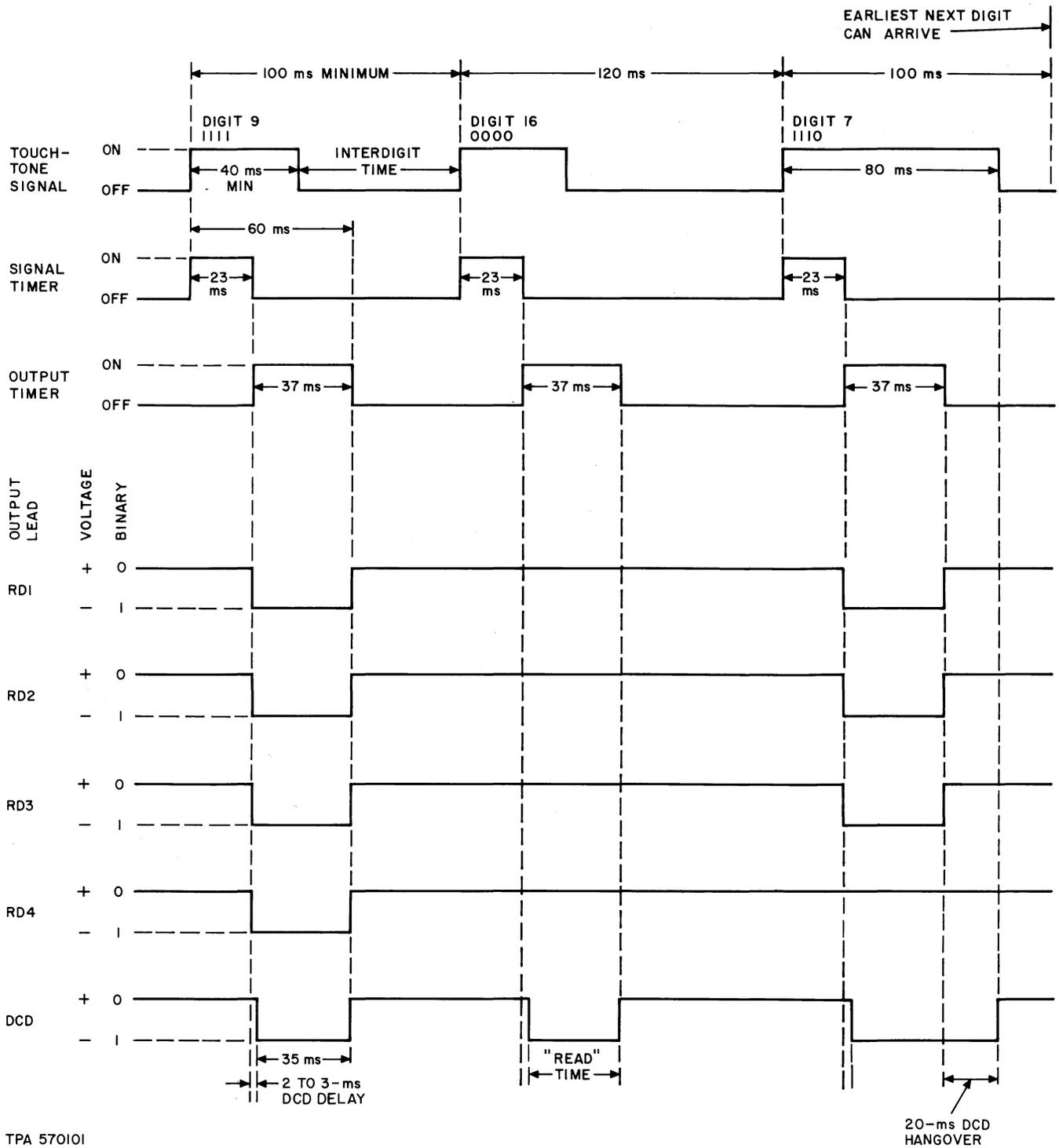
Fig. 42—BCM Input and Output Signals

TPA 570101

B. Data Carrier Detector (DCD) (Fig. 43)

6.05 The DCD signal is derived from +18 volts and −18 volts and the voltage divider R9-R10 (Fig. 43). The +18 volt signal is always present, and drops through R10 and the customer load to +7 volts when the mercury relay K1 (DCD) is *not* operated. When the "no-bounce" DCD relay operates, the −18 volt signal applied through R9 bucks the positive signal previously present at the R9-R10 junction, delivering a −7 volt DCD output signal to the customer load. The DCD signal serves as a "read" signal for the customer business machine, as described in 4.23.

C. Control Circuits

6.06 Eight control circuits are provided in the BCM interface coupler. Two of the control circuits are controlled by data set drivers (DATA SET READY and RING INDICATOR); the other six are controlled by the business machine through terminators in the data set. The terminators are as follows:

- ANSWER-BACK CONTROL A
- ANSWER-BACK CONTROL B
- DATA TERMINAL READY
- OUT OF SERVICE
- DATA RECEIVE
- ATTENDANT.

A voltage input from the business machine in excess of +3 volts will operate (turn on) any of the six terminators listed. A −3 volts produces the off condition. The drivers, in effect, translate data set ground signals to EIA voltage signals for application to the business machine. The terminators translate business machine voltage outputs to ground indications for application to the data set.

6.07 The *data set ready function* is initiated by the data set when the LS relay in the LCC operates. When the LS relay operates, ground originating at P2-19 in the BCM interface coupler (Fig. 33) is connected through the LS2 make contact in the LCC of the basic receiver (Fig. 30 or 31)

and applied through P2-20 on the interface coupler and through terminal 3 of CP AR285 to the DSR driver (Fig. 44).

6.08 Base current is provided through resistor R3.6, while R4.6 and C1.6 filter relay contact chatter. The steady-state output to the customer load (3000 ohms) is −7 volts. When ground is applied to the input of the DSR driver by the DSR relay, transistor Q2.6 operates, causing the DSR output voltage on terminal 23 of the interface cord to shift from −7 volts to +7 volts.

6.09 The *ring indicator function* is supplied to inform the business machine when the 20-Hz ringing signal appears at the data set. This function is initiated by operation of the R relay (K4-3) make contact in the LCC of the basic receiver (Fig. 30 or 31). Ground originating in the BCM interface coupler at P2-23 passes through the closed ring relay contact in the LCC, then back to the BCM interface coupler on P2-22 (Fig. 33), then to the ring indicator (RI) driver via terminal 9 of CP AR285 (Fig. 45).

6.10 Base current is provided through resistor R3.7; R4.7 and C1.7 filter relay contact chatter. The steady-state output to the customer load (3000 ohms) is −7 volts. When ringing occurs, ground is applied to the input of the RI driver by the R relay. Transistor Q2.7 operates, causing the RI output voltage on terminal 14 of the interface cord to shift from −7 volts to +7 volts.

6.11 *Answer-back controls A and B* are provided to permit the customer business machine to signal the sending station. Application of +3 volts on leads 19 and 20 of the interface cord (Fig. 33) turn on transistors Q1.0 and Q1.1, respectively (Fig. 46). When Q1.0 and Q1.1 are operated, ground is connected through terminals 6 and 12, respectively, on CP AR285 and to terminals 16 and 19 of CP AR255. This produces one of three tones which is sent out on the data line, as described in 5.04 through 5.06.

6.12 The *data terminal ready function* is initiated by the business machine by application of +3 volts on terminal 22 of the interface cord. This turns on transistor Q1.2 (Fig. 46), which applies ground at terminal 16 of CP AR285 and out of the interface coupler on P2-27 (Fig. 33).

Fig. 43—Data Carrier Detector—Functional Diagram
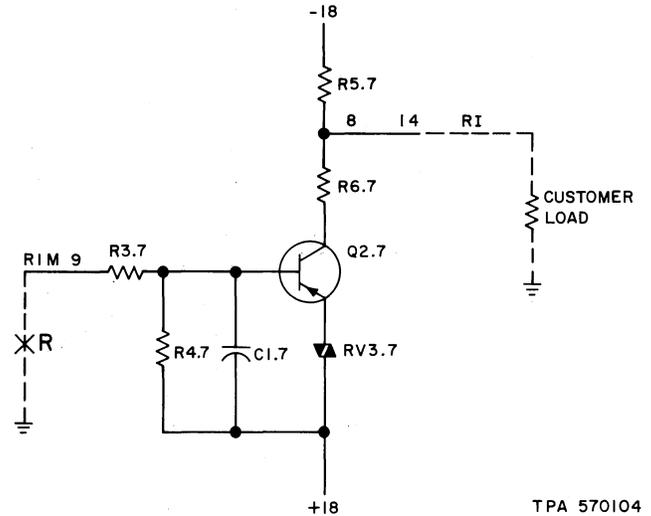
Fig. 45—RI Driver—Schematic
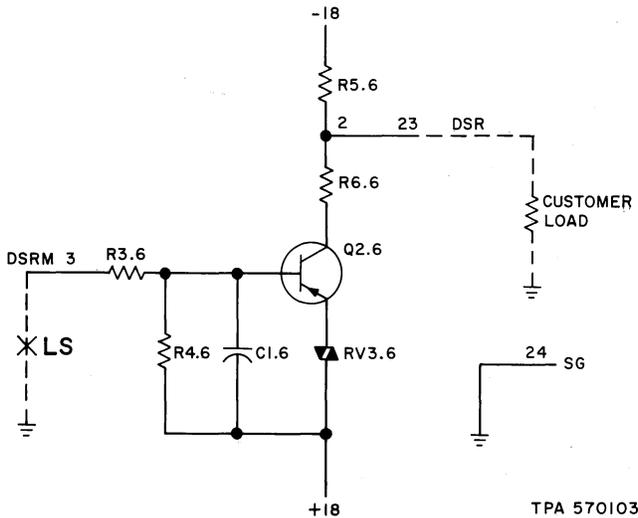
Fig. 44—DSR Driver—Schematic
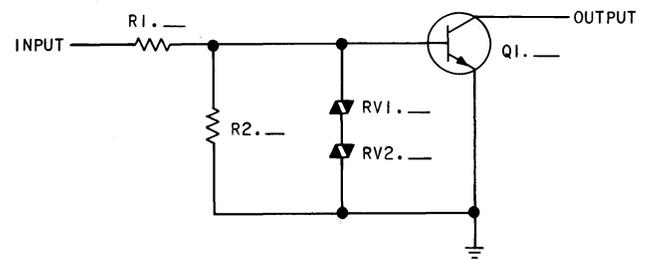
NOTE:
    COMPONENT DESIGNATION SUFFIX NUMBERS ARE AS FOLLOWS:
    ANS BK CONTROL A   0
    ANS BK CONTROL B   1
    DATA TERMINAL READY   2
    OUT OF SERVICE   3
    DATA RECEIVE   4
    ATTENDANT   5

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Fig. 46—Control Function Terminator—Typical Schematic

This permits operation of the C relay on the LCC in the basic receiver (Fig. 30 or 31), provided the H relay is operated, or if the ZA option is installed.

6.13 The *out-of-service function* is initiated by the business machine by application of +3 volts on terminal 25 of the interface cord. This turns on transistor Q1.3 (Fig. 46), which applies ground at terminal 38 of CP AR285 and out of the interface coupler on P2-25 (Fig. 33); this operates the OS relay on the option board (CP AR461) in the basic receiver (Fig. 30 or 31). If

option H or K is incorporated, a ground must be supplied to keep the OS relay operated when the data set is in the remote test mode. This ground originates on the option board (terminal 39); it is connected to the interface coupler via P2-2, and switched in by break contact TB-12 when in test mode, then connected back to the OS relay on the option board via P2-25.

6.14 The *data receive function* is used to control the mode of operation (data or answer-back) and is initiated by the business machine by application of

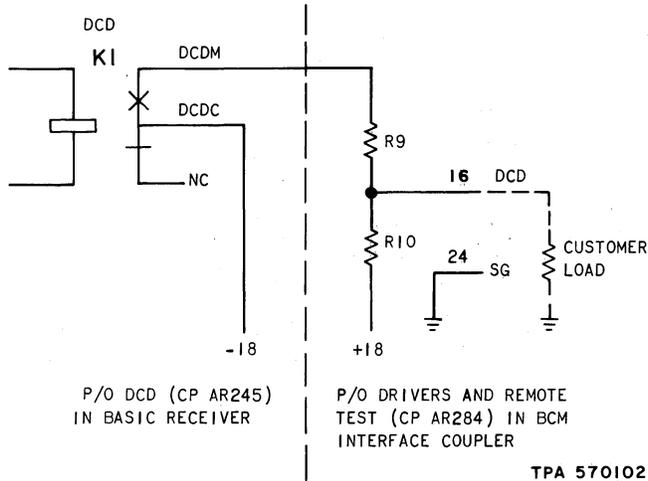of +3 volts on terminal 21 of the interface cord. This turns on Q1.4 (Fig. 46) which applies ground at terminal 14 of CP AR285 and out of the interface coupler on the DR2 lead at P2-18 (Fig. 33). The ground is then connected via J2-18 to the LS-3 make contact on the LCC (CP AR422) and to the DR relay on option board CP AR461 (Fig. 30 or 31). The opposite side of the DR relay is connected back to the interface coupler via J2-21 and then to +18 volts. If the LS relay is operated the DR relay will operate, providing operation in the data mode. A −3 volts on terminal 21 of the interface cord transfers the data set to answer-back mode.

6.15 The *attendant function* is used to summon an attendant by switching the line lamp (L1, etc) from steady to flashing condition on DAS 804K in multiple data set stations. The feature may or may not be present on the DAS 804G in single data set stations. The attendant feature is initiated by the business machine by application of +3 volts on terminal 15 of the interface cord. This turns on Q1.5 (Fig. 46) which applies ground for operation of the ATT relay on CP AR285 (Fig. 33). Operation of the ATT relay applies ground through the make contact at terminal 19 of CP AR285; this ground is connected through break contact TA-3 to the RA lead at P2-8. Lead RA passes through LS make contact K3-1 on the LCC (CP AR422) (Fig. 30 or 31). In single data set stations the RA lead leaves the LCC on terminal 14, passes directly through the MCC (CP AR429) and leaves the basic receiver on J1-7, where it *may* be used as an attendant alert (Fig. 30). In multiple data set stations the RA lead leaves the LCC on terminal 14, then enters the MCC on terminal 21, where it supplies ground to operate relay K4 (Fig. 31). When relay K4-1 operates, it transfers the associated line lamp from steady to flashing, which signals the attendant.

D. Tone Answer-Back Transmitter

6.16 The answer-back transmitter is identical in operation to the AB transmitter used in the CC interface coupler, except that the inputs operate through terminators as discussed in 6.06. For details on the AB transmitter, refer to 5.04 through 5.06.

E. Voice Answer-Back (AB) Limiter

6.17 The voice AB limiter is identical in operation to the AB limiter used in the CC interface

coupler. For details on the AB limiter, refer to 5.07 and 5.08.

F. Remote Test Control Circuits

6.18 The purpose, design criteria, and the method of entering the test mode are the same for remote test circuitry as discussed for the CC interface coupler in 5.09.

6.19 In either single or multiple set data stations, ground is applied to the TM lead (P2-26 on the interface coupler) (Fig. 33). This places ground on terminal 6 of the remote test control circuit on CP AR255 (Fig. 37), causing transistor Q1 emitter current to flow. The base of Q1 is connected to −18 volts through resistors R8, 9, 10, 11, and 13; thus the collector of Q1 goes toward ground when the Q1 emitter is grounded through RV1 and CR6, causing the TA relay to operate. Varistors RV1 and CR6 provide bias for Q1. The TA relay is locked up by transfer of ground at TA-1 (Fig. 33). The momentary ground supplied by operation of the TEST or TST 1 key to initiate the test mode is no longer required to keep the data set in the test mode. Diode CR3 and resistor R5 (Fig. 37) provide protection for Q1 when the TA relay is released.

6.20 Test relays TA and TB transfer alternate data channels in two groups referred to as odd test (OT) and even test (ET). Data channels A1, A3, B1, and B3 are in the OT group; data channels A2, A4, B2, and B4 are in the ET group. Receive data leads RD1, RD2, RD3, and RD4 are transferred away from the customer business machine by relay contacts TA-5, TA-4, TA-6, and TB-4, respectively, and connected to transistors Q4.8 and Q4.9 on CP AR284 (Fig. 47 and 48). Answer-back control A and answer-back control B leads are transferred away from the business machine and connected to +4.2 volts dc by TB-6 and TB-7, respectively (Fig. 33). The +4.2 Vdc is derived from +18 volts by the R, C, RV network in CP AR285. This turns the answer-back transmitter on; the AB transmitter will transmit 1785 Hz when the test starts. Output from the answer-back transmitter is coupled into the voice answer-back limiter by TB-10; the voice answer-back B lead is grounded by the transfer of TB-11. The voice answer-back now is bridged around the AB transfer contact through terminal 13 of CP AR255 and TA-2 to the AB lead (P2-16).

6.21 The data set ready lead is transferred away from the business machine and connected to the ATTENDANT terminator (4) on CP AR285 by release of TB-8 and TB-2 (Fig. 33); TB-2 also transfers the attendant lead away from the business machine. Release of relay contact TB-9 opens the ring indicator lead to the business machine. The data terminal ready lead is transferred away from the business machine and connected to +4.2 volts dc by release of TB-3. This provides a ground indication via P2-27 to terminal 12 of the LCC (Fig. 30 or 31). This ground causes the C relay to operate when the data station is called by the data test center for remote testing. Relay contact TA-7 supplies this ground through the UA lead (P2-28) to pin 7 of the LCC if the data set is wired for "attended" operation (option Z). Relay contact TB-12 transfers the out-of-service lead away from the business machine. If the data set is wired for option H or K, a ground is applied to terminal P2-25 so that the data set does not go out of service.

6.22 When the data test center calls the data set, the LS (K3) relay on the LCC operates, closing the DSRM contact; this applies ground to J2-20 (Fig. 30 or 31), then to terminal 3 of CP AR285 (Fig. 33). This causes transistor Q2.6 to operate (Fig. 44), producing a positive voltage out of the DSR driver (CP AR285 terminal 2), through TB-8 and TB-2 (Fig. 33) and into the ATTENDANT terminator, thus operating the ATT relay K3. Operation of the ATT relay applies ground through TA-3 make contact to terminal 15 of CP AR255. This applies ground at the junction of resistors R27 and R28 on the remote test timer (Fig. 38). Resistors R26 and R28 form a voltage divider which makes the emitter of transistor Q4 about −12 volts. The base of Q4 is initially at −18 volts since capacitor C12 has not yet charged toward ground. Thus, Q4 is initially off and Q5 is also off. Current flowing through resistors R31 and R32 hold transistor Q6 on in the steady state. Thus the RTT relay is normally operated. Varistor RV5 and resistor R33 prevent leakage from turning Q6 on.

6.23 When ground is applied to the R27-R28 junction, C12 charges toward ground; Q4 and Q5 turn on, turning Q6 off. This causes the RTT relay to release. The RTT make contact applies −18 volts dc to R12 (CP AR285, Fig. 33), resulting in −7 volts dc being applied via terminal 33 of CP AR285, TB-1 break contact, and terminal 13 to the DR terminator (4). This causes Q1.4 to

turn on (Fig. 46), giving a ground indication out of the terminator on terminal 14, which connects to the DR2 lead at P2-18 (Fig. 33). The DR2 lead connects through the LS-3 make contact on the LCC (Fig. 30 or 31) then to the DR relay coil on the CP AR461 option board. The opposite side of the DR relay coil is connected to P2-21, then to +18 volts in the BCM interface coupler (Fig. 33). Thus the DR relay releases when ground is applied by the DSR relay, applying a 1785-Hz answer-back tone to the data line as long as the 30-second timer is operated.

6.24 After about 30 seconds, C12 on the remote test timer (Fig. 38) will have charged approximately 6 volts toward ground through R25 and R27 to terminal 15. This will cause transistor Q4 to saturate, and will in turn cause Q5 to saturate. Saturation of Q5 causes Q6 to cut off, releasing the RTT relay. (This relay is identified at TST in the CC interface coupler, and is so identified in Fig. 38). This in turn causes +7 volts to be applied to the DR terminator (4) on CP AR285. Ground supplied by the DR terminator passes over the DR2 lead (P2-18) (Fig. 33), through operated LS relay contact K3-3, and to the DR relay on the option board (CP AR461), causing the DR relay to operate, thus removing the 1785-Hz answer-back tone from the data line. (The data receive channel is again connected to the line.) The answer-back tone applied to the line permits the DTC operator to measure the answer-back frequency, and by checking the level, to gain information regarding loop loss of the line being used.

6.25 To check the operating frequency ranges of the detectors, the DTC operator simultaneously transmits steady tones of equal amplitude from two oscillators. One oscillator is set to 697 Hz; (A-group) the other oscillator is set to 1209 Hz (B-group). No output will be obtained from the detectors until one valid A-group and one valid B-group frequency are applied to the detectors. With the A-group oscillator on continuously, the B-group oscillator is turned on momentarily. This will cause negative output pulses from leads 33 and 29 of CP AR284 to be applied through make contacts of TA-5 and TA-6 to terminals 37 and 38, respectively (Fig. 33 and 48). This causes relay K2 to operate, applying a −18 Vdc pulse to terminal 35 on CP AR285, then through R12 and TB-1 break contact to the DR terminator (4). This causes the DR relay on the option board (CP AR461) to release for 40 ms, returning a 1785-Hz signal to the DTC.

With the DR relay released, the input signal is removed from the receiver and the detectors will release after the 37-ms timer resets. When the data outputs on terminals 33 and 29 cease, relay K2 releases, and the DR relay again operates. When the DR relay operates again, the process will be repeated, and will continue until the DTC test tone is swept out of the operating range of the A1 detector.

6.26 When the A2 frequency range is reached, relay K1 will operate from the negative voltage applied through TA-4 to terminal 14 of CP AR284, again releasing the DR relay and returning a 1785-Hz signal to the DTC. Release of the K1 relay is delayed by the R-C network consisting of R19 and C2 (Fig. 48) so that the 1785-Hz signal duration is 135 ms. Therefore when odd group detectors are being tested, 40-ms signals are returned to the DTC; when even group detectors are being tested, the signal duration is 135 ms. This enables the DTC operator to differentiate between channels.

AND Gate Disable Circuit

6.27 The DCD lead is transferred away from the customer business machine by TB-5 (Fig. 33). The first negative DCD signal appearing on terminal 3 of CP AR284 is coupled to terminal 21 of CP AR285. This signal operates transistor Q3 which in turn operates the AGD relay. Transistor Q3 base current is supplied through R7; R9 prevents leakage current from operating Q3. The AGD relay remains operated after base current is removed from Q3 by operation of make contact K1-2, 6 to ground. The AGD relay cannot operate unless the C relay (K1) on the LCC is operated (Fig. 30 or 31), since −18 volts on P2-15 in the BCM interface coupler is passed through K1-5 make contact before being applied to the AGD relay. Therefore, when the data set is placed on-hook, the AGD relay will release. Contacts K1-3 and K1-7 of the AGD relay connect to P2-7 and P2-13, respectively, and are connected to terminals 3 and 4 of CP AR245 (Fig. 27). Thus, the AND gate will be disabled when the first DCD signal appears and operates the AGD relay. An input on either lead will now turn off transistors Q1 and Q2, starting the signal timer.

6.28 Detector bandwidth, and to some extent receiver sensitivity, may be tested by the DTC operator by sweeping the A- and B-group oscillators. When testing the B-group detectors, the A-group oscillator is set to 900 Hz; when testing the A-group detectors, the B-group oscillator is set at 1400 Hz. The DTC operator must avoid sending the A4 and B4 tones simultaneously, since this combination of tones is used to end the test mode. *If* the test mode is dropped *and* the DTR lead is not operated, the data loop connection will be lost.

6.29 Resistor R10, varistors RV4 through RV9, and capacitor C2 are used to derive a +4.2 Vdc supply from +18 Vdc for use in remote testing the data set (Fig. 33). When in test mode, this voltage is used in lieu of the EIA voltages supplied by the customer. Varistors RV1.8 through RV5.8 and RV1.9 through RV5.9 establish a threshold voltage for transistors Q4.8 and Q4.9, respectively, which provide a means of testing the data output voltages (Fig. 48).

G. Ending Test Mode Remotely

6.30 When the A4-B4 combination of tones is received, transistors Q2.4 and Q2.5 on CP AR284 operate, turning on transistors Q3.6 and Q3.7, respectively (Fig. 48). Outputs from Q3.6 and Q3.7 are coupled to terminals 4 and 10, respectively, on CP AR255 (Fig. 37). This in effect

applies ground to terminals 4 and 10, turning transistor Q1 off and releasing the TA relay. Release of the TA relay in turn operates the TB relay. Capacitors C4 and C5 provide sufficient delay for the TA relay to drop.

6.31 Another method of terminating the test mode remotely is available on the switched network. When the DTC operator hangs up, a battery reversal or interruption appears on the data line. This causes the H (K2) relay on the LCC to drop (Fig. 30 or 31), which in turn releases the C relay. The C relay contact (K1-3) supplies ground through P2-40 (Fig. 30 or 31) to terminal 9 of CP AR255 (Fig. 33 and 37). Since capacitors C1, C2, and C3 have charged to −18 volts through

R3 and R4, an 18-volt positive transient appears on the base of Q1 (Fig. 37). This turns transistor Q1 off, thus releasing the TA relay which then operates the TB relay, and removes the data set from the test mode.

H. Ending Test Mode Locally

6.32 Operating the DATA key on DAS 804G or depressing the TSTR key on DAS 804K places ground on the TR1 lead at J2-35. The TR1 lead connects to terminal 3 of CP AR255 (Fig. 33 and 37), applying ground to the base of transistor Q1, thus releasing the TA relay, which causes the TB relay to operate and restore the data set to normal condition.
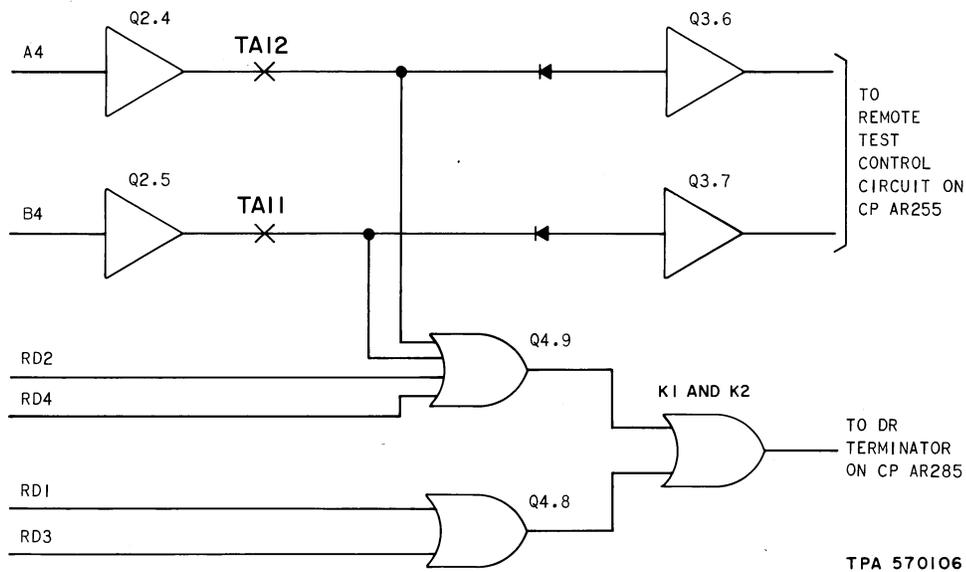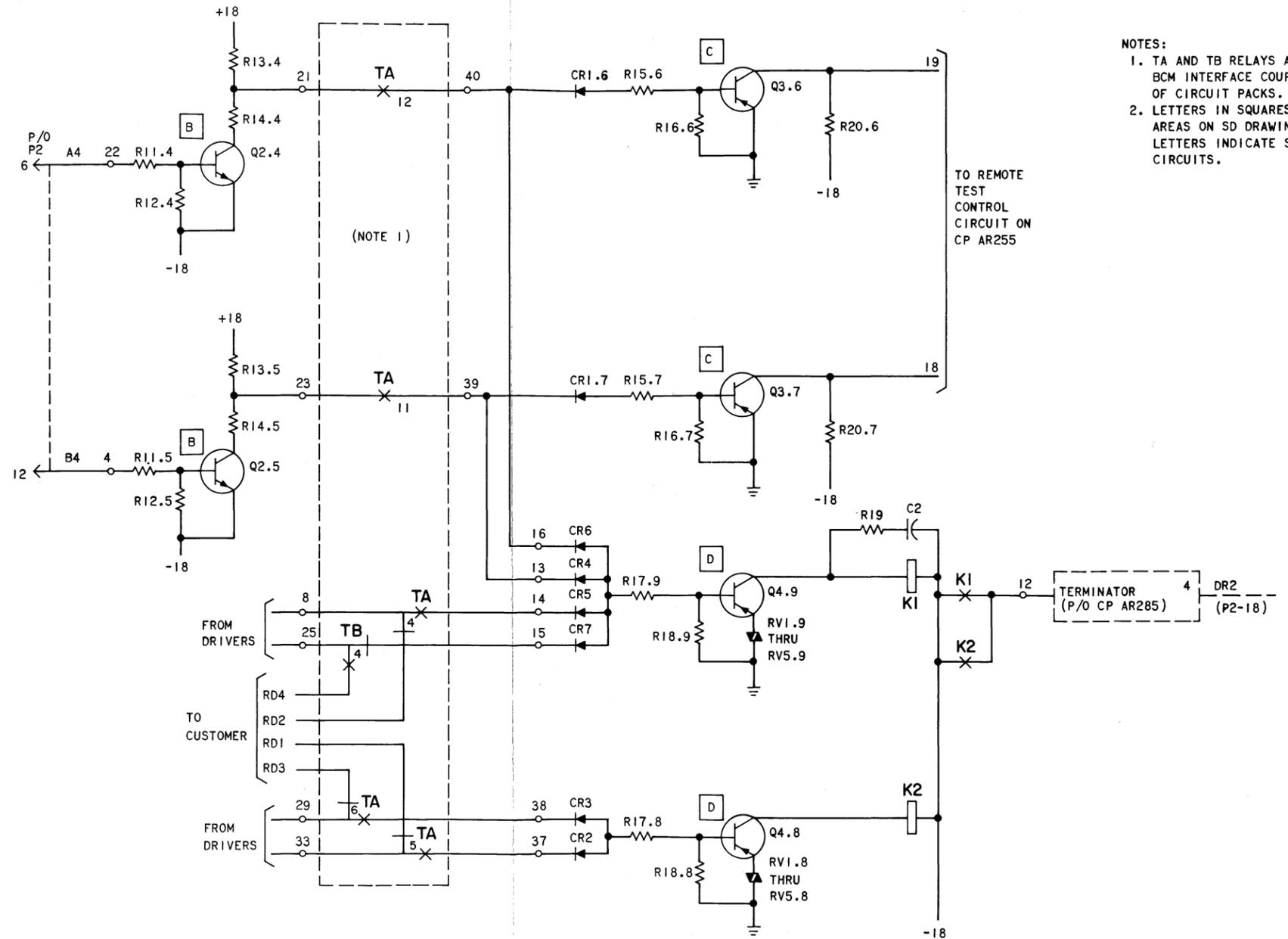

Fig. 47—Remote Test Control Circuits—Logic Diagram

NOTES:
1. TA AND TB RELAYS ARE LOCATED ON BCM INTERFACE COUPLER, OUTSIDE OF CIRCUIT PACKS.
2. LETTERS IN SQUARES INDICATE AREAS ON SD DRAWINGS; SIMILAR LETTERS INDICATE SIMILAR CIRCUITS.

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Fig. 48—Remote Test Control Circuits—Functional Diagram

## 7. THEORY OF OPERATION—ASCII INTERFACE COUPLER

7.01 The ASCII interface coupler (15A3 data unit) contains six circuit packs, two AJ81 relays that are used for remote test purposes, and a voltage regulator. Unlike the CC and BCM interface couplers, which use discrete components, the ASCII coupler relies heavily on integrated circuits (ICs). Data output from the ASCII interface coupler to the business machine is over one lead instead of four, as in the BCM interface coupler, or eight as is the case with the CC interface coupler. The ASCII output is in start-stop serial format, as previously described in 2.10. The ASCII coupler first translates the parallel 2-out-of-7 signals received from the basic receiver into parallel ASCII characters, then converts these signals into serial form. [Remember that the ASCII interface coupler accepts only 12 different signals provided by a 3 x 4 TOUCH-TONE matrix (2-out-of-7); not 16 signals produced by a 4 x 4 matrix (2-out-of-8) as received by the CC- and BCM-equipped receivers].

A. Logic Driver Circuits (Fig. 49)

7.02 Signals from the eight output drivers in the basic receiver (Fig. 30 or 31) are applied through connectors J2-P2 to the logic driver circuits on CP AR286 (Fig. 34). The eight logic driver circuits are identical except for component markings and the extra input to transistor Q2 in the A4 driver (Fig. 49). This extra input is used for test purposes and is discussed later in 7.67. The logic driver circuits are used to shift the incoming data signals from the basic receiver to a form suitable for driving ICs on the format translator (CP AR287). Because of their similarity, only the A1 driver is discussed in detail.

7.03 Incoming A1 lead is connected to terminal 7 of the logic driver, and through resistor R1.0 to transistor Q1.0 (Fig. 49). With no signal applied, Q1.0 is biased to the off state by resistor R2.0. With Q1.0 off, Q2.0 is saturated, and the output at terminal 23 is about +0.1 volt.

7.04 When the A1 detector in the basic receiver applies a signal to Q1.0, the voltage at terminal 7 is clamped at about -2 Vdc. This causes Q1.0 to saturate. With Q1.0 saturated, Q2.0 turns off, producing an output of about +5 Vdc at terminal 23. Thus, a "detector on" signal produces a +5 volt output and a "detector off" signal produces a +0.1 volt output.
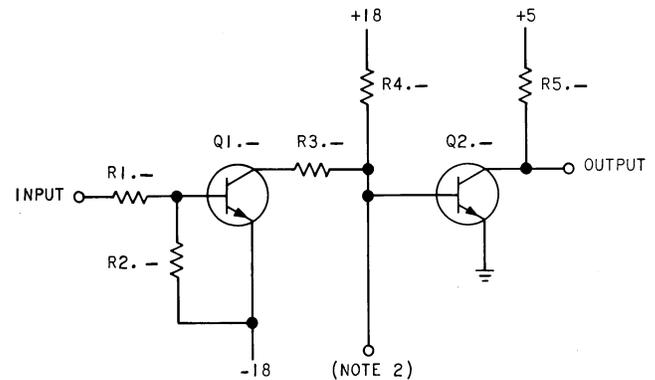
NOTE:
1. COMPONENT DESIGNATION SUFFIX NUMBERS ARE AS FOLLOWS:

DRIVER	SUFFIX	DRIVER	SUFFIX
A1	0	B1	4
A2	1	B2	5
A3	2	B3	6
A4	3	B4	7

2. NO CONNECTION ON THIS LEAD EXCEPT ON A4 DRIVER.

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Fig. 49—Logic Driver—Schematic Diagram

B. Format Translation Circuits (Fig. 50)

7.05 Signals emerging from the logic driver are still in the 2-out-of-7 TOUCH-TONE format. The purpose of the format translator is to convert the 2-out-of-7 signals into 1-out-of-12 signals, corresponding to the 12 buttons on the TOUCH-TONE dial. The logic gates that perform this function are IC NAND gates (Fig. 50). When *all* inputs are in the logical 1 state (> 2.4 volts) the output is in the logical 0 state (< 1.0 volt); when one or more inputs is in the logical 0 state (< 1.7 volts) the output is in the logical 1 state (> 3.4 volts).

7.06 Each IC contains two or more logic elements. To distinguish between elements for purpose of discussion, each gate is identified by its package number and output terminal number. For example, a gate identified as A4-12 means the gate in package A4 having its output on terminal 12. Further, designations used in text and illustrations are for standard-code IC packages, having terminal numbers from 1 through 16. To convert these standard-code designations to F-code (WE) designations, use the following formula:

F-code terminal number = 17 minus standard-code terminal number.

Stated another way, the standard-code numbers are in numerical sequence from 1 through 16; the corresponding F-code numbers are in numerical sequence from 16 through 1. (Both standard-code and F-code ICs have been used in ASCII sets).

7.07 Gates in IC packages A5, A6, and A7 have their inputs connected to the logic driver outputs for detectors A1, A2, A3, A4, B1, B2, and B3 in such a way that when one A-group and one B-group signal appears as a logical 1, only one gate output will go to logical 0; all other gate outputs will remain in the logical 1 state. Thus, the 2-out-of-7 signals are converted to 1-out-of-12 signals, representing the 12 possible signals from the TOUCH-TONE dial. These gates are referred to as the character selector gates.

Digit Translation

7.08 Outputs from the 12 character selector gates are connected to IC packages A1, A2, A3, and A4 in such a manner that the proper ASCII character appears at the gate output for each of the 12 input characters (Fig. 50). However, outputs for the * and # are not coded directly, as explained in 7.11 through 7.18. Gates A3-12, A3-14, A2-14, A2-12, A1-14 and A1-12 are wired to produce ASCII bits b1 through b6, respectively. Gate A4-12 is wired to produce an even parity bit. Since all gates function in a similar manner, only gate A6-3 is described in detail. The output of this gate goes to 0 only if the digit 7 is received by the data set. The output of gate A6-3 is wired to input terminals of gates A3-12, A3-14, A2-14, and A4-12 so that each of these gates has a 0 input whenever the digit 7 is received. Thus, the output of each of these gates will be 1 whenever a 7 is received. Therefore, bits b1, b2, and b3 and b8 (parity bit) will be 1 for the digit 7, as assigned by the ASCII code (Table G). Bits b4 and b7 must be 0 to produce the digit 7; a 0 output requires a 1 input from the detectors. Thus, generation of all bits for the digit 7 except b5 and b6 have been explained. Bits b5 and b6 must be 1s to satisfy the ASCII code for any digit 1 through 9. Receiving any digit 1 through 9 is logically the same as *not* receiving a *, 0, or #, and is represented by detector A4 (lead 8, Fig. 50) being off (ie, not on). The A4 lead is wired directly to the inputs of gates A1-14 and A1-12, so that bits b5 and b6 are 1 whenever detector A4 is not on.

7.09 Coding of the ten digits 0 through 9 is essentially the straightforward process just described for the digit 7. However, the A2 detector is on only when a 4, 5, or 6 is being received (TOUCH-TONE dial insert, upper left, Fig. 50). Each of these digits requires a 1 output for the ASCII b3 bit. Therefore, the A2 input to the format translator is wired through an inverter gate (A4-14) to an input of A2-14 so that bit b3 is 1 whenever the A2 input is 1 (Fig. 50).

0 Translation

7.10 The digit 0 also requires that bits b5 and b6 be 1s. This requirement is satisfied in the same manner as for the other digits, as described in 7.08. (Note that all digits 0 through 9 are translated to ASCII format without use of the coding matrix.)

* Translation

7.11 Encoding the * (A4, B1) is accomplished in a manner similar to that used for the digits 0 through 9, except that the output of the selector gate (A 6-5) is wired to the CODE 1 bus of the coding matrix, rather than to a coding gate input. By positioning straps on the coding matrix, any one of the 64 ASCII characters can be chosen as an output for the * input (Table G). The output of A6-5 is also connected to terminal 32 (Fig. 50), which is connected to the answer-back control circuit on CP AR288 (Fig. 34).

7.12 Diodes CR1 through CR8 are connected to the coding gates as input expanders to increase the effective fan-in to the gates (Fig. 50). The cathode end of each diode is logically and electrically equivalent to the other inputs to which the gates are connected.

 # Translation

7.13 Translation of the # (A4, B3) is handled in a manner different from all of the other characters, to permit generation of a thirteenth character output with only twelve character inputs. The output of the # selector gate (A7-3) is connected to the input of the ## detector circuit, which consists of ICs A8, A9, and A10 (Fig. 50). This circuit permits the first of two consecutive #s to be coded

TABLE G

ASCII CONTROL AND PRINTING CHARACTER OPTIONS AND CODES

CONTROL CHARACTER	B1	B2	B3	B4	B5	B6	B7	B8	PRINTING CHARACTER	B1	B2	B3	B4	B5	B6	B7	B8
NUL	0	0	0	0	0	0	0	0	SP	0	0	0	0	0	1	0	1
SOH	1	0	0	0	0	0	0	1	!	1	0	0	0	0	1	0	0
STX	0	1	0	0	0	0	0	1	"	0	1	0	0	0	1	0	0
ETX	1	1	0	0	0	0	0	0	#	1	1	0	0	0	1	0	1
EOT	0	0	1	0	0	0	0	1	$	0	0	1	0	0	1	0	0
ENQ	1	0	1	0	0	0	0	0	%	1	0	1	0	0	1	0	1
ACK	0	1	1	0	0	0	0	0	&	0	1	1	0	0	1	0	1
BEL	1	1	1	0	0	0	0	1	'	1	1	1	0	0	1	0	0
BS	0	0	0	1	0	0	0	1	(	0	0	0	1	0	1	0	0
HT	1	0	0	1	0	0	0	0	)	1	0	0	1	0	1	0	1
LF	0	1	0	1	0	0	0	0	*	0	1	0	1	0	1	0	1
VT	1	1	0	1	0	0	0	1	+	1	1	0	1	0	1	0	0
FF	0	0	1	1	0	0	0	0	,	0	0	1	1	0	1	0	1
CR	1	0	1	1	0	0	0	1	—	1	0	1	1	0	1	0	0
SO	0	1	1	1	0	0	0	1	.	0	1	1	1	0	1	0	0
SI	1	1	1	1	0	0	0	0	/	1	1	1	1	0	1	0	1
DLE	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1	0	0
DC1	1	0	0	0	1	0	0	0	1	1	0	0	0	1	1	0	1
DC2	0	1	0	0	1	0	0	0	2	0	1	0	0	1	1	0	1
DC3	1	1	0	0	1	0	0	1	3	1	1	0	0	1	1	0	0
DC4	0	0	1	0	1	0	0	0	4	0	0	1	0	1	1	0	1
NAK	1	0	1	0	1	0	0	1	5	1	0	1	0	1	1	0	0
SYN	0	1	1	0	1	0	0	1	6	0	1	1	0	1	1	0	0
ETB	1	1	1	0	1	0	0	0	7	1	1	1	0	1	1	0	1
CAN	0	0	0	1	1	0	0	0	8	0	0	0	1	1	1	0	1
EM	1	0	0	1	1	0	0	1	9	1	0	0	1	1	1	0	0
SUB	0	1	0	1	1	0	0	1	:	0	1	0	1	1	1	0	0
ESC	1	1	0	1	1	0	0	0	;	1	1	0	1	1	1	0	1
FS	0	0	1	1	1	0	0	1	<	0	0	1	1	1	1	0	0
GS	1	0	1	1	1	0	0	0	=	1	0	1	1	1	1	0	1
RS	0	1	1	1	1	0	0	0	>	0	1	1	1	1	1	0	1
US	1	1	1	1	1	0	0	1	?	1	1	1	1	1	1	0	0

as one ASCII character, and the second # to be coded as a separate character.

7.14 In the data mode, terminals 34 and 40 are connected together by test relay break contact TB-1. Thus the # selector gate output (A7-3) is connected to the inputs of gates A8-5, A8-3, A9-15, and A9-3 (Fig. 50). Terminal 19 of the format translator (CP AR287) is connected to the *character present* (CP) pulse generator (CP AR288) (Fig. 34). The CP circuit produces a pulse each time a valid character has been detected by the receiver. Assume that a character other than a # has just been received. The output of A7-3 remains 1, since a # is not being received (Fig. 50). A CP pulse (momentary 1) appears at terminal 19. Thus, all inputs to NAND gate A8-3 are simultaneously 1, and the output goes to 0. This output is connected to input lead 14 on A8-15 and input lead 14 on A10-15. These gates are cross-connected with gates A8-5 and A10-3, respectively, to form set-reset flip-flop multivibrators with terminal 14 on each as the reset lead. When terminal 14 becomes 0, both flip-flops are reset, causing A8-15 and A10-15 output leads to go to 1. Output terminals A8-5 and A10-3 therefore become 0. The ## circuit is now in its reset state.

7.15 Now assume that a # has just been received. This causes the output of A7-3 to become 0, and reset gate A8-3 is disabled. Terminals 7 and 8 of A8-5, which form the set leads of the first flip-flop, are also 0; therefore A8-5 is set. The output of A8-5 and input terminal 13 of A9-15 thus switch to 1. The A8-5 output remains 1 until reset by a 1 from A8-3. Input 13 of A9-15 is 1 but input 14 is 0, so the output of A9-15 remains 1. Thus the second flip-flop remains reset. Gate A9-3 serves as an inverter, so that its output is 1 whenever the output of A7-3 is 0, and vice versa. The 1 output of A9-3 is connected to inputs of A10-5 and A10-9. Since the second flip-flop is still reset, only A10-9 has a 1 on both input terminals; its output goes to 0 and the output of A10-5 remains a 1. The output of A10-9 is connected to terminal 35 of CP AR287; this in turn is connected to the answer-back control circuit on CP AR288 (Fig. 34). The output of A10-9, which is equivalent to the A7-3 selector gate output, is also connected to a code 1 bus in the coding matrix (Fig. 50). Use of the matrix is described in 7.22.

7.16 After about 37 ms, the output timer in CP AR245 of the basic receiver times out. Output from the # selector gate A7-3 returns to 1. Therefore, the output of inverter A9-3 returns to 0, disabling gates A10-5 and A10-9, thus ending the # indication on terminal 35 and the coding matrix. Since gate A9-15 now has 1 at both inputs, its output goes to 0. This makes terminals 1 and 2 of A10-3 go to 0, which sets the second flip-flop. This provides a memory that a # has just been received immediately after the # input at A7-3 ceases.

Translation

7.17 If the next character received is not a #, both flip-flops are reset by gate A8-3 as described in 7.14, thus erasing the # memory just described. However, assume that the next character is a #. Since both flip-flops are set, they are not affected by the # signal. The output of A10-3 is 1 and the output of inverter A9-3 goes to 1 when selector gate A7-3 goes to 0. Thus both inputs to A10-5 are 1 and its output becomes 0, providing an output on terminal 16 which represents a ##. This output is connected to the coding matrix and also via terminal 16 to the answer-back control circuit on CP AR288 (Fig. 34).

7.18 Gate A9-9 provides an OR function, while A9-5 inverts the A9-9 output (Fig. 50). When either input of A9-9 goes to 0, the output of A9-5 is also 0. Input 11 of A9-9 is connected to the output of A10-5 (# indication). Input 10 is connected via terminal 36 to a pseudo-character generator on CP AR288 (Fig. 34). Diode CR9 isolates this input from other circuits connected to terminal 36. The output of inverter A9-5 is connected to the appropriate code 1 bus of the coding matrix (Fig. 50). Thus, either a valid ## or a pseudo-character inserted into the message by logic on CP AR288 is sent to the coding matrix to be translated into an ASCII character.

Test Mode

7.19 When the data set is in the test mode, test relay contact TB-1 breaks the connection between terminals 34 and 40 and connects terminal 40 to +5 volts, which provides a permanent 1 signal (Fig. 34). Since terminal 40 is connected to the set lead of the first flip-flop, the flip-flop cannot be set and the action of the ## detector is inhibited (Fig. 50).

7.20 When a pair of signals appears at the input of the format translator, one of which is the B4 frequency on terminal 37, base current flows through resistor R1 and saturates transistor Q1. This inhibits the CP pulse on terminal 19, preventing the resulting character from being translated to an ASCII character and being sent to the customer as a false character.

7.21 When the character represented by the fourteenth button (A2, B4) is received, the CP pulse is inhibited as in 7.20. Meanwhile, the output of gate A8-9 goes to 0. This signal leaves the ASCII format translator on terminal 38 and is used to control the transfer from test mode A to test mode B.

The Coding Matrix

7.22 The characters *, #, and ## are designated C1, C2, and C3, respectively. The ASCII outputs for these characters depends on customer requirements; they are selected by installer options. Outputs from the * selector gate are connected to the C1 code 1 bus. The # and ## outputs from the ## detector also are connected as inputs to the C2 and C3 code 1 buses, respectively. Positive 5 Vdc is applied to the coding matrix to provide code 0 for the C1, C2, and C3 characters. A3-11, A3-15, and A4-11 are expander inputs to the respective coding gates. Inputs to each of the coding gates are connected to the coding matrix so that a 0 or 1 can be selected for each coding gate. By moving option straps, the installer can predetermine whether each bit in the ASCII character will be 0 or 1. Remember that bits b1 through b7 are the information carrying bits in the ASCII code; in the DS 403D/E, bit b7 is always 0; bit b8 is the even parity bit. For information on option strapping, refer to Section 594-025-201.

HIGH (B) GROUP

FREQ (HZ)	B1 1209	B2 1336	B3 1477	B4 1633
A1 697	1	2	3	(13)
A2 770	4	5	6	(14)
A3 852	7	8	9	(15)
A4 941	*	0	#	(16)

LOW (A) GROUP

TOUCH-TONE DIAL

CODING MATRIX

CODE 1 BUS
C3 (**)
CODE 1 BUS
C2 (#)
CODE 0 BUS
C1 (*)
CODE 1 BUS

+5

b1   b2   b8   b3   b4   b5   b6

* ## #

CR5 CR6 CR4 CR7 CR8 CR2 CR3 CR1

CHARACTER RECOGNITION NETWORK (SELECTOR GATES)

TOUCH-TONE SYMBOL OUTPUT

IC A5   2   5   8   0
IC A6   1   4   7   *
IC A7   3   6   9   #

FROM LOGIC DRIVERS

IC A3
IC A4
IC A2
IC A1

BIT
b1 14
b2 15
b8 23
b3 22
b4 21
b5 4
b6 3

TO PARALLEL-TO-SERIAL CONVERTER

ASCII CHARACTER GENERATING NETWORK (CODING GATES)

DETECTOR

IC A8   1ST FF
IC A9   INVR
IC A10   2ND FF

R2 +5
CR9

R1   Q1

TB
(SEE NOTE)

NOTE:
RELAY TB IS LOCATED ON THE ASCII INTERFACE UNIT, BUT OUTSIDE OF FORMAT TRANSLATOR CP.

CONTROL

9 A1
10 A2
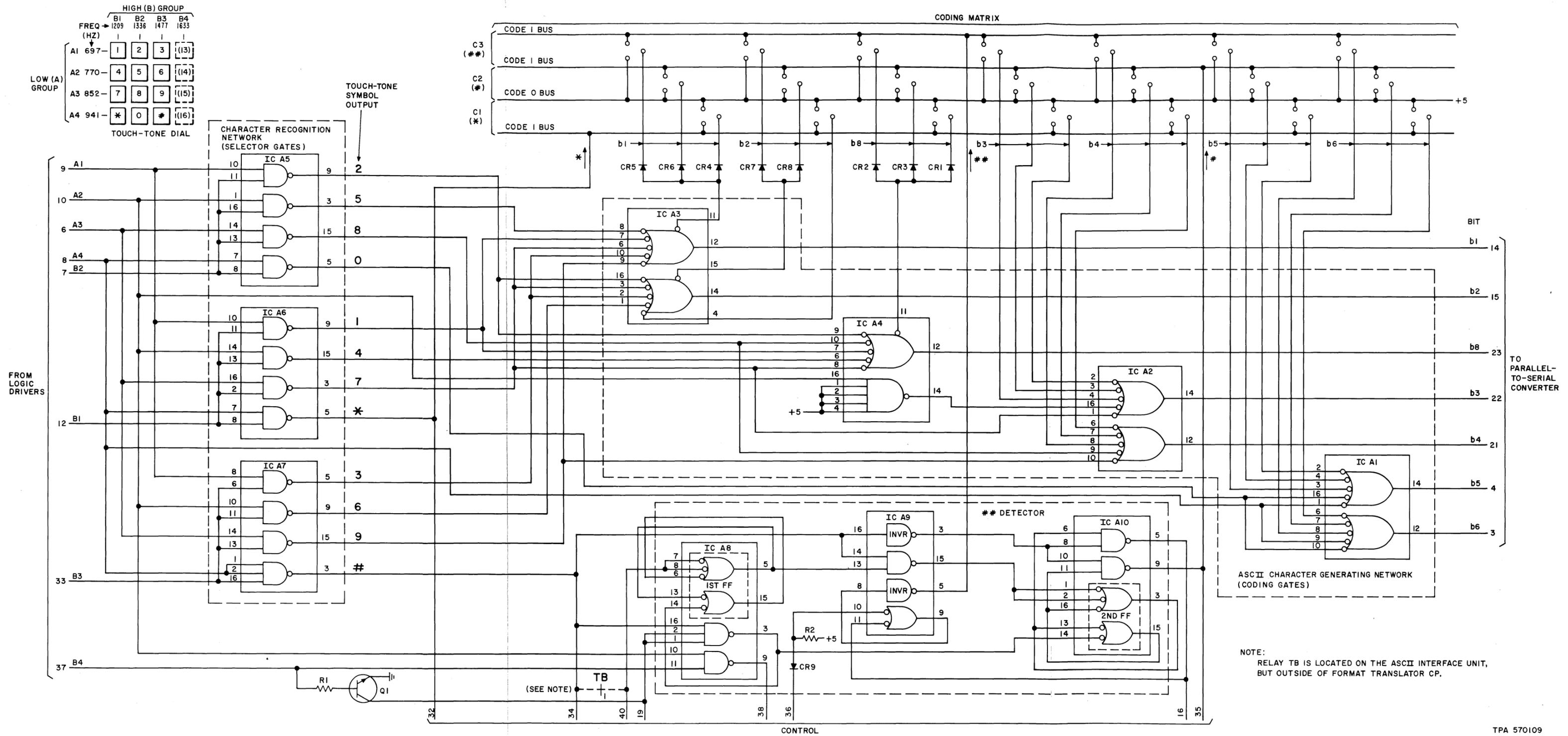6 A3
8 A4
7 B2
12 B1
33 B3
37 B4

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Fig. 50—ASCII Format Translator—Schematic Diagram

C. Parallel-to-Serial Converter (Fig. 52)

Commutator Analogy

7.23 Inputs to the *parallel-to-serial converter* (PSC) are in parallel bit form. The objective of the PSC is to serialize these bits into ASCII format. As a simple electromechanical analogy, assume eight leads connected to eight positions of a rotary switch as shown in Fig. 51. Further assume dc voltages on leads 1 through 8 as shown. With the switch set to lead 1, then rotated at a uniform rate of one step per second to the eighth lead, voltages will appear on lead 9 as shown in the illustration. Thus, we have taken eight voltages which are simultaneously present (parallel form) and converted them into sequential form (serial) by examining each lead one at a time at a uniform rate.

7.24 The PSC performs a commutator function similar to that just described (even if somewhat more complex), using ICs as storage and gating elements. In addition to the commutating of existing input signals, a start bit and two stop bits are added to the information bits at the proper times to form an 11-bit start-stop ASCII character. Provision is also made for an even parity check. As in the ASCII format translator, the individual circuits are referred to herein by the IC package number and the output lead number. For example, flip-flop (FF) A1-14 refers to IC package A1 having its output connected to terminal 14.

Memory Circuits

7.25 Individual ASCII bits b1 through b6 and b8 from the format translator (CP AR287) are connected to FFs A11-6, A11-14, A10-6, A10-14, A9-6, A9-14, and A1-6, respectively, as shown on Fig. 52. The T (toggle or trigger) lead of each of the above FFs are connected together and to the output of gate A6-14. When A6-14 goes to 0, the FFs read and store the state of each of the input leads, providing a short-term input memory.

Clock Control

7.26 As in the analogy given in 7.23, where the switch was advanced one position per second, so are the gates controlled by timing pulses from an external clock. Clock pulses enter the PSC on lead 39. Operation of the clock circuit, located on CP AR291, is controlled by circuitry on the PSC,
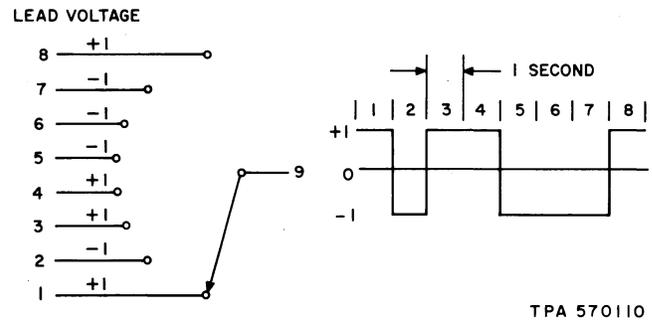

Fig. 51—Analogy of Parallel-to-Serial Converter— Schematic Diagram

and leaves the PSC on lead 32. At the beginning of each character, a CP pulse is generated on CP AR288. This pulse is fed into the PSC on lead 25, and is inverted by gate A15-9. Gates A15-5 and A15-15 are cross-connected to form a set-reset flip-flop. The output of A15-9 is connected to terminal 8 of A15-5, which is the set lead. When a CP pulse appears, the FF sets, and the output of A15-15 goes from 1 to 0. This output is connected via lead 32 to the clock in CP AR291, and is used to control the clock. When the output of A15-15 is 0, the clock runs; when the output is 1, the clock stops.

Binary Counter

7.27 IC packages A7 and A8 are connected as flip-flops (Fig. 52). ICs A7-6, A7-14, A8-14, and A8-6 are each connected as binary elements and cascaded to form a 4-bit binary divider used as a clock-pulse counter. Outputs from the four flip-flops represent binary bits with weights of 1, 2, 4, and 8, respectively. The outputs of each flip-flop change state with each 0-to-1 input change on the L lead. The binary weights, or values, just mentioned thus represent the number of clock pulses per output change-of-state. The clock pulse input to the counter is connected to the L lead of FF A7-6.

7.28 Each of the counter FFs is preset (Q = 1) by a 1-to-0 transition on its P lead from A15-5 when a CP pulse stops. (The clock is also started and stopped by this FF). Thus, when the clock stops, all counter FFs are preset; when the clock starts, all counter FFs are enabled. In the preset condition the counter is "reading" 1111 = 15 (Fig. 53). The first clock pulse causes the

counter outputs to change to 0000 = 0; the second clock pulse is represented by 0001 = 1. Thus, the number of clock pulses is equal to the decimal number +1. Three FFs provide counting to 8 (0 through 7). Since the ASCII code requires a total of 11 bits, a 4-FF counter is used, which has the capacity for counting to 16 (0 through 15).

7.29 The first counter flip-flop (A7-6) is triggered by the leading edge (0-to-1 transition) of the clock pulse. The second, third, and fourth flip-flops (A7-14, A8-14, and A8-6, respectively) are triggered by the 0-to-1 transition on their L leads, each derived from the preceding flip-flop NOT Q lead. Transitions causing the flip-flops to trigger are emphasized on Fig. 53.

Commutator Gates

7.30 Both Q and NOT Q outputs of the counter are connected to the commutator gates (Fig. 52). Gates A6-14, A5-14, A5-12, A4-14, A4-12, A3-14, A3-12, A2-14, A2-12, and A6-12 use the outputs of the counter sequentially to "open" the proper gates for the start bit, information bits b1 through b7, the parity bit, and the 2-element stop bit, respectively. Each of the gates has four of its inputs connected to four of the counter outputs in such a manner that only one gate has all four inputs from the counter at 1 for a given clock pulse. The fifth gate input receives the bit associated with each particular clock pulse.

7.31 *Start Gate:* Start gate A6-14 has its fifth input (terminal 1) connected to set-reset FF A15-5, which is the same that is used to control the clock. When a CP pulse sets this FF, input 1 of A6-14 goes to 1. When the first clock pulse occurs, the other four inputs also go to 1, and the output goes to 0. Note that the start gate receives four Q inputs (1s) from the counter when the first clock pulse occurs (Fig. 52 and 53). When the second and succeeding pulses occur, all of the NOT Q leads are no longer 1s, so the output of A6-14 returns to 1. Thus the gate output is a 0 pulse with a duration equal to the period from the beginning of clock pulse 1 to the beginning of clock pulse 2 (Fig. 53). This pulse is connected to terminal 16 of output NOT-OR gate A12-14, and provides the START pulse out of the data set.

Note: A12-12 and A12-14 outputs are tied together; the expanders are likewise tied together. The effect is that of one 9-input OR gate with a single negated output. Thus, at this point in the circuit, an ASCII 0 is represented by a 1, and vice-versa.

7.32 *Information Gates:* Each of the information bit commutator gates is then activated in turn by successive counter pulses 2 through 7, which produce four of the five 1 inputs required to operate the gate. The fifth input of each gate is connected to the NOT Q memory gate of the associated bit. For example, with the advent of the fifth clock pulse, inputs 6, 7, 8, and 9 of A4-12 are 1. If lead NOT Q of FF A10-14 (b4 memory) is 0, input 10 of A4-12 is 0; the output is thus a 1 for bit b4. Conversely, if lead NOT Q of FF A10-14 is 1, the output is a 0 for bit b4.

7.33 *b7 Gate:* Remember that with the nonalphabetic half of the ASCII code, bit b7 *must* be 0. When clock pulse 8 starts, four of the five leads are activated (1s) by the counter. Input lead 16 of A2-14 is connected to the clock control set-reset FF (A15-3) so that it is also 1. Thus the output of A2-14 is always 0, as required for b7.

7.34 *Even Parity Gate:* Clock pulse 9 activates the even parity gate (A2-12), which reads out the parity bit stored in the b8 memory FF A1-6.

7.35 *Stop Gate:* Clock pulse 10 activates commutator stop gate A6-12, causing its output to go to 0. The output of this gate is not connected as a data output; instead, it is fed to input 14 of A15-15, which is the reset lead of the clock control set-reset FF. This resets the clock control and stops the clock, causing the data set output to return to the rest, or stop state. Because the data set operates at a maximum speed of 10 characters/second, another character cannot appear until a time period equal to two clock pulses has elapsed. Thus, the stop period is equal to two bits in length, as required. The translation of one character, as just described, occurs in 1/10 second. Another character will repeat the process at any time *after* the end of the 2-bit long stop pulse.

Summary of PSC

7.36 Summarizing the parallel-to-serial conversion just described:

● The 7-bit incoming parallel character is stored in 7 memory flip-flops.

● A character present (CP) pulse sets clock control, which starts clock.

● Pulse counter counts first pulse and first commutator gate is activated.

● Output gate transmits start pulse.

● All bit storage FFs "read in" their bits.

● Clock pulses 2 through 7 are counted and appropriate commutator gates operate.

● Each commutator gate passes one ASCII bit.

● Clock pulse 8 allows b7 "always zero" bit to pass through gate.

● Clock pulse 9 allows even parity bit to pass through gate.

● Clock pulse 10 is counted, causing stop pulse to appear at output and reset clock control FF.

● Clock control FF stops clock, resets all memory FFs, and resets clock pulse counter. Circuit is now ready for the next character.

Remote Test Parity Check

7.37 Provision is made in the PSC for remotely checking the validity of each character by using the parity bit. When the data set is in test mode A, test relay contact TA-2 routes the data signal through a test circuit which provides logical inversion (Fig. 34) then via terminal 24 on the PSC to the L lead of IC A1-14 (Fig. 52). The logical inversion makes the signal at the L lead of A1-14 0 whenever the serial output at gate A12-14 is 1, and vice-versa.

7.38 The clock pulses that drive the clock pulse counter circuit also appear on the T lead (terminal 3) of FF A1-14. This FF is connected so that its outputs change state on the trailing edge of the clock pulse (1-to-0 transition) if the signal at L is 1; the outputs do not change state if the signal at L is 0 during the clock pulse transition. The FF is preset to the Q = 1 state by the clock control set-reset FF (A15-3) and is

then reset to the Q = 0 state by the trailing edge of the tenth clock pulse. Therefore, at the beginning of each character, IC A1-14 is always in the Q = 0 state.

7.39 For each ASCII bit which is 1 (0 at terminal 37), the L lead of A1-14 is also 1; the FF outputs change state on the trailing edge (1-to-0 transition) of the clock pulse associated with that particular bit. For 0 bits, the outputs remain unchanged. Thus, at the end of bit b6, the Q output of A1-14 is 1 if an odd number of bits b1 through b6 were 1. If an even number of bits b1 though b6 were 1, the NOT Q output of A1-14 is 1.

7.40 The parity bit is chosen so that the complete ASCII character has an even number of 1s. Therefore, an odd number of information bit 1s require a 1 parity bit; an even number of 1s require a 0 parity bit (Table H). Flip-flop A1-14 counts 1s only, while FF A1-6 stores the parity bit from the format translator. Thus, the output of FF A1-14 after bit b6 can be compared to the parity bit stored in FF A1-6 as a valid character check. Gates A13-3, A13-5, and A13-9 form an EXCLUSIVE-OR comparator gate to perform this check. Output A13-9 is 1 only if inputs A13-2 and A13-16 are 1, or if inputs A13-7 and A13-8 are 1. These inputs are wired to the outputs of FFs A1-6 and A1-14 in such a way that this criterion is met only when the parity bit stored in A1-6 has the same state as that "calculated" by the action of A1-14 as described in 7.39. Thus, after bit b6, the output from A13-9 is 1 only if a valid character has been presented at output terminal 37.

7.41 Gate pairs A14-3, A14-15, and A14-5, A14-9 each act as 3-input AND gates. Inputs 2 and 6 are connected to the output of A13-15, which is 1 only during the time interval allotted to bit b7. Inputs 1 and 7 of IC A14 are connected to the valid character check circuit, which is a 1 under the conditions described in 7.40. Input 16 is 1 only if the parity bit is 1; input 8 is 1 only if the parity bit is 0. During the interval for bit b7, if the valid character check has been satisfied, the output of A14-15 is 1 if the parity bit is 1, and the output of A14-9 is 1 if the parity bit is 0. These outputs appear on terminals 13 and 12, respectively, and are used to control remote test answer-back circuits on CP AR290. If the parity check indicates a valid character, an output will occur on terminal 12 or 13; terminal 12 for a 1

parity bit or terminal 13 for a 0 parity bit. If parity does not check, no output will occur on either terminal.

Note: The valid character check will detect only an odd number of bit errors in a given character; two, four, or six errors in a single character cannot be detected.

TABLE H

EXAMPLES OF ASCII EVEN PARITY BITS

ASCII CHARACTER	INFORMATION BITS						ZERO BIT b7	PARITY BIT b8	NUMBER OF INFO 1s	TOTAL NUMBER OF 1s
	b1	b2	b3	b4	b5	b6				
NUL	0	0	0	0	0	0	0	0	0	0
SP	0	0	0	0	0	1	0	1	1	2
0	0	0	0	0	1	1	0	0	2	2
8	0	0	0	1	1	1	0	1	3	4
<	0	0	1	1	1	1	0	0	4	4
>	0	1	1	1	1	1	0	1	5	6
?	1	1	1	1	1	1	0	0	6	6

Fig. 52—Parallel-to-Serial Converter—Schematic Diagram

Fig. 53—Binary Counter Operation

D. Output Circuits (CP AR291)

7.42 CP AR291 contains the following functionally unrelated circuits:

- Gated Clock

- Voltage Regulator

- EIA Drivers (2)

- Remote Test Logic

- Permanent and Test EIA Signals

These circuits and discussed individually in 7.43 through 7.51.

Gated Clock (Fig. 54)

7.43 The gated clock is a transistorized free-running multivibrator, which provides the timing pulses for the parallel-to-serial converter described in 7.23 through 7.36. The clock is controlled by an input on lead 15 from the PSC (Fig. 34 and 54). The clock pulse output consists of 100-μs pulses spaced 9.09 ms apart, as required for 10 character-per-second operation. The multivibrator consists of transistors Q5 and Q7. Duration (pulse width) of the 100-μs pulse is determined by R19 and C4; the interval between pulses (repetition rate) is determined by C3 and R14, R15, and R16. Resistor R15 is factory-selected to overcome component tolerances, thus providing a rough approximation of the proper repetition rate. Final and precise adjustment is provided by R14, which is adjusted to 9.09 $\pm$0.01 ms. Transistor Q6 and diode CR7 provide a low impedance charging path for C3, which is charged from the +12V regulated supply during the 100-μs output pulse time.

7.44 The multivibrator output is taken from the collector of transistor Q5 and applied to transistors Q8 and Q9 through resistors R21 and R22, respectively. During the 9-ms interpulse period, transistor Q8 is saturated and Q9 is cut off; the output voltage at terminal 12 is near zero. During the 100-μs pulse output period, Q9 is saturated and Q8 is cut off, producing an output pulse of about 5 volts. Transistors Q8 and Q9 also improve the output pulse wave-shape, thus ensuring reliable operation of the flip-flops (FFs) in the PSC.
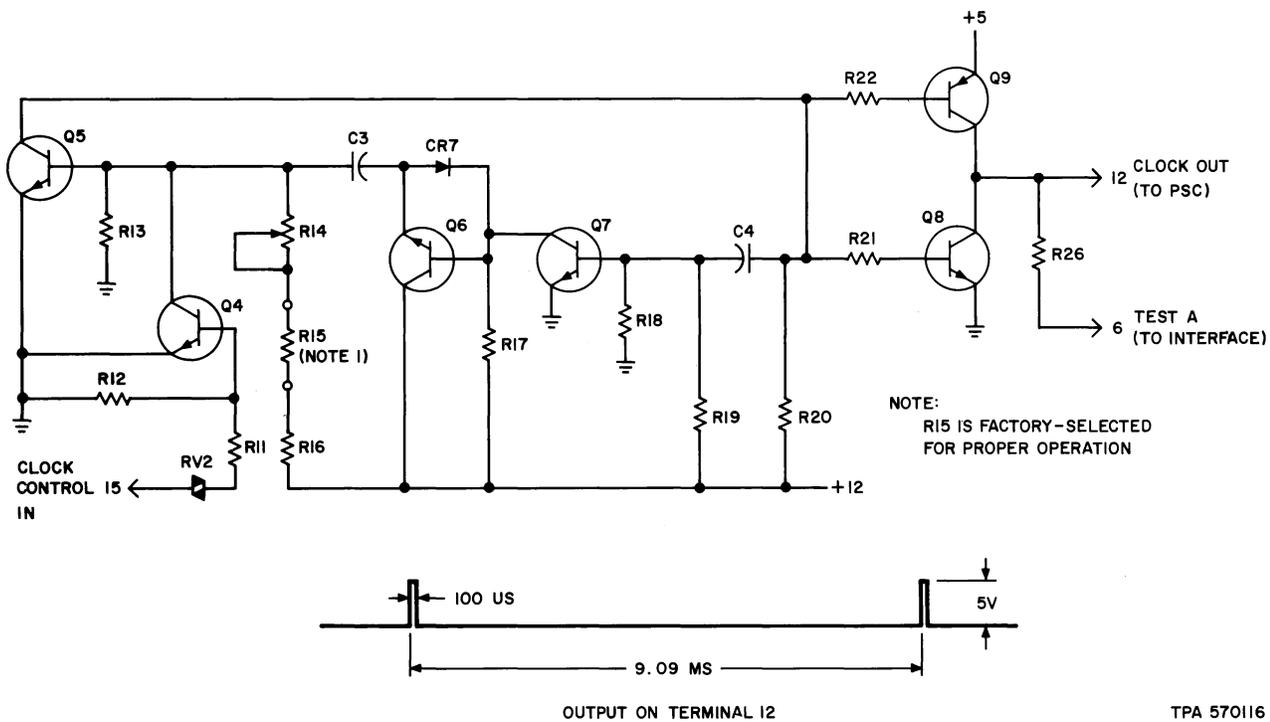

Fig. 54—Gated Clock—Simplified Schematic

7.45 Oscillation of the clock circuit is started and stopped by a control voltage input on terminal 15, which originates in the PSC. Varistor RV2 and voltage divider R11-R12 provide an operating voltage threshold for gating transistor Q4. When the input voltage at terminal 15 is greater than 2.9 volts, Q4 saturates, providing a virtual short from the base of transistor Q5 to ground, thus stopping oscillations. When the voltage at terminal 15 is less than 2.9 volts, Q4 is cut off, and oscillations start. Since terminal 15 is connected to the output of the clock control FF on the PSC (Fig. 52), the first clock pulse occurs immediately after a 1-to-0 transition at the clock control input. The output of the gated clock which is applied to the PSC appears on terminal 12 of CP AR291. In addition, another gated clock output is provided through resistor R26 and terminal 6 to interface cord pin 9 (identified as TEST A), for test purposes only.

Voltage Regulator (Fig. 55)

7.46 Regulated and filtered 12 Vdc is derived from the +18 Vdc supply by the voltage regulator (Fig. 55). The regulator consists of dropping resistor R10, zener diode CR5, and capacitor C2. Output from the regulator is used to supply 12-volt power to the gated clock, and also to supply power to several circuits on CP AR288.

EIA Drivers (Fig. 56)

7.47 The ASCII output signal from the PSC is applied to terminal 8 of the RD driver, where the signal is shifted from IC voltage levels to EIA-standard voltage levels. An operating voltage threshold for transistor Q2 is established by voltage divider R4-R5 and varistor RV1. When the input voltage is greater than 2.3 volts, transistor Q2 saturates, supplying base current bias through R6-R7 for transistor Q3. This causes Q3 to saturate, supplying current through resistor R8 to the customer load, and developing a positive load voltage. When the input voltage is less than the 2.3-volt threshold, both transistors are cut off. Current is then drawn from the −18 volt supply through resistor R9 and diode CR4, producing a negative voltage at the customer load. The negative load voltage provides the "marking" condition; the positive load voltage provides the "spacing" condition for the customer.

7.48 The ASCII data set ready (DSR) indication is determined by the C relay (K1) in the

LCC of the basic receiver (Fig. 30 or 31). The C relay delivers either a +18 volt or a −18 volt signal to terminal 10 of the DSR driver. Resistor R3 (Fig. 56) limits the current and drops the output to the EIA 5-volt level. Capacitor C1 is provided to smooth out possible C relay contact chatter.

Note: The ASCII DSR indication is determined by operation of the C relay, whereas the CC and BCM interface units use the H relay to provide the DSR indication (Fig. 18). Therefore, the ASCII DSR indication is provided some 2.5 seconds *earlier* than the DSR indication in the other two interface units. This timing difference is provided to allow motor start-up time in the customer's ASCII receiver.
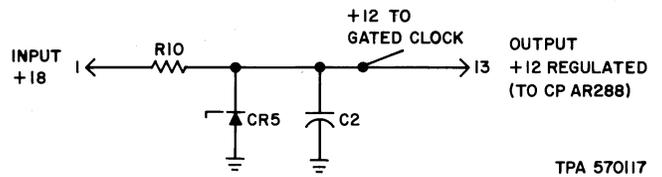

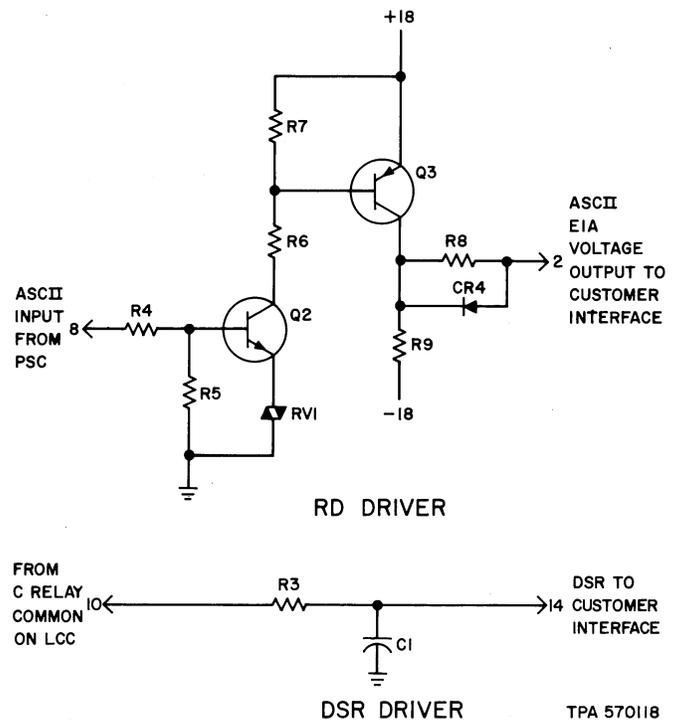**Fig. 55—Voltage Regulator on CP AR291—Simplified Schematic**

Fig. 56—EIA Voltage Drivers—Simplified Schematic

Remote Test Logic on CP AR291 (Fig. 57)

7.49 In test mode, relay TB is operated and relay TA is released. Relay contact TA-2 transfers the ASCII EIA serial output signal away from the customer and to terminal 4 of CP AR291 (Fig. 34). If the EIA output driver is capable of developing +5 volts across R1 in the spacing condition, zener diode CR3 will conduct, causing Q1 to saturate (Fig. 57). The output at terminal 3 will be clamped at about 0 volt. If the EIA output driver is in the marking condition, or is unable to produce +5 volts in the spacing condition, Q1 will remain cut off, and the voltage at terminal 3 will be about +5 volts. If the EIA output driver is operating normally, the output at terminal 3 will be a logically inverted version of the ASCII output signal, shifted to IC logic levels. The output is connected to terminal 24 of CP AR289, and is used to drive the remote test parity check described in 7.37 through 7.41.

7.50 Meanwhile, relay contact TA-3 connects the DSR EIA driver to terminal 9 of the remote test logic circuit on CP AR291 (Fig. 34 and 57). If the DSR circuit is operating properly, the DSR output voltage (terminal 14) will be positive and Q1 will operate as just described in 7.49. However, if for some reason the DSR voltage is negative, Q1 will not operate and no output will be produced at terminal 3.

Permanent and Test EIA Signals (Fig. 58)

7.51 A permanent *off* signal is provided on the clear to send (CS) lead to the customer, as required for receive-only service. This signal is derived from the −18 Vdc power supply through resistor R25 and to the customer via lead 5 of the interface cord (Fig. 58).

7.52 In the test mode, break contact TA-9 provides a negative EIA voltage derived from the −18
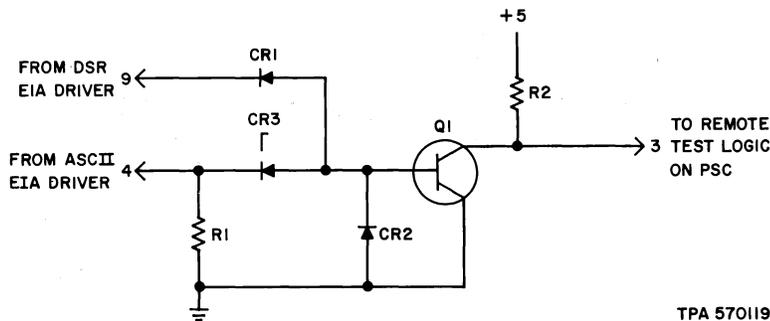
Fig. 57—Remote Test Logic on CP AR291—Simplified Schematic

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Fig. 58—Permanent and Test EIA Signals—Simplified Schematic

Vdc power supply through resistor R23. This signal is delivered to the customer via lead 3 of the interface cord to produce a marking indication on the received data (RD) lead (Fig. 58).

7.53 In the test mode, break contact TA-8 provides a negative EIA voltage derived from the −18 Vdc power supply through resistor R24. This signal is delivered to the customer via lead 6 of the interface cord to produce an *off* indication on the data set ready (DSR) lead (Fig. 58).

E. Control Circuits (CP AR288)

7.54 Circuit pack AR288 contains the following functionally related circuits:
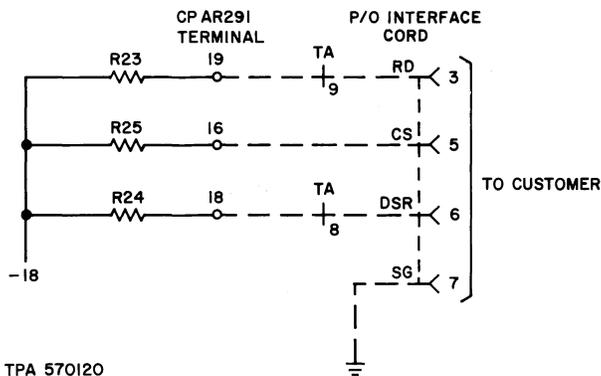
● Answer-Back and Hang-Up Control

- Time-Out Circuit

- Pseudo-Character Generator

- Pseudo-Character Timer

- Character Present Driver

- Data Terminal Ready (DTR) Logic

These circuits are discussed individually in 7.55 through 7.71. The logic circuits are identified in the same manner as described in 7.06.

Answer-Back and Hang-Up Control (Fig. 59)

7.55 Whenever a *, #, or ## is detected by the format translator (CP AR287), a 37-ms 1-to-0-to-1 pulse appears on one of the terminals 22, 21, or 4 of the control circuit (Fig. 59). Assume that the special character enabling options, XF, XH, and XK are installed (options XG, XJ, and XL disable the special character functions). Gate A1-3 acts as a NOT-OR gate. When any one of its 3 inputs goes to 0, its output goes to 1; this 1 signal is connected to input 14 of gate A1-15.

7.56 When no character is being received, the data carrier detector (DCD) relay in the basic receiver is released; terminal 24 of CP AR288 is connected to −18 volts through the DCD break contact (Fig. 59). Current flows through resistor R1, diode CR2, and resistor R6. The voltage at the anode of CR2 is prevented from going negative by diodes CR1 and CR3. This causes input 11 of A1-9 and input 13 of A1-15 to become 0 between characters.

7.57 When a character is being received, the DCD relay is operated, thus removing the −18 volts from terminal 24. The +5 volts through resistor R6 now causes the two gate inputs (A1-11 and A1-13) to go to 1. Gate A1-15 now has a 1 on both of its inputs, and its output goes to 0. This causes input 1 of the first FF (A2-3) to go to 0, which sets the first FF. This in turn causes a 1 to appear on input 13 of A2-15. However, input 14 of A2-15 is held at 0 by inverter A1-9 as long as the DCD relay is operated. This provides a 1 output from A2-15, which is inverted by A2-9 providing a 0 preset on leads 13 and 5 of A4-14 and A4-6, respectively. When the incoming character ceases, the DCD relay releases, and the output of A1-9 again goes to 1. This now provides 1s at

both inputs of A2-15, and its output goes to 0. In effect, this circuit has stored the incoming *, #, or ## in the first FF until the incoming signal stops, then the signal is transferred to the output of A2-15.

7.58 When the output of A2-15 goes to 0 the output of inverter gate A2-9 goes to 1, removing the preset signal from leads 13 and 5 of counter flip-flops A4-14 and A4-6, respectively. Also, a 0 at the output of A2-15 makes the base of Q4 less than the threshold established by resistors R11 and R43. Base current for transistor Q4 cannot flow through R11 when the voltage is below the threshold, so Q4 cuts off. This stops current from flowing through R13, and capacitor C4 starts to charge. When the voltage on Q4 rises to about 12 volts, diode CR4 conducts heavily through resistors R14 and R15, and the base of transistor Q5, turning on Q5. When Q5 turns on, Q6 is turned off because Q5 shunts away the Q6 base current normally supplied by R16. In about 700 μs C4 has discharged to about 2 volts, and diode CR4 stops conducting; C4 then starts charging again. The circuit thus produces short (0.7 ms) pulses at the collector of Q6. Resistors R12 and R13 set the initial voltage on C4 so that the first pulse occurs 100 ms after the output of A2-15 goes to 0. Subsequent pulses occur at 200-ms intervals. These pulses are connected to lead 16 of counter FF A4-14. The initial charge on capacitor C4 is somewhat higher when Q4 first cuts off than on subsequent cutoffs, therefore the 100-ms delay for the first pulse and 200-ms delay for subsequent pulses. Also, diode CR4 is a 4-layer PNPN device that conducts heavily (similar to a thyratron) when the conduction threshold is reached, causing the short duration pulses.

7.59 Flip-flops A4-14 and A4-6 are connected as a 4-bit binary counter which counts the pulses arriving from transistor Q6. Initially, both flip-flops have their Q outputs at 1. The first pulse from Q6 causes both FFs to change state. Thus, both NOT Q outputs become 1, and both inputs to A3-9 are 1. The output of A3-9 goes to 0, which deactivates the DR relay driver in CP AR290, and causes answer-back tone to be sent out over the data line to the sending station. Varistor RV3 provides a threshold voltage for the DR relay driver.

7.60 The second pulse from Q6 causes A4-14 to change state. Thus, Q of A4-14 becomes 1 and NOT Q of A4-6 is still 1. This makes inputs 6 and 7 of A1-5 both 1. Input 8 of A1-5 is also 1, because the second FF is in the reset state. Therefore the output of A1-5 goes to 0, which causes the input of the first FF (A2-5) to become 0, thus resetting the first FF. This causes the output of A2-15 to go to 1, turning on transistor Q4. Capacitor C4 now returns to its initial voltage, and the pulses from Q6 stop. The output of A2-9 goes to 0, causing the counter (A4-14 and A4-6) to be preset to the Q = 1 state. Meanwhile, the output of A3-9 returns to 1, causing the data set to stop sending answer-back tone.

7.61 In summary, the control circuit functions just described, in response to a *, #, or ## are as follows:

● The circuit waits until the end of the incoming character.

● A 100-ms delay ensues after the end of the incoming character.

● The control circuits cause the data set to send a 200-ms answer-back tone.

● The circuit resets and awaits the next character.

If a ## has been received, the control circuits function as just described to send an answer-back tone. In addition, the call is terminated, as described in the following paragraphs.

7.62 The 1-to-0-to-1 pulse appearing on terminal 4 when the ## is received is wired to input 7 of the second FF (A3-5). This input acts as a set lead for the second FF. The output of A3-3 goes to 0, so that the output of A1-5 will not go to 0 after the second pulse from the pulse generator; therefore, the first and second FFs do not reset. However, the output of A3-15 does go to 0 after the second pulse generator pulse, turning on transistor Q7. The emitter voltage on Q7 drops, causing Q8 and Q9 to turn off, thus causing termination of the call. When the call is terminated, relay TB operates, connecting −18 volts through make contact TB-2 to terminal 3. Current drawn through diode CR5, resistors R18 and R10, and diode CR6 drop the voltage on terminal 16 of A3-3 to about −0.65 volt, causing both FFs to reset.

The circuit is thus returned to the quiescent state after sending an answer-back tone and causing the call to be terminated. Actually, the output of gate A3-15 goes to 0 after the second pulse (from the pulse generator) for either *, # or ##. However, gate A1-5 resets the circuit for * or # before transistors Q7, Q8, and Q9 can switch, so the connection is not terminated unless gate A1-5 is disabled by a 0 input on terminal 8.

DTR Logic (Fig. 59)

7.63 Transistors Q8 and Q9 drive the C and OS relays in the basic receiver, which control the data terminal ready and out-of-service functions, respectively. The DTR interface lead is connected to terminal 10 through test relay TA-7 (Fig. 59). When DTR is off, the voltage at terminal 10 is more negative than −3 volts. The cathode of diode CR7 is about −0.65 volt, and transistors Q8 and Q9 are turned off. When DTR is on, the voltage at terminal 10 is more positive than +3 volts. Since the threshold established by RV2 is less than +3 volts, base current flows to Q8 and Q9 through resistor R19. The transistors turn on, providing a current path for the C (DTR) relay via terminal 15, and for the OS (OOS) relay through terminal 35. Thus, this circuit provides control of the line control and out-of-service functions in the basic receiver. The OOS function must be disabled by strapping option ZC on CP AR461 when not used since the OS relay is controlled by this circuit. Transistor Q7 provides an internal override of the DTR signal as explained in 7.62.

Character Present Driver (Fig. 59)

7.64 When a data character is not being received, the DCD relay break contact applies −18 volts on terminal 24 (Fig. 59). Current flows through resistor R1, diode CR1, and diode CR3, holding the base 2 of transistor Q2 at about −0.65 volt. Base 4 of Q2 is held near 0 volt, so both halves of Q2 are cut off. The voltage divider formed by resistors R3 and R7 places an initial voltage of 6 volts on capacitor C1. Resistor R4 supplies base current for Q1, holding it saturated. The output voltage at terminal 19 is at the logical 0 level. When a data character is received, the DCD relay operates, removing the negative voltage at base 2 of Q2. Resistor R2 now supplies base 2 current, and the collector of Q2 goes to nearly zero. The voltage across C1 cannot change instantaneously, so the base of Q1 goes to about

−6 volts and Q1 turns off. Capacitor C1 charges through resistor R4 for about 2 ms, until the base of transistor Q1 becomes slightly positive and Q1 turns on again. This results in a 2-ms character present pulse (a 1 pulse) occuring at terminal 19 each time a data character is received. A CP pulse can also be initiated by transistor Q17, as described in 7.66.

7.65 In the test mode, the TA relay is released, and TA-7 transfers DTR away from the customer and to +12 Vdc. This applies an ON indication to the DTR logic to enable the test mode.

Pseudo-Character Generator and Timer (Fig. 59)

7.66 Transistors Q16 and Q17 and their associated components form a monostable multivibrator which serves as a pseudo-character timer. In the rest state, Q16 is off and Q17 is on. Transistor Q17 holds transistor Q3 off, and also holds base 4 of Q2 off. A signal from either the time-out circuit or the initial character generator circuit causes Q15 to saturate, turning on Q16. This causes Q17 to turn off for about 35 ms until capacitor C8 charges through resistor R36 to a voltage sufficient to turn Q17 on again.

7.67 When Q17 turns off, Q3 and Q2 turn on. Q3 saturates, putting a pseudo-character indication through relay break contact TB-4 to the coding matrix in CP AR287 and to the A4 driver in CP AR286 (Fig. 34 and 59). This signal causes the ASCII character selected by installer option to be presented to the parallel-to-serial converter. In test mode, relay make contact TB-4 switches the signal to the 30-second timer in CP AR290, which initiates the remote test sequence. Meanwhile, at the same time Q3 saturates, the base 4 side of Q2 also saturates, producing a CP pulse at terminal 19. This pulse causes the psuedo-ASCII character generated by the format translator (CP AR287) to be transmitted to the customer.

Initiating Pseudo-Character ## (Fig. 59)

7.68 Assume option XA is installed. (Option XB disables the initial ## insertion). In the data mode, test relay make contact TA-6 connects the +18 Vdc supplied through option XA and terminal 18 to terminal 7 (Fig. 59). When the data set is in the idle state, −18 Vdc is placed on terminal 38 via the DSR break contact (line status relay K3-2). Current flows from terminal 38

through CR10, R41, and R40 to terminal 7, producing about 0 Vdc at the junction of resistors R40, R41, and R42. This places a near zero voltage on capacitor C10. Diode CR13 prevents the voltage across C10 from going more negative than 0.65 Vdc. When the data set answers an incoming call, the LS relay operates, opening the circuit to terminal 38. Current now flows through resistor R42, charging C10 toward +18 volts. This voltage rise is differentiated by capacitor C11, causing transistor Q15 to saturate momentarily to initiate generation of the pseudo-character, as described in 7.66 and 7.67. Diode CR14 provides a recharging path for C11. In the test mode +18 Vdc is supplied to C10 via TA-6 break contact, so that this feature is enabled regardless of whether option XA is installed.

Time-Out Feature (Fig. 59)

7.69 The time-out feature is provided so that the data set will turn off after a predetermined period of inactivity. This period is selected by installer option; either 45 seconds (XC) or 15 seconds (XD) is available. The feature may also be disabled (option XE). Assume option XC is installed. When the data set is in the idle state, −18 volts is applied on terminal 38. Current flows from terminal 38 through diode CR9 and resistors R39 and R27 to the +18 volt source, holding the voltage across capacitor C7 at nearly zero. When the data set answers a call, terminal 38 is open circuited as in 7.68. Current flows through resistor R27 and capacitor C7 starts charging toward +18 volts. Each time **any** data character is received the DCD relay connects −18 volts to terminal 16, discharging capacitor C7 through resistor R39 and diode CR8, causing the time-out circuit to recycle. As long as **no** character is received, the voltage across capacitor C7 will continue to rise. After an uninterrupted absence of incoming data for 45 seconds, base current will flow in transistor Q14, turning on Q13 and then Q10. When Q10 turns on, Q11 rapidly turns off, causing a base-current surge in Q12 and Q15. Resistors R25 and R33 cause the current to divide about equally between Q12 and Q15. Resistor R34 provides a recharging path for capacitor C5. The circuit function to this point is summarized as follows:

- Time-out circuit starts timing at the beginning of each call.

- Circuit resets each time any character is received.

- After 45 seconds without an incoming character, the time-out circuit causes Q12 and Q15 to saturate momentarily.

7.70 When transistor Q12 saturates, it sets the first and second flip-flops, causing the data set to send an answer-back tone to the calling station and terminate the call as previously described. When Q15 saturates, it starts the pseudo-character sequence described in 7.66 and 7.67. Thus, when the data set "times out," it sends an ASCII character to the customer interface and sends an answer-back tone to the calling station, and then terminates the call. Option XD performs the same time-out function in 15 seconds, while option XE disables the time-out feature.

7.71 In the test mode, break contact TA-1 applies —18 volts to terminal 16, thus disabling the time-out feature.
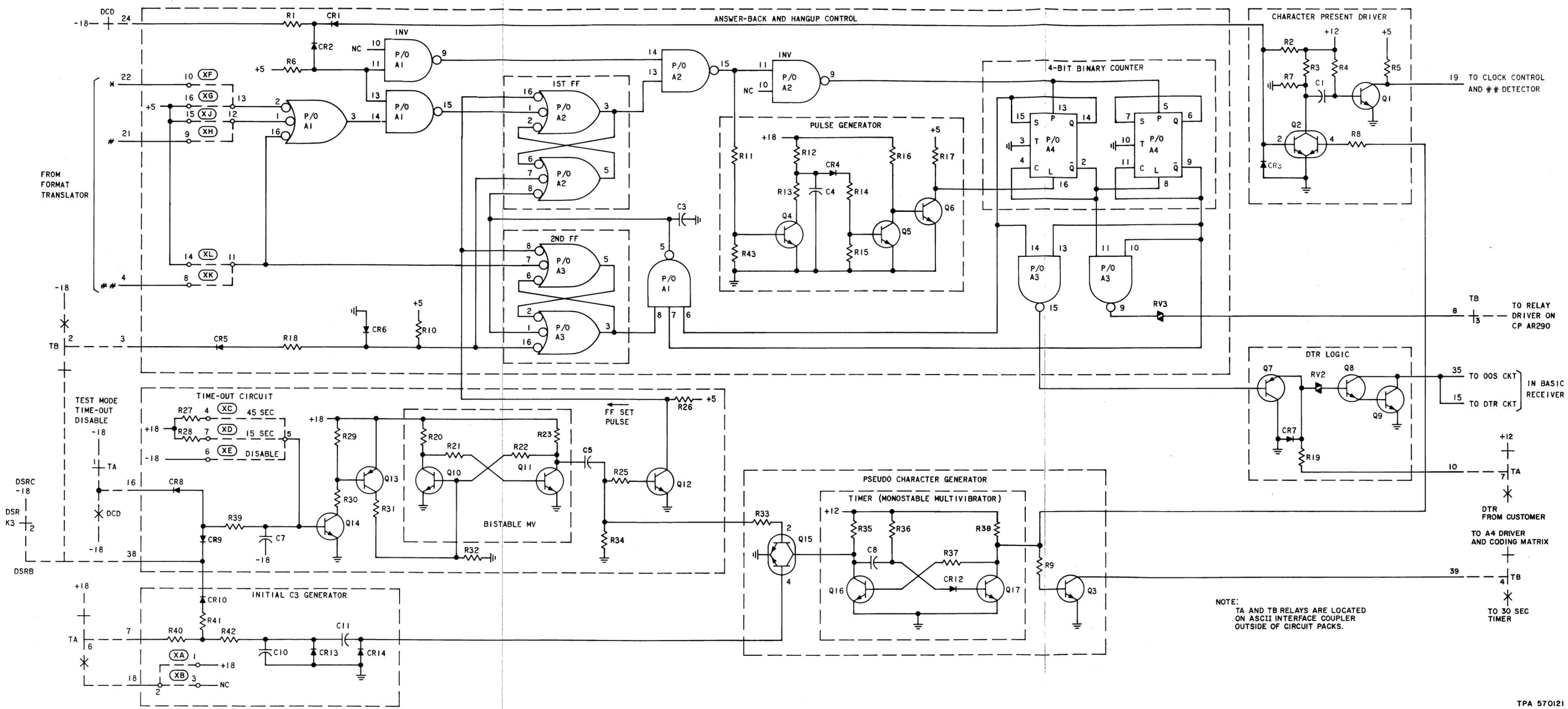
Fig. 59—ASCII Interface Coupler Control Circuits—Functional Diagram

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F. Auxiliary Circuits (CP AR290)

7.72 Circuit pack AR290 contains the following functionally related circuits:
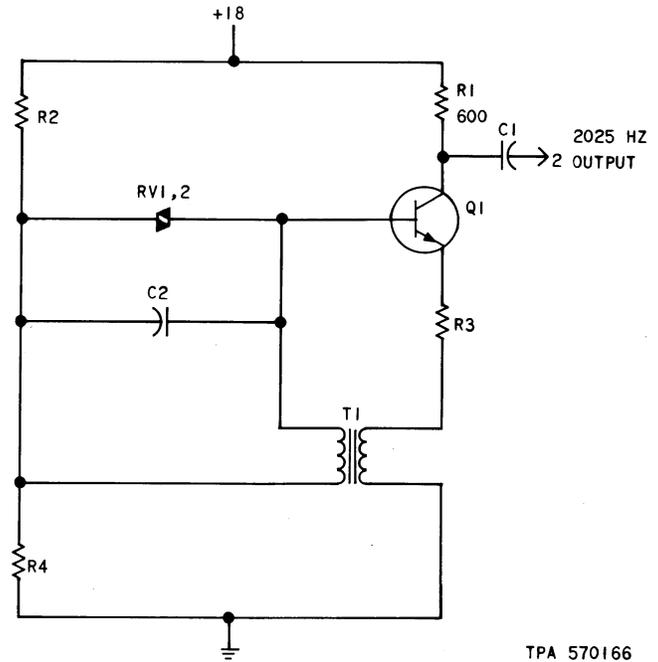
- 2025-Hz Answer-Back Oscillator

- Test Mode Logic and Test Relay Drivers

- 30-Second and 70-Millisecond Timers, OR Gate, and DR Relay Driver

These circuits and discussed individually in 7.73 through 7.85.

2025-Hz Answer-Back Oscillator (Fig. 60)

7.73 The 2025-Hz answer-back oscillator is comprised of transistor Q1 operating as a class A amplifier, with positive feedback supplied by transformer T1. The operating frequency is determined by the resonant circuit T1-C2. Varistors RV1 and RV2 limit the base voltage to ensure class A operation, thus assuring a good output waveform. Collector load resistor R1 establishes the output impedance at 600 ohms.

7.74 The 2025-Hz oscillator operates continuously. Oscillator output is switched to the data line when the DR relay on the option board (CP AR461) is released. The DR relay is controlled by transistor Q11 (Fig. 61). In the data mode, terminal 7 is connected through the break contact of TB-3 to the answer-back and hangup control circuits in CP AR288. The voltage at terminal 7 is about +3 volts, and base current flows through resistor R24. Transistor Q11 saturates, operating the data receive (DR) relay on the option board (CP AR461) in the basic receiver (Fig. 34 and 30 or 31). Resistor R23 (Fig. 61) limits relay coil current. In the answer-back mode, the voltage at terminal 7 drops to about zero. Tranasistor Q11 cuts off, releasing the DR relay; this connects the AB oscillator to the data line.

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Fig. 60—2025-Hz Answer-Back Oscillator—Functional Schematic
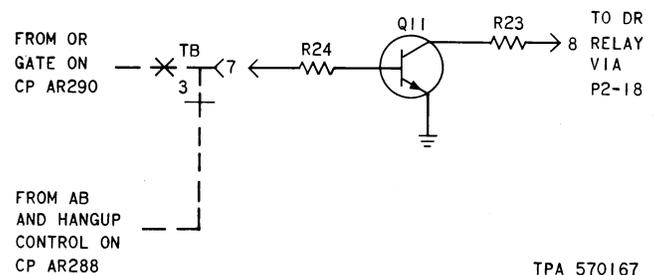
TPA 570167

Fig. 61—DR Relay Driver—Functional Schematic

Entering Test Mode (Fig. 62)

7.75 When power is first applied to the data set, transistor Q4 saturates and relay TA operates (Fig. 62). Break contact TA-12 opens the circuit to terminal 10 so that relay K1 cannot operate. Break contact TA-11 opens the circuit to terminal 12 so that transistor Q2 is inoperative. The data set is now in the normal (data) mode.

7.76 To place the data set in the test mode, the attendant momentarily pushes the TEST key on the associated DAS 804G or the T1 (T2, etc) key on the DAS 804K. This places a temporary ground on terminal 14 of CP AR290 (Fig. 62), completing the circuit through diode CR2 and the coil of test relay TB, causing the TB relay to operate. Current also flows through diode CR3, raising the voltage at the base of transistor Q4 above the threshold set by varistors RV5 and RV6. This causes transistor Q4 to cut off, releasing relay TA. Break contact TA-11 places ground on terminal 12; make contact TB-11 places −18 Vdc on terminal 11. This biases transistor Q2 on, thus keeping relay TB operated. Make contact TB-12 and break contact TB-10 place ground on terminal 18. This keeps transistor Q4 cut off and relay TA released. Break contact TA-12 places −18 Vdc on terminal 10, enabling relay K1. However, relay K1 remains released because transistor Q5 is held cut off by the voltage at terminal 19. The data set is now in test mode A.

7.77 With the data set in test mode, all customer interface leads are transferred away from the customer. Relay break contact TA-9 places a steady marking indication on the receive data (RD) lead, while break contact TA-8 places an off indication on the data set ready (DSR) lead (Fig. 34).

Transfer To Test Mode B (Fig. 62)

7.78 After the data test center has completed tests specified for test mode A, the A2-B4 combination of frequencies is transmitted by the DTC. This causes the voltage at terminal 19 to shift momentarily from about 4 Vdc to about 1 Vdc (Fig. 62). The voltage divider formed by resistors R10 and R11 causes the base voltage of transistor Q5 to drop below the threshold set by

varistor RV7, thus turning Q5 on. Current now flows to operate relay K1. The K1-2, 5 make contact closes, providing a ground path through diode CR5 to keep relay K1 operated. Resistor R12 limits relay coil current. If relay TA had been operated, contact TA-12 would have prevented relay K1 from operating.

7.79 Closed relay contact K1-2, 5 also supplies current through diode CR1 to transistor Q2, raising the base voltage of Q2 above the threshold set by varistors RV3 and RV4. This causes Q2 to cut off, releasing the TB relay. When relay TB releases, the base connection of Q4 to ground via terminal 18 is opened by relay contact TB-12. However, current through relay contact K1-2, 5 and CR4 keeps transistor Q4 cut off and relay TA released. With both test relays released, the data set is now in test mode B.

Returning to Data Mode (Fig. 62)

7.80 When the DTC tests are completed and the terminate test mode signal is sent (or for any other reason) the C relay in the LCC of the basic receiver is released. This places ground on terminal 15 (Fig. 62), causing capacitor C3 to go from +18 volts to zero. Current flows momentarily through C3, R8, R27, and the base of transistor Q3, causing Q3 to saturate for a time sufficiently long for relay TA to operate. Relay contact TA-12 opens the circuit to relay K1, and K1 releases. This opens the K1-2, 5 contact, causing transistor Q4 to turn on and keep relay TA operated. Contact TA-11 opens, keeping relay TB released. If relay K1 had not been operated (test mode A), relay TB would nevertheless be released when contact TA-11 opened. Thus the data set is returned to data mode from either test mode A or B.

7.81 The test mode can be released at the data station by lifting the handset and momentarily depressing the DATA key on DAS 804G or the TSTR (test release) key on DAS 804K (Fig. 30 and 31, respectively). In either case, this places a momentary ground on terminal 16, causing the TA relay to operate (Fig. 62). When relay TA operates, either relay TA or K1 must release as described in 7.80, thus returning the data set to data mode.
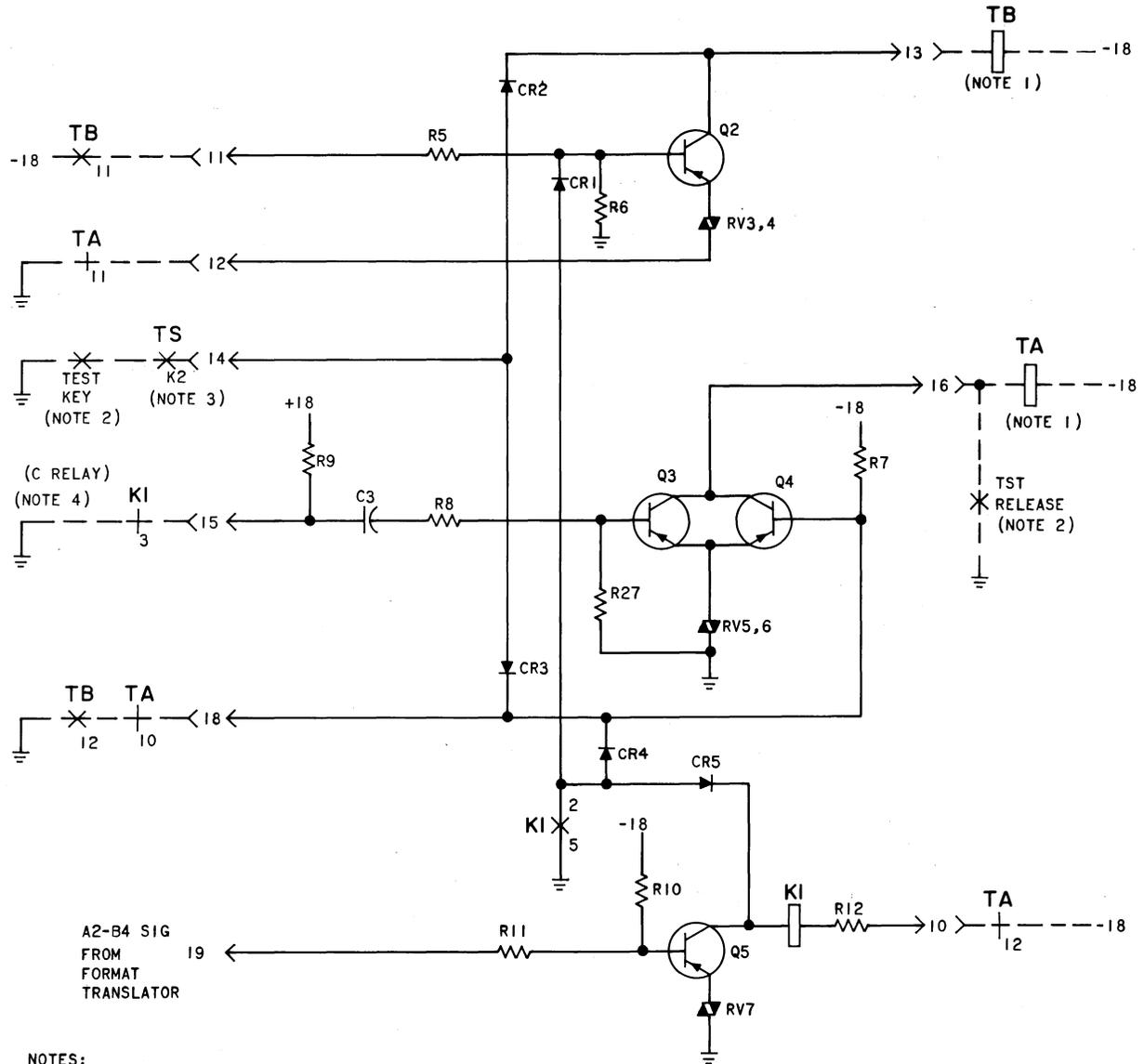
NOTES:
1. TA AND TB RELAYS ARE LOCATED ON ASCII INTERFACE
   UNIT OUTSIDE OF CIRCUIT PACKS.
2. TEST AND TEST RELEASE KEYS ARE LOCATED
   ON DAS 804-TYPE.
3. TS RELAY IS LOCATED ON OPTION BOARD (CP AR461).
4. C RELAY (KI) IS LOCATED ON LINE CONTROL
   CIRCUIT (CP AR422).

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Fig. 62—Test Mode Logic and Test Relay Drivers—Functional Schematic

30-Second Answer-Back Timer (Fig. 63)

7.82   Transistors Q6 and Q7 form a 30-second timer for timing the on-time of the answer-back oscillator. In test mode A, test relay contact TB-4 connects terminal 4 to the pseudo-character generator on CP AR288. At the beginning of a test call momentary ground appears at terminal 4. This causes transistor Q7 to turn off and transistor Q6 to turn on. The circuit remains in this state for about 30 seconds until capacitors C4 and C5 recharge through resistor R14. At the end of the charging period the transistors reverse their respective states.

7.83   When transistor Q6 turns off, current flows through resistor R13, diode CR7, resistors R18 and R19, and to the base of transistor Q8, causing Q8 to saturate. In the test mode, terminal 9 is connected to the DR relay driver via test relay make contact TB-3 (Fig. 61). Thus, when Q8 saturates, the relay driver (transistor Q11) cuts off. This causes the answer-back oscillator (Fig. 60) to send a 2025-Hz tone out over the data line until transistor Q6 turns on again.

7.84   Terminals 3 and 6 of CP AR290 are connected to the remote test logic circuits on CP AR290 (Fig. 34, 52, and 63). When a valid character is received in test mode A, a positive 9-ms pulse will appear on either terminal 3 or 6 from the parallel-to-serial converter. If the received character had a space parity bit, the pulse appears on terminal 3. Current flows through diode CR10, resistor R19, and to the base of transistor Q8, causing Q8 to saturate. This in turn causes a 9-ms answer-back tone to be transmitted. If the received character had a mark parity bit, the pulse appears on terminal 6, actuating the 70-ms timer. Transistor Q10 turns on and transistor Q9 turns off. With Q9 off, current flows through diode CR9 and resistors R18 and R19, causing Q8 to turn on. This causes answer tone to be transmitted. Transistors Q9 and Q10 act as a pulse-stretcher, causing the answer-back tone to remain on the line for about 70 ms until capacitor C7 charges and transistor Q9 turns on again. Thus the DTC receives a series of 9-ms tone bursts to indicate a valid character with a space parity bit, and a series of 70-ms tone bursts to indicate a valid character with a mark parity bit.

7.85   In test mode A, the DTC can test the detector bandwidth, and to some extent the receiver sensitivity, by sweeping the A- and B-group oscillators and listening to the timing of the tone bursts which are returned by the data set. The DTC operator then transmits the A2-B4 combination of tones, which switches the data set to test mode B. The DTC operator then checks the data set answer-tone response to the characters *, #, and ##. The test mode is terminated by the ## signal.

30-SEC TIMER

+18

TO CODING
MATRIX

FROM
PSEUDO-
CHARACTER
GENERATOR ON
CP AR288

TB
(SEE NOTE)

R15 R14   R13

C4,5   R16

Q7   Q6

OR GATE

+18

R17

CR7

Q8

TO DR RELAY DRIVER
ON CP AR290 VIA
TB-3 BREAK CONTACT

FROM RT
LOGIC ON
CP AR289

3

CR10

R18   R19

CR9

70-MS TIMER

+18

R22 R21   R20

C7   R26

Q10   Q9

NOTE:
    TB RELAY IS LOCATED ON ASCII
    INTERFACE UNIT OUTSIDE OF
    CIRCUIT PACKS.

FROM RT
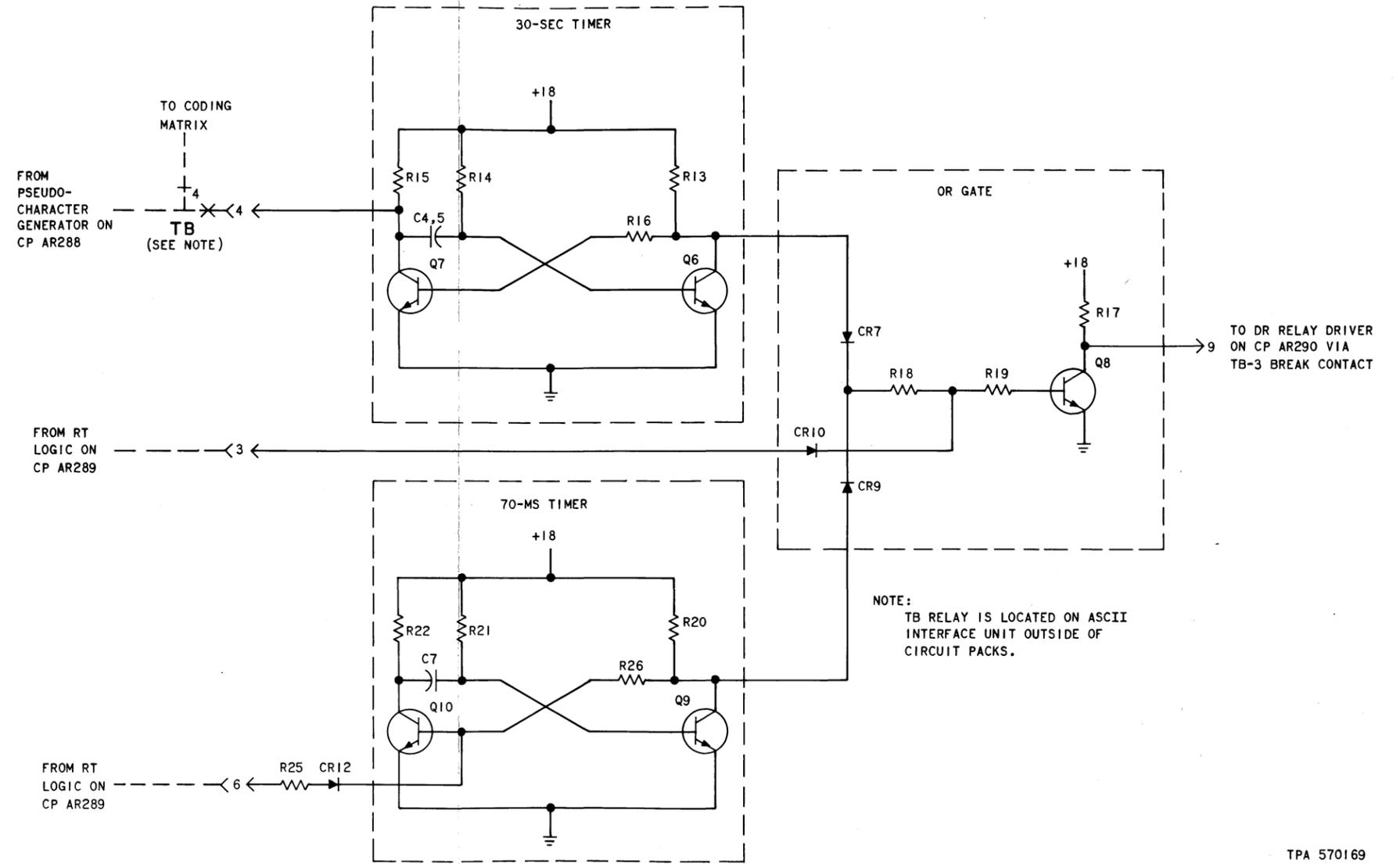LOGIC ON
CP AR289

6   R25 CR12

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Fig. 63—Timers and "OR" Gate—Functional Schematic

G. 166A1 Regulator (Fig. 64)

7.86 Integrated circuits (ICs) require a voltage source on the order of 5 volts for proper operation. Also, overvoltage protection must be provided in the IC power supply to prevent destruction of the ICs in case the supply voltage should exceed 7 volts. The 166A1 regulator provides a well regulated 4.9-volt output, with a "crowbar" overvoltage protection circuit, and a fused input to prevent damage to the power supply in the event of a short circuit.

7.87 The regulator receives its input from the +18 volt regulated supply that supplies the data set. The voltage is applied across resistor R1 and zener diode CR1 to produce a +12 reference voltage for transistor Q1 (Fig. 64). Capacitor C2 provides additional filtering for the reference voltage. Transistors Q1 and Q2 act as a schmitt trigger, except that they do not go into saturation. A low feedback voltage on the base of transistor Q1 tends to turn Q1 off, thus making the collector voltage high. This allows most of the current to flow through resistors R2 and R6, into the base of Q2, and also through resistors R7 and R8 to ground. Capacitor C3 couples the on-off transitions of the transistor Q1 collector to the base of Q2.

7.88 When transistor Q2 turns on, current flows through resistor R9, Q2, and resistor R5. Current also flows through resistors R10 and R11. Capacitor C4 couples transitions from the collector of Q2 to the base of Q3, turning Q3 off. Current also flows through diode CR2, resistor R12, and diodes CR3 and CR4 to the base of transistors Q4 and Q5. Transistors Q4 and Q5 turn on, driving transistor Q6 into saturation.

7.89 The voltage on the emitter of Q6 rises abruptly to essentially the supply voltage, less the drop across resistor R17. This abrupt rise in potential is fed back to transistor Q3 through capacitor C5, raising the voltage at the CR2-R12 junction to about twice the 18-volt supply voltage. Resistor R17 and capacitor C7 filter out current pulses from the 18-volt source.

7.90 The sudden increase in voltage appearing at the emitter of Q6 is impeded by the inductive reactance of inductor L2, so that the voltage at the regulator output cannot follow the abrupt rise at the Q6 emitter. A constant minimum load is presented to the regulator by resistor R18, while capacitor C6 filters ripple voltage from the output.

7.91 As current through L2 increases, the voltage across R18 and C6 increases. This increase in voltage is fed back via resistor R3 to the base of transistor Q1, turning Q1 on. This charge is coupled through capacitor C3 to the base of Q2, turning Q2 off. The output of Q2 is fed through the driver (Q3, Q4, Q5), turning transistor Q6 off. This on-off cycle is repeated at an ultrasonic rate (on the order of 20 kHz). Demand for more current from the supply tends to lower the output voltage. This in turn is sensed by transistor Q1, and the oscillator rate is speeded up to raise the output voltage. Conversely, less current demand will reduce the oscillator rate.

7.92 Inductor L1 and capacitor C1 filter high frequency transients to prevent them from feeding back into the +18 volt power supply. Thermistor RT1 shunted across resistor R8 compensates for reference voltage changes due to variations in temperature.

7.93 Zener diode CR5 provides a crowbar circuit for overvoltage protection of integrated circuits powered by the regulator. At the nominal operating voltage of the regulator (4.9V) the diode draws virtually no current. If a fault should cause the regulator voltage to reach about 7 volts, diode CR5 breaks down (avalanches), becoming a virtual short circuit directly across the regulator output. This in turn causes fuse F1 to "blow", thus opening the input circuit. Meanwhile, this removes power from the crowbar diode, allowing it to reset.

7.94 The 166A1 regulator is capable of delivering 4.9 $\pm$0.05 volts (1 percent regulation) at a maximum of 1 ampere with an input voltage of 18 $\pm$2 volts. The regulator efficiency exceeds 60 percent.

NOTE:
    RESISTOR R6 IS SELECTED DURING
    MANUFACTURE TO PRODUCE AN OUTPUT
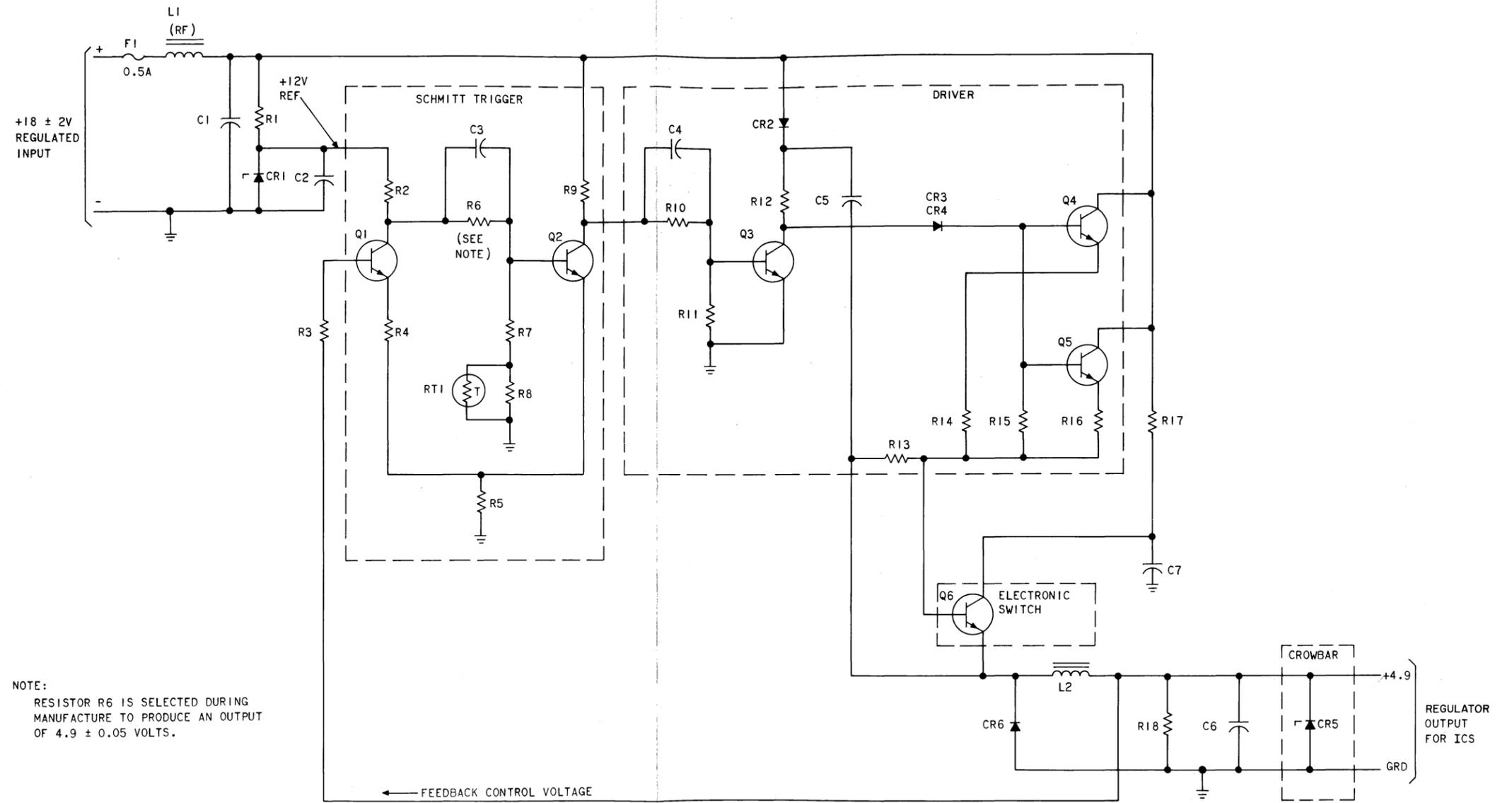   OF 4.9 ± 0.05 VOLTS.

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Fig. 64—166A1 Regulator—Functional Schematic

8. GLOSSARY OF TERMS AND ABBREVIATIONS

8.01   Uncommon terms and abbreviations used in this section are defined as follows:

TERM OR ABBREVIATION	MEANING
A1, A2, A3, A4, B1, B2, B3, B4	(1) Frequencies generated by TOUCH-TONE transmitter (see A- and B- group frequencies)
	(2) Received data lead designations on contact closure interface coupler
AB	Answer-back (lead, relay, or function)
A COM	A group common (CC interface coupler lead designation)
ACU	Automatic calling unit
AGD	AND gate disable
A-group frequency	A1—697 Hz A2—770 Hz A3—852 Hz A4—941 Hz
ASCII	American National Standard Code for Information Interchange (interface coupler designation)
AT	A-lead pickup to test console
ATNDT	Attendant (interface lead designation on BCM interface coupler)
ATT	Attendant relay designation
b1, b2, b3, b4, b5, b6, b7, b8	ASCII bits in time slots 2 through 9. Bits b1 through b7 are information bits; bit b8 is the parity bit.
BCM	Binary coded matrix (interface coupler designation)

TERM OR ABBREVIATION	MEANING
B COM	B group common (CC interface coupler lead designation)
B-group frequency	B1—1209 Hz B2—1336 Hz B3—1447 Hz B4—1633 Hz
C	(1) Connect relay on line control circuit
	(2) Clear lead on IC flip-flop
C1 (*)	Designation of signal produced by 11th button on 12-button TOUCH-TONE telephone set
C2 (#)	Designation of signal produced by 12th button on 12-button TOUCH-TONE telephone set
C3 (##)	Designation of signal produced by two consecutive 12th-button TOUCH-TONE signals, providing 13th output signal for ASCII receivers
CB	C relay break contact
CC	(1) Contact closure (interface coupler designation)
	(2) C relay common
CG	C relay ground
CM	C relay make contact
COB	Central office battery
CP	(1) Circuit pack
	(2) Character present (ASCII interface coupler)

TERM OR ABBREVIATION	MEANING	TERM OR ABBREVIATION	MEANING
CR	Central office ring	EAB	External answer-back
CS	Clear to send (interface designation on ASCII data sets)	EIA	Electronics Industries Association (Standard)
CT	Central office tip	ET	Even group test
DAS	Data auxiliary set	F-code	WE specification (for ICs)
DCD	Data carrier detector (interface lead designation on CC and BCM interface couplers)	FF	Flip-flop (IC 2-state switch)
		f_o	Frequency of operation
DCDI	Data carrier detector integrate (delay)	H	Holding (relay in line control circuit)
DCDM	Data carrier detector make contact.	HA	Enables interruptor for flashing lamp in console
DIVA	Digital inquiry—voice answer	HL	Hold lamp
DL	Data lamp	IC	Integrated circuit
DR	(1) Data receive (interface lead designation on CC and BCM interface couplers)	INV	Inverter
		KR	Console ring
	(2) Data ring	KT	Console tip
DR1	Data receive 1 (lead designation)	KTU	Key telephone unit
DR2	Data receive 2 (lead designation)	L	(1) Line lamp in customer console
DR3	Data receive 3 (lead designation)		
			(2) Latch (or lock) lead on IC flip-flop
DSR	Data set ready (interface lead designation on all interface couplers)	LB	Line bridge (relay in line control circuit)
DSRC	Data set ready common relay contact	LCC	Line control circuit (in basic receiver)
DSRM	Data set ready make relay contact	LF	Lamp flasher
		LS	Line status (relay in line control circuit)
DT	Data tip		
DTR	Data terminal ready (interface lead designation on all interface couplers)	LW	Lamp wink

TERM OR ABBREVIATION	MEANING	TERM OR ABBREVIATION	MEANING
MCC	Mode control circuit (in basic receiver)		(2) Key to access service line on DAS 804K
MT	Make talk relay	SG	Signal ground (interface lead designation)
NOT Q (or Q̄)	IC flip-flop output designation which is the complement of Q output. When Q = 1, NOT Q = 0; when Q = 0, NOT Q = 1.	SR	Spare line ring; service line ring
		ST	Spare line tip; service line tip
OS, OOS	Out-of-service—a feature provided by option (interface lead designation on CC and BCM data sets)	T	(1) Test (relay in single-set mode control circuit)
			(2) Toggle or trigger in IC circuitry)
OSUG	Out-of-service ungrounded (third wire control)	T1, etc	Test key designation on DAS 804K
OT	Odd group test	TA	Test relay A
P	Preset lead on flip-flop	TB	Test relay B
PL	Private line	T_D	Maximum echo delay
PLW	Private line, wet (talk battery)	TL	Test lamp
PSC	Parallel-to-serial converter	TLE	Test lamp enable (lead designation)
Q	IC flip-flop output designation (see NOT Q)	TM	Test mode (lead designation)
RA	Ring attendant	TOBC	Test mode release (lead designation)
RD	Received data (interface lead designation on ASCII interface coupler)	TOMC	Test mode release (lead designation)
RD1, RD2, RD3, RD4	Received data (interface lead designation on BCM interface coupler)	TR1	Test Release (lead designation)
		T_S	Minimum signal duration
RI	Ring indicator (interface lead designation on CC and BCM interface coupler)	TSTR	Test release key designation on DAS 804K
		UA	Unattended answer (lead designation)
S	Set lead on IC flip-flop	* (C1)	11th button on 12-button TOUCH-TONE telephone set
SER	(1) Service line		

TERM OR ABBREVIATION	MEANING
# (C2)	12th button on 12-button TOUCH-TONE telephone set
## (C3)	Two consecutive 12th-button TOUCH-TONE signals providing 13th output signal for ASCII receivers

9. REFERENCES

9.01 The following Bell System Practices provide additional information on Data Sets 403D- and E-types and associated equipment.

Reference Guide

590-004-106	Data Sets 403A-, D-, and E-Types

Data Set 403D-Type

594-025-100	Description
594-025-101	Multiple Data Set Station—Description and Operation
594-025-201	Multiple Data Set Station— Installation and Connections
594-025-301	Multiple Data Set Station—Maintenance
594-025-501	Multiple Data Set Station—Test Procedures
594-010-201	Data Sets—Multiple Installation Information
590-100-111	15A1, 15A2, and 15A3 Data Units—Identification
590-102-101	1B-Type Data Mounting—Identification

Data Set 403E-Type

594-026-100	Single Receiver Station—Description and Operation
594-026-200	Installation and Connections
594-026-300	Single Receiver Station—Maintenance
594-026-500	Single Receiver Station—Test Procedures
590-100-110	8A-Type Data Unit—Identification

Data Auxiliary Set 804G-Type

598-048-100	Description and Operation

Data Auxiliary Set 804K-Type

598-055-100	Identification

9.02 The following schematic drawings (SDs) and circuit descriptions (CDs) provide additional information on Data Sets 403D- and E-types and associated equipment.

SD- & CD-1D092-01 8A-Type Data Unit

SD- & CD-1D093-01 Data Set 403E-Type

SD- & CD-1D102-01 Data Auxiliary Set 804G-Type

SD- & CD-1D109-01 Data Auxiliary Set 804K-Type

SD- & CD-1D130-01 Data Set 403D-Type

SD- & CD-1D135-01 1B2 Data Mounting

SD- & CD-81878-01 31A-Type Power Unit

9.03 The following Development Letter (DL), Engineering Letters (ELs), and Plant Engineering Letter (PEL) contain pertinent information on Data Sets 403D- and E-types and associated equipment.

DL 102	Data Systems—Data Set 403D-Type, Data Set 403E-Type, and Data Auxiliary Set 804G-Type—Low Speed Parallel Transmission System for DATA-PHONE® Service
EL 51	Data Sets 403D- and 403E-Types; Data Auxiliary Sets 804G- and 804K-Types
EL 194	Data Sets 403D7, 403D8, and 403E4; Data Unit 15A3

EL 851   Data Set 403D-Type, Data Set 403E-Type, and Data Auxiliary Set 804G

PEL 7497   Data Set 403A-Type; Data Auxiliary Set 804C

9.04   Interface information is given in the following:

Data Sets 403D and 403E Interface Specification.

9.05   The following miscellaneous publications provide additional background information on Data Sets 403D- and E-types.

- Electronic Industries Association (EIA) Standard RS-232B dated October, 1965 (Superseded) or Standard RS-232C dated August, 1969

- American National Standard Code for Information Interchange—ASCII Standard X3.4 dated 1968 (formerly titled USA Standard Code for Information Interchange)

- Bell System Data Communications Technical Reference—Data Communications Using the Switched Telecommunications Network—dated August, 1970 (AT&T)

- IEEE Transactions on Communication Technology—Vol. Com-15 No. 6—December 1967: The TOUCH-TONE Telephone—Transmission of Digital Information. Also Vol. Com-17 No. 4—August 1969: Concentration and Switching Equipment for a Real-Time Multiple-Access Communication System

- Article—Power Sources for ICs—Electronic Component News—dated February, 1971

- Unnumbered BTL Memorandum—Multiple 403D Data Station—Board of Education of New York City—R. Campbell, G. Clement—dated May 7, 1969