DIGITAL DATA SYSTEM
510A-TYPE DATA SERVICE UNIT
DESCRIPTION AND OPERATION

CONTENTS PAGE

1. GENERAL

1.01 This section contains information concerning the physical and functional description and operation of the 510A-type data service unit (DSU). Other than a description of interface signals and customer options, information pertaining to the associated customer-provided equipment (CPE) is not given.

1.02 Whenever this section is reissued, the reason for reissue will be listed in this paragraph.

1.03 The 510A DSU (Fig. 1) is digital data system (DDS) customer station apparatus designed for transmission and reception of digital data over local transmission facilities. It provides, within a single unit, data transmission and network control functions equivalent to those provided by up to nineteen 500A-type DSUs. (Refer to Section 595-200-100 for information on the 500A-type DSU.)

1.04 Data and control signals from each customer interface circuit enter the DSU via ports at one of the three DDS subrate speeds (2.4, 4.8, or 9.6 kb/s) and are time-division multiplexed into a single bit stream suitable for transmission over a 56-kb/s 4-wire local loop. Received 56 kb/s signals are demultiplexed and distributed to the appropriate ports. The 510A-type DSU always works in conjunction with a subrate data multiplexer (SRDM) in the central office.

1.05 Normally, all ports in a 510A-type DSU operate at the same speed; however, for speeds of 9.6 and 4.8 kb/s, individual ports can be optioned to operate at half-rate.

1.06 The customer interface conforms to Electronics Industries Association (EIA) Standard RS-232-C. Three new test circuits are provided as options for testing through the interface connector.

2. PHYSICAL DESCRIPTION

2.01 The 510A-type DSU, which consists of a 2-shelf nest, measures 10 inches high, 19 inches wide, and 12.9 inches deep and weighs 40 pounds with CPs removed. The DSU will operate in an environment of +40 to +120°F, with a relative humidity of less than 95 percent. The 510A-L1 DSU is equipped with adjustable mounting brackets so that the DSU can be mounted in either a 19- or 23-inch rack. The 510A-L1/2 DSU consists of a 510A-L1 DSU mounted in a KS-20018-L19 cabinet for table or shelf mounting. The KS-20018-L19 cabinet measures 12.9 inches high, 20.3 inches wide, 14.7 inches deep and weighs approximately 13 pounds.

2.02 The two shelves of a 510A-type DSU (Fig. 2 and 3) have space for housing the following equipment.

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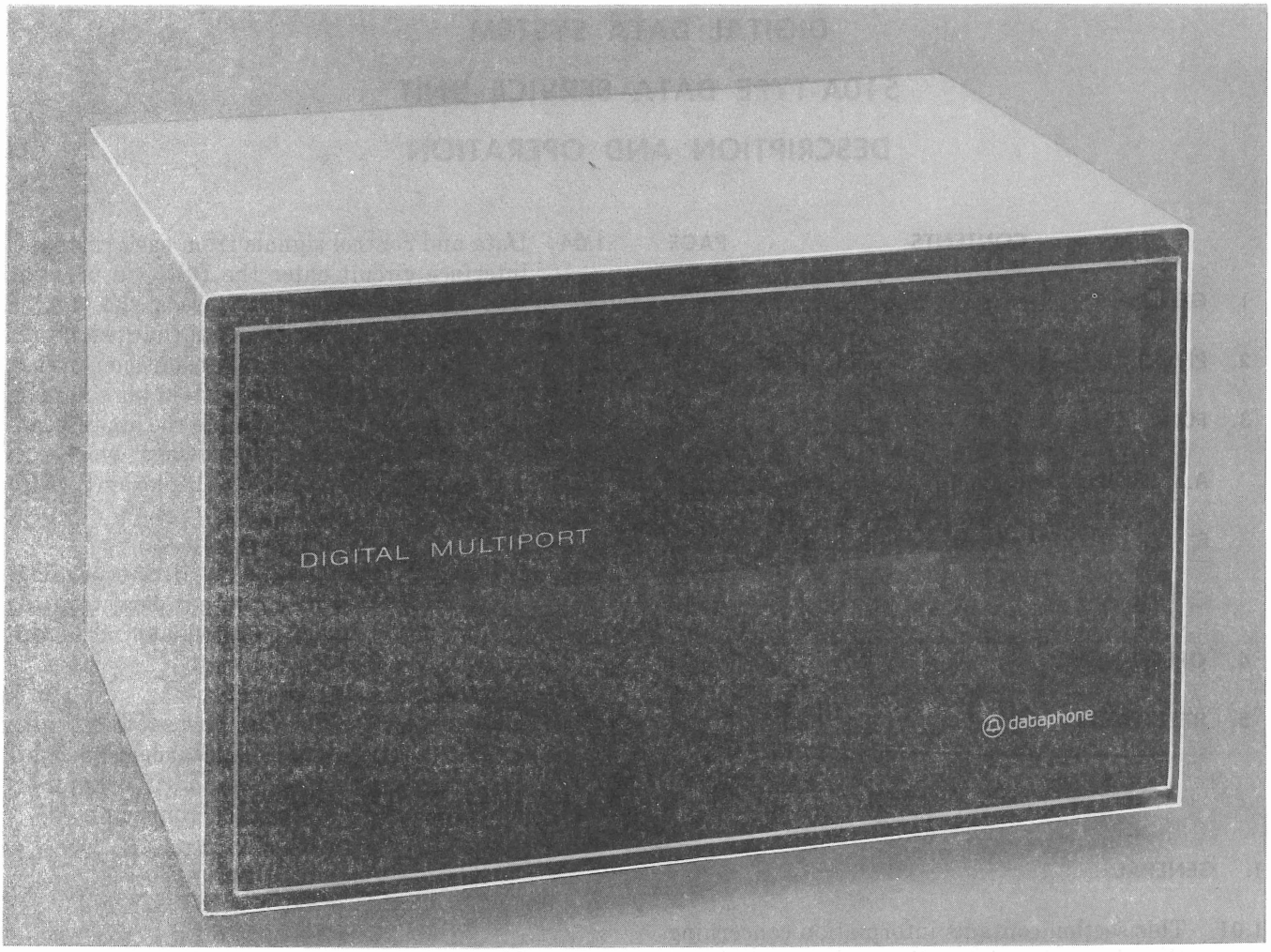

Fig. 1—Front View of a 510A DSU Mounted in a KS-20018-L19 Cabinet (510A-L1/2)

(a) ***112A Power Unit:*** Operates on customer-provided input of 105 to 129 Vac at 57 to 63 Hz with a maximum power requirement of 80 watts. The power unit converts the 117-Vac to output voltages of +5, +12, and -12 Vdc, which appear on terminal strip 1 on the rear of the power unit. The rear of the power unit contains a circuit breaker in the ac input circuit to protect the circuits from overvoltage damage and a Hubbell No. B-12583 male power connector which mates with the connector on the KS-14532-L20 power cable. The front of the power unit is protected by a hinged door which can be opened to gain access to the spare fuse for the fan described below.

(b) ***KS-21296-L1 Fan:*** This fan is used to cool the 112A power unit and is powered by the customer-supplied 117-Vac, 60-Hz source via the power unit. The fan is protected by a 1/2-amp fuse which is located on the rear of the power unit.

(c) ***Maximum of 25 KD-Type CPs:*** These CPs (KD21 through 26) measure 4.1 inches high, 10 inches long, and 0.97 inches wide, except for the KD21 CP which is 1.97 inches wide. All of the CPs consist of a single circuit board attached to a faceplate with the CP removal bracket as an integral part of the faceplate. The CPs that can be contained in a 510A-type DSU are as follows.

- Analog CP KD21 (Fig. 4)—One required per DSU. The faceplate of this CP contains four red (LOOPED, NS, DOS and MOS)

and two green (POWER ON and NORMAL) light-emitting diode (LED) indicators.

- Timing CP KD22 (Fig. 5)—One required per DSU.

- Demultiplexer (DEMUX) CP KD23—One required per DSU.

- Multiplexer (MUX) CP KD24 (Fig. 6)—One required per DSU.

- Group registers (GP REG) CP KD25—One required for ports 2 through 10 and another one required for ports 11 through 20.

- Port CP KD26 (Fig. 7)—One required for each customer data terminal. The faceplate of this CP contains four red LED indicators (RT, LL, RL and ER), four green LED indicators (DM, RS, CS and RR), and four push-to-operate and push-to-release switches (RT, LL, ST and RL).

2.03 A designation strip is located on the front of the 510A DSU for circuit and individual port identification. Two CARD RELEASE levers are also located on the front of the DSU; one is located above the CPs in the upper shelf and the second one is located below the CPs in the lower shelf. The CARD RELEASE levers are used to operate spring-loaded locking bars in the DSU to permit the CPs to be installed in or removed from the DSU.

2.04 To permit access to the rear of the 2-shelf nest, the rear panel on the 510A-type DSU (Fig. 8) is hinged at the bottom with push-pull quick operating fasteners at the top. Mounted on the rear panel are nineteen 25-pin EIA interface connectors and a terminal strip (TS1). The interface connectors terminate the customer interface leads of each individual port of the DSU and mate with customer-provided interface cables terminated in a Cinch or Cannon DB-19604-432 plug and a DA-51226-1 hood or equivalent. TS1 has four screw terminals and provides grounding connections.

2.05 The rear of the 2-shelf nest (Fig. 3) contains 26 KS-21479-L4 50-pin connectors of which 25 provide connections to be made to the circuit boards on each CP. The remaining KS-21479-L4 connector is not connected electrically but is used to retain a spare CP located in the left end of the lower shelf. Connection is made from each of the 19 EIA interface connectors on the rear panel of the DSU to the KS-21479-L4 port CP connectors via 20 conductor flexible cables. The cables to the port CPs in the lower and upper shelves are 8 and 18 inches long, respectively, and are crimped to the rear of the EIA interface connectors on one end. The cables connect to the wire-wrap terminals (pins 5 through 14 and 30 through 39) on the rear of the port CP connectors via a 20-pin crimp connector on the other end. Local loop connections to the 510A DSU are made to the four screw terminals located at the lower right-hand side on the rear of the nest via a 14-foot D4BD-87 cord. Customer-provided ac power is supplied to the power unit via a KS-14532-L20, 10-foot long power cord which has two parallel blades and a grounding pin on one end and a Hubbell No. 6600 connector body, or equivalent, on the other end.

2.06 Attached to the side of the 510A DSU are "L" shaped mounting brackets, with one leg longer than the other, which permit the DSU to be mounted in 19- or 23-inch racks or in a KS-20018-L19 cabinet. The brackets can be mounted at three locations on the sides of the DSU to permit mounting the DSU as follows (Fig. 9):

- 19-inch EIA rack—bracket at front with shorter leg extending outward

- 19-inch Bell rack—bracket at rear with shorter leg extending outward (cabinet use)

- 23-inch Bell rack—bracket at center with longer leg extending outward.

3. FUNCTIONAL DESCRIPTION

3.01 This part contains a brief functional description of the major circuit sections, customer interface circuits, test modes and various options.

3.02 A functional block diagram of the 510A-type DSU is shown in Fig. 10 and is described as follows. The 510A-type DSU exchanges customer data at any or all of the 19 ports (ports 2 through 20) at a data rate corresponding to one of the three DDS subrate speeds (2.4, 4.8, or 9.6 kb/s) which is chosen at the time of installation. Once the basic data rate is selected for the 510A-type DSU, all ports will operate at this data rate or, in the case of 9.6- and 4.8-kb/s ports, optioned to run at one-half the basic data rate. In this manner,

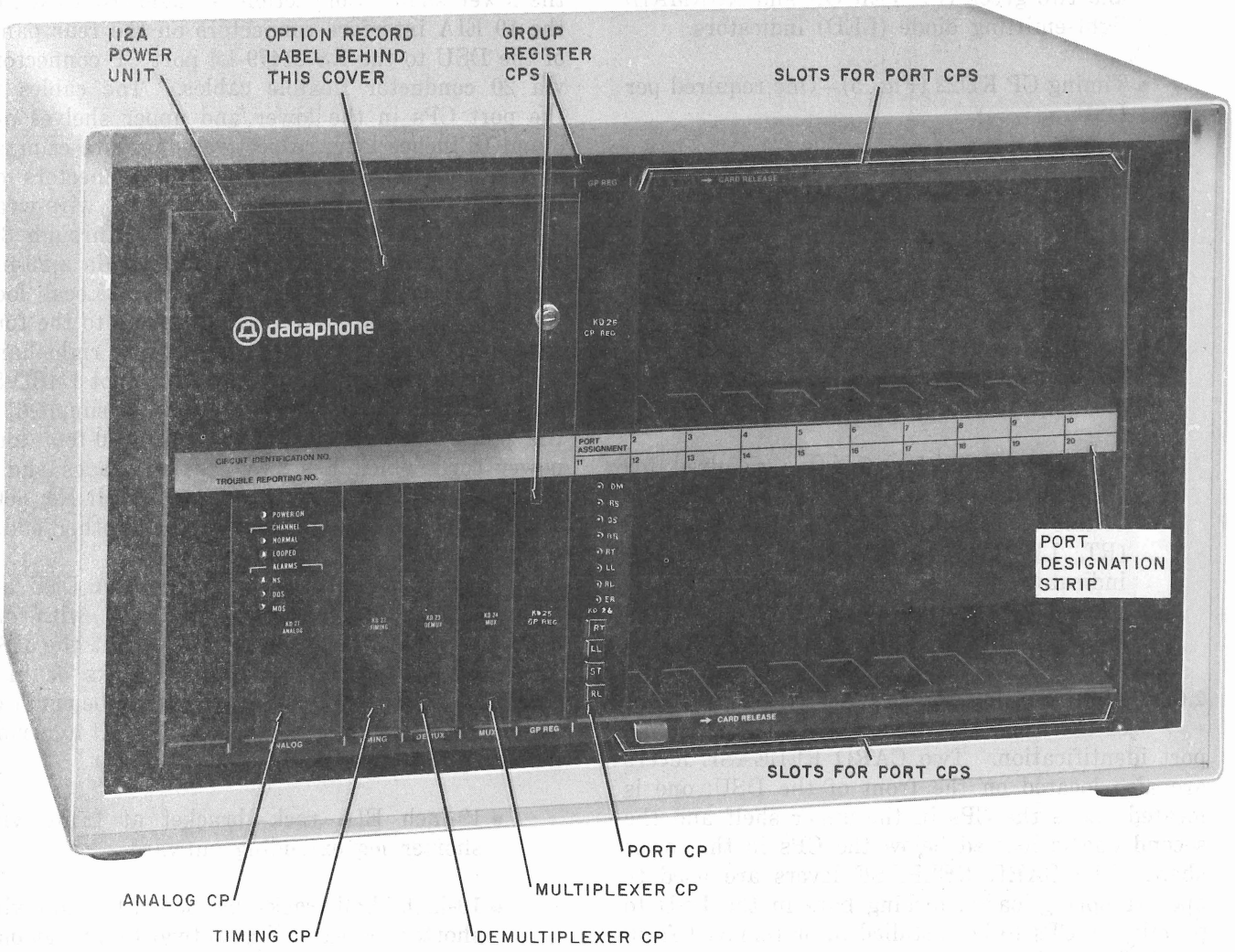

Fig. 2—Front View of a 510A DSU Mounted in a KS-20018-L19 Cabinet With Front Cover Removed

different speed ports may be intermixed in a single DSU.

3.03 Each customer interface connector has a port CP associated with it to provide for the interchange of data, timing, and control information between the CPE and the internal circuits of the DSU.

3.04 The common logic circuits, which are comprised of the group registers, multiplexer, demultiplexer and timing, are shared by all ports. The common logic circuits provide network control and provide for the addition and removal of the zero suppression code when the customer is transmitting and receiving all zeros, respectively. Two group registers containing shift registers and steering logic are required (one for ports 2 through 10 and another for ports 11 through 20) to transfer customer data, in byte format, from the port circuits to the multiplexer and demultiplexer under the control of clock signals from the timing circuit. The multiplexer circuit time-division multiplexes the customer data from the ports into a 56-kb/s bit stream in the form of 7-bit bytes. In order to identify each individual byte with its associated port and to maintain synchronization, each group of bytes (one for each port) contains a framing pattern which is composed of the first bit from each of the bytes. The demultiplexer circuit receives the multiplexed data bit stream and uses the framing pattern to separate the multiplexed data bytes into individual

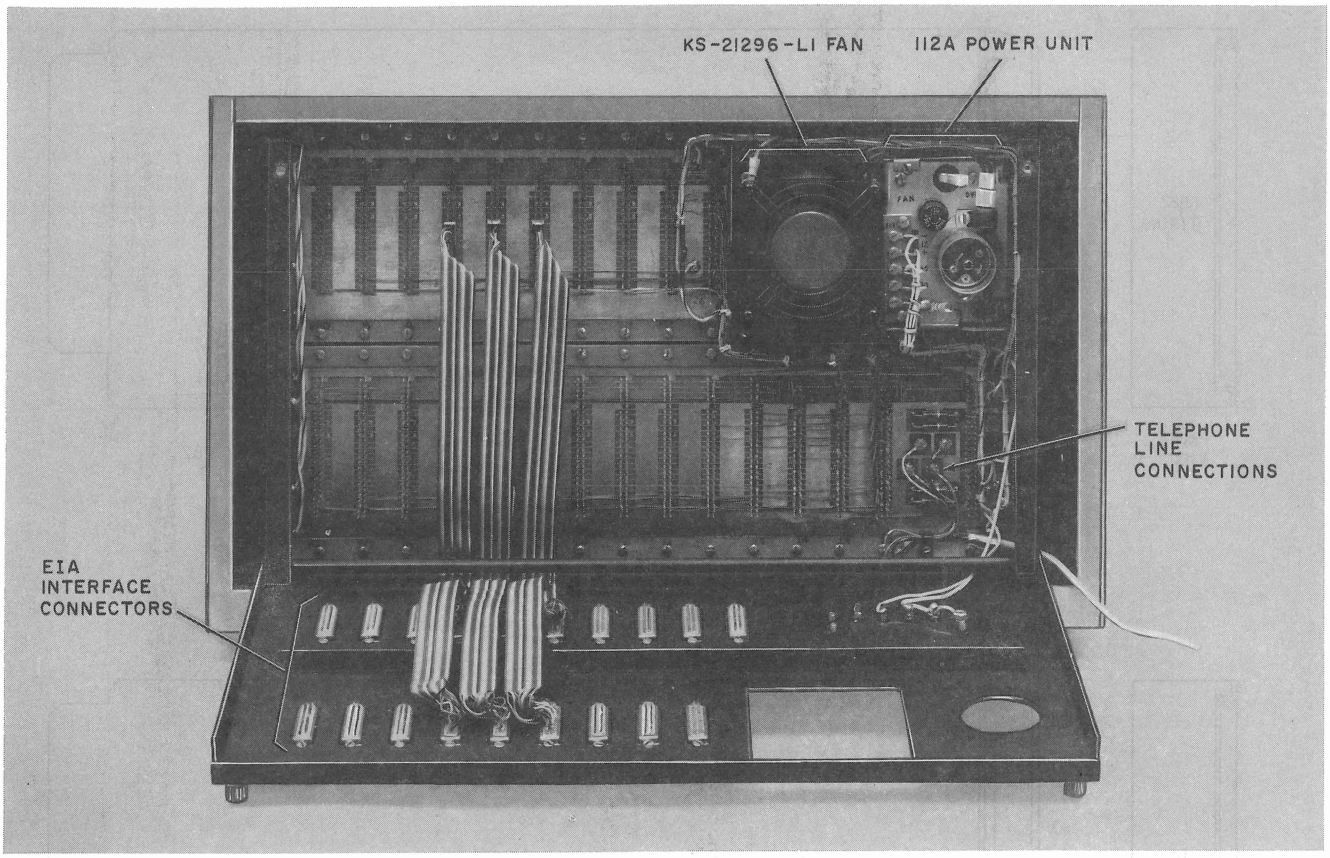

Fig. 3—Rear View of a 510A DSU Mounted in a KS-20018-L19 Cabinet With Rear Cover Lowered

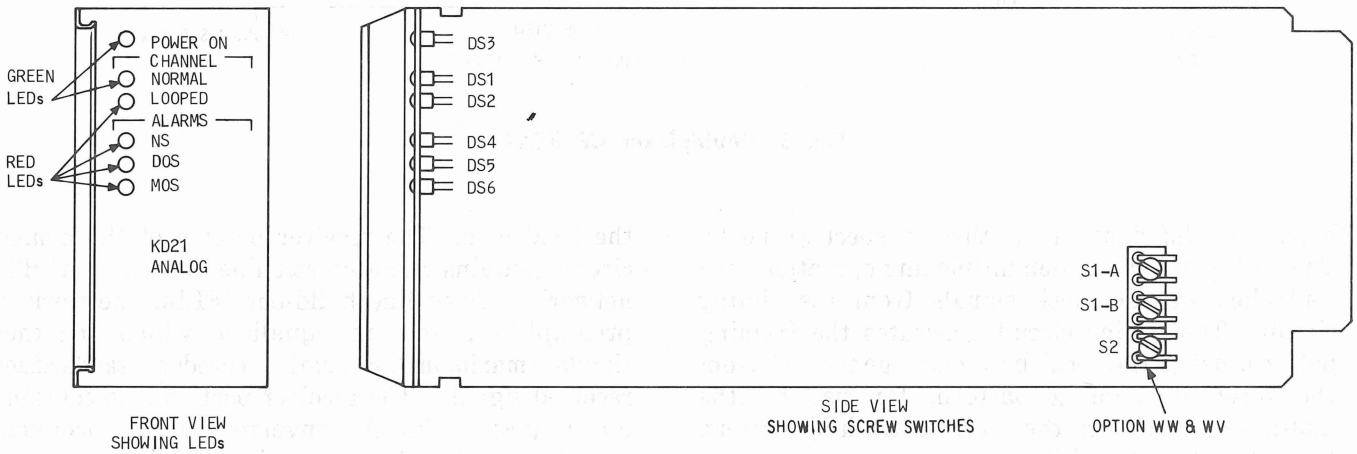

Fig. 4—Analog CP KD21

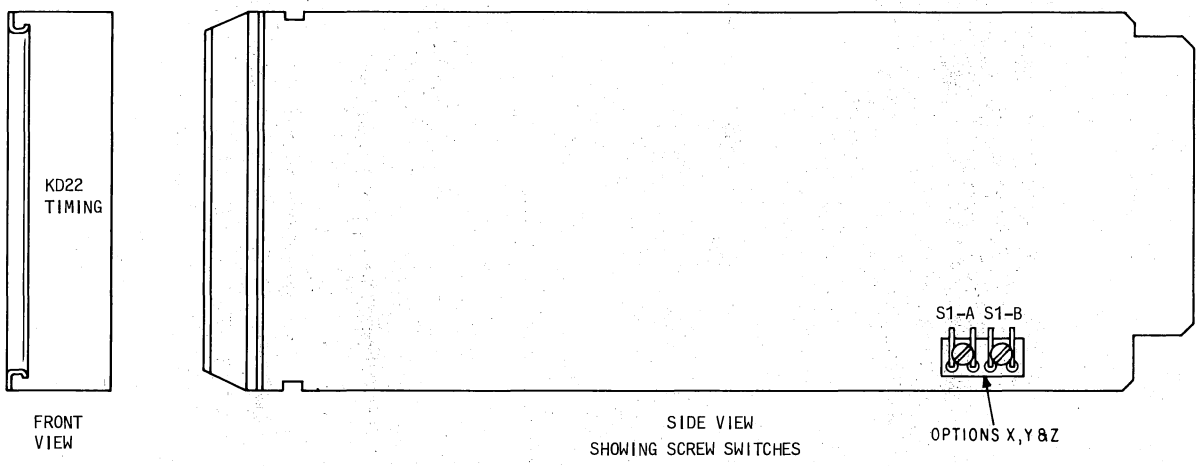

Fig. 5—Timing CP KD22

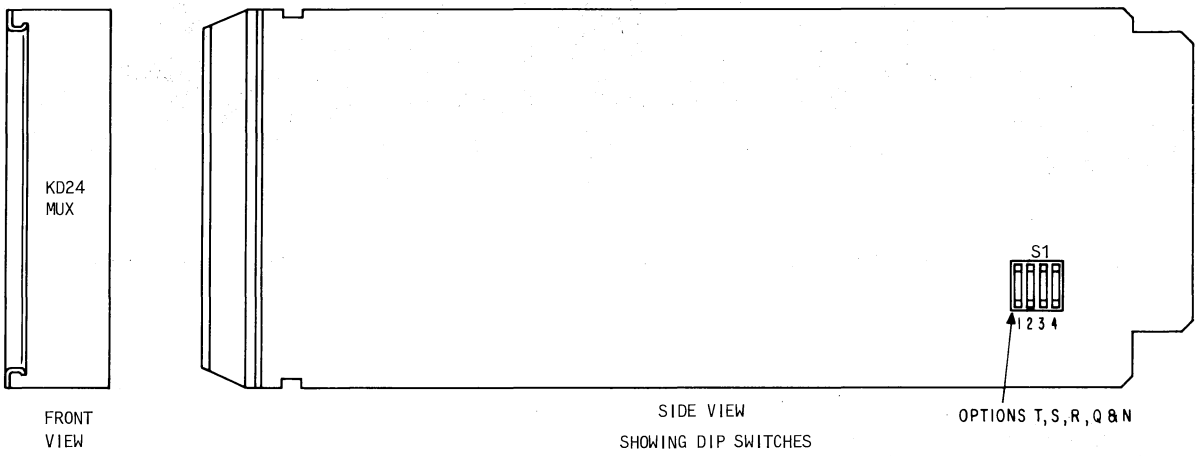

Fig. 6—Multiplexer CP KD24

bytes for distribution to their respective ports. The multiplexing and demultiplexing operations are controlled by the clock signals from the timing circuit. The timing circuit generates the framing pattern, using the local byte clock generated from the received framing pattern, for use by the multiplexer and uses the received framing pattern to control the demultiplexer.

3.05 The analog circuit provides the interface between the 4-wire local loop facility and the remainder of the 510A-type DSU. The line driver in the transmit portion of the circuit buffers and shapes the digital pulses for transmission over the local loop. The receiver portion of the analog circuit contains an automatic line build-out (ALBO) network, a fixed line build-out (FLBO) network, a preamplifier, and an equalizer which together simulate maximum line lengths to produce standardized received signals. The receiver portion also contains an analog-to-digital converter which produces logic-level pulses for processing by the remaining circuits.

3.06 The 112A power unit, which is fan cooled, converts the customer-supplied 117 Vac at 60 Hz to voltages of +5, +12, and -12 Vdc for use by all the circuits.

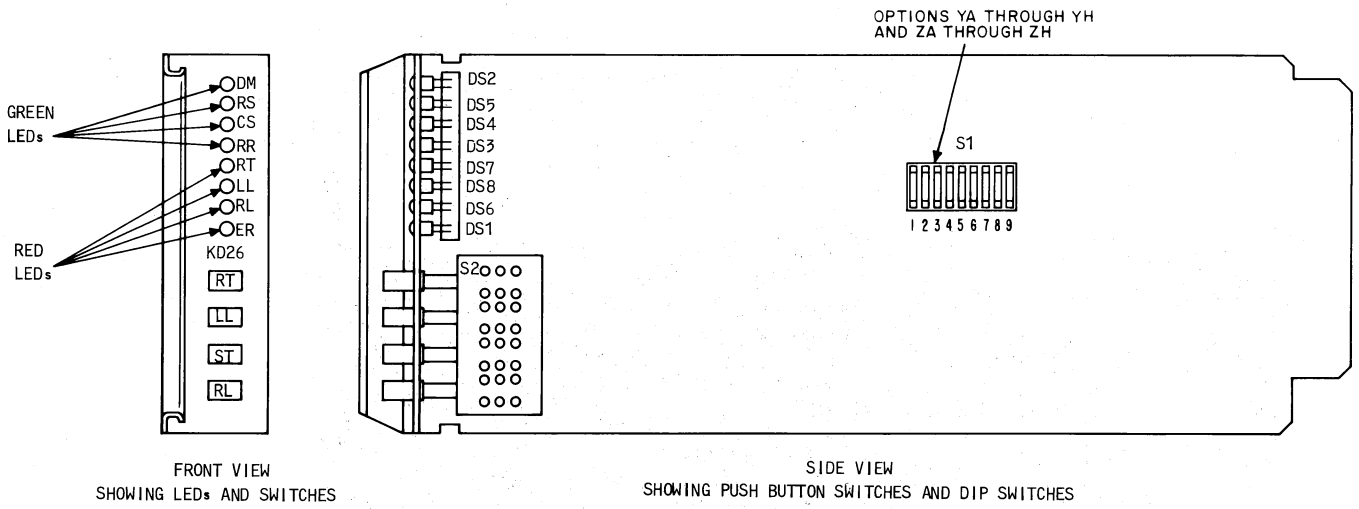

Fig. 7—Port CP KD26

A. Switches and Indicators

3.07 Mounted on the analog CP (KD21) faceplate are LED indicators which indicate the status of various circuit functions. Mounted on the port CP (KD26) faceplate are LED indicators and switches which indicate the status of the customer interface leads and activate tests, respectively. Descriptions of the switches and indicators are given below.

(a) Analog CP KD21

- ***Power On:*** A green LED which lights to indicate that +5, +12, and -12 volt outputs from the 112A power unit are all present.

- ***Channel Normal:*** A green LED which lights to indicate the presence of normal-polarity dc sealing current on the 4-wire local loop.

- ***Channel Looped:*** A red LED which lights to indicate that the sealing current on the local loop is reversed and the DSU is in the CHAN loopback test condition. When this LED is ON, the CHANNEL NORMAL LED will be OFF, and vice versa.

- ***NS:*** A red LED which lights to indicate that no digital signals are being received over the local loop.

- ***DOS:*** A red LED which lights to indicate that the demultiplex circuits are not properly synchronized with the SRDM in the central office.

- ***MOS:*** A red LED which lights to indicate that the multiplex circuits are not properly synchronized with the SRDM in the central office.

(b) Port CP KD26

- ***DM:*** A green LED which lights to indicate that the DSU port has turned the data set ready (CC) interface lead ***on.***

- ***RS:*** A green LED which lights to indicate that the port circuit has received and recognized a request-to-send (CA ***on***) condition from either the customer over the customer interface or from the circuits in the DSU port during the test mode.

- ***CS:*** A green LED which lights to indicate that the DSU port has turned the clear-to-send (CB) interface lead ***on.***

- ***RR:*** A green LED which lights to indicate that the DSU port has turned the received line signal detector (CF) interface lead ***on.***

- ***RT Indicator:*** A red LED which lights to indicate that the DSU port is in the remote terminal (RT) test mode.

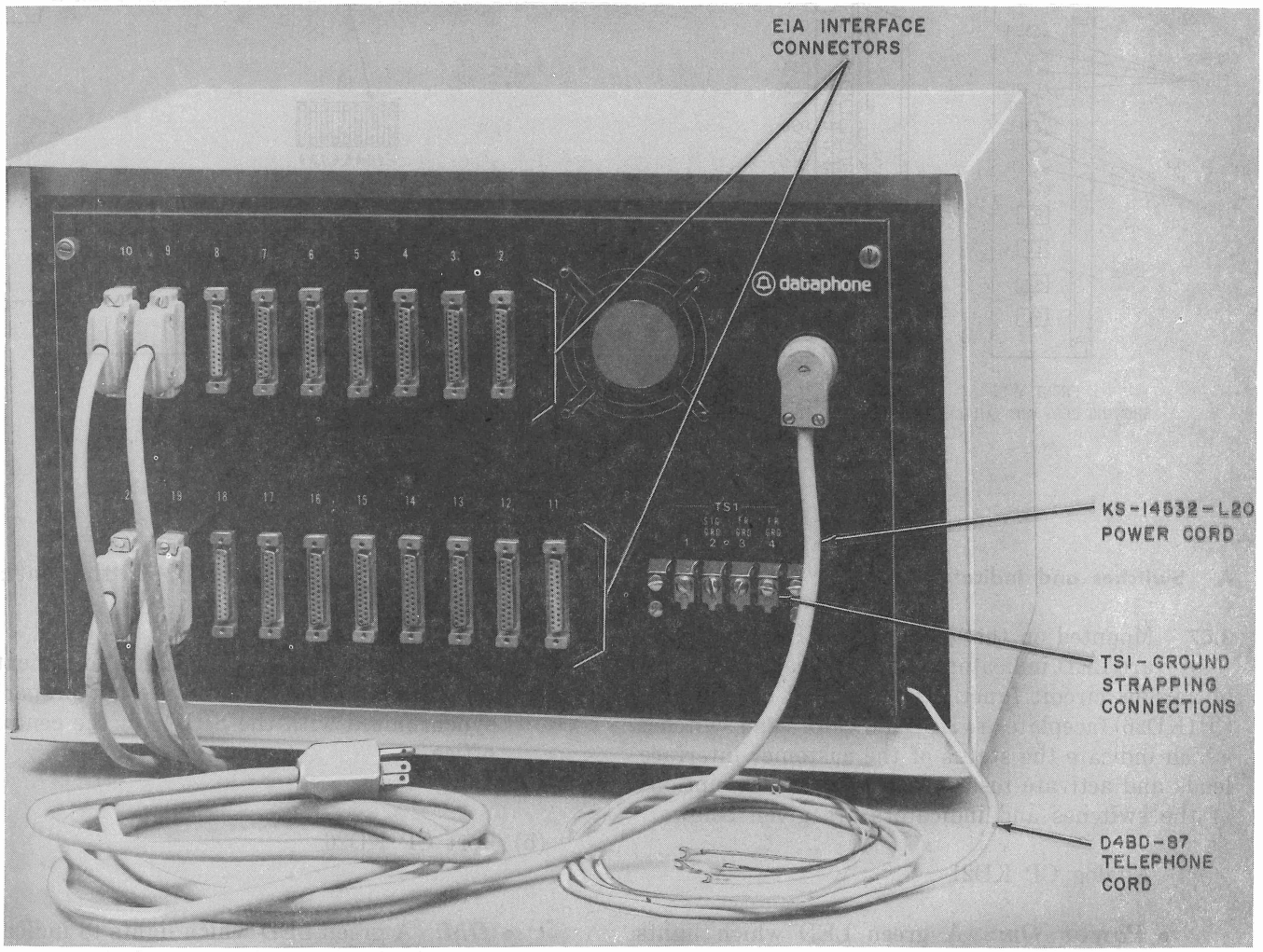

Fig. 8—Rear View of a KS-20018-L19 Cabinet Housing a 510A DSU

- ***LL Indicator:*** A red LED which lights to indicate that the DSU port is in the local line (LL) loopback test mode.
- ***RL Indicator:*** A red LED which lights to indicate that the DSU port is in the remote line (RL) loopback test or self-test (ST) mode.
- ***ER:*** A red LED which indicates the results of the self-test as explained in 3.09.
- ***RT Switch:*** When depressed, the DSU port is placed in the remote terminal test mode and connects the send lead, circuit BA, to the receive lead, circuit BB, at the customer interface.

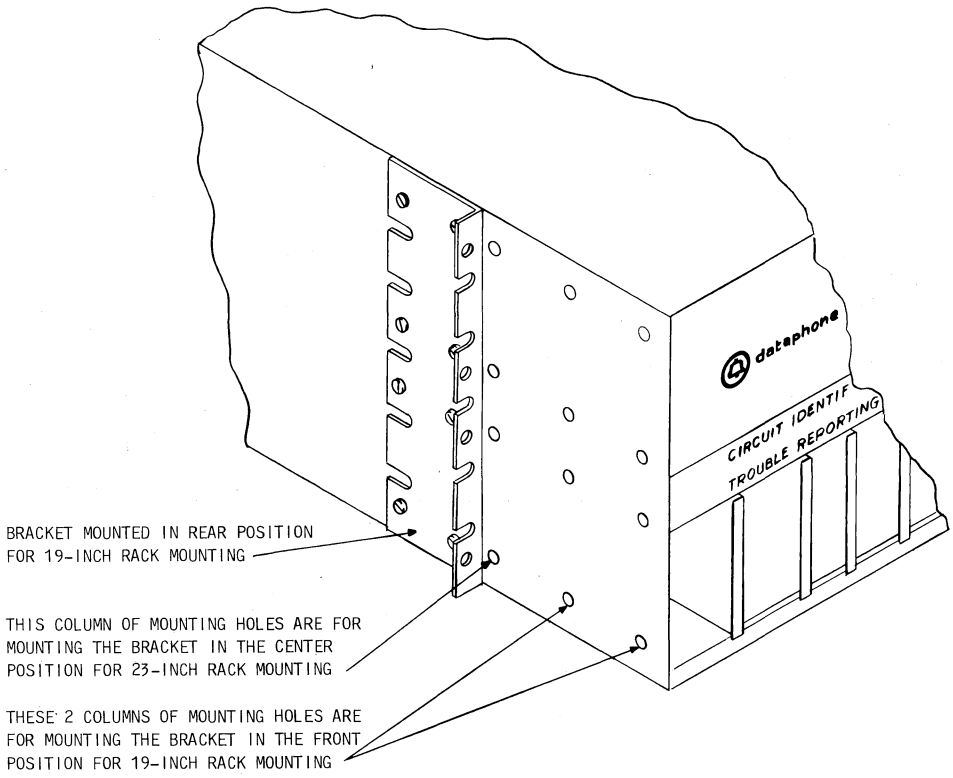

Fig. 9—Location of Mounting Brackets on 510A-L1 DSU

- ***LL Switch:*** When depressed, the DSU port is placed in the local line loopback mode, allowing a particular port to be tested through the customer interface.

- ***RL Switch:*** When depressed, the DSU port generates the DSU loopback code toward the distant DSU and activates the CA, CB and CF interface leads.

- ***ST:*** This switch when depressed, initiates the same actions as the RL switch except the interface leads are not activated.

B. Customer Interface Circuits

3.08 All of the interface circuits necessary for one port (ie, customer interface connector) are contained on one port CP KD26. Brief functional descriptions of the customer interface leads defined by RS-232-C between the DSU port and CPE are given below.

(a) ***Signal Ground:*** This lead is used as the common reference point for all interface circuits and may be connected to the power line ground as an installer option.

(b) ***Serial Clock Transmit (DB):*** The direction of signal flow on this lead is from the DSU port to the CPE. Signals on this lead provide the CPE with a timing signal that defines send data bit intervals.

(c) ***Serial Clock Receive (DD):*** The direction of signal flow on this lead is from the DSU port to the CPE. Signals on this lead provide the CPE with a timing signal that defines receive data bit intervals. DD is identical to DB.

(d) ***Transmitted Data (BA):*** Transmission path for data signals from the CPE to the DSU port. Bit transitions are coincident with positive transitions of DB. Data bits are transmitted if the following control conditions are met: CC, CA and CB leads ***on.***

(e) ***Received Data (BB):*** Transmission path for data signals from the DSU port to

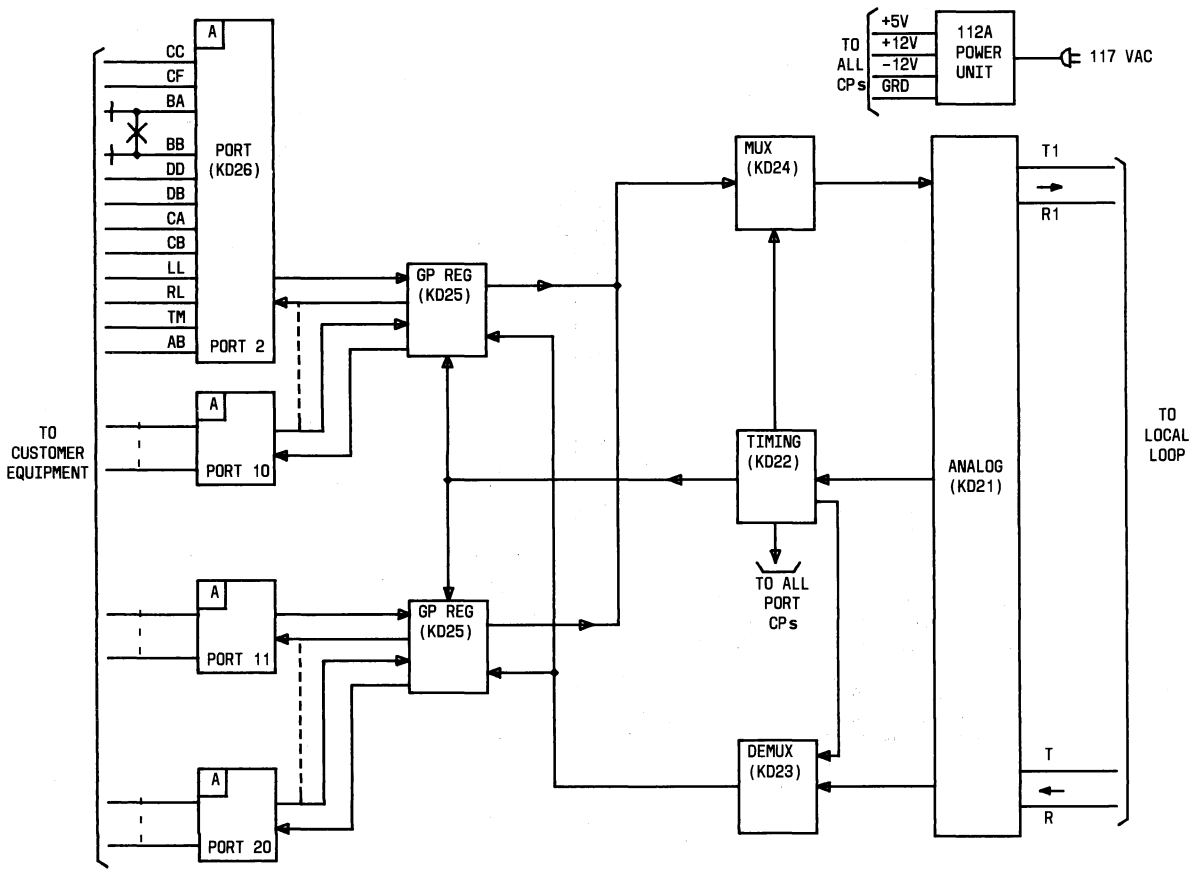

Fig. 10—Functional Block Diagram of a 510A-Type DSU

the CPE. Bit transitions are coincident with positive transitions of DD. BB is clamped in the marking state (binary one) when the CF lead is ***off.***

(f) ***Data Set Ready (CC):*** The direction of signal flow on this lead is from the DSU port to the CPE. Signals on this lead are generated by the DSU port to indicate that the DSU port is operating normally and that the port is not in a test mode. Once ac power is applied to the DSU, this lead is normally in the ***on*** condition. If the DSU port enters the test mode or if the DSU port is equipped with the system status option (option ZG) and an out-of-service indication (system failure) is received, this lead will turn ***off.*** However, if the DSU port is equipped with option ZE, the CC lead will not be turned ***off*** during LL or RL modes.

(g) ***Received Line Signal Detector (CF):*** The direction of signal flow on this lead is from the DSU to the CPE. Signals on this lead are generated by the DSU to indicate that the port is in the data mode. This signal is ***off*** when the port is idle, out of service, or in a test state. When this lead is ***off,*** the BB interface lead is held in the mark-hold (binary one) condition.

(h) ***Request to Send (CA):*** The direction of signal flow on this lead is from the CPE to the DSU. Signals on this lead are generated by the CPE to indicate that the data terminal wishes to transmit data. An ***off*** condition on this circuit causes the port circuit to transmit the idle control signal to the receiving DSU, provided the CC lead is ***on.*** A constant ***on*** condition must be maintained whenever the CPE has data ready for transmission.

(i) ***Clear to Send (CB):*** The direction of signal flow on this lead is from the DSU to the CPE. Signals on this lead are generated

by the DSU to indicate to the CPE readiness to transmit data. This lead turns ***on*** in response to an ***on*** condition on the CA lead, after a delay sufficient to allow the receiving DSU to exit the idle state. This assumes that the DSU common circuits are operating normally and that the port is not in a test mode. With the circuit assurance option (option ZH) installed, the clear-to-send indication is a result of an ***on*** condition on both CA and CF interface leads and the transmitting DSU must have exited the idle state before the CB lead turns ***on.***

Test Modes

3.09 Each DSU port has several test modes which aid in circuit verification and trouble location and the test conditions on each port are independent of those on any other port in the DSU. A brief description of each of these test modes is given below and the loopback locations are shown in Fig. 11.

(a) ***Remote Terminal or DSU Loopback (RT):*** Loops interface lead BA to lead BB and disconnects these circuits from the CPE. The data path through the DSU to this port and back can thus be checked from a remote point. The RT loopback can be activated by transmitting DSU loopback control characters from an STC or from the far-end DSU (if equipped with an RL feature). It can also be activated manually by operating the RT switch on the appropriate port CP.

(b) ***Local Line Loopback (LL):*** Produces a data path from the BA lead through the multiplexing circuits (but not the byte processing logic) and back through the port logic to the BB lead. This path allows the portion of the DSU associated with a particular port to be tested through the customer interface connector. Control circuits CA, CB, and CF are active for this test. The LL loopback can be activated by operating the LL switch on the appropriate port CP. It can also be activated by turning ***on*** circuit LL through the interface connector (LL is not a circuit specified in RS-232-C).

(c) ***Remote Line Loopback (RL):*** When the DSU is placed in the RL test mode, the DSU generates DSU loopback control characters which cause the far-end DSU to enter the RT test mode. When in the RT mode, the far-end DSU returns a distinctive byte pattern which is recognized by the local DSU byte processing circuits. If the proper pattern is returned, a verification signal is sent from the common circuits to the port which initiated the RL test. On that port, the BA circuit is looped through

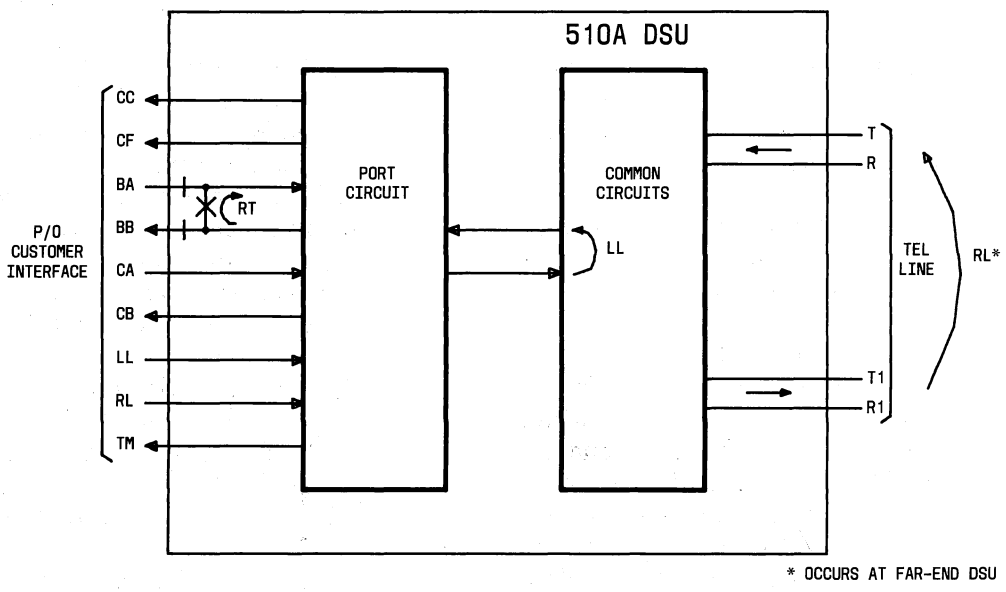

Fig. 11—Station Controlled Loopback Test Modes

an exclusive OR gate along with the verification signal to the BB circuit. Externally generated data signals transmitted via the BA circuit appear at the BB circuit, but not at the distant DSU, modified by the results returned from the RT loopback at the far-end DSU. A normally operating channel causes error-free data to appear at the BB circuit. A line error causes a corresponding error at the BB circuit. Failure to achieve the far-end RT condition causes the near-end BB circuit to be held marking, independent of the BA circuit. The effect of this RL test is to simulate a far-end data loopback test to verify operation of the entire subrate channel. Control circuits CA, CB, and CF are active for this test. The RL loopback can be activated by operating the RL switch on the appropriate port CP or by turning on circuit RL through the interface connector (RL is not a circuit specified in RS-232-C).

(d) ***Self-Test (ST):*** Self-test is the same as RL, except that none of the interface circuits are active. Test results are displayed on the ER indicator LED on the port CP. This LED turns ***off*** for a good test, flashes for each line error, and remains ***on*** if the far-end RT condition is not achieved. The self-test can be activated by operating the ST switch on the appropriate port CP.

C. Options

3.10 Installer options are available on the common circuit CPs and each port CP to adapt the DSU to various operating conditions and customer requirements as described below.

(a) ***Common Circuit Options:*** These options are contained on the common CPs and affect operation of all ports in the DSU.

- ***Option N:*** When this option is installed, a 360-byte delay (45 ms) is activated in the multiplex reframe circuit to maintain synchronization between the DSU and its associated SRDM. This option is located on the KD24 CP and installation depends upon such factors as the distance between the DSU and the associated SRDM, the data rate of the DSU, the data rate of the SRDM, and equipment on the loop between the DSU and the SRDM.

- ***Option Q:*** This option is similar to option N except a 290-byte delay (36.25 ms) is activated.

- ***Option R:*** This option is similar to option N except a 220-byte delay (27.50 ms) is activated.

- ***Option S:*** This option is similar to option N except a 150-byte delay (18.75 ms) is activated.

- ***Option T:*** This option is similar to option N except an 80-byte delay (10 ms) is activated.

Note: The above options (N, Q, R, S and T) adapt the DSU multiplexer reframe circuit to various round-trip circuit delays between the DSU and the associated SRDM. In order to determine which one of the above options should be installed, the total round-trip delay between the DSU and the associated SRDM must be known. The total round-trip delay can be calculated by adding together the delay of individual circuit elements between the DSU and the SRDM. (See Table A).

- ***Option YK and YL:*** These options are used to install (option YK) or remove (option YL) a connection of signal ground (power supply dc common) to frame ground (ac power line ground) via a strap on TS1.

- ***Options WV and WW:*** These options are used to install (option WV) or remove (option WW) an FLBO pad which is needed when the receive loop is so short that the ALBO pad alone cannot provide the proper compensation necessary to simulate a maximum length of local cable pairs. The switches necessary to install or remove these options are located on the KD21 CP.

- ***Option X:*** This option sets the basic data rate for the individual DSU ports to 2.4 kb/s and sets the maximum number of ports in the DSU to 19. The switch associated with this option is located on the KD22 CP.

- ***Option Y:*** This option sets the basic data rate for the individual DSU ports to 4.8 kb/s and sets the maximum number of ports in the DSU to nine. The switch associated

with this option is located on the KD22 CP. Individual ports can also be operated optionally at one-half the data rate by installing option ZA in the desired port CP.

- ***Option Z:*** This option sets the basic data rate for the individual DSU ports to 9.6 kb/s and sets the maximum number of ports in the DSU to four. The switch associated with this option is located on the KD22 CP. Individual ports can also be operated optionally at one-half the data rate by installing option ZA in the desired port CP.

TABLE A

CIRCUIT ELEMENTS DELAY BYTES

CIRCUIT ELEMENT		DELAY (BYTES)
510A DSU	9.6 kb/s	5
	4.8 kb/s	10
	2.4 kb/s	20
Local loop - per mile		0.2
56 kb/s OCU		1
DS-1 level multiplexer (T1DM, T1WB4 or T1WB5)		3.5
1ARDS Radio System - per mile		0.1
T1 carrier - per mile		0.2
SRDM	9.6 kb/s	5
	4.8 kb/s	10
	2.4 kb/s	20

(b) ***Port Circuit Options:*** Each port KD26 CP contains various installer options, which are described below, to adapt operation to customer requirements.

- ***Options ZA and YA (Port Data Rate):*** These options are used with option Y or Z above to allow a port to be operated at half rate (option ZA) or full rate (option YA).

- ***Option ZB and YB (RL Test at Interface):*** When these options are installed, nonstandard interface circuit RL is connected to (option ZB) or disconnected from (option YB) pin 19 on the customer interface connector and allows or inhibits electrical activation of the RL test mode, respectively, by the CPE.

- ***Option ZC and YC (LL Test at Interface)*** When these options are installed, nonstandard interface circuit LL is connected to (option ZC) or disconnected from (option YC) pin 11 on the customer interface connector and allows or inhibits electrical activation of the LL test mode, respectively, by the CPE.

- ***Option ZD and YD (TM Indication at Interface):*** When installed, these options connect nonstandard interface circuit TM to (option ZD) or remove it from (option YD) pin 13 on the customer interface connector , and provide or inhibit, respectively, an electrical indication to the CPE that the port is in a test condition.

- ***Option ZE and YE (CC State During RL or LL Test):*** When these options are installed, interface circuit CC is allowed to turn ***on*** (option ZE) or remain ***off*** (option YE) for RL or LL test modes.

- ***Option ZF and YF (Request-to-send):*** When option ZF is installed, interface circuit CA is always in the ***on*** state regardless of the state of the CA interface lead. When option YF is installed, interface circuit CA is in the ***on*** state when the CA interface lead is turned ***on.***

- ***Option ZG and YG (System Status):*** When these options are installed, interface circuit CC turns ***off*** (option ZG) or remains on (option YG) when the port receives an out-of-service indication.

- ***Option ZH and YH (Circuit Assurance):*** When these options are installed, interface circuit CB is allowed to turn ***on*** (option YH)

or inhibited from turning ***on*** (option ZH) when the receiving portion of the port is not in the data mode (CF ***off).***

4. OPERATION

4.01 This part contains information concerning the manual operation of a 510A-type DSU. The only manual operations required at a 510A-type DSU are performed during manual testing.

4.02 The manual tests are performed using the pushbutton switches on the faceplate of each port KD26 CP. To perform any one of the four tests (RT, LL, ST or RL), the appropriate switch must be depressed (engaged). To remove the DSU from a manually operated test, the switch must be depressed (released) again.

5. REFERENCES

5.01 The following schematic drawings (SDs), circuit descriptions (CDs), and Bell System Practices (BSPs) pertain to the 510A DSU:

NUMBER	TITLE
SD-& CD-1D263-01	Data System—Digital Data System—510A-Type Data Service Unit

CONTENTS PAGE