SWITCHED ACCESS REMOTE TEST SYSTEM 1A (SARTS-1A) PROCESS CONTROLLER 1A (PC-1A) AND ASSOCIATED EQUIPMENT GENERAL DESCRIPTION

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1. INTRODUCTION

A. General

1.01 This section gives a general overview and hardware description of the Process Controller 1A (PC-1A). The PC-1A is a minicomputer which supports the testperson-machine interface. It translates all testperson originated commands and communicates the necessary coded information to the far end. Also, the PC-1A translates all test results and displays them on the TP-52A keyboard display (KD).

1.02 When this section is reissued, the reason for reissue will be given in this paragraph.

1.03 The PC-1A (Fig. 1 and 2) is essentially a real-time computer system using all Digital Equipment Corporation (DEC*) PDP*-11/40 hardware. It can support up to 24 TP-52A positions and can control the testing process for up to 50 Remote Test Systems (RTSs).

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1.04 The PC-1A controls a high volume of traffic which is input not only from the 24 TP-52As but also from other PC-1As which may send messages to the 50 RTSs. Traffic flow is further increased due to the necessity of tracking protocol. Each of these messages must be tracked as they pass through their various stages of completion or failure. The software program to handle this large volume of traffic is covered by Section 666-611-101. Section 666-611-102 will describe the procedure for initializing the PC-1A. Sections 666-611-300, 666-611-301, and 666-611-500 will cover the maintenance and testing of the PC-1A. Related sections are 666-610-100, 666-612-100, and 666-613-100.

1.05 Throughout this section the words asynchronous and synchronous are used. For the purposes of this section, these terms are defined as follows. Asynchronous means that character transmission time is variable, but bits within the character are timed; a character transmission normally includes a start bit, several data bits, one or more stop bits, and an optional parity bit. Synchronous means that the data stream is continuous once the receiver is synchronized; data is generally transmitted in message blocks containing both information and timing signals.

1.06 This section pertains to the DEC PDP-11/40 which is a standard for the system. Software programs do not support nonstandard arrangements. The cabinet arrangement and typical floor plan are indicated in Fig. 1 and 2. For a more detailed description of PDP-11/40, refer to the ***digital PDP-11 peripherals handbook,*** 1975 and ***digital PDP-11/05/35/40 processor handbook,*** 1973.

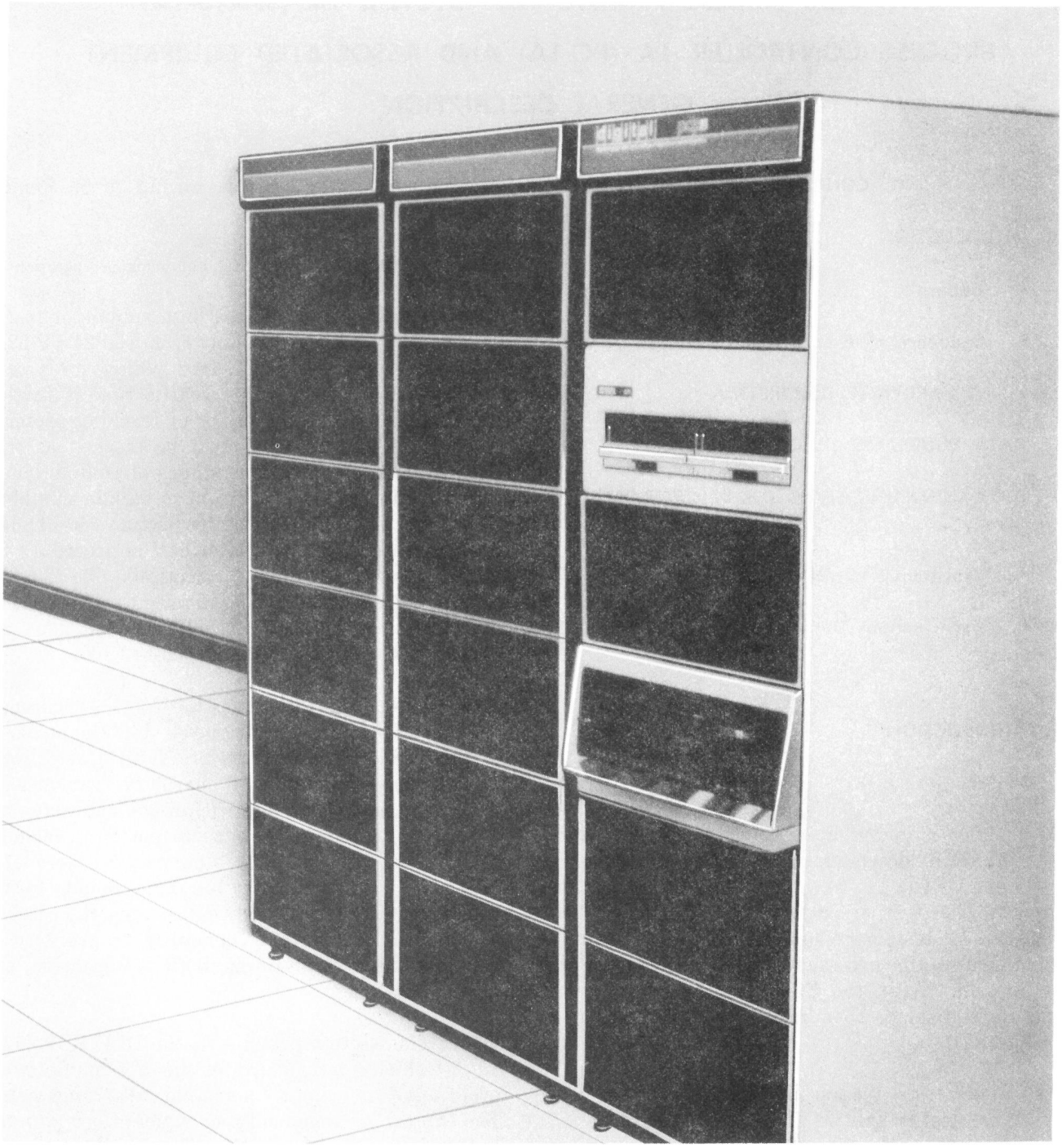

Fig. 1—Basic PC-1A Cabinet Arrangement

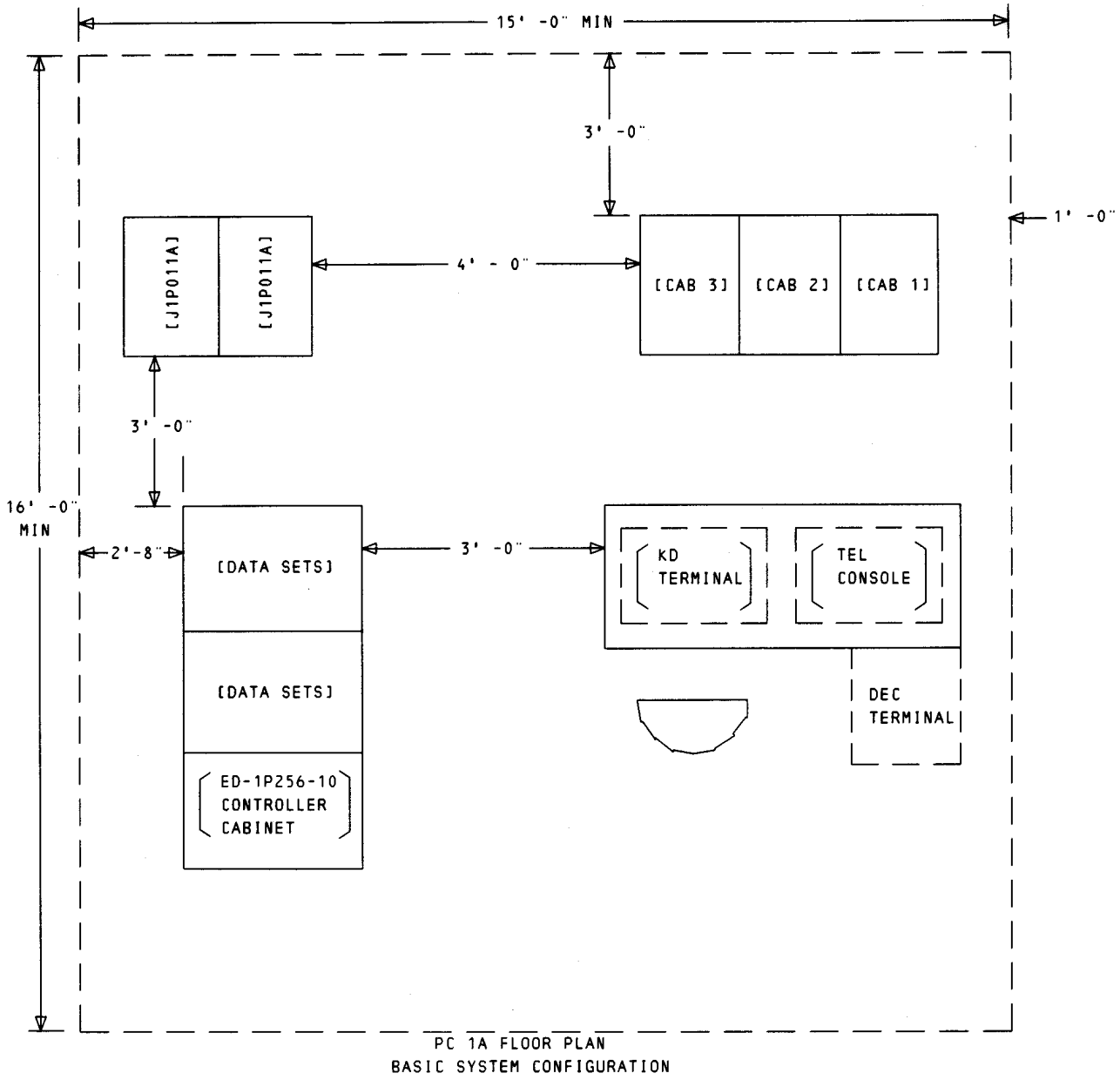

Fig. 2—PC-1A Floor Plan Basic System Configuration

B. Sequence of Events When Testing

1.07 The following paragraphs give a general sequence of events that occur when a testperson at a TP-52A wishes to access and test on a special service circuit at an RTS.

- The testperson keys in a command and circuit identity via a keyboard.
- The PC-1A returns a prompter display requesting the CO location, SMAS number, and other circuit access point identity data.
- When this data is received, the PC-1A determines if there is a private line data link or a DDD data link already established to the desired RTS. If there is, the access point data is passed to the RTS. If a data link is not established, the PC-1A refers to

a look-up table and dials the local (or DDD) number of the RTS through an outgoing Automatic Dial Interface (ADI) circuit.

- The RTS answers the call, receives an indication that the caller is either the primary or alternate PC-1A, and hangs up.

- The RTS now originates a call back to the calling PC-1A from the number stored in memory (either primary or alternate).

Note: The primary PC-1A can serve up to 50 RTSs. During Fallback and Recovery (see Section 666-611-102), these RTSs are served via an alternate PC-1A.

- When the PC-1A receives the call from the RTS and proper identification is made, the local (or DDD) data link is established.

Note: If a private line data link is used between the PC-1A and RTS, the call-up/call-back sequence just described is bypassed. However, a backup local (or DDD) arrangement is provided in the event that a failure occurs in the private line data link.

- The PC-1A sends the information received from the testperson to the RTS to access a circuit for a monitor-for-busy test (described in detail in Section 666-612-101). Once the circuit has been accessed and found to be idle, the testperson may perform various tests after completing entry of the access point testing data.

- The PC-1A receives these commands, verifies that the proper protocol is used, and sends them to the RTS.

Note: If the proper protocol is not used, the PC-1A returns error messages to the testpersons display. This will be covered in detail in Section 666-612-101.

- The RTS performs the tests and sends the results back to the PC-1A.

- The PC-1A sends the results to the testpersons display.

2. PC-1A HARDWARE DESCRIPTION

2.01 The PC-1A consists of processor equipment and input/output (I/O) peripherals to handle both the display terminals (TP-52A) and the data sets for communication with the RTS. The basic PC-1A processor equipment is housed in three DEC cabinets. Each cabinet measures 72 inches high by 21 inches wide by 30 inches deep and contains the following DEC hardware. Refer to FS1 of SD-1P000-01. (See Fig. 3.)

Note: The order in which the following units are listed does not necessarily refer to the way the units are connected to the UNIBUS* or how they are arranged in the DEC cabinets. References in ( ) are DEC coding.

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- UNIBUS and BUS JUMPER—BJ1 and BJ2 (BC 11A-02)

  All computer system components and peripherals connect to and communicate with each other along 56 lines of a bus called the UNIBUS. BUS JUMPERS connect bus cables together and accommodate impedance matching requirements.

- Processor (PDP-11/40 BS)

  Includes: CPU—Central Processor Unit with ECMO—Expandable Core Memory [32K] (PDP-11/40 BS, W/MF11-UR)
  TC—Terminal Controller (DL11-A)
  DEC—DECwriter (LA36-CA)

- CPU—Central Processor Unit (PDP-11/40 BS)

  The CPU connects to and controls the timing of the UNIBUS for peripherals, performs arithmetic and logic operations, and instructs decoding. The CPU decides which units do what and when it should be done.

- TC—Terminal Controller (DL11-A)

  The TC is a character-buffered communication interface that receives and transmits asynchronous data to the UNIBUS. When receiving data, the DL11-A converts an

asynchronous serial character from the LA36-CA into a parallel character required for transfer to the UNIBUS. When transmitting data, a parallel character from the UNIBUS is converted to a serial character and transmitted to the LA36-CA.

- DEC—DECwriter (LA36 Terminal)

  The DECwriter is a DEC equipment machine which looks similar to a typewriter and is located in the vicinity of the PC-1A. The unit communicates with and is responsible for the PC-1A. It interfaces with the PC-1A as a local I/O device. The DECwriter is not to be confused with the SARTS Maintenance Position (SMP), which serves other functions.

- MMU—Memory Management Unit (KT11-D)

  The MMU controls various overall user programs, manages assignment of memory and peripheral resources, and safeguards integrity of the system by control of each user program.

- EAU—Extended Arithmetic Unit (KE11-E)

  The EAU executes high-speed arithmetic operations (multiply, divide, and long shift).

- ECM1—Expandable Core Memory (MF11-US)

  The ECM1 is a read/write random access, coincident current memory. Parity is used to check the integrity of the stored data. Core memory is available in basic increments of 16,384 words (16K) and is designated MM11-U. The MF11-U connects to the UNIBUS and contains cables and mounting assembly that can be expanded to 32K of words. The basic PC-1A has 32K of words in the CPU and an additional 96K of words in ECM1 for a total of 128K of parity core memory.

- SMD—Floppy Disk (RX11-BA)

  The SMD reads program information into the core memory of the PC-1A. The unit accommodates two "floppy disks". One disk contains the generic program and the other disk is used to record Site Dependent Data. (Refer to Section 666-611-102.)

- BL—Bootstrap Loader (BM873-YA)

  The BL is a general purpose program loader for all PDP-11 systems. It consists of one circuit board that fits into a small peripheral controller (SPC) slot. It permits quick loading of the bootstrap programs or restarting of PC-1A programs from the disks. Bootstrap programs are contained in 256-word read-only memory (ROM).

- PC—Programmable Clock (KW11-P)

  The PC furnishes programmed real-time interval interrupts and interval counting. Programs can be given a time period to complete. If not completed within that period, an error message is generated.

- BLF—Bootstrap Loader, Floppy (M792-YL)

  This loader is used with the Floppy Disk similar to the BL listed above.

- BR—Bus Repeater (DB11-A)

  The BR is a physical and electrical extension of the UNIBUS. Each BR allows a 50-foot extension in bus length and will drive 19 extra bus loads.

- WD—Watchdog Timer (KW11-W)

  The WD detects PC-1A system malfunctions by timing out when it is not recycled. It is set for a gross time interval and is recycled from several key hardware and software events. These events are significant in performing assigned tasks. Failure to recycle indicates the system cannot recover from a hardware problem or sanity check.

- Power Supply

  Each PDP-11/40 cabinet contains a Cabinet Power Control Unit (located at the bottom of the cabinet) which is used to distribute the ac power to outlets located on the inside of the cabinet.

2.02 The following units supply data communication in and/or through the Processor.

- LMU [00] and [01]—Line Mux Units [00] and [01] (DH11-AD)

  Each LMU is a programmable asynchronous serial line multiplexer which connects the PC-1A to 16 communication lines. These lines accommodate incoming private lines or dialed connections from RTSs. The basic PC-1A will have two LMUs (units 00 and 01) with space on the UNIBUS to add one additional unit for future growth. Position 07 of LMU 01 is reserved for the Processor Controlled Alarm circuit SD-1P104-01.

- SI—Synchronous Interface, SI0 and SI1 (DU11-DA)

  The SI is a communication unit that interfaces the PC-1A to a serial synchronous line. Technically, the SI is a single-line, program-controlled, double-buffered communication unit. Synchronous data between the PC-1A and the Station Cluster Controller (SCC) and/or a Minicluster Controller (MCC) interfaces through the SI. A List 1 PC-1A is installed with two SIs. Space is reserved on the UNIBUS to add two additional units for future growth. An SI can be used to provide access with a test site when acting as an ***alternate*** PC-1A to an out-of-service ***primary*** PC-1A. The term "test site" is defined in Section 666-612-100 as the interconnection of TP-52As and associated equipment.

- ADI—Auto Dial Interface (DN11-AA)

  An ADI interfaces the PC-1A to an 801 Automatic Calling Unit (ACU). The interface is the Module Set Interface (MSI). This unit permits the PC-1A to dial an assigned telephone number (which has been programmed) to establish a data link to an RTS.

2.03 Each PC-1A installation will be engineered and unique to a specific location. To be able to meet the various requirements, optional equipment has been made available including:

Disk Controller and memory consisting of:
(1) Disk Controller (DCO) [RK 11]
(1) Disk Memory (DMO) [RK 05]

Magnetic Tape Controller and Transport consisting of:
(1) Magnetic Tape Controller [TM11]
(1) Magnetic Tape Transport [TU 10]

Module Set Interface (MSI) 0012 or 0013 (DN11-DA)

Line Multiplex Unit (LMU02) [DH11-AD]

Synchronous Interface (SI) 2 or 3 (DU11-DA)

Null Modem Clock (C) [DFC11-A]

3. DATA EQUIPMENT DESCRIPTION

3.01 All data sets and data cabinets associated with the PC-1A are customer ordered and engineered. They must be located within 50 cable feet of the PC-1A.

3.02 The data sets are mounted in a KS-20018 or equivalent data set cabinet.

3.03 The following data sets or their equivalent are to be used.

- 202T (type)—an asynchronous, 1200 bits/sec. data set used for the private line or dedicated data link between the PC-1A and the RTS. The 202T connects to the PC-1A through the LMU. The 202T will use the 2-wire option.

- 202S (type)—an asynchronous, 1200 bits/sec. data set used for incoming or outgoing calls, over the DDD network, between the PC-1A and the RTS. The 202S connects to the PC-1A through the LMU.

- 801C4 (type)—an ACU used for the purpose of making outgoing calls via the 202S data set from the PC-1A.

- 208A (type)—a synchronous, 4800 bits/sec. data set used between the PC-1A and the SCC when the distance is greater than 50 feet. It may also be used between the SCC and an alternate PC-1A. The 208A connects to the PC-1A through a synchronous interface unit.

4. DATA COMMUNICATION LINK DESCRIPTION

4.01 The PC-1A interfaces TP-52As with RTSs. Communication with

- TP-52As is via synchronous data lines.
- RTSs is via asynchronous data lines.

A. Synchronous Data Links (Figure 3)

4.02 One SI can accommodate a maximum of 24 TP-52As and 12 associated printers. Since two SIs are provided in a basic system, with two more optional, a great amount of flexibility is inherent in the system.

> ***Example:*** Two test sites can be accommodated, one local and one remote, using two SIs. Optional SIs can be used for rehoming plans and/or support an SMP. (See Sections 666-610-500 and 666-611-102.)

4.03 Synchronous interconnection is accomplished using

- Null modems
- Private lines with 208A-type data sets.

Null modems are used if cable to the SCC or MCC is less than 50 feet (a local test site).

> ***Note:*** Null modems can only connect to SIs equipped with null modem clocks numbered 1 and 2.

The 208A-type data sets are used whenever the 50-foot cable length is exceeded. This enables a remote test site to be serviced by a private line. (Dialed up backup of the private line will be available.)

SIs are direct cabled from the PC-1A to the SYNC COMM. — NULL MODEM CONNECTOR PANEL, ED-1P255-30, located in a customer ordered data set cabinet (KS-20018 or equivalent) per the typical arrangement shown on ED-1P376.

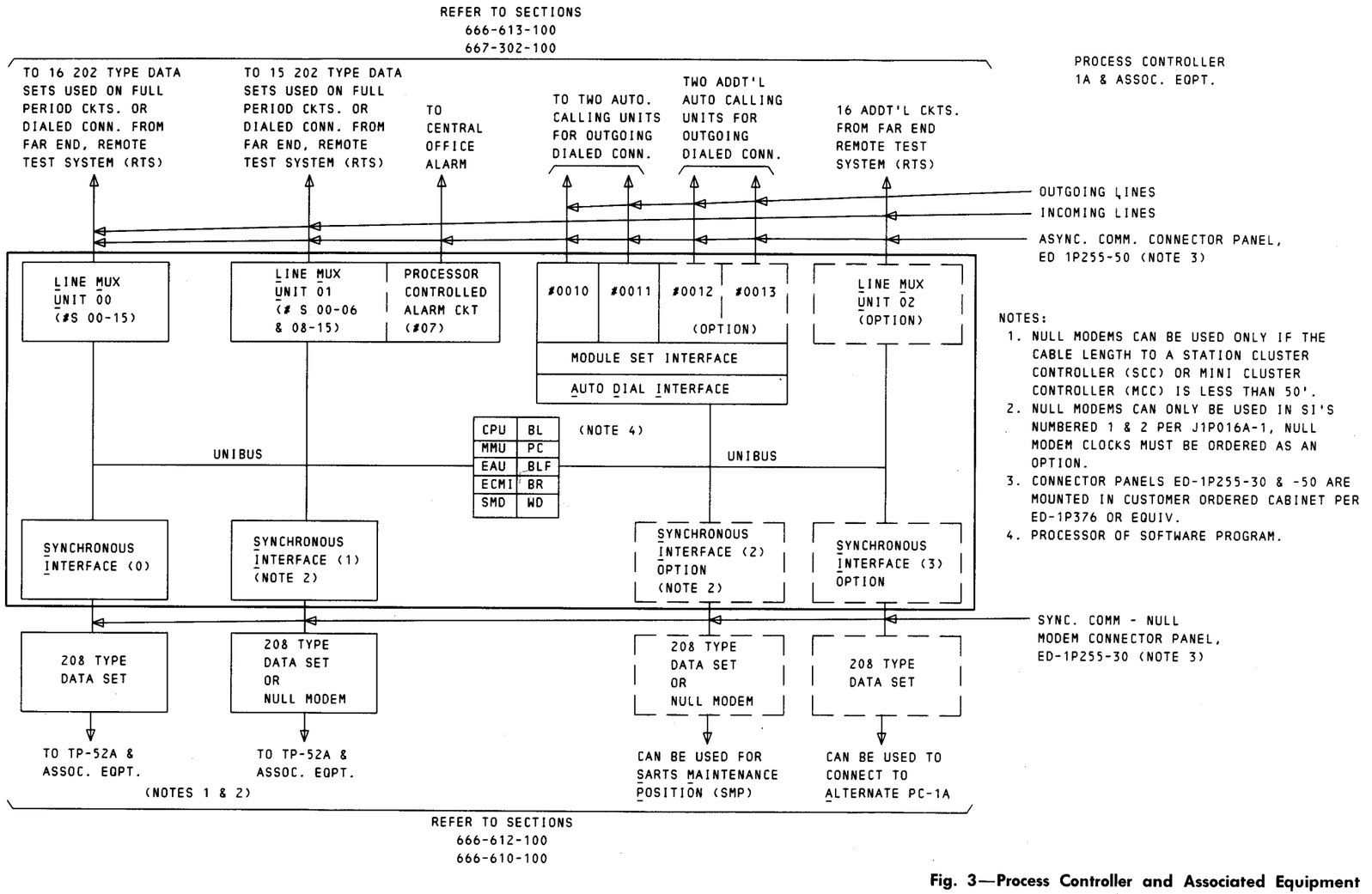
B. Asynchronous Data Links (Figure 3)

4.04 In a basic system, the PC-1A is equipped with two ADIs and 31 lines to LMUs. ADIs connect an LMU line through an 801C4 (or equivalent) ACU for ***outgoing*** calls to the RTSs.

> ***Note:*** The PC-1A calls an RTS, identifies itself, and hangs up. The RTS then places a call to the PC-1A.

The RTSs will place ***incoming*** calls through the LMU lines. The test command procedure will be conducted over this connection. Options allow an increase of two additional ADIs and 16 LMU lines. Certain LMU lines can be assigned to permanent full period circuits connecting to predetermined RTSs requiring full time testing capability.

The LMU lines and ADIs are direct cabled from the PC-1A to the ASYNC. COMM. CONNECTOR PANEL, ED-1P255-50, located in a customer ordered data set cabinet (KS-20018 or equivalent) per the typical arrangement shown on ED-1P376.



NOTES:

1. NULL MODEMS CAN BE USED ONLY IF THE CABLE LENGTH TO A STATION CLUSTER CONTROLLER (SCC) OR MINI CLUSTER CONTROLLER (MCC) IS LESS THAN 50'.
2. NULL MODEMS CAN ONLY BE USED IN SI'S NUMBERED 1 & 2 PER J1P016A-1, NULL MODEM CLOCKS MUST BE ORDERED AS AN OPTION.
3. CONNECTOR PANELS ED-1P255-30 & -50 ARE MOUNTED IN CUSTOMER ORDERED CABINET PER ED-1P376 OR EQUIV.
4. PROCESSOR OF SOFTWARE PROGRAM.

Fig. 3—Process Controller and Associated Equipment