NO. 3 PROCESS CONTROLLER
INTERCONNECTIONS AND COMMUNICATIONS
SWITCHED ACCESS REMOTE TEST SYSTEM 1A

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1. GENERAL

1.01 This practice describes the interconnections and communications between the elements of a Switched Access Remote Test System 1A (SARTS 1A). The No. 3 process controller (No. 3 PC) is referred to as PC in this practice.

1.02 Whenever this practice is reissued, the reason for reissue will be listed in this paragraph.

1.03 The elements, or subsystems, of SARTS 1A are the test position 52A (TP 52A) and associated equipment, the PC and associated equipment, and the Remote Test System 5A (RTS 5A). The RTS is used to access circuits via the Switched Maintenance Access System (SMAS) or the Digital Access Cross-Connect System (DACS). Each subsystem is a software and/or hardware system which interconnects with other subsystems to transmit/receive test commands and results.

1.04 Each subsystem is equipped with one or more standard Electronics Industries Association (EIA) data communication interface(s). Each subsystem also has conventional telephone subscriber line circuit appearances which allow local and/or direct distance dialing (DDD) switched data connections to be established between subsystems. Conventional telephone communications that interconnect the RTSs and TP 52As are also provided for the test status verification (TSV) and talk features of SARTS 1A. All data facilities (private line or switched) and central office (CO) line circuit assignments for the SARTS 1A intersystem communications are locally engineered and furnished.

1.05 The PC and each test site location, consisting of a TP 52A, are interconnected by a private line data facility with manual dial backup. Communication between these subsystems is with synchronous data. The PC and RTSs are interconnected by either a private line data facility or a full-duplex DDD connection between data sets. Communication between these subsystems is with asynchronous data. The subsystem interconnections are shown in Fig. 2. Synchronous data links interconnect the synchronous interface (SI) or synchronous multiplexer (SM) units of the PC with a station cluster controller (SCC) or a minicluster controller (MCC) of a DATASPEED* 40/4 terminal set or a 4500 controller of a DATASPEED 4540 terminal set.

1.06 In the PC, the synchronous data links connect to the SI or SM and controllers through patching arrangements at synchronous communication panels (ED-1P255-30). A typical synchronous data link arrangement for a PC is shown in Fig. 1.

1.07 Asynchronous data links interconnect the asynchronous multiplexer (AM) of the PC with the RTS control circuit of the RTS 5A. When inter-PC communications are required, asynchronous data links are used to interconnect each PC.

1.08 The asynchronous data links connect to the PC and appear as lines on an AM distribution panel. A typical asynchronous data link arrangement to an RTS or to another PC is shown in Fig. 3.

* Registered trademark of AT&T.

2. PC-TO-TEST SITE DATA LINK (SYNCHRONOUS)

A. Facilities

2.01 When the associated equipment at the test site and the PC are located within 50 cable feet of each other, a null-modem 4-wire private line circuit (shown in SD-1P204-01) and patching cords provide the synchronous data line interconnect arrangement.

2.02 The null-modem arrangement must connect an SI with the test site. For SI, a null-modem clock is required for data signal synchronization. An internal card, provided with SM, eliminates the need for the null-modem clock. When the associated equipment at the test site and the PC are located more than 50 cable feet from each other, the interconnection is made with a 4-wire facility and a 2024 DATAPHONE† , 2048 DATAPHONE, or 208A data set. In this interconnect configuration, the null-modem clock is not required.

2.03 In general, each end of all synchronous interconnect arrangements should include at least one 2024 DATAPHONE, 2048 DATAPHONE, or 208A data set having access to local switching or DDD. In the case of null-modem arrangements, a single data set at the PC is adequate. These data sets are used to implement system flexibility features, ie, test-site reconfigurations and backup plans (see Practice 666-611-122). The data sets are also used for establishing synchronous communications over switched facilities in the event of private line facility failure.

> ***Note:*** Manual operations are required to establish both switched connections (when using the 2024 DATAPHONE, 2048 DATAPHONE, or 208A data set) for facility backup procedures and for implementation of the flexibility features of the system.

B. Communications

2.04 The synchronous data communications operate using full-duplex protocol, are software/hardware supported, and agree with EIA standards for synchronous interface channel protocol procedures. The data signals are binary-coded serial bits (0s and 1s). The data signals are transmitted at 2400

† Registered trademark of AT&T.

or 4800 bits per second (bps). The characters are in 7-bit, odd-parity, American Standard Code for Information Interchange (ASCII) code.

2.05 After completion of the PC initialization and software loading procedures (described in Practice 666-611-122), the synchronous communications are initiated and controlled by the communication subsystem manager program in the SARTS 1A generic. The communication subsystem manager program causes the PC and DATASPEED 40/4 or 4540 terminal sets associated with the TP 52As in the test site(s) to operate as a closed system. Continuous polling and selections of keyboard display and printer buffers in the DATASPEED 40/4 or 4540 terminal sets are made by the PC via the SI and the synchronous data link. The synchronous communication is shown in Fig. 4.

2.06 All keyboard entries, displays, and hard-copy data are carried by synchronous communication links. The keyboard entries are stored in buffers and displayed as they are typed. The PC polls for information in the buffers, receives contents of the buffers as input data, and selects the buffers to which it writes information that is displayed or printed as hard copy.

2.07 Interruption to the synchronous communications or a break in facility continuity is identified by software error messages at the PC control terminal (DECwriter* terminal). The PC is equipped with a telecommunications error statistics report which provides a performance summary of each synchronous line.

3. PC-TO-RTS DATA LINK (ASYNCHRONOUS)

A. Facilities

3.01 The asynchronous data facilities, between the PC and RTSs, are either private line facilities or facilities established over full-duplex (local or DDD) connections. The private line facilities are equipped with a 202T data set at each end. A processor switch (DSU-2423) is connected between the PC and the 202T data set. The telephone side of the data sets connect to the CO line circuits for both outgoing and incoming connections.

* Registered trademark of Digital Equipment Corporation.

3.02 The EIA interface jack of all data sets at the PC end of the asynchronous communication links connects, through multiplexing devices, to asynchronous ports of the PC. The PC has two asynchronous ports (AM1 and AM2). The number of asynchronous lines that can be connected to AM1 and AM2 is 16 each.

3.03 At the RTS 5A end of the asynchronous data link, each RTS is equipped with a 202T data set that can be associated with two dial-selectable CO line circuits. The RTS 5A connects the data set to one line for incoming calls from a PC and to a second line when making outgoing calls. When the RTS 5A and PC are interconnected with a private line facility and 202T data sets, the dialable number arrangement is used only for facility backup. The facility backup is software controlled and occurs automatically as a SARTS 1A function (see Practice 666-611-120).

B. Communications

3.04 The asynchronous data communications operate in full-duplex. The data signals consist of binary-coded serial bits (0s and 1s). The data signals are transmitted at 1200 bps. The data communications are software/hardware supported and are initiated by the PC. All data transmitted across the link is in 7-bit, even-parity, ASCII code.

3.05 The protocol and command/response format of the asynchronous communications are based on the master/slave relationship of the PC and the RTS control circuit (SD-1P107-01). The protocol scheme for asynchronous data exchange between the PC and the RTS control circuit basically provides the following:

(a) The PC is informed that an RTS control circuit has received a command string before the RTS control circuit processing commences.

(b) The PC is informed of the status after a command string has been executed.

3.06 The sequence of events at the RTS control circuit, during execution of the receive routine, is shown in Fig. 5. This routine begins unconditionally when the PC causes a transmission of primary data carrier that is detected as derived logic on the EIA interface by the RTS control circuit.

3.07 All commands from the PC are one of the following types:

(a) **P** commands which are associated with a particular remote test port (RTP)

(b) **X** commands which are not associated with the RTP.

3.08 All commands are transmitted in messages beginning with STX and ending with ETX. A single message may have several commands but cannot contain both **P** and **X** commands.

3.09 The following string of characters is a typical command read by an RTS control circuit in the receive routine:

STX/P3/S18230/R48962/U,C,164/R23242/R26432/R38262/R49382/ETX

Note: These can be observed with a 921A data test set, or equivalent.

3.10 The RTS control circuit would interpret the command as follows:

- **STX/** — Start of text
- **P3/** — Port 3 of RTP
- **S18230/** — SMAS access point 18230
- **R48962/** — RTS instruction code
- **U,C,164/** — Command for RTS control circuit
- **R23242/** — RTS instruction code
- **R26432/** — RTS instruction code
- **R38262/** — RTS instruction code
- **R49382/** — RTS instruction code
- **ETX** — End of text.

3.11 The following is an example of the protocol for all asynchronous data exchanges between the PC and an RTS:

- To RTS control circuit: **STX/P2/R48962/ETX**
- From RTS control circuit: **STX/R/ETX** acknowledgement (received)
- From RTS control circuit: **STX/C/ETX** execution status (complete)

3.12 A telecommunications error statistics report furnishes a performance summary of outgoing, incoming, and private lines to the RTS units.

4. INTER-PC DATA LINK (ASYNCHRONOUS)

A. Facilities

4.01 The inter-PC (PC-to-PC) data link uses asynchronous private line facilities with 202T data sets. The PC can support a maximum of five inter-PC data links.

B. Communications

4.02 These facilities connect to the PC at the AM. The inter-PC data link consists of full-duplex asynchronous data communications. These data links operate at a speed of 1200 bps. One or more testers may perform circuit testing over one inter-PC data link. Up to a maximum of 16 test access points are supported on one inter-PC link. A maximum of two inter-PC links can be established between any two PCs.

Note: A test access point is one of a possible two circuit accesses made by a tester at a TP 52A to test circuits and/or sectionalize circuit troubles.

4.03 Data describing the inter-PC data links must be recorded as part of the site dependent data (SDD) as given in Practice 666-611-122. Inter-PC SDD includes the identification of private lines and foreign PCs.

4.04 A telecommunications error statistics report summarizes the performance of the inter-PC data links.

5. DATA LINK MONITORING

5.01 The customer is able to monitor the data links interfacing the PC via digital patch unit 2400 (DPU-2400) manufactured by Spectron Corporation, or equivalent. This unit furnishes a monitor jack that allows the connection of a data line monitor. The data

line monitor is used to assist in sectionalizing data link troubles between the PC and its interfacing systems.

5.02 The data line monitor should be equipped with at least the following features:

- Synchronous/asynchronous operation from 50 to 9.6K baud
- ASCII character set
- Recording capability
- Character width selection
- Framing character selection
- Video display (400 characters minimum)
- Variable playback speed for both synchronous and asynchronous recordings (from 50 to 9.6K baud)
- EIA lead connection display.

6. TELEPHONE CONNECTIONS (TEST SITE AND RTS)

6.01 Each RTP (SD-1P108-01) in an RTS is assigned and cross-connected to two originate-only CO line circuits. One line circuit is used by the RTS to complete a TSV connection whenever a SARTS 1A access is made. The TSV connection is ordered by the PC as a part of the instructions to an RTS. This connection is automatically established by the RTS between the RTP and one of two test lines appearing on a test line telephone console located at the TP 52A requesting the access.

6.02 The other CO line circuit, connected to an RTP, is used by the RTS to complete a connection for talking whenever a tester makes a request after a circuit has been accessed. This connection is established by the RTS to the same TP 52A terminating the TSV connection.

6.03 The test site ends of the telephone connections, originated by the RTSs, are CO line circuits that terminate in the test line control circuits (SD-1P009-01). When both connections have been established, the RTP and the test line control circuit are interconnected on a 4-wire basis. The telephone connections between the RTP and the test line telephone console, for both TSV and talk features, are shown in Fig. 6.

7. OVERVIEW OF SARTS 1A COMMUNICATIONS

7.01 The communications that take place within the SARTS 1A is shown in Fig. 7. An example of the typical asynchronous data communications between a near end and the far ends in CO1 and CO2 is shown. These communications permit the testing of the special service circuit shown in each CO.

7.02 As shown in Fig. 7, one asynchronous data link connects the PC to each far end. The data link to CO1 is switched, and the data link to CO2 is a private line. The far-end equipment interfaces the data link at the RTS control circuit, and the near-end equipment interfaces the data link at the AMs. The CO switching and switched message network trunks are used for the switched lines.

7.03 In Fig. 7, a DDD asynchronous outgoing line has been set up to CO1. The outgoing line is required only briefly to allow the RTS to identify the calling PC. Then, the far-end data set is connected to another line, thus disconnecting the original call from the PC. The far-end equipment calls the PC via a hunt group line arrangement and establishes an asynchronous data link. The PC maintains this incoming connection throughout the testing of the special service circuit. Based on this call relationship, fewer outgoing lines than incoming lines are required by the PC.

7.04 In Fig. 7, the data link to CO2 has been established via a private line. A private line, in addition to being economical for heavy near-end to far-end traffic, permits faster access time because the callup-callback sequence is bypassed. A CO line and data set still must be furnished at the far end (CO2) for backup purposes.

7.05 In addition to the data communications, CO line equipment for the TSV and talk lines to each TP 52A must also be furnished. Four lines are required for each TP 52A. Two lines are required for each RTP in each far end. An RTP in each of the two COs is shown with a TSV line connection established. A TSV line is always required when a special service circuit access is made. The TSV connection allows the tester to make a listen test before beginning circuit tests. The talk line connection, shown connected to

the RTP in CO1, is established at the discretion of the tester and requires a separate test command.

8. SARTS 1A/DACS INTERFACE

8.01 An interface between SARTS 1A and DACS is furnished to allow SARTS 1A to access and test channels in T1 carrier lines via DACS. The interface between SARTS 1A and DACS is furnished via two links. The two links are the test access link and the data communication link (Fig. 8).

8.02 The test access link is furnished via the digital test access connector (DTAC) which performs the ***maintenance connector*** function to allow the SMAS of SARTS 1A to make the connection to DACS. For more information on the operation of the DTAC, refer to Practice 667-303-112.

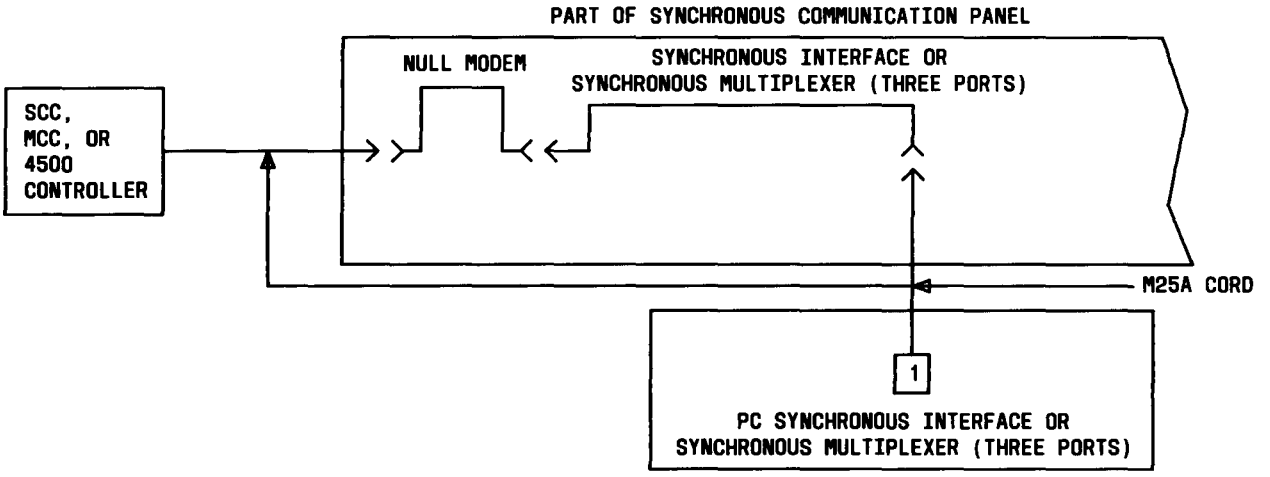
8.03 The data communication link is furnished via an enhancement to the SARTS 1A RTS controller. This enhancement consists of the data link module (DLM) and the data link interface (DLI), and it connects the RTS controller to an administrative port on the DACS frame. This enhancement allows the RTS to support communication links for a maximum of eight separate DACS frames.

A. Facilities

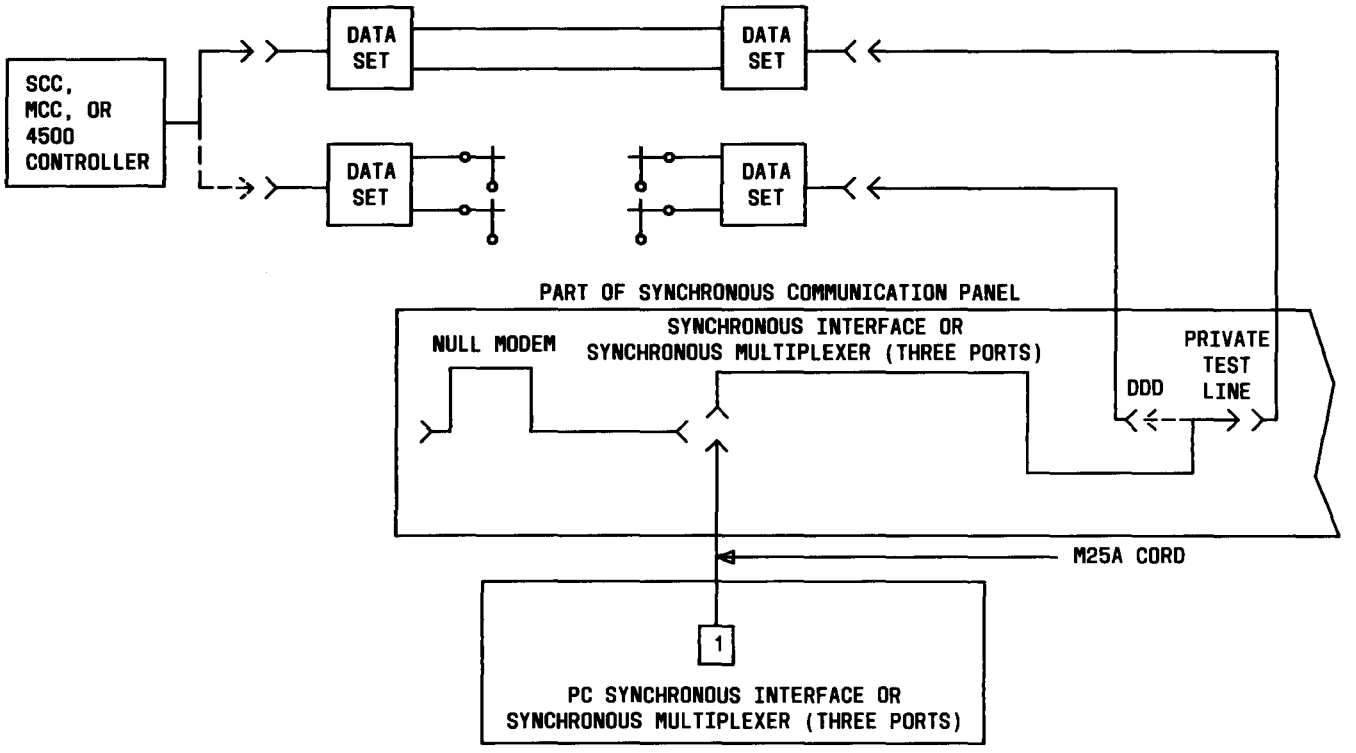
8.04 The asynchronous data facility between the RTS controller and the DACS administrative port is a full-duplex, 1800-bps data link using the RS 449 format. This link may be a direct cabling connection or a private line facility. This data link may be up to 2000 cable feet (M37B cable) before data sets are required. The private line data link uses 202T data sets.

B. Communications

8.05 The asynchronous data communications link protocol is the Snider protocol which supports half-duplex (using full-duplex facilities), asynchronous communications using ASCII characters with even parity.

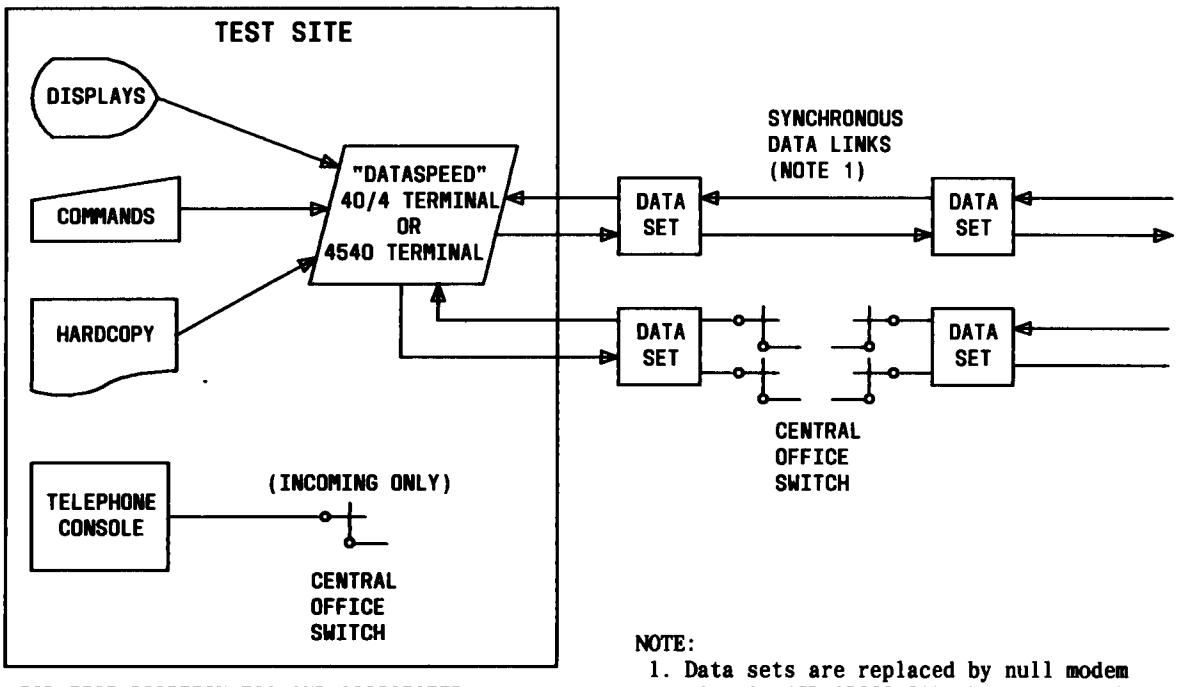


(a) ARRANGEMENT WITH NULL MODEM



(b) ARRANGEMENT WITH PRIVATE LINE

Fig. 1—PC Synchronous Data Interconnect Arrangements



FOR TEST POSITION 52A AND ASSOCIATED EQUIPMENT, REFER TO PRACTICE 666-612-100.

NOTE:
1. Data sets are replaced by null modem circuit (SD-1P000-01) when data link is 50 cable feet or less.

Fig. 2—SARTS 1A Interconnection (Sheet 1 of 2)

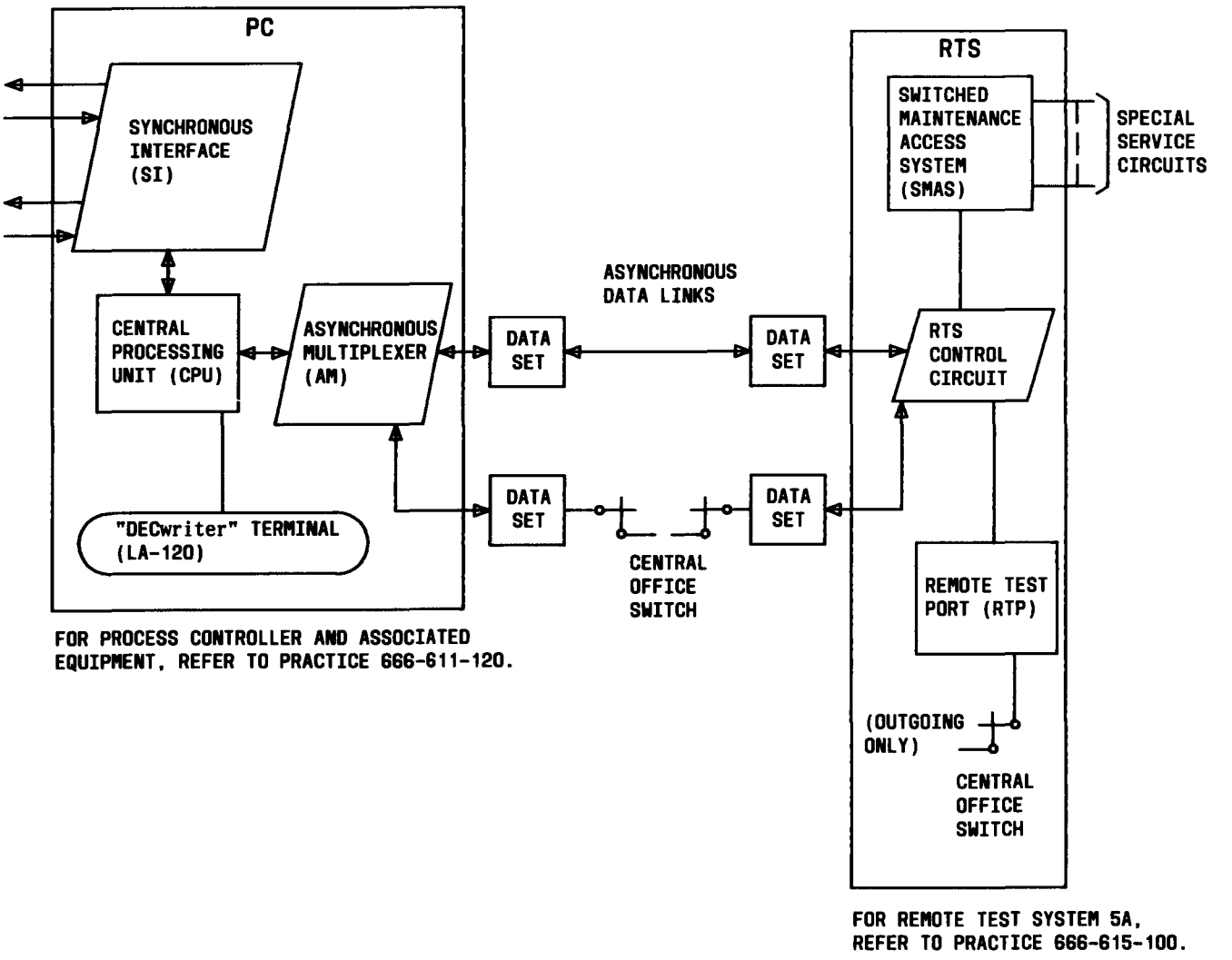
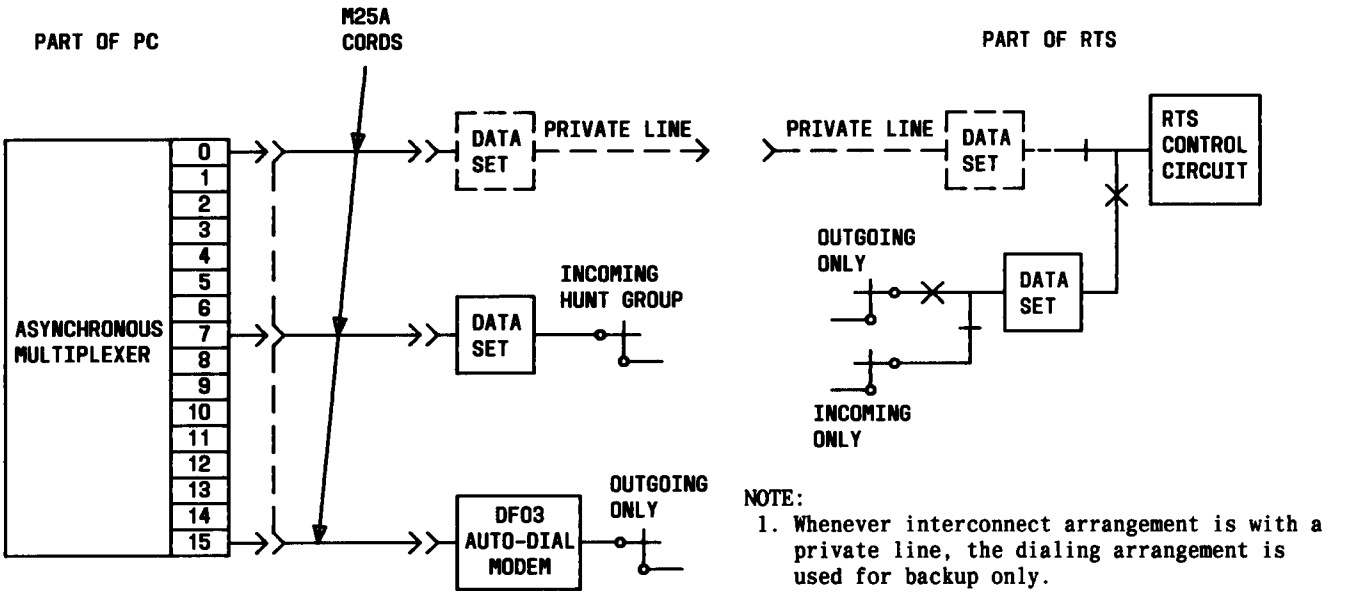
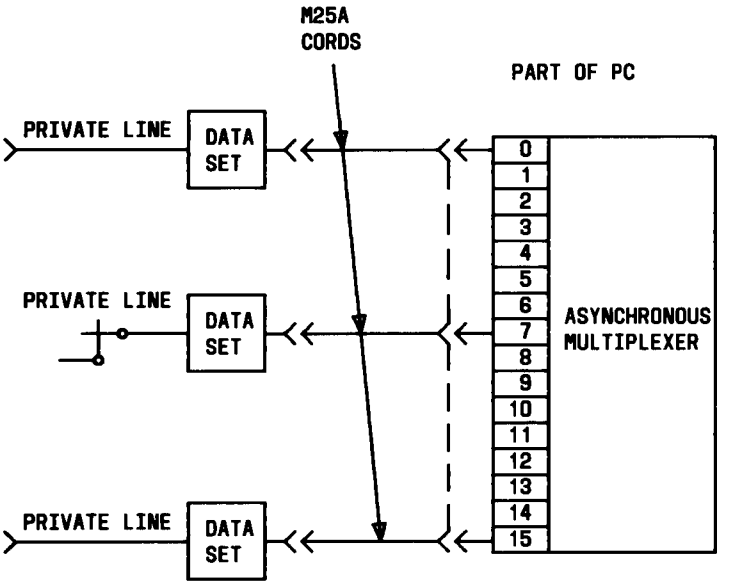


Fig. 2—SARTS 1A Interconnection (Sheet 2 of 2)



NOTE:
1. Whenever interconnect arrangement is with a private line, the dialing arrangement is used for backup only.

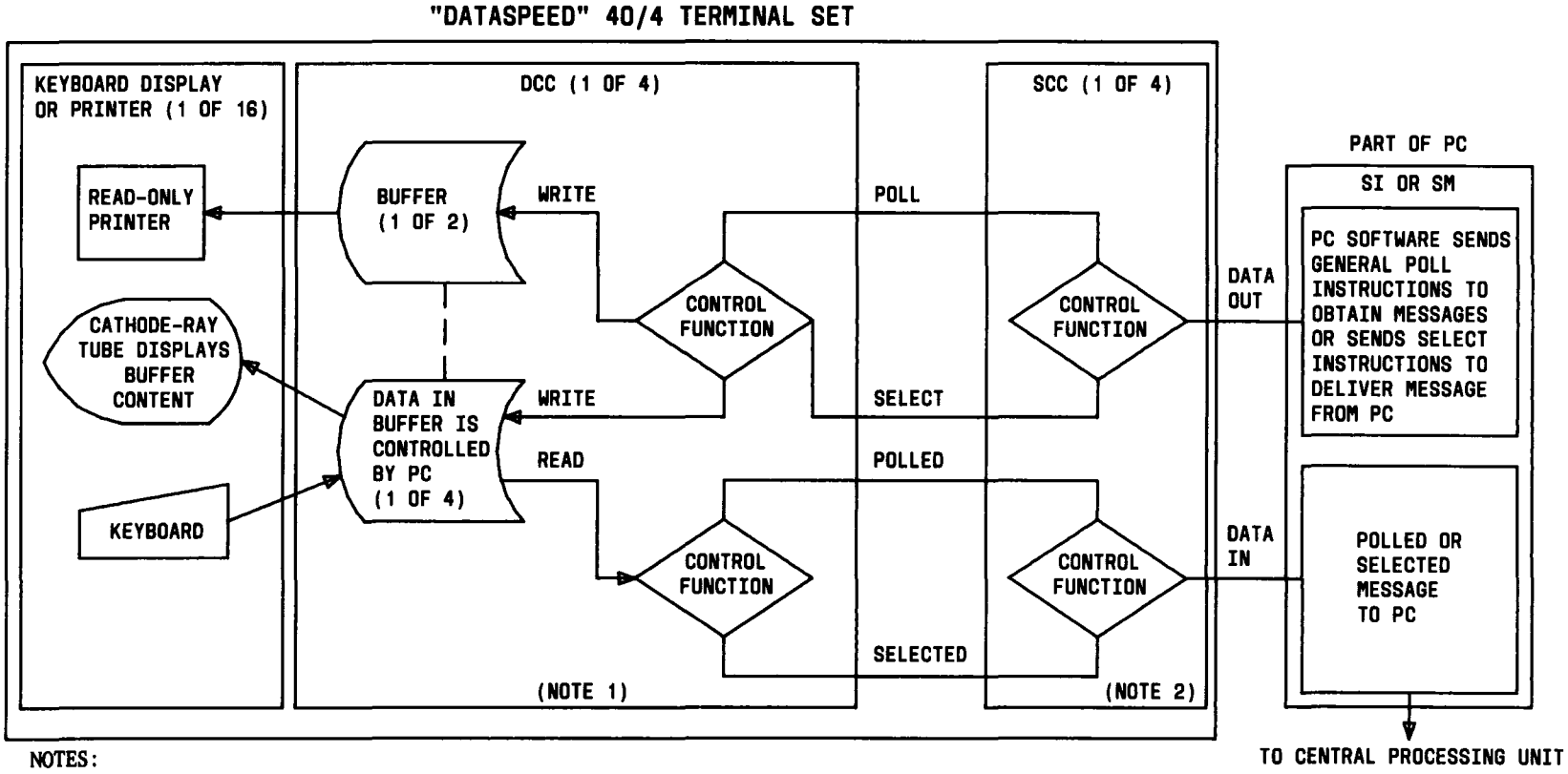
(a) PC-TO-RTS ARRANGEMENT (NOTE 1)



NOTE:
2. Inter-PC interconnect arrangement is private line only.

(b) INTER-PC ARRANGEMENT (NOTE 2)

Fig. 3—Asynchronous Data Interconnect Arrangements



NOTES:
1. Each DCC has 4 buffers for controlling 4 KDs and 4 printers.
2. The SCC controls a maximum of 6 DCCs. A maximum of 4 SCCs may be connected to a PC with a maximum of 24 KDs supported by 1 PC.

Fig. 4—Synchronous Communications

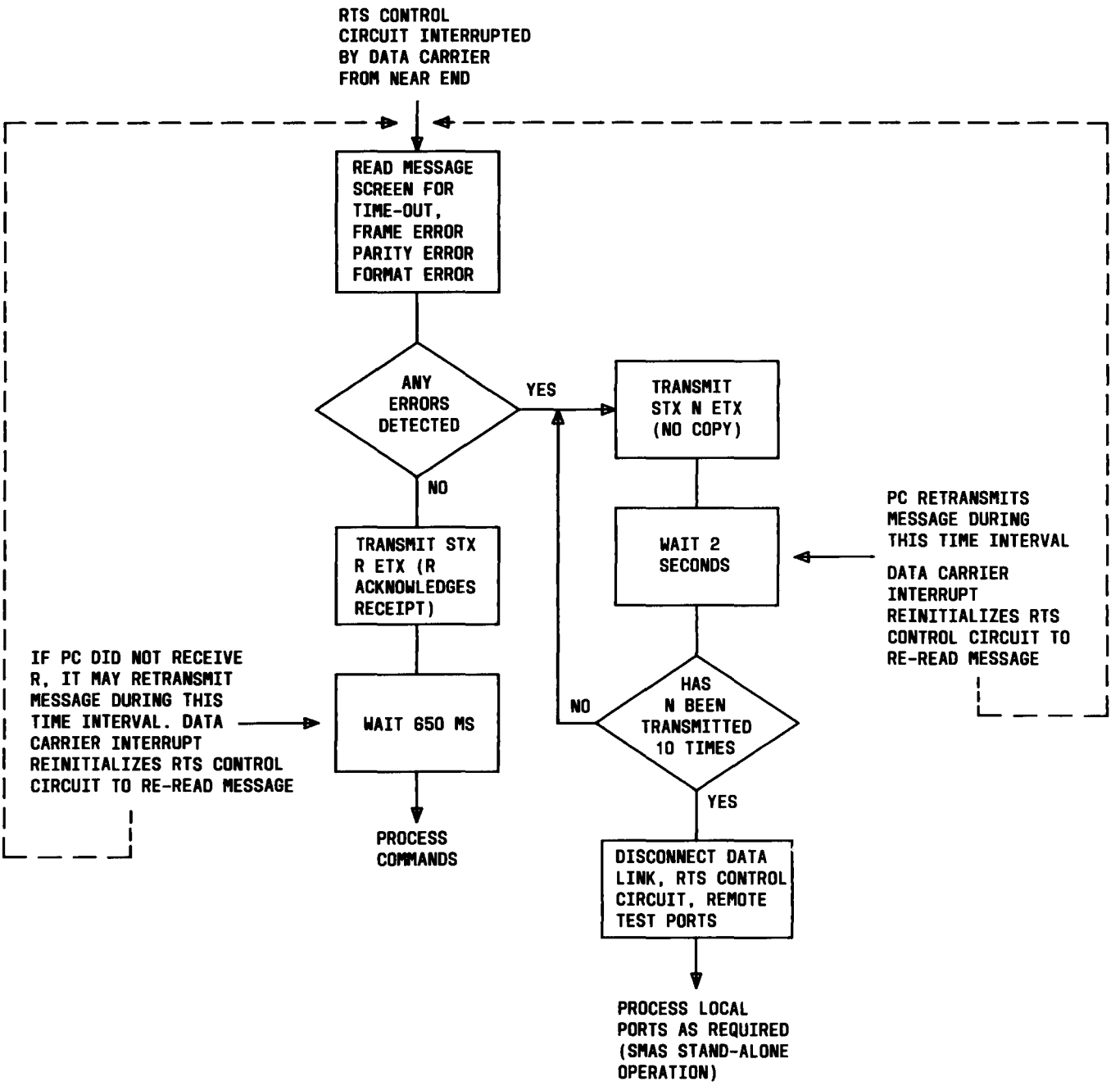


Fig. 5—Receipt of Near-End Message by Far End

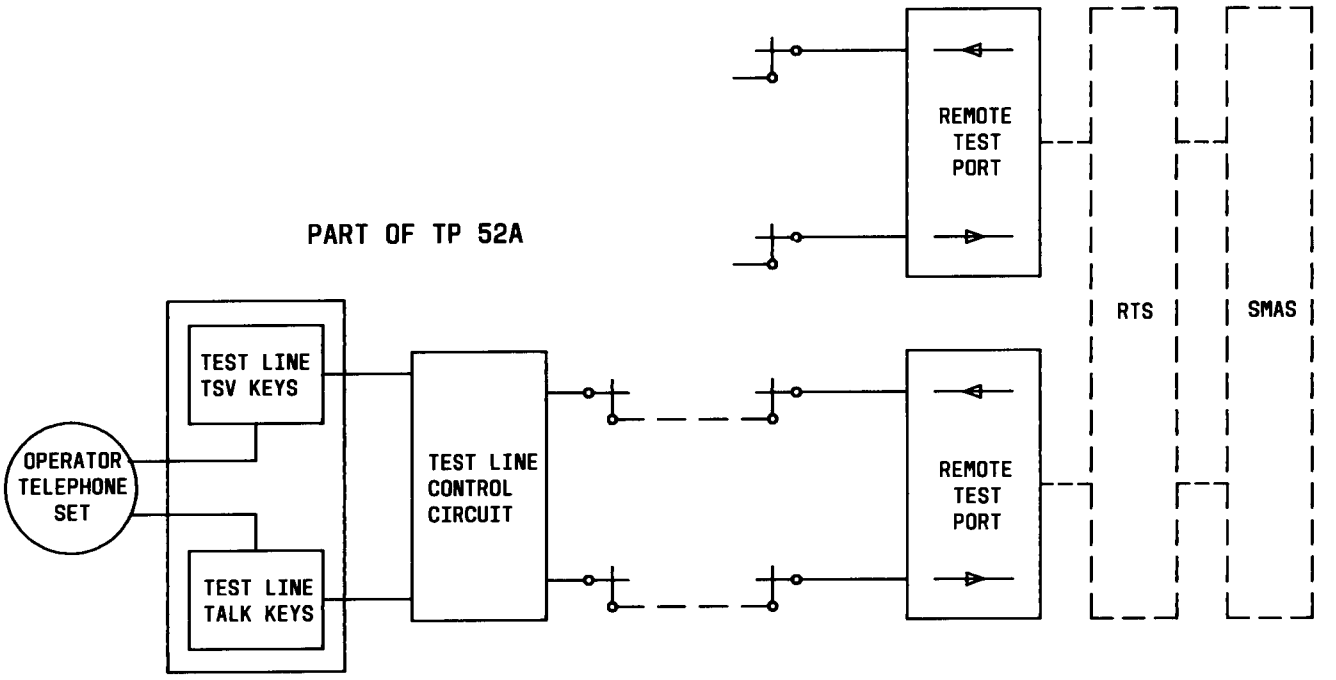


Fig. 6—Talk and Test Status Verify Telephone Connections Established by RTS to TP 52A

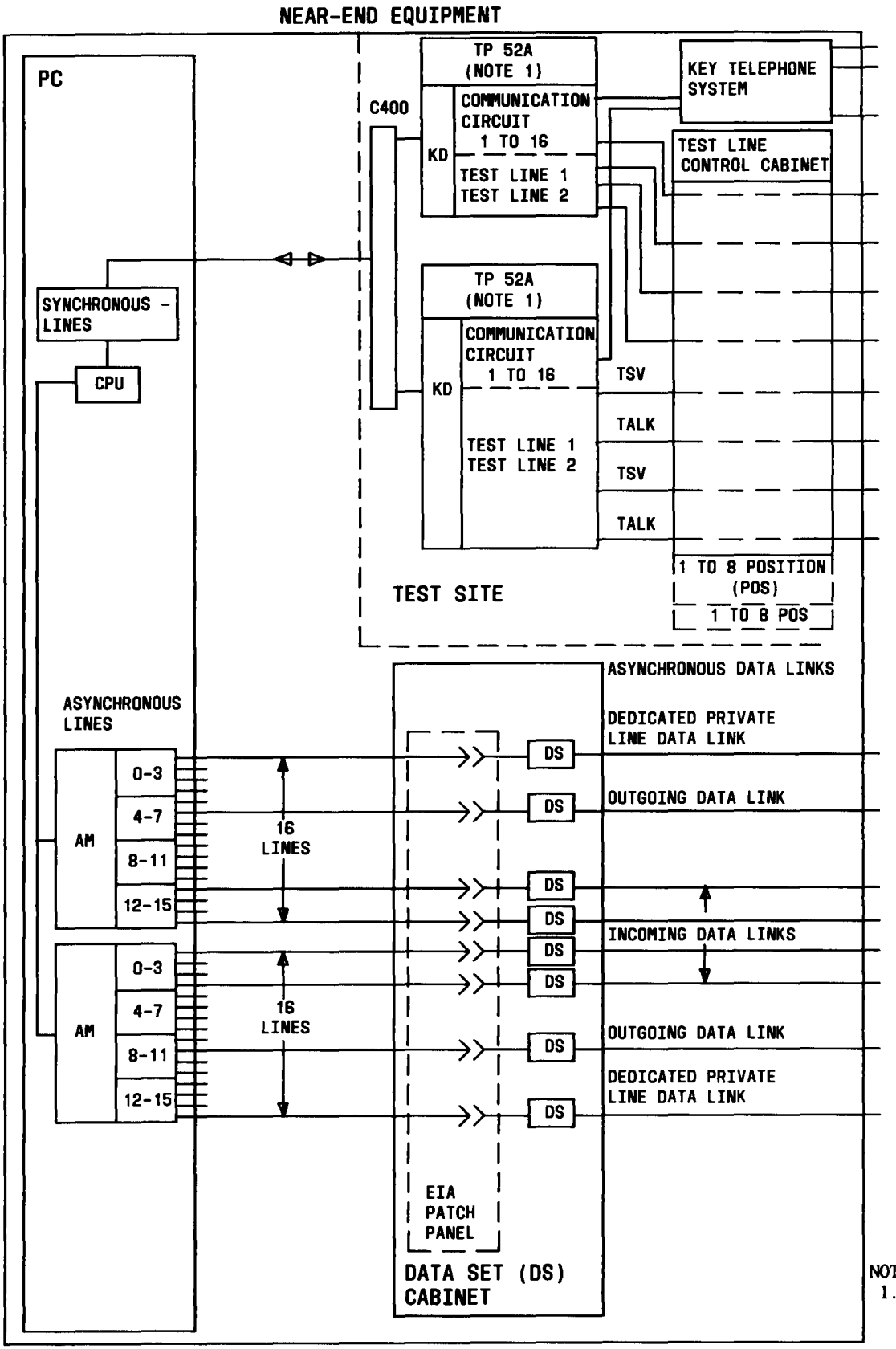


Fig. 7—Overview of SARTS 1A Communication (Sheet 1 of 2)

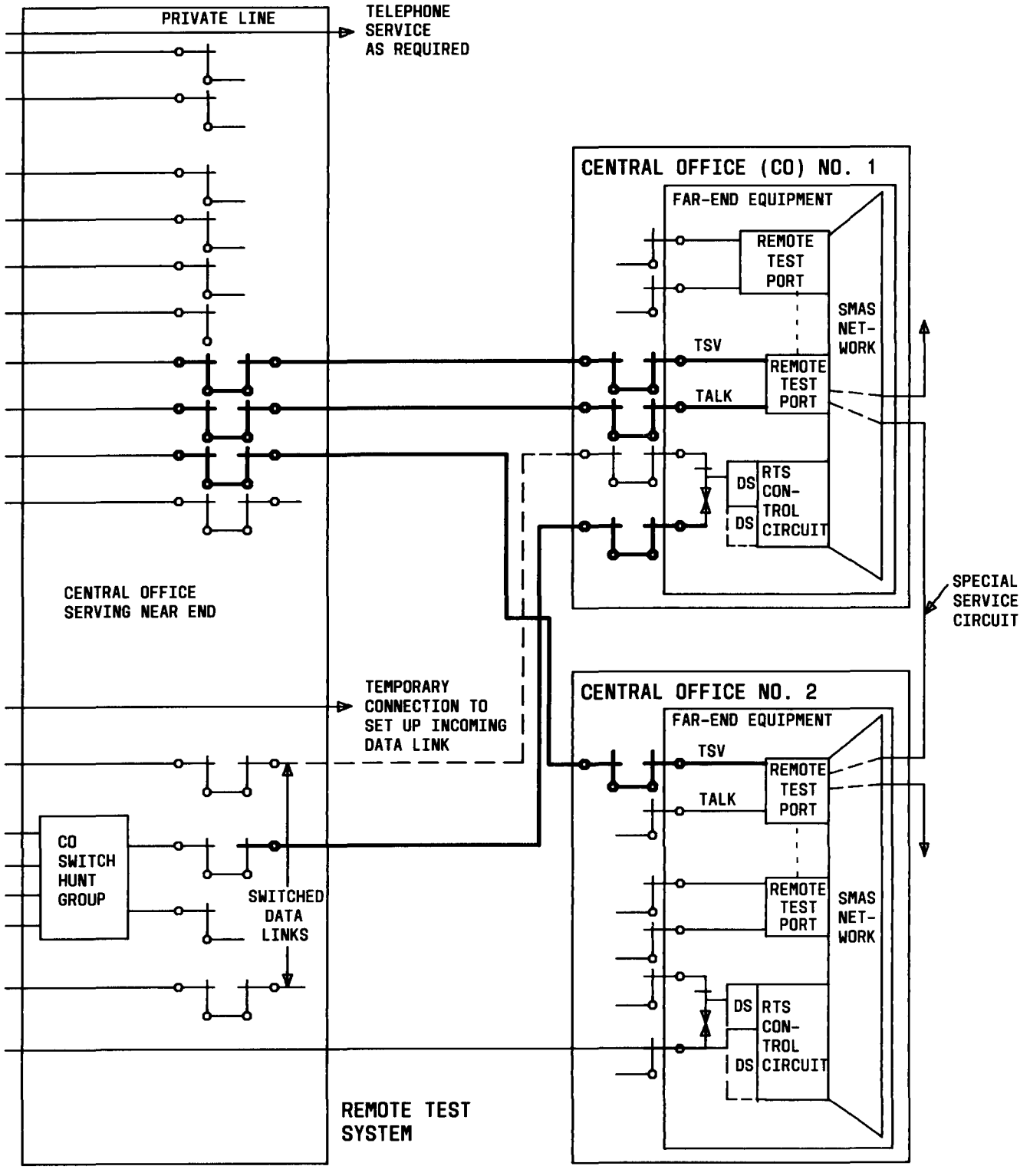


Fig. 7—Overview of SARTS 1A Communication (Sheet 2 of 2)

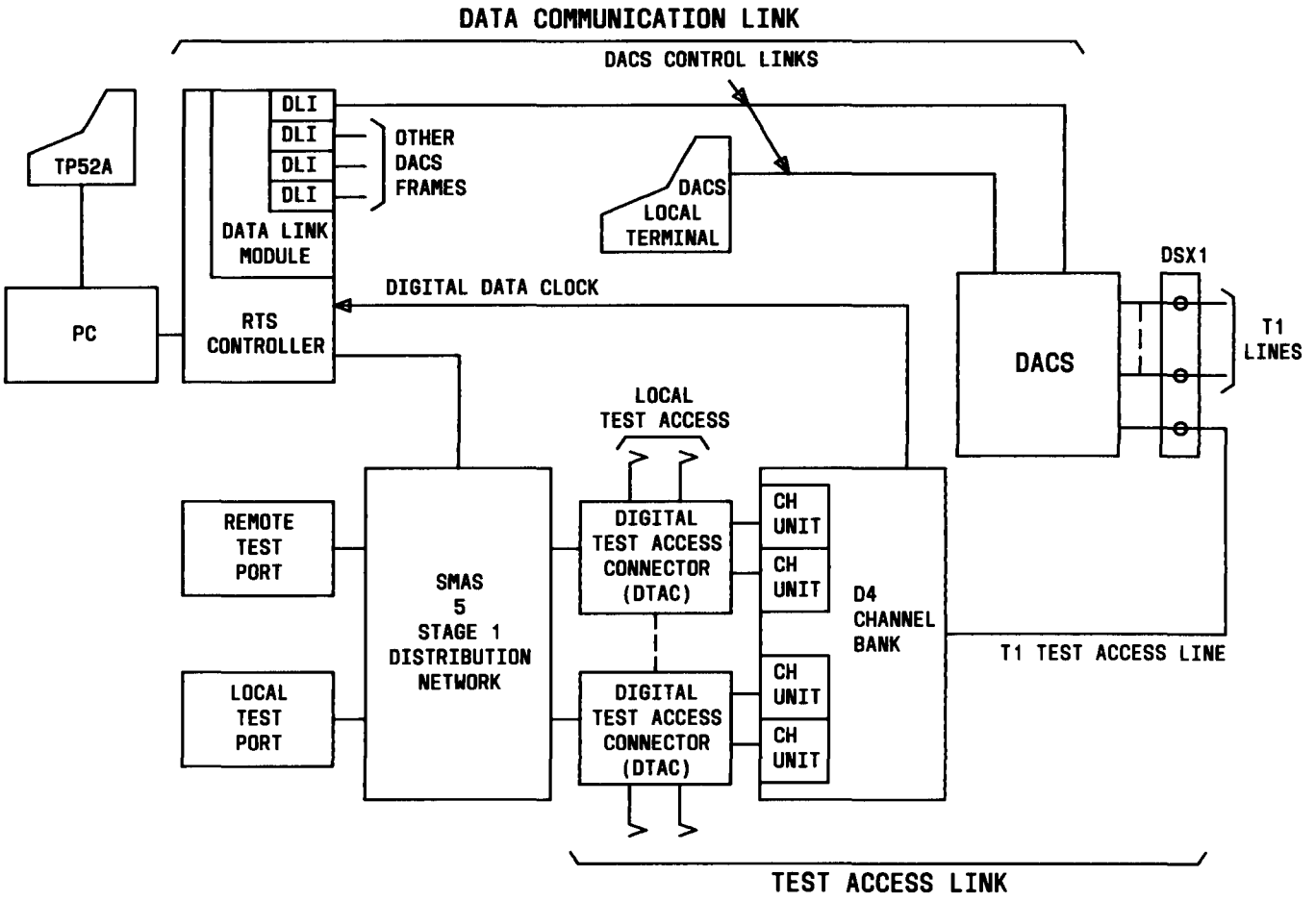


Fig. 8—SARTS 1A/DACS Interface