SWITCHED ACCESS REMOTE TEST SYSTEM (SARTS-1A)

REMOTE TEST SYSTEM 1A (RTS-1A)

TESTS

CONTENTS PAGE

1. GENERAL

1.01 This section gives the test procedures for the Remote Test System 1A (RTS-1A) which is located at the far-end of the Switched Access Remote Test System 1A (SARTS-1A).

1.02 Whenever this section is reissued the reason(s) for reissue will be given in this paragraph.

1.03 The test procedures are for the Far-End Control Circuit (FECC) (Fig. 1), the Test Function Control Circuit (TFCC) (Fig. 2), the RTS-1A controller, the Remote Access Test Port (RATP), and the Test Register and Outpulsing Circuit (TROP).

1.04 Each individual circuit pack (CP) in the FECC and TFCC has been assigned a unique designation, consisting of the character X followed by a 2-digit number. Table A for the FECC and Table H for the TFCC give a cross-reference of the unique designation to the physical location, CP number, ED code number, and functional designation of each CP. Throughout this section, each CP is identified by this unique designation. This technique is used to minimize the number of changes to be made in the section. If, for example, the physical location of a CP in the FECC should change, then only Table A would need revision.

2. TEST EQUIPMENT REQUIRED

2.01 The following equipment is required for testing the FECC and TFCC:

- 1—Far-End Maintenance Test Circuit (SD 99786-01; J99359U, L7), consisting of

  1—Program Counter—CP16 (SD-1P012-01) (Fig. 3)

  1—Test Card—CP17 (SD-1P012-01), (Fig. 4)

  2—INPUT TEST PLUGS [ED-2C433-( ), GR1]

  1—I/O TEST CABLE [ED-2C433-( ), GR2]

  1—MISC TEST PLUG [ED-2C433-( ), GR3]

- 1—Multimeter KS-14510-L1 (or equivalent)
- 2—Clip Leads (each at least 3 feet long)
- 1—Timing Device, capable of measuring an interval of 95 to 220 seconds with an accuracy of 10 seconds (a wall clock or wristwatch with a second hand).

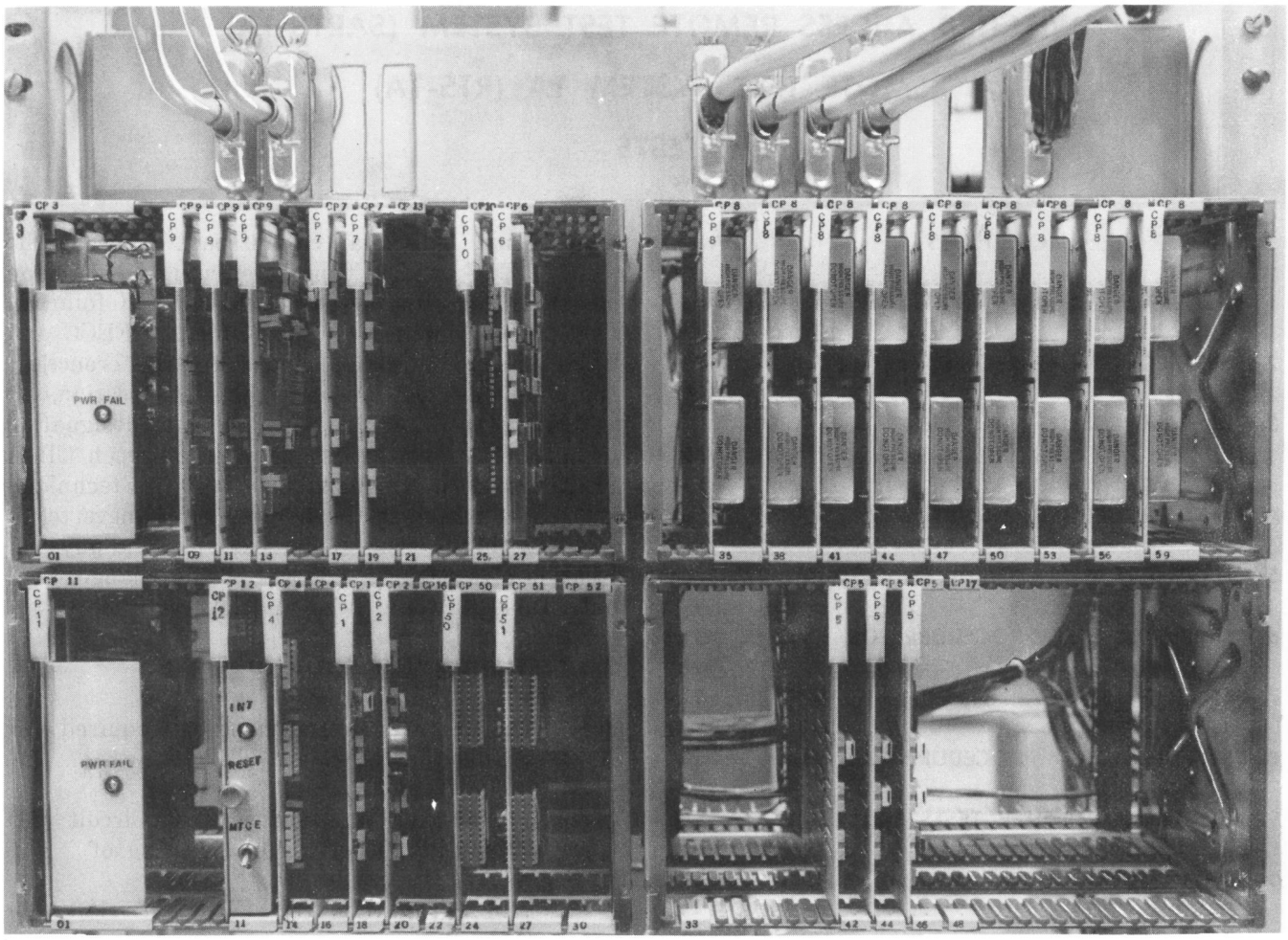


Fig. 1—Far-End Control Circuit

3. DESCRIPTION OF EQUIPMENT AND TESTS

3.01 The following paragraphs are a brief description of CP16 and CP17 and the tests covered in this section. This will give the tester a better understanding of the system and better equip the tester to handle any failures which might occur.

3.02 The Program Counter, CP16, displays the logic states of the memory and Input-Output (I/O) address leads generated by the Central Processor Unit (CPU). The state of each of these 21 address leads is displayed visually with a unique light-emitting diode (LED). CP16 is used to verify the integrity of the address leads in the test sequence.

3.03 The Test Card, CP17, permits the selection of various tests via three thumbwheel switches and displays the test results on four 7-segment LEDs. The setting of the thumbwheel switches determines where the stored program in the CPU starts when an interrupt signal is applied. An interrupt signal is generated by the TEST pushbutton being momentarily depressed. The test result is then either displayed on the TEST RESULTS LEDs, lamps lit on CP16, or voltages brought to defined levels at test points within the circuit. The first six tests of both the FECC and the TFCC are performed by using the left-hand thumbwheel switch settings (0XX through 5XX). Additional tests are available by setting the left-hand thumbwheel switch to 6 and operating the two right-hand switches. The SUBTEST VERIFICATION LEDs duplicate the two right-hand switch settings to add assurance

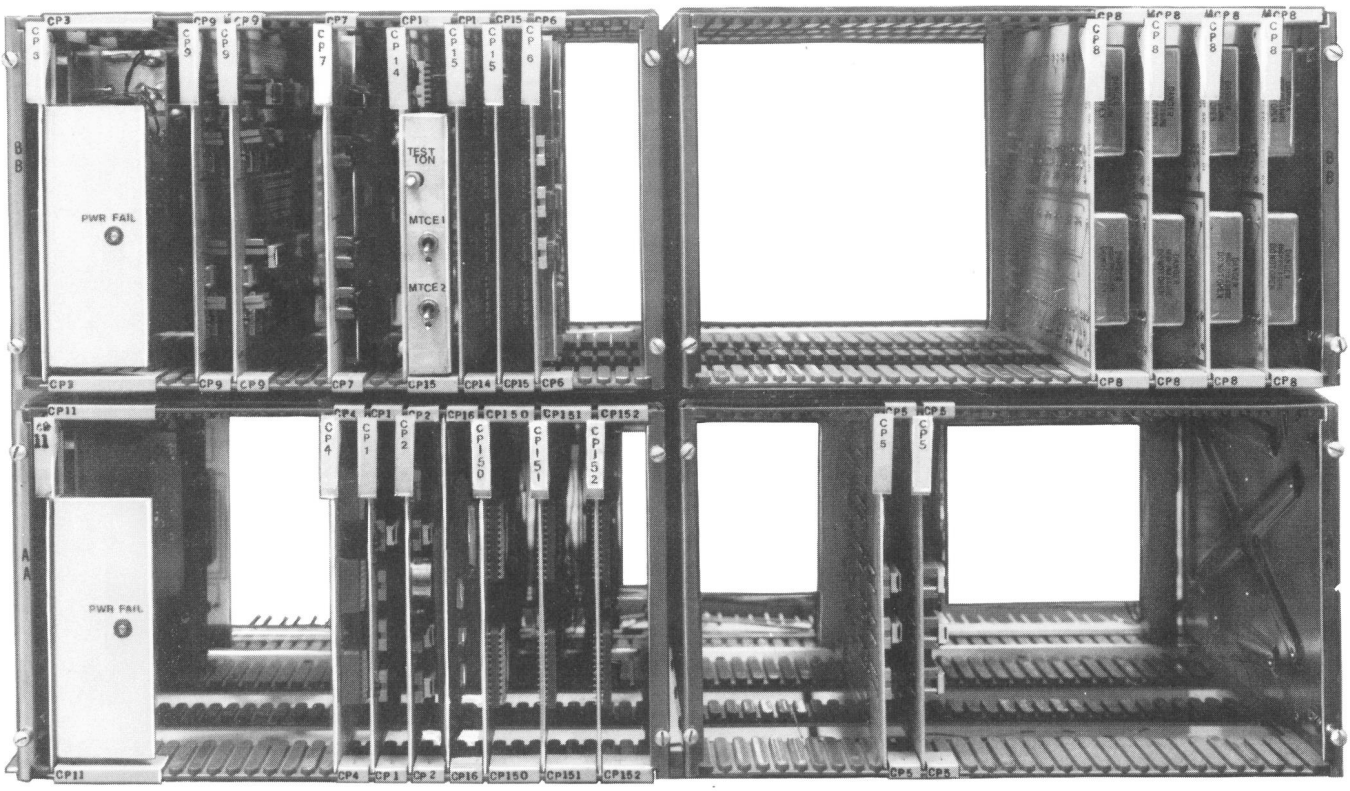


Fig. 2—Test Function Control Circuit

to the tester that the system is performing the requested test. These SUBTEST VERIFICATION numerals are blanked for test codes 0XX through 5XX.

3.04 The purpose of the Power Test is to ensure that the dc voltage sources and distribution within the FECC and TFCC are within the proper range. Test failure may be the result of excessive loading by one or more CPs, a defective power converter, or wiring problems. It should be noted that if a voltage reading is less than one volt, the malfunction is probably being caused by excessive loading on the converters. If the voltage reading is slightly high or low, the converter is probably defective.

3.05 The purpose of the Address Bit Check (both zero and one state) is to monitor the 21 address leads and ensure that they function properly to provide necessary addressing of the memory and I/O CPs.

3.06 The purpose of the ROM Check Sum tests is to test the circuit pack(s) containing the Read Only Memory (ROM).

3.07 During normal operations of the FECC and TFCC, loop opens and loop closures are applied to the Input Buffer CPs and read by the Input circuit packs. The purpose of the Input Test (both open and closed) is to apply dummy opens and dummy closures to the Input Buffers and establish the ability of the CPU to detect and decode the loop opens as logic zeroes and the loop closures as logic ones.

3.08 The purpose of the Output Loopback tests is to make sure that the FECC and TFCC provide output loop opens and output loop closures to the connecting circuits.

3.09 The purpose of the RAM Tests is to verify the integrity of the Random Access Memory (RAM) CPs. This is accomplished by sequentially

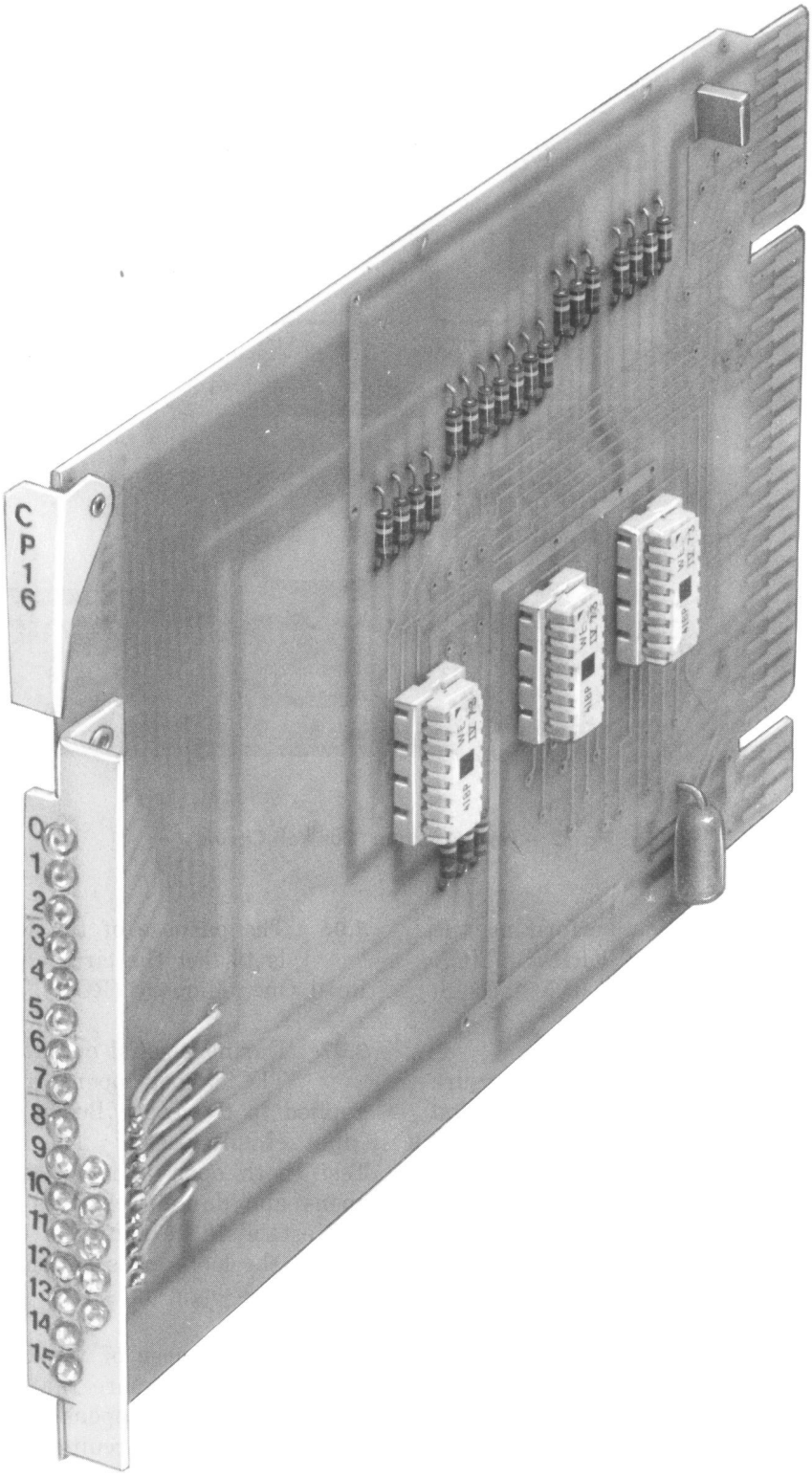


Fig. 3—Faceplate of Program Counter (CP16)

Fig. 4—Faceplate of Test Card (CP17)

writing data into the RAM and then reading the data and verifying that the two match.

3.10 The far-end ID, SMAS capacity, and Port Type tests of the FECC and the DDD Number test of the TFCC are to verify that the rocker switch settings on the CPs are encoded and function properly. The far-end ID is the identity number which is assigned to the far-end being tested and which is encoded in CP10 of the

FECC. The SMAS capacity is the highest assigned connector group number of that far-end, and is encoded in CP10 of the FECC. The Port Type is those crossbar levels to which the RATPs have been assigned and is encoded in CP10 of the FECC. The DDD number is the primary and alternate number and mode of dialing used by the RTS-1A to call back the near-end; this number is encoded in CP15 of the TFCC.

3.11 The purpose of the EIA Input and Output Tests of the FECC and TFCC is to verify that the proper voltage levels are generated and decoded. These voltage levels are required for interfacing with data sets and the remote test meters and for FECC/TFCC intercommunication.

3.12 The purpose of the Interrupt Test is to verify that the Interrupt Circuitry of the FECC and TFCC is functioning. For example, verification is made that the FECC is interrupted by signals from the data set when ringing or primary data carrier is present.

3.13 The purpose of the Ringing Timer tests is to verify the proper operation of various relays and the thermal timer in the TFCC.

4. TEST PROCEDURE

4.01 In most tests of the FECC and TFCC, the problem is isolated to three or fewer CPs. The tester then uses successive replacement of the packs until the test is passed. The tester should then attempt to establish which pack or packs are not defective by successive elimination. For example, assume a test fails and CPs X27, X35, and X51 are identified as the probable causes. The tester replaces X27 and repeats the test, and again the test fails. Leaving the new X27 in place, the tester replaces X35 and repeats the test, and again the test fails. Leaving both the new X27 and X35 in place, the tester replaces X51 and repeats the test. This time the test passes. Obviously X51 was defective. Leaving the new X35 and X51 in place, the tester replaces X27 with the old CP and repeats the test and it passes. With the old X27 and new X51 in place, the tester replaces X35 with the old CP and repeats the test and the test fails. This indicates CP X35 and X51 were defective and CP X27 was not.

4.02 If, at any time during the test procedures for either the FECC or the TFCC, the defective CP is isolated and the trouble corrected, testing may be halted and the circuit returned to normal operation. This is done by removing all test equipment and reconnecting the system cables. In the FECC tests, the RESET pushbutton should also be momentarily depressed.

> ***Note:*** Do not store CP16 and CP17 in the FECC or TFCC during normal operation.

5. FECC TESTS

5.01 The step procedures in this part of the section isolate a defective CP in the FECC. The steps must be performed in order, and the tester should not proceed to the next step until the previous step has been successfully completed. If any test cannot be successfully completed, even with the corrective action described (for example, see Step 22), the intra-unit wiring (wiring between CPs) is the probable cause of trouble. If the intra-unit wiring is to be checked for opens, shorts, grounds, etc, on the FECC at any time during the tests, it is necessary to return to Step 1 and start again.

5.02 The tests and the first step in each test are as follows:

Step 1	A. Power Tests
Step 5	B. Address Bit Check (zero state)
Step 16	C. Address Bit Check (one state)
Step 23	D. ROM 1 Check Sum
Step 30	E. Input Test (open)
Step 36	F. Input Test (closed)
Step 44	G. Output Loopback Test
Step 70	H. ROM 2 Check Sum
Step 76	I. ROM 3 Check Sum
Step 80	J. RAM Test
Step 87	K. Far-End ID Test
Step 93	L. SMAS Capacity Test
Step 99	M. Port Type Test

Step 111	N. EIA Input Test
Step 124	O. EIA Output Test
Step 136	P. Interrupt Test

5.03 Before the following tests are performed, all system cables are to be disconnected from the FECC [all PA ( ), all PB ( ), and PMISC on front of unit and the PEIA1 and PEIA2 on rear of unit].

STEP	PROCEDURE

A. Power Tests

1 Observe PWR FAIL LEDs on CPs X90 and X91 (see Table A). Verify that PWR FAIL LEDS are off.

2 If PWR FAIL LEDs are ***off***, proceed to Step 5. If LEDs are ***on***, proceed to next step.

3 Using a multimeter, measure dc voltage on CPs X90 and X91 (SD-99623). Verify that limits are met as indicated below:

+5—between 4.75V and 5.25V

-9—between -9.4V and -8.6V

+12—between 10.8V and 13.2V

-12—between -13.2V and -10.8V

Note: Variations from these limits may be caused by the malfunction of CPs X90 or X91 or by excessive loading on power converters by a malfunctioning circuit pack.

4 If above limits cannot be met, replace CPs as required and repeat Steps 1 and 2.

TABLE A

CROSS REFERENCE OF CIRCUIT PACK TROUBLE IDENTIFICATION CODES AND THE ASSOCIATED CIRCUIT PACK FAR-END CONTROL CIRCUIT

CIRCUIT PACK TROUBLE SHOOTING IDENTIFICATION CODE	PHYSICAL LOCATION	CIRCUIT PACK NUMBER	ED CODE NUMBER	FUNCTIONAL DESIGNATION
X00	AA18	CP1	ED-1P220-( )	CPU 1
X01	AA20	CP2	ED-1P221-( )	CPU 2
X10	AA24	CP50	ED-2C379-( )	ROM 1
X11	AA27	CP51	ED-2C380-( )	ROM 2
X12	AA30	CP52	ED-2C381-( )	ROM 3
X20 (see Note)	AA14	CP4	ED-1P223-( )	RAM 1
X21 (see Note)	AA16	CP4	ED-1P223-( )	RAM 2
X22	AA14	CP18B	ED-1P393-( )	SRAM 1
X25	AA11	CP12	ED-1P238-( )	INT
X26	BB25	CP10	ED-1P229-( )	DST
X27	BB21	CP13	ED-1P239-( )	EIA
X30	AA42	CP5	ED-1P224-( )	ALT 1
X31	AA44	CP5	ED-1P224-( )	ALT 2
X32	AA46	CP5	ED-1P224-( )	ALT 3
X35	BB27	CP6	ED-1P225-( )	LT 1
X40	BB35	CP8	ED-1P227-( )	PR 01
X41	BB38	CP8	ED-1P227-( )	PR 23
X42	BB41	CP8	ED-1P227-( )	PR 45
X43	BB44	CP8	ED-1P227-( )	PR 67
X44	BB47	CP8	ED-1P227-( )	PR 89
X45	BB50	CP8	ED-1P227-( )	CMR
X46	BB53	CP8	ED-1P227-( )	ADRR
X47	BB56	CP8	ED-1P227-( )	RMTR
X48	BB59	CP8	ED-1P227-( )	TDR
X50	BB17	CP7	ED-1P226-( )	IN 1
X51	BB19	CP7	ED-1P226-( )	IN 2
X60	BB09	CP9	ED-1P228-( )	BUFF 04
X61	BB11	CP9	ED-1P228-( )	BUFF 59
X62	BB13	CP9	ED-1P228-( )	BUFF 1
X90	AA01	CP11	ED-1P230-( )	9V
X91	BB01	CP3	ED-1P222-( )	5V

Note: If FECC is equipped with X22 it will not be equipped with X20 or X21.

STEP	PROCEDURE
	B. Address Bit Check (Zero State)
5	Insert Program Counter [CP16, ED-1P265-( )] and Test Card [CP17, ED-1P378-( )] into the FECC at the physical locations identified on the unit.
6	Place MTCE switch on CP X25 to maintenance position.
7	Using front panel toggle switch on CP17, set power to ON.
8	Set thumbwheel switch to 000.
9	Momentarily depress TEST pushbutton. Verify that all red LEDs on CP16 are ***off*** and all green LEDs are ***on.***
10	If proper results are obtained in Step 9, proceed to Step 16. If proper results are not obtained, proceed to next step.
11	Replace CP X00 and repeat Steps 9 and 10. If proper results are not obtained, proceed to next step.
12	Replace CP X01 and repeat Steps 9 and 10. If proper results are not obtained, proceed to next step.
13	Remove CPs X20, X21, X30, X31, X32, X35, X50, X51, X12, X11 and X10 in that order, repeating Step 9 after each removal. When proper results are obtained, replace the last CP removed, reinsert the other CPs, and repeat Steps 9 and 10.
14	If all CPs have been removed in Step 13 and proper results are not obtained, reinsert CPs, replace CP X25, and repeat Steps 9 and 10.
15	If proper results are still not obtained and Step 3 has not been performed, it should be performed at this time. If Step 3 has been performed, intra-unit wiring is the probable cause of trouble.

STEP	PROCEDURE
	C. Address Bit Check (One State)
16	Set thumbwheel switches on CP17 to 100.
17	Momentarily depress TEST pushbutton. Verify that all red LEDs on CP16, except 14 and 15, are ***on*** and all green LEDs are ***off.***
18	If proper results are obtained in Step 17, proceed to Step 23. If proper results are not obtained, proceed to next step.
19	Replace CP X00 and repeat Steps 17 and 18. If proper results are not obtained, proceed to next step.
20	Replace CP X01 and repeat Steps 17 and 18. If proper results are not obtained, proceed to next step.
21	Remove CP X20, X21, X30, X31, X32, X35, X50, X51, X12, and X11 in that order, repeating Steps 17 and 18 after each removal. When proper results are obtained, replace the last CP removed, reinsert the other CPs, and repeat Steps 17 and 18.
22	If all CPs mentioned in Step 21 have been removed and proper results are not obtained, reinsert all CPs, replace CP X10, and repeat Steps 17 and 18.
	D. ROM 1 Check Sum
23	Remove the Program Counter CP 16 from the FECC.
24	Set thumbwheel switches to 200.
25	Momentarily depress TEST pushbutton. Verify that numbers appearing on the TEST RESULTS LEDs on CP 17 agree with the numbers appearing on the check sum label on CP X10. ***Note:*** The TEST RESULTS LEDs will have a leading zero (example, 0124) which does not appear on the check sum label (example, 124).
26	If proper results are obtained in Step 25, proceed to Step 30. If proper results are not obtained, proceed to next step.
27	Replace CP X10 and repeat Steps 25 and 26. If proper results are not obtained, proceed to next step.
28	Replace CP X00 and repeat Steps 25 and 26. If proper results are not obtained, proceed to next step.
29	Replace CP X01 and repeat Steps 25 and 26.

STEP	PROCEDURE
	E. Input Test (Open)
30	Set thumbwheel switches to 300.
31	Momentarily depress TEST pushbutton. Verify that numbers appearing on the TEST RESULTS LEDs are 0100.
32	If proper results are obtained in Step 31, proceed to Step 36. If proper results are not obtained, proceed to next step.
33	Observe numbers that appear on the TEST RESULTS LEDs and refer to Table B. This table cross-references the numbers that appear on the TEST RESULTS LEDs with the CPs which are probably responsible for the failure.
34	Replace the indicated CPs from Table B one at a time and repeat Steps 31 and 32 after each replacement.
35	Repeat the procedure in Step 34 until the proper result is obtained and then proceed to Step 36.
	F. Input Test (Closed)
36	Set thumbwheel switches to 400.
37	Connect INPUT TEST PLUGS [ED-2C433-( ), GR1] to both the JA1 and JA2 connectors on the FECC unit.
38	Momentarily depress TEST pushbutton. Verify that numbers appearing on the TEST RESULTS LEDs are 0100.
39	If proper results are obtained in Step 38, proceed to Step 43. If proper results are not obtained, proceed to next step.
40	Observe numbers that appear on the TEST RESULTS LEDs and refer to Table B.
41	Replace the indicated CPs from Table B one at a time and repeat Steps 38 and 39 after each replacement.
42	Repeat procedure in Step 41 until the proper result is obtained and then proceed to Step 43.
43	Remove INPUT TEST PLUGS from JA1 and JA2 connectors and proceed to Step 44.

TABLE B

INPUT TESTS FOR FECC
(See Note)

TEST RESULTS	CIRCUIT PACK TROUBLE LOCATION CODE (SEE TABLE A)
0001 THRU 0006	X50, X62, X00, X01
0007 THRU 0011	X50, X60, X00, X01
0012 THRU 0016	X50, X61, X00, X01
0017 THRU 0022	X50, X62, X00, X01
0023 THRU 0027	X50, X60, X00, X01
0028 THRU 0032	X50, X61, X00, X01
0033 THRU 0034	X50, X62, X00, X01
0100	PASS

Note: The INPUT TEST PLUGS are *not* connected to the JA1 & JA2 connectors for the INPUT TEST (OPEN).

The INPUT TEST PLUGS *are* connected to the JA1 & JA2 connectors for the INPUT TEST (CLOSED).

The JA1 connector terminal *pairs* are ordered sequentially 1 to 24 from bottom to top. The numbers marked on the connector are pin numbers. Pins 1 and 26 are pair 1, pins 2 and 27 are pair 2, etc., up to pins 24 and 49 which are pair 24. The number appearing on the TEST RESULTS LEDs indicates the pair that is open or closed, depending on the test being performed. Therefore, if the TEST RESULTS LEDs indicate 0015, pins 15 and 40 or the 15th pair from the bottom of the connector is indicated in trouble.

The JA2 connector terminal pairs are ordered sequentially 25 to 34 bottom to top, pins 1 and 26 are pair 25, pins 2 and 27 are pair 26, etc., up to pins 10 and 35 which are pair 34. Therefore, if the TEST RESULTS LEDs indicate 0030, pins 6 and 31 or the 6th pair from the bottom is indicated in trouble.

STEP	PROCEDURE
	G. Output Loopback Test
44	Set thumbwheel switches to 500.
45	Connect I/O TEST CABLE between JA1 and JB1 connectors.
46	Momentarily depress TEST pushbutton. Verify that numbers appearing on the TEST RESULTS LEDs are 0100.
47	If proper results are obtained in Step 46, proceed to Step 51. If proper results are not obtained, proceed to next step.
48	Observe numbers that appear on the TEST RESULTS LEDs and refer to Table C, column 2. This table cross-references the numbers that appear on the TEST RESULTS LEDs with the CPs which are probably responsible for the failure.
49	Replace CPs indicated on Table C one at a time and repeat Steps 46 and 47 after each replacement.
50	Repeat procedure in Step 49 until the proper result is obtained and then proceed to next step.
51	Disconnect the end of I/O TEST CABLE connected to JB1 and connect to JB2.
52	Momentarily depress TEST pushbutton. Verify that numbers appearing on the TEST RESULTS LEDs are 0100.
53	If proper results are obtained in Step 52, proceed to Step 57. If proper results are not obtained, proceed to next step.
54	Observe numbers that appear on the TEST RESULTS LEDs and refer to Table C, column 3.
55	Replace indicated CPs one at a time and repeat Steps 52 and 53 after each replacement.
56	Repeat procedure in Step 55 until the proper result is obtained and then proceed to next step.
57	Disconnect the end of I/O TEST CABLE connected to JB2 and connect to JB3.
58	Momentarily depress TEST pushbutton. Verify that numbers appearing on the TEST RESULTS LEDs are 0100.
59	If proper results are obtained in Step 58, proceed to Step 63. If proper results are not obtained, proceed to next step.
60	Observe numbers that appear on the TEST RESULTS LEDs and refer to Table C, column 4.

STEP	PROCEDURE
61	Replace indicated CPs one at a time and repeat Steps 58 and 59 after each replacement.
62	Repeat the procedure in Step 61 until the proper result is obtained and then proceed to next step.
63	Disconnect the end of I/O TEST CABLE connected to JB3 and connect to JB4.
64	Momentarily depress TEST pushbutton. Verify that numbers appearing on the TEST RESULTS LEDs are 0006.
65	If proper results are obtained in Step 64, proceed to Step 69. If proper results are not obtained, proceed to next step.
66	Observe numbers that appear on the TEST RESULTS LEDs and refer to Table C, column 5.
67	Replace indicated CPs one at a time and repeat Steps 64 and 65 after each replacement.
68	Repeat procedure in Step 67 until the proper result is obtained and then proceed to next step.
69	Remove I/O TEST CABLE from the FECC and proceed to Step 70.

TABLE C

OUTPUT LOOPBACK TEST FOR FECC

TEST RESULT (COLUMN 1)	CIRCUIT PACK TROUBLE LOCATION CODE (SEE TABLE A)			
	I/O TEST CABLE BETWEEN JA1 & JB1 (COLUMN 2)	I/O TEST CABLE BETWEEN JA1 & JB2 (COLUMN 3)	I/O TEST CABLE BETWEEN JA1 & JB3 (COLUMN 4)	I/O TEST CABLE BETWEEN JA1 & JB4 (COLUMN 5)
0001	X30, X45, X00, X01	X30, X41	X31, X41	X32, X48
0002	X30, X45, X00, X01	X30, X41	X31, X41	X32, X48
0003	X30, X45, X00, X01	X30, X42	X31, X42	X32, X48
0004	X30, X45, X00, X01	X30, X42	X31, X42	X32, X48
0005	X30, X45, X00, X01	X30, X43	X31, X43	X32, X48
0006	X30, X45, X00, X01	X30, X43	X31, X43	PASS
0007	X30, X40, X00, X01	X30, X44	X31, X44	
0008	X30, X40, X00, X01	X30, X44	X31, X44	
0009	X30, X41, X00, X01	X31, X46	X31, X47	
0010	X30, X41, X00, X01	X31, X46	X31, X47	
0011	X30, X42, X00, X01	X31, X46	X31, X47	
0012	X30, X42, X00, X01	X31, X46	X31, X47	
0013	X30, X43, X00, X01	X31, X46	X31, X47	
0014	X30, X43, X00, X01	X31, X46	X31, X47	
0015	X30, X44, X00, X01	X31, X46	X31, X47	
0016	X30, X44, X00, X01	X31, X46	X31, X47	
0017	X30, X45, X00, X01	X31, X46	X32, X47	
0018	X30, X46, X00, X01	X31, X46	X32, X47	
0019	X30, X45, X00, X01	X31, X46	X32, X47	
0020	X30, X45, X00, X01	X31, X46	X32, X47	
0021	X30, X45, X00, X01	X31, X45	X32, X47	
0022	X30, X45, X00, X01	X31, X45	X32, X47	
0023	X30, X40, X00, X01	X31, X40	X32, X48	
0024	X30, X40, X00, X01	X31, X40	X32, X48	
0100	PASS	PASS	PASS	

Note: The JB( ) connector terminal *pairs* are ordered sequentially 1 to 24 from bottom to top. The numbers marked on the connectors are pin numbers. Pins 1 and 26 are pair 1, pins 2 and 27 are pair 2, etc., up to pins 24 and 49 which are pair 24. The number appearing on the TEST RESULTS LEDs indicates the pair that is open or closed, depending on the test being performed. Therefore, if the TEST RESULTS LEDs indicate 0015, pins 15 and 40 or the 15th pair from the bottom of the connector is indicated in trouble.

STEP	PROCEDURE
	H. ROM 2 Check Sum
70	Set thumbwheel switches to 600.
71	Momentarily depress TEST pushbutton. Verify that numbers appearing on the TEST RESULTS LEDs agree with the numbers appearing on the check sum label on CP X11 (except for the leading zero). Verify that the numbers appearing on the SUBTEST VERIFICATION LEDs are 00.
72	If proper results are obtained in Step 71, proceed to Step 76. If TEST RESULTS LEDs do not agree, proceed to the next step. If SUBTEST VERIFICATION LEDs are not 00, reset thumbwheel switches to 600 and repeat Steps 71 and 72.
	Note: If the SUBTEST VERIFICATION LEDs do not give the proper results on the second try, the intra-unit wiring is the probable cause of failure.
73	Replace CP X11 and repeat Steps 71 and 72. If proper results are not obtained, proceed to next step.
74	Replace CP X00 and repeat Steps 71 and 72. If proper results are not obtained, proceed to next step.
75	Replace CP X01 and repeat Steps 71 and 72.
	I. ROM 3 Check Sum
76	Set the thumbwheel switches to 601.
77	Momentarily depress the TEST pushbutton. Verify that the numbers appearing on the TEST RESULTS LEDs agree with the numbers appearing on the check sum label on CP X12 (except for the leading zero). Verify that the numbers appearing on the SUBTEST VERIFICATION LEDs are 01.
78	If the proper results are obtained in Step 77, proceed to Step 80. If the TEST RESULTS LEDs do not agree, proceed to next step. If the SUBTEST VERIFICATION LEDs are not 01, reset the thumbwheel switches to 601 and repeat Steps 77 and 78.
79	Replace CP X12 and repeat Steps 77 and 78.

STEP	PROCEDURE
	J. RAM Test
80	Set thumbwheel switches to 602.
81	Momentarily depress TEST pushbutton. Verify that TEST RESULTS LEDs read 0055. Verify that numbers appearing on the SUBTEST VERIFICATION LEDs are 02.
82	If proper results are obtained in Step 81, proceed to Step 87. If TEST RESULTS LEDs are not 0055, proceed to next step. If SUBTEST VERIFICATION LEDs are not 02, reset thumbwheel switches to 602 and repeat Steps 81 and 82 (see note under Step 72). ***Note:*** If FECC is equipped with CP X22 and proper results are not obtained in Step 81, replace CP X22, repeat Step 81, and if test results are still not obtained, proceed to Step 85.
83	Replace CP X20 and repeat Steps 81 and 82. If the proper results are not obtained, proceed to next step.
84	Replace CP X21 and repeat Steps 81 and 82. If proper results are not obtained, proceed to next step.
85	Replace CP X00 and repeat Steps 81 and 82. If proper results are not obtained, proceed to next step.
86	Replace CP X01 and repeat Steps 81 and 82.

STEP	PROCEDURE

K. Far End ID Test

87 Set the thumbwheel switches to 603.

88 Momentarily depress the TEST pushbutton. Verify that the TEST RESULTS LEDs agree with the Identity Number assigned to that far-end. This number is encoded in rocker switches on CP X26.

Note: Add the total of the numbers by each rocker switch that is depressed toward a number.

Verify that the numbers appearing on the SUBTEST VERIFICATION LEDs are 03.

89 If proper results are obtained in Step 88, proceed to Step 93. If the TEST RESULTS LEDs do not agree with the Identity Number assigned, proceed to next step. If the SUBTEST VERIFICATION LEDs are not 03, reset the thumbwheel switches to 603 and repeat Steps 88 and 89 (see note under Step 72).

90 Replace CP X26 and repeat Steps 88 and 89.

IMPORTANT! Encode the appropriate data on the identity (FE ID), SMAS capacity (SM CAP), and port type (PRT TYP) rocker switches of the new X26 CP.

If the proper results are not obtained, proceed to the next step.

91 Replace CP X51 and repeat Steps 88 and 89. If proper results are not obtained, proceed to next step.

92 Replace CP X35 and repeat Steps 88 and 89.

STEP	PROCEDURE

L. SMAS Capacity Test

93 Set thumbwheel switches to 604.

94 Momentarily depress TEST pushbutton. Verify that TEST RESULTS LEDs agree with the SMAS capacity (highest assigned connector group number) of that far end. This number is encoded in the SM CAP rocker switches on circuit pack X26. Verify that numbers appearing on SUBTEST VERIFICATION LEDs are 04.

95 If proper results are obtained in Step 94, proceed to Step 99. If TEST RESULTS LEDs do not agree with the SMAS capacity number, proceed to next step. If SUBTEST VERIFICATION LEDs are not 04, reset thumbwheel switches to 604 and repeat Steps 94 and 95 (see note under Step 72).

96 Replace CP X26 and repeat Steps 94 and 95.

IMPORTANT! Encode the appropriate data on the FE ID, SM CAP and PRT TYP rocker switches of the new X26 CP.

If the proper results are not obtained, proceed to next step.

97 Replace CP X51 and repeat Steps 94 and 95. If proper results are not obtained, proceed to next step.

98 Replace CP X35 and repeat Steps 94 and 95.

STEP	PROCEDURE

M. Port Type Test

99 Set thumbwheel switches to 605.

Note: See Fig. 5A. The information as to which crossbar levels the RATP have been assigned is encoded in rocker switches on CP X26. Each of the four LED displays in the TEST RESULTS has been allocated to a unique crossbar level of the SMAS-4A. The presence of a one indicates that a RATP has been assigned to that level (as encoded in the rocker switches).

100 Momentarily depress TEST pushbutton. Verify that TEST RESULTS LEDs agree with the encoding on CP X26. Verify that the numbers appearing on the SUBTEST VERIFICATION LEDs are 05.

101 If proper results are obtained in Step 100, proceed to Step 105. If TEST RESULTS LEDs do not agree with the encoding, proceed to next step. If SUBTEST VERIFICATION LEDs are not 05, reset thumbwheel switches to 605 and repeat Steps 100 and 105 (see note under Step 72).

102 Replace CP X26 and repeat Steps 100 and 101.

IMPORTANT! Encode the crossbar levels to which the RATPs have been assigned, the identity number, and the SMAS capacity number with the rocker switches on the new X26 CP.

If the proper results are not obtained, proceed to next step.

103 Replace CP X51 and repeat Steps 100 and 101. If proper results are not obtained, proceed to next step.

104 Replace CP X35 and repeat Steps 100 and 101.

105 Set thumbwheel switches to 606.

106 Momentarily depress TEST pushbutton. Verify that TEST RESULTS LEDs agree with the encoding on CP X26 (see Fig. 5B). Verify that numbers appearing on SUBTEST VERIFICATION LEDs are 06.

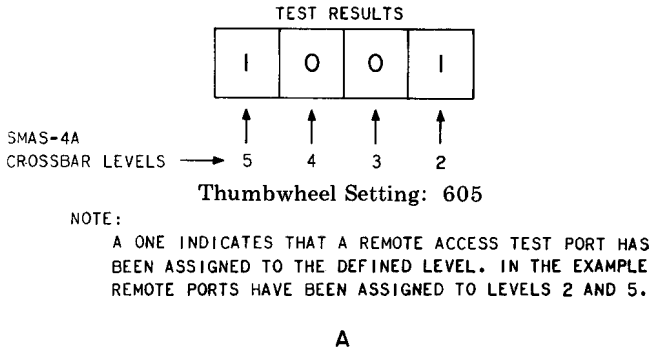
107 If proper results are obtained in Step 106, proceed to Step 111. If TEST RESULTS LEDs do not agree with the encoding, proceed to next step. If SUBTEST VERIFICATION LEDs are not 06, reset thumbwheel switches to 606 and repeat Steps 106 and 107 (see note under Step 72).

108 Replace CP X26 and repeat Steps 106 and 107.

IMPORTANT! Encode the appropriate data as stated in Step 102.

If proper results are not obtained, proceed to next step.

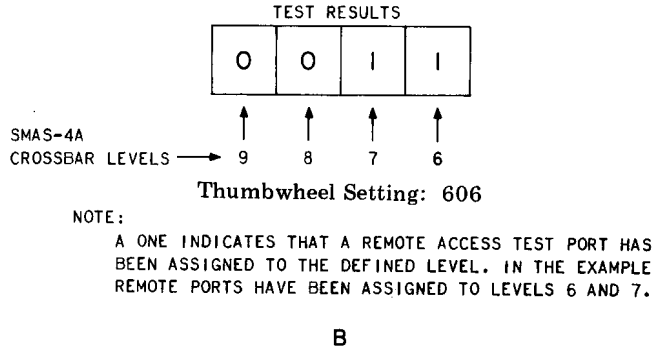
STEP	PROCEDURE
109	Replace CP X51 and repeat Steps 106 and 107. If proper results are not obtained, proceed to next step.
110	Replace CP X35 and repeat Steps 106 and 107.



Thumbwheel Setting: 605

NOTE:
A ONE INDICATES THAT A REMOTE ACCESS TEST PORT HAS BEEN ASSIGNED TO THE DEFINED LEVEL. IN THE EXAMPLE REMOTE PORTS HAVE BEEN ASSIGNED TO LEVELS 2 AND 5.

A



Thumbwheel Setting: 606

NOTE:
A ONE INDICATES THAT A REMOTE ACCESS TEST PORT HAS BEEN ASSIGNED TO THE DEFINED LEVEL. IN THE EXAMPLE REMOTE PORTS HAVE BEEN ASSIGNED TO LEVELS 6 AND 7.

B

Fig. 5—Port Type Test

STEP	PROCEDURE

N. EIA Input Test

111 Connect the MISC TEST PLUG to the JMISC connector of the FECC.

112 Set the thumbwheel switches to 607.

113 Momentarily depress the TEST pushbutton. Verify that the SUBTEST VERIFICATION LEDs are 07.

114 If the SUBTEST VERIFICATION LEDs read 07, proceed to next step. If the SUBTEST VERIFICATION LEDs do not read 07, reset thumbwheel switches to 607 and repeat Step 113.

115 Follow the step procedure in Table D, per the explanation of each column listed below:

COLUMN 1—STEP: Follow these steps one at a time until proper results are obtained in Columns 4, 5, 6, and 7.

COLUMN 2—FROM TERMINAL: Attach a clip lead from this terminal to the terminal listed in Column 3.

COLUMN 3—TO TERMINAL: Attach a clip lead to this terminal from the terminal listed in Column 2.

COLUMNS 4, 5, 6, and 7—TEST RESULTS LEDs TO READ: If a 1 or 0 is listed in a column, this must be what appears on the TEST RESULTS LEDs on CP17. An X in one of these columns means it does not matter what number appears.

COLUMN 8—REPLACE CIRCUIT PACKS: If proper results are not obtained in Column 4, 5, 6, or 7, replace these CPs one at a time from left to right and repeat step listed in Column 9 after each replacement.

COLUMN 9—REPEAT STEP: Repeat this step after each replacement of a CP listed in Column 8.

116 Set the thumbwheel switches to 608.

117 Momentarily depress the TEST pushbutton. Verify that the SUBTEST VERIFICATION LEDs are 08.

118 If the SUBTEST VERIFICATION LEDs read 08, proceed to next step. If the SUBTEST VERIFICATION LEDs do not read 08, reset thumbwheel switches to 608 and repeat Step 117.

119 Follow the step procedure in Table E, per the explanation of each column listed in Step 115.

120 Set the thumbwheel switches to 609.

STEP	PROCEDURE

121 Momentarily depress the TEST pushbutton. Verify that the SUBTEST VERIFICATION LEDs are 09.

122 If the SUBTEST VERIFICATION LEDs read 09, proceed to next step. If the SUBTEST VERIFICATION LEDs do not read 09, reset thumbwheel switches to 609 and repeat Step 121.

123 Follow the step procedure in Table F, per the explanation of each column listed in Step 115.

TABLE D

THUMBWHEEL TO 607

	CROSS CONNECT CLIP LEAD		OBTAIN PROPER RESULTS				IF PROPER RESULTS ARE NOT OBTAINED	
COLUMN 1	2	3	4	5	6	7	8	9
STEP	FROM TERMINAL	TO TERMINAL	TEST RESULTS LEDs TO READ				REPLACE CIRCUIT PACKS ONE AT A TIME	REPEAT STEP
1	54 of TS-B	58 of TS-B	X	X	X	1	X27, X35, X51	113 (Page 23)
2	54 of TS-B	1 of MISC TEST PLUG	X	X	1	X	X27, X35, X51	113 (Page 23)
3	54 of TS-B	3 of MISC TEST PLUG	X	1	X	X	X27, X35, X51	113 (Page 23)
4	54 of TS-B	55 of TS-B	1	X	X	X	X27, X35, X25, X51	113 (Page 23)
5	34 of TS-B	58 of TS-B	X	X	X	0	X27, X35, X51	113 (Page 23)
6	34 of TS-B	1 of MISC TEST PLUG	X	X	0	X	X27, X35, X51	113 (Page 23)
7	34 of TS-B	3 of MISC TEST PLUG	X	0	X	X	X27, X35, X51	113 (Page 23)
8	34 of TS-B	55 of TS-B	0	X	X	X	X27, X35, X25, X51	113 (Page 23)
9	When the proper results are obtained above, proceed to Step 116 (Page 23).							

TABLE E

THUMBWHEEL TO 608

	CROSS CONNECT CLIP LEAD		OBTAIN PROPER RESULTS				IF PROPER RESULTS ARE NOT OBTAINED	
COLUMN 1	2	3	4	5	6	7	8	9
STEP	FROM TERMINAL	TO TERMINAL	TEST RESULTS LEDs TO READ				REPLACE CIRCUIT PACKS ONE AT A TIME	REPEAT STEP
1	54 of TS-B	48 of TS-B	X	X	X	1	X27, X35, X25, X51	117 (Page 23)
2	54 of TS-B	4 of MISC TEST PLUG	X	X	1	X	X27, X35, X51	117 (Page 23)
3	54 of TS-B	32 of MISC TEST PLUG	X	1	X	X	X27, X35, X51	117 (Page 23)
4	54 of TS-B	45 of TS-B	1	X	X	X	X27, X35, X51	117 (Page 23)
5	34 of TS-B	48 of TS-B	X	X	X	0	X27, X35, X25, X51	117 (Page 23)
6	34 of TS-B	4 of MISC TEST PLUG	X	X	0	X	X27, X35, X51	117 (Page 23)
7	34 of TS-B	32 of MISC TEST PLUG	X	0	X	X	X27, X35, X51	117 (Page 23)
8	34 of TS-B	45 of TS-B	0	X	X	X	X27, X35, X51	117 (Page 23)
9	When the proper results are obtained above, proceed to Step 120 (Page 23).							

TABLE F

THUMBWHEEL TO 609

	CROSS CONNECT CLIP LEAD		OBTAIN PROPER RESULTS				IF PROPER RESULTS ARE NOT OBTAINED	
COLUMN 1	2	3	4	5	6	7	8	9
STEP	FROM TERMINAL	TO TERMINAL	TEST RESULTS LEDs TO READ				REPLACE CIRCUIT PACKS ONE AT A TIME	REPEAT STEP
1	54 of TS-B	38 of TS-B	X	X	X	1	X27, X35, X51	121 (Page 24)
2	54 of TS-B	37 of TS-B	X	X	1	X	X27, X35, X51	121 (Page 24)
3	54 of TS-B	36 of TS-B	X	1	X	X	X27, X35, X51	121 (Page 24)
4	54 of TS-B	35 of TS-B	1	X	X	X	X27, X35, X51	121 (Page 24)
5	34 of TS-B	38 of TS-B	X	X	X	0	X27, X35, X51	121 (Page 24)
6	34 of TS-B	37 of TS-B	X	X	0	X	X27, X35, X51	121 (Page 24)
7	34 of TS-B	36 of TS-B	X	0	X	X	X27, X35, X51	121 (Page 24)
8	34 of TS-B	35 of TS-B	0	X	X	X	X27, X35, X51	121 (Page 24)
9	When the proper results are obtained above, proceed to Step 124 (Page 24).							

STEP	PROCEDURE

O. EIA Output Test

124 Set the thumbwheel switches to 610.

125 Momentarily depress the TEST pushbutton. Verify that the SUBTEST VERIFICATION LEDs read 10 and, using a KS-14510-L1 multimeter, verify that the dc potential, to ground, at each of the following points is between -6.5 and -13.2 volts:

Terminal 7 of the MISC TEST PLUG

Terminal 6 of the MISC TEST PLUG

Terminal 26 of TS-B

Terminal 25 of TS-B

Terminal 18 of TS-B

Terminal 17 of TS-B.

126 If the proper results are obtained in Step 125, proceed to Step 130. If the proper results are not obtained, proceed to the next step.

127 Replace CP X27 and repeat Steps 125 and 126. If proper results are not obtained, proceed to next step.

128 Replace CP X32 and repeat Steps 125 and 126. If proper results are not obtained, proceed to next step.

129 Replace CP X35 and repeat Steps 125 and 126.

130 Set the thumbwheel switches to 611.

131 Momentarily depress the TEST pushbutton. Verify that the SUBTEST VERIFICATION LEDs read 11, and, using a KS-14510-L1 multimeter, verify that the dc potential is between +6.5 and +13.2 volts at the same points as listed in Step 125.

132 If the proper results are obtained in Step 131, proceed to Step 136. If the proper results are not obtained, proceed to next step.

133 Replace CP X27 and repeat Steps 131 and 132. If proper results are not obtained, proceed to next step.

134 Replace CP X32 and repeat Steps 131 and 132. If proper results are not obtained, proceed to next step.

135 Replace CP X35 and repeat Steps 131 and 132.

STEP	PROCEDURE
	P. Interrupt Tests
136	Set the thumbwheel switches to 612.
137	Using a clip lead, connect one end to terminal 54 of TS-B (+6V) and momentarily connect the other end to terminal 48 of TS-B (ring). Verify that the TEST RESULTS LEDs read 0201. Verify that the SUBTEST VERIFICATION LEDs read 12.
138	If the proper results are obtained in Step 137, proceed to Step 143. If proper results are not obtained, proceed to next step.
139	Replace CP X25 and repeat Steps 137 and 138. If proper results are not obtained, proceed to next step.
140	Replace CP X27 and repeat Steps 137 and 138. If proper results are not obtained, proceed to next step.
141	Replace CP X35 and repeat Steps 137 and 138. If proper results are not obtained, proceed to next step.
142	Replace CP X51 and repeat Steps 137 and 138.
143	Remove one end of the clip lead from terminal 48 of TS-B and momentarily connect it to terminal 55 of TS-B (data carrier). Verify that the TEST RESULTS LEDs read 0202.
144	If the proper results are obtained in Step 143, proceed to Step 149. If proper results are not obtained, proceed to next step.
145	Replace CP X25 and repeat Steps 143 and 144. If proper results are not obtained, proceed to next step.
146	Replace CP X27 and repeat Steps 143 and 144. If proper results are not obtained, proceed to next step.
147	Replace CP X35 and repeat Steps 143 and 144. If proper results are not obtained, proceed to next step.
148	Replace CP X51 and repeat Steps 143 and 144.
149	Place MTCE switch on CP X25 in nonmaintenance position (down).
	Note: The INT LED may or may not be flashing at this time.
150	Depress and hold RESET pushbutton on CP X25. Verify that INT LED on X25 flashes and that numbers appearing on SUBTEST VERIFICATION LEDs are 12.
151	Release RESET pushbutton.

STEP	PROCEDURE
152	If proper results are obtained in Step 150, proceed to next step. If INT LED is not flashing, replace CP X25 and repeat Steps 149 through 152. If SUBTEST VERIFICATION LEDs are not 12, reset thumbwheel switches to 612 and repeat Steps 149 through 152 (see note under Step 72).
153	Remove FL fuse from fuse panel (SD-99785-01).
154	Wait for more than three seconds and reinsert FL fuse. Verify that TEST RESULTS LEDs read 0200 and SUBTEST VERIFICATION LEDs are 12.
155	If proper results are obtained in Step 154, proceed to Step 158. If proper results are not obtained, repeat Steps 153 through 155 several times before proceeding to next step. ***Note:*** If at any time the TEST RESULTS LEDs read 0200, after reinserting FL fuse, the test should be considered passed.
156	Replace CP X25 and repeat Steps 153 through 155. If proper results are not obtained, proceed to next step.
157	Replace CP X51 and repeat Steps 153 through 155.
158	Set thumbwheel switches to 613.
159	Momentarily depress RESET pushbutton on CP X25. Verify that SUBTEST VERIFICATION LEDs are 13.
160	About 1 second later reset thumbwheel switches to 612, and record amount of time that elapses before SUBTEST VERIFICATION LEDs are 12. Verify that this time is between 90 and 150 seconds. (On some FECC units the TEST RESULT LEDs may READ 0200 but this is not necessary.)
161	If proper results are obtained in Step 160, proceed to Step 164. If proper results are not obtained, proceed to next step.
162	Replace CP X25 and repeat Steps 158 through 161. If proper results are not obtained, proceed to next step.
163	Replace CP X35 and repeat Steps 158 through 161.
164	Set thumbwheel switches to 614.
165	Momentarily depress RESET pushbutton. Verify that SUBTEST VERIFICATION LEDs are 14.
166	About one second later reset thumbwheel switches to 612 and record amount of time that elapses before TEST RESULTS LEDs read 0200. Verify that this time is between 90 and 150 seconds. Verify that SUBTEST VERIFICATION LEDs are 12.
167	If proper results are obtained in Step 166, proceed to Step 170. If proper results are not obtained, proceed to next step.

STEP	PROCEDURE
168	Replace CP X25 and repeat Steps 164 through 167. If proper results are not obtained, proceed to next step.
169	Replace CP X35 and repeat Steps 164 through 167.
170	Set thumbwheel switches to 613.
171	Momentarily depress RESET pushbutton. Using the KS-14510-L1 multimeter on MISC TEST PLUG, verify that there ***is*** continuity between terminals 23 and 48 and between terminals 24 and 49. This measurement must take place within 60 seconds.
172	If proper results are obtained in Step 171, proceed to Step 175. If proper results are not obtained, proceed to next step.
173	Replace CP X25 and repeat Steps 171 and 172. If proper results are not obtained, proceed to next step.
174	Replace CP X48 and repeat Steps 171 and 172.
175	Momentarily depress RESET pushbutton (thumbwheel switches still at 613). Verify that SUBTEST VERIFICATION LEDs are 13.
176	Set thumbwheel switches to 612. Wait at least 150 seconds. Using the KS-14510-L1 multimeter, verify that there is ***no*** continuity between terminals 23 and 48 and between terminals 24 and 49 of the MISC TEST PLUG. Verify that SUBTEST VERIFICATION LEDs are 12.
177	If proper results are obtained in Step 176, proceed to Step 180. If proper results are not obtained, proceed to next step.
178	Replace CP X25 and repeat Steps 175 through 177. If proper results are not obtained, proceed to next step.
179	Replace CP X48 and repeat Steps 175 through 177.
180	Set thumbwheel switches to 000 and remove Test Card (CP17).
181	Remove MISC TEST PLUG from FECC.
182	Momentarily depress RESET pushbutton.
183	Replace all system cables on FECC [all PA( ), all PB( ), PMISC, PEIA1, and PEIA2].

6. SIMPLIFIED STEP PROCEDURE FOR FECC

6.01 Table G is a simplified version of the written step procedures (Part 5). It is intended to be used as a job aid and only after a tester has become familiar with the written step procedures.

A COLUMNS

6.02 An A above a column means an Action is to be taken by the tester. In most tests, several actions must be taken before a result is obtained.

R COLUMNS

6.03 An R above a column means this Result must be obtained before the test is to be considered passed. In some tests, there are two results that must be obtained.

( ) PARENTHESES

6.04 The numbers in parentheses are the steps of Table G that are to be followed in sequential order. Example: Step 6 must not be worked until Step 5 is completed.

6.05 Column 1 (TYPE OF TEST) and Column 2 (FIRST STEP IN TEST) are to be used as references to the written step procedures when the proper results are not obtained in Table G.

6.06 Before using Table G, verify that PWR FAIL LEDs on CPs X90 and X91 are ***off***. If PWR FAIL LEDs are ***on***, perform Part 5A, "Power Tests" (Steps 1 through 4), of the written step procedures.

7. TFCC TESTS

7.01 The step procedures in this part of the section are to isolate a defective CP in the TFCC. The steps must be performed in order and the tester should not proceed to the next step until the previous step has been successfully completed. If any test cannot be completed with the corrective action described (for example, see Step 22), the intra-unit wiring (wiring between CPs) is the probable cause of trouble. If the intra-unit wiring is to be checked for opens, shorts, grounds, etc, on the TFCC at any time during the tests, it is necessary to return to Step 1 and start again.

7.02 The tests and the first step in each test are as follows:

Step 1	A. Power Tests
Step 5	B. Address Bit Check (zero state)
Step 16	C. Address Bit Check (one state)
Step 23	D. ROM 1 Check Sum
Step 30	E. Input Test (open)
Step 36	F. Input Test (closed)
Step 44	G. Output Loopback Test
Step 64	H. ROM 2 Check Sum
Step 70	I. ROM 3 Check Sum
Step 74	J. RAM Test
Step 80	K. DDD Number Test
Step 94	L. EIA Output Test
Step 105	M. EIA Input Test
Step 118	N. Interrupt Tests
Step 155	O. Ringing Timer Tests

7.03 Before the following tests are performed, all system cables are to be disconnected from the TFCC [all PA( ), all PB( ), and PMISC].

TABLE G

SIMPLIFIED STEP PROCEDURE FOR FECC

TYPE OF TEST	FIRST STEP IN TEST	A CP16	A CP17	A MTCE SWITCH TO (ON X25)	A TOGGLE SWITCH (ON CP17)	A THUMB-WHEEL SETTING	A INPUT TEST PLUG CONNECTED TO	A I/O TEST CABLE CONNECTED BETWEEN	A TEST PUSHBUTTON MOMENTARILY DEPRESSED	R RED LEDs (ON CP16)	R GREEN LEDs (ON CP16)	R TEST RESULTS LEDs TO READ	R SUBTEST VERIFI-CATION LEDs TO READ
A. POWER TEST (See 6.06)	1												
B. ADDRESS BIT CHECK (Zero state)	5	(1) IN	(2) IN	(3) MTCE	(4) ON	(5) 000			(6) YES	(7) OFF	(8) ON		
C. ADDRESS BIT CHECK (One state)	16					(9) 100			(10) YES	(11) ON Note 1	(12) OFF		
D. ROM 1 CHECK SUM	23	(13) OUT				(14) 200			(15) YES			(16) Note 2	
E. INPUT TEST (OPEN)	30					(17) 300			(18) YES			(19) 0100	
F. INPUT TEST (CLOSED)	36					(20) 400	(21) JA1 & JA2		(22) YES			(23) 0100	
	43						(24) Remove						
G. OUTPUT LOOPBACK TEST	44					(25) 500		(26) JA1 & JB1	(27) YES			(28) 0100	
	51							(29) JA1 & JB2	(30) YES			(31) 0100	
	57							(32) JA1 & JB3	(33) YES			(34) 0100	
	63							(35) JA1 & JB4	(36) YES			(37) 0006	
	69							(38) Remove					
H. ROM 2 CHECK SUM	70					(39) 600			(40) YES			(41) Note 3	(42) 00

A = Action to be taken by tester.

R = Results to be obtained.

( ) = Number of step (work in sequential order).

Note 1: Except LEDs 14 and 15.

Note 2: Same as Check Sum label on circuit pack X10.

Note 3: Same as Check Sum label on circuit pack X11.

TABLE G (Cont)

SIMPLIFIED STEP PROCEDURE FOR FECC

TYPE OF TEST	FIRST STEP IN TEST	A MISC TEST PLUG CONNECTED TO JMISC	A THUMB-WHEEL SETTING	A TEST PUSHBUTTON MOMENTARILY DEPRESSED	R TEST RESULTS LEDs TO READ	R SUBTEST VERIFI-CATION LEDs TO READ	A & R CROSS CONNECT CLIP LEADS AND OBTAIN PROPER RESULTS PER TABLE:			A & R DC POTENTIAL IS BETWEEN −6.5 & −13.2 ON TERMS: (SEE NOTE 9)	A & R DC POTENTIAL IS BETWEEN +6.5 & +13.2 ON TERMS: (SEE NOTE 9)
							D	E	F		
I. ROM 3 CHECK SUM	76		(43) 601	(44) YES	(45) Note 4	(46) 01					
J. RAM TEST	80		(47) 602	(48) YES	(49) 0055	(50) 02					
K. FAR-END ID TEST	87		(51) 603	(52) YES	(53) Note 5	(54) 03					
L. SMAS CAPACITY TEST	93		(55) 604	(56) YES	(57) Note 6	(58) 04					
M. PORT TYPE TEST	99		(59) 605	(60) YES	(61) Note 7	(62) 05					
	105		(63) 606	(64) YES	(65) Note 8	(66) 06					
N. EIA INPUT TEST	111	(67) YES	(68) 607	(69) YES		(70) 07	(71) YES				
	116		(72) 608	(73) YES		(74) 08		(75) YES			
	120		(76) 609	(77) YES		(78) 09			(79) YES		
O. EIA OUTPUT TEST	124		(80) 610	(81) YES		(82) 10				(83) YES	
	130		(84) 611	(85) YES		(86) 11					(87) YES

A = Action to be taken by tester.

R = Results to be obtained.

( ) = Number of step (work in sequential order).

Note 4: Same as Check Sum label on circuit pack X12.

Note 5: Same as Far-End ID number encoded on circuit pack X26.

Note 6: Same as SMAS Capacity encoded on circuit pack X26.

Note 7: Same as RATP Assignment encoded on circuit pack X26 (Fig. 5a).

Note 8: Same as RATP Assignment encoded on circuit pack X26 (Fig. 5b).

Note 9: Terminal 7 of the MISC TEST PLUG
Terminal 6 of the MISC TEST PLUG
Terminal 26 of TS-B
Terminal 25 of TS-B
Terminal 18 of TS-B
Terminal 17 of TS-B.

TABLE G (Cont)

TYPE OF TEST	FIRST STEP IN TEST	A MISC TEST PLUG CONNECTED TO JMISC	A THUMB-WHEEL SETTING	A TOGGLE SWITCH (ON CP17)	A CP17	A MTCE SWITCH TO (ON X25)	A RESET PUSHBUTTON MOMENTARILY DEPRESSED	A REMOVE FL FUSE MORE THAN 3 SEC AND RE-INSERT	R INT LED FLASHING	R ON TS-B MOMENTARILY CONNECT CLIP LEAD BETWEEN TERMINAL 54 AND TERMINAL	R TEST RESULTS LEDs TO READ	R SUBTEST VERIFI-CATION LEDs TO READ	R CONTINUITY BETWEEN TERM. 23 & 48 AND TERM. 24 & 49 (OF MISC TEST PLUG)	
													WITHIN 60 SEC	AFTER 150 SEC
P. INTERRUPT TEST	136		(88) 612							(89) 48	(90) 0201	(91) 12		
	143									(92) 55	(93) 0202			
	149					(94) NON-MTCE	(95) YES Note 10		(96) YES					
	153							(97) YES			(98) 0200	(99) 12		
	158		(100) 613				(101) Note 11					(102) 13		
	160		(103) 612								(104) 0200 Note 12	(105) 12		
	164		(106) 614				(107) Note 13					(108) 14		
	166		(109) 612								(110) 0120 Note 12	(111) 12 Note 12A		
	170		(112) 613				(113) YES					(114) 13	(115) YES	
	175						(116) Note 14					(117) 13		
	176		(118) 612									(119) 12		(120) NO
RESTORAL	180	(121) REMOVE	(122) 000	(123) OFF	(124) REMOVE		(125) YES							

A = Action to be taken by tester.

R = Results to be obtained.

( ) = Number of step (work in sequential order).

Note 10: Hold depressed for the results of Step 96.

Note 11: Perform Step 103 in about ONE second.

Note 12: This reading may appear in some FECC units. It is not necessary.

Note 12A: SUBTEST VERIFICATION LEDs will read 12 between 90 and 150 seconds after depressing RESET pushbutton.

Note 13: Perform Step 109 in about ONE second.

Note 14: Perform next step in about ONE second.

STEP	PROCEDURE

A. Power Tests

1 Observe PWR FAIL LEDs on CPs X90 and X91 (see Table H). Verify that PWR FAIL LEDs are off.

2 If PWR FAIL LEDs are ***off***, proceed to Step 5. If LEDS are ***on***, proceed to next step.

3 Using a multimeter, measure dc voltage on CPs X90 and X91 (SD-1P003). Verify that limits are met as indicated below:

+5—between 4.75V and 5.25V

-9—between -9.4V and -8.6V

+12—between 10.8V and 13.2V

-12—between -13.2V and -10.8V

Note: Variations from these limits may be caused by the malfunction of CPs X90 or X91 or by excessive loading on power converters by a malfunctioning circuit pack.

4 If above limits cannot be met, replace CPs as required and repeat Steps 1 and 2.

TABLE H

CROSS REFERENCE OF CIRCUIT PACK TROUBLE IDENTIFICATION CODES AND THE ASSOCIATED CIRCUIT PACK TEST FUNCTION CONTROL CIRCUIT

CIRCUIT PACK TROUBLESHOOTING IDENTIFICATION CODE	PHYSICAL LOCATION	CIRCUIT PACK NUMBER	ED CODE NUMBER	FUNCTIONAL DESIGNATION
X00	AA18	CP1	ED-1P220-( )	CPU 1
X01	AA20	CP2	ED-1P221-( )	CPU 2
X10	AA24	CP150	ED-1P271-( )	ROM 1
X11	AA27	CP151	ED-1P272-( )	ROM 2
X12	AA30	CP152	ED-1P273-( )	ROM 3
X20	AA16	CP4	ED-1P223-( )	RAM 1
X20	AA16	CP18A	ED-1P393-( )	SRAM 1
X25	BB20	CP14	ED-1P263-( )	DATA/INT
X26	BB23	CP15	ED-1P264-( )	PDDD
X27	BB25	CP15	ED-1P264-( )	SDDD
X30	AA42	CP5	ED-1P224-( )	ALT 1
X31	AA44	CP5	ED-1P224-( )	ALT 2
X35	BB27	CP6	ED-1P225-( )	LT 1
X40	BB53	CP8	ED-1P227-( )	RELAY 1
X41	BB56	CP8	ED-1P227-( )	RELAY 2
X42	BB59	CP8	ED-1P227-( )	RELAY 3
X43	BB62	CP8	ED-1P227-( )	RELAY 4
X50	BB16	CP7	ED-1P226-( )	IN 1
X60	BB11	CP9	ED-1P228-( )	BUFF 1
X61	BB09	CP9	ED-1P228-( )	BUFF 2
X90	AA01	CP11	ED-1P230-( )	9V
X91	BB01	CP3	ED-1P222-( )	5V

STEP	PROCEDURE
	B. Address Bit Check (Zero State)
5	Insert Program Counter [CP 16, ED-1P265-( )] and Test Card [CP 17, ED-1P378-( )] into the TFCC at the physical locations identified on the unit.
6	Operate MTCE 1 and MTCE 2 switches on CP X25 to maintenance position (up).
7	Using front panel toggle switch on CP 17, set power to ON.
8	Set thumbwheel switch to 000.
9	Momentarily depress TEST pushbutton. Verify that all red LEDs on CP 16 are ***off*** and all green LEDs are ***on***.
10	If proper results are obtained in Step 9, proceed to Step 16. If proper results are not obtained, proceed to next step.
11	Replace CP X00 and repeat Steps 9 and 10. If proper results are not obtained, proceed to next step.
12	Replace CP X01 and repeat Steps 9 and 10. If proper results are not obtained, proceed to next step.
13	Remove CPs X20, X30, X31, X35, X50, X12, X11, and X10 in that order, repeating Step 9 after each removal. When proper results are obtained, replace the last CP removed, reinsert the other CPs, and repeat Steps 9 and 10.
14	If all CPs have been removed in Step 13 and proper results are not obtained, reinsert CPs, replace CP X25, and repeat Steps 9 and 10.
15	If proper results are still not obtained and Step 3 has not been performed, it should be performed at this time. If Step 3 has been performed, intra-unit wiring is the probable cause of trouble.

STEP	PROCEDURE
	C. Address Bit Check (One State)
16	Set thumbwheel switches on CP 17 to 100.
17	Momentarily depress TEST pushbutton. Verify that all red LEDs on CP 16, except 14 and 15, are ***on*** and all green LEDs are ***off***.
18	If proper results are obtained in Step 17, proceed to Step 23. If proper results are not obtained, proceed to next step.
19	Replace CP X00 and repeat Steps 17 and 18. If proper results are not obtained, proceed to next step.
20	Replace CP X01 and repeat Steps 17 and 18. If proper results are not obtained, proceed to next step.
21	Remove CPs X20, X30, X31, X35, X50, X12, and X11 in that order, repeating Steps 17 and 18 after each removal. When proper results are obtained, replace the last CP removed, reinsert the other CPs, and repeat Steps 17 and 18.
22	If all CPs mentioned in Step 21 have been removed and proper results are not obtained, reinsert all CPs, replace CP X10, and repeat Steps 17 and 18.
	D. ROM 1 Check Sum
23	Remove the Program Counter CP16 from the TFCC.
24	Set thumbwheel switches to 200.
25	Momentarily depress TEST pushbutton. Verify that numbers appearing on the TEST RESULTS LEDs on CP 17 agree with the numbers appearing on the check sum label on circuit pack X10. ***Note:*** The TEST RESULTS LEDs will have a leading zero (example, 0124) which does not appear on the check sum label (example, 124).
26	If proper results are obtained in Step 25, proceed to Step 30. If proper results are not obtained, proceed to next step.
27	Replace CP X10 and repeat Steps 25 and 26. If proper results are not obtained proceed to next step.
28	Replace CP X00 and repeat Steps 25 and 26. If proper results are not obtained, proceed to next step.
29	Replace CP X01 and repeat Steps 25 and 26.

STEP	PROCEDURE
	E. Input Test (Open)
30	Set thumbwheel switches to 300.
31	Momentarily depress TEST pushbutton. Verify that numbers appearing on the TEST RESULTS LEDs are 0100.
32	If proper results are obtained in Step 31, proceed to Step 36. If proper results are not obtained, proceed to next step.
33	Observe numbers that appear on the TEST RESULTS LEDs and refer to Table I. This table cross-references the numbers that appear on the TEST RESULTS LEDs with the CPs which are probably responsible for the failure.
34	Replace the indicated CPs from Table I one at a time and repeat Steps 31 and 32 after each replacement.
35	Repeat the procedure in Step 34 until the proper result is obtained and then proceed to Step 36.
	F. Input Test (Closed)
36	Set thumbwheel switches to 400.
37	Connect INPUT TEST PLUG [ED-2C433-( ), GR1] to the JA1 connector on the TFCC unit.
38	Momentarily depress TEST pushbutton. Verify that numbers appearing on the TEST RESULTS LEDs are 0100.
39	If proper results are obtained in Step 38, proceed to Step 43. If proper results are not obtained, proceed to next step.
40	Observe numbers that appear on the TEST RESULTS LEDs and refer to Table I.
41	Replace the indicated CPs from Table I one at a time and repeat Steps 38 and 39 after each replacement.
42	Repeat procedure in Step 41 until the proper result is obtained and then proceed to Step 43.
43	Remove INPUT TEST PLUG from JA1 connector and proceed to next step.

TABLE I

INPUT TESTS FOR THE TFCC
(SEE NOTE)

TEST RESULTS	CIRCUIT PACK TROUBLE LOCATION CODE (SEE TABLE H)
0001 thru 0016	X50, X60, X00, X01
0017	X50, X61, X25, X00, X01
0018 thru 0020	X50, X61, X00, X01
0021 thru 0024	X50, X25, X00, X01
0100	PASS

Note: The INPUT TEST PLUG is ***not*** connected to the JA1 connector for the INPUT TEST (OPEN).

The INPUT TEST PLUG ***is*** connected to the JA1 connector for the INPUT TEST (CLOSED).

The JA1 connector terminal ***pairs*** are ordered sequentially 1 to 24 from bottom to top. The numbers marked on the connector are pin numbers. Pins 1 and 26 are pair 1, pins 2 and 27 are pair 2, etc., up to pins 24 and 49 which are pair 24. The number appearing on the TEST RESULTS LEDs indicates the pair that is open or closed, depending on the test being performed. Therefore, if the TEST RESULTS LEDs indicate 0015, pins 15 and 40 or the 15th pair from the bottom of the connector is indicated in trouble.

STEP	PROCEDURE
	G. Output Loopback Test
44	Set thumbwheel switches to 500.
45	Connect I/O TEST CABLE between JA1 and JB1 connectors.
46	Momentarily depress TEST pushbutton. Verify that numbers appearing on the TEST RESULTS LEDs are 0100.
47	If proper results are obtained in Step 46, proceed to Step 51. If proper results are not obtained, proceed to next step.
48	Observe numbers that appear on the TEST RESULTS LEDs and refer to Table J, column 2. This table cross-references the numbers that appear on the TEST RESULTS LEDs with the CPs which are probably responsible for the failure.
49	Replace CPs indicated on Table J one at a time and repeat Steps 46 and 47 after each replacement.
50	Repeat procedure in Step 49 until the proper result is obtained and then proceed to next step.
51	Disconnect the end of I/O TEST CABLE connected to JB1 and connect to JB2.
52	Momentarily depress TEST pushbutton. Verify that numbers appearing on the TEST RESULTS LEDS are 0100.
53	If proper results are obtained in Step 52, proceed to Step 57. If proper results are not obtained, proceed to next step.
54	Observe numbers that appear on the TEST RESULTS LEDs and refer to Table J, column 3.
55	Replace indicated CPs one at a time and repeat Steps 52 and 53 after each replacement.
56	Repeat procedure in Step 55 until the proper result is obtained and then proceed to next step.
57	Disconnect the end of I/O TEST CABLE connected to JB2 and connect to JB3.
58	Momentarily depress TEST pushbutton. Verify that numbers appearing on the TEST RESULTS LEDs are 0009.
59	If proper results are obtained in Step 58, proceed to Step 63. If proper results are not obtained, proceed to next step.
60	Observe numbers that appear on the TEST RESULTS LEDs and refer to to Table J, column 4.

STEP	PROCEDURE

61 Replace indicated CPs one at a time and repeat Steps 58 and 59 after each replacement.

62 Repeat the procedure in Step 61 until the proper result is obtained and then proceed to next step.

63 Remove I/O TEST CABLE from the TFCC and proceed to Step 64.

TABLE J

OUTPUT LOOPBACK TEST FOR TFCC

TEST RESULTS (COLUMN 1)	CIRCUIT PACK TROUBLE LOCATION CODE (SEE TABLE H)		
	I/O TEST CABLE BETWEEN JA1 & JB1 (COLUMN 2)	I/O TEST CABLE BETWEEN JA1 & JB2 (COLUMN 3)	I/O TEST CABLE BETWEEN JA1 & JB3 (COLUMN 4)
0001 THRU 0004	X30, X40, X00, X01	X30, X41	X31, X43
0005 THRU 0008	X30, X40, X00, X01	X30, X42	X31, X43
0009	X30, X40, X00, X01	X31, X42	PASS
0010 THRU 0014	X30, X40, X00, X01	X31, X42	
0015 THRU 0018	X30, X41, X00, X01	X31, X42	
0019 THRU 0024	X30, X41, X00, X01	X31, X43	
0100	PASS	PASS	

Note: The JB ( ) connector terminal *pairs* are ordered sequentially 1 to 24 from bottom to top. The numbers marked on the connectors are pin numbers. Pins 1 and 26 are pair 1, pins 2 and 27 are pair 2, etc., up to pins 24 and 49 which are pair 24. The number appearing on the TEST RESULTS LEDs indicates the pair that is open or closed, depending on the test being performed. Therefore, if the TEST RESULTS LEDs indicate 0015, pins 15 and 40 or the 15th pair from the bottom of the connector is indicated in trouble.

STEP	PROCEDURE
	H. ROM 2 Check Sum
64	Set thumbwheel switches to 600.
65	Momentarily depress TEST pushbutton. Verify that numbers appearing on the TEST RESULTS LEDs agree with the numbers appearing on the check sum label on CP X11 (except for the leading zero). Verify that the numbers appearing on the SUBTEST VERIFICATION LEDs are 00.
66	If proper results are obtained in Step 65, proceed to Step 70. If TEST RESULTS LEDs do not agree, proceed to the next step. If SUBTEST VERIFICATION LEDs are not 00, reset thumbwheel switches to 600 and repeat Steps 65 and 66. ***Note:*** If the SUBTEST VERIFICATION LEDs do not give the proper results on the second try, the intra-unit wiring is the probable cause of failure.
67	Replace CP X11 and repeat Steps 65 and 66. If proper results are not obtained, proceed to next step.
68	Replace CP X00 and repeat Steps 65 and 66. If proper results are not obtained, proceed to next step.
69	Replace CP X01 and repeat Steps 65 and 66.
	I. ROM 3 Check Sum ***Note:*** If the TFCC is not equipped with CP X12 (CP 152), bypass this test and proceed to Step 74 (J. RAM Test).
70	Set thumbwheel switches to 601.
71	Momentarily depress TEST pushbutton. Verify that numbers appearing on the TEST RESULTS LEDs agree with the numbers appearing on the check sum label on CP X12 (except for the leading zero). Verify that the numbers appearing on the SUBTEST VERIFICATION LEDs are 01.
72	If proper results are obtained in Step 71, proceed to Step 74. If TEST RESULTS LEDs do not agree, proceed to the next step. If SUBTEST VERIFICATION LEDs are not 01, reset thumbwheel switches to 601 and repeat Steps 71 and 72. ***Note:*** If the SUBTEST VERIFICATION LEDs do not give the proper results on the second try, the intra-unit wiring is the probable cause of failure.
73	Replace CP X12 and repeat Steps 71 and 72.

STEP	PROCEDURE
	J. RAM Test
74	Set thumbwheel switches to 602.
75	Momentarily depress TEST pushbutton. Verify that TEST RESULTS LEDs read 0100. Verify that numbers appearing on the SUBTEST VERIFICATION LEDs are 02.
76	If proper results are obtained in Step 75, proceed to Step 80. If TEST RESULTS LEDs are not 0100, proceed to next step. If SUBTEST VERIFICATION LEDs are not 02, reset thumbwheel switches to 602 and repeat Steps 75 and 76 (see note under Step 72).
77	Replace CP X20 and repeat Steps 75 and 76. If proper results are not obtained, proceed to next step.
78	Replace CP X00 and repeat Steps 75 and 76. If proper results are not obtained, proceed to next step.
79	Replace CP X01 and repeat Steps 75 and 76.

STEP	PROCEDURE

K. DDD Number Test

Note: See Section 666-613-100 (under TFCC) for method of encoding CPs X26 and X27.

80 Remove CP X26 from the TFCC. Record the Primary DDD number encoded in the Binary Coded Decimal (BCD) switches S 0 to S 11. Also, record the mode of dialing encoded in switch S 15. See note under Step 82.

81 Reinsert CP X26.

82 Remove CP X27 and record the Alternate DDD number and mode of dialing encoded in BCD switches S 0 to S 11 and S 15.

Note: If CP X26 and/or X27 have not been encoded, set the BCD switches to any DDD number, making sure to include numbers 8, 4, 2, and 1, and set the switch following the last digit of the DDD number to a BCD value of 15 (all rocker switches depressed toward the label).

83 Reinsert CP X27.

84 Set the thumbwheel switches to 603.

85 Momentarily depress TEST pushbutton. Verify that the letter E or d appearing in the left [or A (see Fig. 6)] LEDs of the TEST RESULTS LEDs agree with the setting of the BCD switch S 15 on CP X26. Verify that numbers appearing on the SUBTEST VERIFICATION LEDs are 03.

86 If proper results are obtained in Step 85, proceed to next step. If proper results are not obtained, proceed to Step 93.

87 Momentarily depress TEST pushbutton. Verify that the letter E or d appearing in the B LEDs (see Fig. 6) of the TEST RESULTS LEDs agree with the setting of BCD switch S 15 on CP X27.

88 If proper results are obtained in Step 87, proceed to next step. If proper results are not obtained, proceed to Step 93.

89 Momentarily depress TEST pushbutton. Verify that the numbers appearing in the C LEDs at half-second intervals, with the character A inserted between each digit at half-second intervals, agree with the setting of the BCD switches S 0 to S 11 on CP X26. Verify that after the last DDD number appears, the character A is displayed and held.

Note: This test may be repeated, as necessary, by depressing the TEST pushbutton.

90 If proper results are obtained in Step 89, proceed to next step. If proper results are not obtained, proceed to Step 93.

91 Momentarily depress TEST pushbutton. Verify that the numbers appearing in the D LEDs at half-second intervals, with the character A inserted between each digit at half-second

STEP	PROCEDURE

intervals, agree with the setting of the BCD switches S 0 to S 11 on CP X27. Verify that after the last DDD number appears, the character A is displayed and held.

Note: This test may be repeated, as necessary, by depressing the TEST pushbutton.

92 If proper results are obtained in Step 91, proceed to Step 94. If proper results are not obtained, proceed to next step.

93 Replace CP X50 and repeat the previous step. If proper results are still not obtained, replace CP X35 and repeat previous step. If proper results are still not obtained, replace CP X26 (if testing the Primary DDD number and mode of dialing) or CP X27 (if testing the Alternate DDD number and mode of dialing).

IMPORTANT! Encode the respective DDD numbers and mode of dialing on the replacement CP. If the difficulty is confined to the Primary DDD number or mode, replace CP X26 first. If the difficulty is confined to the Alternate DDD number or mode, replace CP X27 first.

TEST RESULTS

TEST RESULT LED'S DISPLAY ON CP 17	(A)	(B)	(C)	(D)
	MODE OF DIALING FOR PRIMARY DDD NUMBERS E IF TOUCHTONE d IF DIAL PULSE	MODE OF DIALING FOR ALTERNATE DDD NUMBERS	PRIMARY DDD NUMBERS DIGITS WILL APPEAR SEQUENTIALLY SEPARATED BY THE CHARACTER A. SECOND DIAL TONE DETECTION WILL BE REPRESENTED BY THE CHARACTER d .	ALTERNATE DDD NUMBERS

Fig. 6—DDD Number Test for TFCC

STEP	PROCEDURE
	L. EIA Output Test
94	Connect the MISC TEST PLUG to the JMISC connector of the TFCC.
95	Set thumbwheel switches to 604.
96	Momentarily depress the TEST pushbutton. Using the KS-14510-L1 multimeter on MISC TEST PLUG, verify that the dc potential between terminals 3 and 28 is between -13.2 and -6.5 volts. Verify that SUBTEST VERIFICATION LEDs are 04.
97	If proper results are obtained in Step 96, proceed to Step 100. If proper results are not obtained, proceed to next step.
98	Replace CP X25 and repeat Steps 96 and 97. If proper results are not obtained, proceed to next step.
99	Replace CP X35 and repeat Steps 96 and 97.
100	Set thumbwheel switches to 605.
101	Momentarily depress the TEST pushbutton. Using the KS-14510-L1 multimeter on MISC TEST PLUG, verify that the dc potential between terminals 3 and 28 is between +13.2 and +6.5 volts. Verify that SUBTEST VERIFICATION LEDs are 05.
102	If proper results are obtained in Step 101 proceed to Step 105. If proper results are not obtained, proceed to next step.
103	Replace CP X25 and repeat Steps 101 and 102. If proper results are not obtained, proceed to next step.
104	Replace CP X35 and repeat Steps 101 and 102.

STEP	PROCEDURE

M. EIA Input Test

105 Using a clip lead, connect terminal 4 to terminal 29 on the MISC TEST PLUG (MISC TEST PLUG still connected to JMISC connector).

106 Set thumbwheel switches to 606.

107 Momentarily depress TEST pushbutton on CP17. Verify that SUBTEST VERIFICATION LEDs are 06.

108 Operate MTCE 1 and MTCE 2 switches on CP X25 to nonmaintenance position (down).

109 Using a second clip lead, connect one end to terminal 1 of the MISC TEST PLUG and connect the other end to terminal 54 of TS-B (+6VDC) on the FECC (see note). Verify that a ***zero*** appears on the right LEDs of the TEST RESULTS LEDs (see Fig. 7).

Note: Terminal 54 at +6VDC, and terminal 34, at -6VDC, of TS-B on the FECC is a voltage source with an output impedance of 1.5 kilohms. When performing this test, the FECC must be operational or an equivalent voltage source must be substituted.

110 If proper results are obtained in Step 109, remove the clip lead from terminal 54 of TS-B on the FECC and proceed to Step 113. If proper results are not obtained, proceed to next step.

111 Operate MTCE 1 and MTCE 2 switches to maintenance position (up), replace CP X25, and repeat Steps 108 through 110. If proper results are not obtained, proceed to next step.

112 Replace CP X35 and repeat Steps 108 through 110.

113 Operate MTCE 1 and MTCE 2 switches to maintenance position (up). Momentarily depress TEST pushbutton and operate MTCE 1 and MTCE 2 switches to nonmaintenance position (down).

114 Connect the clip lead to terminal 34 of TS-B (-6VDC) on the FECC (see note in Step 109). Verify that a ***one*** appears on the right LEDs of the TEST RESULTS LEDs (see Fig. 7).

115 If proper results are obtained in Step 114, remove the two clip leads and the MISC TEST PLUG from the TFCC and proceed to Step 118. If proper results are not obtained, proceed to next step.

116 Replace CP X25 and repeat Steps 114 and 115. If proper results are not obtained, proceed to next step.

117 Replace CP X35 and repeat Steps 114 and 115.

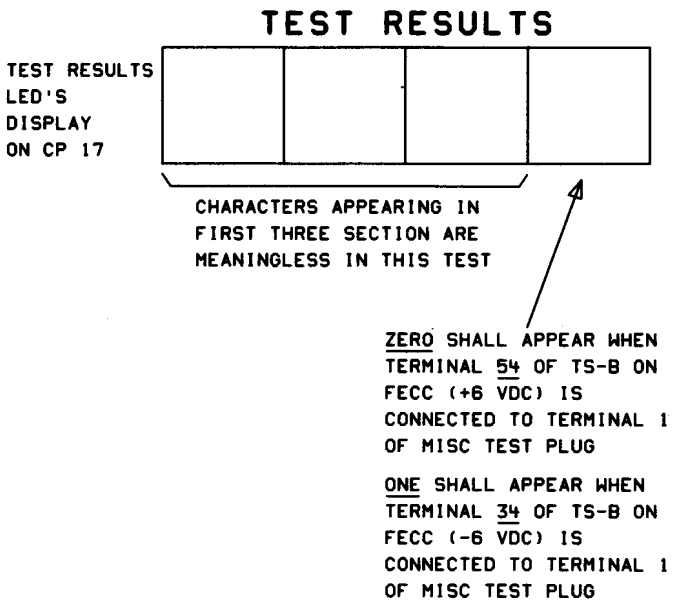


Fig. 7—EIA Input Test

STEP	PROCEDURE
	N. Interrupt Tests
118	Using a clip lead, connect terminal 29 at the rear of connector JMISC on the TFCC.
119	Connect the MISC TEST PLUG to connector JA1 on the TFCC.
120	Verify that the MTCE 1 and MTCE 2 switches are in the maintenance position (up).
121	Set the thumbwheel switches to 607.
122	Momentarily depress the TEST pushbutton. Verify that the SUBTEST VERIFICATION LEDs are 07.
123	Operate the MTCE 1 and MTCE 2 switches to the nonmaintenance position (down).
124	Using a second clip lead, momentarily connect terminal 21 to terminal 46 on the MISC TEST PLUG. Verify that the numbers appearing on the TEST RESULTS LEDs are 0200.
125	If proper results are obtained in Step 124, proceed to next step. If proper results are not obtained, replace CP X25 and repeat Steps 118 through 125.
126	Remove the clip lead from terminal 21 and 46.
127	Operate the MTCE 1 and MTCE 2 switches to the maintenance position (up).
128	Momentarily depress the TEST pushbutton.
129	Operate the MTCE 1 and MTCE 2 switches to the nonmaintenance position (down).
130	Using a clip lead, momentarily connect terminal 22 to terminal 47 on the MISC TEST PLUG. Verify that the numbers appearing on the TEST RESULTS LEDs are 0201.
131	If proper results are obtained in Step 130, proceed to next step. If proper results are not obtained, replace CP X25 and repeat Steps 118 through 131.
132	Remove the clip lead from terminals 22 and 47.
133	Operate the MTCE 1 and MTCE 2 switches to the maintenance position (up).
134	Momentarily depress the TEST pushbutton.
135	Operate the MTCE 1 and MTCE 2 switches to the nonmaintenance position (down).
136	Using a clip lead, momentarily connect terminal 23 to terminal 48 on the MISC TEST PLUG. Verify that the numbers appearing on the TEST RESULTS LEDs are 0202.
137	If proper results are obtained in Step 136, proceed to next step. If proper results are not obtained, replace CP X25 and repeat Steps 118 through 137.

STEP	PROCEDURE
138	Remove the clip lead from terminals 23 and 48.
139	Operate the MTCE 1 and MTCE 2 switches to the maintenance position (up).
140	Momentarily depress the TEST pushbutton.
141	Operate the MTCE 1 and MTCE 2 switches to the nonmaintenance position (down).
142	Using a clip lead, momentarily connect terminal 24 to terminal 49 on the MISC TEST PLUG. Verify that the numbers appearing on the TEST RESULTS LEDs are 0203.
143	If proper results are obtained in Step 142, proceed to next step. If proper results are not obtained, replace CP X25 and repeat Steps 118 through 143.
144	Remove the clip lead from terminals 24 and 49.
145	Operate the MTCE 1 and MTCE 2 switches to the maintenance position (up).
146	Momentarily depress the TEST pushbutton.
147	Operate the MTCE 1 and MTCE 2 switches to the nonmaintenance position (down).
148	Remove the clip lead from terminals 4 and 29 at the rear of connector JMISC on the TFCC. Verify that the numbers appearing on the TEST RESULTS LEDs are 0200.
149	If proper results are obtained in Step 148 proceed to Step 151. If proper results are not obtained, proceed to next step.
150	Replace CP X25 and repeat Steps 118 through 149.
151	Remove the MISC TEST PLUG from connector JA1.
152	Set the thumbwheel switches to 000.
153	Momentarily depress the TEST pushbutton.
154	On CP 17, operate power switch off and remove CP 17 from TFCC. Proceed to next step.

STEP	PROCEDURE
	O. Ringing Timer Test
155	Remove the TL fuse from the Filter, Fuse, and Alarm Panel (SD-99785-01).
156	Using the KS-14510-L1 multimeter between terminals 37 and 47 on TS-A of the TFCC, verify that there is continuity for 2 to 5 seconds when a clip lead is placed between terminals 57 and 18 of TS-A.
157	If proper results are obtained in Step 156, proceed to next step. If proper results are not obtained, inspect the wiring and operation of relays TM and TO, resistor RT 1, and the D3 circuit packs. Take corrective action and repeat Step 156 until proper results are obtained.
158	Using a second clip lead between terminals 17 and 27 of TS-A (first clip lead still on terminals 57 and 18) verify that there is continuity for 95 to 175 seconds with the KS multimeter still between terminals 37 to 47 of TS-A.
159	If proper results are obtained in Step 158, proceed to next step. If proper results are not obtained, inspect the wiring and operation of relays TTA and CR and thermal timer TT. Take corrective action and repeat Step 158 until proper results are obtained.
160	Replace all system cables on the TFCC [all PA( ), all PB( ), and PMISC]. Remove clip leads and multimeter.
161	Replace the TL fuse.

8. SIMPLIFIED STEP PROCEDURE FOR TFCC

8.01 Table K is a simplified version of the written step procedures in Part 7. It is intended to be used as a job aid and only after a tester has become familiar with the written step procedures.

A COLUMNS

8.02 An A above a column means an Action is to be taken by the tester. In most tests several actions must be taken before a result is obtained.

R COLUMNS

8.03 An R above a column means this Result must be obtained before the test is to be considered passed. In some tests, there are two results that must be obtained.

( ) PARENTHESES

8.04 The numbers in parentheses are the steps of Table K that are to be followed in sequential order. Example: Step 6 must not be worked until Step 5 is completed.

8.05 Column 1 (TYPE OF TEST) and Column 2 (FIRST STEP IN TEST) are to be used as references to the written step procedures when the proper results are not obtained in Table K.

8.06 Before using Table K, verify that the POWER FAIL LEDs on CPs X90 and X91 are ***off***. If LEDs are ***on***, perform Part 7A, "Power Tests" (Steps 1 through 4), of the written step procedures.

9. RTS-1A CONTROLLER TESTS

9.01 At the present time, there are no trouble isolation tests available for the RTS-1A

TABLE K

SIMPLIFIED STEP PROCEDURE FOR TFCC

TYPE OF TEST	FIRST STEP IN TEST	A CP16	A CP17	A MTCE1 AND MTCE2 SWITCHES TO (ON X25)	A TOGGLE SWITCH (ON CP17)	A THUMB-WHEEL SETTING	A INPUT TEST PLUG CONNECTED TO	A I/O TEST CABLE CONNECTED BETWEEN	A TEST PUSHBUTTON MOMENTARILY DEPRESSED	R RED LEDs (ON CP16)	R GREEN LEDs (ON CP16)	R TEST RESULTS LEDs TO READ	R SUBTEST VERIFI-CATION LEDs TO READ
A. POWER TEST (See 8.06)	1												
B. ADDRESS BIT CHECK (Zero state)	5	(1) IN	(2) IN	(3) MTCE (up)	(4) ON	(5) 000			(6) YES	(7) OFF	(8) ON		
C. ADDRESS BIT CHECK (One state)	16					(9) 100			(10) YES	(11) ON Note 1	(12) OFF		
D. ROM 1 CHECK SUM	23	(13) OUT				(14) 200			(15) YES			(16) Note 2	
E. INPUT TEST (OPEN)	30					(17) 300			(18) YES			(19) 0100	
F. INPUT TEST (CLOSED)	36					(20) 400	(21) JA1		(22) YES			(23) 0100	
	43						(24) Remove						
G. OUTPUT LOOPBACK TEST	44					(25) 500		(26) JA1 & JB1	(27) YES			(28) 0100	
	51							(29) JA1 & JB2	(30) YES			(31) 0100	
	57							(32) JA1 & JB3	(33) YES			(34) 0009	
	63							(35) Remove					
H. ROM 2 CHECK SUM	64					(36) 600			(37) YES			(38) Note 3	(39) 00
I. ROM 3 CHECK SUM	70					(40) 601 Note 4			(41) YES			(42) Note 5	(43) 01
J. RAM TEST	74					(44) 602			(45) YES			(46) 0100	(47) 02

A = Action to be taken by tester.

R = Results to be obtained.

( ) = Number of step (work in sequential order).

Note 1: Except LEDs 14 and 15.

Note 2: Same as Check Sum label on circuit pack X10.

Note 3: Same as Check Sum label on circuit pack X11.

Note 4: If TFCC is not equipped with circuit pack X12, bypass this test.

Note 5: Same as Check Sum label on circuit pack X12.

TABLE K (Cont)

SIMPLIFIED STEP PROCEDURE FOR TFCC

TYPE OF TEST	FIRST STEP IN TEST	A MTCE1 AND MTCE2 SWITCHES TO (ON X25)	A CONNECT TERM. 4 TO 29 AT REAR OF JMISC CONNECTOR	A MISC TEST PLUG CONNECTED TO JA1	A ON MISC TEST PLUG PLACE A CLIP LEAD FROM TERM.	A THUMB-WHEEL SETTING	A TEST PUSHBUTTON MOMENTARILY DEPRESSED	A TOGGLE SWITCH (ON CP17)	A CP17	R TEST RESULTS LEDs TO READ	R SUBTEST VERIFI-CATION LEDs TO READ
N. INTERRUPT TEST	118		(83) YES	(84) YES		(85) 607	(86) YES				(87) 07
	123	(88) Non-MTCE (down)			(89) 21 to 46 Note 11					(90) 0200	
	127	(91) MTCE (up)					(92) YES				
	129	(93) Non-MTCE (down)			(94) 22 to 47 Note 11					(95) 0201	
	133	(96) MTCE (up)					(97) YES				
	135	(98) Non-MTCE (down)			(99) 23 to 48 Note 11					(100) 0202	
	139	(101) MTCE (up)					(102) YES				
	141	(103) Non-MTCE (down)			(104) 24 to 49 Note 11					(105) 0203	
	145	(106) MTCE (up)					(107) YES				
	147	(108) Non-MTCE (down)	(109) Remove							(110) 0200	
	151			(111) Remove		(112) 000	(113) YES	(114) OFF	(115) Remove		

A = Action to be taken by tester.

R = Results to be obtained.

( ) = Number of step (work in sequential order).

Note 11: Hold clip lead to terminals until results of next step (XX) are completed and then remove clip lead.

TABLE K (Cont)

SIMPLIFIED STEP PROCEDURE FOR TFCC

TYPE OF TEST	FIRST STEP IN TEST	A MTCE1 AND MTCE2 SWITCHES TO (ON X25)	A PLACE A CLIP LEAD FROM TERM. 4 TO 29 ON MISC TEST PLUG	A PLACE A CLIP LEAD FROM TERM. 1 ON MISC TEST PLUG TO TERM.	A MISC TEST PLUG CONNECTED TO JMISC	A THUMB-WHEEL-SETTING	A TEST PUSHBUTTON MOMENTARILY DEPRESSED	R DC POTENTIAL BETWEEN TERM. 3 & 28 OF MISC TEST PLUG IS BETWEEN	R TEST RESULTS LEDs TO READ	R SUBTEST VERIFI-CATION LEDs TO READ
K. DDD NUMBER TEST	80					(48) 603	(49) YES		(50) Note 6	(51) 03
	87						(52) YES		(53) Note 7	
	89						(54) YES		(55) Note 8	
	91						(56) YES		(57) Note 9	
L. EIA OUTPUT TEST	94				(58) YES	(59) 604	(60) YES	(61) −13.2 & −6.5		(62) 04
	100					(63) 605	(64) YES	(65) +13.2 & +6.5		(66) 05
M. EIA INPUT TEST	105		(67) YES			(68) 606	(69) YES			(70) 06
	108	(71) Non-MTCE (down)		(72) 54 of TS-B on FECC					(73) − − −0 Note 10	
	110			(74) Remove						
	113	(75) MTCE (up)					(76) YES			
	113	(77) Non-MTCE (down)		(78) 34 of TS-B on FECC					(79) − − −1 Note 10	
	115		(80) Remove	(81) Remove	(82) Remove					

A = Action to be taken by tester.

R = Results to be obtained.

( ) = Number of step (work in sequential order).

Note 6: Same as mode of dialing encoded on circuit pack X26 (Fig. 7).

Note 7: Same as mode of dialing encoded on circuit pack X27 (Fig. 7).

Note 8: Same as Primary DDD number encoded on circuit pack X26 (Fig. 7).

Note 9: Same as Alternate DDD number encoded on circuit pack X27 (Fig. 7).

Note 10: The first three LEDs are meaningless in this test.

TABLE K (Cont)

SIMPLIFIED STEP PROCEDURE FOR TFCC

TYPE OF TEST	FIRST STEP IN TEST	A TL FUSE ON FILTER, FUSE AND ALARM PANEL	A CONNECT MULTIMETER TO TERM. 37 & 47 OF TS-A	A FIRST CLIP LEAD BETWEEN TERM. (TS-A)	A SECOND CLIP LEAD BETWEEN TERM. (TS-A)	R CONTINUITY BETWEEN TERM. 37 & 47 OF TS-A EXISTS FROM		A ALL SYSTEM CABLES
						2 TO 5 SEC	95 TO 220 SEC	
O. RINGING TIMER TEST	155	(116) Remove	(117) YES	(118) 57 & 18		(119) YES		
	158				(120) 17 & 27		(121) YES	
	160		(122) Remove	(123) Remove	(124) Remove			(125) Replace
	161	(126) Replace						

A = Action to be taken by tester.

R = Results to be obtained.

( ) = Number of step (work in sequential order).

controller. If trouble occurs, CD- and SD-1P002-01 should be used.

10. RATP TESTS

10.01 At the present time, there are no trouble isolation tests available for the RATP. If trouble occurs, CD- and SD-1P001-01 should be used.

11. TROP TESTS

11.01 At the present time, there are no trouble isolation tests available for the TROP. If trouble occurs, CD- and SD-1P005-01 should be used.