

STORED PROGRAM CONTROL NO. 1A GENERAL DESCRIPTION

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NOTICE

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1. GENERAL

1.01 This section provides general descriptive information on the Stored Program Control (SPC) No. 1A, an electronic control system for selective use in telephone switching applications. The SPC No. 1A is a stored program electronic processing system. It can provide either electromechanical or electronic switching systems with access to a large-capacity high-speed memory and to stored program logic.

1.02 Reasons for reissuing this section are listed below. Since this is a general revision, no revision arrows are used to denote changes.

- (a) Added Fig. 3 to show communications bus details
- (b) Added Fig. 4 to show the bus transformer and terminal block assembly
- (c) Added information in Part 2 to give a better description of the physical appearance and function of all major equipment units of the SPC No. 1A
- (d) Increased information on the processor maintenance matching system
- (e) Added information on common channel interoffice signaling (CCIS) direct signaling (DS) equipment used with TSPS

- (f) Added information in Part 6 on the bootstrap transfer card extender.

SYSTEM APPLICATION

1.03 The SPC No. 1A is basically a computer and memory system which is independent of application. However, it has generalized interfaces to which hardware and software may be readily applied in the development of specific application systems.

1.04 The SPC No. 1A was developed concurrently with one of its application systems, the Traffic Service Position System (TSPS) No. 1. The TSPS is basically a cordless electronic switchboard with associated peripheral equipment designed to improve operator assistance facilities. The SPC No. 1A is also used in No. 4A/4M toll offices equipped with the Electronic Translator System (ETS) and in Signal Transfer Point (STP) stand-alone offices.

1.05 The SPC No. 1A provides a flexible control system for implementing new or modernized telephone services. Through the use of stored program techniques, improved telephone services can be implemented more effectively and at a substantially lower cost than by electromechanical means.

1.06 Common programs for controlling and maintaining the SPC No. 1A equipments are provided in all SPC installations. Application programming is limited to the services of the application system and to the maintenance of non-SPC equipment when not provided for by the SPC generic program.

1.07 The following is a summary of objectives and features of the SPC No. 1A:

- (a) The SPC No. 1A is a highly reliable stored program processing system for selective application in telephone switching
- (b) It represents a flexible means to extend newly conceived telephone services to both electronic and electromechanical installations with a minimum of transition costs
- (c) The SPC No. 1A offers the advantages of a large, expandable, and electronically alterable high-speed memory.

1.08 The remainder of this section will deal with the control system itself and not with service features the stored program can offer.

DESIGN CONSIDERATIONS

1.09 The SPC No. 1A is designed to provide the consumer with economical, reliable, high-quality telephone services. To achieve this goal, the following basic system techniques are employed in the SPC No. 1A:

- Stored program logic
- Functional concentration
- Time-shared control
- Modular design
- Plug-in equipment units
- Duplication
- Automatic fault location and system reconfiguration.

1.10 *Stored Program Logic:* Functions to be performed by the system are specified by programs consisting of precisely defined instructions. These instructions, suitably encoded, are stored in a memory unit from which they are transmitted one at a time to a control unit for execution. Thus, operation of the system can be altered considerably by program changes without any circuit modification.

1.11 *Functional Concentration:* System equipment is concentrated in a small number of highly efficient units, each specialized in some broad system function such as control, input, output, memory, etc. The result is an overall equipment organization that is simple.

1.12 *Time-Shared Control:* A single control unit (processor) directs the operation of all other system units in accordance with the program instructions. Using electronic devices, this control unit can operate at speeds much faster than the rate at which events associated with these instructions occur. Consequently, the control equipment is time-shared by all the functions handled by the system. This is accomplished by subdividing the work required to control each task into functional

segments and by interweaving these segments with those associated with other tasks.

1.13 Modular Design: Equipment units are provided in modular blocks so that growth can be accommodated economically and conveniently.

1.14 Plug-in Equipment Units: In a major portion of the equipment, circuit components (such as transistors, resistors, etc.) are mounted on circuit packs (CPs) which are plug-in units with printed wiring. Faulty CPs can be quickly replaced.

1.15 Duplication: All major SPC No. 1A units are either duplicated or partially duplicated for system reliability. This duplication enables the software maintenance programs to establish a working system in various configurations, thereby providing for excellent recovery of call processing ability in the event of system failure.

1.16 Automatic Fault Location and System Reconfiguration: The SPC No. 1A does a large portion of its own checking for system troubles. It is possible with this checking scheme for the system to detect the existence of a malfunction, to identify automatically the malfunctioning unit, to take the unit out of service, to diagnose the unit, and to notify maintenance personnel that a malfunction has occurred and of the results of diagnostic testing.

SYSTEM CONFIGURATION

1.17 Equipment which comprises the SPC No. 1A is shown in Fig. 1. The major units involved are the processor, stores, central pulse distributor (CPD), signal distributor (SD), master scanner (MS), control and display (CD), teletypewriter (TTY), and program tape unit (PTU). The duplication scheme, major communication buses, and interconnections of the units are also shown in Fig. 1.

1.18 The processor and stores comprise the SPC No. 1A data processor. The data processor communicates with the rest of the system via the CPD, SD, and MS and causes an orderly sequence of events to occur.

1.19 The CD, PTU, and TTY are mounted in the same 3-bay frame (called the CD-PT-TTY frame). These equipments provide for maintenance and administrative functions in the system. The

CD-PT-TTY frame is usually located near or adjacent to equipment performing the same function for the application system. This area is referred to as the master control center (MCC).

1.20 The maintenance TTY provides for communication between the system and craft personnel. The PTU is used to write program and data information into the stores or to record information contained in the stores onto magnetic tape. The controls and displays which aid in maintaining the SPC No. 1A equipment are located on the CD panel.

1.21 Functions to be performed by the SPC No. 1A and the application systems with which it is used are specified by programs stored in the piggyback twistor (PBT) and/or semiconductor insulated gate field effect transistor (IGFET) stores (effective with PG-1C003). These stores contain both programmed instructions and office data. All instructions and some data are stored on a relatively permanent basis and are changed as dictated by changes in service and procedures in the application system. Some of the data is relatively temporary in nature, since it may be entered into memory, modified, and erased during the processing of a call. Programmed instructions provide the intelligence necessary to instruct the processor to function as required in any call situation which the system may encounter. Instructions may also be referred to as orders or commands.

1.22 Data differs from instructions in that data consists of information such as results of computations, records of dialed digits, and information as may be required at some time for processing.

1.23 The processor, according to instructions in the store, either directly or indirectly controls operation of circuits in the application system and the SPC No. 1A. Commands specifying operations in application system circuits originate within the SPC, and answers signifying states of circuit points within the system are returned to the processor. Certain instructions result in actions which are entirely confined within the SPC. For example, an instruction or series of instructions may command the processor to perform logical and/or arithmetic operations on data currently contained within it. Other instructions may cause the SPC to command a peripheral circuit to perform an operation such as transmitting status information to the processor from a scanner.

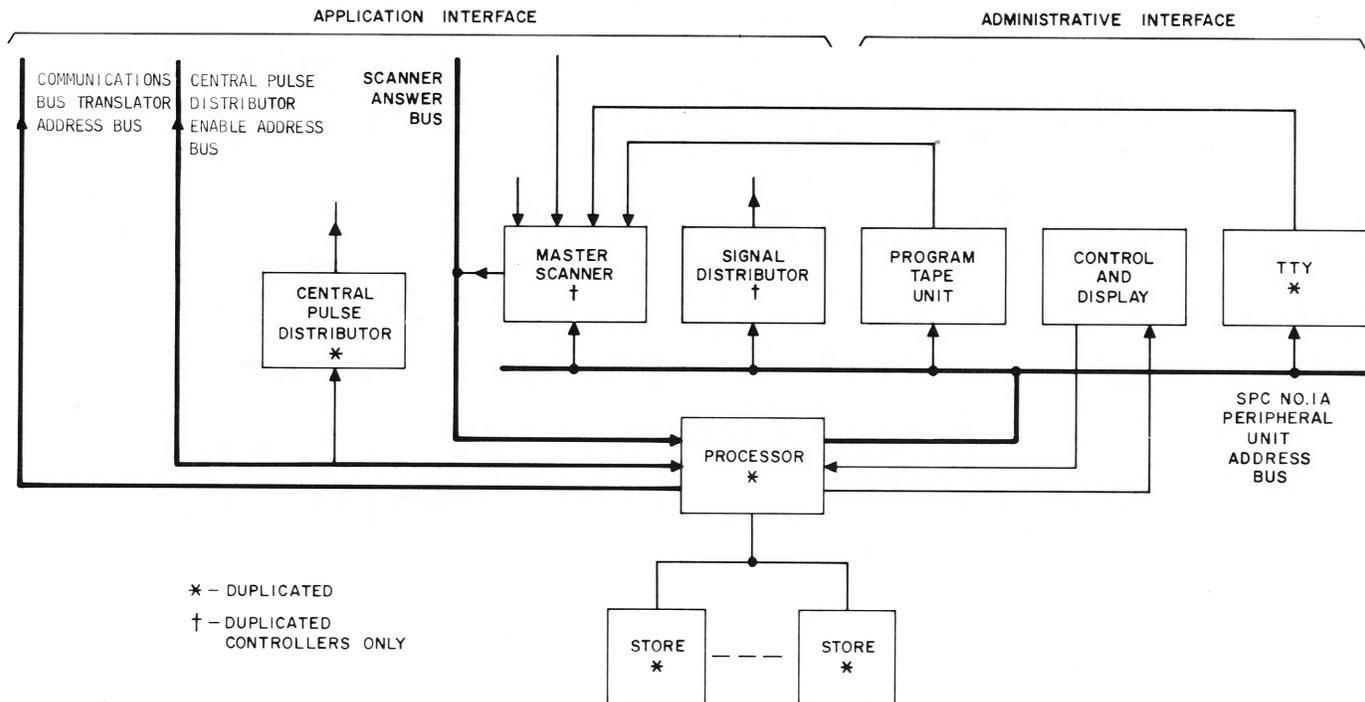


Fig. 1—SPC No. 1A Equipment Diagram

1.24 The SPC No. 1A communicates with the application system via the communication bus system, the CPD, and the scanners. Address information is transmitted in binary form from the SPC No. 1A to the communication bus translator (CBT) unit (for the TSPS) or to the peripheral function translator (PFT) unit (for the ETS and STP stand-alone systems) via the CBT address bus [sometimes referred to as the peripheral unit address bus (PUAB) for the application system]. Translation from binary to a 1-out-of-N type code, when required, is performed by the translator. The translator (CBT or PFT) is part of the application system equipment; however, it is physically located on the SPC No. 1A CPD frame. For communication with units within the SPC No. 1A, translated address information is transmitted in 1-out-of-N form via the SPC PUAB.

1.25 The 1-out-of-N type code used by the processor to communicate with most peripheral units is a selection code. "N" designates the number of inputs from which one particular input is to be selected.

1.26 Commands received by CPDs instruct CPDs to enable the receiving portion of a specified

peripheral circuit in order that it, and only it, may receive and register the command currently on the address bus.

1.27 Answer signals are transmitted over the scanner answer bus (SCAB) back to the SPC. Information represented by these signals indicates the states of various circuit points within the system.

2. EQUIPMENT DESCRIPTION AND FUNCTION

A. General

2.01 The following is a description of the organization, appearance, and layout of the SPC No. 1A equipments and associated power equipments. The basic SPC No. 1A frame requirements, excluding store frames, are given in Table A. The required number of store frames depends on the type of office (TSPS, ETS, or STP), the generic program load of the office, the amount of office data to be stored, and the type of store configuration used. Table B lists schematic drawing numbers, circuit description numbers, and equipment description section numbers for each unit of the SPC No. 1A and is provided as a quick reference

for locating some of the documents dealing specifically with individual units of the system.

2.02 SPC No. 1A equipment units are mounted in frames which consist of from one to several standardized bays. Each bay is 7 feet high and 2 feet 2 inches wide. The bays of any multibay frame are numbered consecutively, from left to right, starting with bay 0. Frames are 1 foot deep and except for MCC frames line up on floor plans with minimum maintenance aisles 2 feet 6 inches wide and minimum wiring aisles 1 foot 8 inches wide. Since cable racks are placed directly over each lineup of frames, a minimum ceiling height of 10 feet under beams is required.

2.03 Cable racks, which conceal and shield all interframe cabling, are frame supported over each line of frames and cross aisles. Typical lineups may be a uniform 39-foot length, although deviations are possible to adapt to building areas of almost any configuration. A cable rack support stanchion supports a cable rack where frames are omitted for spans of from 6-1/2 to 13 feet. Figure 2 is a sectional view of a cable rack showing its four shielded compartments.

2.04 The address and answer buses are cabled in the lower compartment with minimum lead length exposed between the compartment and the transformers mounted at or near the top of each frame. The scanner cables are cabled in a shielded channel at the front of the cable rack where they can drop down to frame terminal strips with relatively short exposures. Control leads are placed in the center top section with AC and DC power distribution cables running in the rear top section.

2.05 Buses are made up of twisted pairs of standard switchboard cable as shown in Fig. 3. Each individual pair is terminated at each end in a 100-ohm bus termination resistor. The resistors are mounted in blocks on end guards at the end of frame rows. For reliability, the termination resistors associated with the 0 and 1 buses are located in different end guards.

2.06 All buses are grounded at one point by a balanced inductor grounded at the midtap. The maximum cable length between a balanced inductor and the farthest cable receiver is 450 feet for peripheral buses and 100 feet for store buses.

2.07 Inputs to each bus are fed through cable drivers. Signals from within the frames are amplified by cable-driver amplifiers and cable-driver output transformers. The output transformer is connected in parallel across the bus pair.

2.08 Outputs from each bus are fed through cable receivers. These have low-impedance cable receiver transformers located such that they connect in series with bus pairs. The transformer feeds through a cable receiver amplifier into the unit at its destination. Bus transformers are incorporated in terminal blocks (Fig. 4) located on each unit frame.

2.09 Cable drivers may be grouped together on one bus pair and receivers may be located at both ends, but receivers cannot be placed in the center with drivers at both ends.

2.10 End guards, 4 inches deep, are used at main aisle ends of frame lineups. Each end guard has a swinging door to give access to cables, bus termination resistors, holders for spare fuses, and other equipment. An aisle alarm lamp, an aisle directory which lists equipment frames located on the aisle, and a light switch which controls aisle lighting are mounted on the end guard swinging door. Whenever one or more frames are omitted in a lineup, each exposed end of a frame is dressed with an end guard 2 inches deep, except where a frame is within 8 inches of a column. When terminating resistors are required at both ends of a lineup, the 4-inch deep guards are used at each end.

2.11 A miscellaneous circuit (SD-1C110-01) is associated with every frame in the SPC lineup. With some exceptions, this circuit provides filters, fuses, and means of power removal for these frames. Abnormal conditions within the frames are reported to the system via scan points while also providing visual alarms and initiating audible ones. The miscellaneous circuit also provides appliance outlets, test pin voltage jacks, and a means of communicating between frames.

2.12 Head telephone sets, frame line telephone (TEL) jacks, and the local frame line circuit provide the means of communicating between frames in the SPC office. The TEL jacks are located, in most cases, on the extreme left-hand side of the frame control panel. The local frame line circuit is located in the CD bay of the CD-PT-TTY frame.

TABLE A

**BASIC SPC NO. 1A FRAME REQUIREMENTS
(EXCLUDING STORE FRAMES)**

FRAME	MINIMUM NUMBER
Processor	2*
Master scanner	1
Signal distributor	1
Central pulse distributor	2*
Control and display, program tape unit, teletypewriter	1

* These numbers include duplication.

TABLE B

MAJOR SPC NO. 1A EQUIPMENT DOCUMENTATION

UNIT	CD AND SD NO.	SECTION NO.
Processor	1C101-01	254-100-101
Control and display	1C107-01	254-106-301
Program tape unit	1C108-01	254-107-101
Program tape unit	1C396-01	254-107-102
Teletypewriter	1C106-01	254-105-101
Master scanner	1C105-01	254-103-101
Signal distributor	1C104-01	254-104-101
Central pulse distributor	1C103-01	254-102-101
Store (PBT)	1C102-01	254-101-101
Store (semiconductor IGFET)	1C602-01	254-101-103

The head telephone sets, when plugged into the TEL jacks, complete the talking path.

2.13 The spare (SP) jack circuit provides a 3-wire belt line around the office for miscellaneous

use. The SP jack is located on the frame control panel next to the TEL jacks.

2.14 Test pin jack circuits provide ground (GND), high-resistance ground (HRG), and -48 and

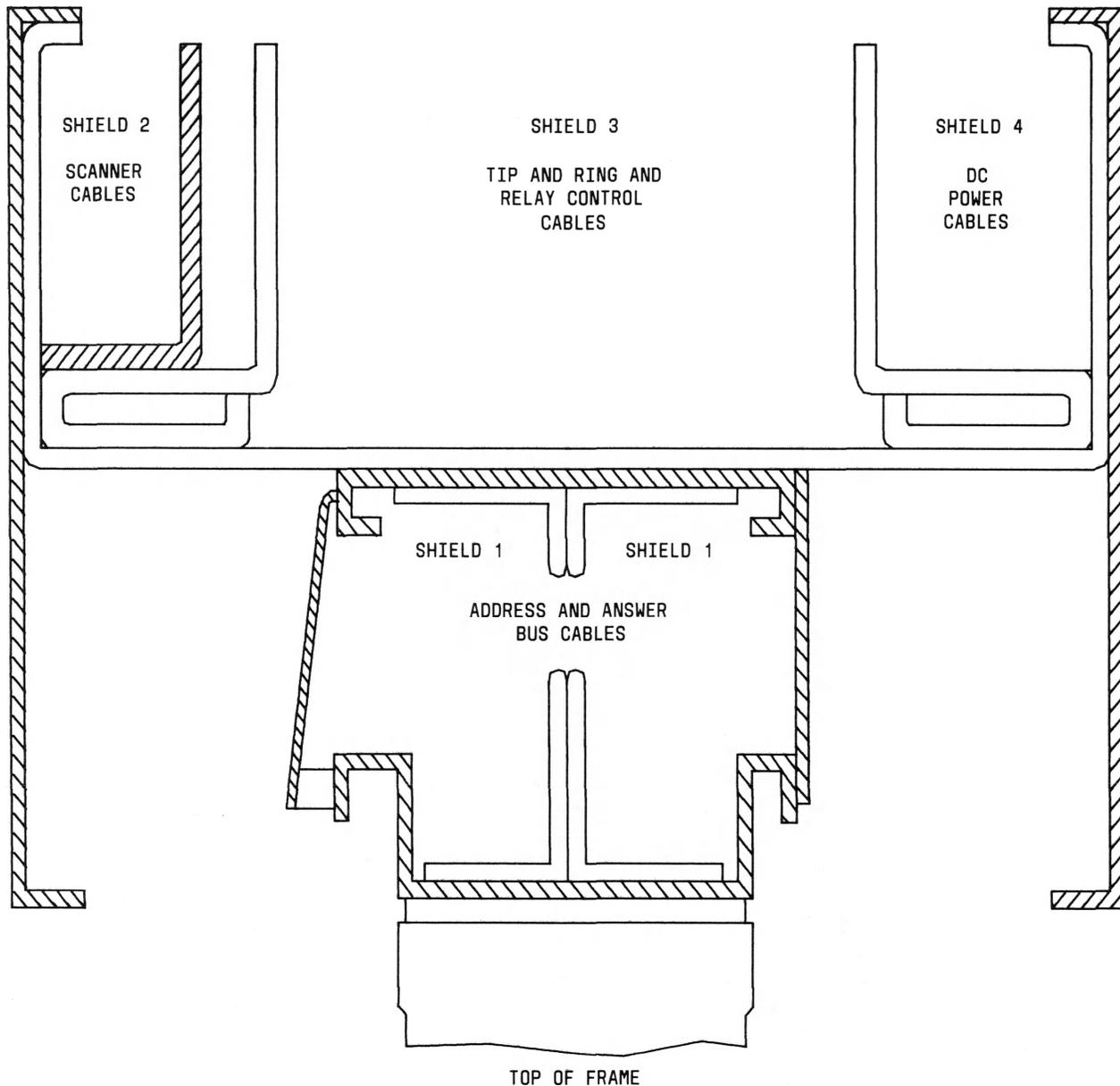


Fig. 2—Cable Rack (Sectional View)

+24 volt batteries for testing in the frames. These jacks are located on the frame control panel and have access from both the front and back of the panel.

2.15 Duplex appliance outlets, which are part of the miscellaneous circuit, are located on the front and rear base of the SPC frames, where required. These outlets supply 120 volts AC at the frame locations.

2.16 Filters, fuses, and fuse alarm circuits in the miscellaneous circuit monitor and control voltages supplied to various SPC frames. Nonalarm fuses provide voltages to various lamps and displays located on the frames.

2.17 Except for the semiconductor IGFET store units, SPC No. 1A equipment units contain A-type CPs. A-type CPs are plug-in printed wire board assemblies. Figure 5 shows the A-type CPs with an apparatus mounting. The CPs in each bay

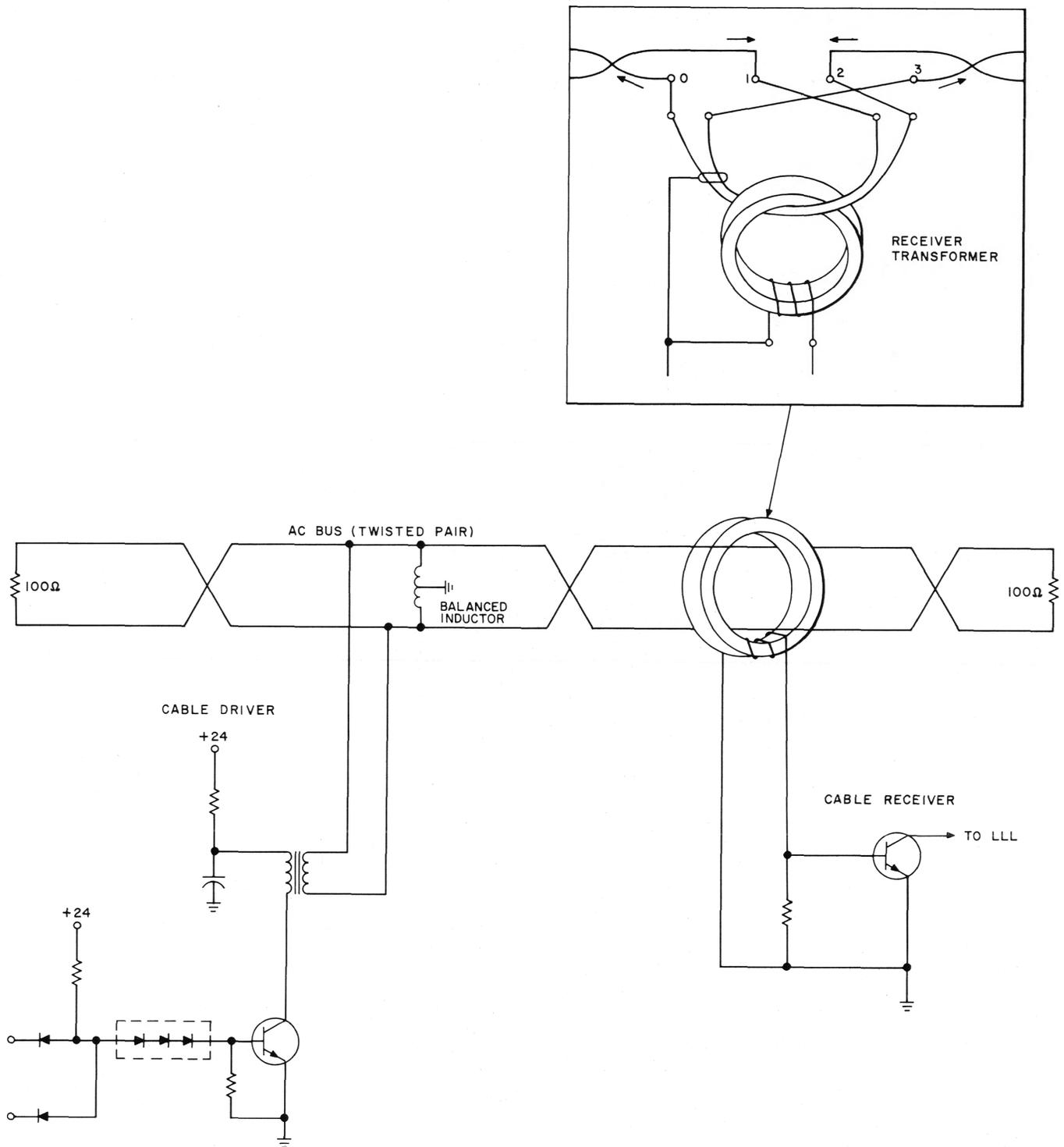


Fig. 3—Interframe Communications System Detail

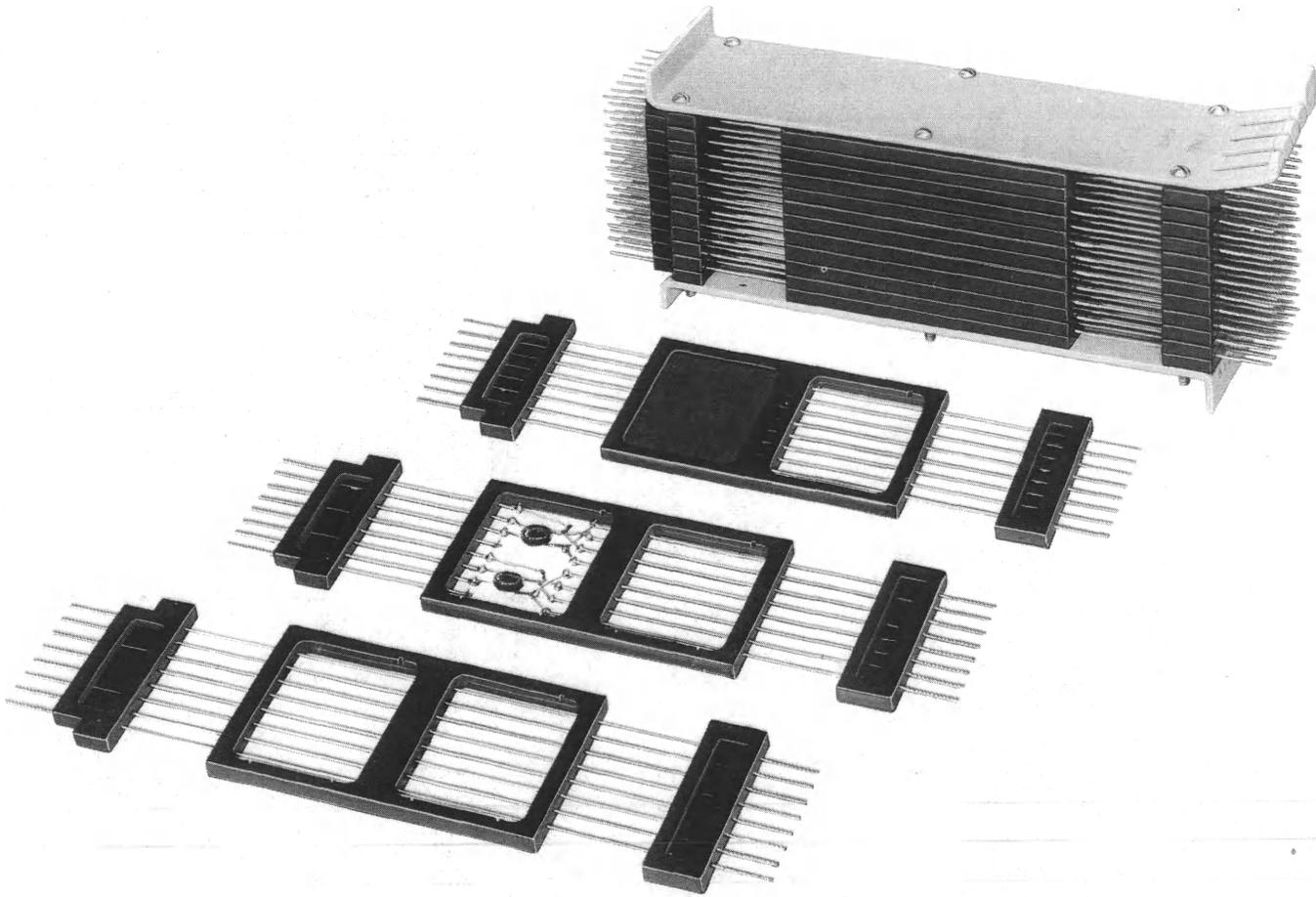


Fig. 4—Bus Transformer and Terminal Block Assembly

of each equipment frame are arranged in groups to make up functional units of SPC No. 1A equipments.

2.18 Each CP apparatus mounting has a hinged designation strip across the top with designation cards, front and rear, to show the position in the mounting, the apparatus code, and the color code for each CP. CPs are physically, but not electrically, interchangeable. Each CP bears one of three color codes: red, yellow, or blue. No damage will be done if a wrong apparatus code is plugged into a connector with the same color if the color is yellow or blue. Damage **can result** if red CPs are interchanged; extra care is required with them to make sure that the proper code is inserted in any red location.

2.19 Semiconductor IGFET store units contain a new series of circuit packs and backplane connectors. These include JK-type circuit packs

and 947C connectors. For more information on these circuit packs and connectors, refer to Section 254-101-103.

2.20 Power is supplied to the SPC No. 1A equipment frames via a power distributing frame (duplicated for reliability), which is part of the application system equipment.

2.21 Special frame insulating procedures are followed in the SPC No. 1A to avoid electrical interference from stray ground potentials. Frames for the SPC No. 1A, together with frames of the electronic system in which it is incorporated, are grounded from a single point. Except at this point, grounding of frames of the SPC No. 1A and its application system is separate from the grounding of:

(a) Commercial power

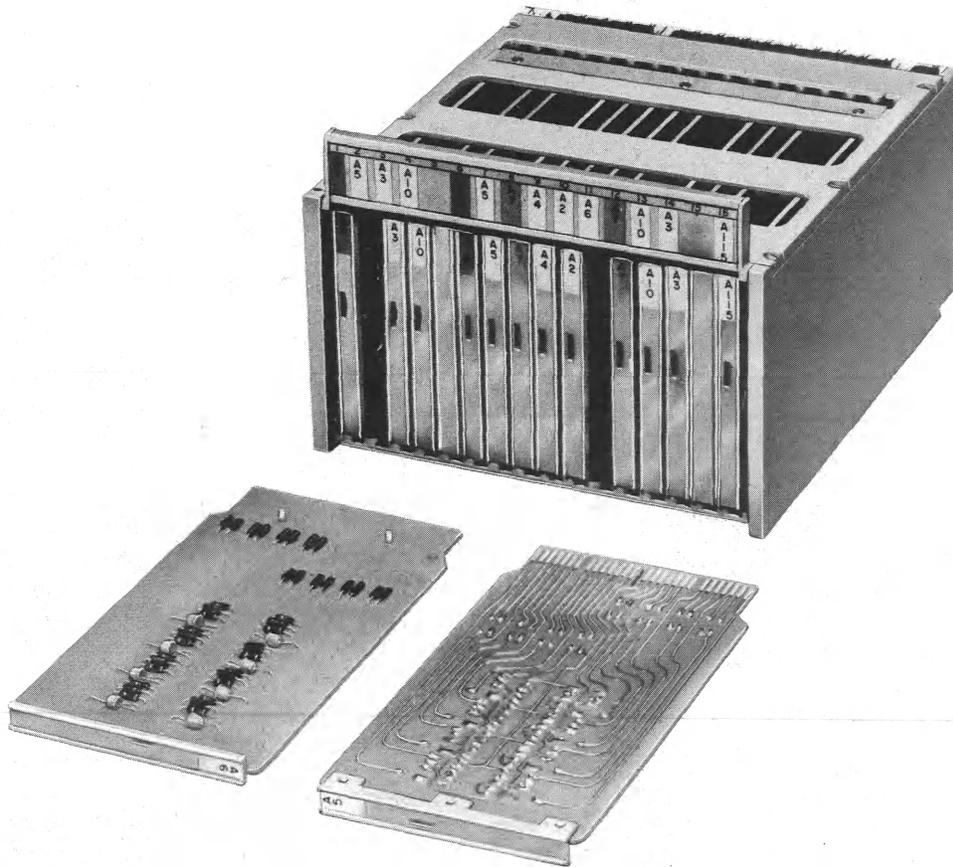


Fig. 5—Type A Circuit Packs With Apparatus Mounting

(b) Protector frames

(c) Frames of common systems and of other systems (in the same building) that are powered from other than an Electronic Switching System (ESS) type power plant.

2.22 All frames and cable racks of the SPC No. 1A and its application system are insulated from the building. All the frames are connected together by ground feeders between the frames and the power distributing frames. In addition, a No. 6 copper wire, run in the cable rack, provides a secondary grounding network for all frames. A ground lead is run between the SPC No. 1A (and its application system) central grounding point and the central office building ground.

2.23 Frames are insulated from the building by the use of leveling blocks made of insulating material and by the use of insulating bushings and washers around each bolt that secures frames to the floor.

2.24 Cable racks (and conducting cable sheaths) from any uninsulated frames, including protector frames, frames in the power room, and frames in other switchrooms (or other switchroom areas), are insulated from the insulated frames either by interruption or by insulating pads and insulating fastenings.

B. Processor

2.25 The processor is a 3-bay frame, 7 feet high and 6 feet 6 inches wide (Fig. 6) which contains circuits for the logic, clock, and processing functions of the SPC No. 1A. Approximately 1800 A-type CPs are used in one processor frame. Groups of these CPs make up the various functional units of the processor (Fig. 7). The following is a brief description of the circuitry in each functional unit.

2.26 *Inductors, Transformers, and Terminal Strips:* The inductors, transformers, and terminal strips provide balance, coupling, and

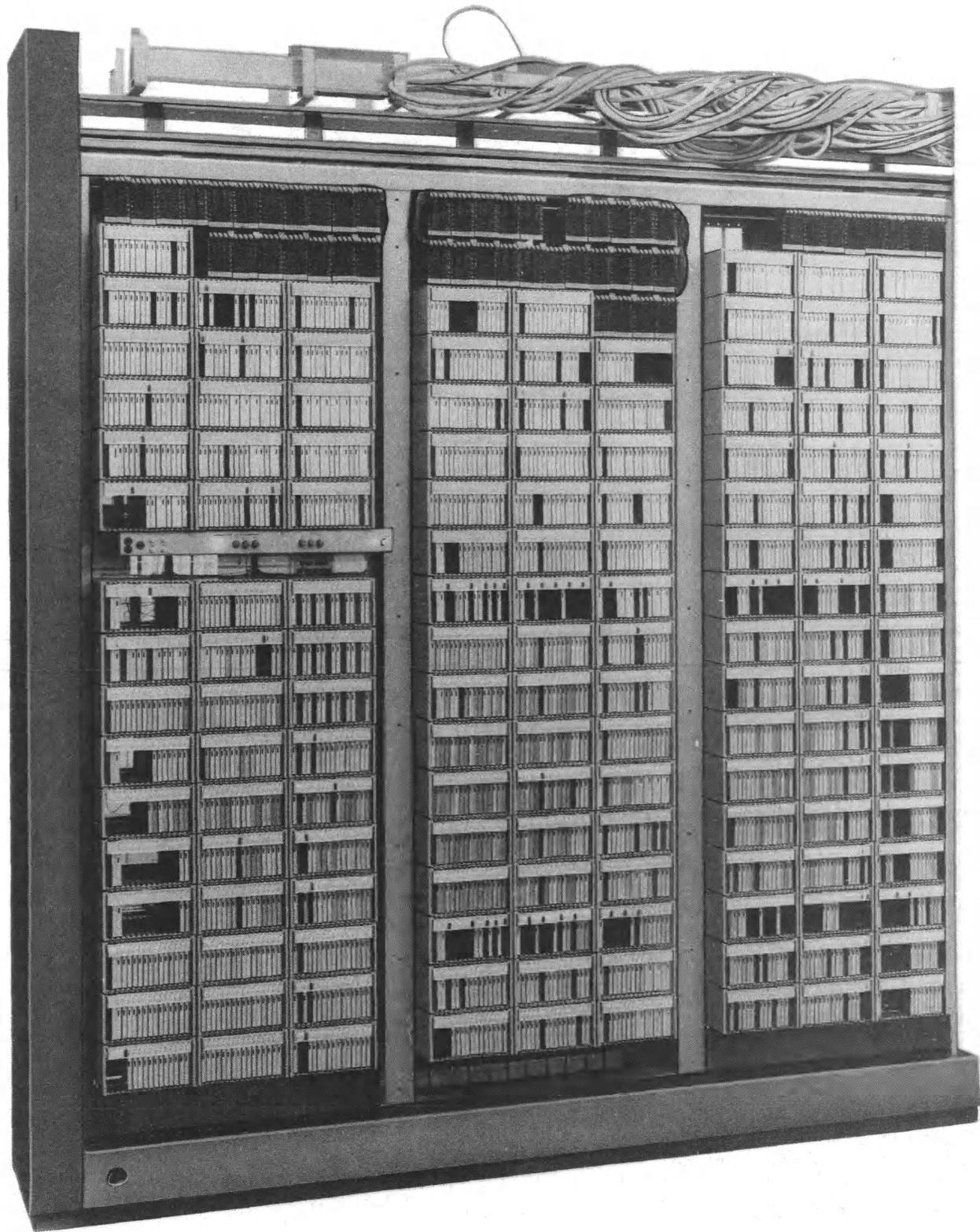


Fig. 6—Processor Frame

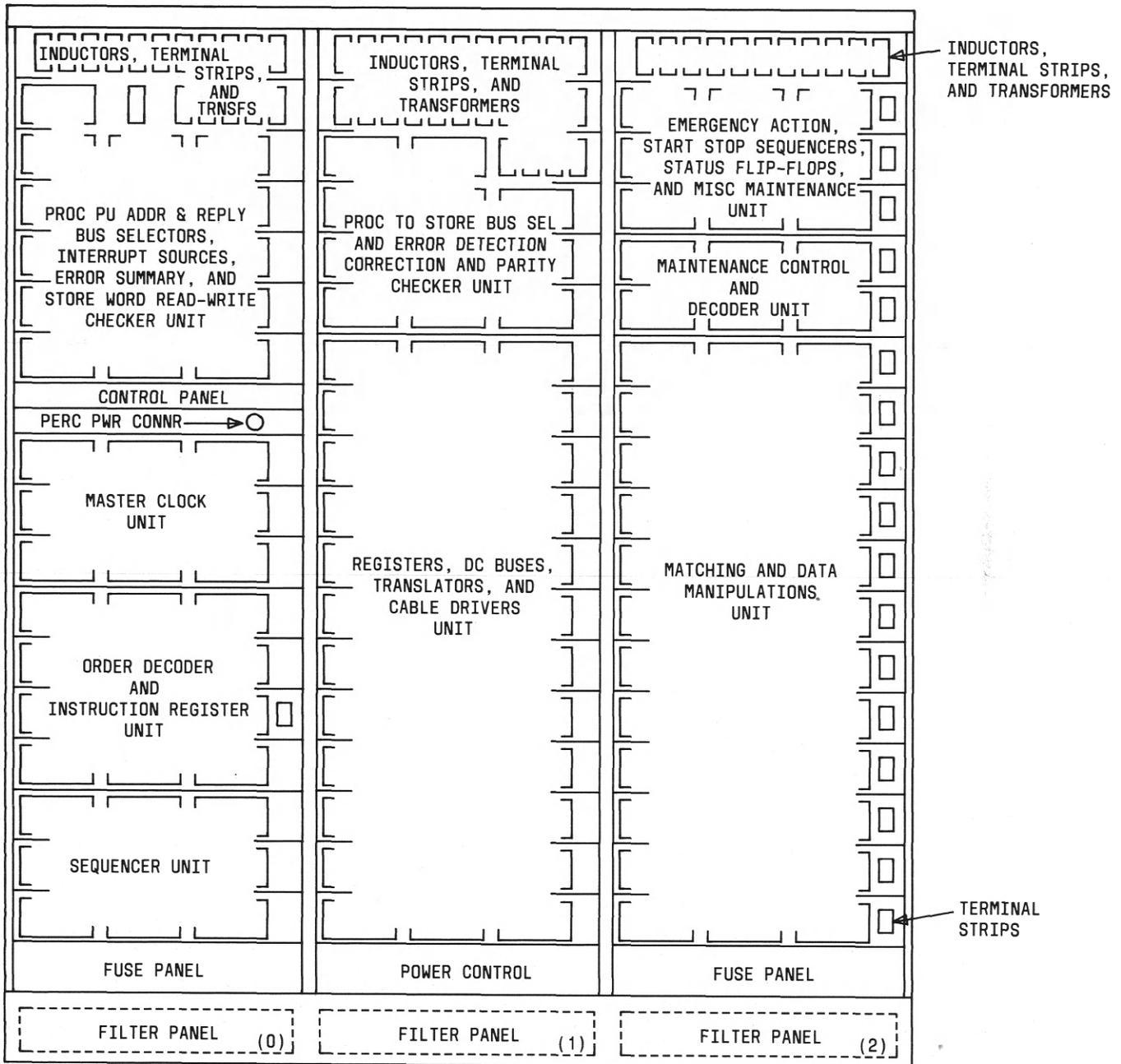


Fig. 7—Processor Frame Elements

termination, respectively, for the buses between the processor and external equipment.

2.27 Processor Peripheral Unit Address and Reply Bus Selectors, Interrupt Sources, Error Summary, and Store Word Read-Write Checker Unit: The processor peripheral unit address circuit is used to select and enable the SPC No. 1A and application equipment. The reply bus selectors determine which of the duplicated buses (1 or 0) connects the peripheral equipment to the processor and which bus will supply data to the processor. The interrupt sources are used to control normal and maintenance level interrupts and to monitor the processor for certain troubles. The error summary and store word read-write checker provides error control of data transmitted between the processor and stores.

2.28 Processor Frame Control Panel: The control panel, located on bay 0 of the processor frame, contains jacks, controls, and indicators used during operation and maintenance of the processor.

- (a) By use of a telephone set, the TEL jacks provide access to the local frame line for voice communications.
- (b) The SP jack provides access to the 3-wire local belt line circuit for local maintenance use.
- (c) The GRD, HRG, and +24 jacks are used for testing. Access to these jacks can be from either the front or rear of the control panel.
- (d) The FRAME CONTROL—OS (out-of-service) lamp is lighted to indicate that the processor is removed from service.
- (e) The FRAME CONTROL—OFF key removes power from the processor cable drivers, CPs, and relays.
- (f) The FRAME CONTROL—REQ INH (request inhibit) key initiates a program-controlled verification of the processor's operational status to prevent both processors from being inoperative simultaneously. TTY output messages verify the appropriate action. The REQ INH key also provides a mechanical interlock between the FRAME CONTROL—OFF and NOR keys.
- (g) The FRAME CONTROL—NOR key provides circuit paths required during a power-up procedure.
- (h) The ST (start) key applies power to the cable drivers, CPs, and relays. It also alerts the program of the intent to turn on power.
- (i) The CLK ST (clock start) key enables the clock system of the processor and alerts the program that power is restored and that the clock is operational.
- (j) The OFF NOR lamp is lighted to indicate that the FRAME CONTROL—REQ INH or OFF key is operated.
- (k) The PWR OFF lamp is lighted to indicate that processor power has been removed manually or as the result of a fuse failure.

2.29 Master Clock Unit: The master clock provides the timing required to execute program instructions and other related functions.

2.30 Order Decoder and Instruction Register Unit: The instruction register supplies instructions to the order decoder. The order decoder translates these instructions into a set of DC states which cause the specific action required by the instructions.

2.31 Sequencer Unit: The sequencer unit supplements the control of instruction processing in conjunction with the order decoder.

2.32 Processor to Store Bus Selector and Error Detection Correction and Parity Checker Unit: The processor to store bus selector determines the bus configuration from the stores to the processor. The error detection correction and parity checker monitors the memory access register (MAR) for bit errors and parity errors in the data received from the stores. It also provides limited correction of this data when an error is detected.

2.33 Registers, DC Buses, Translators (CPD Address), and Cable Drivers Unit: The registers store data being gated between internal circuits of the processor. A common DC bus system enables data to be manipulated between the registers and associated circuitry. The translators (CPD address) translate

processor data into codes which are used to enable the CPD. The cable drivers provide coupling, isolation, and amplification of data being transmitted from the processor to external circuits.

2.34 Emergency Action, Start-Stop Sequencers, Status Flip-Flops, and Miscellaneous Unit:

The emergency action circuit reconfigures the processors and stores when the processor program deviates from its ordered sequence so that the processor is unable to recover to normal operating sequence. After store-processor reconfiguration occurs, the emergency action circuit verifies that the configuration is operational. The start-stop sequencers are used during the off-line mode to stop an off-line processor. They also restart the processor from the state it was at when stopped. The status flip-flops, which are controlled by the CPD, MCC, and internal processor circuits, direct various processor operations. The miscellaneous maintenance circuit is a group of flip-flops used to control various processor maintenance functions.

2.35 Maintenance Control and Decoder Unit:

The maintenance control and decoder unit controls and executes matching operations in the processor.

2.36 Matching and Data Manipulations Unit:

The matching circuit provides access to maintenance matching circuitry; and the data manipulation circuits provide the shift, rotate, mask, test logic, and logic operation functions of the processor.

2.37 Power Circuitry: Each bay of the processor is supplied +24 volts by power feeders from the power distribution frame. Power is supplied to the processor through three filter panels, one located in the base of each bay. Components on these panels protect the processor from voltage surges and noise. A contactor on each filter panel controls input power to the fuse panels. Fanout of individual power lines to the internal processor circuitry and protection of internal circuitry are provided by two fuse panels, one located near the base of bay 0 and the other near the base of bay 2. DC-DC converters located throughout the processor provide +4.5 volts required to power the logic circuits. A power control panel, located near the base of bay 1, contains relays used to control and monitor processor power.

2.38 Processor Emergency Recovery Circuit (PERC) Connector:

The +24 volt power from the processor is used to supply operating voltage to the PERC unit (used with the dead start feature effective with PG-1C002). A jack (labeled PERC) on the processor connects the power circuits via cables to the PERC unit. The PERC (which is a portable test set and not part of the frame) is used to control and monitor the processor during catastrophic failures.

2.39 Two processor frames (P0 and P1) are required in each SPC No. 1A office. The system is under control of only one processor (called the active processor) at any time. The second processor (called the standby processor) operates in parallel with the active processor to execute identical instructions derived independently from independent duplicate stores.

2.40 The standby processor provides continuous checks of operations for the active processor through the use of DC matching (**maintenance matching**). If a trouble occurs in the active processor, the standby processor assumes control of the system to assure the continued execution of system functions.

2.41 Figure 8 illustrates the processor matching system. It consists of two independent matching units, matcher A and matcher B. The match control is a buffer bus register which is controllable through a memory write instruction. This register controls the match sources which are to be used, the times at which the matches will occur, and the action to be taken on an abnormality. The A matcher unit in each processor is capable of matching any one of five groups of data against the same information in the other processor.

2.42 Each of the five groups may contain as many as 24 individual bits. The selected group of bits in each processor is gated from the source to the A match register. This 24-bit register provides inputs to the 24-bit logical matcher which is located only in processor 0. The match result is then gated over a DC connection to the control circuitry in each processor for subsequent action. The B matcher operates identically though independently with the exception that it can sample any one of six different groups and the match for this unit takes place in processor 1. The match sources provide access to strategic points within the processor such as buses, decoders, and sequencers.

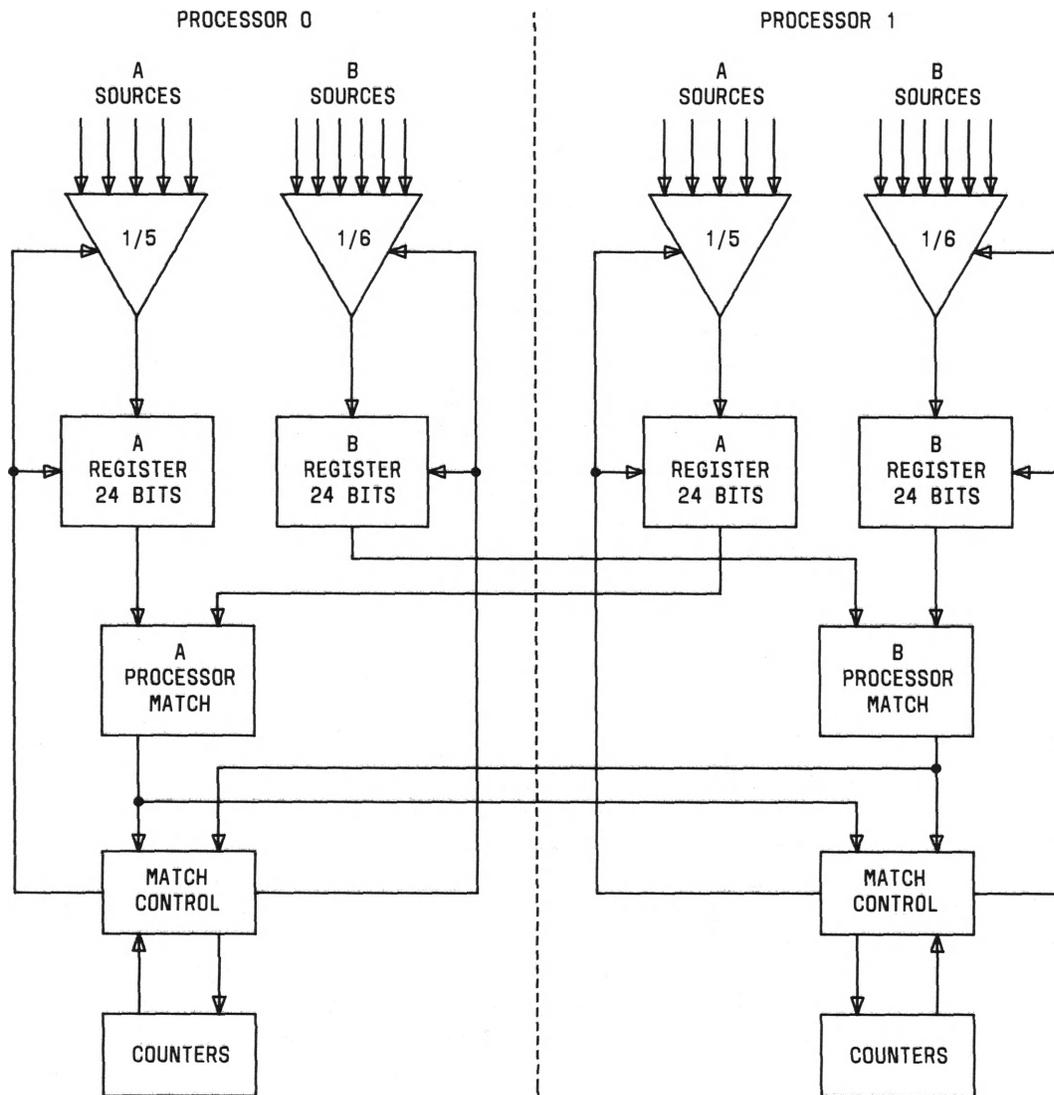


Fig. 8—Processor Matching System

2.43 The match control counters consist of a cycle counter, a phase counter, and a multipurpose counter. The cycle counter is automatically set to zero at the beginning of each instruction and incremented once for each cycle of that instruction. The phase counter is basically a modulo-3 counter which is incremented on each of the three clock phases during a complete $6.3 \mu\text{s}$ cycle. The multipurpose counter can be controlled to count cycles over many instructions or may be used to count instructions from some predetermined starting instruction.

2.44 When the results of the match operation indicate a malfunction, the match registers

and counters are inhibited from further operation. All of these circuits are registers which may be interrogated with a read instruction. The match registers and counters are frozen with the data which caused the abnormality. This information is used by the maintenance program in detecting and isolating hardware faults.

2.45 The matching system may be operated in either the sample match mode or the directed match mode. In the sample mode, a single match is taken in one or both of the matcher units at a previously designated cycle and phase of an instruction as specified by the match control. This mode is terminated as soon as the match is taken,

with the match registers containing the sampled data.

2.46 When the directed mode is used, the match control establishes sources and times for sampling for each matcher unit. Samples may be taken in any or all of the three phases of each cycle. The selected sources are then matched at the specified phases until the mode is terminated by an abnormality or by program control. The directed mode is active during normal operation with DC buses specified as the sources, and a match is taken during each of the three phases. Virtually all the pertinent data associated with the execution of an instruction passes over these buses, so a malfunction will be quickly detected.

2.47 The control section may be initialized to react to either a match or a mismatch as an abnormality. When an abnormality occurs, all subsequent gating of information to a destination register is normally inhibited. Since essentially no registers change during the instruction, it is a relatively easy matter to retry the instruction under control of a maintenance program. In addition to this inhibit there are two different switching actions which may be invoked on an abnormality. First the standby machine may be stopped by inhibiting all gating and decoding functions in that unit. The other choice is to initiate a maintenance interrupt request which will transfer program control to a special maintenance program. If the abnormality occurs during normal operation, the processor retrieval programs are accessed; and if it occurs during processor diagnostics, a special recording program is given control.

2.48 The processors also have the ability to read the A match register and the B match register in the other processor via DC connections. Thus, the state of the match registers in an unreliable machine may be correctly read after the occurrence of an abnormality.

2.49 This matching system provides a powerful method of detecting processor malfunctions and, together with the diagnostic program, permits isolation of the faulty hardware.

2.50 The use of DC matching requires that the two processor matching circuits be located near each other, because excessive cable lengths would introduce noise interference and time delay. To satisfy this requirement, processor 1 is placed

adjacent to processor 0 but turned around so that the wiring side of processor 1 is in the equipment aisle of processor 0 and vice versa. In this configuration, terminal strips on the two processors are only 4.5 inches apart, thus providing for the shortest possible cable lengths between matching circuits.

C. Store

General

2.51 The SPC No. 1A store system may consist of two physically different types of store units: the PBT store and the more modern semiconductor IGFET store. A store system may consist of PBT store units only, semiconductor IGFET store (effective with PG-1C003) units only, or a combination of both.

2.52 SPC No. 1A store units are always supplied in pairs (duplicated) and operated in parallel with duplicated processors. In normal operation, the information in one store unit of a pair is always an exact copy of the information in the other unit.

2.53 The number of store units required in an SPC No. 1A office varies according to the needs of the associated application system. The maximum number of store units allowable in an office is a function of the processor addressing capacity (30 store name codes), maintenance software store identification limitations (20 or 24 member numbers for the TSPS application system only), and the type of store unit configuration used.

2.54 Maintenance software identifies a physical store unit (semiconductor IGFET module/PBT store) as a member number. A member number corresponds to 16K words for a PBT store or 32K words for a semiconductor IGFET module. There is a one-to-one correspondence between name codes and member numbers for PBT stores (16K words). In the case of the semiconductor IGFET memory, however, two adjacent or complementary name codes are variably assigned to a member number since a semiconductor IGFET memory module has a 32K-word capacity.

2.55 The number of store member numbers required to cover the available 30 name codes is a function of the particular PBT-semiconductor IGFET memory configuration. The largest hybrid PBT-semiconductor IGFET memory configuration

prior to PG-1C004 is limited to 20 store units. Effective with PG-1C004 (for TSPS only), the largest hybrid memory configuration is limited to 18 PBT stores and 6 semiconductor IGFET modules which, for the 30 available name codes, correspond to a maximum of 24 store member numbers (0 through 23). The all-semiconductor IGFET memory configuration requires a maximum of 15 member numbers for the 30 name codes.

2.56 SPC No. 1A store name codes consist of five code bits and a parity bit. The code bits are capable of generating 32 different codes of which 30 are used (codes 0 and 31 are not used for store addressing). A parity bit generator located in the processor provides a parity bit according to the number of ones (odd or even) in the code. As a general example of generating a parity bit for a code of 00001, the parity bit would be a one if even parity is desired or a zero if odd parity is desired. Normally, the parity bit is formed so that an odd number of ones is present in the six bits that comprise the name code and the parity bit. This operation conforms to the odd parity convention used in the processor.

2.57 For the TSPS application system only, the SPC No. 1A processor uses even name code parity to address the station signaling and announcement subsystem (SSAS) announcement stores. The announcement stores are used to store automated announcement information for use with the automated coin toll service (ACTS) feature. The announcement stores are connected to the store bus only during loading or diagnostic testing operations. Using even parity for SSAS announcement stores doubles the number of name codes available, thus providing for future expansion capabilities on the store bus. This requires the addition of an inverse parity flip-flop to the parity bit generator to invert the name code parity of the announcement stores.

Piggyback Twistor Store

2.58 Equipment for the PBT store unit is contained in a 2-bay frame, 7 feet high and 4 feet 4 inches wide (Fig. 9). The frame base is 12 inches deep and houses AC appliance outlets, front and rear, and three frame battery supply filters that eliminate noise picked up by the power feeders.

2.59 Bay 0 of the frame contains four surface-wire units and the filter panel. From top to

bottom the four units are the AC bus input, control, and register unit; AC bus output, data register, and write unit; readout and write unit; and diagnostic and power supply unit.

2.60 Bay 1 contains two surface-wired units mounted in the top positions of the frame to perform access functions. The access and bias current regulator unit at the top of the bay contains five plug-in current regulators which supply constant current for read and write operations and bias for the PBT modules. The access unit mounted directly under the current regulator unit contains CPs which provide access switches for selecting a word location in memory.

2.61 Bay 1 also has a 2-inch high control panel which contains test jacks, keys for power control, and lamps to indicate operational status of the frame. A power control unit and fuse panel unit, for power distribution to functional units on the frame, are mounted in the lower positions of bay 1.

2.62 Four PBT modules, requiring 34 inches of bay height, are mounted at the center of bay 1. Each module has the capacity to store 4,096 words, 47 bits in length, with spare twistor pairs (bit pairs) provided for field maintenance. If a twistor pair becomes inoperative, it can be replaced by a spare twistor pair. A description of the change should be recorded on a designation card which is provided with the frame. These designation cards are located to the left of each module.

2.63 The four PBT modules contained in bay 1 have a combined capacity of 16,384 words, 47 bits in length. These four modules combined make up one PBT store unit, which is assigned one store name code. PBT store frames are always supplied in pairs for reliability.

2.64 The PBT store unit has the following desirable characteristics:

(a) **Electrical Alterability:** Contents of the PBT store can be changed by means of electrical pulsing circuitry which operates at electronic speeds.

(b) **Nondestructive Readout:** Reading from the PBT store can be accomplished without destroying its contents.

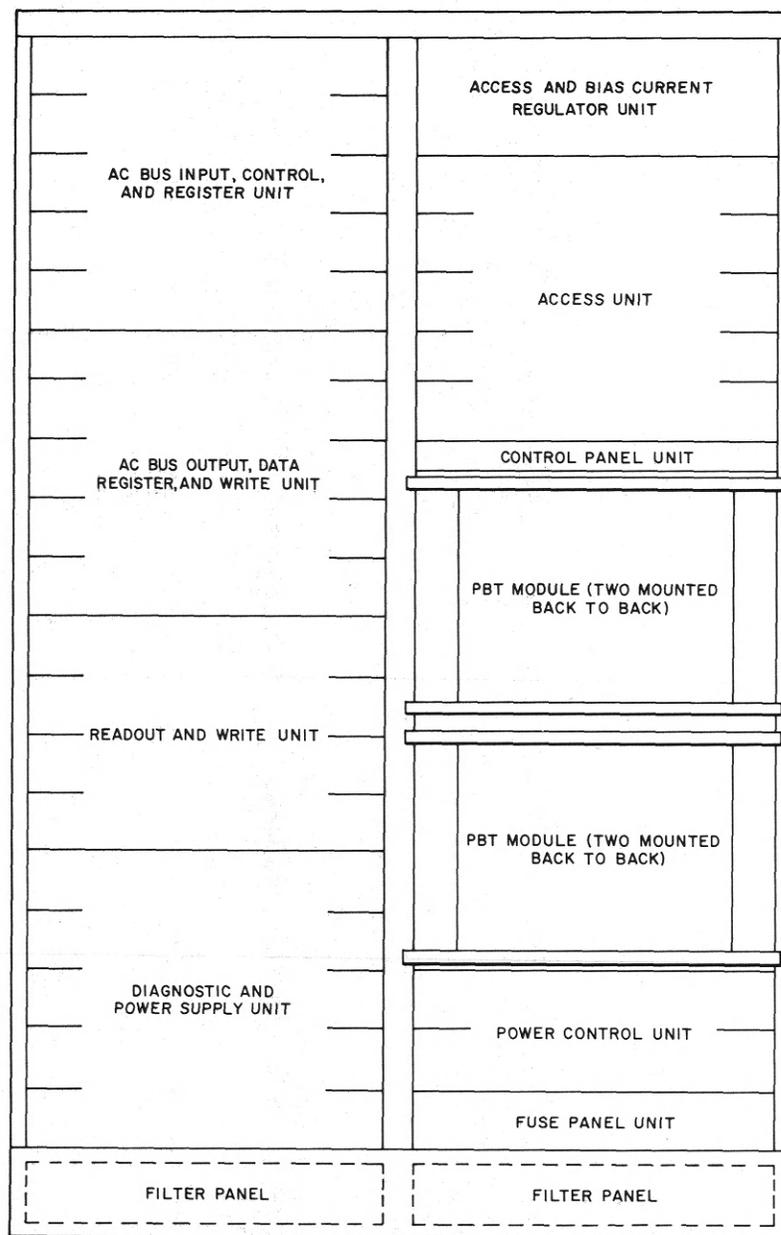


Fig. 9—PBT Store Frame

(c) **Nonvolatility:** Loss of power to the PBT store does not result in the loss of its contents.

Semiconductor IGFET Store

2.65 Semiconductor IGFET store unit equipment is contained in a single-bay frame, 7 feet high and 2 feet 2 inches wide (Fig. 10). There can be a minimum of one and a maximum of six

memory modules per frame. The frame also contains a bus unit, store controller, logic unit, power control panel, fuse panel, and filter unit. A brief description of the circuits on the store frame follows.

2.66 Bus Unit: The bus unit consist of transformers and terminal strips. It interfaces the store frame with the AC bus.

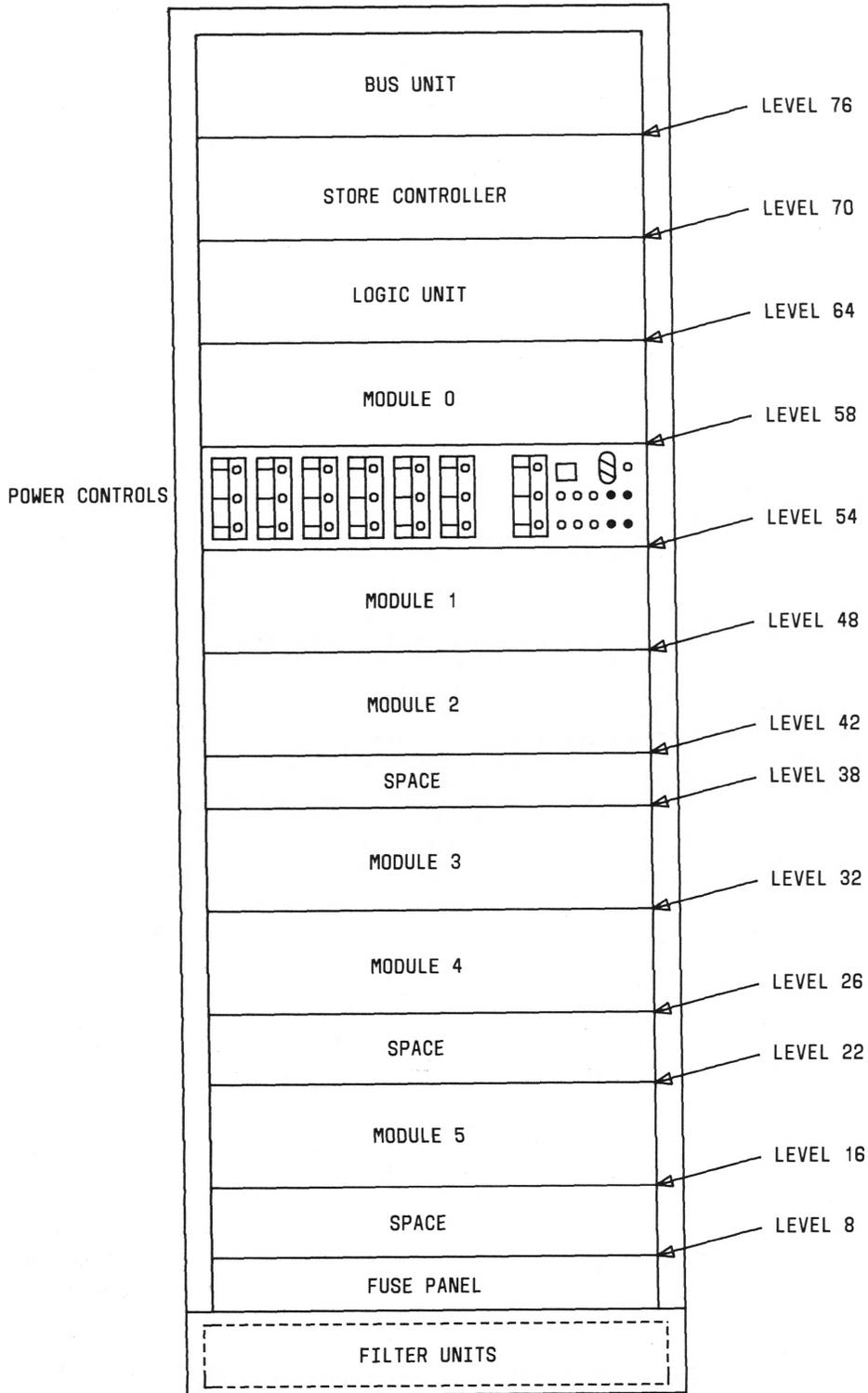


Fig. 10—Semiconducter IGFET Store Frame

2.67 Store Controller: The controller unit provides a common interface between the store bus and all memory modules on a store frame. This unit is comprised of four mounting plates. The first two plates contain the common control circuits for the frame. The third mounting plate is the first memory module that is always provided on the store frame. The fourth mounting plate is the power control panel.

2.68 Logic Unit: The logic unit consists of a sequencer, data and address registers, module administration (MAD) CPs, power related CPs and an optional read-only memory (ROM) (which contains a simplified bootstrap program and is provided only when store name codes 01 and 36, containing the system bootstrap program, are implemented with semiconductor IGFET stores).

2.69 Power Control Panel: The power control panel provides the capability for turning power on or off the controller or an individual memory module.

2.70 Fuse Panel and Filter Units: The fuse panel and filter units monitor and control voltages supplied to the frame by the power distributing frame.

2.71 Memory Module: A semiconductor IGFET memory module is a 6-inch high mounting plate containing 24 memory planes, 2 power supplies, and 2 fanout boards. Each memory plane contains 32,768 words by 2 bits. The complete module has a capacity of 32,768 words by 47 bits (the 48th bit is not used). The 2 power supplies provide voltages needed by the memory module CPs. The fanout boards receive and check addresses from the store controller and drive the address inputs of the memory planes.

2.72 Each memory module may be divided into two protected areas and two unprotected areas. "Write" operations into protected areas are controlled by switch settings on MAD CPs. Address bits are compared to settings on these manually set switches to gain access. The unprotected area is that portion which is constantly being read or written into during normal operation of the store unit.

2.73 Each semiconductor IGFET memory module, consisting of 32,768 words, is addressed as two 16,384-word blocks of memory (name codes).

Each semiconductor IGFET store name code (block of 16,384 words) is functionally equivalent to a PBT store name code. The two name codes assigned to a semiconductor IGFET module can be either adjacent or complementary.

2.74 The semiconductor IGFET store unit has the following characteristics:

- (a) **Electrical Alterability:** Contents of the semiconductor IGFET memory can be changed by means of electrical pulsing circuitry which operates at electronic speeds.
- (b) **Nondestructive Readout:** Reading from the semiconductor IGFET store can be accomplished without destroying its contents.
- (c) **Small Size:** By using the semiconductor IGFET store, floor space requirements can be considerably reduced (over the requirements when PBT memory is used).
- (d) **Volatility:** Loss of power to the semiconductor IGFET store results in the loss of its contents.

D. Central Pulse Distributor

2.75 CPD equipment is contained in a single-bay frame, 7 feet high and 2 feet 2 inches wide (Fig. 11). The CPD has two equally important functions: to send unipolar pulses that are used to enable various peripheral units and to send bipolar pulses to change the state of a flip-flop or operate a logic circuit in a peripheral unit. The CPD frame is composed of the following functional units.

2.76 CBT or PFT: Located at the top of the CPD frame is the CBT for TSPS or the PFT for ETS or STP.

2.77 Communication and CPD Matrix Output Unit: Outputs of the CPD are on a terminal strip field located just below the CBT or PFT. Terminals of the terminal strip field are identified by the same number as the CPD point in the matrix to which the terminal is wired. CPD matrix assignments of unipolar and bipolar points for various SPC No. 1A units are specified in SD-1C119-01. For any office, certain points are fixed; i.e., in all offices, these points are assigned to the same function.

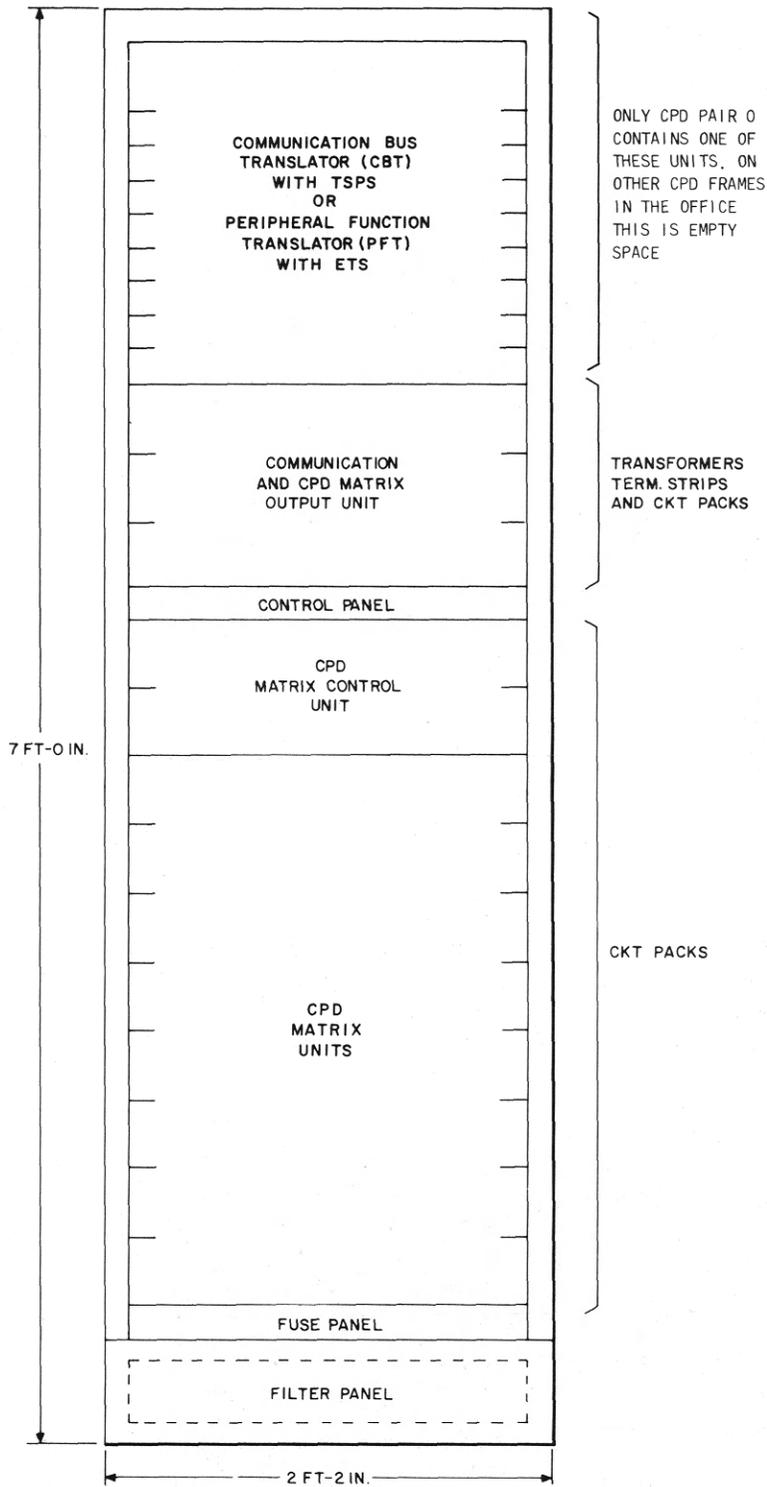


Fig. 11—Central Pulse Distributor Frame

2.78 CPD Control Panel: The CPD control panel contains jacks, controls, and indicators used during operation and maintenance of the CPD and CBT or PFT. The jacks, controls, and indicators used with the CPD are described below:

- (a) The TEL jacks provide access to the local frame line for voice communications.
- (b) The SP jack provides access to the 3-wire local belt line circuit for local maintenance use.
- (c) The GRD, HRG, and +24 jacks provide access to supply voltage and ground.
- (d) The CPD—OS lamp is lighted to show that the CPD has been removed from service.
- (e) The CPD—OFF key removes power from the CPD.
- (f) The CPD—REQ INH key requests permission from the processor to remove power from the CPD.
- (g) The CPD—NOR key restores the CPD to normal operation.
- (h) The CPD—OFF NOR lamp lights to indicate that the NOR key has been released.
- (i) The CPD—PWR OFF lamp lights to show that power has been removed from the CPD.

2.79 CPD Matrix Control Unit: The control circuitry controls the operations of the CPD in addition to performing a parity check on the enable address information.

2.80 CPD Matrix Unit: The CPD matrix unit is composed of CPs which perform various functions required in the enabling of peripheral units.

2.81 A CPD normally provides 512 unipolar and 256 bipolar outputs; however, these quantities can vary according to the system needs. The CPDs are supplied in pairs with each pair consisting of an even-numbered and odd-numbered frame. Bipolar CPD outputs must be multiplied to the other CPD of the pair to provide the redundancy of access needed to ensure system reliability.

Unipolar outputs are not multiplied from CPD to CPD, but both CPDs of a pair must be capable of enabling all associated controllers. Therefore, two unipolar outputs, one on each CPD of a pair, must be connected to each peripheral unit controller.

2.82 One pair of CPDs can supply more outputs than are needed by SPC No. 1A equipments. The spare outputs are used to enable application system equipment. For the TSPS application only, a second pair of CPDs is required to provide enough outputs. The SPC No. 1A was designed to function with a maximum of four pairs of CPDs in any one office. This provides extra capacity for system growth.

E. Signal Distributor

2.83 The SD is used in the SPC No. 1A to operate and release magnetic latching relays in response to instructions distributed by the processor. The SD acts as a buffer between the high-speed processor and those circuits having low-speed relays controlled by the processor. The SD applique circuit provides the means by which the processor, acting through the SD circuit, can close a metallic path to operate relays, lamps, etc.

2.84 The basic 256-point master SD (Fig. 12A) is mounted on a 7-foot high, 2-foot 2-inch wide equipment frame (SD00) which includes the following units: communication bus and terminal strip unit, control unit, relay matrix, frame control unit, store monitor lockout units, and SD applique units. A fuse panel and a filter panel (part of the miscellaneous circuit) are mounted at the bottom of the frame. A description of each of the functional units follows.

2.85 Communications Bus and Terminal Strip: The communications bus and terminal strip unit provides termination for leads entering and leaving the SD. The SPC—PUAB leads, which bring signals from the processor to the SD, are terminated in this unit. Leads originating at the relay contacts in the SD applique and store monitor lockout units are brought directly by switchboard cable to other units of the SPC No. 1A which require them.

2.86 Control Unit: The control unit contains buffer registers and logic circuitry. The control unit stores incoming address signals for one complete SD operating cycle. The signals are then translated by the relay matrix unit to control

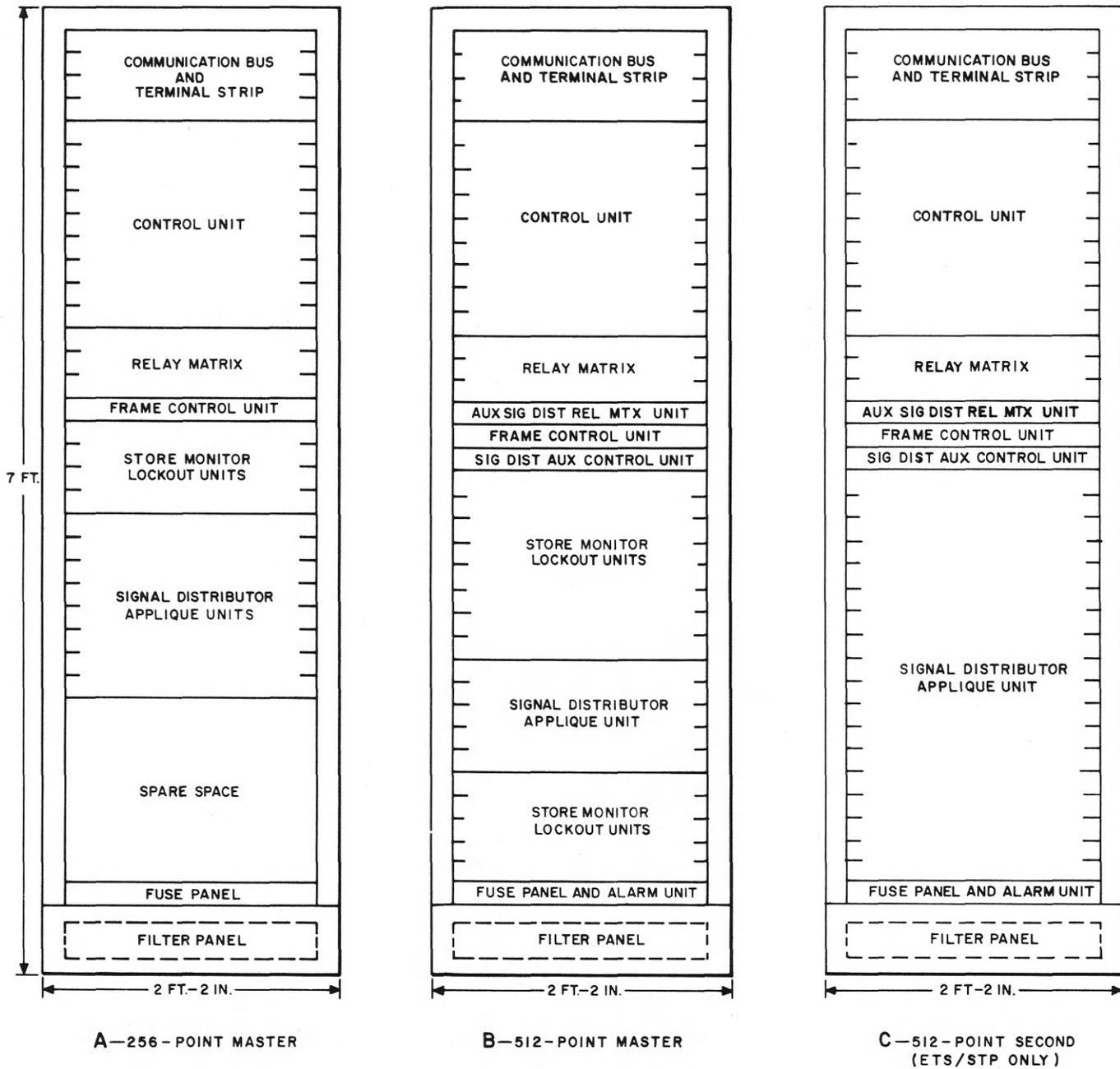


Fig. 12—Signal Distributor Frames

a particular magnetic latching relay in an applique or store monitor lockout unit. The magnetic latching relays, controlled by the SD, control other relays, lamps, and circuits in other units.

2.87 Relay Matrix: The relay matrix unit consists of a multiplicity of wire spring relays. It provides an output path selection tree

composed of several sections. A signal passing through this tree will result in a single output. This output can control one particular magnetic latching relay in an SD applique unit or in a store monitor lockout unit.

2.88 Frame Control Unit: The frame control unit is mounted on the SD frame to provide

the controls and indicators associated with operation of the SD circuitry.

- (a) The TEL jacks provide access to the local frame line for voice communications.
- (b) The SP jack provides access to the 3-wire local belt line circuit for local maintenance use.
- (c) The GRD, HRG, -48, and +24 jacks provide access to supply voltages and ground.
- (d) The FRAME CONTROL—OFF—0 and OFF—1 pushbutton keys are provided on the frame control panel so that either SD controller can be manually quarantined. These keys are interlocked so that power cannot be removed from both controllers simultaneously.
- (e) The FRAME CONTROL—OS—0 and OS—1 lamps are provided to indicate the in-service or out-of-service state of each controller.
- (f) The FRAME CONTROL—NOR key is used to restore both SD controllers to normal operation.
- (g) The BUS CONTROL—OFF—0 and OFF—1 pushbutton keys are provided to remove power from either the 0 or 1 section of the communications bus circuitry. These keys are interlocked so that power cannot be removed from both bus sections simultaneously.
- (h) The BUS CONTROL—NOR pushbutton key is used to restore both bus sections to normal operation.
- (i) Frame status lamps (OFF NOR and PWR OFF) provide visual indication of the state of the frame and the controllers.

2.89 SD Applique Units and Store Monitor Lockout Units: The SD applique units and the store monitor lockout units contain magnetic latching relays which provide loop closures to operate relays, lamps, etc., on other frames in the SPC No. 1A. Leads from the other frames in the SPC No. 1A are connected by switchboard cable to the SD frame and then are wired to the appropriate magnetic latching relay on one of the units.

2.90 The optional 512-point master SD (Fig. 12B) is also mounted on an SD00 frame. In addition to equipment units found on the basic 256-point SD00, the 512-point SD00 contains an auxiliary SD relay matrix unit, an SD auxiliary control unit, and an alarm unit (located in the same area as the fuse panel).

2.91 The 512-point second SD (Fig. 12C) is used in ETS/STP offices only. It is mounted on the SD01 frame which is equipped similarly to the optional 512-point SD00; however, this frame arrangement does not provide mounting space for store monitor lockout units.

2.92 The optional 512-point SD frame (Fig. 12B) provides additional SD points for operating relays in the SD applique and store monitor lockout units for use with a maximum of 48 store units (24 duplicated). This maximum number of store units can consist of 18 PBT store units (and their duplicates) and 6 semiconductor IGFET store units (and their duplicates). The frame arrangement mounts only enough store monitor lockout units for 26 store units (13 duplicated). The SD points for the remaining 22 store units (11 duplicated), if required, are wired to store monitor lockout units located on a miscellaneous frame.

2.93 The 512-point SD frame shown in Fig. 12C is used in ETS/STP offices to implement common channel interoffice signaling (CCIS). It provides additional SD points for operating relays in SD applique units for use in switching voice-frequency links. However, the frame arrangement only mounts enough SD applique units to accommodate 432 SD points. The remaining 80 SD points must be wired to SD applique units located on a miscellaneous frame.

2.94 The supplementary signal distributor (SSD), used in TSPS only, is mounted on a miscellaneous trunk frame (Fig. 13). The following units are mounted on this frame: communication bus and terminal strip unit, SD control unit, frame control unit, SD matrix, SD and interrupter applique units, fuse panel, and two filter panels.

2.95 The SSD provides 1000 SD points for TSPS No. 1 offices that require more SD applique and interrupter applique units than the other SD frames can provide.

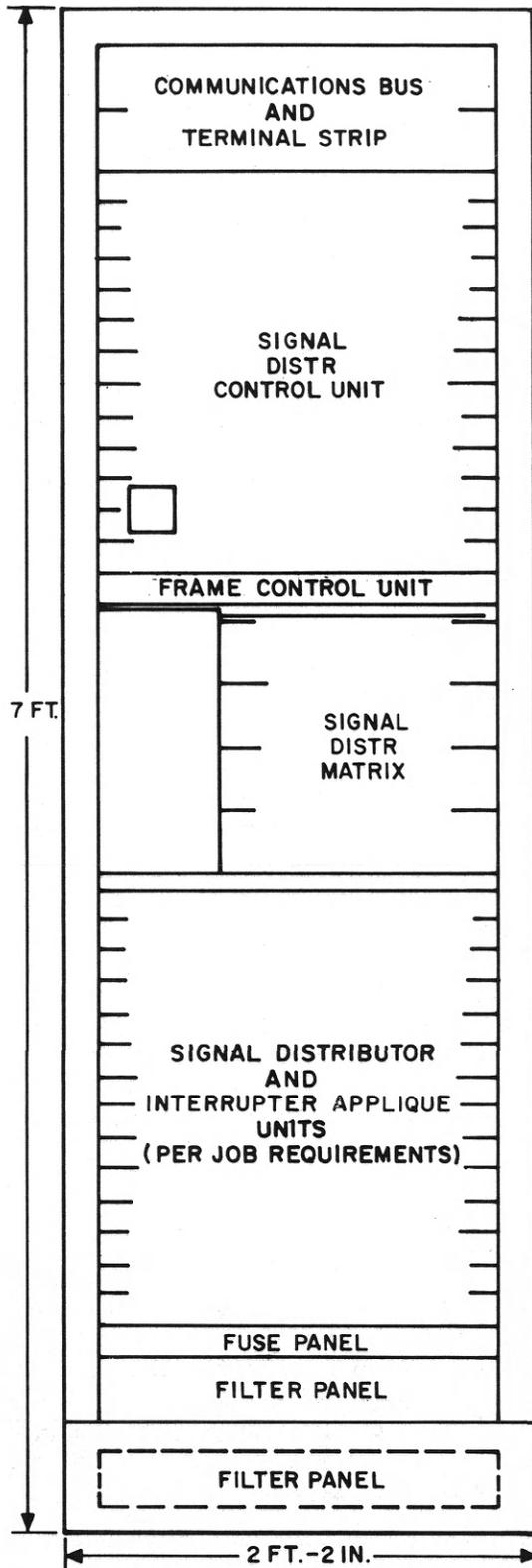


Fig. 13—Miscellaneous Trunk Frame Equipped With a Supplementary Signal Distributor (TSPS No. 1 Only)

F. Master Scanner

2.96 The SPC MS (MS00) is a single-bay frame, 7 feet high and 2 feet 2 inches wide, that provides status data to the SPC processor. Mounted on the frame (Fig. 14) are 1024 ferrod sensors plus control equipment, a frame control panel, fuse panel, and power supply filter. MS00 control equipment is duplicated for reliability. The following is a brief description of the circuitry in each MS functional unit.

2.97 Peripheral Bus and Scanner Control Unit: The peripheral bus and scanner control unit provides access to the scanner matrixes and enables interrogation and readout of a scanner row.

2.98 Scanner Control Panel: The scanner control panel provides test points, controls, and indicators used during maintenance of the scanner. The panel provides the following facilities:

- (a) By use of a telephone set, the TEL jacks provide access to the local frame line for voice communications.
- (b) The SP jack provides access to the 3-wire local belt line circuit for local maintenance use.
- (c) The GRD, HRG, +24, and -48 jacks supply test voltages and ground.
- (d) The OS-0 lamp lights when controller 0 is out of service.
- (e) The FRAME CONTROL-OFF-0 key removes power from controller 0.
- (f) The FRAME CONTROL-NOR key restores power to a controller. An additional function of the NOR key is to release the mechanical interlock between the OFF-0 and OFF-1 keys.
- (g) The FRAME CONTROL-OFF-1 key removes power from controller 1.
- (h) The OS-1 lamp lights when controller 1 is out of service.
- (i) The BUS CONTROL-OFF-0 key removes power from the scanner cable receivers

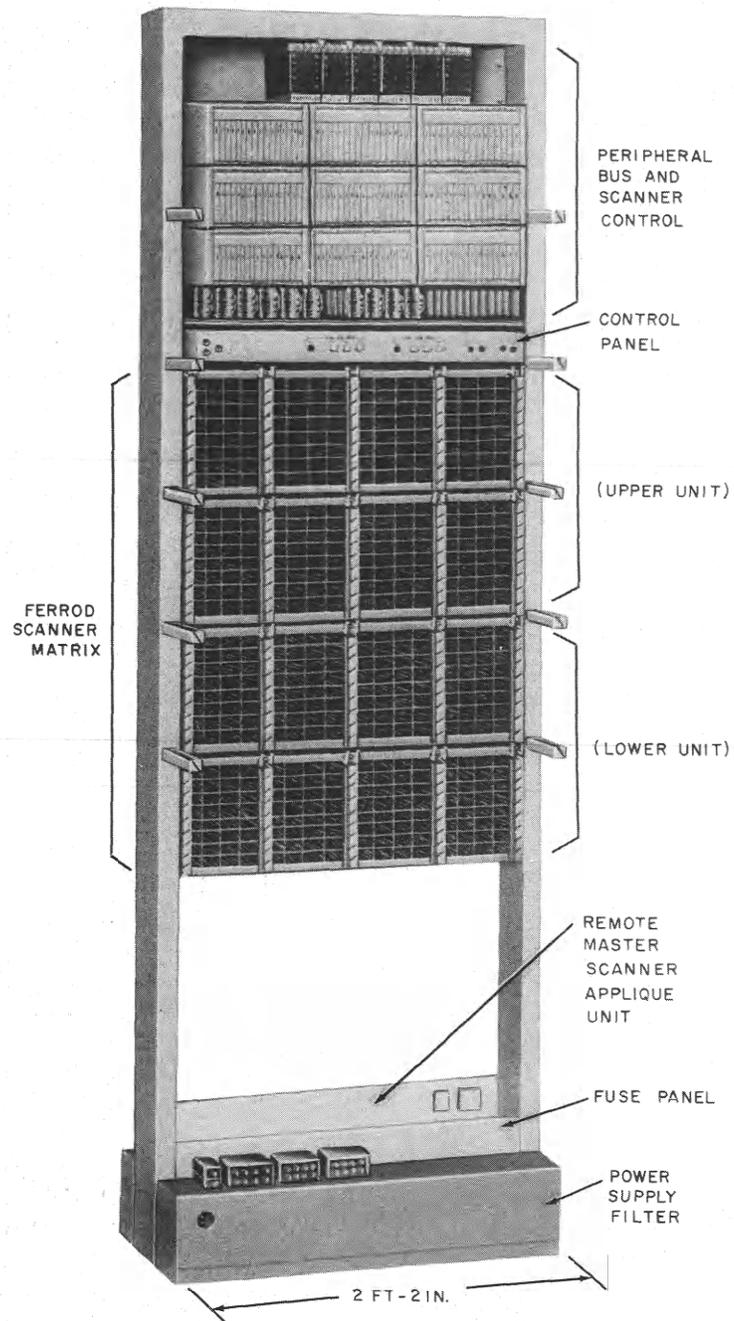


Fig. 14—Master Scanner Frame

associated with the TSPS 1/N address bus 0 or the SPC PUAB 0.

(j) The BUS CONTROL—NOR key restores power to the scanner cable receivers associated with the TSPS 1/N address bus 0 or 1 or the SPC PUAB 0 or 1. The NOR key also controls the mechanical interlock between the OFF—0 and OFF—1 keys.

(k) The BUS CONTROL—OFF—1 key removes power from the scanner cable receivers associated with the TSPS 1/N address bus 1 or the SPC PUAB 1.

(l) The SCANNER BIAS—TBL—0 and TBL—1 lamps light when the bias current of the access core matrixes is not normal.

(m) The OFF NOR lamp lights when either the FRAME CONTROL—NOR or BUS CONTROL—NOR keys have been operated.

(n) The PWR OFF lamp lights when a BUS CONTROL—OFF or FRAME CONTROL—OFF key is operated or when a fuse failure occurs.

2.99 Scanner Matrix, Upper and Lower Units:

The scanner matrixes contain the ferrod sensors used to provide status data from the monitored circuits.

2.100 Remote Master Scanner Applique Unit:

The remote MS applique unit enables remote circuits (i.e., a power plant) to be connected to ferroids for sensing by the MS. Up to eight circuits can be connected to the MS via one remote scanner applique unit, and more than one remote scanner applique unit may be equipped per frame.

2.101 Fuse Panel and Power Supply Filter:

The fuse panel and power supply filter are used to provide the required power to the scanner circuits. Two +24 volt power feeders, one for each controller, are routed from the power distributing frames to the filter panel located at the base of the scanner frame. A filter is connected to each feeder to suppress extraneous noise voltages. The output of each filter is fanned out through fuses located on the fuse panel mounted above the filter panel. The individual power feeders are connected to the appropriate controller and to the frame control panel.

2.102 The ferrod sensor (Fig. 15) is the basic unit of the scanner. It can be considered a 2-winding transformer with a ferrod core whose coupling is controlled by the current in a third control winding. The primary and secondary windings of the transformer are associated with the access and readout equipment and are referred to as the interrogate and readout windings, respectively. The control windings are connected to the circuit requiring scanner monitoring. The interrogate signal induces a signal into the readout winding, if there is insufficient current in the control windings to inhibit any coupling.

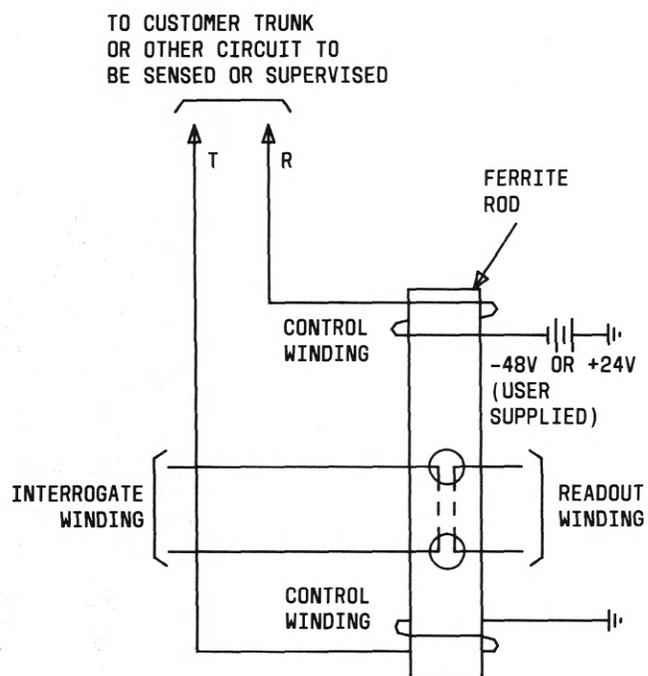


Fig. 15—Ferrod—Simplified Schematic

2.103 MS00 provides ferroids to sense the circuit conditions of 1024 separate scan points. This allows MS00 to monitor all SPC No. 1A peripheral equipment and to provide limited monitoring of the application system equipment. Additional MSs may be required in an office depending upon the application system and the generic program load.

2.104 Through SPC generic program PG-1C006, the TSPS application system contains a maximum of five additional MSs (MS01-MS05). The use of MS01 through MS03 is dependent on office

size. MS04 and MS05 are required to monitor the base office remote trunk arrangement (RTA) and Position Subsystem No. 2 (PSS2) equipment, SSAS equipment, and common channel interoffice signaling (CCIS) equipment and to provide additional scan points for office growth. CD- and SD-1B061-01 provide detailed information on MS00 through MS05 scan point assignments.

2.105 The ETS application system uses peripheral scanners (PSCs) to obtain and supply information to the SPC No. 1A. Operation of the PSCs is similar to that of MSs, but length of the data word supplied to the processor is different. PSCs supply a 20-bit word as compared to the MS 16-bit word. Section 212-801-101 contains general operating and descriptive information and scan point assignment data for the PSCs.

2.106 In the STP stand-alone application system, a PSC obtains information and supplies it to the SPC No. 1A.

G. Control and Display, Program Tape Unit, and Teletypewriter

General

2.107 The CD, PTU, and TTY are contained in a 3-bay frame (called the CD-PT-TTY), 7 feet high and 6 feet 6 inches wide. This frame (Fig. 16) is the centralized point of manual control and communication with the SPC No. 1A.

Program Tape Unit

2.108 The PTU, which consists of the tape transport (recorder) and the PTU circuitry, is located in bay 0 of the CD-PT-TTY frame (Fig. 17). Also contained in bay 0 are the PTU control panel, a KS-19829 L2 or L4 control unit or KS-20573 power supply, and a filter panel. The following is a brief description of the circuitry in the bay.

2.109 *Program Tape Unit Circuitry:* This circuitry contains the CPs which provide the read, write, and register circuitry necessary for its operation.

2.110 *Program Tape Unit Control Panel:* This unit consists of keys and lamps necessary to assert manual control over the tape transport and to display the various operating modes.

2.111 *Tape Transport:* The tape transport contains the read and write heads which retrieve information from or store information on the magnetic tape.

2.112 *Control Unit or Power Supply:* Either a KS-19829, L2 or L4 control unit for use with the KS-19829 L1 or L3 tape transport or a KS-20573 power supply for use with the KS-20571 L1 tape transport is mounted as part of the tape transport.

2.113 The PTU is used to initially load the stores with the system program. In addition, this equipment is used for bootstrapping the system; i.e., reloading mutilated stores in the event of catastrophic failures; updating of generic programs; extensive changes in translation data; and, in general, all additions to the store that would be too time consuming to be put in via the TTY. The PTU equipment can also write information onto tape under direction of the processor.

2.114 The PTU can exist in one of the following three configurations:

- (a) The PTU circuit, SD-1C108-01, equipped with the KS-19829 tape transport
- (b) The PTU circuit, SD-1C108-01, retrofitted with the newer KS-20571 tape transport
- (c) The new PTU circuit, SD-1C396-01, equipped with the KS-20571 tape transport.

2.115 With the configuration described in paragraph 2.114 (c), the PTU circuitry has provisions for an optional 25 inch-per-second (IPS) tape speed (standard tape speed is 5 IPS). Space is provided for the optional feature CPs. CPs for this optional feature consist of an additional delay circuit and three additional analog timer circuits. For this circuitry to be effective, the fast bootstrap (FBOOT) program must be part of the generic program load.

2.116 The KS-20571 tape transport comes equipped with a 25-IPS speed selector key/lamp. However, when the KS-20571 is used as in the configuration described in paragraph 2.114 (b), the optional 25-IPS tape speed cannot be used since the SD-1C108-01 circuitry cannot support the optional feature CPs.

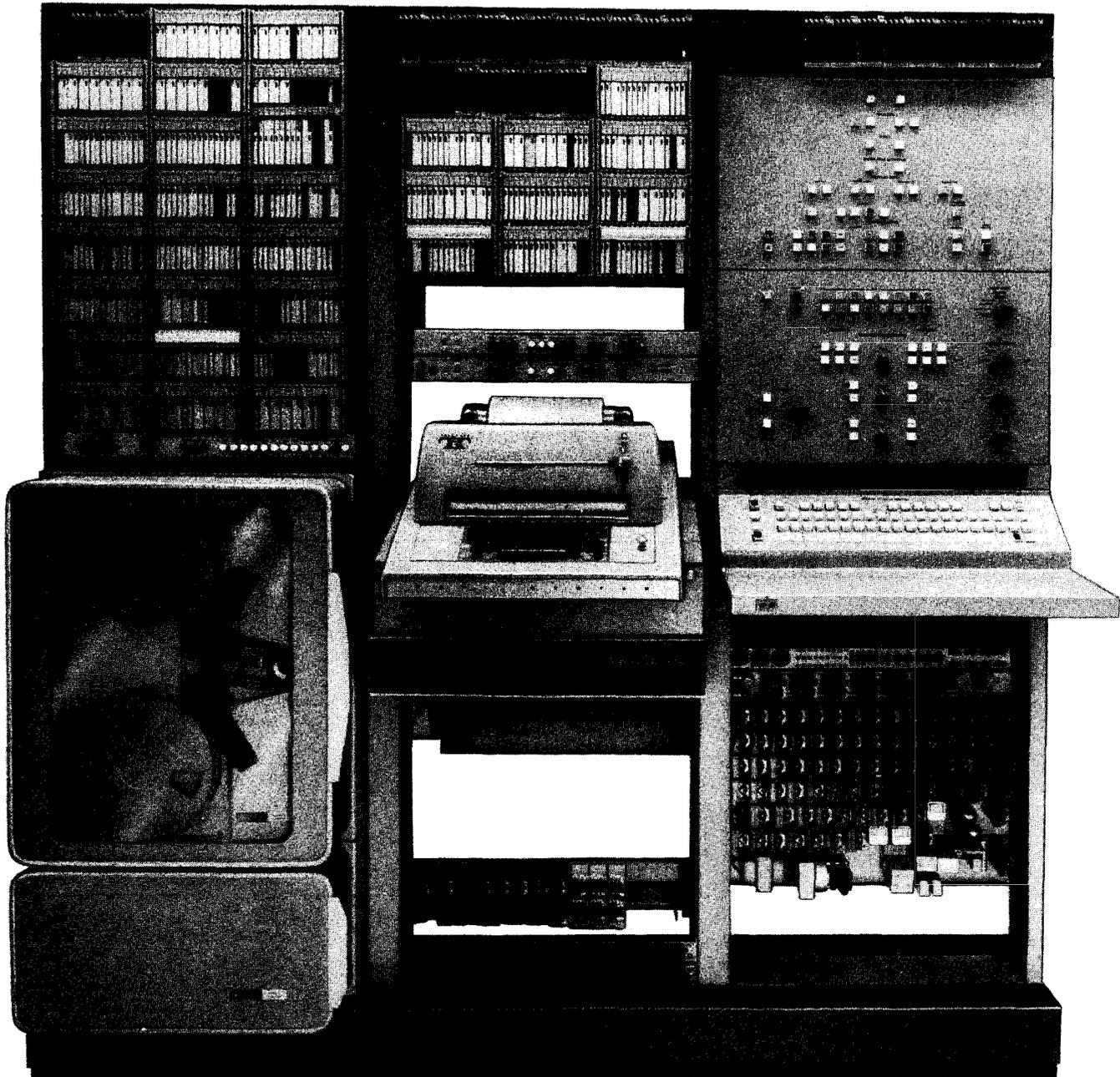


Fig. 16—Typical CD-PT-TTY Frame

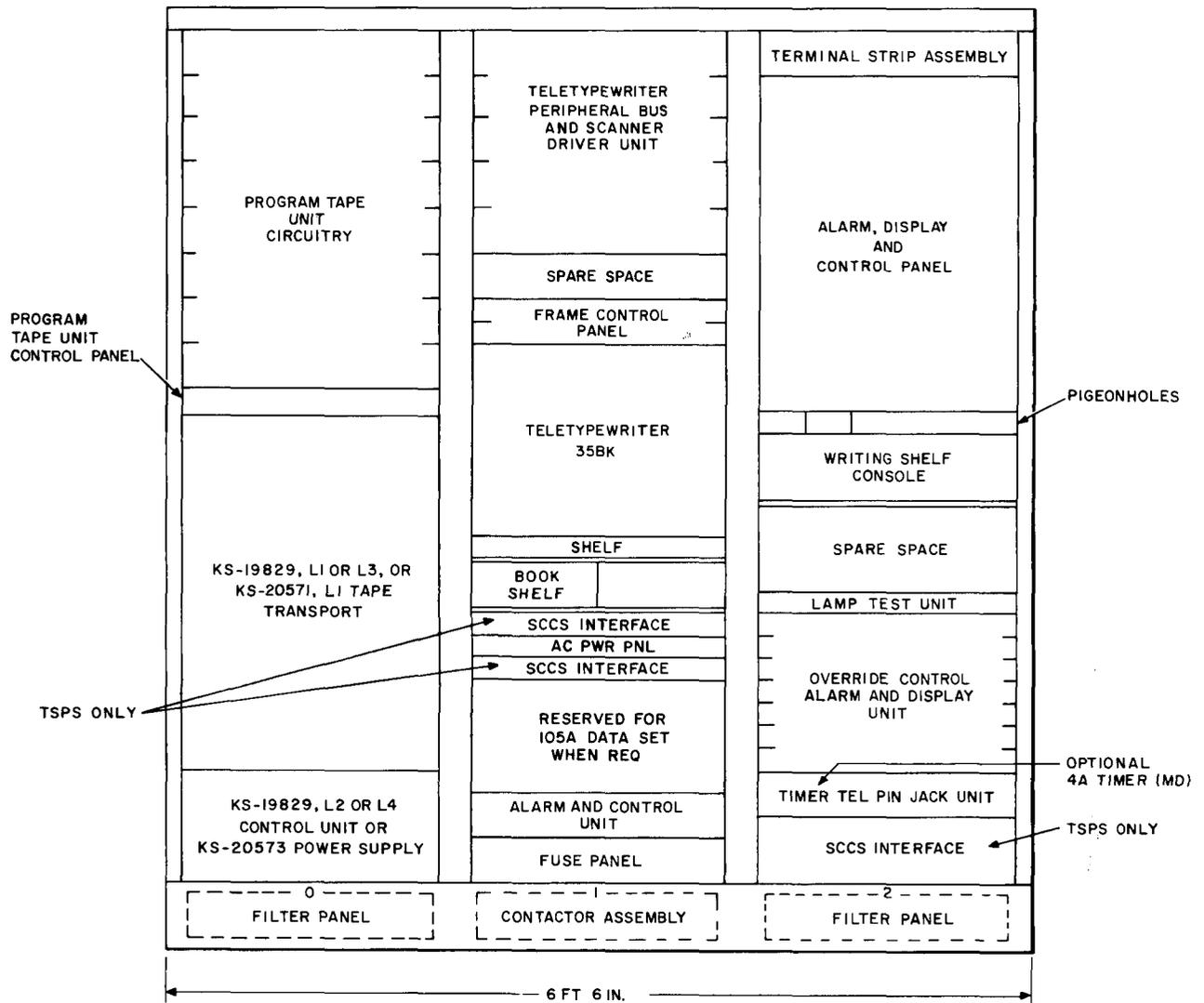


Fig. 17—CD-PT-TTY Frame

2.117 The PTU is also used to load automated announcement information into the SSAS announcement stores. The SSAS peripheral equipment is applicable to TSPS No. 1 only.

Teletypewriter

2.118 Bay 1 of the CD-PT-TTY frame contains the TTY which is located on a sliding shelf 3 feet 6 inches from the floor. A brief description of other units in bay 1 follows.

2.119 **Teletypewriter Peripheral Bus and Scanner Driver Unit:** This unit contains the CPs necessary for the independent operation

of two TTY machines in addition to cable drivers and receivers necessary for communication between this frame and the rest of the SPC No. 1A system.

2.120 **Frame Control Panel:** The frame control panel contains control keys and indicator lamps for the local (channel 0) and remote (channel 10) maintenance TTYs, the other equipment on the CD-PT-TTY frame, and the communication buses.

2.121 **AC Power Panel:** This unit provides the necessary AC voltage required for the PTU, TTYs, 4A timer, and optional data set.

2.122 105A Data Set: A space is reserved beneath the AC power panel for a 105A data set for systems requiring a data set.

2.123 Alarm and Control Unit: This unit furnishes fuse alarm relays and certain dropping resistors necessary for obtaining particular voltages required in the electronic circuitry.

2.124 TTYs used in the SPC No. 1A are model 35BK-type TTYs. The SPC No. 1A and its associated systems may have as many as 32 TTY channels depending upon the particular application and needs of the operating telephone company. However, there are always two independent base TTY channels for maintenance purposes (channel 0 and channel 10).

2.125 One TTY machine is always mounted in bay 1 of the CD-PT-TTY frame. The second maintenance TTY is located at some remote attended point. The TTY located in the CD-PT-TTY frame is referred to as the local maintenance TTY or TTY 0. The second TTY is referred to as the remote maintenance TTY or TTY 10. If the local TTY fails, the SPC No. 1A automatically transfers all messages to the remote TTY.

2.126 When the two maintenance TTYs are separated by a distance greater than 4 miles, 105A data sets convert the DC TTY signals to AC tones and vice versa for transmission purposes.

2.127 The dial-up monitoring feature, associated with the TTY 0 monitor loop, permits remote monitoring of TTY output messages by Columbus Products Engineering Control Center, Bell Telephone Laboratories, etc. This allows engineers at these locations to analyze any troubles which may develop in the system. Normally, data from a remote monitoring location is automatically excluded from the SPC No. 1A. A monitor input inhibit (MII0) key, located on the TTY power control panel, allows data to be received from the remote monitoring location.

2.128 The No. 2 Switching Control Center System (SCCS) (for TSPS only) provides the means to transmit status information to a No. 2 SCCS computer that translates the information and formats a cathode-ray tube display. A backup TTY is provided for recording when the computer is off-line. The No. 2 SCCS computer contains

software features that assist craft personnel in analysis and evaluation of TSPS No. 1 performance.

2.129 Data sets 103G or 113A (manufacture discontinued) are provided for use with the dial-up monitoring feature. Data set 108F is provided for connection to the No. 2 SCCS. This arrangement provides a terminal interface for two TTYs. These data units are mounted on the miscellaneous frame.

Control and Display

2.130 Bay 2 of the CD-PT-TTY frame contains the CD panel for the SPC No. 1A. The CD panel, equipped with lamps, pushbutton keys, and rotary switches, provides the primary man-machine interface with the SPC No. 1A.

2.131 The CD is divided approximately in half by a writing shelf. Located on the edge of the writing shelf is a head telephone jack which is part of the circuit which provides a means of communication between frames in the SPC No. 1A office. A brief description of the units in the CD follows.

2.132 Alarm Display and Control Panel: The CD panel, which is composed of lamps, keys, and switches, allows the craft person to monitor and exert manual control over the system.

2.133 Lamp Test Unit: The lamp test unit is used to verify that all lamps on the CD panel are in working condition.

2.134 Override Control, Alarm, and Display Unit: The override control, alarm, and display unit contains circuitry needed by the CD panel to perform its functions.

2.135 Timer Telephone Pin Jack Unit: The timer circuitry, local frame line circuitry, and pin jacks are mounted on the timer telephone pin jack unit. The optional timer circuitry consists of a 4A timer (manufacture discontinued); the local frame line circuitry is used in conjunction with the head telephone jacks; and the pin jacks provide GND, HRG, and -48 and +24 volt batteries for testing purposes.

2.136 Filter Panel: Filters, fuses, and fuse alarm circuits, located at the bottom of

the bay, provide -48 and +24 volt power for CD equipment.

2.137 Lamp displays on the CD panel aid the craft person when asserting manual control over the system. The software controlled lamps:

- (a) Monitor status of data routing flip-flops in processors and stores
- (b) Indicate troubles such as peripheral control failures, system time-outs, and loss of power
- (c) Provide a continuous status display such as service configuration and units out of service
- (d) Display a single data word or program action
- (e) Serve as a visual alarm for system detected troubles
- (f) Display special mate failure data for emergency recovery.

2.138 Each lamp on the display panel is one of four colors to indicate the following:

- (a) **Red** lamps indicate a primary trouble.
- (b) **Amber** lamps generally indicate a secondary trouble.
- (c) **Green** lamps indicate an activated locking pushbutton key.
- (d) **White** lamps are monitoring lamps that indicate an active condition or the selection of a particular key.

Lighting of a red lamp is usually accompanied by a critical (for TSPS only) or a major alarm. A steady amber lamp indicates that one controller is in trouble; a flashing amber lamp indicates more than one controller is in trouble. Amber lamp indications are also used with controls that interlock with certain switches; lighting of an amber lamp in such a case signifies caution.

2.139 Manual CD controls are provided so the craft person can perform various maintenance functions. Operation of keys and rotary switches causes the software program to respond as follows:

- (a) Selects processors as active or standby

- (b) Changes peripheral units, buses, and the first eight stores out of and into service

- (c) Reconfigures and establishes an operational system

- (d) Causes program interrupts for specific purposes

- (e) Inserts data to monitor system action

- (f) Initiates call processing recovery

- (g) Inhibits program interrupts for specific purposes

- (h) Retires and transfers alarms.

2.140 Rotary switches and pushbutton keys, both locking and nonlocking, provide various means for manual control over the system. These switches and keys are used to override program control of system functions and configurations. Circuit interlocks are provided on all critical override controls to avoid any possible system disruption due to improperly selected override conditions.

3. STORED PROGRAM COMMUNICATION AND CONTROL

A. Bus System

3.01 Information is exchanged between units of the SPC No. 1A over routes of communication as shown in Fig. 18. A group of leads referred to as a bus provides a common path that serves a number of associated units on a time-shared basis. This arrangement eliminates the need for a larger number of individual unit-to-unit interconnections.

3.02 In the scheme of bus communications between units of a system, two general methods are used to select (enable) the unit that must respond to information transmitted over a bus shared by several units.

3.03 One method, used principally in communication between the processor and store units, consists of transmitting "names" in the form of a binary code on the bus simultaneously with the information to be acted upon. A unit responds to the message only if its code name matches the transmitted enabling code.

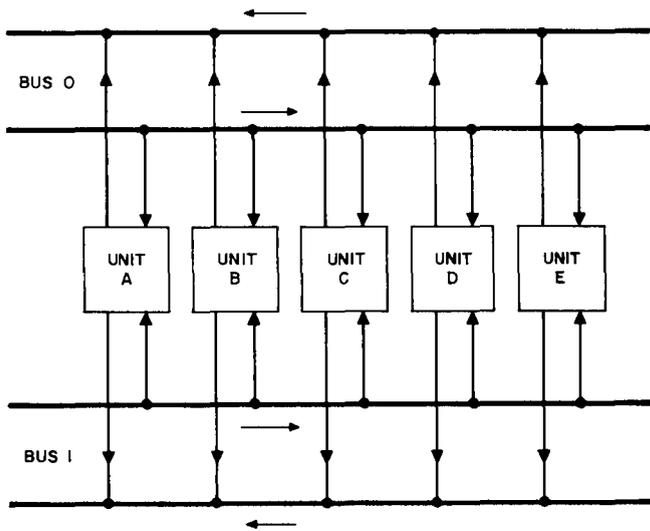


Fig. 18—Simplified Bus Scheme

3.04 The other method of enabling, used primarily for CPDs and peripheral units, consists of an enabling pulse which is sent over a "private" path between units apart from the common bus.

B. Processor and Store Communication

3.05 Details of the duplicated processor and store interconnection are shown in Fig. 19.

3.06 Each processor normally communicates only with one copy of memory. However, if required, either processor may communicate with either memory. Thus, processor 0 may write into memory 0 via bus 0 and into memory 1 via bus 1. Similarly, processor 1 may write into memories 0 and 1 via buses 0 and 1, respectively. The same relationships hold true for processor read operations.

3.07 Each store of a particular store group has its corresponding image or copy in the opposite store group. Each store group is permanently assigned to one bus (0 or 1). The two processors normally run in parallel, synchronously executing the same program. The program instructions are obtained by each processor from its associated store group. Bus switching can be accomplished at the processor; either or both buses can be connected to either or both processors.

3.08 At any given time, only one processor can be in control of the system (active). Communication channels to the CPDs and other

peripheral units are established only for the active processor except during certain maintenance programs.

3.09 Since a change in the system status is established via the CPDs, the active processor is in command of system configuration. The active processor determines bus choice between stores and processors; selects the bus configuration for the appropriate processor-store communication mode; and as a result, dictates the treatment of instruction and data communication to and from the stores. The active processor, which always calls for its own instructions, can send on either or both buses; while the standby processor can only send on a bus not being used by the active processor.

3.10 Communication between the stores and the processor is in the form of 47-bit words. Seven of these bits (one parity and six Hamming bits) provide error control in communication between the stores and the processor. The parity bit is set to either 1 or 0 (by the processor) in order to maintain an odd number of 1s in the memory word. The processor parity check circuit verifies that memory words transferred from the stores to the processor arrive unchanged by testing for the odd number of 1s. The six Hamming bits condition the memory word for a Hamming check. In the processor, each bit position in the memory access register (MAR) and address image register (AIR) is assigned a correction bit value. A conversion of correction bit values for all bits set in the MAR and AIR results in a correction value. This value and results of the parity check determine the validity of the memory word and provide control of the processor correction circuit when an error has been detected. Section 254-109-101 contains additional information on Hamming and parity.

3.11 Two types of words are stored in memory:

- (a) Instructions, sometimes called orders or commands, tell the processor which course of action to take. Instructions are 40 bits long (excluding error bits).
- (b) Data includes any type of information, other than instructions, which will be required at some time by the processor.

3.12 Data is stored in various word sizes by fitting "chunks" of data into 40-bit words (packing). Since the basic data word length required by the processor is 20 bits, the store word addresses

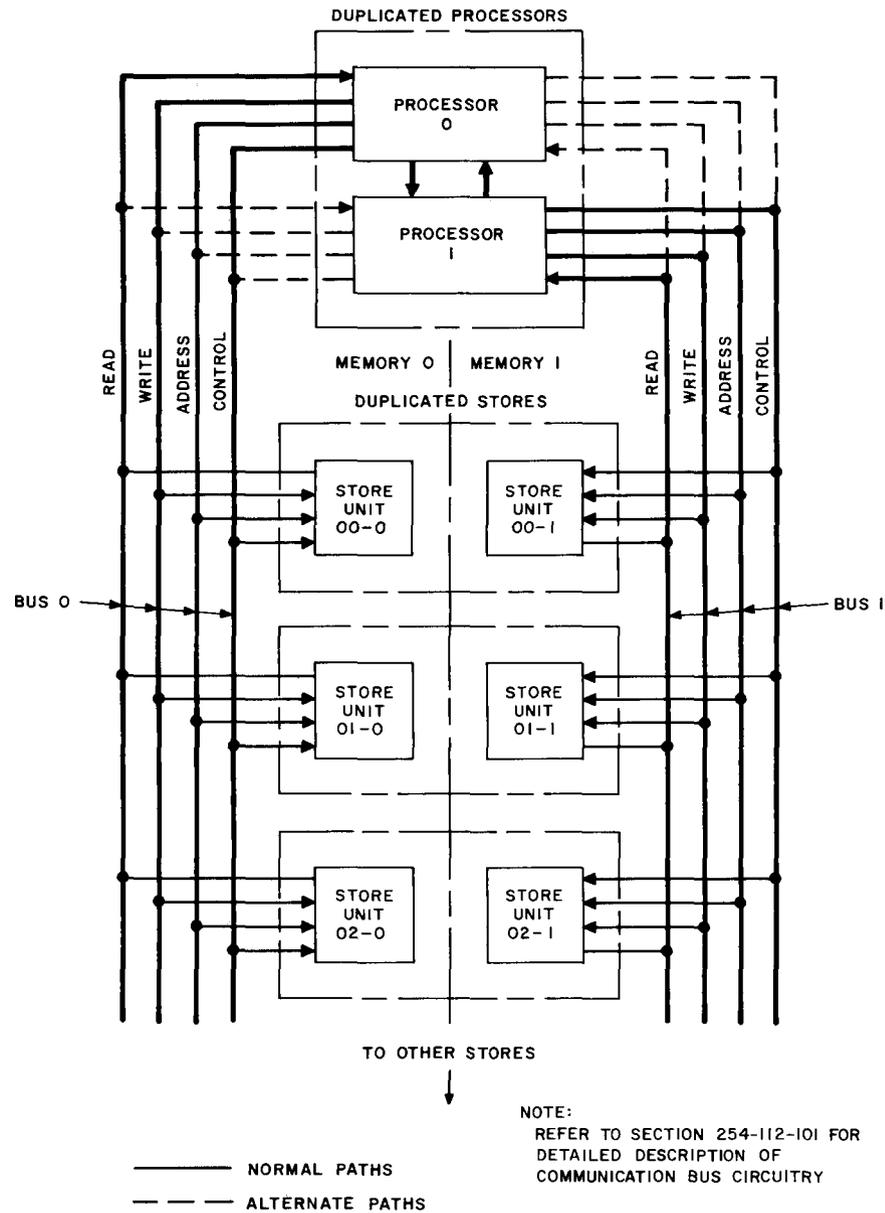


Fig. 19—Processor and Store Communication

are set up on a 20-bit or half-word basis. The least significant half of a 40-bit store word (0 through 19) is assigned an even address, while the next higher numbered address (odd) is assigned to the 20- through 39-bit half-word. The half-word store address format is illustrated in Fig. 20.

3.13 If data at location $AA+3$ were required by the processor, both 20-bit half-words (locations $AA+2$ and $AA+3$) would be sent to the processor MAR but only the left half-word would be used.

3.14 Instructions are coded into full words and occupy two locations. By convention, instructions are defined as being placed at their even (least significant) address. The even location of an instruction contains the address field and the odd location contains the operation code and options. Instructions and 40-bit data words (location $AA+4$) are accessed by even addresses only.

3.15 Program instructions for the SPC No. 1A are encoded into a symbolic language using

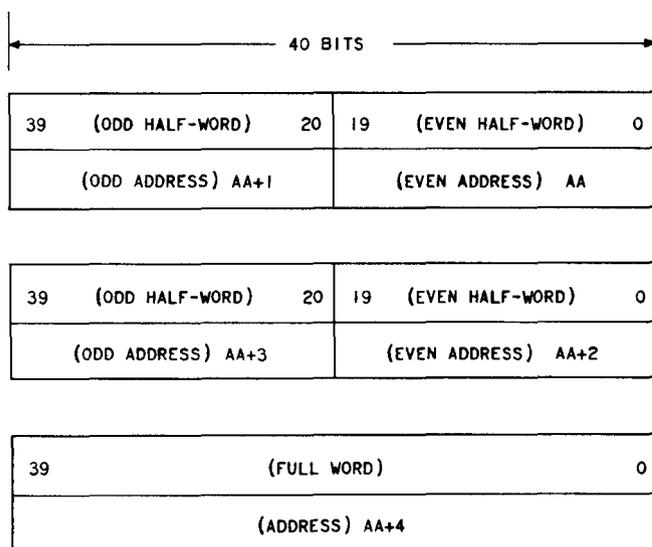


Fig. 20—Store Address Format

a mnemonic code as described in Section 254-109-101. The symbolic language is assembled into binary *object* programs. These object programs are then loaded into the memory from a system program tape which is the end result of the compiling and assembling operation.

3.16 Each 40-bit instruction consists of the following fields:

Operation (\emptyset P)

Address (ADDR)

Index (INDEX)

Function (FUNCT).

The encoded format is shown in Fig. 21. The example shown in Fig. 21A is a memory-to-register (MR) instruction. The destination register is the X register; the memory address is location AA plus the contents of the Y register; and the function to be performed on the word is a logical product with the complemented contents of the F register. Figure 21B shows bit assignments for the various fields and subfields in the format. Section 254-109-101 gives a detailed explanation of each field and subfield.

3.17 For the TSPS application system only, the SPC No. 1A processor also uses the store bus system to communicate with the SSAS announcement stores. The announcement stores are used to store automated announcement information for use with the ACTS feature. The announcement stores are connected to the store bus only during loading or diagnostic testing operations.

C. Processor and Peripheral Unit Communication

3.18 The SPC No. 1A uses duplicated AC buses to transmit instructions, addresses, and other data to such peripheral equipments as network frames, scanners, distributors, tape units, and data links. The simplified bus communication flow is illustrated in Fig. 22. There are four main AC buses associated with information flow between the processor and a peripheral unit: the SPC PUAB, SCAB, CPD enable bus, and CBT address bus.

3.19 The SPC PUAB is dedicated to the peripheral units which are a part of every SPC No. 1A installation. They are the units which are considered to be SPC peripheral units.

3.20 The CBT address bus is used to address all peripheral units which are considered to be part of the application system equipment.

3.21 The CPDs are located on a dedicated CPD enable bus which is used by the processor to activate one CPD on every peripheral order.

3.22 The SCAB is used to inform the processor of the states of scan points in a particular group as requested by the program.

3.23 Each peripheral unit connecting with an address bus is assigned at least one unipolar "enable" point on the CPD. To deliver information to a particular unit, the processor first transmits the enable address to the CPD which produces an enable pulse to be transmitted to the unit via a private path. This pulse enables that unit, and only that unit, to receive from the processor the information which follows on the address bus.

3.24 Effective with PG-1C006, for TSPS only, capability is provided for the growth and maintenance of the CCIS DS equipment. The CCIS equipment becomes operational with PR-1C007

ØP	ADDR	INDEX	FUNCT
MX	AA	Y	PFC

A — MNEMONIC FORM

OPERATION FIELD		FUNCTION FIELD			INDEX FIELD		ADDRESS FIELD
ØP CODE	ØFR	RMRA	LBQ	MZC	INDR	ICR	
*39---36	*35---33	*32---30	*29---25	24	*23---21	*20	*19-- -- --0

* BIT NUMBERS

B — BINARY FORM

DEFINITIONS

ØFR	OPERATION FIELD REGISTER
RMRA	REGISTER/MASK/RETURN ADDRESS
LBQ	LOGIC/BIT TO TRANSFER ON/ROTATE
MZC	MASK/ZERO/COMPLEMENT
INDR	INDEX REGISTER
ICR	INCREMENT REGISTER

Fig. 21—SPC No. 1A Encoding Format

[TSPS generic PG-1B108 (1T10)] and is used with the auto bill calling (ABC), originating station treatment (OST), and billed number screening (BNS) features of TSPS. The processor uses the CBT address bus and the SCAB to communicate with the CCIS equipment.

3.25 A detailed description of all major SPC No. 1A buses is contained in Section 254-112-101.

4. FUNCTIONAL DESCRIPTION OF THE SPC

4.01 The SPC No. 1A processor performs all of its functions on a time-shared basis. The processor operates at a rate of one cycle each 6.3 μ s (machine cycle). One instruction may require one or more machine cycles to complete. The processor executes instructions by gating information internally from one place to another, by performing logic operations on the information, and by sending

signals to equipment such as the stores and peripheral units which the processor controls.

4.02 Instructions from the stores periodically direct the processor to monitor circuit conditions within the SPC No. 1A via the MS. Since the MS is addressed by the processor on a time-shared basis, the system cannot continuously observe any circuit but must sample or scan it at periodic intervals.

4.03 The MS is enabled as shown in Fig. 23. Orders are sent from the processor to the CPD in three consecutive 1.25- μ s time slots. First a bus sync signal is sent. This order indicates that an enable address will be transmitted to the CPD in the next time slot. Next an enable address is sent from the processor AIR to the CPD via the CPD enable address bus. In the third time slot, an execute signal is sent from the CPD enable register (located in the processor) to the CPD via

individual leads. The enable address together with the execute pulse select one particular pair of output leads and cause an enable pulse to be sent over these leads to the MS.

4.04 After a 2- μ s delay, an enable verify pulse is returned to the CPD from the enabled MS. The CPD then relays an enable-verify signal to the processor, informing the processor that one, and only one, peripheral unit was enabled.

4.05 An address, which is sent over the SPC PUAB, is accepted and used by the MS. This address will be an order to interrogate a specific row of ferrods. Figure 24 illustrates this order using row 30 as an example. The states of all 16 ferrods in the row (therefore, the states of the circuits to which they are assigned) are then returned to the processor via the SCAB. The MS transmits 17 bits back to the processor [16 bits of data and one all-seems-well-scanner (ASW-S) bit]. This indicates the result of MS controller internal checks.

4.06 The data obtained by scanning the row of ferrods is accepted by the processor and compared to the previous states of the ferrods stored in memory (obtained on the last scan of the row). Depending upon the state of any ferrod and its state on the last scan, software can detect system activities and determine appropriate actions to be taken. After comparison, the data obtained on the most recent scan of the row is stored in an unprotected area of memory for comparison on the next scan.

4.07 Information obtained by scanning a row of ferrods could result in software actions such as directing the operation of relays in system circuits. Figure 25 illustrates the use of the SD in the operation of circuit relays. (In Fig. 25, the objective is to operate relay B in circuit Y.)

4.08 The processor instructs the CPD to enable the SD. When the SD has been enabled, it sends an enable-verify pulse back to the CPD. This pulse constitutes a verification that a controller of a particular SD unit has been seized by the system. The CPD sends a pulse to the processor verifying that one, and only one, peripheral unit was enabled.

4.09 The processor sends an order to the SD to operate relay B in circuit Y. The SD accepts

this order and sends a battery pulse (-48 volts to operate) to relay B. Relay B is a magnetic latching relay and will remain operated until a pulse of opposite polarity (+24 volts) is sent to release it.

5. PROGRAM DESCRIPTION AND OPERATION

SYSTEM PROGRAM

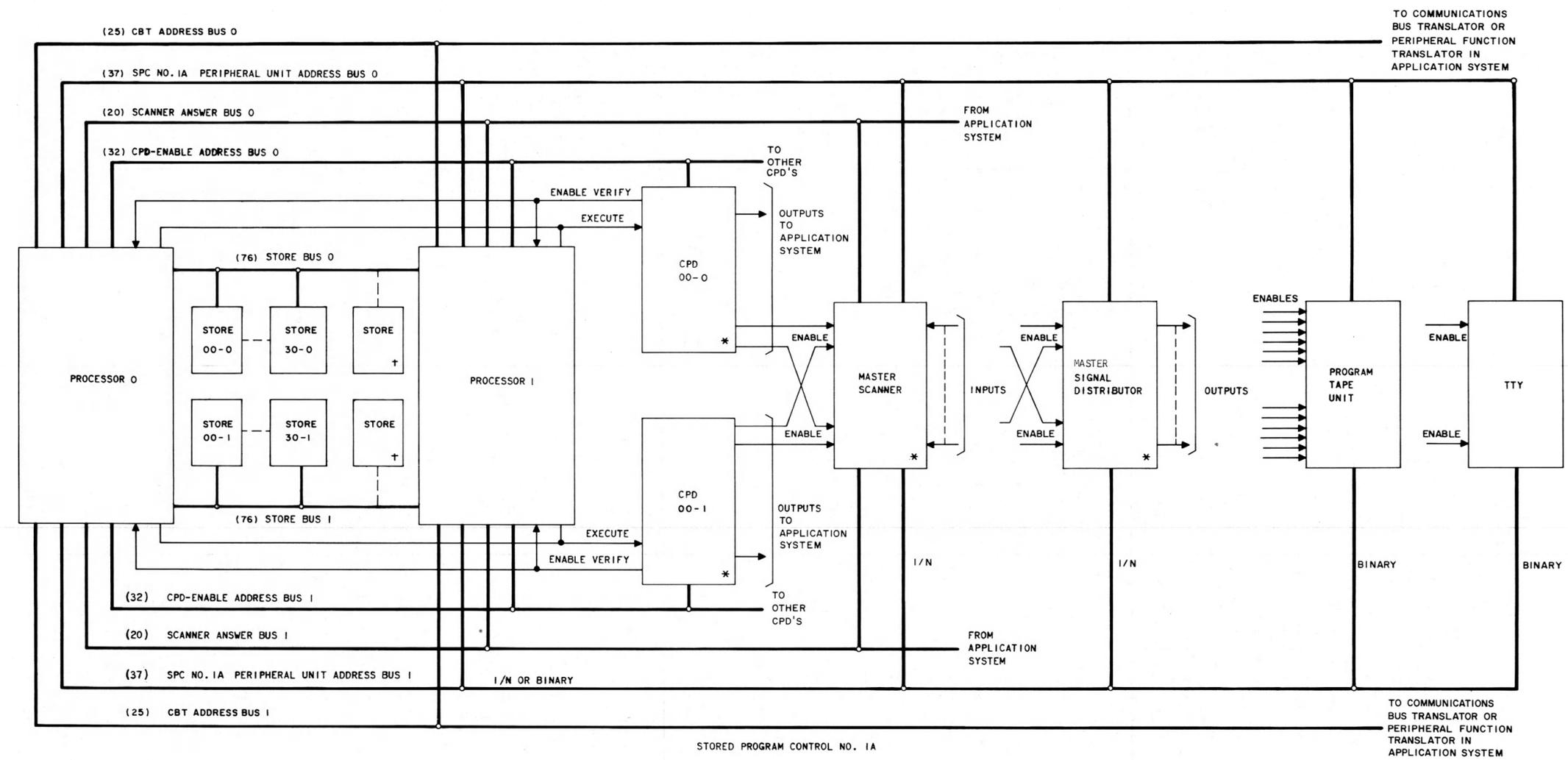
5.01 Programs for controlling and maintaining equipment in an SPC No. 1A office are provided to the operating telephone company by way of data contained on a system program tape. This system program tape is unique for each operating telephone company office and contains the following information:

- (a) An SPC No. 1A generic program that controls functions common to all SPC No. 1A offices
- (b) An application system generic program that controls services of the application system and maintenance of non-SPC No. 1A equipment when not provided for by the SPC No. 1A generic program
- (c) Office data which is specific to the operating telephone company office.

These three distinct groups of data are integrated into one complete system program tape.

5.02 Generic programs are assigned unique program numbers which are prefixed by *PG*. A separate series of program numbers exists for the SPC No. 1A and each of its application systems. These program numbers identify the specific services and features found in the associated generic program. Each generic program contains new services or features in addition to all services and features contained in the preceding generic programs of that series. The SPC No. 1A program number for any given generic must be coordinated with a specific corresponding program number belonging to the associated application system. This coordination of generic program numbers is necessary to establish a workable system program tape.

5.03 The system program tape is a 9-track magnetic tape containing two types of words: data words (which can consist of data or instructions) and identity words. Words are entered in blocks of up to 150 data words preceded by a single identity word. Each word contains 40 bits divided



* ADDITIONAL FRAMES OF THESE UNITS MAY BE REQUIRED DEPENDING ON THE NEEDS OF THE APPLICATION SYSTEM.
 † AT PRESENT, ADDITIONAL STORE FRAMES ARE USED ONLY IN THE TSPS (EQUIPPED WITH SSAS) AND ARE CONNECTED TO THE STORE BUS ONLY DURING LOADING OR DIAGNOSTIC TESTING OPERATIONS.

Fig. 22—Processor/Peripheral Unit Communication Bus System

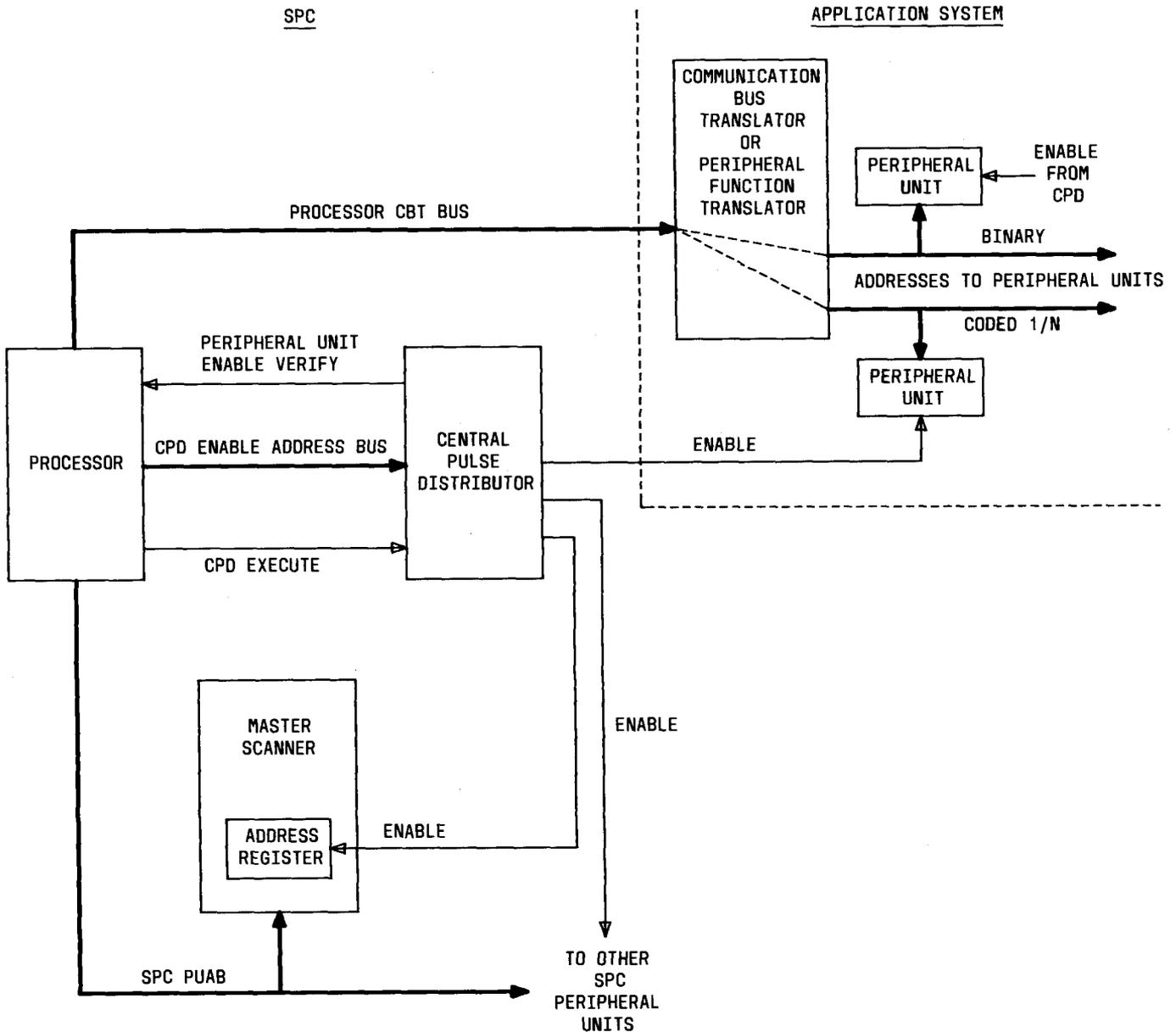


Fig. 23—Enabling of Master Scanner

into 5 tape characters. When a computer is writing the tape in the binary mode, an odd parity bit is generated over the 8 data bits of each character. These parity bits are written in track 3 of the 9-track tape. The identity word at the beginning of each word block designates the memory location of the first data word in the block.

5.04 The system program is loaded into the SPC No. 1A stores from the magnetic tape via

the PTU. In the initial state (prior to program loading), the stores contain no useful information. Consequently, the processor does not have access to the basic set of instructions (called a bootstrap program) which enables it to do simple repeated scanning, assembling, and storing operations. In offices where the base store is a PBT store, the bootstrap program must be loaded manually from the processor via a bootstrap transfer card extender or PERC unit. Use of the bootstrap transfer card

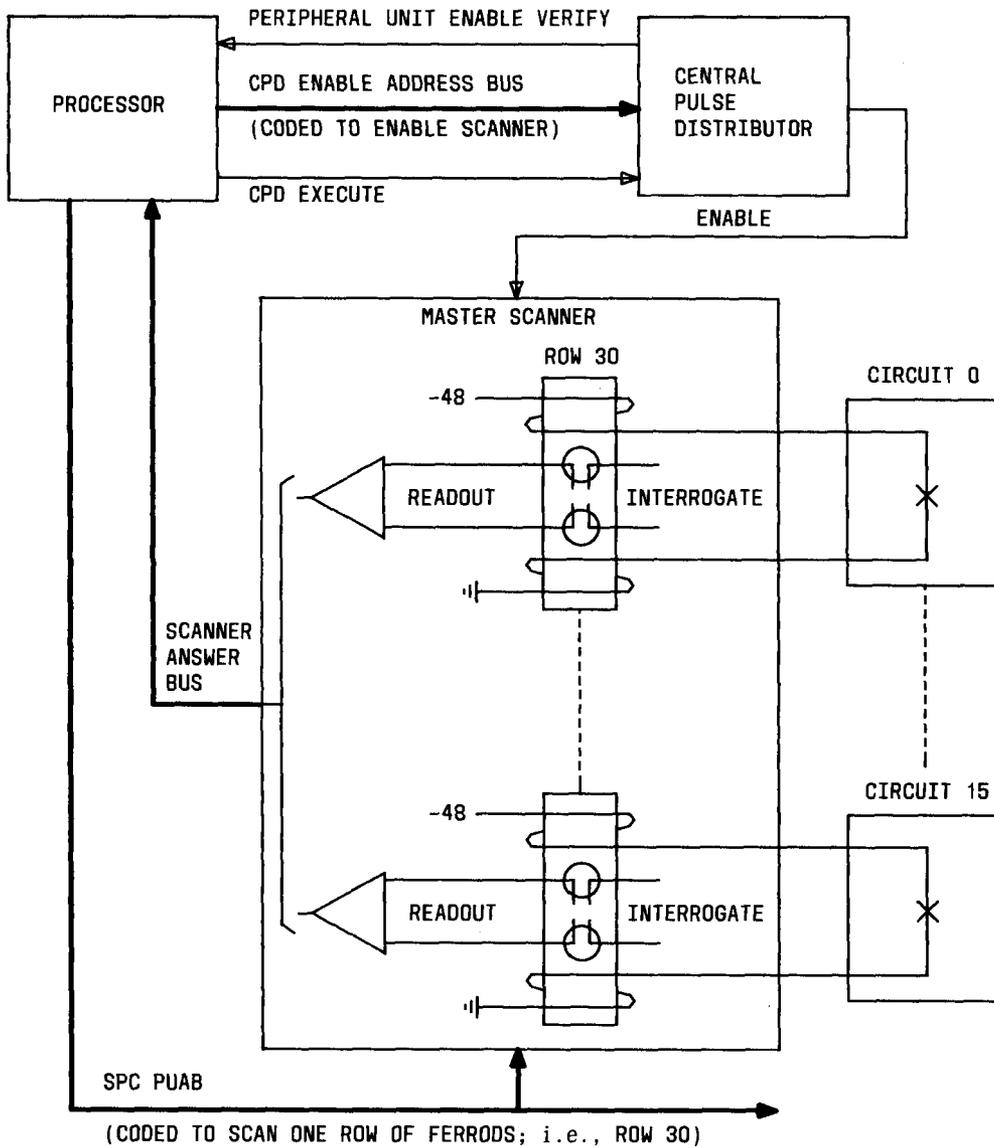


Fig. 24—Typical Use of Master Scanner

extender is preferable and should be the first choice for the bootstrap procedure. The PERC unit should only be used if the bootstrap transfer card extender is damaged or in some other way is rendered inoperative. In offices where the base store is a semiconductor IGFET store, a secondary bootstrap program is provided in a nonvolatile read-only memory (ROM) which is located in and powered by the store controller.

5.05 The bootstrap program enables the processor to do simple repeated scanning, assembling, and storing operations. When the PTU has read and registered 40 bits of a single data word in

the MS, it informs the processor via another scan point. The processor retrieves the data word from the MS, generates seven check bits (Hamming and parity), and writes the word and check bits into the store at an address which was obtained from the identity word. The memory locations for succeeding data words are obtained by successively incrementing the store address portion of the identity word by two for each data word following the first one. This process is repeated until the stores are loaded with the complete system program.

5.06 When loading of the system program is complete, the SPC No. 1A stores contain all

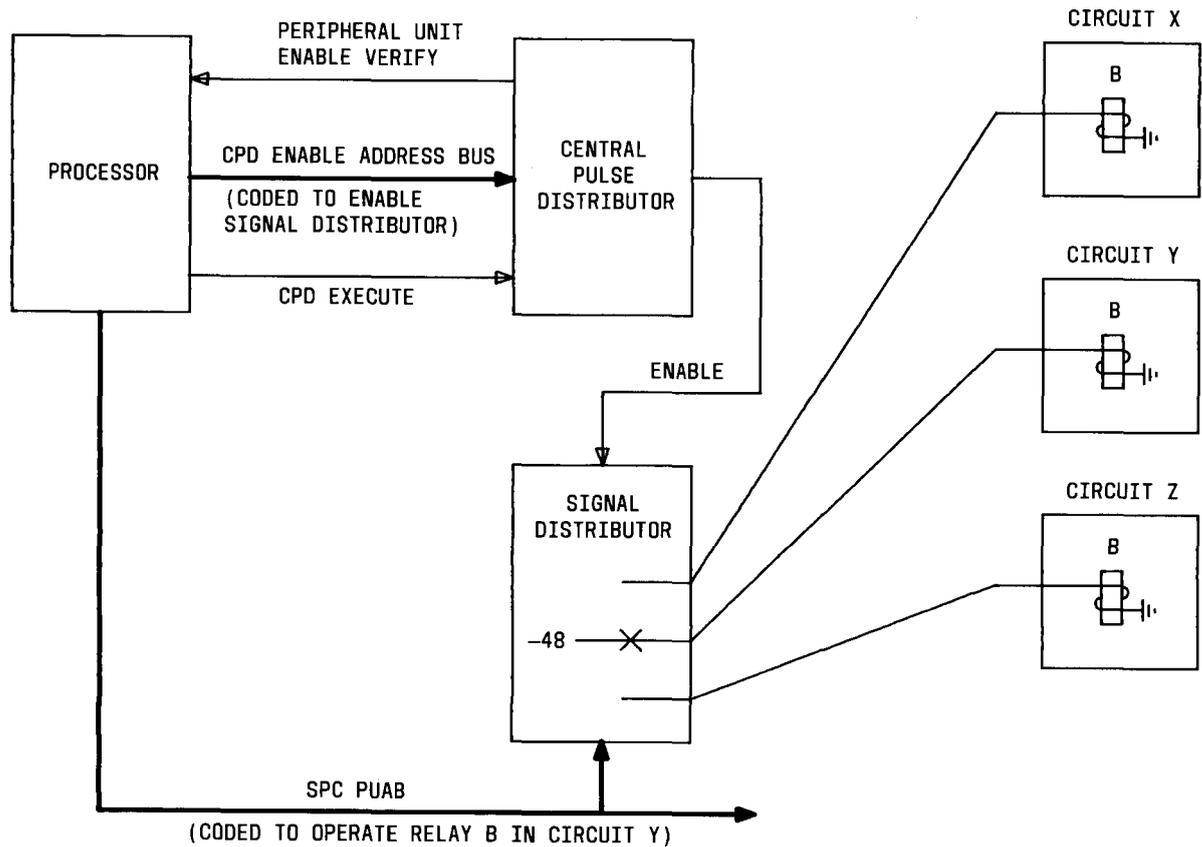


Fig. 25—Typical Use of Signal Distributor

information necessary to direct processing of telephone calls.

SPC NO. 1A GENERIC PROGRAM

A. Overall Program and Interrupt Plan

5.07 Since the SPC No. 1A processor operates on a time-shared basis, the SPC No. 1A program is divided into various operating levels (referred to as interrupt levels). Groups of program instructions (programs, subroutines, etc.) are assigned to the various operating levels in accordance with their levels of importance in maintaining an operational system. Table C shows a list of the levels of operation.

5.08 There are interrupts of nine priority levels: A, B, C, E, F, G, H, J, and K from the highest to lowest. In the absence of all interrupts, the system is said to operate on the so-called base or L-level. An interrupt can seize control from

the base level or from any interrupt level of lower priority. (A and B are exceptions which can interrupt themselves; and B can interrupt A.) Control can be in only one level at a time, and the states of certain processor flip-flops keep track of the active level. The program segment being executed at a given time does not necessarily identify the level, since a few subroutines are executed in different levels (at different times). However, most programs are assigned specific levels, with the bulk of them being level L or base level programs.

5.09 All base level programs collectively can be said to form the **base level program**. Despite functional subdivisions that are made for various purposes, this is operationally a single program made up of a complex of loops without a beginning or an end. The core of this base level program is the executive control program, often called the main program and abbreviated MP. For a sequential listing of the program instructions

TABLE C

SPC NO. 1A LEVELS OF OPERATION

LEVEL	DESCRIPTION	REMARKS
A	Manual action	
B	Emergency action	
C	Processor mismatch	Maintenance interrupts to recover a trouble-free system
E	Store communication failures	
F	Peripheral unit failures	
G	Store error analysis	
H	Input/output high priority processing	5-ms processing interrupts
J	Input/output low priority processing	
K	Processor diagnostic recording	Storage or diagnostic data, main program
L	Base level	

contained in the executive control program, refer to program listing PR-1C004.

5.10 Interrupts of the base level or of any lower level interrupt program are caused by various conditions in the processor: a time-out of a 5-ms interval by a processor clock causes an H-level or J-level interrupt (used for normal input/output functions); a failure to receive the expected response from peripheral unit causes an F-level interrupt; a mismatch between the active and the standby processors causes a C-level interrupt, etc. When any of these occur, control is seized almost immediately from the program being executed (usually within 6.3 μ s); however, a delay of an additional cycle or two must follow certain special orders. Certain information is saved by the interrupt circuits (including the program address at which the interrupt occurred), and control is given to the program of the interrupting level. Before starting its own work, the latter saves in unprotected memory all other information left in the processor registers by the interrupted program.

5.11 After doing its work, the higher level program restores the processor registers to their original state before returning control to the

lower level program at the point at which it was interrupted, so that the latter program is unaware of the interruption and its processing is unaffected. The exception to this procedure is the 5-ms H-level and J level interrupts. For these interrupts, contents of the index registers are gated automatically into the index image registers by the interrupt circuitry at the time of the interrupt and restored automatically to the index registers when control is returned to the interrupt program. Thus, the control program for each interrupt level can be said to have a beginning (the instruction to which control is forced by the interrupt circuitry) and an end (the point at which it relinquishes control to the interrupt program). However, when programs of all levels are combined with the interrupt mechanism of the processor, a closed system or endless loop again results.

5.12 Certain hard faults and errors create conditions that make return to the interrupted point impossible. In these cases, the return is made to a reference point in the main processing stream where continuity of index register data is not required. All programs at lower levels must defend against this possibility.

5.13 Figure 26 shows the basic SPC No. 1A program control plan. The hierarchy of interrupt sources and the associated programs to which they give control are shown as boxes A, B, C, E, F, G, H, J, and K. The ovals A through E and INTERJECT represent the classes of base level programs. These are preference classes in the sense that the programs in class A are executed nearly twice as often as those in class B, which in turn are executed twice as often as class C, etc. These frequencies are obtained by repeating endlessly the sequence of execution shown on line 1 of Table D. The related repetition rate for each class in the sequence is shown in lines 2 through 6.

5.14 Within each base level class, there is a fixed sequence of program units called task dispensers. The great majority of these are for processing and administration. In general, they dispense program control to one or more task programs a consecutive number of times, depending on the number of tasks the task dispenser program finds waiting.

5.15 Occasionally, another task program is interjected in the flow just described between any two task executions. When a task program returns control to its task dispenser program, the latter checks to see if an interject request has been made and, if so, allows this to be executed before resuming its own dispensing of tasks. Thus, in Fig. 26 the interject class is shown as having a higher preference or priority than any of the five classes (A through E).

5.16 Task dispensers vary greatly in size, complexity, and function. One task dispenser, the maintenance control program, administers a large part of the total SPC No. 1A program. Its structure is explained in Part 6.

5.17 For further explanation of SPC program organization, the total program is divided into two broad categories: processing (with most administrative functions) and maintenance.

B. Processing Program Plan

5.18 For virtually all of the work involved in handling SPC No. 1A traffic, the processor can serve only one input at a time. Thus, it must be time-shared by the many inputs that may be simultaneously in the process of being set up, taken down, or otherwise changed. Moreover, the

system operates in real time; i.e., its inputs are submitted and its outputs demanded at times determined by the outside world, rather than at times decided by the system itself. In addition, the method of sequential program control requires that the input devices such as scanners be passive; i.e., they report information only when the processor program specifically asks for it, rather than initiating action as an immediate response to an input. These basic requirements determine some fundamental characteristics of the SPC plan. Some of the common elements of this plan, occurring in many of the processing and administrative programs, are described here.

Clock Interrupts

5.19 To respond promptly to signals and data submitted to it by inputs, the system must regularly interrogate its scanners rapidly enough not to miss any input. Scanning for most inputs is done in the interrupt level which is initiated by a processor clock every 5 ms, regardless of what is being done by a base level program at that time. Similarly, most outputs must be sent to peripheral equipment (e.g., scanners and signal distributors) on a precise schedule; these too are handled by clock interrupt programs.

Buffers

5.20 A buffer is a general purpose memory area used for storing data until it can be used by the system. A peripheral order buffer (POB) is used to store orders which are transmitted to peripheral units. The buffer memory area is loaded by data processing programs and unloaded by input/output programs.

Task Dispensers

5.21 Task dispensers are the base level programs that unload an assigned buffer. Each entry unloaded represents an analysis and processing task, and this task is dispensed (together with program control) to the appropriate task program. When the task program completes its work, it returns control to the task dispenser, which unloads the next entry and dispenses it appropriately. When all entries in that buffer have been dispensed and processed, the task dispenser program passes control via the executive control program system to the next task dispenser program. When the task dispenser that has just relinquished control receives

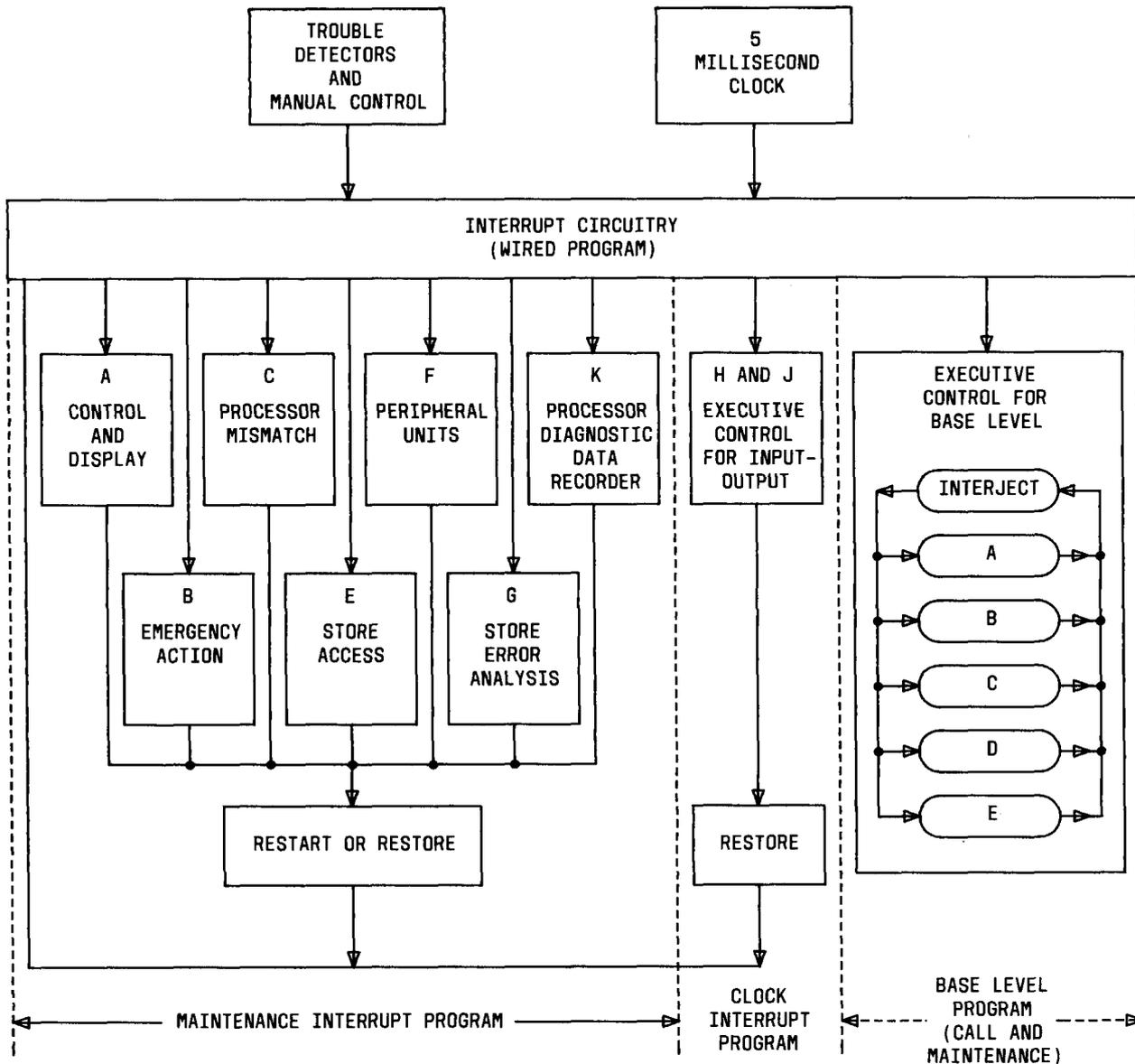


Fig. 26—Program Control Plan

control again, it will again examine its associated buffer and will then unload any new entries that may have been placed there in the intervening time.

5.22 It is sometimes convenient to define as task dispensers all programs that receive control from the executive control program in the same way as the task dispensers just described, even though this definition includes programs that do not truly unload buffers, but rather perform some single timing or other administrative task. Such a

task can be viewed, however, as a special case which, instead of being done only occasionally, is found waiting to be done every time the main program reaches that point in its cycle. Such a definition allows a useful though somewhat oversimplified view of the base level program hierarchy, as:

- (a) Executive control program (main program)
- (b) Task dispenser programs (task dispensers)

TABLE D
BASE LEVEL JOB CLASS EXECUTION

LINE	SEQUENCE
1	ABACABADABACABAEABACABADABACAB
2	A A A A A A A A A A A A A A A
3	B B B B B B B B B
4	C C C C
5	D D
6	E

(c) Task programs (tasks)

(d) Subprograms (subroutines).

5.23 A general explanation of the executive control program (in base level) is given in the overall program plan (paragraphs 5.07 through 5.17). Its operation will be made clearer by examining the ways in which subordinate programs receive and relinquish control.

Task Programs

5.24 The bulk of SPC No. 1A programs are base level, and the bulk of base level programs are task programs. These are the programs at the end of the line of control that perform the ultimate work of the particular application. Most of the processing task programs do a particular kind of work on a single input at a time. Others perform various administrative functions, such as assembling traffic counts to be printed. They differ, too, in the manner in which they receive control from the executive control program. Some receive it directly from a single-task dispenser program, while others require a series of dispensers, each triggering the next.

5.25 A task program rarely retains continuous control for more than a few milliseconds, and only a few exceptional ones hold control for more than 10 ms. Often this fragmentation of work results from the nature of the input. Additional real-time breaks are introduced by the relatively

slow operating time of relays compared to the speed of processor program execution. When no such natural or hardware enforced time break occurs, breaks must be inserted at convenient places so that a single program does not keep control for so long a time that other program functions are excessively delayed.

C. Maintenance Functions

5.26 The SPC No. 1A depends primarily on hardware checking circuits (called trouble detection circuits) for trouble detection during operation. When a trouble detection circuit locates a problem in the system, it notifies an interrupt circuit. The interrupt circuit immediately stops operational program processing and transfers control to the maintenance program associated with the particular type of trouble indication. Maintenance programs comprise a large percentage of SPC generic programming and are described separately in Part 6.

6. MAINTENANCE

SOFTWARE MAINTENANCE

A. Purpose

6.01 As shown in Fig. 27, maintenance programs comprise a large percentage of the SPC generic program plan. Maintenance programs provide trouble-recovery and trouble-isolation routines that keep the system in satisfactory working

condition. These maintenance routines localize troubles and faults within specific SPC equipment units. The maintenance plan provides for:

- (a) Manual intervention when automatic recovery of processing capability fails.
- (b) Trouble detection circuits that sense improper hardware operation; e.g., processor matchers, store error sequencer, peripheral unit ASW and enable-verify signal detectors, etc. Circuit duplication and switching facilities permit satisfactory reconfiguration for multiple troubles as long as mate units are unaffected.
- (c) Fault recognition programs that recover the processing ability of the system upon detection of a circuit trouble.
- (d) Diagnostic programs which automatically test faulty units to isolate troubles.
- (e) Exercise programs that periodically test maintenance circuits not otherwise exercised by the system and that provide back-up testing capability which can be used by the maintenance personnel when automatic fault isolation fails.
- (f) Audit programs that check the data stored in memory.

B. System Status (Manual Intervention)

6.02 When automatic recovery of the processing capability of the system fails, manual intervention is available through the use of the facilities at the CD panel.

6.03 The CD panel is equipped with lamps, keys, and switches to give indications of the system status and to provide means for asserting manual system control. Thus, tests can be initiated and/or individual units can be removed from service in order to maintain a working system.

C. Trouble Detection

6.04 The SPC No. 1A maintenance plan is implemented in part by circuits and in part by programs. A number of different types of trouble detection circuits are used. The primary trouble detection facility incorporated into the processors is the match system which is capable of comparing between processors a number of

internal data source points. To match information between processors, each processor transmits information describing its internal state to the duplicate processor. The match information is buffered in the match registers, and the registers are then compared. Each match operation compares the bits in parallel; i.e., one word of data. The match circuits are designed to operate in a number of match modes. The processor also includes circuits which make checks on facility clock, loss of power, or locked up sequencers.

6.05 The processor can detect and correct single errors in the received word and can detect most multiple errors in the data based on the Hamming error detecting and correcting bits stored with each word in the memory. Within the stores, there are internal timing checks, waveform checks, and 1-out-of-N checks. If all these checks pass, the store transmits an ASW pulse back to the processor together with the bits in the word readout.

D. Fault Recognition Programs

6.06 Fault recognition programs recover an operational system as rapidly as possible from interrupts caused by errors and faults. An error is defined as a malfunction, the symptoms of which cannot be reproduced under program control. A fault is defined as a malfunction, the symptoms of which can be reproduced by the program at will.

6.07 The fault recognition programs are divided into a control program, test programs, and service routine programs. The control program controls the general course of action to be taken. The test programs are programmed questioning of circuits to determine whether or not the circuits respond properly. Service routine programs perform common functions; such as, initializing registers or establishing desired configurations. A common restart program (PR-1C007) used by all maintenance interrupt levels determines at which program point processing should resume, restores the processors to the appropriate state, and returns program control back to the proper level, which could be a lower maintenance level, H- or J-level, or the base level.

6.08 For the processors and stores, there is a one-to-one correspondence between the interrupt level and the fault recognition program.

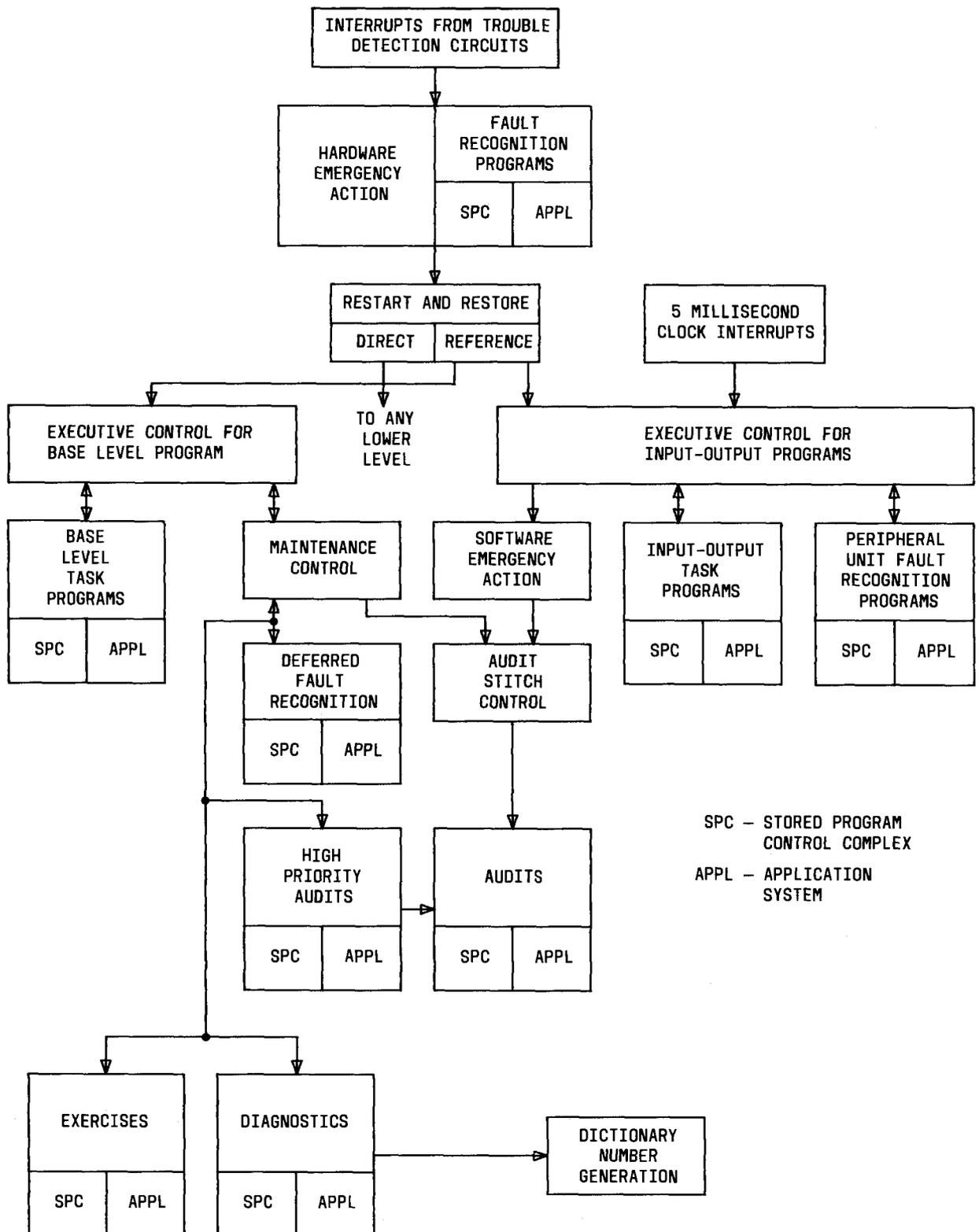


Fig. 27—SPC No. 1A Generic Program

For the peripheral units, the F-level interrupt first leads into a filter program [described in PR-1C025, the central pulse distributor fault recognition (CPFR) program] which determines the fault recognition program to be called in. For example, the scanner fault recognition program (PR-1C028) is called in this way. The signal distributor fault recognition program (PR-1C301) may be required as a result of an enable-verify failure and is initiated in the F-level interrupt in the same manner. However, the bulk of the fault recognition work (retrials and reconfigurations) for slow-acting units such as the SD must be performed in J-level.

6.09 When circuit troubles occur and are detected by fault detection circuits, program control is usually transferred immediately to the fault recognition programs that recover the processing ability of the system. The transfer of program control is implemented by the processor interrupt circuits.

6.10 There are a total of nine interrupt levels designated level A, level B, ..., level K (D and I omitted), in descending order of priority. The base level programs may be interrupted in the manner described previously to begin the execution of one of the nine interrupt programs. Once one of these programs is entered, it in turn may be interrupted to permit performance of higher level interrupt functions. However, with the exception of levels A and B, a given interrupt program may not be interrupted to perform a function at the same or lower level. The high priority programs are assigned to the levels in the interrupt hierarchy according to the relative urgency of the action to be taken.

6.11 In order of descending urgency, classes of maintenance programs are:

- (a) Programs that recover the data processing ability of the system; these programs operate on interrupt levels A through E.
- (b) Programs that recover proper operation of the peripheral system; these programs operate in interrupt levels F and J.
- (c) The store error analysis programs that attempt to isolate the cause of excessive error rates in store system and operate in G and base levels.

- (d) A program that handles processor diagnostic data recording and operates in level K.

- (e) Diagnostic and exercise programs that operate in the base level (level L).

6.12 A mismatch between processors generates a C-level interrupt, whereas a trouble in the peripheral unit is detected in level F or J. Mismatches of duplex answer buses on a scan instruction to a peripheral unit result in C-level interrupts. In the case of a processor mismatch, the data processing ability of the entire system is in jeopardy; in case of a peripheral unit malfunction, the data processing ability is intact, although some services may be affected.

6.13 For the TSPS application system only, SSAS fault recognition programs reside both internal and external to the SPC No. 1A processor. A programmable controller (PROCON) is located in the SSAS equipment to detect faults in equipment which is not directly accessible by the SPC processor. The PROCON detects faults and sends this information to the SPC processor via the SCAB.

6.14 The function of the fault recognition programs is to recover the processing ability of the system. The objectives of these programs in decreasing order of priority are:

- (a) The data processing ability must be recovered as long as a sufficient number of fault-free units exist to form an operational configuration.

- (b) The programs should attempt to minimize interference with the information being processed. Such interference could occur in a number of ways:

- (1) The information handled in the processor at the time of interrupt might be mutilated.

- (2) The information processing ability may be lost for a sufficient time to cause input/output information to be lost. For example, if the store fault recognition program that operates on interrupt level E takes a long time to recover the system, no scanning will take place during this interval and information in process may be lost.

- (c) The faulty unit should be located and switched out of service. In some situations, it may

be possible to recover an operational system without isolating the faulty unit. For example, it may be known that a fault exists in either a store, a store bus, or a processor. By switching out all these units, an operational active configuration can be established. However, isolation of the faulty unit is also considered a function of the fault recognition program but is performed at base level as a deferred task.

(d) The fault recognition program must distinguish between errors and faults. If the fault recognition program determines that an error caused the interrupt, it will make a record of the error. These records are utilized by error analysis programs to recognize abnormally high error rates and to determine the cause of such error rates.

6.15 It is not feasible to design a fault recognition program which will always recover an operational system, isolate the faulty unit, and separate errors from faults rapidly enough so that there is no interference with the processing. For example, if the E-level fault recognition program were to check thoroughly all stores in the system before returning the system to processing, input information to the system would be lost, since such a check would take several hundred milliseconds. Therefore, the fault recognition programs are designed to minimize the **average** recovery time by performing as follows:

- (a) The programs are designed to recover an operational system rapidly (within 5 ms) from the great majority of interrupts; i.e., from interrupts caused by errors and most faults.
- (b) Where the recovery is not simple, whatever time is required to recover an operational system will be taken.
- (c) To expedite the return to processing once an operational configuration is recovered, the isolation of the faulty subsystem and the analysis of errors are postponed where possible and initiated later as a base level program.

6.16 A common restart program (see PR-1C007) used by all maintenance interrupt levels determines at which program point processing should resume, restores the memory and processors to the appropriate state, and returns program control back to the proper level which could be a

lower maintenance level, H- or J-level, or the base level.

E. Diagnostic Programs

6.17 Diagnostic programs are described as follows:

(a) The ultimate end of any diagnostic program is to generate test data that will isolate a fault to a small number of plug-in CPs.

(b) Whether the diagnostic program is requested by a fault recognition program or by the craft personnel via a TTY, the request is first recorded in the maintenance control register (see PR-1C005). The maintenance control register is administered by the maintenance control program, which is periodically entered from the system main program. The maintenance control program recognizes the request for the diagnostic action and initiates the diagnostic program.

(c) Basically, a diagnostic program can be divided into two distinct parts: control (administrative) and the actual tests. The control part determines whether or not the required diagnosis can be undertaken; establishes an appropriate system configuration for diagnosis; initializes the unit to be diagnosed; processes the test results to a form suitable as input to the program which generates the trouble number from the raw diagnostic result (see PR-1C009); and upon termination of the diagnosis, reestablishes the appropriate system configuration.

(d) A diagnostic program carries out a fixed sequence of tests. These tests are performed by observing the normal outputs of a unit or monitoring some special test points strategically located in the unit. The test points may be observed via special diagnostic facilities (such as those used by the control read operation of the stores) or via scan point reading of data on special communication buses (such as the monitor bus of the stores). Test results are recorded in the store and then processed by a number compression algorithm (PR-1C009) to develop the 16-decimal digit number printed on the TTY. This number defines for the craft personnel the CPs to be replaced. The translation from trouble number to the faulty circuit is done with the maintenance trouble-locating manuals. Since the diagnostic programs normally operate at a time when an operational configuration already exists,

they can be assigned a low position in the hierarchy of system programs.

(e) Diagnostic program length may vary from a few milliseconds to several minutes depending upon the unit being diagnosed. To prevent their interference with information processing, diagnostic programs are divided into 10-ms segments. At the end of each segment, the diagnostic program returns control to the maintenance control program which, in turn, returns to the main program. On the subsequent main program visits to the maintenance control program, the maintenance control program initiates the successive segments of the diagnostic program until the diagnostic program has been completed.

(f) The maintenance control program also administers priority across diagnostic programs (processor diagnostic programs are given higher priority than the peripheral unit diagnostic programs), ensures that no program holds the maintenance control register for more than 10 minutes, and performs functions that are common to many of the maintenance programs; such as, timing and control of common maintenance facilities.

(g) Certain parts of the diagnostic programs must be carried out with the maintenance interrupts below level C and with levels H and J inhibited. For example, while a store configuration is being changed, a fully operational configuration may not always exist; therefore, H- and J-level interrupts must be inhibited during this period to prevent return of the system to call processing. Such tests are performed in 2-ms segments. The maintenance control program establishes and removes the inhibit controls in these cases.

F. Exercise Programs

6.18 Routine exercise programs are initiated automatically by the system or they may be requested by craft personnel via the TTY. When the exercises are automatically initiated, the initiation is made by the maintenance control program (PR-1C005). The frequency of executing these exercises is determined by the size and the importance of the circuit being checked and by the length of the program required for checking. Routine exercise programs for the SPC are the processor program (PR-1C017), store program

(PR-1C021), central pulse distributor program (PR-1C027), and scanners program (PR-1C029).

G. Audit Programs

6.19 Proper SPC No. 1A operation depends heavily on the accuracy of the store memory. Errors in the information stored in the memory of the stores may affect single inputs or leave registers unnecessarily busy or, at worst, may cause a cumulative effect that completely paralyzes normal processing.

6.20 Memory errors can be caused by circuit errors or, during early stages of system life, by latent program or design bugs. Store Hamming and parity checks and matching between processors will help prevent memory errors.

6.21 If the system is not operating in a duplex configuration, circuit errors can still go undetected and cause memory errors. For example, when the system is operating with one processor, some errors it makes in the store address or data may go undetected.

6.22 There are basically two defenses against memory errors: defensive programming and audits. Defensive programming is program design techniques which take into account the possibility of memory (or other) errors and which attempt to immunize the program against such errors. For example, a program may include checks on reasonability of the data, or one sequence of performing a series of tasks may be chosen as being safer than others in terms of consequences of processing errors. The defensive program aspects of each program are described in individual program specifications (PDs).

6.23 The defensive program techniques attempt to prevent the errors or their effects; the audit programs are corrective programs which audit the memory for inconsistencies and correct the inconsistencies found.

6.24 Upon finding an inconsistency, the audit programs correct the memory by either reconstructing the information or reinitializing the memory so that it and associated equipment are freed for future use. The audit programs will run routinely at base level on a low-priority basis; they may be called in via TTY or other programs; or they may be executed as a part of software

emergency action. The control of audits is administered by the maintenance control program (see PR-1C005). The generic audit programs are described in PR-1C019.

H. Error Programs

6.25 A class of maintenance programs called error programs is provided to perform both a trouble detection function and a system recovery (trouble isolation) function. These programs are generally concerned with hardware troubles which are intermittent or not consistently reproducible. Troubles of this nature may elude the normal trouble detection mechanisms; e.g., a store may frequently require a reread, but the reread always passes and no interrupt is generated. Even if detected by normal trouble detection mechanisms, intermittent troubles may not be reproducible by the fault recognition programs that normally recover the systems and isolate failed units.

6.26 Error programs handle troubles of this nature by integrating trouble experienced over a period of time. This integration allows **fault detection** (e.g., high number of processor interrupts in a short time meaning something is wrong) and **fault isolation** (excessive store errors that may be traced to a particular store). Error programs usually accomplish trouble detection by retaining overall counts of transient trouble symptoms (store errors, interrupts, etc.) and then periodically comparing these with established limits. Once the presence of a recurring trouble has been established, error programs attempt to isolate the trouble by recording pertinent characteristics for each type of trouble incident and then correlating these characteristics in an attempt to find a common denominator of equipment.

I. Emergency Action Facilities

6.27 Hardware troubles are normally detected by trouble detection circuits and then the call processing ability of the system is recovered by means of fault recognition programs. The audit programs are designed as a defense against unprotected data mutilation problems. This approach requires a reasonably good processor or a reasonably good state of memory. The circuit trouble may be in the active processor or store system and of such a nature that it prevents the fault recognition program from performing any valid actions. Similarly the audit programs are executed on low system

priority levels; if the memory mutilation disrupts the normal program flow, the audit programs may never have a chance to correct the memory. To recover a sane hardware configuration, a combined circuit-program facility named hardware emergency action was designed. To recover from situations where the memory is so altered that call processing is seriously affected and the audit programs are unable to correct memory, a software emergency facility called call processing recovery was designed.

6.28 The hardware emergency action circuit is activated by certain check circuits or timers in the processor; e.g., by sanity timers which the program must reset periodically. Once activated, the emergency action circuit establishes various combinations of processors and store buses. Once a configuration is assembled, the program (operating on B-level) is used to determine whether or not the assembled configuration is operational. If not, a new B-level interrupt occurs and a new configuration is established and tested. New configurations are tried until a good configuration is found.

6.29 The mutilated data recovery operation is activated by certain checks on programs (e.g., by failure to complete E-to-E base level cycles in a given amount of time) or by an excessive rate of maintenance interrupts. The data recovery is divided into phases which are executed until an operational memory is obtained.

6.30 Both recovery facilities were designed as backups for the normal recovery facilities and should occur very infrequently in normal system operation. The emergency action program facilities are described in PR-1C015.

J. Trouble Location

6.31 Once a faulty unit has been switched out of service and operational configuration has been established, it remains to:

- (a) Test the faulty unit
- (b) Translate the test results to the location of the fault
- (c) Repair the fault.

The tests are performed by diagnostic programs. The test results are translated into the location of the fault by means of trouble-locating manuals

and/or program supplementary information (PK) documents. The repair, in most cases, consists of replacing the faulty CPs.

HARDWARE MAINTENANCE

6.32 When catastrophic failures of the SPC No. 1A occur, the PERC unit is used in conjunction with the dead start feature to provide craft personnel with a tool that will permit efficient recovery of a sane system. The PERC unit provides offices with the ability to control and monitor SPC No. 1A processor actions.

6.33 Through the use of the PERC unit, craft personnel can perform prescribed selected tests on a processor and have the results of these tests displayed for interpretation. The unit provides the ability to read memory, write into protected and unprotected memory, and enter selected programs to effect controlled testing of the processor or other units. Section 212-820-302 (ETS) and Section 250-110-302 (TSPS) detail the procedural use of the PERC for emergency recovery conditions in offices equipped with the dead start feature.

6.34 When manual troubleshooting, adjusting, and maintenance of SPC No. 1A equipment frames is required, the following portable maintenance equipment and tools (or equivalent) are recommended:

- (a) Tektronix 453 oscilloscope model 221T with scopemobile; probe
- (b) Hewlett-Packard model 428B clip-on DC milliammeter (0 to 10 amperes)
- (c) Bell System KS-14510 L1 model 6300 meter; 20,000 ohms/Vdc; 3,000 ohms/Vac
- (d) 158A and 159A adapters for testing of CPs; three of each per office
- (e) 723A tools for withdrawing CPs from apparatus mountings.

6.35 In addition, various specialized test and maintenance sets described in the following paragraphs are available for use with SPC No. 1A PBT store frames.

6.36 The SPC No. 1A store test set, SD-1C281-01:

- (a) Scans all store addresses checking for ASW errors and data errors
- (b) Provides store write patterns which are used for evaluation and debugging
- (c) Provides a store strobe window when used with the digital strobe set SD-1C282-01.

6.37 The SPC No. 1A store test set is housed in an aluminum box approximately 19 by 15 by 11 inches with a light gray textured-vinyl finish. The hinged cover is 3 inches deep and is used to store the cable and connectors. A ventilating fan is mounted on the aluminum box.

6.38 On the front panel there are 3 connectors, a Nixie display, 70 toggle switches, 53 lamps, 1 fuse, and 2 handles.

6.39 Attached to the bottom of the first panel are three power supplies and one board that contains all electronic components.

6.40 The digital strobe set, SD-1C282-01, is used with the SPC No. 1A store test set to obtain the optimum adjustment of the A277 circuit pack, which is used in the SPC No. 1A store frame.

6.41 The digital strobe set consists of three printed wiring boards, two thumbwheel switches, three lamps, and a position for inserting the A277 circuit pack to be adjusted. A decorative cover is placed over the support structure.

6.42 The exposed portion of board A is inserted into store position 126-24.

6.43 The PBT store demagnetization set, SD-1C283-01, is used to demagnetize bit wires in the PBT modules. Demagnetization is accomplished by applying a decaying alternating current to the bit wires in all four PBT modules of the store.

6.44 The demagnetization set is housed in an aluminum box approximately 16 by 10 by 10 inches with a light gray textured-vinyl finish. The hinged cover is 2-1/2 inches deep and is used to store the printed wiring boards and cables.

- 6.45** On the front panel there are two switches, two lamps, two cable connectors, a pin jack, a fuse, and an AC ammeter.
- 6.46** Attached to the bottom of the front panel are the motor drive variable transformer (T2), the isolation transformer (T1), the 24-volt transformer (T3), the TST relay, and two diodes.
- 6.47** The 24-volt transformer is used to supply the TST relay, which is used as a safety feature. The TST relay will operate only if both printed wiring boards are plugged into the store frame. The diodes are used for contact protection.
- 6.48** The external match interrupt circuit, SD-1C121-01, provides the capability of detecting a particular program address and provides an output pulse whenever the address is recognized. The circuit consists of three boards that plug into the SPC processor circuits. One board provides feed-through of input paths, one board provides an output path to the opposite processor, and one board contains the octal switches and circuitry necessary to recognize the address specified.
- 6.49** The bootstrap transfer card extender is used to manually bootstrap the SPC No. 1A system.
- 6.50** The bootstrap transfer card extender causes the fetch for the first instruction of the interruption program to be modified to always fetch the first instruction of a bootstrap program at location 010. The clamp-store-name-flip-flop in the processor is reset to allow store name codes other than name code 01.
- 6.51** This specially wired card extender, when combined with an A6-type circuit pack and inserted into the processor test connector at location 106-22, will cause a transfer to one of the two duplicated bootstrap programs when the POWER key is operated and a program interrupt occurs.
- 6.52** The NAME key on the bootstrap transfer card extender may be set to either store name code 01 or 36. Store name code 02 is also selectable but should be regarded only as a spare, since no bootstrap resides there at present.

7. GLOSSARY

7.01 The following is a glossary of certain terms pertinent to the SPC No. 1A.

Active The state of a unit, circuit, etc., when it is handling the switching or other functions for which it was normally intended.

Address The identity of a location in a storage device or equipment unit.

Address Register A register in which an address is stored.

Binary Number System A number system that has two symbols (usually denoted by 0 and 1) and two as its base, just as the decimal number system used ten symbols (0, 1, 2, 3, 4, 5, 6, 7, 8, 9) and ten as its base.

Bipolar Pulse A pulse that has both positive and negative polarity.

Bistable Pertaining to a device capable of assuming either one of two stable states.

Bit (a) An abbreviation of "binary digit." (b) A single character of a language employing two distinct kinds of characters.

Buffer (a) An isolating circuit used between two other circuits. The isolation may be between high-speed and low-speed circuits, between high-impedance and low-impedance circuits, etc. (b) An isolating circuit used to avoid reaction of a driven circuit on the corresponding driving circuit. (c) A storage device used to compensate for a difference in rate of flow of information or time of occurrence of events when transmitting information from one device to another.

Bus One or more conductors over which information is carried from any of several sources to any of several destinations.

Central Pulse Distributor That part of a system which provides the control unit of the system with means for distributing high-speed control pulses to various system circuits.

Circuit Pack A compact assembly containing mounted electrical and/or electronic components interconnected so as to form one or more discrete circuits and

arranged so that it can be inserted into a connector to become an integral part of an overall group of circuits or a system. In some circuit packs, the components are not interconnected but become functional as part of a circuit when the circuit pack is inserted into a connector. Such circuit packs, therefore, are merely a convenient mounting arrangement for the components.

Clock (a) A device that generates periodic signals used for synchronization. (b) A device that measures and indicates time.

Communication Bus Same as Bus.

Counter A device (such as a register) or a storage location used to record the number of occurrences of an event.

Data Any coded information, particularly as taken in, operated on, or put out by a computer or other machine for handling such information.

Diagnostic Program A program that is applied by a system to effect a sequence of operations aimed at localizing a fault to a small number of circuit packs or other types of equipment. The program is applied either automatically upon detection of a fault by a built-in fault-detection operation performed by the system or as a result of a manual request.

Electromechanical System A mechanical system actuated or controlled electrically.

Emergency Action Facility A combined circuit-program facility designed to recover an operational system either by reconfiguring hardware or reinitializing memory when normal recovery means fail to do so.

Enable Pulse A pulse that causes a unit or circuit to become operative.

Error A malfunction the symptoms of which *cannot* be reproduced under program control.

Fault A malfunction the symptoms of which *can* be reproduced under program control.

Fault Recognition Program A program used to recover the call processing ability of the system after a fault and to find the faulty unit.

Ferrod A current-sensing device used in scanners and other equipments having comparable functional capabilities for supervisory and other purposes.

Flip-Flop A circuit capable of assuming either of two stable states at a given time (set or clear), thereby storing a bit of information. It remains in either state until a signal changes it to the other state.

Gate A circuit having an output and a multiplicity of inputs so designed that the output is energized *only* when certain input conditions are met.

Hardware Physical equipment such as mechanical, magnetic, electrical, or electronic devices.

Input Message Data addressed to a system by means of a maintenance TTY or other media to request the system to do such things as: execute various diagnostic programs and report the results, perform tests and report the results, report the status of its parts, report traffic information, and introduce changes into its memory.

Interface The place at which independent systems meet and act on or communicate with each other.

Interrogate To determine the state of a device or circuit.

Logic Circuit That type of circuit having the ability to select one of a multiplicity of output conditions depending upon the type or the coincidence nature of one or more inputs.

Magnetic Latching Relay A type of relay which, on application of an operate current pulse, will remain in the operated state after the pulse is removed and until a release pulse is applied.

Maintenance Any activity intended to keep equipment in satisfactory working condition, including tests, measurements, replacements, adjustments, and repairs.

Master Control Center That part of a system which includes the manual means for controlling the system and the administration of maintenance procedures.

Master Scanner That part of a system which provides the control unit of the system with information access to scan points of test and alarm

circuits and scan points of other circuits that are not equipped with their own scanners.

Memory The faculty or medium for retaining information.

Microsecond One millionth of a second. Denoted as μ s.

Millisecond One thousandth of a second. Denoted as ms.

Module A unit of equipment capable of being combined with others to form a larger unit.

Multipled An arrangement where two outputs, one from each of two units, are connected in parallel.

Network A system of interconnected elements.

Nondestructive Read A read process that does not erase the data in the source.

Output Message Data delivered from a system by means of a maintenance TTY, tape printer, or other medium after the system has performed certain operations that were automatically initiated or manually requested. The data may be delivered in code form. This data, when matched with data contained in a trouble-locating manual, helps to locate trouble in the system or reveals the status of parts of the system or information pertaining to traffic conditions.

Parity Bit A bit appended to a word to make the total number of ones, including the parity bit, odd (or even).

Parity Check Verification of the validity of a binary word by determining whether the number of ones in the word is odd (or even).

Peripheral Unit One of a number of parts of a system that is used with the basic processing and store units to effect overall system operation; examples of such units are scanners, signal distributors, the master control center, etc.

Processor That part of a system which exercises major control of the system through the translation of data in accordance with stored program instructions.

Program An organized set of instructions used to control system functions.

Read (a) To extract information from the memory of a storage device. (b) To determine the state of a device or circuit.

Real Time (a) Pertaining to the actual time during which a physical process occurs. (b) Pertaining to the performance of a computation during the actual time that the relating physical process occurs in order that results of the computation can be used in guiding the physical process.

Redundancy The provision of duplicate equipment and facilities to make possible continuity of service in the presence of trouble in either one of the equipments or facilities.

Register (a) A functionally associated set of memory elements, with or without its controls. (b) A word repository.

Reset (a) To place a binary cell in its initial or zero state. (b) To restore to the original state or starting position.

Routine A sequence of programmed instructions intended to perform a particular function.

Scan To examine sequentially, part by part.

Scanner That part of a system which provides the processor with information access to each of a plurality of inputs.

Scan Point An address that, when read, reveals certain information, such as the status of a line or trunk.

Set (a) To place a storage device into a specified state, usually that state denoting 1. (b) To place a binary cell into the state denoting 1.

Signal Distributor That part of a system which acts as a buffer for and provides access to the control unit of the system for the control of relays in trunks, junctors, and other circuits.

Software Programs, routines, documents, etc., associated with a system.

Standby The state of a unit, circuit, etc., when it is not handling the switching or other functions

for which it was normally intended but is able and available to do so. A unit, circuit, etc., in the standby state may perform certain work, such as checking operations or matching against the active unit, circuit, etc.

Store A repository for information, comprising memory, access, and control. For *equipment* purposes, store may be prefixed by adjectives suggesting the nature of the memory medium of other salient features; such as, piggyback twistor store, magnetic core store, etc.

Stored Program Control A mode of operation of a system in which a series of coded instructions (the program) used to control data manipulation and decision-making functions are stored in a memory and read out and acted upon sequentially.

Stored Program Control No. 1A An electronic, word-organized, data processing equipment having character packing and unpacking capabilities and incorporating a stored program. The latter controls a continuous monitoring of the state of circuits of a system caused by external influences such as the action of operators or customers. It records this state, compares it with the previous state, and then causes the switching circuits to assume a new state as specified by the information in memory.

Subroutine A routine that is common to a number of other routines.

System An assemblage of all of the facilities, united by some form of regular interaction or interdependence, required to accomplish a comprehensive function or functions.

Time-Shared A method of performing many tasks simultaneously by monitoring the progress of each

task and performing the next step in each task when required.

Translation The operation of converting information from one form to a different form.

Translator (a) A device for converting a word from one form (code) to another; for example, from binary to decimal. (b) A network or system having a number of inputs and outputs and so connected that signals representing information expressed in a certain code, when applied to the inputs, cause output signals to appear which are a representation of the input information in a different code. (c) A device that converts information relating to a particular call to a form needed for the subsequent operation.

Trouble A malfunction or other condition that causes a deviation from normal system operation.

Trouble-Locating Manual A document containing information used to locate trouble in a system employing a diagnostic program.

Trouble Number A number (or alphanumeric) used as an index and associated with one or more specific test failures or test conditions. Trouble numbers are listed in an orderly sequence in trouble-locating manuals.

Unipolar Pulse A pulse which has only one polarity (either positive or negative).

Word A set of characters associated to express system information. The term "word" may be prefixed by an adjective describing the nature of the characters; such as binary word.

Write To introduce information into the memory of a storage device.

8. ABBREVIATIONS

8.01 The following is a list of abbreviations used in this section and the words they represent:

ABBREVIATIONS	WORDS		
ABC	Auto Bill Calling	MR	Memory-to-Register
ACTS	Automated Coin Toll Service	MS	Master Scanner
AIR	Address Image Register	OST	Originating Station Treatment
ASW	All Seems Well	PBT	Piggyback Twistor
ASW-S	All Seems Well Scanner	PD	Program Specification
BNS	Billed Number Screening	PERC	Processor Emergency Recovery Circuit
CBT	Communication Bus Translator	PFT	Peripheral Function Translator
CCIS	Common Channel Interoffice Signaling	PK	Program Supplementary Information
CD	Control and Display	POB	Peripheral Order Buffer
CD-PT-TTY	Control and Display, Program Tape, Teletypewriter	PR	Program Listing
CP	Circuit Pack	PROCON	Programmable Controller
CPD	Central Pulse Distributor	PSC	Peripheral Scanner
DS	Direct Signaling	PTU	Program Tape Unit
ESS	Electronic Switching System	PUAB	Peripheral Unit Address Bus
ETS	Electronic Translator System	ROM	Read-Only Memory
FBOOT	Fast Bootstrap	RTA	Remote Trunk Arrangement
IGFET	Insulated Gate Field Effect Transistor	SCAB	Scanner Answer Bus
IPS	Inches Per Second	SCCS	Switching Control Center System
MAD	Module Administration	SD	Signal Distributor
MAR	Memory Access Register	SPC	Stored Program Control
MCC	Master Control Center	SSAS	Station Signaling and Announcement Subsystem
MORSTR	More Store/Bus	SSD	Supplementary Signal Distributor
		STP	Signal Transfer Point
		TSPS	Traffic Service Position System
		TTY	Teletypewriter
		WRMI	We Really Mean It