

CIRCUIT DESCRIPTION

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ELECTRONIC SWITCHING SYSTEMS
NO. 1
ARRANGED WITH 2-WIRE AND DATA FEATURES
TRUNK SWITCHING CIRCUIT

CHANGES

D. Description of Changes

- D.1 On sheet D1, an error in the cross connection information notes for B-Link wiring is corrected.

BELL TELEPHONE LABORATORIES, INCORPORATED

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ELECTRONIC SWITCHING SYSTEMS

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ARRANGED WITH 2-WIRE AND DATA FEATURES

TRUNK SWITCHING CIRCUIT

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SECTION I - GENERAL DESCRIPTION1. PURPOSE OF CIRCUIT

1.01 The trunk switching circuit establishes a metallic tip-ring path between any pair of input terminals (trunk terminals) and a pair of output terminals (link terminals).

2. GENERAL DESCRIPTION OF OPERATION

2.01 The network fabric of the trunk switching circuit consists of four octal grids. The grids are numbered 0, 1, 2, and 3. These grids are functionally divided into two groups, each group containing two grids. Group 0 consists of grids 0 and 1 and associated logic circuits, registers, translators, a high current pulser circuit, and test circuits. Similarly, the same amount of circuitry is associated with the second pair of grids, grids 2 and 3; these circuits are referred to as group 1. Both groups of circuits are functionally independent. Both circuit groups may be enabled and addressed simultaneously; also connections may be set up and tests may be performed simultaneously.

2.02 This duplication gives the circuit a relatively high traffic handling capacity. New connections may be established at a rate of 100 per second. Each of the two major groups of circuits contains some circuitry which is not used while the circuit works into its normally associated pair of grids. These added circuits, combined with some intercircuit group wiring, make it possible for one circuit group to work into the alternate pair of grids. In such a case, one circuit group would control all four grids.

2.03 One circuit group may be out of service because of circuit failure of routine maintenance without losing the control of any of the grids. The only effect on the over-all operation of the trunk switching circuit is that the maximum traffic handling capacity has been reduced to half its normal maximum rate.

2.04 The circuit receives all its information from the peripheral bus circuit. The circuit returns verification signals to the peripheral bus circuit. The trunk switching circuit receives this information in the form of high-speed 0.5-USEC pulses on a specific number of leads. Each of the two major circuit groups connects to the peripheral bus circuit by means of 76 wires. Half of these wires go to the 0 half of the bus circuit, and the other half go to the 1 half of the bus circuit. The 0 and 1 parts of the peripheral bus circuit represent the two sources from which the circuit may receive its information. Valid information requires that pulses are

present on only thirteen of the wires at any time. Furthermore, these pulses must appear simultaneously and on specific groups of wires. The information from the peripheral bus circuit contains three major types of data: link data (28 bits), order group data (6 bits), and administration data (2 bits).

2.05 The link data specifies where in the network fabric some action should be performed. The order group data specifies what action should be performed, and the administration data specifies which of the two major circuit groups of the trunk switching circuit should execute the information and also from which bus the circuit should accept the information. The administration data includes such information as enable signal and reset signal.

2.06 The sequence of events during the execution of an instruction is controlled by internal circuitry. Central control is kept informed as to the status of the operation by means of special connections to the master scanner circuit. Each circuit half can execute different instructions at a maximum rate of 1 every 20 ms.

2.07 The circuit has three modes of operation: normal mode, test point access mode, and quarantine mode. In addition, the power may be removed from either circuit group by operating a power-off key. The power can only be removed from one circuit group at a time. When power is removed from either of the two circuit halves, the remaining active circuit automatically assumes control of all four grids.

2.08 In the normal mode of operation, the circuit is capable of operating simultaneously in both pairs of grids. Information is returned to the central control to indicate the status of either circuit group at any particular time.

2.09 The circuit is in the test point access mode if either of the two major circuit groups is connected to the diagnostic bus. The change in mode of operation is initiated by the central control. One circuit group can be put into the test point access mode only by the other circuit group. Similarly, the circuit can only be restored to normal mode of operation by an instruction from the central control. In the test point access mode of operation, a number of circuit test points are connected to the master scanner circuit via the diagnostic bus. This provides central control with more detailed information as to circuit behavior. The operation of the trunk switching circuit in the test point access mode is similar to its operation in the normal mode.

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2.10 The central control may take either of the two major circuit groups out of service by transmitting an instruction to quarantine that group of circuits. When a circuit group is quarantined, it no longer has access to any of the grids. In a quarantine mode of operation, the remaining active circuit group has control over all four grids. Test point access mode may be combined with a quarantine mode. A circuit group may be taken out of service. Test point access allows the system to perform more detailed diagnostic operations on that particular circuit half. The circuit may be restored to normal mode

of operation by an instruction transmitted to the remaining active circuit group.

2.11 Power may be removed from one of the two circuit groups only by manually operating a power-off (OFF-0 or OFF-1) key. Whenever power is removed from one of the two major circuit groups, the remaining active circuit automatically assumes control over all four grids.

2.12 Power can only be restored by manual operation of the NOP key. After power has been restored, the circuit is left in a quarantine mode.

SECTION II - DETAILED DESCRIPTION1. BUFFER REGISTER AND TRANSLATOR (FS 1)

1.01 The buffer register and translator circuit consists of two parts, circuit 0 and circuit 1, which are nearly identical. The operation of circuit 0 is similar to the operation of circuit 1. The following detailed description of circuit 0 also pertains to circuit 1; the description can be applied directly to circuit 1 by adding 16 to all cases where equipment locations are mentioned.

1.02 The buffer register and translator circuit connects to the communication bus circuit for peripheral units by means of two major groups of leads. The communication bus circuit for peripheral units will be referred to as the communication bus circuit in the following description.

1.03 The two groups of address leads are identified by their lead designation OAD00-CAD35 and 1AD00-1AD35 and connect to either the 0 or 1 half of the communication bus circuit as indicated by the first digit of the lead designation.

1.04 The link data and order group data are received over these leads. The circuit may accept this information from either circuit 0 or circuit 1 of the communication bus circuit depending upon how the buffer register and translator circuit is enabled (leads ERO or ER1). The information is present on the address leads as negative-going pulses which are normally 0.5 USEC wide. Each address lead should remain at a quiescent nominal dc potential of +24 volts. When a pulse is present, the potential on that lead should momentarily change to ground and remain at this potential for approximately 0.5 USEC. The presence of such a pulse is referred to as the presence of a bit. The last two digits of the lead designation of each address lead signifies the bit position. The buffer register and translator circuit uses all bit positions from 00 up to and including 21, and bit positions 24 up to and including 35. The bit positions 22 and 23 are not used in the trunk switching circuit.

1.05 The trunk switching circuit is arranged to receive information on these 34 address leads as several groups of 1 out of N rather than in binary form. The information which is received as negative pulses in certain bit positions is stored in the buffer register. This stored information is translated into a 1-out-of-8 selection in five different groups, and two groups of 1 out of 2 selections each.

1.06 A 1-out-of-8 selection is performed in groups 1, 2, 3, 4, and the order groups. A 1-out-of-2 selection is performed in groups 5 and groups 6 (C0, C1).

1.07 The 1-out-of-8 selection in group 1 is derived from a 1-out-of-4 selection using bit positions 00, 01, 02, and 03, and 1-out-of-2 selection using bit positions 16 and 17. Similarly, group 2 uses bit positions 04, 05, 06, 07, and 18, 19. Group 3 uses bit positions 08, 09, 10, 11, and 20, 21. Group 4 uses bit positions 12, 13, 14, 15, and 24, 25, and the order group uses bit positions 30, 31, 32, 33, and 34, 35.

1.08 Groups 5 and 6 do not require any translation. The 1-out-of-2 selections in these two groups are determined directly by the bits present in positions 26, 27, and 28, 29.

1.09 The buffer register and translator circuit serves two primary functions: to store the combination of high-speed pulses received from the communication bus circuit, and to translate the state of the buffer register into a number of selected metallic paths.

1.10 The circuit contains 4-bit register boards and 1-out-of-8 translator boards. Each register board contains four bi-stable circuits or flip-flops. The 1-out-of-8 translator boards contain reed relays which have the contacts interconnected in such a manner that continuity may be established between the common terminal 27 and any of its eight output terminals. Each register board has two terminals, 8 and 5, which are referred to as enable terminals. These terminals are common to all flip-flops on a board. Furthermore, each bi-stable circuit has a single output terminal. The bi-stable circuit is considered to be set or reset if the dc potential on this output terminal is ground or +24 volts, respectively. Each bi-stable circuit on a board becomes reset as a positive pulse is applied to terminal 12 and ground is applied to terminal 3. All flip-flops of the register become reset if a positive pulse is applied to the RR lead, and ground is present on the RG lead. This positive pulse is nominally 0.5 USEC wide. Each of the two enable terminals is associated with an input terminal in such a manner that a flip-flop becomes set if the positive pulse appears on terminal 8 at the same time that a negative pulse appears on terminal 6. Similarly, the flip-flop also becomes set when a positive pulse appears on the enable terminal 5 the same time that a negative pulse appears on terminal 4.

1.11 In order to set any of the flip-flops on a printed circuit board, the same requirements of coincidence between signals on an enable terminal and an input terminal must be met for all other circuits on the same board. The nominal time of coincidence between these two pulses should be approximately 0.5 USEC. When a positive pulse is present on the ER0 or ER1 lead, the buffer register will respond to signals present on either the 0 or 1 half of the communication bus circuit. The positive enable pulse is nominally 2.6 USEC wide, and the negative pulse on the input terminal is nominally 0.5 USEC wide. The flip-flops which are set remain in this state until a positive reset pulse appears on the RR lead and ground is present on the RG lead. All output terminals of the register boards are connected to input terminals of the translator boards except for two flip-flops located on board 2810. Whenever a flip-flop is set, a reed relay on a translator board operates. At least two reed relays on a translator board must be operated in order to establish continuity between the common terminal 27 and any of eight output terminals. Furthermore, one of the two reed relays operated must be associated with terminal 4 or 0; the second relay is associated with one of the remaining four input terminals. In this manner, an input state of 1-out-of-2 plus 1-out-of-4 is converted into a 1-out-of-8 selection.

1.12 Ground present on either terminal 0 or terminal 4 establishes continuity between the common terminal 27 and terminal 2 or 18, respectively. This feature is used specifically on translator board 2802.

1.13 Two translator boards are always operated in parallel. Circuit 0 and circuit 1 of the buffer register and translator circuit differ in respect to the manner in which the bit positions 28 and 29 are terminated on the register boards 2810 and 2826.

1.14 During normal operation of the trunk switching circuit, continuity is established on each translator board between the common terminal 27 and one of the associated output terminals. Terminal 27 of the translator boards are each connected to a cut-through lead. All eight leads connected to the output terminals of a translator board are functionally considered as a group. The groups are numbered, the first digit in the lead designation signifying the number of the group to which the lead belongs. The eight leads in the order group all have the letters OR as part of the lead designation.

1.15 The path through a translator board is part of the operate path of a wire-spring relay. All leads that connect

to the output terminals of the translator boards also connect to a wire-spring relay winding. The operate path is completed at the time of cut-through which occurs after a path has been established through each translator board.

1.16 The outputs C0 and C1 from two flip-flops in location 2810 are not translated. When cut-through takes place, +24 volts is applied through a resistance (20 ohms) to terminal 27 of one set of translator boards. Address bits 28 and 29 are considered the most significant pair of bits in the link data. Cut-through should only take place on one of the two translator boards that operate in parallel in each group. Whenever the flip-flop associated with this C0 lead is set, cut-through occurs on one set of translator boards and when the flip-flop associated with the C1 lead is set, cut-through occurs on the other set of translator boards.

1.17 C0 should always be used when the circuit is in a normal mode of operation. When either of the two major circuit groups is quarantined, C1 is used in the remaining active circuit group when that group is instructed to operate into its alternate pair of grids.

2. GROUP CHECK (FS 2)

2.01 There are two portions of the group check circuit, circuit 0 and circuit 1, that are functionally the same. Circuit 0 is closely associated with circuit 0 of the buffer register and translator circuit. Similarly, circuit 1 is closely associated with circuit 1 of the buffer register and translator circuit. The major function of the group check circuit is to verify that, when cut-through occurs, only one path exists through each of the reed relay translator boards. Only one path in each group should exist. If this is not the case, the group check circuit indicates either that more than one path exists or that no path exists. The group check circuit provides means for connecting the VCT lead to either terminal 1 or 15 of 2608. During normal mode of operation, it is only possible to cut through or connect the VCT lead to terminal 1 of 2608. This occurs when ground is present on the C0 lead. In order to connect or cut through to terminal 15 of 2608, the relay CT1 must be operated. Relays CT0 or CT1 are controlled over the two leads C0 and C1, respectively. When cut-through occurs, +24 volts is connected to the VCT lead. Voltage cut-through should normally occur at some time after the relay CT0 or CT1 has operated.

2.02 Minus 48 volts is connected to terminal 10 of each group check board. Minus 48 volts is connected to terminal 10 of the boards 2611 and 2613 only when the

relay CP0 is released. Minus 48 volts is permanently connected to terminal 10 on boards 2411 and 2413. Due to continuity on each group check board, -48 volts appears on terminals 6, 7, and 8. Each group check circuit contains four group check boards. Group check boards are used in pairs. At the instant of cut-through, a path should exist through each reed relay translator board in the buffer register and translator circuit.

2.03 Plus 24 volts is applied to terminals 2, 3, and 4 of boards 2611 and 2613 at the instant of cut-through. Simultaneously, +24 volts is applied to terminals 3, 4, 5, 8, 9, 10, and 11 of 2608 through the make contact of CT0.0 and the input terminal 1 of 2608. At the instant of cut-through, a transient current enters each input terminal of two group check boards, 2611 and 2613. The group check boards compare the conditions on terminals 6 and 2, 7 and 3, and 8 and 4; an output signal appears on terminals 19 or 22 if an unbalance is detected between any of these terminals in pairs. The comparison of the transient currents are performed on the group check boards. An unbalance exists, for instance, if on terminal 6 a signal is completely missing. Similarly, an unbalance exists if the signal on terminal 6 is larger than the transient current flowing in terminal 2 at the instant of cut-through. The transient current entering terminal 6 and terminal 2 should be very nearly equal. Similarly, the currents entering terminals 7 and 3, and 8 and 4 should be very nearly equal. Terminals 19 and 22 remain at a quiescent dc level of approximately +8 volts.

2.04 Whenever an unbalance is detected, a negative signal appears on either of the two output terminals 19 or 22. A 10-volt negative signal appears on terminal 19 when a transient current is missing on terminal 6. Similarly, if the transient current is less than the reference current on any of the terminals 6, 7, or 8, a negative signal will appear on terminal 19. When the transient current entering terminals 6, 7, and 8 is larger than the reference found on terminals 2, 3, 4, respectively, a negative signal appears on terminal 22.

2.05 A signal on either of the two output terminals is inverted by the circuit 24-09. Terminal 0 or 3 of 24-09 will, therefore, have a positive signal whenever an unbalance is detected. Terminals 6 and 10 of 24-09 are normally high (+24 volts). At the instant of cut-through, the F0 and VCT0 flip-flops of the controller circuit become set and the TCV lead becomes high. If the coincidence of the TCV lead being high and a signal being present on either 0 or 3 of 24-09 exists, flip-flop GC1 or GC0 becomes set.

Either or both flip-flops may become set depending upon whether or not a signal was present on terminal 0 or terminal 3 or on both. When a group check failure is detected, the 3W0 lead goes high due to the reset of flip-flop VCT0. After the group check failure signal(s) has disappeared from terminal 6 and/or 10 of 24-09, the TCV lead is forced low due to terminal 0 of 26-09. This condition ensures that the state of flip-flop GC0 or GC1 will not be disturbed by any circuit actions that follow.

2.06 A large transient current entering terminals 6, 7, or 8 may be due to the condition that more than one path has been established through a translator board in the buffer register and translator circuit. A transient current missing on any of these input terminals may similarly be due to a lack of continuity through one of the reed relay translator boards. A more-than-1 indication (large transient current) is detected if a positive signal appears on terminal 0 of 2409, and flip-flop GC1 is set. Similarly, the absence of a transient current on one or more of the input terminals 6, 7, or 8 produces a positive signal on terminal 3 of 2409, and flip-flop GC0 becomes set. A more-than-1 indication and a less-than-1 indication (the absence of transient current) may exist at the same time. This will set both GC0 and GC1 flip-flops. A group check failure is indicated if either or both of these flip-flops becomes set. Terminals 18 and 21 of 2409 are normally high. A group check failure causes these points to go low. At the instant of cut-through, leads GCR (group check reset) and P are both high. The normal condition is that terminal 1 of 2609 is low. Furthermore, terminal 24 of 2409 is normally high. A group check failure causes terminal 6 of 2609 to go low; the GF (group check failure) lead will also go low.

2.07 When the CP1 (12) contact is closed, ground may be applied to the C1 lead. When a ground is present on the C1 lead, the CT1.0 relay operates and cut-through may be applied to terminal 15 of 2608.

2.08 When the relay CP0 is operated, the circuit is in a non-normal mode of operation (quarantined). Terminals 19 and 16 of 2409 are connected to contact 4 of the CP0 relay. When this relay is operated, the group check failure indication from circuit 0 is inhibited. Operation of contact 5 of relay CP0 also switches network R2.0-C1.0 in series with -48 volts to terminal 10 of group check boards 2611 and 2613 for diagnostic purposes.

2.09 In this non-normal mode of operation, group check circuit 0 is

inhibited. Group 0 circuits of the trunk switching frame are quarantined. However, the 0 circuit half may still be addressed.

2.10 The main function of the group check circuit is to compare the transient currents existing between pairs of terminals. It is also the purpose of this circuit to allow -48 volts to appear on all terminals 6, 7, and 8 of the group check boards through some internal path on each board. This -48 volts is ultimately used in the path selector circuit for the purpose of operating wire-spring relays. In the quarantine mode, relay CP0 is operated, and -48 volts is removed in such a manner that wire-spring relays may not operate while in this mode. On the other hand, it is possible with this configuration to check and exercise the group check circuitry without operating any of the associated wire-spring relays. It is possible to monitor the response of the circuit over the diagnostic bus observing the state of the leads designated GC0 or GC1.

2.11 The BP (bypass) relay is for protection purposes. It operates approximately 1.5 ms after the instant of cut-through. It is the purpose of this relay to short-circuit the group check boards so that in the event of a major problem, the boards will not be damaged by excessive current. This bypass path exists only when the circuit is in a normal mode of operation. In a quarantine mode of operation, the bypass path is opened by contact 6 of the CP0 relay. In this mode, the bypass condition is not required, as the direct connection between terminal 10 on the group check boards and -48 volts has already been removed.

2.12 The group check failure state may be reset by a negative signal on the GCR lead. This negative-going signal resets flip-flops GC0 and GC1, and propagates through circuit packs 2609, terminal 1, and 2409, terminal 24. Similarly, a negative signal on the P lead propagates through the same two circuit packs. A negative signal will, in both these cases, appear on the GF lead.

2.13 The cut-through leads which are connected to the output terminals of 2608 are individually isolated from each other by the diodes on the common diode access matrix board (2608). Each wire-spring relay operate path is isolated by means of this diode board.

3. PATH SELECTOR (FS 3)

3.01 The path selector consists of 76 wire-spring relays. These are double-wound relays, and each winding has a 185C contact protection network connected in parallel. The path selector

interconnects the buffer register and translator circuit and the group check circuit. All wire-spring relays are grouped in the same manner as the output leads of the buffer register and translator circuit. Each group, except for the fifth order group contains eight relays. The four wire-spring relays designated PS are not associated with the buffer register and translator circuit. With the exception of the relays designated PS, each relay may be controlled over either of its two windings. The P30 relay may be operated by +24 volts connected to the P30 lead from buffer register and translator circuit 0 and -48 volts on the G30 lead from group check circuit 0. Similarly, the same relay may be operated by +24 volts appearing on the P30 lead from the buffer register and translator circuit 1, and -48 volts on the G30 lead to group check circuit 1. In this manner, all relays may be operated from either of the two halves of the buffer register and translator circuit.

3.02 At the instant cut-through occurs, +24 volts is connected to one side of the relay winding and the group check side of the relays, which are all strapped together, carry a transient current. This transient current is mainly due to the contact protection network across each winding of the relay. The magnitude and duration of this transient current are controlled by the components of the network. The group check side of the wire-spring relay carries a transient current which is compared with a reference current in the group check circuit. During normal operation of the trunk switching circuit, only one wire-spring relay in any group should be operated. At the instant of cut-through, only one wire-spring relay operate path should exist for each wire-spring relay group through the buffer register and translator circuit. If a path is missing in any of the groups, the transient current will also be missing on the group check side of the relays.

3.03 Similarly, if more than one path exists at the instant of cut-through, too large a transient current will exist on the group check side of the relays. The outside terminals of the primary winding of wire-spring relays is connected together and, furthermore, connected to the group check circuit. Similarly, the outside terminal of the secondary windings is interconnected and connected to the group check circuit. The relays belonging to wire-spring relay groups 1, 2, 3, 4, and 5 all may be operated from either the 0 or the 1 half of the buffer register and translator circuit.

3.04 When a relay is operated from the 0 circuit of the buffer register and translator circuit, group check circuit 0 is used. The buffer register and

translator circuit 0 or 1 is always associated with the same numbered half of the group check circuit.

3.05 The relays in the order group are controlled in a different manner. The two lower-numbered relays are controlled from the buffer register and translator circuit 0. The two higher-numbered relays are controlled from buffer register and translator circuit 1. The corresponding numbered group check circuit is used in each case. The use of the primary winding or the secondary winding depends upon what cut-through has been selected.

3.06 Group checking is not performed on the PS (pulse steering) relays. These four relays are directly controlled from the two group check circuits.

4. CONTROLLER LOGIC CIRCUIT (FS 4)

4.01 The controller logic circuit performs all necessary timing and sequencing needed for the operation of the trunk switching circuit. The circuit also provides high-speed answer signals to the communication bus circuit. The circuit receives information directly from the communication bus circuit. An operating cycle in the following description is considered as the time between the receipt of an enable signal (EN00 or EN01) and the final execution of the instruction.

4.02 An enable signal may be received by controller logic circuit 0 on either the EN00 or the EN01 lead. The receipt of an enable signal sets the corresponding enable flip-flop EN0.0 or EN1.0. The receipt of an enable signal on the EN00 lead initiates the timing and sequencing required to properly generate the enable signal on the ERO or ER1 lead as well as the enable verification signals to the communication bus circuit. An enable signal is a negative-going signal with a nominal width of 0.5 USEC. The receipt of such a signal on the EN00 lead sets the EN0.0 flip-flop. The setting of this flip-flop changes the state of terminal 0 of circuit 2604 from a high state (+24 volts) to a low state (ground). This dc change on terminal 0 initiates a timing sequence which is performed by the timing circuit in location 2404. The negative-going signal on input terminal 7 of 2404 generates a negative pulse 2.6 USEC wide on output terminal 24. This pulse appears inverted on output terminal 21 of circuit 2604 and drives a differentiating network in location 2404 on input terminal 15. The positive timing pulse on terminal 14 of 2604 also connects to input terminals 1 and 2 of circuit 2404. With the EN0.0 flip-flop set, terminal 0 of 2404 will be high. The coincidence of this terminal being high and the 2.6-USEC positive timing pulse on terminal 1 generates a positive pulse on the ERO lead. This pulse is 2.6 USEC wide. The ERO lead

(enable register 0) enables the buffer register and translator circuit to accept peripheral bus information that might be present at that time of the 0 half of the peripheral bus circuit.

4.03 The sequence of events would have been the same if an enable signal had been received on the EN01 lead. In this case, the EN1.0 flip-flop would have become set and the potential change on terminal 6 of 2404 would have generated a similar timing pulse as discussed previously. In this case, terminal 3 of 2404 would be in a high state, and a positive 2.6-USEC enable pulse would appear on the ER1 lead. During the presence of this 2.6-USEC enable pulse, the buffer register and translator circuit is enabled, and able to receive peripheral bus information from the 1 half of the communication bus circuit.

4.04 The ERO and ER1 leads which connect to output terminals 5 and 4 of 2404 enable only the 0 half of the buffer register and translator circuit. The timing and sequence of events are the same in circuit 1 of the controller logic circuit. All sequences and timing discussed for circuit 0 are the same for circuit 1. All references to circuit pack location in circuit 0 should be changed by adding 16 to the 0 circuit pack location.

4.05 The differentiating network located on pack 2404 responds to the timing pulse which appears on its input terminal 15 and generates a positive-going pulse on its output terminal 21. This pulse coincides with the trailing edge of the input pulse and has a nominal width of 0.5 USEC. This pulse resets flip-flop S0, appears inverted at terminal 24 of 2604, and sets flip-flops F0 and VCT0. Furthermore, this negative 0.5-USEC pulse is applied to input terminal 26 of 2604 and is inverted, appearing as 0.5-USEC positive pulse on terminals 7 and 11 of 2406. If flip-flop EN0.0 is set, the coincidence of terminal 10 being high and a positive pulse on terminal 11 initiates the transmission of an enable verification signal to the communication bus circuit over the lead pair EVOOP and EVOON. Similarly, an enable verification signal will be transmitted to the communication bus circuit if the flip-flop EN1.0 had been set. In this case, coincidence would exist between terminal 8 of 2406 and the positive 0.5-USEC pulse on terminal 7 of 2406. The enable verification signal is, in both cases, nominally 0.5-USEC wide. The negative 0.5-USEC pulse appearing on terminal 24 of 2604 sets flip-flop F0 and flip-flop VCT0. The setting of these two flip-flops starts to operate two mercury relays, F0 and VCT0. Relay F0 operates within 1.5 ms while relay VCT is delayed so as not to operate until 2.5 ms after the setting of the associated flip-flop. The relay RRO is held operated during the time

relay F0 is released. When relay F0 has operated, relay R0 starts to release. The voltage-dividing action of the winding resistance of relay R0 and resistors R7.0, R8.0, and R9.0 leaves terminal 25 of 2409 at a quiescent dc potential of approximately +5 volts.

4.06 At the instant relay F0 operates, terminal 25 of 2409 goes low, and terminal 27 of the same board goes high. This is the beginning of the time when group check responses may be detected. The TCV lead serves as a gate to limit the time during which group check responses will be accepted. This is approximately 1.5 ms after the enable signal was received. Approximately 2.5 ms after the receipt of the enable, the VCT0 relay operates. At this time, voltage cut-through has been completed and +24 volts is present on the VCT lead (voltage cut-through). Similarly, at this time, battery appears on the BPO lead. This is the beginning of the time when the bypass relay of the group check circuits is energized. The release of the R0 relay serves to remove ground from terminals 19 and 3 of circuit pack 2402.

4.07 If the group check is successful, the GF lead which terminates on terminal 7 of the VCT0 flip-flop remains high. The cut-through relay is allowed to remain operated for several milliseconds. If, on the other hand, a group check failure is detected, a negative group check failure signal appears on the GF lead. This signal resets the VCT0 flip-flop and starts to release the VCT0 relay. This will open and remove the voltage cut-through condition on the VCT lead. The VCT condition will only have existed for the length of time it takes to release the VCT0 relay. This time is not sufficient to operate any wire-spring relays in the path selected. The circuit remains in this complete state. The two flip-flops R0 and S0 remain in their enabled state of 1 and 0, respectively. While the circuit is in this state, it is unable to respond to further enable signals. It is, therefore, necessary to reset the circuit by means of a signal on either the QAD36 or 1AD36 lead. These two leads are often referred to as the reset leads. If the circuit was initially enabled over the EN0 lead, the EN0 flip-flop would be set. Terminal 8 of 2603 would be high. In order to reset the circuit it is necessary to receive a signal on the QAD36 lead. A signal on this lead appears as a positive 0.5-USEC pulse on terminal 8 of 2603. The coincidence of terminal 8 of 2603 being high and this positive 0.5-USEC pulse on terminal 9 of the same circuit allows terminals 6 and 10 of 2603 to go momentarily negative. The negative pulse at this point resets flip-flop F0, and sets flip-flop S0. The reset pulse also appears on input terminal 15 of 2402 but has no effect,

since at this time, relay R0 is released and, effectively, terminal 18 is high.

4.08 The resetting of the F0 flip-flop starts to release the F0 relay. When relay F0 has released, the R0 relay starts to operate. When the R0 relay has operated, ground is again applied to terminal 18 of 2402 and terminal 3 of the same circuit. The differentiating network portion of 2402 responds to this new application of a ground at its input terminal 3. At this time, a 0.5-USEC negative-going differentiated pulse appears on terminal 10 of 2402. This pulse is inverted by 2603 and appears as a positive pulse on terminal 24. This 0.5-USEC positive reset pulse appears at both terminal 25 of 2404 and terminal 20 of 2603.

4.09 In the first case, a positive 0.5-USEC pulse appears on the RR lead. A positive 0.5-USEC pulse on the RR lead resets the buffer register. This pulse appears approximately 1.5 ms after the release of the F0 relay. The initial release of the F0 relay opens the VCT lead. This stagger in time ensures that the reed relays in the buffer register and translator circuit release sometime after power has been removed from the contacts. This should ensure a dry release of the reed relays. The positive pulse on terminal 20 of 2603 is inverted and appears as a negative pulse on terminal 21 of 2603. This pulse resets the EN0.0 and VCT0 flip-flops. The reset of the VCT0 and EN0.0 flip-flops prepares the circuit to respond to a new enable signal on either of the two enable leads.

4.10 A successful group check allows the VCT lead to remain connected to +24 volts through resistors R8.0 and R9.0. Within approximately 7 ms after closure of the VCT lead, a combination of wire-spring relays operate. This combination is determined by the state of the buffer register and translator circuit. Following the operation of the relay, a pulse appears on the P1 lead to the ferreed pulser and path check circuit. The presence of this positive pulse is an indication of a successful sequence of events. At this time the positive signal on terminal 1 of 2402 is inverted by 2604 terminal 18. The same signal appears on the P lead which goes to the group check circuit. It propagates through the group check circuit and again appears on the GF lead, and resets the VCT0 and F0 flip-flops. This signal, which comes from the ferreed pulser and path check circuit, is an indication that pulse amplitude has been sufficient. At this time, the TCV lead is grounded through terminal 18 of 2603. The resetting of the F0 and VCT0 flip-flops starts the release of both the F0 and VCT0 relays. When relay F0 has released, relay R0 starts to operate, and in about 1.5 ms the

RR0 relay has operated and again a ground is applied to input terminal 3 of 2402. The resetting sequence of events is similar to the one discussed previously. Again, the staggering in time between the opening of the VCT lead and the 0.5-USEC reset signal that is transmitted on the RR lead should be noted. A successful sequence of events results in both the F0 and S0 flip-flops being reset. These are referred to as being in the 0-0 state. The state of these two flip-flops may at any time be monitored by means of leads F0 and S0 which are connected to circuit 2406 terminals 0 and 3. These leads, furthermore, connect to the diagnostic bus and eventually connect to the master scanner for the purpose of monitoring the state of the controller circuit.

4.11 A cycle may be interrupted by means of a reset signal. This signal must appear on either of the two reset leads 0AD36 or 1AD36. The reset signal for the purpose of interrupting the cycle must be received within 5 ms of the enable signal. Furthermore, it must appear on the lead corresponding to the lead over which the circuit was first enabled. The reset signal appears as a negative pulse on terminals 6 and 10 of 2603. It resets the F0 flip-flop and initiates the release of the F0 relay. This, in turn, opens the voltage cut-through lead, and in this manner, interrupts the operation of any wire-spring relays. Furthermore, the reset pulse propagates through the group check circuit over the GCR lead. If the reset signal appears before the RR0 relay has released, the reset signal will appear on terminal 23 of 2402. This negative signal is, in turn, inverted by circuit 2603 and appears as a positive pulse on terminal 24 of this circuit. From this point, the sequence of resetting is the same as for the previous cases. If the relay RR0 had released, the resetting of the enable flip-flops would have to wait until the RR0 relay has reoperated due to the resetting of the F0 flip-flop. From that point on, the sequence of events in the reset chain is the same as discussed previously.

4.12 Lead P0 relay is operated during normal operation of the circuit. It is used during the power-restore sequence. It insures that, immediately following the restoration of power, important flip-flops and circuits are forced to assume the reset state. The P0 relay forces the RR0 relay to operate. The operation of RR0 initiates the same reset sequence as discussed earlier. The RR0 lead insures that a number of flip-flops assume the reset state immediately following the power restoration. The VCT0 lead which connects to terminal 24 of circuit 2406 serves a similar function as the F0 and S0 leads which also connect to the diagnostic bus.

4.13 The description of the functions, the timing, and the sequence of events which have been discussed concerning the 0 circuit of the controller logic circuit also pertains to the 1 circuit. Equipment locations differ only by the number 16, and in some cases the lead designations carry the character 1 instead of 0. Both circuits are independent and may operate in parallel. When one major circuit half of the trunk switching circuit is in the quarantined mode, leads EN and ENM will be connected together through the diagnostic control. This inhibits the quarantined circuit from transmitting enable verification signals to the communication bus circuit.

5. PULSE STEERING (FS 5)

5.01 The pulse steering for grids 0, 1, 2, and 3 interconnect the ferreed pulser and path check circuits and the pulse paths for stages 0 and 1, and resistive dummy loads. Order relays numbered OR1 and OR3 are associated with circuit 0 of the buffer register and translator circuit. The higher-numbered order relays are all associated with circuit 1 of the buffer register and translator circuit. Each relay is associated with a particular instruction to be executed within the trunk switching circuit.

5.02 These instructions and relay numbers are associated in the following manner. Order relay OR1 prepares a pulse path between such wires and of such a pulse polarity that the frame executes a connect order. Order relay OR3 is a test order relay. The operation of this relay steers the output of the ferreed pulser and path check circuit into a dummy load. For each order execution, the pulse path is unique and specific. The ferreed pulser and path check circuit 0 may pulse into grid 0 by means of a number of paths. As an example, continuity between the pulser circuit 0 and a pulse path in grid 0 may be established by the operation of order relay 1 (OR1). The pulser terminal designated PC1 is positive with respect to terminal PC0.

5.03 When a path has been detected, pulse current flows in the following manner: through the released contact of the CP0 relay, through the make contact of the OR1 relay, and out on lead designated E0. The pulsing path is completed back into the pulse steering circuit over the A0 lead; continuity established back through the second terminal of the pulser through operated contact 1 of the OR1 relay and contact 9 of the CP0 relay.

5.04 The operation of relay OR3 establishes a connection between resistor R88 and pulser circuit 0. The continuity in this case between the pulser and the resistor is established through the

released contacts of relay CP0, the operated contact 3 of relay OR3, the closed contact 20 of relay P31, resistor R88, contact 8 of relay CP1, the closed contact 1 of relay OR3, and back to lead PC0 of the pulser circuit. Also the operation of relay OR3 and P34 places a ground on the PC0 pulse lead. The continuity between pulse lead PC0 and ground is established through operated contact 23 of the OR3 relay and 23 of the P34 relay. This ground is established to permit the diagnostic program to test the short to ground circuit of the ferreed pulser.

5.05 The ferreed pulser and path check circuit may gain access to grid 1. The pulse current flows in either grid, depending upon where continuity exists. Continuity should only exist in one grid at a time. The function of the relay PS00 is to steer the output of the ferreed pulser and path check circuit to grids 0 and 1. With the CP0 relay operated, pulser circuit 0 pulses into dummy load resistor R87 whenever PS00 is operated. In this case, resistor R87 provides continuity between the pulser terminals, allowing the pulser circuit 0 in this mode of operation to pulse into a dummy load. When the CP0 relay is operated, the 0 half of the trunk switching circuit is in a quarantined mode.

5.06 The OR3 relay is associated with the test order. With this relay operated, the pulser does not pulse into the grids.

5.07 It is the primary function of the 0 half of the trunk switching circuit to control grids 0 and 1. When the CP0 relay is operated, access to grids 0 and 1 is established only when the PS11 relay is operated. In this case, connections are established between grids 0 and 1 and pulser circuit 1. This is the alternate access to the pulse paths of grids 0 and 1 in the case that the 0 circuit group of the trunk switching circuit is out of service. The order relays numbered OR9 and OR11 are associated with the 1 circuit half of the trunk switching circuit. The output terminals of pulser circuit 1 may pulse into the two grids 0 and 1 if the PS11 relay has been operated. The method of steering the pulse in this case is the same as previously discussed concerning circuit 0.

5.08 The ferreed pulser and path check circuit 1 normally pulses into paths belonging to grids 2 and 3. The operation of relay PS10 steers the pulser into these two grids. In a similar manner, the operation of an order relay steers the pulser to particular portions of the pulse paths. Similarly, the CP1 relay is required in order for the pulser to gain access to these two grids; the OR11 relay is the test order relay in this case.

Pulser circuit 1 may pulse into any one of the three resistors shown: R83, R84, or R85. As an example, the pulser circuit may pulse into resistor R84 whenever the PS10 relay is operated, the CP1 relay is released, the OR11 relay is operated, and P311 and RS1 relays are operated. These pulsing paths are associated with particular test orders.

5.09 If the circuit 1 half of the trunk switching circuit is quarantined, the CP1 relay will be operated. Again, R86 serves as a dummy load for pulser circuit 1. This is associated with features included in the trunk switching circuit for performing automatic diagnosis. As for grids 0 and 1, an alternate pulse path may be established in case the circuit 1 half of the trunk switching circuit is out of service. In this case, access to grids 2 and 3 is made to pulser circuit 0. In this case, the PS01 relay is operated. Access to the grids 2 and 3 is now established in a similar manner as before, by means of the lower-numbered relays.

6. DIAGNOSTIC BUS (FS 6)

6.01 The diagnostic bus circuit provides means for connecting a number of circuit testpoints to the master scanner circuit. These testpoints are used to monitor the operations of the trunk switching circuit. Each testpoint is terminated in a ferrod in the master scanner circuit. Therefore, it is normal to expect to find continuity between any wire and its mating conductor. The diagnostic bus circuit can connect battery and ground to each wire pair. When this is the case, current flows. The state of a test point is considered as being in the 1 state when no current is flowing. Therefore, current flowing in any diagnostic testpoint is regarded as a 0. The diagnostic bus applies battery or ground to the conductors through an 1800-ohm resistance. This provides dc balance of the pair, and also serves as a protective component in case of external troubles.

6.02 The diagnostic bus circuit connects to both major circuit halves of the trunk switching circuit. During the normal mode of operation, all test point access relays are released. These relays are designated T0, T1, TP0, and TP1. Furthermore, the Q0 and Q1 relays are also released. The only connections that exist to the master scanner circuit are the leads designated T0, S0, F0, F1, S1, and T1. Each of these wires has a mating conductor which also connects to the master scanner circuit. The three test points that have the number 0 in their lead designation are all associated with the operation of controller logic circuit 0. Similarly, the three scanpoints containing the number 1 in

the lead designation are associated with the controller logic circuit 1.

6.03 During normal operation of the trunk switching circuit, current should flow in a loop that consists of leads T0 and TOM. The current in this loop is limited by resistors R12 and R18 plus the resistance of the wires and the ferrod in the master scanner circuit. Similarly, current should flow in the loop that contains leads T1 and T1M. In a non-normal mode of operation, relays Q0 or TP0, or both, may be operated. Either of these relays operated opens this monitoring loop and indicates to the master scanner circuit that controller logic circuit 0 is in a non-normal mode. Similarly, the controller logic circuit 1 is in a non-normal mode whenever relays Q1 or TP1, or both, are operated. The absence of current flow in the associated loop indicates to the master scanner circuit that the circuit is in a non-normal mode of operation. The leads designated S0 and F0, which connect to the controller logic circuit 0, are terminated to ground or in an open circuit depending upon the state of the flip-flops that have the corresponding functional designations. If the F0 flip-flop is set, the F0 lead is an open circuit; if the same flip-flop is reset, the F0 lead is terminated to ground. In this case, a current monitoring loop is complete between local ground and battery. This loop consists of resistor R11, the break contact of relay TP0, terminal 2, the break contact 4 of relay Q0, and F0 lead, F0M lead, resistor R17, and terminate at the +24 volt battery lead. No current in this loop indicates that the flip-flop is set, the binary value 1, and current will flow when the flip-flop is reset. In a similar manner, a monitoring loop that is associated with the flip-flop S0 or the S0 lead may be traced. The same pair of loops may be found associated with controller logic circuit 1.

6.04 The three scanpoints S0, F0, and T0, which are associated with controller logic circuit 0, will, at any time, either indicate the mode of operation of that circuit half or the state of that circuit half during a normal operating cycle. The three scanpoints associated with the controller logic circuit 1 will in a similar manner indicate the state of that major circuit half.

6.05 The combinations of states of these scanpoints is associated with seven different states of a major circuit half. If the presence or absence of current in a scanpoint loop is referred to by the binary numbers 0 and 1, respectively, then the meaning of each of the combinations of states are as shown in Table A.

6.06 When controller logic circuit 0 is in a normal mode of operation, the T0

TABLE A

CIRCUIT STATES

STATES	S	F	T
Success	0	0	0
Enabled	0	1	0
Reset	1	0	0
Power Removed	1	1	1
Test Point Access	0	1	1
Test Point Access and Quarantine	0	0	1
Quarantined	1	0	1

scanpoint is in the 0 state; current is flowing in this scanpoint loop. Whenever the 0 circuit is in a non-normal mode of operation, the T0 scanpoint assumes the state 1. The operation of relays Q0 or TP0 opens the monitoring loop associated scanpoint T0. The associated scanpoints S0 and F0 are both disconnected from their previous connection to controller logic circuit 0. The S0 and F0 scanpoints are forced into a particular state depending upon which of the two relays has operated. In the case where relay TP0 operated, the F0 scanpoint assumes the 1 state while the S0 scanpoint assumes the 0 state. The S0 and F0 leads which connect to controller logic circuit 0 now appears connected to the F and S leads which also connect to the master scanner circuit, but at a different location. If only the Q0 relay is operated, the F0 scanpoint is forced into the 0 state due to the connection made to the F0 lead through contact 4 of the Q0 relay. The S0 lead is opened and assumes the 1 state. In the case where both TP0 and Q0 are operated, the two scanpoints S0 and F0 are forced into the 0 states. In this manner, the scanpoints indicate at this time only the mode of controller logic circuit 0. With the TP0 relay operated, the state of controller logic circuit 0 during the execution of an instruction now appears on the leads F and S. The three scanpoints associated with controller logic circuit 1 are controlled in a similar manner.

6.07 A number of additional scanpoints are provided which may be connected to selected points within the trunk switching circuit. These scanpoints may be connected upon request by the switching system. These points all serve the purpose of informing central control by the way of the master scanner as to the over-all

performance of the circuit. These points are a major tool in the automatic diagnosis of this circuit. When relays TP0 and T0 have operated, these scanpoints become connected to test points belonging to the 0 half of the trunk switching circuit. Similarly, when the TP1 and T1 relays are operated, these points become connected to the 1 half of the trunk switching circuit. These monitoring scanpoints can only be connected to one of the two circuit halves at any one time. This is insured by means of an interlock.

6.08 These test points are often referred to as diagnostic points. Each test point is a monitoring loop, which is completed by the ferrod in the master scanner circuit, and battery and ground supply to the loop at the circuit end. The connection between the circuit and the master scanner circuit terminals is often referred to as the diagnostic bus. When the TP0 and T0 relays are operated, test points in the 0 circuit half of trunk switching circuit are connected to the diagnostic bus. This mode is referred to as the test point access mode. In this mode of operation, the S and F leads monitor and indicate the state of the F and S flip-flops in controller logic circuit 0. This information previously appeared on leads S0 and F0. The VCT test point monitors the FCT flip-flop. When this flip-flop is set, current flows in this monitoring loop and is read to be in the 0 state. This test point indicates the beginning of the time when the controller starts to operate the wire-spring relays. Furthermore, this test point returns to the 1 state when the circuit has completed the execution of an instruction.

6.09 The GC0 test point is associated with the group check circuit. Specifically, this lead is associated with that portion of the group check circuit which responds whenever a failure has occurred to establish a wire-spring operate path. Similarly, the GC1 test point is associated with that portion of the group check circuit which responds when more than one operate path has been established in a wire-spring relay group. A group check failure of either kind is indicated by these test points. A failure has occurred when either of these or both assume the state 1 (no current flow).

6.10 The test points designated G1, G2, G3, G4, G5, and OG are all associated with a wire-spring relay group. The G1 test point is associated with wire-spring relay group 1, and the OG test point is associated with the order group. These test points each assume the state 1 (no current flow) when all relays in the associated group are released.

6.11 The STG (short-to-ground) test point is associated with the ferreed pulser and path check circuit. This test point normally should be in a 0 state. Whenever this test point assumes the 1 state, this indicates that the ferreed pulser and path check circuit has detected that a short-to-ground exists somewhere in the pulsing path. This point remains in this state until it has been released by the system.

6.12 By correlating the states and the sequence in the change of states of these test points, it is possible to diagnose malfunctions that may occur in the circuit. The actual state of each test point, the sequence of events, and the duration of these individual states all should reflect and indicate malfunctions that might occur. In this manner, it is possible by means of these diagnostic points to perform automatic diagnosis on the trunk switching circuit.

6.13 The meaning of all these test points is the same for the 1 circuit half of the trunk switching circuit. The 1 circuit half is considered to be in a test point access mode whenever relays TP1 and T1 are operated.

7. DIAGNOSTIC CONTROL (FS 7)

7.01 The diagnostic control circuit provides the means for controlling the mode of operation of the trunk switching circuit. This diagnostic control also contains lamps that indicate the state of the trunk switching circuit. The mode of operation may be changed either by manually operating keys or by means of orders transmitted to the circuit by central control.

7.02 In a normal mode of operation all relays shown on the diagnostic control are released.

7.03 Either of the two circuit halves may be put into a test point access mode by operating relays TP0 or TP1. The 0 circuit half is put into a test point access mode by operating relay TP0. The operation of this relay also operates the relay T0. This TP0 relay may only be operated by an instruction transmitted to the 1 half of the circuitry by the system. The operate path for relay TP0 is from ground through make contact 5 of relay OR11, make contact 18 of relay P310, and release contact 7 of relay TP1. The TP0 relay can only be operated if relay TP1 has previously released. In a similar manner, the operate path for contact 18 of relay P32, and the released relay TP1 is through contact 5 of relay OR3, contact 7 of relay TP0. Whenever the TP0 relay is operated,

it locks up through its own contact 10 and contact 8 of relay RS1. Relay TP1 may be released by the operation of relay RS1. Similarly, relay TP1 will lock operated through its own contact 10 and contact 8 of relay RS0. This relay is released in a similar manner by operating relay RS0.

7.04 Either of the two circuit halves may in a similar manner be put into a quarantined mode by operating relays Q0 or Q1. Relays CP0 and CP1 operate in shunt with the quarantine relays. The operate path of relay Q0 is through contact 5 of relay OR11, contact 18 of relay P39, and the released contact 1 of relay Q1. A similar path to operate relay Q1 is found through contact 5 of relay OR3, contact 18 of relay P31, and the released contact 1 of relay Q0. The relays Q0 and CP0 will lock operated through contact 2 of relay Q0 and released contact 11 of relay RS1. Similarly, relays Q1 and CP1 lock up over a similar path. The release of either of these pairs of relays is possible by the operation of either relay RS0 or RS1.

7.05 The three manual pushbutton keys designated OFF-0, OFF-1, and NOR are shown in a released state. These keys are mechanically interlocked in such a manner that only one of the three may be depressed at any one time. Furthermore, it is the normal state of these control keys that the NOR key is depressed. This means that the NOR key is normally operated. The contacts shown as make contacts are normally closed.

7.06 The purpose of these keys is to manually remove power from either of the two circuit halves. The operation of the OFF-0 key removes power from the 0 circuitry. Similarly, the operation of the OFF-1 key removes power from the 1 circuitry. From either of these non-normal states of the keys, power is restored by operating again the NOR key. The operation of the OFF-0 key mechanically forces the NOR key to release. The operation of any of the keys overrides any other non-normal state that the circuit might be in at the time. As an example, if the 1 circuit half is quarantined (Q1 and CP1 relays operated) at the time the OFF-0 key is operated, the sequence of events would be as follows. The operation of the OFF-0 key applies a ground to the PW1 relay through the contact 1B and 2B. This insures that power cannot be removed from the 1 circuit half. Furthermore, the release of the NOR key removes ground through the key contacts from the PW0 relay. The operation and closure of the OFF-0 contact 2T and 1T forces the operation of the relay RS0. The operation of this relay starts the release of any relays, belonging to the 1 circuit half, that may be operated at the time. The closure of contacts 4B and 3B of the OFF-0 key starts the operation of relays Q0 and

CP0. The operation of relay Q0 removes the ground that was applied to the PW0 relay through contact 2 of the Q0 relay, and the operation of the RS0 relay removes the last connection to ground from the PW0 relay. This starts the release of the PW0 relay, through which power has been applied to the 0 circuit half. This sequence of events insures that the 1 circuit half is taken out of a quarantined mode of operation.

7.07 The power-restore sequence is initiated by operating the NOR key. The operation of this key removes the paths for Q0, CP0, and RS0 relays. The closure of the NOR key contacts 4B and 3B applies ground to the PW0 relay. The opening of contacts 2T and 1T starts the release of relay RS0, and the release of contacts 4B and 3B allows the release of the Q0 and CP0 relays.

7.08 A similar sequence of events occurs when the OFF-1 key is depressed. Again the NOR key releases due to the mechanical interlock that exists. It is necessary to restore the NOR key to the operated position in order to restore the circuit to the normal mode of operation. It is not possible to release the OFF-1 key by an attempt to operate the OFF-0 key. The sequence of events always includes the operation of the NOR key.

7.09 The OS-0 and OS-1 lamps (out-of-service circuit 0 and circuit 1) indicate the state of the two circuit halves. With the 0 circuit quarantined, the CP0 relay is operated and the out-of-service lamp 0 should be on. Similarly, the out-of-service lamp 1 is on whenever circuit 1 is quarantined. The OFF-NOR lamp is on when the NOR key is released.

7.10 The two pairs of wires which connect to the controller logic circuit 0 and to the controller logic circuit 1, designated EN and ENM, inhibit the return of an enable verification signal from that circuit half which is in a quarantined mode of operation. The two leads, RO0 and RS1, which connect to the two ferreed pulses and path check circuits, are the lock-up paths for the circuitry in the pulser circuit which locks up whenever a short-to-ground has been detected on any of the pulsing paths in the network fabric. The lock-up path is through contact 12 of relay RS0 or RS1, respectively.

7.11 The operate path for relay RS0 is contact 5 of OR3 and contact 18 of relay P33. This indicates that relay RS0 is controlled by the 0 circuit half of the trunk switching circuit. Relay RS1 operates through contact 5 of relay OR11 and contact 18 of relay P311. Neither of these relays will lock up. They momentarily operate and remain in this

operated state only long enough to initiate the release of any lock-up paths that might exist.

8. FERREED PULSER AND PATH CHECK (FS 8)

8.01 The ferreed pulser circuit provides the high-amplitude pulse of greater than 9.0 A. It also provides a means for detecting shorts to ground in the pulse path and a means for detecting a successful pulse operation, through use of the biased core detector (T2). It detects the presence of a pulse path through trunk switching, delays several milliseconds, and fires a pulse through the path.

8.02 The pulser circuit interfaces with the trunk switching circuit via connector J1. It receives its power (+24, -48, and ground) from the trunk switching circuit.

8.03 Refer to CD-1A232-01 for a description of operation of the pulser circuit.

9. PULSE PATH, STAGE 0, GRID 0 (FS 9)

9.01 Stage 0 of each octal grid contains eight switches, each consisting of an 8-by-8 ferreed switch. The selection of a pulse path within each octal grid is, in principle, the same. A pulse path is selected by means of operating combinations of wire-spring relays. One and only one relay should operate in each of the wire-spring relay groups.

9.02 Each switch has a 3-digit functional designation. The first digit indicates the grid number to which the switch belongs. The second digit indicates stage number, and the last and least significant digit indicates the switch number within the grid.

9.03 The operation of relay P50 selects grid 0. The operation of relay P51 selects grid 1. In a similar manner, the wire-spring relays in group 5 selects one of the four grids. In grid 0, relay group 1 selects input pulse terminals. The operation of relays P10 through P17 selects one of the input pulse terminals numbered from 00 to terminal 07. The operation of one of the wire-spring relays in wire-spring relay group 1 selects one out of the eight input pulse terminals. The selection of an input switch (stage 0 switch) depends upon which A link pulse terminal has been selected. While input terminals may be selected in grids 0 and 1 by means of relays P10 through P17, input terminals belonging to grids 2 and 3 are selected by relays P18 through P115. The lower-numbered relays are associated with the two lower-numbered grids. Similarly, the high-numbered relays are associated with the two higher-numbered grids.

9.04 Each A link pulse lead has a 2-digit lead designation preceded by the letter C. The numbers signify the stage 0 connection of each of these link pulse leads. The first digit indicates stage 0 switch and the second digit indicates stage 0 level. The A link pulse lead designated C16 connects switch 1 level 6 in stage 0. This same pulse link lead terminates in stage 1 on switch 6 level 1. This association between lead designations and A link pulse wiring is true for all A link pulse wiring within a grid. The grid 0 pulse path connects to the pulse steering circuit over the lead designated A0, and similarly, grid 1 connects to the pulse steering over the 1A wire.

9.05 As an example of a pulse path through a ferreed switch, it can be assumed that the P50 and the P13 relays are operated. Furthermore, if it is assumed that link C34 has been selected, a pulse path is established through the switch in the following manner. This partial pulse path consists of the A0 lead, contact 4 on the P50 relay, contact 4 on the P13 relay and switch 003, terminal 03. Continuity is established between terminal 03 and terminal 10, which in turn is strapped to terminal 9, and further, through the switch which is in the intersection between vertical 3 and level 4 connected to terminal 16, will operate. All ferreed crosspoints which belong to either the same vertical or same horizontal which were just pulsed will release in case they were previously operated.

9.06 If, instead, the link lead designated C04 has been selected, a pulse path is established through contact 1 of relay P50, contact 1 of relay P13, and level 4 terminal 16 of switch 000. A ferreed crosspoint belonging to switch 000 will close which, within this switch, has the same relative position as that discussed in the previous example. In this manner, an input switch is selected by means of the selection of the A link pulse leads.

10. PULSE PATH, STAGE 1 (FS 10)

10.01 The stage 1 pulse pair constitutes another portion of the over-all pulsing pair. A path through this stage is established when continuity exists between any of the A link leads and the lead E0. In order to establish a unique path between one A link pulse lead and E0 lead, one relay belonging to group 2, one relay is group 3, and one relay in group 4 must be operated.

10.02 In grid 0, relays P40 through P47 select the output switch. The relays in group 2 which include relays P20 through P27, select output terminals (B links). Group 3 relays, which include relays P30

through P37, select 1 out of 8 A link pulse leads (A link input terminal). In grid 1, the selecting functions in groups 2 and 4 are interchanged. In this grid, an output switch is selected by operating one relay within group 2. An output level is selected by operating one relay in group 4.

10.03 As an example, in order to select A link pulse lead designated C23, it is necessary to operate relays P43 and P32. In addition, one relay in group 2 must be operated. This relay selects the desired output terminal. It should be noted that the last digit of the number of the switch-selecting relay corresponds to the number of the switch. In a similar manner, the number of the relays within a group corresponds to levels selected or links selected. In grid 0, relay P43 selects output switch 3, relay P25 selects output level 5 and relay P32 selects input level 2.

10.04 In all of stage 1, the third wire-spring relay group selects the input switch to be used. Since all A link pulse leads associated with a particular output switch (stage 1 switch) are all connected to different input switches (stage 0 switch), the operation of one relay within the third relay group automatically selects the stage 0 switch to be used.

10.05 A path is selected through stage 1 of grids 2 and 3 in a similar manner as discussed for grids 0 and 1. A different set of wire-spring relays is used in these two grids. These higher-numbered relays are primarily associated with the 1 circuit half of the trunk switching circuit. The selecting functions of wire-spring relay groups 2 and 4 are interchanged in a similar manner between grids 2 and 3 as in grids 0 and 1. In grid 2, relay group 4 selects stage 1 output switch while relay group 2 selects output level. In grid 3, wire-spring relay group 2 selects the output switch while relay group 4 selects the output level. In both of these grids, relay group 3 selects input level or A link pulse lead.

10.06 Stage 1 of each grid contains eight switches, each switch being an 8-by-8 ferreed switch. The pulse path within a switch is similar to the example given for a pulse path in stage 0. The control of any ferreed crosspoint is independent of the direction of pulse current. Grids 2 and 3 connect to the pulse steering relays by means of leads E2 and E3, respectively. The direction of pulse current is determined by the pulse steering circuit.

10.07 Each switch in stage 1 has a functional designation which contains three digits preceded by the letters SW. Similar to stage 0, the first digit indicates the grid number, second digit indicates stage

number, and the last and least significant digit indicates the switch number within the grid. The differential method of controlling a ferreed crosspoint is indicated on the symbolic representation of the 8-by-8 ferreed switch. The terminals 09 and 10 are interconnected on all switches. Therefore, the pulse path through a switch always contains the windings of eight ferreeds belonging to one vertical and eight ferreeds belonging to a horizontal. The ferreed crosspoint which is associated with both this vertical and horizontal will be operated. All ferreeds that either belong to the vertical or the horizontal release if they were previously operated. Therefore, an instruction to disconnect is never required in the trunk switching circuit. The release of any crosspoint within any switch relies upon the operation of a different crosspoint within the switch. Consequently, in this general configuration there must always be at least one crosspoint closed in each switch.

11. TALKING PATH, STAGES 0 AND 1 (FS 11)

11.01 The talking path stage 0 shows symbolically the tip-ring wiring of the ferreed switch. This symbolic representation indicates between which terminals a connection may possibly be established.

11.02 The interstage wiring is the same for all grids. The tip-ring interstage connection is often referred to as the A link leads. Each tip-ring A link has a functional designation which contains two digits. The two digits are preceded by either a T or an R in order to indicate the tip and the ring conductor of a pair. Similar to the A link pulse lead, the first digit indicates the stage 0 switch to which the wire is connected. The second and less significant digit indicates the switch level in stage 0 to which the wire is connected. The stage 1 connection of any tip-ring pair may be found by interchanging the meanings of the two digits. As an example, the tip-ring pair designated R54, T54, indicates that this pair is connected to switch 5 level 4 in stage 0, and connects to switch 4 level 5 in stage 1.

11.03 The eight pairs of tip-ring conductors that connect to switch terminals 00 through terminal 15 of the stage 0 switches are often referred to as the trunk terminals. Each tip-ring conductor has a functional designation similar to the A link designations.

11.04 The eight tip-ring conductors which connect to the switch terminals 00 through 15 of stage 1 are referred to as B links.

11.05 A tip-ring connection is established between a trunk terminal and a B-link terminal by operating one crosspoint in each stage of switching. This connection, therefore, contains two ferreed contacts in each conductor.

11.06 Any trunk terminal may be connected to any B-link terminal within the same grid. There exists only one path between a particular trunk terminal and a particular B-link terminal.

12. POWER CONTROL (FS 12)

12.01 The power control circuit shows the power distribution to the switching network of the trunk switching circuit. All power is applied to the circuitry through contacts on power relays PW0 and PW1, with the exception of the -48A2 and B2 supplies. The -48A2 and B2 power leads control the power relays PW0 and PW1. Contact 7 on the PW0 and PW1 relays goes to the miscellaneous circuit to light the power-off lamp if either relay is not operated. The -48 ALM and +24 ALM leads to the miscellaneous circuit are used as fuse alarms to indicate that a power fuse has opened on the frame. Relays P0 and P1 are operated through the make contact 6 of the PW0 and PW1 relays, respectively. The contacts of the P0 and P1 relays are used

in the controller logic (FS 4) and pulse steering (FS 5) sections.

13. DESCRIPTION OF OPTIONS

13.01 Options Y and Z: Connector J1, on the trunk switching circuit side of the ferreed pulser, was changed, on a class B basis, from one with a metal cover (KS-14672,L2) to one with a plastic cover (KS-14672,L9). The plastic-cover connector is made to be compatible with a retaining clip mountable on the ferreed pulser circuit. This is to prevent accidental removal of the plug from the pulser.

13.02 Options W and X: AJ703 relays have been replaced on a class B basis with AJ704 relays, options X and W, respectively. The AJ704 relays have winding terminals 2U and 2L moved away from the rubber mounting pads. This is to prevent leakage current from flowing through the rubber pads, a problem which manifests itself only during diagnosis of a controller, as an incorrect group-check response.

13.03 Options S and T: Resistors R5.0 and R5.1 were changed on a class B basis from KS-16266,L3C to KS-20289,L3C. This change affects new manufacture only.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 None.

2. FUNCTIONAL DESIGNATIONS

2.01

<u>Designation</u>	<u>Meaning</u>
EP	Bypass
CT	Cut through
EN	Enable
ETO	Early time-out
F	Failure
GC	Group check
H	Horizontal
HC	Horizontal common
L	Level
NOR	Normal
OFF-NOR	Off-normal
OR	Order
OS	Out-of-service
P	Path selector
PS	Pulse steering
PW	Power
Q	Quarantine
RS	Reset
S	Success
SW	Switch
T	Test
TP	Test point
V	Vertical
VC	Vertical common
VCT	Voltage cut-through

3. FUNCTIONS

3.01 Provides the means for responding to high-speed signals from the peripheral bus circuit when these signals coincide with a proper enable signal.

3.02 Provides the means for memorizing these signals and translating the result into the selection of unique wire-spring relay operate paths.

3.03 Provides the circuits for checking the validity of the address received and the proper functioning of memorizing or translating circuitry.

3.04 Provides the means for timing and assuring proper sequential operations, and for returning verification signals to the central control.

3.05 Provides the means, via the master scanner, to inform the central control as to the status of the circuit at any time.

3.06 Provides the circuitry for the purpose of detecting the presence of a ferreed pulse path.

3.07 Provides the means to generate and steer the high-current (10-amp) pulse into a selected ferreed pulse path and for monitoring the amplitude of the high-current pulse.

3.08 Provides the means for establishing tip-ring metallic connections between a trunk terminal and a B-link terminal within a grid.

3.09 Provides the means, via the master scanner circuit, to convey to the central control the state of a number of test points within the circuit.

3.10 Provides the means for allowing the central control to change the mode of operation of the circuit.

3.11 Provides the means to manually change the mode of operation of the circuit.

4. CONNECTION CIRCUITS

4.01 When this circuit is listed on a keysheet, the connecting information thereon should be provided.

- (a) Junctor Switching Circuit - SD-1A108-01.
- (b) Master Scanner Circuit - SD-1A118-01.
- (c) Communication Bus Circuit for Peripheral Units - SD-1A119-01.
- (d) Power Distribution Frame Circuit - SD-1A126-01.
- (e) Miscellaneous Circuit for All Frames - SD-1A129-01.
- (f) High Current Pulser and Path Check Circuit - SD-1A232-01.

5. MANUFACTURING TESTING REQUIREMENTS

5.01 The manufacturing testing requirements are detailed in X-77177.

6. TAKING EQUIPMENT OUT OF SERVICE

6.01 Either major circuit group may be taken out of service. A circuit is out of service when it is quarantined or when power has been removed from that circuit. A specific instruction must be transmitted to that circuit half which will remain active in order to quarantine the second circuit group. Only one out of two groups of circuits (circuits 0 or 1) may be taken out of service at any time. The remaining active circuit half will assume control of all four grids.

6.02 A circuit may be taken out of service or put back into service only by orders from the central control. Power may be removed from either circuit group by manually operating the OFF-0 or OFF-1 key. This will take that circuit group out of service. Preceding such action, the central control should normally be informed about the intended power removal. Power is restored by operating the manual key. When power is restored to one circuit half, this circuit will remain in a quarantined mode. It is normal that only the central control can restore into service any circuit half. Since all non-normal modes of operation of a circuit group are controlled by means of wire-spring relays, it is therefore possible manually to put any circuit half into a non-normal mode by manually forcing these relays into the proper state. With the exception of a case of emergency, the central control should be requested to change the mode of operation of any circuit group.

6.03 The following steps are recommended whenever a circuit must be taken out of service.

- (a) Request that the central control quarantine a particular circuit half.
- (b) Verify that this circuit has been taken out of service (quarantined) by observing that the OS-0 or OS-1 lamp is lit. The lamp that is lit should correspond with that circuit half which was requested to be quarantined.
- (c) If it is desirable to remove power from that circuit half which has just been quarantined, the corresponding OFF-0 or OFF-1 key should be depressed.
- (d) Power may be restored to either of the two circuit halves by operating the NOR key.
- (e) Observe that the out-of-service lamp (OS-0 or OS-1) remains on.
- (f) Inform the central control that earlier requests to take a particular circuit half out of service have been canceled.

SECTION IV - REASONS FOR REISSUE

D. Description of Changes

D.1 The circuit rating was changed from AT&TCo Standard to A&M only. The ferreed circuit is no longer required for new installations because of the new remreed trunk switching circuit (SD-1A327-01).

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