

12

COMMON SYSTEM

3A CENTRAL CONTROL
CIRCUIT

CHANGES

D. Description of Changes

- D.1 Changed circuit to allow the use of the cost-reduced processor frame power unit (8-ampere version).
- D.2 Added two options:
 - (a) Option X, for the noncost-reduced (4-ampere) power unit (rated Mfr Disc.).
 - (b) Option W, for the cost-reduced (8-ampere) power unit (rated AT&T Co Standard).

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 5515-DJM-LEG

CIRCUIT DESCRIPTION

CD-1C900-01
ISSUE 1
APPENDIX 5D
DWG ISSUE 6D
DISTN CODE 1N98

COMMON SYSTEMS

3A CENTRAL CONTROL
CIRCUIT

CHANGES

D. Description of Changes

D.1 Changed circuit to allow removal of four power converters in the processor frame power unit, as a cost reduction when using microprogram store circuit packs with 1024 words per pack.

D.2 Added two options:

- (a) Option Z, for microprogram stores with 512 words per pack (rated A & M Only);
- (b) Option Y, for packs with 1024 words per pack (rated Standard).

D.3 Removed ground wiring no longer required with the 1024-words-per-pack microstore.

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DEPT 5435-DJM-LEG

CIRCUIT DESCRIPTION

CD-1C900-01
ISSUE 1
APPENDIX 4A
DWG ISSUE 5A
DISTN CODE 1N98

COMMON SYSTEMS

3A CENTRAL CONTROL
CIRCUIT

CHANGES

D. Description of Changes

- D.1 Changed processor bus controller (PBC) logic so that store complete (SCM) and store error C (SERC) are checked prior to sending store GO. This prevents GO from being issued before the store removes SCM or SERC.
- D.2 Eliminated a race condition between clock phase P2 and SCM on the ENSCM flip-flop.
- D.3 Corrected a design problem to prevent the DR flip-flop from being set by an SCM intended for another user of the store bus when the 3A CC is in the update mode.
- D.4 Changed PBC logic so that SERC is checked for the inactive state prior to clearing the SEZ flip-flop.
- D.5 Prevented the store bus from being released too soon when doing double store read and complement correction operations. With this change, only the GO flip-flop is cleared with the BR to MMS crosspoint and the double store read signal. The SEZ flip-flop remains set until the store bus becomes idle.
- D.6 Prevented the issue of a false SERC to lower-priority users of the store bus. The SEZ flip-flop, rather than the GO flip-flop, will be used to control the SERC repeater.
- D.7 Removed the store busy (SBY) signal. This signal is no longer used by the 3A CC or other users of the store bus.
- D.8 Added nets EN0.INV1 and EN1.INV1 to eliminate a race condition involving the ENGDRL signal.

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DEPT 5435-DJM-LEG

CIRCUIT DESCRIPTION

CD-1C900-01
ISSUE 1
APPENDIX 3A
DWG ISSUE 4A
DISTN CODE 7N98

COMMON SYSTEMS

3A CENTRAL CONTROL
CIRCUIT

CHANGES

D. Description of Changes

- D.1 Provided for the automatic collection of data during a double store read (DSR). During a DSR the 3ACC saves the address in the AK register, the bad data in the DK register, and the good data in the DI register. This automatic trap of data and address is inhibited when the AME and/or DME bits of the system status register are set.
- D.2 Added wiring to allow the use of microprogram store circuit packs containing either 512 or 1024 words.

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DEPT 5435-DJM-LEG

COMMON SYSTEMS

3A CENTRAL CONTROL
CIRCUIT

CHANGES

D. Description of Changes

- D.1 Provided single-bit error correction (complement correction) of main store words when the 3A CC system is operating in the non-update mode.
- D.2 Provided fourth store port cabling access to the 3A CC.
- D.3 Provided load resistor pullups on the microstore address register for all possible microstore configurations.
- D.4 Provided additional maintenance access so that the complement correction hardware can be more fully exercised by diagnostics. (MS bits 7 and 13 are affected.)
- D.5 Provided additional pullup loads on lightly loaded backplane nets that have potential speed problems.
- D.6 Added new clock design to improve timing margins of the two clock phases sent to the I/O channels.

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DEPT 5344-DJM-LAW

COMMON SYSTEMS
3A CENTRAL CONTROL
CIRCUIT

CHANGES

D. Description of Changes

- D.1 Improved system reliability for duplex operation is provided by performing an automatic read of the off-line store when a parity error is detected during a read of the corresponding on-line word (double-store read).
- D.2 Test set access is provided so that functions such as program transfer trace and call store imaging can be performed in a field environment.
- D.3 The ability to "optionally" implement an 8-bit OP code field for possible future application is provided.
- D.4 A maintenance state from the 3ACC to its main store is provided to override the disabling of the I/O serial channel port from the other 3ACC.
- D.5 The ability to drive the MANUAL light on the CC panel directly from the MANUAL key instead of indirectly over the maintenance channel is provided.
- D.6 Maintenance channel access to the POWER key and the TEST MODE REVERSAL key via the MB register is provided.
- D.7 A gating path from the BR(8-15) into the PT and a miscellaneous decoder crosspoint to control the gating is provided.
- D.8 The "stop and switch" miscellaneous decoder crosspoint is changed to be conditional on the LOCK ON-LINE flip-flop.

D.9 A wiring change is made so that a future redesign of the clock oscillator board FB486 can result in improved timing margins for I/O serial channel operation.

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DEPT 5344-DJM-LAW

COMMON SYSTEMS
3A CENTRAL CONTROL
CIRCUIT

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SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The purpose of the 3A central control (3ACC) is to obtain a sequence of instructions or commands from the main store (MAS) and translate these commands into a sequence of actions within the 3ACC and/or the circuitry attached to the 3ACC.

2. GENERAL DESCRIPTION OF OPERATION

2.01 The 3ACC comprises a large number of registers and their associated control logic circuitry. The 3ACC obtains the sequence of commands from the MAS and translates them into action. This action, usually results in the movement of data between the registers in the 3ACC or between the register in the 3ACC and the MAS. The translation is performed by a sequence of microinstruction steps. Each microinstruction step consists of reading a word out of the microstore. This word indicates the microinstruction to be performed on this microcycle as well as the address of the next microinstruction to be performed. In this way, an instruction obtained from the MAS is used to point to the starting address in the microstore of a sequence of microinstructions that will cause the microcontrol to perform a required action.

2.02 At the completion of the sequence of microinstructions, the microcontrol interrogates the MAS to determine whether the next instruction has been fetched from the MAS. If not, the microcontrol goes into a loop in which it constantly interrogates the completion of the MAS cycle. When the MAS does complete, the next instruction is loaded into the 3ACC and a new microinstruction sequence is initiated.

2.03 The 3ACC also has the ability to write into the MAS. Writing is normally performed in a temporary storage portion of the MAS. The other portions of the MAS are write-protected and a sequence of

operations is needed to allow the 3ACC to write into protected areas of the MAS.

2.04 The 3ACC is a self-checking machine. That is, it contains check circuits that indicate the correct operation of the instruction executions.

2.05 The 3ACC contains I/O serial channels that allow it to communicate with peripheral devices, such as TTYS, a tape cartridge unit, and peripheral frames in an ESS office.

2.06 A maintenance channel (MCH) is used to communicate between two identical 3ACCs that are used in an ESS application. The MCH is a serial link between two 3ACCs which provides the ability for one 3ACC to diagnose another.

SECTION II - DETAILED DESCRIPTION

1. FS 1 - MICROPROGRAM CONTROL

1.01 The microprogram control performs a sequence of microinstructions that translates the main memory instruction that is fetched from the MAS. Microprogram control contains a read only microstore, an address register (MAR), and an output register (MIR). Attached to the MIR are instruction decoders that decode each individual microinstruction. The instruction decoders are broken down into two types, the FROM decoder and the TO decoder. The FROM decoder defines a source register, and the TO decoder defines the destination register. In this way, the microprogram control can issue a microinstruction to gate data from one register to another register.

1.02 Translation of each instruction from the MAS, therefore, consists of a series of gating instructions from one register to another register or from the output of the combinational logic attached to one or more registers to some other register. In special cases, the outputs of the TO and FROM field decoders are combined to form a miscellaneous decoder that is used to set and clear individual flip-flops in the 3ACC.

1.03 In addition to the TO and FROM fields contained in the MIR, an address field is included. This address field primarily provides the address for the location of the next microinstruction to be executed. In some cases the address field contains data that can be gated to other registers in the 3ACC. In these cases the next address is obtained by adding one to the previous address.

1.04 The microcontrol contains a microcontrol status register (MCS). This register saves such states as adder overflows, I/O channel status, etc. The microcontrol has the capability of

conditionally transferring or testing each of the bits in the MCS.

2. FS 2 - DATA MANIPULATION LOGIC

2.01 The data manipulation logic (DML) is used to perform the arithmetic and logic operation in the 3ACC. It consists of a series of registers to which logic is attached to perform addition, subtraction, and Boolean operations. In addition, it contains logic to perform rotations from one register within the DML to another register within the DML. The DML is also used to compute parity on the DML output so that it may be gated to other parts of the 3ACC without causing parity errors.

3. FS 3 - GENERAL REGISTERS

3.01 There are 16 general registers in the 3ACC. These registers are 16-bits wide and are used primarily for high-speed scratch pad storage for the main memory programmer. They are numbered R0 through R15. General registers 9, 10, and 11 are also used to interface with the I/O serial channel and, therefore, have special hardware access to them.

4. FS 4 - MAIN MEMORY INTERFACE

4.01 The main memory interface consists of those registers and associated control logic in the 3ACC that are used to communicate between the MAS and the 3ACC. The SAR register is used to load the address of the word of memory that is to be accessed. The store instruction register (SIR) is used to buffer instructions read from the MAS. The store data register (SDR) is used to buffer data on either a read or a write command. The MMS register is used to control the mode of operation for a given store cycle. For example, it defines which store (my store or the other store) is to be active for a given MAS memory cycle. In addition, there is some sequential logic that is used to buffer the store requests from 3ACC and determine whether the store bus is busy or not, and if not, issue store requests to the MAS.

5. FS 5 - SPECIAL REGISTERS

5.01 The special registers in the 3ACC are used for dedicated purposes. The following is a list of those registers and their specified functions.

- (a) CR - C register, a general purpose register used for the microcontrol. It is generally used to buffer the results of the DML operations.
- (b) ER - Error register, used to buffer the output of check circuits in the 3ACC. Each bit in the ER register corresponds to a particular check circuit and therefore indicates what portion of the 3ACC has failed.

- (c) HG - The hold-get register, used as a pointer into main memory. The contents of the hold-get area in main memory contain the state of the 3ACC at the time of a subroutine call.
- (d) IK - The interrupt mask register, used to mask individual interrupt bits in the IS. That is, if the corresponding bit in the IK is set and it does not allow that interrupt to be served.
- (e) IS - The interrupt set register, used to buffer interrupts coming into the 3ACC.
- (f) MS - The maintenance state register, used to buffer maintenance states of the 3ACC. This allows the diagnostic program to set up conditions that enable it to test the correct operation of the 3ACC.
- (g) SS - System status register used to buffer the various states of the 3ACC.

6. FS 6 - DATA TRANSFER CHECK CIRCUITS

6.01 The data transfer check circuits insure the correct operation of the 3ACC. The two main checkers are the TO field checker and the FROM field checker. These checkers will fire when an error in the TO field or the FROM field has occurred. The BA check is a check circuit that will fire when a transfer to an improper memory location has occurred. The gating bus parity checker will fire when the contents of a register are gated onto the gating bus with incorrect parity (unless the checker is inhibited). The I/O main channel checker insures that the proper I/O main channel has been selected.

7. FS 7 - CONSOLE FUNCTIONS

7.01 The console functions are those functions that are associated with the CC panel. The primary function here is the operation of the display buffer and the control of the switch registers into the display buffer. Under microprogram control, the contents of the switches on the front panel can be selectively gated into the display buffer. Once in the display buffer, the switches are interpreted and the appropriate action taken. In addition, address and data match registers are provided to allow the panel to match on memory operations that use the address and data as indicated in the registers.

7.02 The processor initialization hardware is also contained in this FS 7. It consists of series of inputs from which hardware initialization signals may be received. These signals are buffered and used to initialize the clock and some key

flip-flops in the 3ACC, and to jam a starting address into the MAR. Control logic will then allow the 3ACC to start at this known address in the microstore and sequence through a series of steps that will result in initializing the 3ACC. Eventually the microprogram control will turn the initialization over to the program contained in main memory.

7.03 The system status panel (SSP) interfaces through this FS 7 and allows the system status panel to control the lock-off line and the lock-on line flip-flops. In addition, an initialization signal comes from the SSP.

7.04 The disable flip-flop and the associated sequential logic contained in this FS gives the MCH the ability to disable one 3ACC from another 3ACC.

8. FS 8 - PROGRAM TIMER AND TIMING COUNTER

8.01 This circuit provides the basic timing for the 3ACC. It consists of a crystal oscillator driving a ring counter, which generates a 4-phase clock. Each clock phase is 1/4 of the basic 150-ns microcycle interval. The four clock phases are distributed throughout the 3ACC and are used whenever clocking is required. The two primary uses of the clock are: (1) to gate in and out of the registers associated with the microstore, and (2) for the strobing of check circuits.

8.02 The output of the clock also drives a binary counter that provides a number of time intervals for use by other timed functions in the CC. One of these counter outputs, which is a 19.2 microsecond pulse, is used to increment a prescaler on the program and timing counter circuit pack. The prescaler in turn increments the timing counter. The timing counter outputs provide four basic time intervals: (1) a 1.25 millisecond pulse, (2) a 5.0 millisecond pulse, (3) a 10.0 millisecond pulse, and (4) a 25 millisecond pulse. These four time intervals are available on the backplane of the 3ACC and may be optionally wired depending upon the application.

8.03 The 25 millisecond pulse is used to increment the program timer, which is a binary counter that counts 25 millisecond intervals. The purpose of the program timer is to provide a basic backup mechanism for the failure of hardware or software. If the program timer counts up to 1.6 seconds, it will initiate a sequence that will attempt to initialize the system. If improper action takes place at 1.6 seconds, a second timeout will occur at 3.6 seconds and will again attempt to initialize the system. It is a function of the software to routinely reset the program timer to prevent initializations.

9. FS 9 - MAINTENANCE CHANNEL

9.01 The maintenance channel is a serial link that allows one 3ACC to communicate with another. Its three primary purposes are: (1) to indicate to the standby 3ACC that an error has occurred in the on-line machine and hence the off-line 3ACC should start up, (2) to allow the on-line machine to send diagnostic orders across to the off-line machine in order to determine the location of a fault after an error has occurred, and (3) to provide the communication path for the on-line machine to monitor the state of the off-line machine in order to determine the system configuration.

10. FS 10 - I/O CHANNEL

10.01 The I/O channels are used to communicate to the peripheral world from the 3ACC. They are a serial link in which a dedicated pair of wires goes from each subchannel in the 3ACC to each device that is to be communicated with. The 3ACC is wired to grow to three main channels, each with 20 subchannels. In addition, the 3ACC has the ability to address a total of 20 main channels. The serial channel consists of a buffer register (IOD) that shifts out the information to the periphery and a control register (IOS) that determines the state of a given I/O channel.

11. FS 11 - EXTENDED MAIN MEMORY BUS

11.01 The extended main memory bus is a wider interface to the MAS. For those applications that need wider than 16 data bits (plus 2 parity bits) in the MAS, this feature allows the main memory width to be extended to 24 bits (plus 3 parity bits). Therefore, the store instruction register and store data register are made wider to accommodate the wider store.

12. FS 12 - MICROPROGRAM STORE

12.01 The microprogram store consists of a maximum of 4K of 32-bits wide of read only memory. The memory is growable in 512- by 32-bit word blocks. Each block is selected with a plane select lead that determines which one of the 512 blocks is to be accessed. It is presented with an address on address leads, and 65 ns later the output of the address location appears at the output of the microprogram store.

13. FS 13 - PROTECTION CIRCUITS

13.01 The protection circuits are used to buffer the signals that cross-connect between the two half systems in the 3ACC control complex. Those leads that cross connect are mainly the store bus signals that go from one 3ACC and into the other 3ACC. The protection circuits prevent an over-voltage or over-current condition from affecting both 3ACCs.

14. FS 14 - 3-VOLT REFERENCE AND FILTER CIRCUIT

14.01 The 3-volt reference and filter circuit provides the interface between the 3-volt power supply and the 1A logic used in the 3ACC. This circuitry monitors a reference source and the incoming voltage source from the power supplies and feeds back a signal to the 3-volt supplies if more or less than a fixed amount is indicated. The power supply will respond with the appropriate voltage change. The filter circuit allows time for the power supply to respond to the signal from the reference source. If the reference indicates an out-of-limits range, a power alarm will result.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 None.

2. FUNCTIONAL DESIGNATIONS

<u>Designation</u>	<u>Meaning</u>
AI	Address match input register
AK	Address match mask register
AR	A Register
BR	B Register
CR	C Register
DB	Display buffer
DI	Data match input register
DK	Data match mask register
DML	Data manipulation logic
ER	Error register
FN	Function register
HG	Hold-get register
IB	Instruction buffer
IK	Interrupt mask register
IOD	Input/output data register
IOS	Input/output status register
IS	Interrupt set register
MAR	Microstore address register
MB	Miscellaneous bits register
MCS	Microcontrol status register
MCHT/R	Maintenance channel transmit receive register

<u>Designation</u>	<u>Meaning</u>
MIR	Microcontrol instruction register
MMS	Main memory status register
MS	Maintenance state register
PA	Program store address register
PT	Program timer
RAR	Return address register
R0-R15	General registers 0-15
SAR	Store address register
SDR	Store data register
SIR	Store instruction register
SS	System status register
TC	Timing counter
TI	Timing register

3. FUNCTIONS

3.01 This circuit executes commands obtained from main memory, provides clock and control for some of the connecting circuits, automatically switches itself off-line in case of certain faults, and provides error indication of all hardware faults.

4. CONNECTING CIRCUITS

4.01 When this circuit is listed on a keysheet, the connecting information

thereon is to be followed. The following are typical connecting circuits.

- (a) JACC Control Panel Circuit - SD-1C901-01.
- (b) Main Store Controller Circuit - SD-1C902-01.
- (c) Main Store Memory Circuit - SD-1C903-01.
- (d) TTY Controller Circuit - SD-1C905-01.
- (e) System Status Panel Circuit - SD-1C906-01.
- (f) System Status Panel Control Circuit - SD-1C907-01.
- (g) System Status Panel Power Circuit - SD-1C908-01.
- (h) Maintenance Frame Power Circuit - SD-1C909-01.
- (i) Processor Frame Circuit - SD-1C910-01.
- (j) Processor Frame Power Circuit - SD-1C911-01.
- (k) Maintenance Frame Circuit - SD-1C912-01.
- (l) No. 2B ESS Input/Output Circuit - SD-2H099-01.

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