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COMMON SYSTEMS

3A CC CONTROL PANEL CIRCUIT

CHANGES

D. Description of Changes

D.1 Updated component list to show the proper LED codes and to specify KS codes, rather than commercial codes, for switches.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 5435-DJM-LEG

CIRCUIT DESCRIPTION

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CHANGES

D. Description of Changes

D.1 Changed designation of the STANDBY lamp to NOT ACTIVE.

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DEPT 5435-DJM-LEG

COMMON SYSTEMS

3A CC CONTROL PANEL CIRCUIT

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SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The 3A CC control panel provides manual access to, and display of, internal registers and main memory associated with the 3A central control (3A CC). The control panel makes it possible to step through a program and to compare a memory address and/or data with a desired address or data pattern. Power for the control unit and certain status conditions are controlled and monitored at the panel.

SECTION II - DETAILED DESCRIPTION

1. PHYSICAL ARRANGEMENT

1.01 The 3A CC control panel allows manual intervention to, and monitoring of, the operation of the 3A CC. The apparatus which comprise the control panel circuit are mounted on a printed wiring (PW) board which provides interconnection for the apparatus. This PW board is designated CP1 in the circuit drawing and is shown as FS 1. Connection to the 3A CC circuits is via nine cables which are attached to the panel PW board and plug onto the 3A CC backplane via Berg connectors. A mask, in which the panel controls and indicators are identified, fits over the PW board. Information Note 303 shows a sketch of the panel with the mask in place.

2. CIRCUIT ARRANGEMENT

2.01 The control panel circuit is shown in FS 1 with its apparatus grouped into functional elements, A through K. Cables 1 through 8 are also shown terminating at terminal strips (TSs) 1 through 8 at one end and connectors 1 through 9 at the other end. TSs 1 through 8 are composed of

printed wire land areas. Cables 1 through 6 are flat tape cables. Cable 7 is comprised of coaxial cables. Cables 8 and 9 consist of individual wires of various gauges. Tables A and B identify the connection of each lead from a terminal in a particular TS on the panel to a terminal at a particular 3A CC location. Note that the leads shown in Table B are strapped to other 3A CC terminals, where they are picked up by other Berg connectors and cabled to the processor frame power circuit via the processor frame circuit. This is shown in Information Note 302.

3. DESCRIPTION BY ELEMENT

GENERAL

3.01 The various elements of CP1 are shown in detail on sheets J2, J3, and J4. Lead designations ending in 0 are low when active or in the one state. Lead designations ending in 1 are high when active or in the one state. The state of each key is monitored by the 3A CC and/or processor frame power circuit, and it is these circuits that take the appropriate action to perform the operations initiated from the control panel. Likewise, all panel indicators (lamps and LEDs), reflect the state of appropriate 3A CC and processor frame power unit circuits. (Three exceptions to this are the TEST MODE lamp which operates directly from a TEST MODE key contact, the GENERAL LED which operates directly from a REGSEL key contact, and the LAMP & PWR TEST key which has a contact to directly operate each status indicator.) The manner in which the 3A CC handles panel operation is determined by microstore instructions. This could be altered if the microstore is altered. The operations described herein assume the basic 1K word microstore loading used by No. 3 and No. 2B ESS.

COMMAND SWITCH - ELEMENT A

3.02 The EXEC (EXECUTE) key is a momentary-action key that is operated to initiate the preselected panel function. When this key is operated, the ground signal from the 3A CC on leads EXECK0G and EXECK1G (coaxial shields) is returned to the 3A CC double-rail on leads EXECK0 and EXECK1. Here it causes an interrupt signal that is recognized by the 3A CC as a control panel operation. The 3A CC routine to service this interrupt includes scanning other panel switches to identify the control panel operation that is to be performed.

3.03 Described in 3.04 through 3.14 are locking keys that preselect the panel function that is initiated by operating the EXEC key. UP is considered the operated or one position; DOWN is the nonoperated or zero position. A ground is sent to the 3A CC on the designated lead when the switch is operated to cause the defined action.

MODE SWITCHES - ELEMENT B

3.04 The following locking keys select modes:

(a) HALT - Cycle in a loop (HALT loop), where panel requests are honored but main memory instructions are not performed.

(b) STEP - Execute the main memory instruction at the address contained in the associated program address (PA) register.

(c) BASIC/EXTENDED - Allows the panel to operate with a 16-bit or 24-bit main memory. The BASIC position is used for a 16-bit memory. The EXTENDED position allows the high 8 or low 16 bits of memory to be accessed (under control of the HIGH BITS/LOW BITS key) in a 24-bit memory. The EXTENDED position is used by No. 2B ESS.

FUNCTION SWITCHES - ELEMENT C

3.05 Two register functions may be selected by locking keys.

(a) LOAD - Put the data pattern determined by the LOAD keys into the selected register.

(b) DISR (Display Register) - Show the contents of the selected register on the DISPLAY LEDs.

Note: Operation of both LOAD and DISR keys will cause a load operation followed by a display operation.

3.06 Two compare functions may be selected by locking keys.

(a) CMP ADR (Compare Address) - Match the 3A CC store address (SA) register with the address input (AI) register under mask of the address mask (AK) register. The 3A CC generates an internal signal when a match occurs.

(b) CMP DATA (Compare Data) - Match the 3A CC store data (SD) register with the data input (DI) register under mask of the data mask (DK) register. The 3A CC generates an internal signal when a match occurs.

Note: If both keys are operated, the 3A CC generates the match signal only when the data and address match simultaneously.

3.07 Four memory functions may be selected by locking keys.

(a) STO (Store) - The data determined by the LOAD keys is written into the memory at the address contained in the SA register.

(b) DISM (Display Memory) - The contents of the memory at the address contained in the SA register is shown on the DISPLAY LEDs.

(c) INC ADR (Increment Address) - The address contained in the SA register is incremented by one.

(d) HIGH BITS/LOW BITS - Selects the high 8 data bits (23 through 16) or low 16 data bits (15 through 0) to be read or stored when the BASIC/EXTENDED key is in the EXTENDED position. This key has no effect when the BASIC/EXTENDED key is in the BASIC position. When the control panel is in the EXTENDED mode and the HIGH BITS/LOW BITS key is in the LOW BITS position, only the low 16 LOAD keys and DISPLAY LEDs are valid for a memory function. Only the low eight bits of the LOAD keys and DISPLAY LEDs are valid when the HIGH BITS/LOW BITS key is in the HIGH BITS position. These low eight bits represent the high eight bits of memory.

Note: When more than one memory function key is operated, the designated functions will occur in the following order: store, display, and increment address.

REGISTER SELECT SWITCHES - ELEMENT D

3.08 The following keys select registers for the 3A CC control panel circuit.

(a) REGSEL - Selects one of two 16-register groups. When the key is not operated, GENERAL registers are selected and lead SGK1 provides the ground to light the GENERAL LED. SPECIAL registers are selected when the key is operated. In this case the GENERAL LED is not lit, but the SPECIAL LED is lit via a signal from the 3A CC.

(b) REGSEL 8, 4, 2, 1 - These keys are encoded hexadecimally to select 1 out of 16 registers in a group.

LOAD SWITCHES - ELEMENT E

3.09 The following switches are used to load data:

(a) LOAD switches 0 through 19 - Determine a data pattern (up to 20 bits) to be loaded into memory or registers.

(b) EN MAN PAR (Enable Manual Parity) - Defeats automatic parity generation on data patterns that are loaded and enables the PH and PL switches to determine the parity.

(c) PH (Parity High) - Sets parity over the high data field (bits 19 through 8 for a 20-bit word, bits 15 through 8 for a 16-bit word).

(d) PL (Parity Low) - Sets parity over the low data field (bits 7 through 0).

STATUS AND TEST SWITCHES - ELEMENT F

3.10 Five switches are used to control status and testing.

(a) RES CKT (Reset Circuits) - A momentary-action key that starts an initialization sequence in the 3A CC. Operation of this key causes ground from the 3A CC on leads RESK0G and RESK1G to be returned as a double-rail signal on leads RESK0 and RESK1.

(b) MANUAL - An alternate-action switch that selects manual or nonmanual states in the 3A CC. Panel functions are allowed only when the 3A CC is in the manual state. The ground on lead MANKG0 from the 3A CC is returned on lead MANK0 to achieve the manual state.

(c) TEST MODE - When this switch is operated, the ground on lead TMK0G is returned to the 3A CC on lead TMK0. Operation of the TEST MODE switch puts the 3A CC in the test mode, which allows certain operations that would not otherwise be permitted on an active 3A CC. These operations include power removal, panel operation, and disabling the on-line timers. Operation of the TEST MODE switch is not normally required, and the system is in a vulnerable state while the key is operated. Consequently, the TEST MODE key is a safety type (pull before operate) and is mounted behind the control panel. One contact on the TEST MODE switch lights the TEST MODE lamp to call attention to the test mode whenever the switch is operated.

(d) PWR (Power) - An alternate-action double-pole switch which controls the logic power for the 3A CC and other units in the processor frame. Leads PWRKAM (with PWRKAMG) and PWRKAB (with PWRKABG) signal the processor frame power circuit to turn power on (PWR switch operated) and off (PWR switch not operated). However the circuits within the processor frame power circuit also consider other signals from the 3A CC and will turn

power off only if the 3A CC is in the manual state and is either in the test mode or is locked off-line. Since it is possible to have the PWR switch in the OFF position and not have the power off, the state of this switch is monitored. Leads PKEY and PKEYR control a scan point, and lead PWRKBB is monitored directly via the 3A CC to alarm this condition.

(e) LAMP & POWER TEST - A momentary-action, double-pole switch. One contact completes the path to the STATUS indicators, so that all will light when the switch is operated. Lead LPTKAB operates the power alarm test (PAT) relay in the processor frame power circuit to test the power alarm circuits of the power modules in the frame. During the power alarm test, leads LPTKBC and LPTKBM bridge the appropriate relay contact to prevent the alarm signal that would otherwise occur.

STATUS INDICATORS - ELEMENT G

3.11 The MANUAL, ERROR STOPPED, ACTIVE, and STANDBY lamps are controlled directly from the 3A CC. Resistors R2 and R3 set the signal level compatible with the 3A CC driver, and transistor Q1 inverts the signal so that a high input causes the lamp to light. Resistor R4 keeps a current flowing through the lamps at a level too low to provide distinguishable illumination. This eliminates the transient current which would otherwise occur when a cold bulb is turned on. Diode CR1 provides the operate path for lamp tests.

3.12 The POWER and TEST MODE lamps are controlled by the processor frame power circuit and TEST MODE switch, respectively. Resistor R5 and diode CR2 provide the same "keep warm" current and lamp test access described in 3.11.

MODE AND FUNCTION INDICATORS - ELEMENT H

3.13 Three LEDs are used to monitor modes and functions.

(a) ENABLED - This LED is lit when the 3A CC grounds lead ENABL0 to indicate a compare function in process.

(b) HALTED - Lead HALTL0 is grounded by the 3A CC to light the HALTED LED when the 3A CC is cycling in a HALT loop.

(c) REJECT - Lead REJL0 is grounded by the 3A CC to light the REJECT LED when a requested panel function was not performed. In addition, the DISPLAY LEDs will all light at this time. Reasons for rejection include specifying more than one type of function (register and memory), combining the step mode with either a register or memory function, or attempting to load a register which is not allowed to be changed (eg, timing counter).

REGISTER SELECT INDICATORS - ELEMENT J

3.14 The following indicators show which register has been selected at the 3A CC control panel.

(a) SPECIAL - Lead SPLL0 is grounded by the 3A CC to light the SPECIAL LED when the SPECIAL/GENERAL key is in the SPECIAL position.

(b) GENERAL - Lead SGK1 is grounded by a contact on the SPECIAL/GENERAL key to light this LED when the key is in the GENERAL position.

(c) REGISTER 0 through REGISTER 15 - Leads R0L0 through R15L0 are grounded by the 3A CC to light the LED(s) dictated by the REGISTER SELECT keys.

Note: The EXTENDED designations for the REGISTER SELECT LEDs correspond to the dedicated assignment of some GENERAL registers for No. 2B ESS.

DISPLAY INDICATORS - ELEMENT K

3.15 The following display indicators occupy the top row of the 3A CC control panel.

(a) DISPLAY 0 through 19, PH, PL - Leads DB0L0 through DB19L0, PHL0, and PLL0 are grounded by the 3A CC to light the corresponding LED. These leads follow the state of the display buffer (DB) register.

(b) ENABLE MANUAL PARITY - Lead MPL0 is grounded by the 3A CC to light this LED when the ENABLE MANUAL PARITY key is operated.

4. OPERATION OF THE CONTROL PANEL

4.01 Usually, the HALT key is operated along with the keys that select the desired panel operation, so that the 3A CC cycles in the HALT loop following execution of the panel function. If a display operation is executed without the HALT key operated, the 3A CC will return to its regular program instruction sequence following the panel operation. This will alter the display. Call processing is not performed while the 3A CC is cycling in the HALT loop. Thus, using the TEST MODE key to allow use of the panel in the on-line 3A CC should be limited to emergency situations.

4.02 An exception to keeping the HALT key operated with the keys that select the panel function is the compare operation.

The 3A CC must be allowed to cycle through its program instructions in order to satisfy, and to act cn, the matching condition.

4.03 The following sequence of operations to load and display a register illustrates the operaticn of the 3A CC control panel.

(a) In the standby 3A CC, operate the MANUAL key and cbserve that the MANUAL lamp lights.

(b) Operate the register LCAD and DISPLAY keys and the MODE HALT key. No other function key should be operated.

(c) Use the REGISTER SELECT keys to define the desired register. Observe that the proper LED is lit.

(d) Set the data to be loaded into the register on the LOAL keys.

(e) Operate and release the EXECUTE key.

(f) Observe the loaded data on the DISPLAY IEDs.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 None.

2. FUNCTIONAL DESIGNATIONS

2.01 Lead designatiors ending in 0 are low (ground) when active, or in the one state. Lead designaticns ending in 1 are high (battery) when active, or in the one state.

2.02 Leads

Designation	Meaning
BAEXK0	Basic/Extended Operation Key
CADRK0	Compare Address Key
CDATK0	Compare Data Key
DB0I0-DBL19LC	Display 0 - Display 19 LED
DISMK0	Display Memory Key
DISPK0	Display Register Key
ENABI0	Enabled IED
EXECK0,1 EXECKK0G,1G	Execute Key
HAITI0	Halted IED
HIIOK0	High Bits/Low Bits (Memory) Key
IADRK0	INCR ADR (Memory) Key
I0K0-I19K0	Load (Input) Keys
LOADK0	Load Register Key
LPTKAB	Lamp and Power Test Key A Section Break-Contact
LPTKBC	Lamp and Power Test Key B Section Common-Contact
LPTKBM	Lamp and Power Test Key B Section Make-Contact
MANK0,0G	Manual Key
MANL1	Manual Lamp
MPK0	Manual Parity Key
MPL0	Manual Parity LED
OFFL1	Standby Lamp
ONL1	Active Lamp
PHK0	Parity High Key
PHL0	Parity High LED
PKEY	Power Key B Section Make-Contact
PKEYR	Power Key B Section Common-Contact
PLK0	Parity Low Key
PLL0	Parity Low LED
PWRKAB	Power Key A Section Break-Contact
PWRKABG	Ground Lead Paired with PWRKAB
PWRKAM	Power Key A Section Make-Contact
PWRKAMG	Ground Lead (Coaxial Shield) Associated With PWRKAM
PWRKBB	Power Key B Section Break-Contact
PWRL0	Power Lamp
REJL0	Reject LED
RESK0,1 RESK0G,1G	Reset Circuits Key
R0L0-R15L0	Register 0 - Register 15 LED
RS1K0,2K0,4K0,8K0	Register Select Keys

Designation	Meaning
SGK0,1	Special/General (Registers) Key
SPLL0	Special (Register) LED
STEPK0	Step (Through Program Instructions) Key
STCK0	Store (Load Memory) Key
STCPL1	Error Stopped Lamp
TMK0,0G	Test Mode Key

3. FUNCTIONS

3.01 Allows a data pattern to be loaded into any of the 3A CC GENERAL registers or designated 3A CC SPECIAL registers.

3.02 Allows the contents of the designated SPECIAL and GENERAL registers to be displayed.

3.03 Allows a comparison to be made between the main memory address and an external data pattern and between the main memory data and an external data pattern.

3.04 Allows the contents of a main memory location to be displayed.

3.05 Allows a data pattern to be written into a main memory location.

3.06 Allows a main memory program to be executed one instruction at a time.

3.07 Controls and monitors control unit power, and the 3A CC TEST MODE and MANUAL status bits.

3.08 Displays the following 3A CC status bits: ACTIVE, STANDBY, ERROR.

3.09 Provides the means for setting the 3A CC in an initialized state.

4. CONNECTING CIRCUITS

4.01 When this circuit is listed on a keysheet, the connecting information thereon should be followed.

(a) 3A Central Control Circuit - SD-1C900-01.

(b) Processor Frame Circuit - SD-1C910-01.

5. MANUFACTURING TESTING REQUIREMENTS

5.01 Manufacturing testing requirements are specified in the X-78889 specification.

SECTION IV - REASONS FOR REISSUE

D. Description of Changes

D.1 Corrected minor drawing errors.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 5344-RAM-LAW