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CIRCUIT DESCRIPTION

COMMON SYSTEMS

TAPE DATA CONTROLLER
CIRCUIT

SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The purpose of the tape data controller (TDC) circuit is to provide a magnetic tape memory system for the 3A central control (3A CC). In ESS applications, it provides a magnetic tape copy of the ESS generic programs, office translation modules, and other miscellaneous programs and data files needed as backup for the volatile main stores. It can be used to provide a semipermanent storage medium onto which office traffic study data, etc, can be written for analysis at a later time. It also provides a user-specified option to allow transmission of main store contents to and from a remote location.

2. GENERAL DESCRIPTION OF OPERATION

2.01 The TDC circuit contains the following functional units: serial peripheral interface (SPI), bus terminator (BT), buffer (BUF), cartridge tape transport (CTT), cartridge tape transport controller (CTTC), -48 volt to +5 volt dc-to-dc converters, power control switch, and, optionally, a synchronous data set controller (SDSC).

2.02 The CTT is a KS-21447 L2 minirecorder used to record and reproduce digital data in the ANSI-proposed 1600 bit-per-inch (BPI) phase-encoded format on a KS-21439, 1/4-inch magnetic tape cartridge.

2.03 The SDSC is a 2-circuit-pack option required for 2B ESS installations with the EF-2 generic. It may also be used in other systems where synchronous data link capability is required.

SECTION II - DETAILED DESCRIPTION

1. SERIAL PERIPHERAL INTERFACE (FS 1)

1.01 Communication between the TDC and the 3A CC is accomplished via the standard 3A serial channel. The SPI is a serial-to-parallel and parallel-to-serial converter used in all communication between the 3A CC and the TDC.

1.02 There is a serial input port to the SPI from each CC in the processor frame

and a serial output port from the SPI to each CC. The serial channel messages are 21 bits long and are encoded to contain both a data and a clock component.

1.03 The two input ports from the CCs are logically ORed together in the SPI and connected to a single data and clock recovery circuit, which separates the data and clock components of the input message. The clock portion shifts the data into a 21-bit register.

1.04 A parallel bus extends from the SPI to the other logical devices of the TDC. This bus consists of 16 information leads and two associated parity leads, six control leads, a clock lead, and four device response leads. The message from the CC (in the receiving register) is presented via this bus to all logical devices in the TDC. All command messages to the TDC contain a device address code which is interrogated by each device connected to the bus. Only the device with the matching address code will accept the command message.

1.05 When the proper device in the TDC has accepted the message, it requests, via one of the device response leads, that the SPI remove the message from the parallel bus.

1.06 A reply message from the selected unit will then be gated back onto the parallel bus, and back to the SPI to be shifted over the serial output port to the CC issuing the corresponding command message.

1.07 Additionally, the SPI checks each incoming 21-bit message from the CC for serial parity errors. If a serial parity error (an odd number of logical ones) is detected, the message is not gated onto the parallel bus; instead, a special serial parity error reply is transmitted back to the CC originating the message.

2. BUS TERMINATOR (FS 2)

2.01 The bus terminator provides the following three functions for the TDC:

(a) It provides a proper far-end electrical termination for the parallel bus extending from the SPI.

(b) It generates parallel parity on status replies to be sent to the CC at the request of the selected device.

(c) It contains a 16-bit register into which data can be loaded from the parallel bus and from which the data may be subsequently dumped back to

the bus for return to the CC. The latter function is provided strictly for maintenance purposes.

3. BUFFER (FS 3)

3.01 The BUF, a logical device on the SPI parallel bus, is used as temporary storage for data moving to or from the tape. The BUF reduces the real-time demands on the 3A CC during TDC data transfer. The BUF contains two 1024-bit serial buffer memories (shift registers), which are alternately available to either the CC (via the SPI), the CTTC, or the SDSC.

3.02 The control of these memories provides that one buffer memory (the off-line buffer memory) is available to and under the control of the CC. The other (the on-line buffer memory) is available to and under the control of the CTTC or the SDSC.

3.03 As a block of data is being read from tape, the input of the on-line buffer memory is connected, via a serial bus data line, to the output of the CTTC. Data read from the tape (approximately one bit every 21 USEC) passes through the CTTC, and into the on-line buffer memory. The output of the off-line buffer memory is connected to the input of a 16-bit word-framing shift register (ITR) in the BUF.

3.04 The CC can request data from the off-line buffer memory independently of on-line buffer memory operations. In response to each CC data request, the BUF shifts 16 bits out of the off-line buffer memory into the ITR and gates them, via the parallel bus, to the SPI to be sent to the CC.

3.05 When the on-line buffer memory is full (it has received 1024 data bits from the CTTC), the BUF control circuit automatically switches the on-line/off-line status of the buffer memories. That is, the buffer memory just filled by the CTTC becomes the off-line buffer memory, and its output is connected to the input of the 16-bit ITR. Also, the buffer memory just emptied by the CC becomes the on-line buffer memory, and its input is connected to the data output of the CTTC.

3.06 When the buffers switch, a BUF status bit is set, which indicates to the CC that the off-line buffer memory requires servicing.

3.07 When the system writes data onto the tape, this procedure is reversed. The output of the on-line buffer memory is connected to the data input of the CTTC, and the input of the off-line buffer memory is connected to the serial output of the

16-bit ITR. When the CTTC needs a data bit to write onto tape, it sends a shift pulse to the on-line buffer memory, and the next data bit is shifted to the CTTC write circuit.

3.08 The CC can send data, 16 bits at a time via the SPI, to the off-line buffer memory independently of any on-line buffer memory operations. Each 16-bit data word is loaded from the parallel bus into the ITR and then shifted into the buffer memory.

3.09 When the CTTC empties the on-line buffer memory, the buffers automatically switch in a manner similar to that described for a read operation. A BUF status bit is then set, indicating to the CC that the off-line buffer memory is available to be loaded with the next 1024 bits to be written.

3.10 An additional feature of the BUF circuit is that data transfers to and from the CTTC need not be in 1024-bit increments. Circuitry is provided in the BUF to take a segment of data (less than 1024 bits) in the off-line buffer memory and move it to the output of that buffer memory at the request of the CC. A counter in the BUF circuit retains a count of the number of valid data bits in the buffer memory.

3.11 When this buffer memory goes on-line, it will automatically switch after outputting only the valid data segment. A complementary feature is provided when reading into the on-line buffer memory via the CTTC. A control line from the CTTC can be asserted, which moves a data block of less than 1024 bits to the on-line buffer output and then switches the buffers. Data transfers from and to the SDSC are handled similarly.

4. CARTRIDGE TAPE TRANSPORT CONTROLLER (FS 4)

4.01 The CTTC accepts commands from the CC via the SPI and parallel bus, decodes the commands, and causes the proper sequencing of the control and data lines to the CTT and the BUF (if data transfer is involved). All data transfers to and from the magnetic tape involve use of the BUF circuit.

4.02 Information is stored serially on the magnetic tape, using a phase-encoded format at a data density of 1600 BPI on four independent data tracks. The data transfer rate during reading and writing is 48,000 bits per second (BPS).

4.03 The four tracks may be identified by number. Track 1 is unique in that it is write-protected by the CTTC so that program data cannot be overwritten or mutilated inadvertently. Information is grouped on each track in blocks consisting of a 16-bit data preamble, a string of 16-bit data words, a 16-bit cyclic redundancy check character, and a 16-bit data postamble. The preamble and postamble are automatically added to the data blocks by the CTTC during write operations and stripped from the data blocks by the CTTC during read operations.

4.04 Each block is separated from adjacent blocks on the same track by interblock gaps (IBG), which are nominally 1.55 inches long. Data error detection is performed automatically by a cyclic redundancy check (CRC) circuit in the CTTC read circuitry. This CRC check is performed during every read and write operation. When a writing operation is being performed, the data is read back from the tape, checked for CRC errors, and discarded by the CTTC. During a read operation, the data is checked by the CRC circuit and passed to the BUF for transmission to the CC. During the write operation the CRC character is computed and supplied as part of the data to the TDC by the processor.

5. SYNCHRONOUS DATA SET CONTROLLER (FS 7)

5.01 The SDSC accepts commands from the 3A CC and replies to the 3A CC via the parallel bus. Data is transferred between the 3A CC and the SDSC via the BUF circuit and the serial buffer bus.

5.02 The SDSC communicates with a remote location via its EIA interface to a user-supplied synchronous data set (SDS), key telephone set, and dial-up line. It is capable of operating at 2K,* 2.4K, 4.8K, and 9.6K BPS in half duplex mode. No hardware modification is required for operation at the various speeds, as timing is derived from the SDS. Both ends of the data link must have SDSs compatible in speed and function.

5.03 The SDSC is transparent to the data communications protocol used, except that the first characters of any message must be ASCII standard synchronization (SYN) characters. All data manipulations are done by the 3A CC.

5.04 Data transmitted or received via the SDSC is not transferred to or from tape but rather to and from the 3A CC main store.

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* K = 1000.

5.05 In a data transfer sequence a data link must first be established, either via an automatic calling unit (ACU) or by manual dial-up followed by switching of the telephone set to the data mode. Before manual switching to the data mode, the 3A CC must address the SDSC and set the data terminal ready bit in the control register.

5.06 The correct handshaking is then done between opposite ends of the line and between the respective SDSs and controllers. This handshaking is a function of the data communications protocol used and is performed by the 3A CC.

5.07 When the SDSC transmits data, the BUF circuit is first loaded from main store. The transmit clock from the SDS is then used to shift data serially from the BUF circuit through the SSSSDSC to the DS. The control characters needed by the receiving end for correct data interpretation are placed in the data stream by the transmitting 3A CC.

5.08 One of the bits in the control register may be set when the 3A CC loads the last 1024 bits of data into BUF to provide automatic line turnaround. This causes the transmitting SDSC to switch to the receive state as the last data bit is shifted from BUF to the DS. Switching from receive to transmit mode is done only under program control.

5.09 In the receive state, data is clocked from the SDS through the receive message register. Incoming data is discarded until detection of the first non-SYN after two or more consecutive SYN characters. The first non-SYN and all succeeding characters are shifted into the on-line buffer memory by the receive clock from the SDS. This continues until the carrier detect signal from the SDS stops, halting the clock.

5.10 The 3A CC must service the off-line buffer memory independently, emptying it as it automatically switches from on-line status. A failure to do this will result in a buffer overflow, setting the error state in the SDSC status register.

5.11 A call may be terminated under program control if the SDS has the proper options selected; or it may be done manually, by switching both ends of the data link to voice mode and hanging up the handset.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 **Battery Ranges**

+24V - 20.7 volts through 26.2 volts

-48V - -52.0 volts through -42.0 volts

1.02 The ambient office temperature range is 0º through 50º Centigrade.

2. FUNCTIONAL DESIGNATIONS

2.01 **Circuit Packs**

Designation	Meaning	FS
BT-A	Bus Terminator Circuit A	2
BT-B	Bus Terminator Circuit B	2
BUF-A	Buffer Circuit A	3
BUF-B	Buffer Circuit B	3
BUF-C	Buffer Circuit C	3
BUF-D	Buffer Circuit D	3
CTTC-A	Cartridge Tape Transport Controller Circuit A	4
CTTC-B	Cartridge Tape Transport Controller Circuit B	4
CTTC-C	Cartridge Tape Transport Controller Circuit C	4
CTTC-D	Cartridge Tape Transport Controller Circuit D	4
SDSC-A	Synchronous Data Set Controller Circuit A	7
SDSC-B	Synchronous Data Set Controller Circuit B	7
SPI-A	Serial Peripheral Interface Circuit A	1
SPI-B	Serial Peripheral Interface Circuit B	1
SPI-C	Serial Peripheral Interface Circuit C	1

2.02 **Power Converters**

Designation	Meaning	FS
PM1	Power Module 1	6
PM2	Power Module 2	6

2.03 Switches

Designation	Meaning	FS
SW1	TDC Power Switch	6

2.04 Tape Transports

Designation	Meaning	FS
CTT-J5	Cartridge Tape Transport Jack 5	5
CTT-J6	Cartridge Tape Transport Jack 6	5

3. FUNCTIONS

3.01 Provides a read/write magnetic tape memory system for the 3A CC.

3.02 Provides an optional capability to permit data linking between the 3A CC and a remote location.

4. CONNECTING CIRCUITS

4.01 When this circuit is listed on a keysheet, the connecting information thereon is to be followed.

(a) 3A Central Control - SD-1C900-01.

(b) Frame Power - SD-1C909-01.

(c) Maintenance Frame - SD-1C912-01.

(d) KS-21447 Mini-Recorder Circuit for Recording and Reproducing Digital Data - SD-97736-01.

5. MANUFACTURING TESTING REQUIREMENTS

Intermediate Requirements

5.01 None.

End Requirements

5.02 The manufacturing testing requirements are specified in the X-78886 specification.

SECTION IV - REASONS FOR REISSUE

B. Changes in Apparatus

B.1 Added

SDSC-A Circuit Pack JK14, Option Y - App Fig. 2

SDSC-B Circuit Pack JK15, Option Y - App Fig. 2

D. Description of Changes

D.1 Added the synchronous data set controller (SDSC) as a circuit option. This requires a complex blackplane wiring (option Z) in addition to the circuit packs (option Y) described in B.1.

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