

CIRCUIT DESCRIPTION

CD-1C905-01
ISSUE 3A
APPENDIX 3AC
DWG ISSUE 7AC
DISTN CODE 1N98

12

COMMON SYSTEMS

TELETYPEWRITER CONTROLLER UNIT

CIRCUIT

CHANGES

B. Changes in Apparatus

B.1 Replaced

FA1059 series
three packs

Replaced by

FA1072 circuit
pack

D. Description of Changes

D.1 Used new FA1072 circuit pack in ESS applications
instead of FA1059 series three pack.

D.2 FA1059 circuit pack used on auxiliary processor applica-
tions only.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 2511-CMD-TSG

CIRCUIT DESCRIPTION

CD-1C905-01
ISSUE 3A
APPENDIX 2A
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COMMON SYSTEMS

TELETYPEWRITER CONTROLLER UNIT
CIRCUIT

CHANGES

D. Description of Changes

D.1 Strapped pin 7 to pin 14 on the 927D connector of the teletypewriter controller unit (TTYC). This change squelches the carrier from the associated 108D data set and thus eliminates interference on call placement through a 4A office. The carrier is now initiated after the call is placed.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 5511-CMD-TSG

CIRCUIT DESCRIPTION

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ISSUE 3A
APPENDIX 1AC
DWG ISSUE 5AC
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10

COMMON SYSTEMS

TELETYPEWRITER CONTROLLER UNIT
CIRCUIT

CHANGES

D. Description Changes

- D.1 Changed drawing to provide for the connections of alarm output and alarm reset leads when the TTYCU is mounted in a miscellaneous frame for No. 2B and No. 3 ESS or similar applications. Equipment Note 207, and Information Notes 316 and 317.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 5515-AAN-LEG

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COMMON SYSTEMS
 TELETYPEWRITER CONTROLLER UNIT
 CIRCUIT

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<u>SECTION I - GENERAL DESCRIPTION</u>	
<u>1. PURPOSE OF CIRCUIT</u>	
1.01 The teletypewriter controller unit (TTYCU) supplies mounting facilities and power conversion for two teletypewriter controllers (TTYCs). A TTYC provides the interface between the 3A central control (3A CC) and system teletypewriters (TTYs). The controller connects the 3A CC and up to four TTY ports in a hub arrangement whereby signals from any one are seen by the others. Communications between the 3A CC and the TTYC are over a 6.67-megabit serial I/O channel. A connection to the 3A CC interrupt bus is also provided so that the TTYs can be serviced on a demand (rather than a scheduled) basis.	
1.02 The ASCII-formatted characters are passed between the TTYC and TTY, or data set, in an asynchronous serial format. Each port can accommodate (in any combination) a local Electronic Industries Association (EIA) compatible TTY, a 20-mA current loop TTY, or a remote TTY via a 108-type data set private line arrangement.	
<u>SECTION II - DETAILED DESCRIPTION</u>	
<u>1. PHYSICAL ARRANGEMENT</u>	
1.01 The TTYCU provides mounting, connecting, and power-control facilities for two TTYCs. The TTYCs are called left and right (as viewed from the rear of the TTYCU). The TTYC ports 0 through 3 are associated with the right TTYC, and ports 4 through 7 are associated with the left TTYC. A 25-terminal line connector and an interface circuit pack (CP) are available for each port to allow operation with a local current loop, EIA compatible, or remote TTY.	

1.02 The TTYC was designed to operate with the 3A CC and will be described in that light. Other processors that employ the serial I/O data format of the 3A CC can be substituted for it. Each TTYC has a receive (R), send (S), and interrupt (I) connector assigned to each of two 3A CCs (CC0 and CC1). A 3A CC serial I/O channel connects to the R and S connectors (receive and send are as viewed from the TTYC). The 3A CC serial I/O channel uses transformer coupling and matched transmission lines (coaxial cables). The coaxial cable shields are grounded at the 3A CC and are floating at the TTYC to achieve dc isolation. The interrupt signal is a 1-microsecond pulse sent by the TTYC when a TTY character becomes available to the 3A CC. This signal connects to the 3A CC interrupt circuits when the TTY is serviced in the demand mode.

1.03 The left TTYC is shown on FS 1 and FS 3. The right TTYC is described on FS 2 and FS 4. Power and alarm circuits for the unit are shown on FS 5. In the following functional description of each FS, a common description will be given for FS 1 and FS 2, as these are for corresponding portions of the two controllers. The same treatment will also be given to FS 3 and FS 4. In the common description, the leading mnemonic character, L for left and R for right, will be omitted and can be applied by the reader as appropriate. The TTYC ports identified as 0/4 through 3/7 in the common description should be interpreted as 0 through 3 for the right TTYC and 4 through 7 for the left TTYC. Refer to the appropriate circuit pack schematic (CPS) drawings for descriptions at the gate level.

1.04 In general, the elements identified as "channel" circuits are involved in operations between the 3A CC and the TTYC. Those called "line" circuits function in the information exchange between the TTYC and the TTY. Mnemonics that end in 1 generally indicate a high condition for the active or one state. Those that end in 0 generally describe a low condition for the one or active state.

2. CONTROL AND INTERFACE CIRCUITS - FS 1 AND FS 2

OVERVIEW

2.01 These circuits control the exchange of information between the 3A CC and the TTYC port connectors regarding direction, format, signal level, data rate, and availability of the port. Data exchanged between the 3A CC and TTYC are in the form of bipolar pulses. The 21-bit 3A CC I/O message format is used with the TTYC as shown in Information Note 302. Only the low data field of the 3A CC output

message is used. The high data field is important only because its low two bits (message bits 12 and 13) affect the parity of the incoming message as recorded by the TTYC. These bits should be the same so as to retain the parity set by the PL bit. Usually, the 3A CC sends an all-zeros high data field. The PH bit associated with this data has no effect, as the TTYC is not recording parity when it is received.

2.02 Two types of message are sent by the 3A CC to a TTYC. A character message is one that is headed by a 011 start code and in which the low data field contains an ASCII-encoded character that is to be printed on the TTY. The control message is headed by the 101 start code. The data field in this message is used to enable or disable the TTYC ports and/or clear, or set a flip-flop that simulates port alarms. Bits labeled PA through PD in this message correspond to ports 0/4 through 3/7, and the bit labeled ALM controls the test flip-flop. The EN/DIS bit functions with these bits such that if the EN/DIS bit is a one, each port (or the test flip-flop) which has a one in its bit position will be enabled. If the EN/DIS bit is a zero, each port (or the test flip-flop) which has a one in its bit position will be disabled. Each port (or the test flip-flop), that has a zero in its bit position will not be changed for either condition of the EN/DIS bit.

2.03 The 3A CC follows the data portion of its transmission with an all-zeros bit stream until it receives a return message from the TTYC (or until a time period is exceeded in which the return message is expected). The TTYC uses the continuing bit stream to process the received message and to generate bipolar data for the return message. Thus, data is passed from the TTYC to the 3A CC only when (and every time that) the 3A CC sends to the TTYC. Two modes of operation are currently used. The 3A CC can communicate with the TTYC on a scheduled basis or when stimulated by an interrupt signal from the TTYC.

2.04 As shown in Information Note 302, the TTYC to 3A CC message format resembles the received message. In this direction, the "noncharacter" message contains the present status of each port. A one in the state field for a port indicates that port is enabled. A one in the alarm field for a port indicates that the port has an alarm. If the test alarm flip-flop is set, all ports will indicate an alarm regardless of the true alarm state. As was the case for the received message, the "noncharacter" outgoing message is headed by a 101 start code, and the character message is headed by a 011 start code. An additional data field (encoded 1-out-of-3 to require a PH bit of zero) is part of each TTYC to 3A CC message. This provides the 3A CC with information about the TTYC disposition of

the incoming message. A return code of 001 indicates that the TTYC received the incoming message with bad parity. The 010 code indicates that the TTY is actively typing or printing a character (ie, it is busy). The 100 return code indicates that the TTY is idle.

2.05 The action taken by the TTYC in response to a 3A CC message depends on:

- (a) The parity (bad or good) of the message received
- (b) The type (control or character) of message received
- (c) The availability in the TTYC of a character that has not been returned to the 3A CC (character ready or not ready)
- (d) The busy-idle state of the TTY (rest or not rest).

2.06 The TTYC response for all combinations of input is summarized in Information Note 303. Important points regarding the treatment of the input message are:

- (a) No action will be taken for the data field of a bad parity message.
- (b) The data field for each good-parity control message will update the port status.
- (c) The data field for a good-parity character message is forwarded to the TTY only if there is no character ready and the TTY is idle.

2.07 Important characteristics of the return message include:

- (a) A status message with the bad-parity return code will be returned for a bad-parity incoming message regardless of other conditions.
- (b) A ready character will be returned, and the ready flag cleared, in response to either good-parity incoming message.
- (c) The port and alarm status returned is current (ie, as updated by an incoming good-parity control message).

2.08 Two 3A CC messages are required for each character to be printed. The first message delivers the character to the TTYC. As the character is sent to the TTY, it is looped around in the TTYC and sets the character-ready flag. A new character will not be passed to the TTY by the TTYC until the ready character is retrieved by the 3A CC. Thus, the second message is required. This loop-around feature allows

the 3A CC to verify that the character was handled properly by the TTYC.

2.09 A character to be printed is sent to the port connectors of all enabled ports via leads S0/40 through S3/70. At this point the character is at EIA level in an 11-bit, serial, 100-WPM start-stop format as shown in Information Note 304. A typed character appears at EIA level on leads R0/30 through R7/0 in the format shown in Information Note 304. Only one port on the 3A CC should be the source of the typed character at a given time. The input signal from a disabled port is ignored by the TTYC. Note that a typed character is inputted on the appropriate R0/40 through R3/70 lead and is outputted on the associated S0/40 through S3/70 lead (as well as the other S0/40 through S3/70 leads) to be printed.

2.10 The port alarm signal is at EIA level on alarm leads AL0/40 through AL3/70. The alarm is used to indicate low paper for local TTYS and loss of carrier for remote TTYS.

CHANNEL INTERFACE (CHIF) *FC 200*

2.11 These circuits properly terminate the 3A CC I/O lines and perform the level conversion (pulse/logic) for signals exchanged between the 3A CC and the TTYC. Bipolar data input from 3A CC0 or 3A CC1 are on leads DI0P/N and DI1P/N, respectively (P indicates the signal lead, and N indicates the shield connection of the coaxial cable that connects the units). The data bits appear at logic level on lead ID0. A timing signal is produced for each data bit on lead SHFT0. This signal occurs nominally in the center of the bit interval when lead ID0 is stable and dictates when lead ID0 is sampled. When incoming data is present, lead IDPC is active and arms the reset pulse produced on the IDOV1 lead when the incoming data stops. The IDOV1 lead produces a 500-ns pulse (nominal) that occurs within 150 ns after the last data bit. It initializes CHIF and channel control (CHCTL) circuits to the state to receive the next message. Leads ZACT0 and OACT0 indicate which 3A CC is the source of incoming data. Lead ZACT0 is active with CC0 and blocks the input from CC1. The ZACT0 lead also signals the CHCTL to activate the ENZ00 lead when it is time to transmit, so that the outgoing message is directed to CC0. The OACT0 and ENO00 leads act in a similar manner for CC1 when it is active.

2.12 The outgoing data appears at logic level on lead OF0. It is converted to bipolar form and sent to CC0 or CC1 via lead DO0P/N or DO1P/N as directed by lead ENZ00 or ENO00.

2.13 The character-ready signal appears on lead SINT0. It is converted to a 1-USEC

(nominal) pulse and sent as an interrupt signal to CC0 and CC1 by leads ICP/N and IIP/N.

CHANNEL CONTROL (CHCTL) *FA 1058*

2.14 The CHCTL circuits capture and process the 3A CC message. These circuits consist of a 15-bit shift register, the channel buffer (CB), an 8-bit status register, the status buffer (SB), and a sequencer to control the data operations. The CB is initialized to the all-zero state by the previous IDOV1 signal. Each data bit of an incoming message is shifted into the CB by its SHFT0 signal until a one is in the least-significant CB position. Further shifting of the CB is inhibited at this time, and the SHFT0 signals from the continuing incoming bits drive the sequencer through the various operations required to process the message. Each incoming bit interval defines a time period during which a control signal may be active. The start code and parity of the incoming message, the character-ready flag (RDYG10), and busy/idle status (RSIA0) of the line circuits are combined with the timing signals to process the message. The RDYG10 and RSTAO signals are buffered by the CHCTL circuits so that their indications are stable through the process cycle.

2.15 The message data field is enabled to control the SB port enable bits by lead CBXSB0 (which is shown as a test point). Port enable signals for ports 0/4 through 3/7 are passed to the line control (LNCTL) circuits on leads EPAG0 through EPDG0, respectively.

2.16 A character is passed from the CB to an LNCTL register, the line buffer (LB), on leads CB0G10 through CB7G10. When this is to occur, lead CLRLE0 clears the LB and, at a later bit interval, lead CBXLE0 enables the gating path for this data. Lead STRT0 is active at a subsequent time interval to start the transmission of the character to the TTY by the LNCTL circuits.

2.17 When the incoming message data field is disposed of, the CB is cleared and the return message is loaded into it. If conditions dictate a status message, an internal CHCTL signal, SBXCB0, is active. The SBXCB0 signal sets the 101 start code and gates the SB to the CB data field. The SB contains the enable status for each port in its low four bits and the alarm status of each port as determined by leads SALMA1 through SALMD1 or by the alarm test flip-flop in the high four bits.

2.18 When conditions indicate that a character should be returned to the 3A CC, LBXCB0 (shown as a test point) is active to load the CB. This sets the 011 start code and gates the contents of the line register

(LR), the LNCTL register that has the character received from the TTY, to the CB data field. The leads LROG10 through LR7G10 are the LR output leads. Lead CLRDY1 clears the ready flag at a following bit interval whenever the LR has been gated to the CB.

2.19 At the appropriate time, lead ENZ00 or ENO00 becomes active, based on lead ZACT0 or OACT0. This enables the CB contents to be shifted out on lead ODO to the CHIF circuits. Shifting of the CB is once again controlled by lead SHFT0. Parity is calculated for the low data field as it is shifted through the CB, and the PL bit is sent accordingly. All zeros are sent following the 1-out-of-3-bit return code as long as the 3A CC continues to send data. The zero PH bit seen by the 3A CC will be correct, since it interprets the 3-bit return code plus the next five zeros as the high data field.

2.20 When the data stream from the 3A CC stops, lead IDOV1 pulses to initialize the CHCTL circuits. The CB and the parity detector are cleared, and lead ID0 is connected to the CB serial input in preparation for the next message at this time.

LINE CONTROL (LNCTL) *FA 1059*

2.21 Access to and from a common signal line by each TTYC port and the 3A CC is provided by the LNCTL circuits. Leads TPA0 through TPD0 pass a character as it appears on the signal line to ports 0/4 through 3/7. Leads FPAI1 through FPDI1 pass the character from the ports to the signal line. The character is passed over the signal line in a 10- or 11-bit serial start-stop format. This is shown in Information Note 304. The path to and from the signal line for each port is under control of the appropriate enable lead, EPAG0 through EPDG0. The LB provides the 3A CC connection to and from the signal line.

2.22 The LNCTL circuits are in the rest state when there is no TTY traffic. The LB and all ports present the mark (one) condition to the signal line in this condition. This mark signal is sent by the LNCTL circuits to all ports and the LB. When a port is disabled, its connection to and from the signal line is held in the mark state. The signal line will follow an input from any enabled port on the LB, and this signal will be sent to all enabled ports and the LB.

2.23 A typed character from an enabled port will appear on the signal line in the format shown in Information Note 304. This will be forwarded from the signal line to all other enabled ports and will cause the character to be printed on the devices connected to the enabled ports. The signal will not appear on the output of the port

from which it is being received. Local copy at the TTY from which the character emanated is provided in another manner and is described in Section III. The transition of the signal line from mark to space (caused by the leading edge of the start bit) takes the LNCTL circuits out of the rest state into the receive state. The signal line is resampled at 1/4 and 1/2 of the start bit interval. If the signal line has returned to the mark state during the sample times, the LNCTL circuits will return to the rest state. If the signal line is still in the space state, the LNCTL circuits will continue in the receive state until the entire character has been received.

2.24 Bit-timing signals for this process are derived by counting LTIM1 signals. Each bit of the data field is shifted serially into the LB at the center of the bit interval. The LB is not shifted for the start or stop bits. Thus, the LB contains the complete character at the middle of bit time eight and retains it until another operation is started. At the end of bit time 9 or 10 (the first or second stop bit, depending on the selected option) the LB contents are gated to the LR, the LNCTL circuits are returned to the rest state, and lead RDYG10 is set to the character-ready state. The latter generates an interrupt signal to the 3A CC via lead SINT0 and the CHIF circuits. The LR retains the character until it is replaced by another. For a continuous input stream with no gap between characters, the LB holds a character for three or four bit intervals (from the middle of the last data bit, through one or two stop bits and one start bit, to the middle of the first data bit) and the LR holds the character for one character interval.

2.25 A character that is to be sent from the 3A CC to a TTY is passed from the CHCTL to the LB on leads CB0G10 through CB7G10 under control of leads CLRLB0 and CBXLB0. The CHCTL then activates lead STRT0 to put the LNCTL in the state where the character will be transmitted to the TTYs. In this mode, the signal line is held in the space condition for one bit time. Then each bit of the LB is shifted onto the signal line in sequence. The signal line is returned to the mark condition for the two stop bits. At the end of the 10th- or 11th-bit time, the LNCTL circuits are returned to the rest state, the LB is gated to the LR, and lead RDYG10 is activated. As the LB is shifted to the signal line, the signal line is shifted back into the LB. As a result the character that was sent over the signal line is back in its original position in the LB when the LB is gated to the LR. The 3A CC can thus monitor the manner in which the character was handled by the TTYC.

LINE TIMER (INTIM)

2.26 A 308.48-kHz signal (LTIMO1) is supplied on lead LTTBC1. This is the source of bit-timing signals for the LNCTL circuits to process the TTY character. The LNCTL circuits contain a counter, the outputs of which can be optionally wired to provide 110-, 150-, 300-, 600-, and 1200-BAUD transmission rates (See Circuit Note 109 for optional wiring information).

LINE INTERFACE (LNIF) *FC 200*

2.27 These circuits convert between EIA-level signals at the port connectors and logic-level signals at the LNCTL circuits. Correlation between the converted signals is shown in Table A.

MATED OR NONMATED OPERATION - OPTIONS 3 AND 4

2.28 The description thus far applies to nonmated operation of the TTYC which is the usual mode. The two controllers are affected by these modes in that a choice of CPs is available to provide the CHIF, LNTIM, and LNIF circuits. The CHIF and LNTIM circuits are identical on each of the two CPs. The LNIF circuit function previously described is for the FC200 CP. The LNIF circuits on the FC261 CP are modified to accommodate the mate arrangement. This will be described in detail in another section of this CD. The two CPs are pin compatible so that no unit wiring changes are required to provide either arrangement.

2.29 The LNCTL circuits can be optionally wired for 10- or 11-bit character operation. With 10-bit operation, the character contains one stop bit. With 11-bit operation, the character contains two stop bits (See Information Note 304). Model 33 or 35 TTYs operate with 11-bits per character at 110 BAUD. Model 40 TTYs are generally optioned to operate with 10-bits per character.

3. TTYC PORT CONNECTORS - FS 3 AND FS 4

3.01 Each port has an associated CP connector, and line connector. These allow the flexibility of tailoring the TTYC output to a TTY type. The ports can be arranged in any combination. No unit wiring modifications are required to accommodate the different types of TTY. The TTYC output is defined by the CP type that is provided in the CP connector, and by connections to the plug that mates with the line connector. Operation of the TTYC port arranged for each type of TTY is described in 3.02 through 3.14.

TABLE A
SIGNAL COPRELATIONS

SIGNAL	EIA LEVEL	LOGIC LEVEL
Received Data	R0/40 - R3/70	FPAI1 - FPD11
Transmitted Data	S0/40 - S3/70	TPA0 - TPD0
Alarm	AL0/40 - AL3/70	SALMA1 - SALMD1

LOCAL EIA OUTPUT

3.02 Four signals are exchanged with the EIA device. No CP is required for this output, because the LNIF circuits function at the EIA level. Leads S00/70, R00/70, and AL00/70 connect to the EIA devices EA (transmitted data - to EIA device), EB (received data - from EIA device), and CF (loss of carrier or other alarm indication) leads, respectively, at the line connector.

LOCAL CURRENT LOOP

3.03 The CP connector is equipped with an AR17 CP, which provides level conversions between the LNIF EIA signals and a TTY that operates from a 20-mA current loop (eg, a model 35 TTY). A send loop, a receive loop, and an alarm loop connect the TTYC and the TTY. The TTY is connected for full duplex, although the operation is actually half duplex in that send loop signals from the TTY are repeated by the TTYC on the receive loop. The send and receive loops share a common battery lead. In the idle condition, the negative signal on the S00/70 lead is connected through terminals 14 and 11 of the line connector and its associated plug to terminal 9 of the CP connector. This turns on the PNP transistor on the AR17 that connects through 470 ohms to terminal 3. Receive loop current thus flows from -24 volts at line connector terminal 10, through the TTY select magnet driver (SMD) and limiting resistor, through line connector terminal 2 and CP terminal 3, and through the AR17 limiting resistor and saturated PNP transistor to ground. When a character is to be printed, the TTYC will change lead S00/70 between positive and negative in the format shown in Information Note 304. This causes opens and closures of the TTY receive loop in the same format. The TTY decodes the loop signals and prints the proper character.

3.04 The TTY send circuit is from -24 volts at terminal 10 of the line connector, through the signal regeneration

(SIG REGEN) circuit at the TTY, and through terminal 3 of the line connector to CP terminals 2 and 4 to the R00/70 lead. The R00/70 lead is held negative (marking) when the TTY is not typing. A character typed at the TTY causes the SIG REGEN circuit to open and close the send loop in the format shown in Information Note 304. When the send loop is open, CP terminal 4 is pulled positive by the AR17 by means of its +24 volt connection through the 8200-, 2200-, and 1500-ohm resistors. The loop opens and closures are passed to the TTYC line circuits via lead R00/70.

3.05 The local copy diode D1, on the AR17 circuit pack, allows for the printing of a character which has been typed on the TTY keyboard. The NPN transistor conducts when the TTY signal regenerator opens for the space condition. This cuts off the PNP transistor and opens up the TTY receive loop for the space condition.

3.06 The TTY alarm signal is a closure to the ground supplied on line connector terminal 7. In the alarm state, ground appears at terminal 8 of the line connector, which connects to the LNIF circuits via alarm lead AL00/70.

REMOTE OPERATION

3.07 When the TTY is at a distance that exceeds the limits for local operation (See Part 1 of Section III.), it can be operated over a private telephone line with a 108-type data set (DS). In this mode, a 108D data set is equipped at the port CP connector. The mark/space conditions at lead S00/70 connect through line connector (and its associated plug) terminals 14 and 2 to CP terminal 3. The 108 DS converts these to frequency shift data at CP terminals 15 and 16. These signals appear at line connector terminals 25 and 18, where they are available as ring and tip for a private telephone line. The 108D sends data at 1270 kHz for a mark and 1070 kHz for a space.

3.08 Received data at 2225 kHz for a mark and 2025 kHz for a space is converted to EIA level at CP terminal 10. This connects to the LNIF circuits via lead R00/70.

3.09 The incoming signal is also monitored for its presence by the DS. Loss of signal results in CP terminal 7 going to ground, which is forwarded to the LNIF circuits as a port alarm by lead AL00/70.

3.10 Provision must be made at the remote location for converting the frequency shift data to a form acceptable by the remote TTY. This can be accomplished with a DAS820D/DS108E arrangement if the remote TTY is a model 35.

3.11 The DS108D is at the TTYC end of the private line by convention. Operationally, the 108D and 108E can be interchanged. The 108E must be arranged with options corresponding to those designated for the 108D in this event. The two types of data sets are pin compatible.

3.12 With the options specified, the 108-type data sets and the AR17 CP are pin compatible over the range of terminals used. This avoids wiring changes on the unit to select the desired interface.

MATED OPERATION

3.13 Mated operation allows two TTYCs to be interconnected such that a TTY connected to either is accessible from each. This arrangement is used for the maintenance TTY channel in the No. 2R ESS where TTYC0, powered from the A power bus, is mated to TTYC1, powered from the B power bus. The local maintenance TTY connects to port 0 of TTYC0, while the remote maintenance TTY connects to port 0 of TTYC1. Information Note 305 shows the cross-coupling of two TTYCs. Two ports of each TTYC are involved in the interconnection, leaving two ports at each controller to connect TTYS. An FC261 CP in each TTYC provides the LNIF circuits for mated operation. Space limitation on this CP dictates a further restriction. Port 1 of each TTYC cannot receive data or alarm signals and therefore should operate with receive only (RO) TTYS.

3.14 The 3A CC is active with one of the mated controllers at a time. For instance, a character outputted via TTYC0 appears on lead TPA0 and is passed to its TTYS on leads S00/40 and S10/S50. The same information on lead TPD0 is fed to TTYC1 LNIF circuits through leads S30/S70 of TTYC0 and S20/S60 of TTYC1, and sent to TTYS connected to TTYC1 via leads S00/S40 and S10/S50. An input from the TTY at TTYC1 port 0 is passed through leads R00/40 and R20/00 of TTYC1 to lead R30/70 of TTYC0, where it is passed to the TTYC0 signal line in the usual manner on lead

FDPD11. Thus, the TTY at TTYC1 operates via TTYC0. Similar operations occur if the roles of TTYC0 and TTYC1 are interchanged in the preceding description. Note that the TTYS connected to the TTYC to which the 3A CC is not communicating (ie, the standby mated TTYC) are accessible even when the standby TTYC is inoperable except for its LNIF and power circuits. In the event of a power or LNIF failure, the TTY connected to that TTYC is inoperable, but the TTY at the mated TTY will function.

3.15 Any combination of local, remote, EIA, and current loop TTY is allowed at the available ports of mated controllers subject only to the RO limitation at port 1 as discussed in 3.13.

4. POWER AND ALARMS - FS 5

4.01 The TTYCU operates from the office +24 and -48 volt power sources. Converters in the TTYCU derive +3 volts for the logic and -24 volts for the EIA circuits from these potentials. Unit power is controlled by the power switch (PWPSW) which supplies -48 volts to the -24 volt converter (-24VCONV) and +24 volts to the +3 volt converter (+3VCONV). A lamp in the PWRSW is lit for the power-on state. Direct connections supply -48 volts to the +3VCONV and +24 volts to the FB152 reference CP(REF).

4.02 The +3VCONV is a switching regulator that converts -48 volts to +3 volts at up to 5 amperes. The FC21 CP (FIL) and REF circuits function with the +3VCONV to maintain its output in the range of 2.95 to 3.11 volts. Excursions outside this range will cause a power alarm (PA) signal to be generated by the +3VCONV. This will illuminate the +3VCONV alarm LED. The PA signal follows the voltage output (ie, if the voltage returns to within limits, the signal will cease), but the LED remains lit until the alarm is reset by grounding the NPA lead or turning off unit power.

4.03 If the overvoltage condition is sufficient (in excess of the PA limit but always less than 4.4 volts) or if an overcurrent condition exists (6.6 amperes \pm 1.2 amperes), a fuse alarm (FA) signal is generated by the +3VCONV which will also shut down. The converter is restarted by turning power off and back on when the FA condition is removed.

4.04 A 12-volt reference signal is generated by the REF circuit for the 3-volt power regulation circuits. If this signal is detected to be out of limits by the REF circuit, it will cause a PA. This PA will light an LED on the FB152 CP. The LED can be extinguished when the trouble is cleared by momentarily grounding the NPA lead.

4.05 The FIL circuit provides filtering for the +3 volt bus and monitors its potential. The FIL circuit functions with the +3VCONV via +3REF and +3REG to maintain the +3 volt bus within limits.

4.06 The -24VCONV circuit contains two switching regulators that convert -48 volts to -24 volts. A separate -24 volt output (L-24 and R-24) capable of 500 mA is provided for each TTYC in the unit. Independent overcurrent protection shuts down the appropriate regulator without affecting the other.

4.07 The FALM and PALM circuits latch the FA1 and PA1 signals when they occur and operate the MJ and MN relays, respectively. A make-contact of each of these relays is connected across the +24 volt and fuse alarm buses when the TTYCU is equipped in a miscellaneous frame. The frame fuse alarm relay operates for either alarm condition. The alarm signal is removed by turning the TTYC power off. If the cause of the alarm has been removed, the alarm relays will be released when power is restored.

4.08 The FA1, PA1, PAT, and NPA nets are connected to the maintenance frame power unit for TTYCUs equipped in that frame. Circuits in the power unit collect and report alarms. Grounding the NPA lead extinguishes the +3VCONV and REF LEDs in this frame. A reset key in the power unit provides this capability. The PAT1 lead is activated to test the ability of the +3VCONV to generate a PA. The PAT1 lead is controlled, and the converter response on leads PA1 and NPA0 is monitored, by the maintenance frame power unit circuit.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 TTY Loop Length: For current loop operation, the total loop resistance between the TTYC port and the TTY machine should not exceed 40 ohms. The TTY machine should be arranged for 20-mA operation.

1.02 EIA Operation: The cable connecting the TTYC to the EIA machine shall not exceed 50 feet and shall have capacitance such that the sum of cable plus terminator capacitance does not exceed 2500 picofarads measured between a signal lead and signal ground.

2. FUNCTIONAL DESIGNATIONS

2.01 Circuit Pack Elements

<u>Designation</u>	<u>Meaning</u>
FALM	Fuse Alarm
FIL	+3 Volt Reference and

<u>Designation</u>	<u>Meaning</u>
	Filter
L/R CHCTL	Left/Right Channel Control
L/R CHIF	Left/Right Channel Interface
L/R LNCTL	Left/Right Line Control
L/R LNIF	Left/Right Line Interface
L/R LNTIM	Left/Right Line Timing
PALM	Power Alarm
REF	+12 Volt Reference
-24VCONV	-48 to -24 Volt Converter

2.02 Key/Lamp

<u>Designation</u>	<u>Meaning</u>
PWRSW	TTYCU Power Switch

2.03 Plug-in Units

<u>Designation</u>	<u>Meaning</u>
P0DS - P7DS	Data Set for Ports 0 through 7
P0TTYIF - P7TTYIF	TTY Current Loop Interface Ports 0 through 7
+3VCONV	-48 to +3 Volt Converter

3. FUNCTIONS

3.01 Converts the ASCII character received from the 3A CC I/O channel connection to serial, 10- or 11-bit, start-stop format 110-, 150-, 300-, 600-, or 1200-BAUD transmission rates and repeats the character over each enabled TTY port.

3.02 Converts the ASCII character received from a TTY to a format compatible with the 3A CC I/O channel.

3.03 Repeats the character received from one TTY port to all other enabled TTY ports.

3.04 Provides a return message in response to each I/O message received from the 3A CC. The return message contains a character, if available, or TTYC status information.

3.05 Provides an interrupt signal to the 3A CC at the end of each character received from or sent to a TTY port.

3.06 Provides current loop or EIA signals to each TTY port designated for local operation.

3.07 Provides for private line operation via 103-type data set for each TTY port designated for remote operation.

4. CONNECTING CIRCUITS

4.01 When this circuit is listed on a keysheet, the connecting information thereon should be followed:

- | | | | |
|-----|-----------------------------|---------|-----------|
| (a) | 3A Central
SD-1C900-01. | Control | Circuit - |
| (b) | Processor
SD-1C910-01. | Frame | Circuit - |
| (c) | Maintenance
SD-1C912-01. | Frame | Circuit - |

4.02 Refer to the information notes for typical TTY connections.

5. MANUFACTURING TESTING REQUIREMENTS

5.01 Manufacturing testing requirements are specified in the X-78888 specification.

SECTION IV - REASONS FOR REISSUE

B. Changes in Apparatus

B.1 Added

L1 lamp Cutler-Hammer Type GL - App Fig. 1

D. Description of Changes

D.1 Added operation at 110-, 150-, 300-, 600-, and 1200-BAUD with 10- or 11-bit.

D.2 Changed the method of generating local copy.

D.3 Local copy must be provided for at the remote end. In remote operation, the character received from the TTY is no longer echoed back to the far end.

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