

CIRCUIT DESCRIPTION

CD-1C907-01
ISSUE 2A
APPENDIX 3D
DWG ISSUE 5D
DISTN CODE 1N98

11

COMMON SYSTEMS

SYSTEM STATUS PANEL CONTROLLER
CIRCUIT

CHANGES

D. Description of Changes

D.1 Removed unused 947A connectors from equipment locations
4 to 12 on J1C055A-1, as per sheets 2 through 5.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 5515-TKS-LEG

Printed in U.S.A.

Page 1
1 Page

CIRCUIT DESCRIPTION

CD-1C907-01
ISSUE 2A
APPENDIX 2A
DWG ISSUE 4A
DISTN CODE 7N98

COMMON SYSTEMS

SYSTEM STATUS PANEL CONTROLLER
CIRCUIT

CHANGES

D. Description of Changes

- D.1 Inhibited software access to the lock bit while it is being set by the E2A telemetry unit.
- D.2 Prevented setting of the force bit when both select bits are set erroneously by the E2A telemetry unit.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 5435-TKS-LEG

COMMON SYSTEMS

SYSTEM STATUS PANEL CONTROLLER
CIRCUIT

CHANGES

D. Description of Changes

D.1 The controller now inhibits the output signal to the system status panel (SSP) system normal lamp driver when either the panel time-out bit (flip-flop) or critical alarm (audible) bit is set. Previously, only the panel time-out bit inhibited the system normal lamp output.

D.2 A circuit power indicator lead at an SSPC CTF is provided for plug-in connection to an E2A telemetry unit.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 5344-DJM-LAW

COMMON SYSTEMS
SYSTEM STATUS PANEL CONTROLLER
CIRCUIT

TABLE OF CONTENTS	PAGE
<u>SECTION I - GENERAL DESCRIPTION.</u> . . .	1
1. <u>PURPOSE OF CIRCUIT</u>	1
<u>SECTION II - DETAILED DESCRIPTION.</u> . .	1
1. <u>GENERAL.</u>	1
LOGIC LEVELS	2
LEAD MNEMONICS	2
KEY MEMORY FLIP-FLOP	2
I/O GATING CONTROL AND DISPLAY REGISTERS (FS 1)	2
FORCE CU (FS 2)	3
FORCE CU (3A CC-0)	4
SCC ACCESS TO FORCE CU (SYC) . . .	4
SYSTEM INITIALIZATION (FS 3) . . .	5
ALARM CONTROL, PANEL TIMEOUT AND TIMING GENERATOR (FS 4)	5
PANEL TIMEOUT AND TIMING GENERATOR	6
RELAY DRIVER (FS 5)	6
TELEMETRY INTERFACE (FS 6)	6
MISCELLANEOUS FUNCTIONS (FS 7) . .	6
ALTERNATE BUS.	6
DISREMAC FLIP-FLOP	6
TTYINIT.	6
TESTEXEC	7
EMGLNTRF	7
POWER (FS 7)	7

TABLE OF CONTENTS	PAGE
<u>SECTION III - REFERENCE DATA</u>	7
1. <u>WORKING LIMITS</u>	7
2. <u>FUNCTIONAL DESIGNATIONS.</u>	7
3. <u>CONNECTING CIRCUITS.</u>	7
4. <u>MANUFACTURING TESTING REQUIREMENTS</u>	7
<u>SECTION IV - REASONS FOR REISSUE</u> . . .	7

SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The system status panel controller (SSPC) provides the electronic interlock and control logic and display buffers necessary for the operation of the system status panel (SSP). It also provides input/output (I/O) circuits for communicating between a 3A central control (3A CC) and the SSP, and pulse driver circuits for the system initialization function (3A CC MRF) and force or lock function appearing on the SSP. In addition, this unit contains buffering circuitry which is connected between the SSP and the E2A telemetry unit. This allows a switching control center (SCC) to monitor the SSP and to operate selected emergency manual control functions appearing at the SSP.

SECTION II - DETAILED DESCRIPTION

1. GENERAL

1.01 The system status panel controller (SSPC) circuit is comprised of flip-flop memory elements (CPS FA1100) controlled by serial data message between the 3A CCs and SSPC, and/or mechanical contact closures initiated by SSP switches, and/or E2A telemetry mercury contact closure initiated via an SCC. When required, electronic interlocks are provided to prevent possible race conditions or multiple function selection.

LOGIC LEVELS

1.02 Generally a logic zero is less than +0.4VDC and a logic one is greater than +0.7VDC, hereafter referred to as zero or one, respectively. Due to the interface requirements with the SSP, some logic one levels may be greater than +1.5VDC but less than +2VDC while the interface connections to the E2A could have logic ones equalling +3VDC.

LEAD MNEMONICS

1.03 A lead mnemonic will generally end in a zero or one designating the active state of the signal in question. EG signal DB00 represents data bus bit 0 (DB0) which is active zero. Therefore, DB00 represents a data one when the signal is zero active. Lead mnemonics preceded by the letters IC refer to internal connections within an FS.

KEY MEMORY FLIP-FLOP

1.04 The FA1100 circuit packs contain 24 flip-flops that are used primarily as memory devices reflecting the state of an SSP key or controlling an SSP status LED or lamp. The 24 flip-flops are partitioned into three data groups (DG0, DG1, and DG2) with eight flip-flops per data group. A common write-read 8-bit data bus services all data groups in the SSPC and provides the only control for DG1 and DG2 appearing on an FA1100 circuit pack. Data group DG0 is writeable in most cases and in all cases DG0 is readable via the data bus and is also controlled via inputs KEYXI00, KEYXI10, and INHX1. The DG0 flip-flops have certain attributes which enable them to respond as toggle flip-flops that respond to the first toggle only or to repetitive toggles depending on the status of input KEYXI00. Since this configuration is used repeatedly in the SSPC, the reader is directed to FA1100 CD Section II for details. Information Note 306 shows a DG0 key memory flip-flop with typical connections from the E2A telemetry and connections to an SSP lamp driver or LED. Notice that an open circuit from the SSPC to SSP will cause the related lamp/LED to light. Since the LED circuits are shunt controlled, the total current drain for the LED circuits is almost constant. The same output that controls the SSP LED/lamp driver circuits also may control the related E2A telemetry interface circuit (FA1103) with the pull-up voltage supplied to the FA1103 inputs via the SSP LED or lamp driver circuits (+24VDC source).

* X = 0-5
Y = 0-2

I/O GATING CONTROL AND DISPLAY REGISTERS (FS 1)

1.05 The SSPC is accessed by the 3A CC via a serial 21-bit data message. The message is transmitted as a transformer-coupled bipolar pulse stream by way of the coax leads RCV(N)01 and RCV(N)11. Each bipolar pulse is decoded into either a data one or zero (net IDAT0) and the bipolar pulse period is used to form a shift pulse (CLK0) for the I/O shift register (FA1101). Sequence chart 1 (SC 1) shows portions of a typical (ideal) bipolar pulse data message. A positive lobe prior to the negative lobe indicates a data one. Data (IDAT0) is determined by the second lobe while the I/O shift pulse (CLK0) encompasses both pulse lobes.

1.06 Table A shows the message format required for I/O communications. The expected start code is 011 (bits 2, 1, and 0). Failure to receive this start code, or receipt of bad parity will cause a maintenance start code message (101) with the data bits equal to zeros to be immediately transmitted back to the sending 3A CC only.

1.07 The OP code decoder on FA1101 determines what type of operation is in progress. Bit 3 equaling 1 and bit 4 equaling 0 (net OPCD0) are used as a write-read operation with all other combinations providing a read only function. The 3/6 address bits are decoded on FA1101 and the outputs ADDXY0* determine which data group on a specific FA1100 is selected. The PL is the parity bit for bits 3 through 11 and PH is the parity bit for bits 13 through 20. Odd parity is required in both bits to indicate a good message. The data bits 13 through 20 correspond to data bits 0 through 7 on a selected FA1100 data group.

1.08 During a message reception the FA1101 is in control state S0. When the shift register bit STA0 becomes a data one, the control logic recognizes this as a complete message received. Note that the 3A CC continues to transmit data zeros after the message is received, until the 3A CC I/O circuit receives a return message or a software timeout occurs. This provides the necessary timing required for the gating functions and return I/O message. At the end of the CLK0 shift pulse (150 ns later) the control state advances to S1. During the 150-ns interval when the last data bit was shifted in until the control state advances to S1, the entire message is being checked for parity via a parity tree on FA1102. The start code is checked and added on FA1102 with the parity results. A correct format message will result in net STPK0 being a zero before the control state advances to S1. If the message is good, S1 becomes a dummy state and the next CLK0 leading edge

TABLE A
MESSAGE FORMAT

PH	DATA BITS											PL	3/6 ADDRESS CODE						OP CODE		START CODE		
21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		

will advance the control state to S2. At S2 the decoded OP code and address code are made available to the appropriate backplane net. The data appears on nets DB00 through DB70. The selected OP code output lead will remain active through control state S3 and the address select output remains active through control state S5. The data outputs from the shift register to the selected FA1100 data group are active during control states S2 and S3. If a write-read OP code is present, the data from the selected FA1100 data group is blocked from the data bus and the contents of the FA1101 shift register data group are written into the selected data group. At S4 when the write-read OP code output (OPCD0) disappears, the data currently in the selected data group appears on the common data bus (DB00 through DB70) and is gated to the shift register data bits. During S4 and S5, the parity circuit is computing parity for the data in the shift register data bits. At S5 the transmit enable lead (TEN0) on the pulse encoder circuit on FA1102 becomes active. At S6 the shift signal inhibit is removed so that the next positive transition of CLK0 will shift the first information bit (start code bit C) to the pulse encoder data out (DAT0) flip-flop. When the first shift occurs, the PH bit is fed a dummy data one, which occurs only during S6 and is done to insure that a premature all zeros indication of shift register data does not occur. A premature all zeros indication would advance the control state to S0 and thus inhibit sending a complete 21-bit message to the 3A CC. The first pulse is transmitted to the sending 3A CC only during the next zero active state of CLK0. The FA1102 utilizes the incoming bipolar pulses to generate the appropriate message corresponding to the state of the FA1102 DAT0 flip-flop.

1.09 As previously indicated the shift register looks for all zero data as a requirement to advance from the send state to the receive state. When this occurs several bipolar pulses may still be received, but since they are data zeros the shift register remains cleared. The transmit enable signal is removed when in the receive state, but no attempt is made to insure blockage of pulses after the last meaningful data bit is transmitted. The 3A CC I/O is capable of blocking further pulses when it has received a full 21-bit message. Approximately 250 ns after the

last bipolar pulse is received by the SSPC, the I/O sequence reset monopulser becomes active. This causes the control state to be jammed to the S0 state and the PH bit to be cleared. During a normal message send-receive routine this is an unnecessary function, but it reduces the number of wasted messages in case of a single pulse bit on the receive cables. The pulse decoding circuits on FA1102 are self protecting against transient pulses (see CD for FA1102).

1.10 The display register portion of FS 1 represents DG1 and DG2 on all FA1100 circuit packs plus any DG0 flip-flops used exclusively as an SSP lamp-LED, or E2A critical indicator memory flip-flop. The DG0 flip-flops appear individually as elements on FA1100, thus they appear as separate symbols on FS 1. When the bit is a data one the related KMR__1 net is a one, and if the net is connected to an SSP lamp driver or LED circuit, the net will cause the lamp or LED to light. The KMR__1 outputs are also usually connected to either an E2A telemetry interface gate (FA1102) or directly to an E2A input because some flip-flops are assigned as SCC critical indicators.

FORCE CU (FS 2)

1.11 The force CU function may be initiated at the SSP by either manually operating both the desired select key and then the force key, or by operating the lock key (software selects the active 3A CC). The force CU (SYC) function, when active, causes the selected 3A CC to be forced active and the other 3A CC to be marked unavailable. A transformer-coupled pulse is sent via coax cable every 27 ms from the SSPC to each 3A CC. The 3A CC selected to be active receives a positive pulse and the other 3A CC a negative pulse. Each pulse enters a rectifier circuit at the 3A CC and then sets the 3A CC system status (SS) register LON bit 8 for the selected active 3A CC or the LOF bit 9 of the other 3A CC. When the force active signal is removed, the rectifier circuit times out, and automatically clears both the LON and LOF bits in both 3A CCs. When the SSP lock key is operated, software control of the force active function is enabled. The correct "select" function is chosen and then "force" is set, plus a software operated flip-flop (LOCKP) which mirrors the lock flip-flop. The 3A CCs

receive the same signals as they did when the select and force switches were manually operated at the SSP. The SSP will also indicate that the corresponding select and force bits are active via their respective lamps. When in the LOCK mode of operation, depressing any of the force active switches on the SSP will stop the force action by clearing the LOCK, LOCKP, and FORCE flip-flops. If the active select switch is operated, then all force active bits are cleared and all related SSP lamps are extinguished. The normal method of retiring the lock mode of operation is to operate the SSP lock switch. The LOCKP flip-flop maintains the ability of software access to the select 0 and 1, FORCE, and LOCKP flip-flops. When software interrogation discovers that the LOCK flip-flop is cleared, it will send a message to clear first the FORCE then SELECT and then the LOCKP flip-flops. When the LOCKP flip-flop is cleared the software can no longer control the force CU function unless the LOCK flip-flop is set again.

FORCE CU (3A CC-0)

1.12 To force 3A CC-0/1 active (referred to as CU0/1 or SYC0/1), the desired SSP SELECT 0/1 switch and the FORCE switch are operated (see Note 3.7). The SSP force active switches SELECT 0 and 1, FORCE, and the SSP LOCK switches are nonlocking. Select 0/1 flip-flop (FF) input lead KR02(3)I00 becomes a one and KR02(3)I10 becomes a zero in this order. The select 0/1 flip-flop being set causes lead INSEL1 to be active and KR01INH1 to be inactive. The active INSEL1 signal is connected to the one active inhibit inputs of both select 0 and 1 flip-flops. This action is instantaneous (less than 100 ns) and thus prevents operation of both select flip-flops during a force CU operation. Net KR11INH1 is connected to the one active inhibit input of the force flip-flop. Since KR11INH1 is a zero, the force flip-flop may be set when the SSP force switch is operated. When this switch is operated, net KR11I00 becomes a one and then net KR10I10 is a zero, thus setting the force flip-flop. With both the select 0/1 and force flip-flops set, the "and" function of transformer driver gates FCU0(1)P0 and FCU1(0)N0 is satisfied whenever a 27 ms timing pulse occurs. As previously stated, this causes a positive pulse to be transmitted via the coax to 3A CC-0/1 and a negative pulse to 3A CC-1/0. When the force CU is retired, operating any SSP force active switch (SELECT 0 and 1, or FORCE) will cause net KR10I10 to be a zero, thus resetting the force flip-flop. If the SELECT 0/1 switch is operated, the select 0/1 flip-flop is also retired via the zero active net KR02(3)I10 (KR02(3)I00 is a one). Information Note 307 details the switch connections to the SELECT 0/1 and force flip-flops. The force flip-flop inputs are

obtained via a network arrangement of transfer contacts with the select 0 and 1, and force switches. The switches are arranged in such a way that only the force switch may set the force flip-flop. Whenever SELECT 0/1 is operated, the related break contact opens the ground path to net I1FOR1, prior to the corresponding make contact grounding net KR10I10. The open circuit on net I1FOR1 is seen as a one by gate INFOR0 on FA1102, which forces gate ENFOR0 to a one. This action inhibits setting the force flip-flop.

1.13 The LOCK flip-flop when set, enables software access to flip-flops SELECT 0 and 1, FORCE, and LOCKP. Software access is normally inhibited by an inactive signal on net KMR01100 which is the "OR" of LOCK and LOCKP. To set the LOCK flip-flop from the SSP, the LOCK switch is operated. Net KR01I00 becomes a one and then nets KR01I10 and INHKR011 become zero, thus setting the LOCK flip-flop. The SSP LOCK switch is partitioned in a manner that to provide isolates the LOCK flip-flop inhibit set input (INH11) from the controlled toggle input (KR01I10). Note 307 shows a second make contact of the LOCK switch connected to input INH11 via buffer gates I1KOCK0 and INHLOCK1 on FA1102 (gate I0LOCK0 enables an active INSEL1 signal to inhibit setting the LOCK flip-flop). When the LOCK switch is operated, ground is provided via both make contacts through the FA1102 buffer gates to the LOCK flip-flops INH11 input, thus enabling it to be set. The SSP force active switches are able to clear the LOCK flip-flop via a buffered connection to net KR01I10 from net KR11I00 but are unable to set it because input INH11 is a one. When software interrogates the LOCK flip-flop and discovers it set, a message is sent to the SSPC that causes the LOCKP flip-flop to be set. When the LOCKP flip-flop is set it maintains the KMR01100 net at a zero until such time that the software clears the flip-flop. After software discovers the LOCK flip-flop is reset. The LOCKP flip-flop may also be reset only (INH01 is an open circuit one) by operating any FORCE active switch with the LOCKP flip-flop set, software activates first the appropriate select flip-flop, and then the FORCE flip-flop. The subsequent pulsing to the 3A CCs is the same as during a manually selected force action.

SCC ACCESS TO FORCE CU (SYC)

1.14 When an SCC attempts to force a CU, the only significant differences are that the KRI00 inputs to the flip-flops remain grounded and gate delay chains, internal to the FA1103 telemetry interface circuit are used. Since the E2A telemetry provides a nonbouncing mercury-wetted contact closure to ground, the flip-flops can be left in the repetitive toggle mode. The E2A gives one contact closure to user

provided ground, for each momentary operation of the SCC status panel switches. The SCC should see an immediate response since the output of the corresponding SSPC flip-flop controls the switch related lamp on the SCC status panel. To retire a function, the SCC is again momentarily operated and the E2A again provides a nonbouncing pulse to the selected lead. The gate delay chains employed by the SSPC provide the ability to respond functionally the same to an SCC or SSP, eg, operating an active-select switch will retire both the force and select functions.

SYSTEM INITIALIZATION (FS 3)

1.15 The system initialization function provides a single transformer-coupled pulse to each 3A CC for each system initialization sequence executed at the SSP. The SSP system initialization procedure is as follows.

- (a) Momentarily operate the SSP ENABLE switch.
- (b) Momentarily operate one, all, or none of the initialization level switches at the SSP. This includes STABLE CALLS, MEMORY RELOAD, RECENT CHANGE PAST OFFICE DATA or the BACKDT OFFICE DATA SWITCHES.
- (c) Momentarily operate the SSP INIT EXECUTE switch.

1.16 The enable flip-flop, when reset, inhibits setting the STBLCALL, MEMRLOAD, RECENTCHG, BACKDT, or the INITEEXEC flip-flop. The INITEEXEC flip-flop when set (enable FF is already set) will generate a single MRF pulse to each 3A CC. The length of the MRF pulse is determined by gate delays on FA1102 and the reset time of the enable flip-flop. The enable flip-flop is automatically reset by hardware circuits as part of the MRF pulse generation scheme. The 3A CC software, upon recognizing a MRF, will scan the SSPC to determine if it was the originator of the MRF, and if so, what initialization level flip-flops, if any, are set. The INITEEXEC flip-flop is reset by software control at some short interval of time after the 3A CC receives the MRF and the initialization level flip-flops may or may not be reset by software control depending upon system requirements. Prior to operating the SSP INITEEXECUTE switch, the initialization routine may be aborted (or changed) by momentarily operating the switches related to the function to be aborted, retired, or selected.

1.17 The KMR000 output of the enable flip-flop is input directly to the INH1 input of key memory flip-flops (STBLCALL, MEMRLOAD, RECENTCHG, and BACKDT) and "Ored" with the output of the INITEEXEC flip-flop (KMR170) on FA1102, whose output, net TENSTEX0, is input to the INH71 input of

the INITEEXEC flip-flop. When net KMR000 is active, the initialization level and the INITEEXEC flip-flops may be set. The JRing of the INITEEXEC and enable flip-flop outputs relates to timing considerations pertaining to SCC control. If the INITEEXEC flip-flop INH71 input is enabled while a toggle pulse is still present after setting the flip-flop, then the same pulse will cause the flip-flop to reset. Since the enable flip-flop is reset approximately 50 ns after the INITEEXEC flip-flop is set, the enable signal to INH71 would be removed while the toggle pulse was present. Now, however, the INITEEXEC output is active and the "Ored" output of INITEEXEC and ENABLE remains active after the enable flip-flop is set. The enable flip-flop is reset via a zero active pulse from FA1102. The DREN60 gate, which is outputted to net KR00110, is a delayed "AND" of the active enable and INITEEXEC flip-flops. After the enable flip-flop is reset, the "AND" condition no longer exists at FA1102 and KR00110 become a one, and thus a complete toggle pulse has been inputted to the enable toggle input.

ALARM CONTROL, PANEL TIMEOUT AND TIMING GENERATOR (FS 4)

1.18 This FS consists of a 27-ms timing generator that provides clocking for the SSPC time out counter (symbol 2), and the force CU transformer-pulsing circuit. It also contains the panel time out flip-flop (PNTIMOUT) and other flip-flops used for alarm control. With the exception of ALARMREL, all flip-flops appearing on this FS control a relay in the SSPR circuit. The flip-flops and the related SSPR relays are as follows:

<u>FLIP-FLOP</u>	<u>RELAY</u>
PNTIMOUT	CRIT
CRITICAL	CRIT
INHBLDLM	BLDG-ALM
ALRMXFER	ALM-XFER
MAJOR	MAJOR
MINOR	MINOR
MJPOWER	MJ-PWR
MNPOWER	MN-PWR
ALARMCKT	ALM-BATT

1.19 Generally the ALARMREL flip-flop is set when any system alarm occurs that requires the alarm release lamp (switch) on the SSP to light. When the craftsperson operates the alarm release switch, the ALARMREL flip-flop will be reset and when scanned will provide an indication that a request to release alarms has been issued. The specific type of alarm and system requirements determine if the ALARMREL flip-flop remains cleared (and thus the alarm release lamp extinguished). Also, the SSP alarm release switch cannot set the ALARMREL flip-flop (input INH41 is open circuited).

1.20 Two SSP alarm control keys that can set the related SSPC flip-flops are ALARM TRFR (ALRMXFER) and INHIBIT BUILDING ALARMS (INHBDALM). These are both straightforward implementations of a break/make switch input to the FA1100 controlled toggle flip-flop with the INH1 input grounded. Four of the flip-flops control corresponding SSP lamp driver circuits (PNTIMOUT, INHBDALM, ALRMXFER, and ALARMREL) and can also be monitored by an SCC. The SCC (via E2A mercury wetted contact closure) may also exercise control over the INHBDALM, ALRMXFER, and ALARMREL flip-flops.

PANEL TIMEOUT AND TIMING GENERATOR

1.21 The 27-ms timing generator is comprised of discrete components located on FC208. The timing generator output (net 27MSTIM0) is input to FA1102 input TIM01. On FA1102 a pulse-shaping circuit comprised of a gate-delay chain provides the necessary pulse width for control of the force CU transformer-driver gates. A binary counter comprised of seven GDFs configured as toggle flip-flops provides an output when the flip-flop reaches 120 (approximately 3.3 seconds). If the count reaches 120, the PNTIMOUT flip-flop is set (net KR21I10 is active) and the counter output signal blocks further advance the upper portion of the counter. The counter remains in this mode until the 3A CC software causes a message to be sent to the SSPC that will reset the counter (net ADD520). The normal system operating mode is to send messages frequently enough to prevent the counter from reaching 120. If the PNTIMOUT flip-flop is set it will cause the SSPR CRIT relay to operate (net KMR270) the SSP panel time out lamp to light (net KMR2011), and the SSP system normal lamp to be extinguished. This is an indication of a possible loss of service. When the system has recovered, the PNTIMOUT flip-flop will be reset by a software generated message to the SSPC. Depending on the system this may require operating the SSP alarm release switch or a TTY request.

RELAY DRIVER (FS 5)

1.22 The relay driver is comprised of FC209 only. This circuit pack has three double inverter and 20 inverter lamp/relay driver circuits. When used as relay driver circuits, the single inverter stages are connected externally to form a double inverter. A zero active input from a signal source is double inverted and the output to the associated relay is grounded, thus causing the relay to operate. A one active input will cause the output to turn off and the associated relay will release.

TELEMETRY INTERFACE (FS 6)

1.23 The telemetry interface is comprised of three FA1103 circuit packs that buffer the E2A telemetry inputs from the SSPC flip-flop outputs. Each buffer circuit is a double inverter or an "OR" output of two double inverted inputs (see FA1103). The pullup voltage for the inputs is usually derived from the lamp driver or LED circuit on the SSP. The FA1103 also buffers and provides gate delay chains for E2A mercury-wetted contact inputs to the SSPC. The E2A provides zero active signals to the SSPC and the SSPC provides one active signals to the E2A.

MISCELLANEOUS FUNCTIONS (FS 7)

1.24 This FS is comprised of several miscellaneous flip-flops. Three respond as controlled toggle flip-flops (TTYINIT, TESTEXEC, and EMGLNTRF) while the remaining two flip-flops respond differently.

ALTERNATE BUS

1.25 The ALTBUS flip-flop monitors the state of the SSPR and maintenance frame power circuit alternate power bus relays. These relays are all usually held operated and one make contact from each one is series connected with the others to apply ground to net KR14I10. When this net is grounded any attempt to write the associated ALTBUS flip-flop by software will result in resetting the flip-flop. If an alternate power bus switch should occur, net KR14I10 is ungrounded and a subsequent software message will cause the ALTBUS flip-flop to be set. The return message to the 3A CC will provide the information for software interrogation, and the ALTBUS lamp on the SSP will light. The alternate bus function may also be manually initiated for testing by depressing the SSP alternate bus switch.

Note: When an alternate power bus switch occurs, the SSPC circuits are initialized as if a circuit power off/on sequence had occurred. This flip-flop is not controllable by the SCC.

DISREMAC FLIP-FLOP

1.26 The DISREMAC flip-flop operates similarly to the ALTBUS flip-flop except that the SSP disable remote access switch in series with a TTY stunt box relay contact normally provide ground to net KR15I10. Removing ground from net KR15I10 is sufficient to block the E2A functions to the SSPC. The flip-flop only controls the SSPC lamp and informs software of the occurrence.

TTYINIT

1.27 The TTYINIT flip-flop is set by momentarily operating the SSP TTYINIT

switch. After software scans the flip-flop it sends a message to reset the flip-flop.

TESTEXEC

1.28 The TESTEXEC flip-flop is controlled by the PF relay in the SSPR instead of directly from the SSP test execute switch. This allows many switches placed on frames throughout the central office to operate this flip-flop through the buffering action of the PF relay. As with TTY INIT this function is scanned and subsequently controlled via software.

EMGLNTRF

1.29 The EMGLNTRF flip-flop is not controllable by software I/O message. It requires a manually initiated operation of the SSP emergency line transfer (EMER LINE TRFR) switch. When this occurs the corresponding SSPR relay operates, and if implemented, will cause selected telephone lines to be switched to an alternate system.

1.30 The latter three flip-flops are also controllable by E2A mercury-wetted relay contacts connected to nets KR04I10, KR05I10, and KR30I10, respectively.

POWER FS 7

1.31 This FS contains the +0.3 volt reference and filter circuits and +12VDC reference circuits required for operation with A8 +3VDC power converters for 1A TTL logic circuits.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 None.

2. FUNCTIONAL DESIGNATIONS

2.01 Message Registers

<u>Designation</u>	<u>Meaning</u>
D G (0-2)	Data group 0 through 2 appearing on each FA1100 circuit pack. Each group contains eight memory flip-flops.
KMR (0-1)	Key/Lamp memory register circuit packs 0 through 3 (FA1100 type CPS).

3. FUNCTIONS

3.01 Provides flip-flop memory elements that control light indicators appearing on the SSP.

3.02 Provides key memory flip-flops that reflect the status of the SSP-related key operations. These flip-flops control the corresponding indicators on the SSP.

3.03 Provides I/O circuits that enable a 3A CC to monitor and, in selected cases, control the flip-flop memory elements contained therein.

3.04 Provides electronic interlocks that require certain emergency manual control key functions on the SSP to be sequentially operated.

3.05 Provides pulse driver circuits for the SSP force active and lock functions, and the 3A CC MRF.

3.06 Provides relay driver circuits for the system status panel relay (SSPR) unit.

3.07 Provides buffer circuits to the E2A telemetry unit for communicating between the SSP, SSPC, and the SCC.

3.08 Provides a self-contained alarm circuit (panel timeout circuits) that generates a local critical alarm signal and a critical alarm signal to the SCC, if not reset via an I/O message from a 3A CC.

4. CONNECTING CIRCUITS

4.01 When this circuit is listed on a keysheet, the connecting information thereon is to be followed.

- (a) System Status Panel (SSP) - SD-1C906-01.
- (b) System Status Panel Relay Unit (SSPR) - SD-1C908-01.
- (c) Maintenance Frame Power Unit - SD-1C909-01.
- (d) Maintenance Frame Circuit - SD-1C912-01.
- (e) E2A Telemetry Unit - SD-2P021-01.

5. MANUFACTURING TESTING REQUIREMENTS

5.01 The manufacturing testing requirements are furnished in the X-78890 specification.

SECTION IV - REASONS FOR REISSUE

D. Descriptions of Changes

D.1 Provided a hardware Ored function, "SYSEM1" (system emergency) for switching control center (SCC) use as a critical indicator. It is comprised of SSPC functions "panel timeout" and "service loss."

D.2 Replaced zero-active signals with one-active signals to the SCC CO E2A telemetry unit. It should be noted that all nets to the E2A previously designated zero active are now designated one active by the last numeric in the name. As an example, net KMR0010 is now KMR00101.

D.3 Added power-up sequence lead STMV0 to start the panel timeout counter, 27-MS multivibrator.

D.4 Provided the capability of connecting a TTY stunt box relay contact (break) in series with the disable remote access function by means of a wiring option shown on SD-1C912-01.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 5344-JPL-LAW