CIRCUIT DESCRIPTION

CD-1C913-01
ISSUE 2A
APPENDIX 5A
DWG ISSUE 7A
DISTN CODE 1N98

10

COMMON SYSTEMS
ELECTRONIC REMREED PULSER
CIRCUIT

CHANGES

B. Changes in Apparatus

B.1 Removed

CR11 diode 458A - CPS 2

Replaced By

C20 capacitor KS-19774, L7, 1000 pf - CPS 2

B.2 Added

R78 resistor KS-20616, L1A, 187 ohms - CPS 2

D. Description of Changes

D.1 Replaced diode CR11 in the output and inhibit circuit (ED-4C082-31) by capacitor C20. This change in the overvoltage protection circuit reduces its susceptibility to false turn-on by noise pulses.

D.2 Added R78 in series with zener diode CR17 to prevent voltage spikes from occurring when the output transformer field collapses at the trailing edge of the prerelease pulse. Without this change, noise spikes can have sufficient amplitude to induce voltage transients into the mate controller and cause it to lock up.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 5329-RLB-JSC

CIRCUIT DESCRIPTION

CD-1C913-01
ISSUE 2A
APPENDIX 4A
DWG ISSUE 6A
DISTN CODE 1N98

COMMON

ELECTRONIC REMREED PULSER

CIRCUIT

CHANGES

B. Changes in Apparatus

B.1 Added

R74 Resistor, KS-19150 L1, 10 kΩ - App Fig. 1
R75 Resistor, KS-19150 L1, 10 kΩ - App Fig. 2

D. Description of Changes

D.1 Added a 10 kΩ resistor across each output transformer secondary winding to prevent ringing on the transformer output lead during diagnostic testing.

BELL TELEPHONE LABORATOIRES, INCORPORATED

DEPT 5333-RLB-GH

COMMON SYSTEMS
ELECTRONIC REMREED PULSER
CIRCUIT

CHANGES

B. Changes in Apparatus

B.1 Removed	Replaced by
1 - R72, R73 Resistors, KS-20200,L1 1 MEGOHM - App Fig. 1	1 - R72, R73 Resistors, KS-16645,L1 39 KOHM - App Fig. 1

D. Description of Changes

D.1 Changed the value of resistors R72 and R73.

D.2 Changed the transformer cover.

D.3 Changed the AT&TCo rating from Provisional to Standard

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 5362-EBJ-GH

CIRCUIT DESCRIPTION

CD-1C913-01
ISSUE 2A
APPENDIX 2AR
DWG ISSUE 4AR
DISTN CODE 7N98

COMMON SYSTEMS

ELECTRONIC REMREED PULSER CIRCUIT

CHANGES

B. Changes in Apparatus

B.1 Added

R74 Resistor 257A, 10 KOHMs - CPS 2

R75 Resistor 257A, 10 KOHMs - CPS 2

B.2

Removed	Replaced By
Q(2,3,4,5,10,11,12,13) Transistors 66J - CPS 1	Q(2,3,4,5,10,11,12,13) Transistors 66AE - CPS 1
Q(6,14,16,17,18,19) Transistors 66J - CPS 2	Q(6,14,16,17,18,19) Transistors 66AE - CPS 2
Q8 Transistor 20S - CPS 2	Q8 Transistor KS-21445 L1 - CPS 2
Q23, Q24 Transistors 59A - CPS 2	Q23, Q24 Transistors 85A - CPS 2
R8 Resistor 257A, 2370 ohms - CPS 1	R8 Resistor 257A, 2870 ohms - CPS 1
R17 Resistor 257A, 1.5 KOHMs - CPS 2	R17 Resistor 257A, 511 ohms - CPS 2

D. Description of Changes

D.1 Changed all 66J transistors to 66AE transistors to prevent high voltage breakdown.

D.2 Changed Q8 transistor from 20S to KS-21445 L1 to prevent transistor failure resulting from a second breakdown.

D.3 Added 10-KOHM resistors R74 and R75 to provide base emitter shunt.

D.4 Changed 59A PNPN transistors Q23 and Q24 to new version.

D.5 Changed resistor R8 from 2370 ohms to 2870 ohms to expand the adjustment range of output current amplitude.

D.6 Changed resistor R17 from 1.5 KOHMs to 511 ohms. This prevents the power transistors Q20, 21, and 22 from turning on as a result of collector-base leakage.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 5341-GMC-EN

CIRCUIT DESCRIPTION

CD-1C913-01
ISSUE 2A
APPENDIX 1A
DWG ISSUE 3A
DISTN CODE 7N98

COMMON SYSTEMS
ELECTRONIC REMREED PULSER
CIRCUIT

CHANGES

D. Description of Changes

D.1 Changed resistors R60 and R59 from 500 ohms to 2000 ohms.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 5341-GMC-BJY

COMMON SYSTEMS

ELECTRONIC REMREED PULSER CIRCUIT

TABLE OF CONTENTS

SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The primary function of this circuit is to provide a long-duration high-amplitude current pulse to operate and release selected members of a network of remreed switches in No. 2 and No. 3 ESS.

2. GENERAL DESCRIPTION OF OPERATION

2.01 This circuit was designed to be used in a No. 2 ESS or No. 3 ESS remreed network to operate or release the remreed network switches. The pulser is used with -48 V, +18 VP, and ground (No. 3 ESS) or with -48 V, +24 V, +18 VR, and ground (No. 2 ESS).

2.02 The pulser is comprised of three sections, two waveforming sections and a power output section. The operate waveforming section forms the waveshape which provides an operate pulse to the remreed switches. The prerelease wave forming section provides a waveform which ensures that the switch is released prior to sending an operate pulse. The power output section amplifies the prerelease and the operate waveforms to a level which is compatible with the remreed switch requirements.

2.03 There are two input leads, the OP and PRP leads, which control the output of the pulser. A signal on the OP lead activates the pulser to produce an operate pulse which has a 4.2-ampere peak amplitude and a duration of 2.5 milliseconds at the quarter amplitude points, and a duration of 4 milliseconds or more at the base level.

2.04 A pulse on the PRP leads produces a prerelease pulse which is a half sine wave of 4.2 amperes peak and 1 millisecond at the base level.

2.05 In the output stage, leads are brought out in sufficient numbers so that a variety of design configurations may be obtained.

SECTION II - DETAILED DESCRIPTION

1. NO. 2 ESS APPLICATION

1.01 In No. 2 ESS, +24 V and -48 V are used in conjunction with the pulser. The +24 V supply is connected to terminal 1 of transformer T2. The pulser provides a current source to the series connection of the primary windings of transformers T1 and T2, producing a 4.2-ampere pulse on the secondary of both T1 and T2. Two transformers are needed since the voltage generated at the secondary of each transformer individually is approximately 120 volts and the use of one single transformer would have a secondary voltage

which would exceed the breakdown voltage of the PNPNs that are used in the No. 2 ESS switching network.

1.02 Using two pulsing transformer necessitates the use of two bias core detectors, transformers T3 and T4, to detect that a 3.8-ampere or greater pulse is supplied to both portions of the No. 2 ESS network. Both bias core detector transformers are tied together through CR30 and CR31 to form an AND circuit. This gives the network controller an indication that both network paths have received 4.2-ampere pulses.

1.03 The output pulse is either provided to two network fabric paths, two dummy load resistors (R61 and R62), or a combination of one network fabric path and one dummy load resistor. The network controller determines and controls the appropriate path to be pulsed. If it is desired to pulse through one or both of the dummy load resistors, the switching network controller will provide current and appropriate grounds to turn on either transistor Q23 or transistor Q24 or both.

1.04 If an error occurs, it is possible that there will be no path established for the 4.2-ampere pulse. If that situation arises, a very high voltage will appear on terminal 3 of the transformer which does not have a path load. The high voltage occurring on T1, T2, or both, will be directed to the protection circuit via the SEN A or SEN B lead or both. The high voltage will trigger a monostable which in turn will shut off the pulsing current supplied to the base lead of transistors Q20, Q21, and Q22. This will shut off the current source and prevent any damage from being done to the power output transistors or to the network path select PNPNs. The monostable output also passes through transformer T5 whose output triggers the dummy load access SCRs (Q23 and Q24) directing the open circuit voltage through the dummy loads. The pulsing current supplied to the base lead of transistors Q20, Q21, and Q22 also can be shut off by applying -48 volts to the INH lead. This is used in No. 2 ESS when some diagnostic orders are run where the pulser is not to produce an output current pulse.

1.05 When an output pulse occurs, an indication is also given to the network controller when the current level in the secondary has reached approximately 1 ampere. This signal is used within the remreed network controllers. The 1ALVL (1-ampere level) signal is generated by Q19 when the voltage across resistor R53 has reached a level of approximately 0.8 volts.

1.06 The secondary of transformers T1 and T2 are connected through diodes CR18 and CR20 to +24 V via the T2SC lead when the pulser is used in the No. 2 ESS application. This is used to prevent triggering of network PNPNs due to the voltage that appears on the secondary of the pulser transformer.

2. NO. 3 ESS APPLICATION

2.01 The No. 3 ESS application requires a lower power output than the No. 2 ESS application. Therefore, in the No. 3 ESS application, -48 V and ground are used and only output transformer T1 is used.

2.02 Bias core detector T4 is used to produce an output signal on the POKT2 lead when the pulse into the No. 3 ESS network exceeds the 3.8-ampere level. Bias core detector T3 is used to produce an output signal on POKT1 when a pulse, directed to the dummy load resistor (R61), exceeds 3.8 amperes.

2.03 The output pulse may be either connected to the switching network or connected through the dummy load resistor R61, depending on the current applied by the No. 3 ESS switching network controllers to the gates of Q23 or Q24.

2.04 If there is no load applied to transformer T1, the high voltage that occurs at the SEN A lead will be used to shut off the pulser in a manner similar to that which occurs when the pulser is used in the No. 2 ESS application, except that only Q23 is gated and, therefore, only dummy load resistor R61 is accessed.

2.05 A 1-ampere signal indication is given to the No. 3 ESS network in a manner identical to that used for giving 1-ampere signal to the No. 2 ESS network.

3. WAVEFORMING CIRCUIT DESCRIPTION

3.01 At the time of an operate pulse, the OP lead will go from either +3 or +5 V to ground for at lease 2 milliseconds. At this time, the level shifter comprised of Q1 and Q2 will convert the negative-going signal on the base of Q1 to a negative-going signal on the collector of Q2, referenced to -48 V.

3.02 Integrated circuit IC1 is a 24-volt regulator circuit, providing a voltage at terminal 2 that is 24 volts more positive than the -48 V lead into the pulser. The voltage is used to charge up capacitor C2 and to provide a constant current to resistors R8 and R60, through CR35 to inductor L1, and transistor Q5 which is normally on.

3.03 When the collector of transistor Q2 goes low, transistor Q5 turns off. At the same time, transistor Q4 turns off, turning on transistor Q3. The current that had been flowing through diode CR35,

resistors R8 and P60, inductor L1, and transistor Q5, now flows instead into capacitor C3, producing a positive-going half sine wave voltage on the base of transistor Q6. The half sine wave produced on the base of Q6 is coupled to the base of Q7 and to resistor R15.

3.04 When the current through L1 decreases to zero, the voltage on capacitor C3 is at its maximum. The current then reverses and flows back through R70 and Q3, producing an overdamped current waveform. Capacitor C17 is charged by the voltage drop across R70, producing a higher frequency dampened sinusoid that is superimposed on the basic overdamped waveform. The resulting voltage across capacitor C3 produces the output current shown in Fig. 1 of sheet H3 of the SD. The effect of the overdamped circuitry is to lengthen the trailing edge of the pulse, and extend the waveform to a length of at least 4 milliseconds. The overall waveform is seen at the emitter of Q8 which connects to the power output circuit.

3.05 The prerelease pulse is provided in a manner similar to that of the operate pulse except that the prerelease pulse has no pulse stretching network similar to C17, R70, and CR35 to lengthen the trailing edge of the prerelease pulse. The pulse is terminated when the polarity of the voltage across C7 reverses, causing CR6 to be forward biased. The prerelease pulse is 1-millisecond wide at the base with L2 and C7 used to determine this narrower prerelease pulse.

3.06 The power output circuit is comprised of transistors Q20, Q21, and Q22, and functions as a current source. The voltage on the emitter of Q8 from either the prerelease or the operate pulse waveforming section is connected to transistors Q20, Q21, and Q22. The emitter resistors of these three transistors convert the voltage on the emitter of Q8 into an essentially constant current with three separate resistors insuring that equal current flows through each of the output transistors. The current flowing through the three transistors is connected in common to the output transformers T1 and T2.

3.07 The output transformers have a turn ratio of 5 to 1. Thus a 4.2-ampere secondary current requires a primary current of approximately 23 amperes, allowing for loses in the transformers. The heavy 23-ampere primary transformer current requires the use of multiple connector pins to minimize voltage drop through the connector. In addition, the wires leading from the switching network to the pulse connector should be adequately sized to give minimum voltage drop through the wires.

3.08 The diode CR17, is used to control the recovery time of transformer T1 for No. 3 ESS and transformers T1 and T2 for No. 2 ESS. Diode CR17 is a zener diode which breaks down only when the voltage on the transformer primary exceeds 50 volts, allowing rapid transformer recovery. This time must be less than 2 milliseconds for use on No. 3 ESS.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 The +24 volts must be between 20.5 and 26.5 volts. The -48 V must be between -53.5 and -42.5 volts. The +18 VR must be between 17.6 and 18.4 volts.

2. FUNCTIONAL DESIGNATIONS

2.01 Leads

Designation	Meaning
BRT2BP	Bias resistor transformer 2 bypass
GR2BP	Gate transformer 2 bypass
GT1BPP	Bias resistor transformer 1 bypass
INH	Inhibit
OP	Operate
PGR	Concentrator open circuit bypass
PGRM	Concentrator bypass inhibit gate
POKC	Pulser OK common
POKG	Pulser OK ground
POKT2	Pulser OK transformer 2
POKT1	Pulser OK transformer 1
PRP	Prerelease
RKN	No. 3 positive out
T1N	Transformer 1 negative
T1BPN	Transformer bypass 1 negative
T1SC	Transformer 1 secondary clamp
T2BPN	Transformer 2 bypass negative

Designation	Meaning
T2N	Transformer 2 negative
T2P	Transformer 2 positive
T2SC	Transformer 2 secondary clamp
1ALVL	1-Ampere level

3. FUNCTIONS

3.01 Provides a high current pulse to operate and release remreed switches.

3.02 Provides a means of recognizing when a pulse of sufficient amplitude has occurred (3.8 amperes).

3.03 Provides a means of recognizing when the 4.2-ampere pulse has reached a level of 1 ampere.

3.04 Provides a means of connecting the 4.2-ampere pulse through internal dummy load resisitors to avoid pulsing into the remreed switching network.

3.05 Provides a means of protecting the pulser and connected circuits if a high impedance pulse path occurs.

4. CONNECTING CIRCUITS

4.01 When this circuit is listed on a keysheet the connecting information thereon should be followed.

(a) No. 2 ESS Remreed Switching Network - SD-2H211-01.

(b) No. 3 ESS Control Frame - SD-3H902-01.

5. MANUFACTURING TESTING REQUIREMENT

5.01 Manufacturing testing requirements are covered in X-79112.

6. TAKING EQUIPMENT OUT OF SERVICE

No. 2 ESS

6.01 Normally, two pulsers are associated with each network. Each pulser is required to operate with the entire switching network. Under trouble conditions, one of the pair of pulsers may be required to handle all the functions normally required of the two. The pulser in trouble may be removed from service, after central control has taken the required action of quarantining the circuitry associated with the pulser being removed. When the indicating light on the associated switching circuit shows that the controller and pulser have been quarantined, power can be removed manually and the pulser removed physically. The quarantine mode of operation must be maintained until an operative pulser has been installed and power manually restored. The central control may then remove the quarantine mode and restore normal operation.

No. 3 ESS

6.02 There are two pulsers associated with No. 3 ESS. Each is associated with a network controller. The on-line pulser performs all functions in the network while the second pulser is in standby. To take a pulser out of service, its associated network controller must be placed in the standby mode by the central processor and power removed manually. The pulser may then be physically removed. Operation can be restored by installing a working pulser, manually restoring power, and using the central processer to put the pulser and associated network controller back in normal operation.

SECTION IV - REASONS FOR REISSUE

D. Description of Changes

D.1 Provided complete CD information.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 5341-GMC-LEG