DATA SYSTEMS STATION DATA SET 202T TYPE 39A1 DATA MOUNTING AND 40B1 DATA MOUNTING

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SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 Data set 202T is intended for private-line service only. It provides asynchronous transmission and reception of medium-speed, binary, serial data using frequency-shift-keying modulation. The data set places no restrictions on codes used or the number of consecutive marks and spaces, and provides no timing.

1.02 Data set 202T can communicate over 2- or 4-wire private line facilities with another data set 202T or with data sets 202D or 202R. Data set 202T has an option for a reverse channel when used on a 2-wire facility. With reverse channel, it is compatible with data set 202D with reverse channel.

2. GENERAL DESCRIPTION OF OPERATION

2.01 Data set 202T provides transmission and reception of data at speeds up to 1400 b/s on basic 3002 private lines and 1800 b/s on C2 conditioned lines. Two- or 4-wire service is provided by option switches selected by the installer.

2.02 The basic data set without reverse channel consists of a single circuit pack. Two versions coded 202T-L1 and 202T-L1A are available. Data set 202T-L1, rated Mfr Disc., does not perform satisfactorily at 1800 b/s on all C2 conditioned lines when reverse channel is installed. Data set 202T-L1A with JY4 reverse channel does not have this restriction. Other features and improvements are offered on data set 202T-L1A (refer to Section II).

2.03 In 2-wire service, the data set can transmit or receive, but not both simultaneously without the reverse channel (half-duplex). With the reverse channel option installed, signaling at speeds up to 5 b/s is provided in the direction opposite to the primary channel. Data set 202T with reverse channel installed has a maximum bit rate for the primary channel of 1200 b/s on basic 3002 private lines. The local copy feature may be provided for either or both channels by installer-selected option switches. The data set terminates the 2-wire line with a 600-ohm impedance.

2.04 The reverse channel circuit consists of a single circuit pack that plugs into the data set circuit pack. Three versions, coded JY1, JY2, and JY4, are available. Code JY1, rated Mfr Disc., provides a dependent type of operation; the request-to-send circuit of the data set must be on to receive the reverse channel signal. The JY2 and JY4 circuits provide an independent type of operation similar to that provided by the reverse channel circuit of data set 202D. With independent operation, a reverse channel signal may be received regardless of the state of the request-to-send circuit. The JY1 and JY2 circuits may only be used with data set 202T-L1. Data set 202T-L1A requires the use of the JY4 reverse channel which may also be used on data set 202T-L1.

2.05 In 4-wire service, the data set can transmit and receive simultaneously and independently (full-duplex). The data set terminates each pair of the 4-wire line with a 600-ohm impedance.

2.06 The single circuit pack of data set 202T may be installed in the 39A1 or the 40B1 data mounting which holds 16 sets without reverse channel or eight sets with reverse channel. The data sets are powered by an ac power supply in the data mounting which connects to a customer-provided 105- to 129-volt, 60 ±3.0 Hz nonswitched source. The ac supply employs fuse protection against overload.

2.07 For single data set installations, the circuit pack mounts in a housing. Electrical power is supplied by an external transformer which mounts on the customer-provided 105- to 129-volt, 60 ±3.0 Hz nonswitched outlet. The transformer is protected internally against overload and conforms to the class 2 power transformer requirements of Underwriters Laboratories.

2.08 Electrical signals at the interface of the customer data terminal and data set 202T are in bipolar voltage form and conform to Electronics Industries Association (EIA) Standard RS-232-C. Frame and signal ground may be isolated from each other as specified in the EIA Standards by operation of a screw switch in the single set housing and a wire strap in the data mountings. All data sets share a common signal ground in the data mountings.

2.09 Three test switches are provided on the 202T for the analog loop (AL), local self-test (LT), and remote test (RT) modes. In analog loop, the customer interface leads may be monitored for proper operation while off-line. In local self-test, the data set tests itself automatically while off-line. In remote test in 2-wire operation, test signals generated in the data set may be monitored at the serving test center for proper operation. In remote test in 4-wire operation, the data set behaves as a repeater for signals sent from the serving test center.

2.10 Six lamps provide the customer with a visual indication of the status of the data equipment. The lamps are monitor power (CN), modem ready (MR), request-to-send (RS), clear-to-send (CS), carrier detector on (CO), and test mode (TM).

2.11 Data set 202T has provisions for connection to a data auxiliary set 828 or 829 type to provide direct distance dialing (DDD) backup capability.

SECTION II - DETAILED DESCRIPTION

1. GENERAL

1.01 The signal-processing functions of data set 202T and their interactions with external circuitry are explained with references to the functional schematics (FSs). A more detailed description of each circuit is given with references to the circuit pack schematics (CPSs).

2. 202T-L1 TRANSMISSION-RECEIVER AND REVERSE CHANNEL - FS1 (MFR DISC.)

2.01 The data set 202T transmitter-receiver circuit consists of one circuit pack (CP1) providing all functions except reverse channel and an optional circuit pack (CP2) which plugs into CP1 for reverse channel.

2.02 From a nominal 24-volt ac center-tapped source transformer connected to terminals AC1, AC2, and GRD, regulated and unregulated dc voltages are derived by the power supply.

INTERFACE CIRCUITS

2.03 The following signals supplied by the customer are received by terminators in the data set:

(a) BA - Transmitted Data. The serial binary data for transmission with mark a negative voltage and space a positive voltage is applied to this lead.

(b) CA - Request-to-Send. A positive voltage on this lead indicates the customer wishes to transmit data, and the RS lamp is turned on. The CA terminator is off for a negative applied voltage or if the CA terminal is left unconnected. A strapping option plug is provided to hold the terminator on for continuous carrier operation.

(c) CR - Carrier Detector Reset. A positive pulse of greater than 0.1 ms duration resets the carrier detector so that the receiver is ready immediately for new data. The CR terminator is off for a negative applied voltage or if the CR terminal is left unconnected. A strapping option plug is provided to disable the CR terminal.

(d) SCA - Secondary Request-to-Send. The signal for transmission from the optional reverse channel is applied to this terminal. The SCA terminator is off for a negative applied voltage or if the SCA terminal is left unconnected.

2.04 Drivers in the data set supply the following signals to the customer:

(a) BB - Received Data. This is the serial binary data received by the customer with mark a negative voltage and space a positive voltage.

(b) CB - Clear-to-Send. A positive voltage is supplied to the customer, and the CS lamp is turned on when the data set is ready to transmit data. Delay intervals of approximately 8, 30, 60, or 180 ms between CA and CB going positive may be obtained.

(c) CC - Data Set Ready. A positive voltage is supplied to the customer, and the MR lamp is on when the data set is ready to transmit or receive data.

(d) CF - Received Line Signal Detector. A positive voltage is supplied to the customer and the CO lamp is on when carrier is detected by the receiver.

(e) SCF - Secondary Received Line Signal Detector. The customer receives the optional reverse channel signal on this terminal.

2.05 The following additional leads appear at the customer interface:

(a) AA - Frame Ground. Connected to the frame of the data set. This lead is not provided on later model data sets.

(b) AB - Signal Ground. Connected to the ground for all of the circuitry of the data set.

(c) +P, -P - Supply Voltages. The +14 and -14 supply voltages are supplied through current-limiting resistors for test purposes.

2.06 At the telephone interface of the data set, the following leads are provided:

(a) DT, DR - First Tip and Ring Pair. In 2-wire operation, these terminals are not used. In 4-wire operation, data signals are received through these terminals.

(b) DT1, DR1 - Second Tip and Ring Pair. In 2-wire operation, data signals are transmitted and received through these terminals. In 4-wire operation, data signals are transmitted through these terminals.

(c) TEK5, TEK6 - Data Auxiliary Set Control. A relay contact may be connected to these terminals to remotely control the data set ready (CC) and clear-to-send (CB) customer interface drivers.

MOS LSI CIRCUITS

2.07 A crystal-controlled oscillator supplies an 844.8-kHz squarewave to the MOS LSI circuit IC3 which performs the following functions:

(a) Modulation of transmitted carrier

(b) Clear-to-send timing

(c) Line control logic (not used in data set 202T)

(d) Answer tone timing (not used in data set 202T)

(e) Soft turnoff and squelch timing

(f) Reverse channel carrier modulation.

2.08 The MOS LSI circuit IC4, in conjunction with IC3, performs the following functions:

(a) Demodulation of received carrier

(b) Carrier detection

(c) Test signal processing.

INSTALLER OPTIONS

2.09 Ten contacts in the S2 switch assembly provide installer-selected options for the clear-to-send, soft turnoff, squelch, and carrier detector time intervals, and for the clamp, local copy, and data auxiliary set features.

2.10 The clear-to-send interval is the delay in the CB output going positive in response to a positive CA input with the BA input negative (mark). Clear-to-send intervals of approximately 8, 30, 60, or 180 ms may be obtained by various settings of the contacts on the AX and BX inputs of IC3 (see 3.04).

2.11 The soft turnoff and squelch intervals start after CA is switched negative. During soft turnoff, a 900-Hz signal appears on PTDX and is transmitted to reset the carrier detector of the receiving data set. After soft turnoff, the PTDX output maintains a constant dc level. During the squelch interval, the carrier detector output (CFOX) is held low, making the received line signal detector output (CF) negative. Soft turnoff intervals of approximately 0, 8, or 24 ms and squelch intervals of approximately 0, 9, or 156 ms are selected by various settings of the NFSQX, NFSFX, FSSQX, and FSSFX inputs of IC3 and IC4 (see 3.05).

2.12 Normal or fast response times of the carrier detector are selected by the contact on the FCDX input to IC4. With the contact closed, the carrier detector is in the normal mode, and will turn on in approximately 20 ms if the carrier frequency is between 1075 and 2325 Hz. The carrier detector will turn off in approximately 10 ms if the carrier frequency is less than 1050 Hz or greater than 2350 Hz. With the contact open, the carrier detector is in the fast mode; it will turn on in approximately 5 ms if the carrier frequency is between 1185 and 1325 Hz. It will turn off in approximately 5 ms for carrier frequencies between 860 and 940 Hz. If the carrier frequencies are outside these limits for the fast mode but are within the limits for the normal mode, the normal mode response times apply.

2.13 A data auxiliary set may be used to control the CB and CC drivers by opening the S2 contact connected to the TEK5 terminal. Then, with an open relay contact in the data auxiliary set connected between the TEK5 and TEK6 terminals, the CB and CC terminals will be held negative. With the relay contact closed, the CC terminal will be positive, and the CB terminal will respond as explained in 2.10.

2.14 Local copy in the 2-wire mode, where the receiver monitors the transmitter when the data set is transmitting, is selected by closing the S2 contact at the input of the local copy control (LCC) circuit.

2.15 A clamped or unclamped received data output (BB) when the carrier detector output CFOX is low is selected by the contact on the CLMPX input to IC4. With the contact open, the clamp mode is in. With the contact closed, the clamp mode is out, and data may be received on the BB lead when the carrier detector is off if the carrier frequency is within the frequency range of the demodulator.

2.16 Ten contacts in the S3 switch assembly provide the 2- or 4-wire and the reverse channel (for 2-wire only) installer-selected options. The contacts for 2- or 4-wire are labeled S3(A), and the contacts for reverse channel are labeled S3(B). The states shown correspond to 2-wire without reverse channel. For 2-wire with reverse channel, the S3(B) contacts are switched to the other state. For 4-wire, the S3(A) contacts are switched to the other state. Also, the S3(B) contact connected to the reverse channel terminal E10 and the local copy S2 contact must be switched to the opposite state shown.

TRANSMITTER-RECEIVER

2.17 While transmitting data, the CA and CC leads must be in the positive state and the CB lead should be positive. The modulator in IC3 generates a frequency-shift modulated signal consisting of mark (1200 Hz) and space (2200 Hz) frequencies corresponding to the serial binary data applied on the BA lead. A digital-to-analog converter in IC3 supplies the signal at the PTDX output. The shaping filter smoothes the signal into an

approximate sinewave and amplifies it to a level of 0 dBm at the DR1 and DT1 terminals.

2.18 During 2-wire operation, the transmitted signal from the shaping filter is applied to the two inputs of the equalizer. The main signal path is the one through the S3(A) break-contact. The other path carries a lower level signal which is important while in the test modes. The output of the equalizer is applied to the demodulator through the limiter and the limiter buffer. If the local copy option is not selected, the LCC circuit has a high output state which disables the BB and CF drivers and the output of the amplitude detector (AMP DET). The output of the LCC circuit is high because the CA lead is positive, the inverting input to the CA switch is low, and the noninverting input is high because the lamp driver output is high.

2.19 Closing local copy switch S2 makes the output of the LCC circuit low, regardless of the state of CA, which enables the BB and CF drivers and the output of the amplitude detector for local copy reception and also for the received signal in 4-wire operation.

2.20 At the end of a transmitted message, the customer may switch CA negative which immediately switches CB negative. Soft turnoff and squelch intervals occur as selected by the options.

2.21 The received data signal path for 2- or 4-wire operation is determined by the S3(A) switch contacts. With 2-wire operation, the contacts are as shown, and the signal is received by the T1 transformer. With 4-wire operation, the contacts are in the opposite state, and the signal is received by the T2 transformer.

2.22 In 2-wire operation, CA must be negative while in the receive mode. The PTDX output of IC3 is clamped at a constant dc level, and the output of the shaping filter is a virtual ground point. The resistor between the T1 transformer and the virtual ground provides the 600-ohm termination for the telephone line. WIth CA negative, the output of the LCC circuit is low, and the BB and CF drivers and the output of the amplitude detector are enabled.

2.23 In both 2- and 4-wire operation, the received signal is processed by the equalizer, limiter, amplitude detector, and the demodulator and carrier detector in IC4. The equalizer provides fixed gain and delay equalization of the telephone channel and rejects out-of-band (OOB) noise. The limiter converts the signal into an approximately constant amplitude squarewave.

2.24 The limited signal on the LIMINX input of IC4 is demodulated by a digital-type demodulator. Signal frequncies below 1585 Hz and from 1765 to 2345 Hz are converted to low and high voltages, respectively, at the BBX output under control of the amplitude and carrier detectors if the clamp option is selected as described in 2.15.

2.25 The carrier detector, in conjunction with the amplitude detector, responds to a valid incoming signal and does not respond to excessive noise and OOB signals. Received line signals greater than -32 dBm will turn on the amplitude detectcr. The turnon time is approximately 1 ms for line signals greater than -24 dBm. In the on state, the output is low unless disabled by the LCC circuit. After the amplitude detector turns on, the carrier detector responds as described in 2.12. The carrier detector and the received data outputs are presented to the customer on the CF and BB leads, respectively.

TEST MODES

2.26 The data set test modes are analog loop, local self-test, and remote test. The three test switches are labeled AL, LT, and RT.

2.27 In the analog loop mode, the data signal applied on BA with CA positive is processed through the normal transmitter and receiver signal paths to the BB output. The customer interface leads may be monitored for proper operation. The CC terminal is clamped negative.

2.28 Depressing the AL switch until it locks operates the four sets of S1A contacts which perform the following functions:

(a) Switch IC3 and IC4 into the analog loop mode.

(b) Disconnect the T1 transformer from the shaping filter and connect a 600-ohm resistor to T1.

(c) Disconnect the T2 transformer from the 4-wire signal path and connect the output of the shaping filter to the S3(A) make-contact.

(d) Modify the feedback network of the shaping filter to decrease the signal level.

(e) Override the LCC circuit through the diode connected to its input and light the test mode (TM) lamp.

2.29 The modification of the feedback of the shaping filter attenuates the signal into the inverting equalizer input more than the signal into the noninverting input. The difference signal resulting at the equalizer output is equivalent to a received line signal of approximately -20 dBm. This attenuated loop-back signal provides a tougher test for the receiver circuits than an unattenuated one.

2.30 In the local self-test mode, IC3 and IC4 are switched into the test mode. A repeating 63-bit pseudorandom word, identical to that in the 903, 914, and 921 test sets, is generated at 1547 b/s in IC4, processed by the transmitter and receiver circuitry, and the resulting word is compared in IC4 to the original word. The TM lamp remains lit as long as the LT switch is depressed unless an error is detected. A properly operating data set will infrequently fail in a self-test interval of greater than 15 seconds because an error in only one bit is required, but more than one failure in five successive tests of 15 seconds duration should not occur. All interface leads are made inoperative during the test, and lamps are lit to check for lamp failures.

2.31 Depressing the LT switch and holding it depressed operates the four sets of S1B contacts which perform the following functions:

(a) Switch IC3 and IC4 into the test mode.

(b) Enable the lamp driver which turns on, causing the TM lamp to light and the LCC circuit to go low, permitting local copy.

(c) Switch the inverter whose output controls the inverting input of the CA switch and the output of the CA terminator, to simulate the request-to-send state and turn on the RS lamp.

(d) Operate an inverter which turns on the MR, CO, and CS lamps, and switches another buffer which decreases the differential delay between any two frequencies in the equalizer. The slope compensation is also reduced.

(e) Modify the feedback network of the shaping filter to decrease the signal level.

(f) Disconnect the T1 transformer from the shaping filter and connect a 600-ohm resistor to T1.

(g) Disconnect the T2 transformer from the 4-wire signal path and connect the output of the shaping filter to the S3(A) make-contact.

2.32 The resulting loop-back signal path is the same as for the analog loop mode. If an error is detected, the LMPX output of IC4 goes high, turning off the lamp driver and the TM lamp.

2.33 The remote test mode for 2-wire operation allows the attendant at the serving test center to test data set circuitry with the exception of the customer interface circuits. Depressing the locking RT switch puts IC3 and IC4 into the test mode. As with local self-test, a repeating 63-bit word is generated, processed by the transmitter and receiver circuitry, and compared to the original word. If an error is detected, constant spacing is generated instead of the test word.

2.34 At the serving test center, the telephone line signal waveforms of the test word or the constant spacing can be observed. The attendant at the test center can apply a tone to the line to cause errors in the internal loop-back signal of the set, and observe the line signal change from test word to constant spacing in a properly operating set. All customer interface leads are made inoperative during the test, and all lamps are lit.

2.35 Depressing the RT switch operates the three sets of S1C contacts which perform the (a) through (e) functions listed in 2.31 with the following exceptions. An S1C make-contact overrides the TM lamp driver control and the LCC circuit so that these circuits

are not turned off when the lamp driver turns off if an error is detected. The shaping filter output level is not attenuated as much because the signal is monitored at the serving test center. The signal level across the DR1 and DT1 terminals, when terminated in 600 ohms, is -11 dBm, and the loop-back signal is equivalent to a line signal of -20 dBm as opposed to -24 dBm for self-test. When the optional reverse channel is installed, additional tests may be performed by the serving test center as outlined in the reverse channel description.

2.36 The remote test mode for 4-wire operation allows the attendant at the data test center to test data set circuitry with the exception of the customer interface circuits. Depressing the locking RT switch puts IC3 and IC4 into the digital loop-back (DLB) mode. The output of the demodulator is coupled to the input of the modulator so that the attendant at the serving test center may perform a loop-back test. All customer interface leads are made inoperative during the test, and only the TM and ON lamps are lit.

2.37 Depressing the RT switch operates the three sets of S1C contacts which perform the following functions during 4-wire operation:

(a) Switch IC3 and IC4 into the DLB mode.

(b) Control the lamp switch (LP SW) for the RS lamp so that the lamp is off regardless of the state of CA.

(c) Turn on the TM lamp. Because the local copy switch is operated in the 4-wire mode, the contact that controls the TM lamp does not affect the state of the LCC circuit.

(d) The signal level at the output of the shaping filter is not modified.

REVERSE CHANNEL

2.38 In 2-wire service, the optional reverse channel, JY1 or JY2, provides a 5-b/s supervision channel in the opposite direction from the primary channel. A 387-Hz on-off amplitude-modulated carrier is used. Insertion of the reverse channel circuit pack and switching of the S3(B) option contacts enable reverse channel. The primary channel is modified as follows:

(a) The frequency reject network (FRN) connected between the equalizer and limiter rejects frequencies around 387 Hz from the receive path.

(b) A low-pass T network is connected to the high-pass section of the shaping filter to form a twin-T notch filter centered at 387 Hz. This network eliminates frequencies around 387 Hz from the primary transmit channel spectrum.

(c) The center frequency and Q of the equalizer are modified to equalize for the phase introduced by the FRN and twin-T.

2.39 The transmit or receive state of the reverse channel is determined by the state of request-to-send (CA). The CA switch controls the FSN switching circuit (JY1 only) and a negative level results in the following states:

(a) The reverse channel transmit signal path from RCTOUTX of IC3 to FSN is enabled (JY1).

(b) The signal path from FSN to the shaping filter is enabled (JY1).

(c) The reverse channel receive signal path from transformer T1 to the equalizer to FSN is disabled (JY1).

(d) The reverse channel driver output is negative if the reverse channel local copy option is not selected. Removal of the option strapping plug enables the driver for local copy (JY1 and JY2).

2.40 (JY1 and JY2) The reverse channel is in the transmit mode. A positive voltage (space) applied to terminal SCA produces a 387-Hz squarewave from RCTOUTX to the FSN. The low-pass FSN supplies a 387-Hz sinewave to the shaping filter. The line signal level with DR1 and DT1 terminated in 600 ohms is -1 dBm. The FSN output is also converted to a dc voltage by the reverse channel demodulator (RC DEMOD) and a positive voltage is applied to the SCF terminal if local copy is selected. No 387-Hz signal is generated for a negative voltage (mark) applied to SCA.

2.41 With CA positive, the output of the CA switch is high, resulting in a reversal of the states just described. The reverse channel receive signal path from T1 through the equalizer, FSN, RC DEMOD, and the driver (always enabled for JY2) is enabled for JY1.

2.42 (JY2) A second FSN eliminates the need for the FSN switching on the JY2 reverse channel. A FSN is always in the receive path, thereby allowing receipt of reverse channel signal regardless of the state of request-to-send.

TEST MODES WITH REVERSE CHANNEL

2.43 In the analog loop mode with the reverse channel installed, a signal applied on the SCA terminal with CA negative will produce a modulated 387-Hz squarewave on RCTOUTX which is supplied to the FSN. Two signal paths are established from the FSN to the shaping filter. One is the normal transmit mode path, and the other is the path through terminal E10 provided to boost the level of the loop-back reverse channel signal. A level equivalent to a -6 dBm received line signal results at the

equalizer. This signal is blocked by the FRN. However, the reverse channel signal from the FSN is supplied to the RC DEMOD, and a signal is received at the SCF terminal if local copy is selected.

2.44 In the local self-test mode with reverse channel, terminals SCA and SCF are made inoperative, and the lamp driver holds the output of the CA switch low unless an error is detected. With IC3 and IC4 in the test mode, a 387-Hz squarewave on-off modulated signal at 4.3 b/s is supplied at RCTOUTX, filtered by the FSN, and supplied to the shaping filter via the two signal paths as in the analog loop mode. The FRN must reject this -6 dBm signal for the set to pass self-test.

2.45 In the remote test mode, the same reverse channel states are established as in local self-test except that terminal E10 is not connected to the shaping filter and the reverse channel signal is applied to the 2-wire line. The reverse channel signal level transmitted is -14 dBm, and the loopback signal level is -18 dBm. The reverse channel signal transmitted simultaneously with the primary channel signal may be monitored at the serving test center to verify proper reverse channel transmit operation.

2.46 After an error is caused in the test mode by a tone sent from the serving test center, the LMPX, lamp driver, and CA switch outputs all go high, putting the reverse channel in the receive mode. No signal appears at the RCTOUTX output. As in the case without reverse channel, constant spacing (2200 Hz) is supplied at PTDX and transmitted. Proper reverse channel receive operation is verified by sending a 387-Hz tone from the test center which is demodulated, making the RC DEMOD output high and the RCRX input of IC4 low. Constant marking (1200 Hz) is transmitted in a properly operating data set.

3. 202T-L1 TRANSMITTER-RECEIVER CIRCUIT - CPS1 (MFR DISC.)

POWER SUPPLY

3.01 The KS-21239 L1, L4, or L5 transformer or the ac supply of the 39A1 or 40B1 data mounting provides a nominal 24-volt ac center-tapped source to the AC1, AC2, and GRD inputs of the full-wave bridge rectifier CR2-CR5. Nominal +14 and -14 volt outputs result with up to 1.7-volts peak-to-peak (P/P) ripple and approximately ±2.5 volts tolerance. When commercial ac power is not available, dc voltages of ±15 ±1.5 volts may also be connected to the AC1, AC2, and GRD inputs to power the set. Voltages approximately 0.7 volt less than the inputs result at the rectifier outputs.

3.02 Resistor-capacitor filters derive ±11 volts with a maximum of 0.5 volt peak-to-peak ripple and a tolerance of approximately ±3.0 volts. An integrated circuit voltage regulator IC2 supplies +5 ±0.25 volts with less than 0.1 volt P/P ripple. Zener diode CR1 derives -12 volts. With an ac input voltage much less than nominal, corresponding to a power line voltage of 105 volts, the zener diode may drop out of conduction, but the instantaneous voltage across the zener diode should remain within the range -12 ±1.2 volts.

MOS LSI CIRCUITS

3.03 MOS LSI circuits IC3 and IC4 provide four operating modes in data set 202T which are determined by the ANALX, TESTX, and DLBX inputs as follows:

(a) Data mode (ANALX=TESTX=DLBX=0)

(b) Analog loop mode (ANALX=1, TESTX=DLBX=0)

(c) Test mode (TESTX=1, ANALX=DLBX=0)

(d) Digital loop-back (DLB) mode (DLBX=1, ANALX=TESTX=0).

3.04 With IC3 and IC4 in the data mode or the analog loop mode, the clear-to-send interval is determined by the AX and BX inputs as shown in Table A. Logic level 1 is with the switch contact open. If CAX changes state during the interval, the duration of the interval is undefined.

TABLE A

CLEAR-TO-SEND INTERVAL OPTIONS

AX	BX	Interval Range (ms)
0	0	171.8 - 188.4
1	0	57.3 - 62.5
0	1	29.0 - 30.6
1	1	7.7 - 8.3

3.05 Soft turnoff and squelch intervals are determined by the NFSQX, NFSFX, FSSQX, and FSSFX inputs as shown in Table B. Logic level 1 is with the switch contact open.

3.06 An 844.8 ±0.42 kHz squarewave is applied to the CL844X input to make IC3 and IC4 function. The duty cycle of the squarewave must be 50 ±10 percent, and the rise and fall times must be less than 0.2 us for proper operation. For this and all other inputs, the logic 0 level must be between 0 and 0.4 volts and the logic 1 level must be between 4 and 5 volts. Most inputs have internal pullup resistors to the +5 volt supply so logic level 1 is assumed if the input is open-circuited. The exceptions are ALX, AMPDETX, CDX, D1X, LIMINX, RCRX, and SCAX.

3.07 Most of the outputs swing between a logic 0 level of 0 to 0.4 volt and a logic 1 level of 4 to 5 volts. The exceptions are: the PTDX output which has three levels, approximately 0, +2.5, and +5 volts, to provide a better approximation to a sinewave than is obtained with a squarewave; and the DRYX output which has a logic 1 level of approximately +5 volts but a logic 0 level that is determined by the external components connected to it.

TABLE B

SOFT TURNOFF AND SQUELCH INTERVAL OPTIONS

NFSQX	NFSFX	FSSQX	FSSFX	STF INT Range (ms)	SQ INT Range (ms)
0	0	*	*	0	0
0	1	*	1	7.8 - 8.4	0
0	1	*	0	23.2 - 24.0	0
1	0	1	1	0	8.4 - 9.0
1	0	*	0	0	148.2 - 164.5
1	0	0	*	0	148.2 - 164.5
1	1	1	1	7.8 - 8.4	8.4 - 9.0
1	1	0	1	7.8 - 8.4	148.2 - 164.5
1	1	*	0	23.2 - 24.0	148.2 - 164.5

* Indicates don't care, ie, either 0 or 1.

LINE TRANSFORMER CIRCUITS

3.08 The T1 and T2 transformers present 600-ohm terminations to the lines, and have electrostatic shields to reduce longitudinal line noise. Signals are attenuated approximately 2 dB by the transformers. Resistors R17 and R25 limit surge currents, and surge rated diodes CR8 and CR9 limit voltage surges to approximately 20 volts.

SHAPING FILTER

3.09 The shaping filter, an active fourth-order bandpass filter, has a transfer function of the form $as^2/(bs^4+cs^3+ds^2+es+1)$. It is composed of high-pass sections C6,R14 and C7,R5 and low-pass sections C1,R6 and C2,R7 with nominal cutoff frequencies of 780 and 2800 Hz, respectively. Feedback to R14 and C1 from R2 shifts the 3-dB points of the bandpass response further apart. Capacitor C8, necessary when reverse channel is installed, reduces the gain at higher frequencies in the passband. The resulting 3-dB cutoff frequencies are approximately 600 and 3000 Hz, and the response falls off at 12 dB per octave. The signal level into 600 ohms connected across the DT1 and DR1 terminals is approximately 0 dBm.

3.10 Terminals E6, E7, and E8 are connected to R15, R16, and C7 of CPS2 to form a twin-T notch filter and a reverse channel signal path through the shaping filter when reverse channel is installed. Approximately 40 dB of attenuation at 387 Hz and 1.5 dB of attenuation in the passband results for the primary channel response of the shaping filter.

EQUALIZER

3.11 The compromise equalizer is composed of two second-order stages that provide slope equalization with a low-pass filter and delay equalization with an all-pass filter. The filters are realized using a single amplifier biquadratic type realization for the low-pass filter and a Sallen-Key type realization for the all-pass filter.

3.12 The low-pass network is comprised of IC9B, R39 through R42, and C16 through C18. The response of this network is a linear gain versus frequency starting with 0 dB at about 1000 Hz and rising to approximately +5.5 dB at 2700 Hz. The response falls off after 2700 Hz at about 12 dB per octave.

3.13 The all-pass network is composed of IC9A, R43 through R47, R49 through R52, and C19 and C20. Resistors R44 and R50 are switched into the network when the data set is equipped with reverse channel. This changes the center frequency and Q as outlined below to provide additional

filtering to phase equalize the filters of the reverse channel circuit:

(a) With reverse channel, the center frequency of the network is approximately 1925 Hz. The differential delay measured between 1000 and 1925 Hz is approximately 700 us.

(b) Without reverse channel, the center frequency of the network is approximately 1775 Hz. The differential delay measured between 1000 and 1750 Hz is about 540 us.

3.14 When the data set is in the local self-test mode or in the remote test mode during 2-wire operation, R52 is bypassed to ground by Q5. This change decreases the Q of the all-pass network which decreases the differential delay measured between any two frequencies, without appreciably changing the center frequency.

3.15 On series 6 and later data sets, R52 may be paralleled by R74 via an option strap inserted in E28. This option reduces the Q of the delay equalizer to provide less compromise equalization for local or short-haul reception.

LIMITER - AMPLITUDE DETECTOR

3.16 Amplifier IC10 and the six diodes in the feedback loop form a soft limiter at nominal input levels. When the input swings slightly negative, the output rises, and when it reaches approximately +1 volt, CR16 and CR17 start to conduct to provide negative feedback. For positive inputs, CR19 and CR20 conduct when the output reaches -1 volt. Resistors R5, R6, R9, and R15 establish the voltage gain when the output exceeds ±1 volt. Diodes CR15 and CR18 limit the output swing to approximately ±2 volts when high-level inputs are applied. Transistor Q6 is biased on the edge of conduction and produces a hard-limited output.

3.17 Resistor R8 provides positive feedback around the limiter, which makes it respond to very low level signals (and noise). The output frequency is a maximum of 1/3 of the frequency of any input below approximately -60 dBm because C25 and C26 are in the feedback loop and slow down the response. The positive feedback is small enough so as not to interfere at signal levels above -45 dBm (0.012 volt P/P).

3.18 At the junctions of CR19 and CR20 and of CR16 and CR17, negative and positive half-wave rectified signals result which are filtered by RC networks. The resultant dc voltages are applied through R4 and R11 to the differential inputs of IC11, which operates at its open loop voltage gain. Voltages derived by CR21 and CR22 establish the amplitude detection level. When the rectified and filtered signals are such that they cancel the reference levels at the inputs to IC11, IC11 is at the point of switching from a positive to a negative output level. This state occurs for received line signals of approximately -32 dBm. The maximum amplitude detection time is approximately 6 ms, which occurs with low signal levels. The maximum release time is approximately 10 ms, which occurs with high signal levels.

SWITCHING CIRCUITRY

3.19 In the normal mode (S1A, S1B, S1C not operated) the customer-controlled terminal CA determines the state of Q11. The emitter of Q11 is clamped to +5 volts. With the CA terminal positive, Q11 is on and terminal E20, which controls the reverse channel, is at +5 volts. The emitter of Q8 is at approximately 6.5 volts if contact 1 of S2 is open so Q7 is on, regardless of the state of IC11. The inverting inputs of IC6A and IC7 are held at approximately 6 volts which makes the BB and CF terminals negative regardless of the state of BBX and CFCX. With contact 1 of S2 closed, Q8 is off and Q7 is controlled by IC11, and the inverting inputs of IC6A and IC7 are at approximately 1.5 volts, making the drivers operational.

3.20 With the CA terminal negative, Q11 is off and terminal E20 is at approximately -5 volts with contact 1 of S2 open or closed. Transistor Q8 is off.

3.21 When test switch S1B or S1C is operated in the 2-wire mode, Q12 turns on when the LMPX output is at logic 0 level. Transistor Q11 turns off because its emitter is switched to approximately ground potential. If the LMPX output switches to logic 1 level because of an error in the test mode of IC3 and IC4, Q12 turns off and Q11 turns on. The TM lamp turns off during self-test but is held on by an S1C control during remote test.

3.22 The lamps are light-emitting diodes (LEDs). Each LED is biased with a current of approximately 10 mA when it is lit, which produces a voltage drop of approximately 2 volts across the LED. In the series connection arrangement of LEDs, a transistor is turned on to turn off the LED connected in parallel with it.

4. JY1 REVERSE CHANNEL CIRCUIT - CPS2 (MFR DISC.)

FRN

4.01 The frequency reject network (FRN) consists of two identical second-order single amplifier biquadratic (SAB) networks, in tandem. Maximum attenuation of the notch filter response occurs at 387 ±8 Hz and should be greater than 55 dB to provide adequate rejection. At frequencies higher than 387 Hz, the response increases, and from approximately 1000 Hz and higher the gain is 0.0 ±0.5 dB. Resistors R11 and R12 form a

gain enhancement divider network that provides for the correction gain.

FSN

4.02 The frequency select network (FSN) consists of two identical second-order SAB networks, IC3A and IC3B, and associated components, in tandem. An underdamped low-pass response is obtained with 23 dB of gain at 387 Hz and 49 dB of attenuation at approximately 1200 Hz. The peak has a Q of approximately 7.8 and a 3-dB bandwidth around 387 Hz of approximately ±15 Hz. When in the reverse channel transmit signal path, an approximate 6-volt P/P signal results at the output of IC3B.

REVERSE CHANNEL DEMODULATOR

4.03 Amplifiers IC4 and IC5A and associated components form a demodulator that produces a positive output level for input signals with frequency near 387 Hz and amplitude greater than the threshold voltage of approximately 0.08 volt P/P. The input is at the junction of R39 and R40. Positive feedback around IC4 establishes the threshold voltage. Input signal levels below threshold have little effect on the output of IC4 which oscillates at approximately 770 Hz determined by the network made up of R42, R43, C12, and C15. A 387-Hz signal above threshold is amplified by nearly the open loop gain of IC4.

4.04 A high-pass filter, comprised of R50 and C16, and a low-pass filter, comprised of R49 and C17, are connected to the output of IC4. A 387-Hz output experiences less attenuation through the low-pass section and produces approximately +0.5 volt on C19 and -0.5 volt on C18 which drive the output of IC5A positive. A 770-Hz output favors the high-pass circuit path and produces a negative output.

SWITCHING CIRCUITS

4.05 In the FSN switching circuit, the signal flow through three separate circuit paths is controlled by the voltage applied to the E20 terminal. With E20 held at +5 volts, Q2 holds Q3 off and Q4 and Q5 on. The path from E2 to the FSN is enabled and the other two paths are disabled. With E20 held at -5 volts, Q2 holds Q3 on and Q4 and Q5 off. The paths from E4 to the FSN and the FSN to E7 are enabled and the other path is disabled.

4.06 The customer interface driver IC5B is disabled such that SCF is negative when +5 volts is applied to terminal E20 with the strapping plug between the base and emitter of Q7 removed. Transistor Q7 is on and the inverting input of IC5B is at +5 volts. Application of a voltage between +2.5 and +5 volts to terminal E1 also disables IC5B.

5. INTERFACE CIRCUIT AND POWER TRANSFORMER (47B1 DATA MOUNTING) - FS2

5.01 This assembly, used for single data set installations, consists of a printed circuit board CP3 with a data set connector, a telephone interface connector, a power transformer, a 6-foot power cord, a 5-1/2 foot telephone connection cord, and an aluminum and plastic housing and frame.

6. 40B1 DATA MOUNTING - FS3

6.01 The 40B1 data mounting consists of a backplane printed circuit board CP5; 16 printed circuit flex tapes, each containing a data set connector and a customer interface connector; an ac power supply; a power cord; and a rack-mountable frame. Connections to the telephone system are made through two 50-pin connectors mounted on the backplane.

6.02 A nominal voltage of 24 volts ac is supplied to each data set by the T1 or T2 transformer. The data sets in positions 1 through 4 and 9 through 12 are powered by T1, and the sets in the other eight positions are powered by T2. The 70-type fuses used provide a visual indication if a fuse operates.

7. 39A1 DATA MOUNTING - FS4

7.01 The 39A1 data mounting is similar to the 40B1 data mounting, but it does not contain a backplane or the flex tapes. Sixteen data set connectors with wire-wrap terminals are provided for connecting the data sets.

8. JY2 REVERSE CHANNEL CIRCUIT - CPS2B

FRN

8.01 See 4.01 for a description of the frequency reject network.

FSN

8.02 The transmitter and receiver FSNs each consist of two identical second-order SAB networks. An underdamped low-pass response is obtained with 3 dB of gain at 387 Hz and an attenuation greater than 50 dB at 1000 Hz. The peak has a Q of approximately 7.8 and a 3-dB bandwidth around 387 Hz of approximately +15 Hz. When a 387-Hz signal is being transmitted, the signal level at the output of transmitter FSN is approximately 6 volts P/P. At the input to the receiver FSN, a clipping circuit, consisting of diodes CR1 and CR2, resistor R13, and capacitor C28 is provided to prevent transients on the loop during call setup from producing spurious outputs from the reverse channel demodulator.

REVERSE CHANNEL DEMODULATOR

8.03 Amplifiers IC4 and IC5A and associated components form a demodulator that produces a positive output level for input signals with frequency near 387 Hz and amplitude greater than the threshold voltage of approximately 0.08 volt P/P. Positive feedback around IC4 establishes the threshold. Input signal levels below the threshold have little effect on the output of IC4, which oscillates at approximately 770 Hz, determined by the network composed of resistors R25 and R26 and capacitor C14. A 387-Hz signal above threshold is amplified by nearly the open loop gain of IC4.

8.04 A high-pass filter, composed of resistor R31 and capacitor C15, and a low-pass filter, made up of resistor R30 and the effective capacitance resulting from capacitors C16 and C17, are connected to the output of IC4. A 387-Hz output experiences less attenuation through the low-pass section and produces approximately +0.5 volt on capacitor C16 and -0.5 volt on capacitor C17, which drive the output of IC5A positive. A 770-Hz output favors the high-pass circuit path and produces a negative output.

TERMINATOR, DRIVER, AND CONTROL CIRCUITS

8.05 Data signal SCA is inverted by the terminator, which consists of transistor Q2 and associated components and is applied to IC3 and the control circuit, which consists of transistor Q3 and associated components. The control circuit controls the driver, which consists of IC5B, to enable or disable the reverse channel output at terminal E3.

8.06 With terminal SCA negative, terminal E2 is negative, transistors Q2 and Q3 are off, and the inverting input of IC5B is held at approximately ground potential by a resistor network on the data set circuit pack. The driver and the reverse channel receiver are enabled.

8.07 With terminal SCA positive, terminal E2 is positive, transistor Q2 is on, but the state of transistor Q3 depends on the voltage applied to terminal E20 and on the reverse channel local copy option. With local copy, selected by strapping terminal E21 to terminal E22, transistor Q3 is off and the driver is enabled. Without local copy, selected by strapping terminal E21 to terminal E23, transistor Q3 is on if terminal E20 is at ground potential and the driver is disabled with terminal E3 negative. A voltage of 5.7 volts is applied to terminal E20 if terminal CA is positive or the data set is in the analog loop-back test mode. Then transistor Q3 is off and the driver is enabled.

8.08 The local copy signal received at terminal E3 is delayed approximately 50 ms from the signal provided at terminal E2. When local copy is not provided, the driver must be held disabled for at least 50 ms after terminal E2 goes negative to suppress the delayed signal. Capacitor C18 holds the driver disabled by slowly discharging from 5 volts toward ground potential. The driver becomes enabled when the voltage at terminal E1 reaches approximately 0.6 volt.

9. 202T-L1A TRANSMITTER-RECEIVER AND JY4 REVERSE CHANNEL - FS5

9.01 Data set 202T-L1A offers the following features not provided with data set 202T-L1:

(a) Compromise amplitude equalizer installer option. When in the MIN position, this option inserts a low-pass RC filter in the receive signal path, which effectively removes the compromise amplitude equalization.

(b) Channel condition installer option. Modifies the demodulator of IC229C for improved performance on C2 conditioned lines at all rated bit speeds.

(c) State of CC (DSR) during analog loopback installer option. Allows the customer to choose the state of CC during the analog loopback test.

(d) A filter on TEK5. Permits data auxiliary set 828 or 829 to be placed up to 1000 feet away.

(e) Lower distortion during analog loopback. This is achieved by forcing the MIN delay equalizer option during the loopback test.

(f) An improved 2-wire remote test hybrid. This provides more cancellation of the locally generated signal at the equalizer input, thereby allowing a higher signal level to be transmitted to the remote station, ensuring a more reliable remote test.

(g) A clamp on BBX when the amplitude detector is low. This improves performance when the received data clamp option is OUT.

(h) Improved self-test. A nonfunctioning crystal oscillator is detected during self test by checking on the state of Ampdetx.

(i) A high-pass RC filter in the receive path. Increases rejection of 60 Hz and its harmonics when reverse channel is not installed. This filter is not in the receive path when reverse channel, which provides low-frequency rejection, is installed.

(j) Improved loopback test. When the reverse channel circuit is installed on data set 202T-L1A, loopback of reverse channel during analog loopback is independent of the reverse channel local copy option.

(k) An additional delay equalizer stage. This is used only when reverse channel is installed to compensate for degradation to the primary channel caused by the FRN.

(l) Improved fast mode carrier detection. The fast mode carrier detection operate time is 9 dB more tolerant of second harmonic distortion and is also less affected by noise.

(m) Improved digital loopback test. The carrier detector must now be on in order for digital loopback to occur. The demodulator output is clamped at mark level when the carrier detector is off.

INTERFACE CIRCUITS

9.02 See 2.03 through 2.06 for description of the interface circuits with the exception that the strapping option plugs mentioned in parts (b) and (c) of paragraph 2.03 are replaced by S4 switch contacts.

MOS LSI CIRCUITS

9.03 See 2.07 and 2.08 for description of the functions of the MOS LSI circuits.

9.04 IC4, a KS-21217 L1 device in data set 202T-L1, has been replaced by a WE229C IC in this application. The 229C device has provision for a new option which allows for changing the demodulator for improved performance on C2 conditioned lines. It also has an improved carrier detector circuit.

INSTALLER OPTIONS

9.05 See 2.09 through 2.14 for a description of installer options provided by nine of the contacts of the S2 switch. A filter has been added to the TEK5 terminal (described in 2.13) which allows the data auxiliary set to be placed up to 1000 feet from the data set.

9.06 A clamped or an unclamped received data output (BB) when the carrier detector output is low is selected by the S2 contact on the CLMPX input to IC4. With the control open, the clamp mode is in. With the contact closed, the clamp mode is out and data may be received on the BB lead prior to turnon of the carrier detector if the carrier frequency is within the frequency range of the demodulator and is of a high enough level to operate the amplitude detector.

9.07 Ten contacts in the S3 switch assembly provide the 2- or 4-wire, the reverse channel (for 2-wire only), the compromise delay equalization, the compromise amplitude equalization, and the channel condition installer-selected options. The contacts for 2- or 4-wire are labeled S3(A); the contacts for reverse channel are labeled S3(B). The states shown correspond to 2-wire without reverse channel. For 2-wire with reverse channel, the S3(B) contacts are switched to the other state. For 4-wire, the S3(A) contacts are also switched to the other state. The S2 contact that provides local copy must also be switched to the opposite state of that shown.

9.08 An S3 switch contact parallels R67 of the delay equalizer section. Closing this contact lowers the Q of the stage, thereby reducing the amount of compromise equalization. This option may be used for local and short-haul data reception.

9.09 The compromise amplitude equalizer option is provided by an S3 switch contact used to switch capacitor C30 to form a low-pass RC network with resistor R58. The response of the network cancels the compromise amplitude response of the equalizer.

9.10 The channel condition option is used to modify the demodulator for operation over C2 conditioned 3002 lines. This option is provided by the S3 switch contact connected to FCDX of IC4.

9.11 The three S4 switch contacts provide the carrier detector reset and continuous carrier options (see 9.02) and the state of CC (DSR) during analog loopback option (see 9.14).

TRANSMITTER-RECEIVER

9.12 See 2.17 through 2.25 for description of the operation of the transmitter-receiver with the exception that 2.24 should refer to 9.06 instead of 2.15.

TEST MODES

9.13 The data set test modes are analog loop, local self-test, and remote test. The three test switches are labeled AL, LT, and RT.

9.14 See 2.27 and 2.28 for a description of the data set in the analog loopback mode with the exception that in 2.27 whether or not the CC terminal is at a negative level (OFF) is dependent on the setting of the option labeled state of CC (DSR) during analog loopback. Part (d) of 2.28 should read: Force the MIN delay equalizer option to reduce distortion during the test. Also, add part (I) which reads: Place a low voltage on inverting input of CA switch via diode CR23.

9.15 Paragraph 2.29 does not apply. The signal level is not reduced.

9.16 See 2.30 and 2.31 for a description of the data set when in the local self-test mode with the exception that part (a) of 2.31 should read: Switch IC3 and IC4 into the test mode which also lifts the emitter of the RS control transistor so that the RS lamp turns on. Part (c) of 2.31 should read: Place a low voltage on the inverting input of

10.03 The low-pass network is comprised of IC9B, R49 through R51, and C22 and C23. The response of this network is a linear gain versus frequency starting with 0 dB at about 1000 Hz and rising to approximately +4.5 dB at 2700 Hz. The response falls off after 2700 Hz at about 12 dB per octave.

10.04 During 2-wire remote test transmission, an error in the locally looped-back signal is caused by receipt of a tone from the serving test center. In order for this tone to cause an error, the level of the transmitted signal at the input to the local limiter must be relatively low. Resistors R29, R59, and R60 with capacitors C24 and C25 form a network to the positive input of IC9B giving a response similar to that of the low-pass network of the equalizer. The difference amplifier thus formed reduces the transmit signal level at the input to the limiter without affecting the receive level.

10.05 The first stage of the all-pass network is made up of IC9A, R52 through R56, R61 and R67, and C25 and C27. The second stage of all-pass network is made up of IC11B, R62 through R66, R68 and R69, and C36 and C37. The differential delay of the first all-pass network is about 5601 usec between 1000 and 1750 Hz for the MAX setting of the delay option. The total differential delay for the two all-pass networks is 6650 usec between the same two frequencies.

10.06 When the data set is in the local self-test mode or in the 2-wire remote test mode, R61 of the first and R68 of the second all-pass network are bypassed to ground by the ON states of Q7 and Q8. An S3 switch contact in parallel with R67 can be used to bypass the resistor to ground, thus providing the MIN compromise delay equalization option.

10.07 Capacitor C28 and resistor R57 form a high-pass RC filter in the receive signal path when reverse channel is not installed. It aids in the rejection of 60 Hz and its harmonics.

LIMITER-AMPLITUDE DETECTOR

10.08 The description of the limiter-amplitude detector applies to data set 202T-L1A as well as data set 202T-L1. It is repeated here (10.09 through 10.11) with data set 202T-L1A component numbers which are different from data set 202T-L1 and too numerous to list separately.

10.09 Amplifier IC10 and the six diodes in the feedback loop form a soft limiter at nominal input levels. When the input swings slightly negative, the output rises, and when it reaches approximately +1 volt, CR14 and CR15 start to conduct to provide negative feedback. For positive inputs, CR17 and CR18 conduct when the output reaches -1 volt. Resistors R5, R6, R9, and R15 establish the voltage gain when the output exceeds ±1 volt. Diodes CR13 and CR16 limit the output swing to approximately ±2 volts when high-level inputs are applied. Transistor Q6 is biased on the edge of conduction and produces a hard-limited output.

10.10 Resistor R8 provides positive feedback around the limiter, which makes it respond to very low level signals (and noise). The output frequency is a maximum of one-third of the frequency of any input below approximately -60 dBm because C34 and C35 are in the feedback loop and slow down the response. The positive feedback is small enough so as not to interfere at signal levels about -45 dBm (0.012 volt P/P).

10.11 At the junctions of CR17 and CR18 and of CR14 and CR15, negative and positive half-wave rectified signals result which are filtered by RC networks. The resultant dc voltages are applied through R4 and R11 to the differential inputs of IC11A, which operates at its open loop voltage gain. Voltages derived by CR19 and CR21 establish the amplitude detection level. When the rectified and filtered signals are such that they cancel the reference levels at the inputs to IC11A, IC11A is at the point of switching from a positive to a negative output level. This state occurs for received line signals of approximately -32 dBm. The maximum amplitude detection time is approximately 6 ms, which occurs with low signal levels. The maximum release time is approximately 10 ms, which occurs with high signal levels.

LCC, CA, AND LAMP SWITCHING CIRCUITS

10.12 The description of the switching circuits (see 3.19 through 3.21) applies to data set 202T-L1A as well as data set 202T-L1 with the exception that reference to Q7 and Q8 should be to Q5 and Q9, respectively.

10.13 When test switch S1A is depressed, the TM lamp is turned on by an S1A contact which also pulls the base of Q11 low through diode CR23. The emitter of Q11 remains at +5 volts so Q11 turns on enabling local copy on the reverse channel if reverse channel is installed.

10.14 The lamps are light-emitting diodes (LEDs). Each LED is biased with a current of approximately 10 mA when it is lit, which produces a voltage drop of approximately 2 volts across the LED. In the series connection arrangement of LEDs, a transistor is turned on to turn off the LED connected in parallel with it.

11. JY4 REVERSE CHANNEL - CPS2C

11.01 The description of the JY2 reverse channel (see 8.01 through 8.08) applies to the JY4 reverse channel as well with the exception of minor changes to the FRN.

11.02 FRN notch depth and width are reduced, there is approximately 4.5 dB of gain at 550 Hz, and approximately 2 dB of loss at 1700 Hz. The filter is realized with two STAR-DIPS.

10.03 The low-pass network is comprised of IC9B, R49 through R51, and C22 and C23. The response of this network is a linear gain versus frequency starting with 0 dB at about 1000 Hz and rising to approximately +4.5 dB at 2700 Hz. The response falls off after 2700 Hz at about 12 dB per octave.

10.04 During 2-wire remote test transmission, an error in the locally looped-back signal is caused by receipt of a tone from the serving test center. In order for this tone to cause an error, the level of the transmitted signal at the input to the local limiter must be relatively low. Resistors R29, R59, and R60 with capacitors C24 and C25 form a network to the positive input of IC9B giving a response similar to that of the low-pass network of the equalizer. The difference amplifier thus formed reduces the transmit signal level at the input to the limiter without affecting the receive level.

10.05 The first stage of the all-pass network is made up of IC9A, R52 through R56, R61 and R67, and C25 and C27. The second stage of all-pass network is made up of IC11B, R62 through R66, R68 and R69, and C36 and C37. The differential delay of the first all-pass network is about 5601 usec between 1000 and 1750 Hz for the MAX setting of the delay option. The total differential delay for the two all-pass networks is 6650 usec between the same two frequencies.

10.06 When the data set is in the local self-test mode or in the 2-wire remote test mode, R61 of the first and R68 of the second all-pass network are bypassed to ground by the ON states of Q7 and Q8. An S3 switch contact in parallel with R67 can be used to bypass the resistor to ground, thus providing the MIN compromise delay equalization option.

10.07 Capacitor C28 and resistor R57 form a high-pass RC filter in the receive signal path when reverse channel is not installed. It aids in the rejection of 60 Hz and its harmonics.

LIMITER-AMPLITUDE DETECTOR

10.08 The description of the limiter-amplitude detector applies to data set 202T-L1A as well as data set 202T-L1. It is repeated here (10.09 through 10.11) with data set 202T-L1A component numbers which are different from data set 202T-L1 and too numerous to list separately.

10.09 Amplifier IC10 and the six diodes in the feedback loop form a soft limiter at nominal input levels. When the input swings slightly negative, the output rises, and when it reaches approximately +1 volt, CR14 and CR15 start to conduct to provide negative feedback. For positive inputs, CR17 and CR18 conduct when the output reaches -1 volt. Resistors R5, R6, R9, and R15 establish the voltage gain when the output exceeds ±1 volt. Diodes CR13 and CR16 limit the output swing to approximately ±2 volts when high-level inputs are applied. Transistor Q6 is biased on the edge of conduction and produces a hard-limited output.

10.10 Resistor R8 provides positive feedback around the limiter, which makes it respond to very low level signals (and noise). The output frequency is a maximum of one-third of the frequency of any input below approximately -60 dBm because C34 and C35 are in the feedback loop and slow down the response. The positive feedback is small enough so as not to interfere at signal levels about -45 dBm (0.012 volt P/P).

10.11 At the junctions of CR17 and CR18 and of CR14 and CR15, negative and positive half-wave rectified signals result which are filtered by RC networks. The resultant dc voltages are applied through R4 and R11 to the differential inputs of IC11A, which operates at its open loop voltage gain. Voltages derived by CR19 and CR21 establish the amplitude detection level. When the rectified and filtered signals are such that they cancel the reference levels at the inputs to IC11A, IC11A is at the point of switching from a positive to a negative output level. This state occurs for received line signals of approximately -32 dBm. The maximum amplitude detection time is approximately 6 ms, which occurs with low signal levels. The maximum release time is approximately 10 ms, which occurs with high signal levels.

LCC, CA, AND LAMP SWITCHING CIRCUITS

10.12 The description of the switching circuits (see 3.19 through 3.21) applies to data set 202T-L1A as well as data set 202T-L1 with the exception that reference to Q7 and Q8 should be to Q5 and Q9, respectively.

10.13 When test switch S1A is depressed, the TM lamp is turned on by an S1A contact which also pulls the base of Q11 low through diode CR23. The emitter of Q11 remains at +5 volts so Q11 turns on enabling local copy on the reverse channel if reverse channel is installed.

10.14 The lamps are light-emitting diodes (LEDs). Each LED is biased with a current of approximately 10 mA when it is lit, which produces a voltage drop of approximately 2 volts across the LED. In the series connection arrangement of LEDs, a transistor is turned on to turn off the LED connected in parallel with it.

11. JY4 REVERSE CHANNEL - CPS2C

11.01 The description of the JY2 reverse channel (see 8.01 through 8.08) applies to the JY4 reverse channel as well with the exception of minor changes to the FRN.

11.02 FRN notch depth and width are reduced, there is approximately 4.5 dB of gain at 550 Hz, and approximately 2 dB of loss at 1700 Hz. The filter is realized with two STAR-DIPS.

the CA switch via a diode connected to the collector of the TM lamp driver which is ON as noted in part (b). Part (d) of 2.31 should read: Operate an inverter which turns on the MR, CO, and CS lamps, and switches two buffers which decrease the differential delay between any two frequencies in the two delay equalizer sections. Part (e) of 2.31 should read: Attenuate by 28 dB the signal from PTDX to the shaping filter input.

9.17 If an error is detected during local self-test, the LMPX output of IC4 goes high, turning off the lamp driver and the TM lamp.

9.18 The TM lamp is held off by the amplitude detector through diode CR25 if the LSI logic is inoperative as a result of a malfunctioning crystal oscillator.

9.19 See 2.33, 2.34, and 2.35 for a description of the data set while in the 2-wire remote test mode with the exception that reference to -11 dBm in 2.35 should be to -5 dBm and reference to -24 dBm for self-test should be omitted.

9.20 A hybrid arrangement (see 10.04) reduces the level of the local signal at the input to the limiter.

9.21 See 2.36 and 2.37 for a description of the data set when in the 4-wire remote test mode.

REVERSE CHANNEL

9.22 Those portions of 2.38 through 2.42 that apply to the JY2 reverse channel also apply to the JY4 reverse channel as used on data set 202T-L1A with the exception of part (c) of 2.38. The FRN of the JY4 provides some low-end amplitude compensation and also adds less delay distortion to the receive path of the primary channel.

9.23 An extra section of delay equalizer is provided on the data set circuit pack in the path of the FRN insertion point. The additional compensation helps correct for delay distortion added by the FRN and twin-T.

TEST MODES WITH REVERSE CHANNEL

9.24 In the analog loopback mode with reverse channel installed, a signal applied on terminal SCA with terminal CA negative and terminal CD positive produces a modulated 387-Hz squarewave on the RCTOUTX output of IC3, which is filtered by the XMIT FSN. The signal passes through the shaping filter, REC FSN, RC DEMOD, and EIA driver to terminal SCF. The local copy option does not have to be installed because an S1A switch contact makes one input to the CA switch low, producing a high level at terminal E20, which enables the EIA driver if local copy is not selected. The shaping filter signal also passes through the equalizer, but is rejected by the FRN.

9.25 In the local self-test mode with reverse channel, terminals SCA and SCF are made inoperative. With IC3 and IC4 in the test mode, a 387-Hz squarewave, on-off modulated at 4.3 b/s, is supplied at RCTOUTX, filtered by the XMIT FSN, and supplied to the shaping filter. The result is a reverse channel signal level of -2 dBm at the input of the equalizer. The FRN must reject this signal for the set to pass self-test.

9.26 In the remote test mode the same reverse channel states are established as in local self-test. The reverse channel signal is transmitted over the 2-wire line at a level of -7 dBm together with the primary channel signal. The looped-back level to the input of the FRN is reduced by hybrid action (see 10.04) to approximately -20 dBm for the reverse channel signal and -18 dBm for the primary channel signal with T1 terminated in 600 ohms. The transmitted signal may be monitored at the serving test center to verify proper reverse channel transmit operation.

9.27 A tone transmitted from the data test center to the data set in the remote test mode, causes errors to occur in the looped back signal. The reverse channel modulator turns off and constant spacing (2200 Hz) from PTDX is transmitted. Proper reverse channel receive operation is verified by sending a 387-Hz tone from the test center which is demodulated, making the RC DEMOD output high and the RCRX input of IC4 low. Constant marking (1200 Hz) is transmitted in a properly operating data set.

10. 202T-L1A TRANSMITTER-RECEIVER CIRCUIT - CPS1B

POWER SUPPLY, MOS LSI CIRCUITS, LINE TRANSFORMERS, AND SHAPING FILTER

10.01 The descriptions of the power supply, the MOS LSI circuits, the line transformers, and the shaping filter (see 3.01 through 3.10) apply to data set 202T-L1A as well as data set 202T-L1 with the exception that in 3.08, resistors R17 and R25 should be R27 and R32, and surge rated diodes CR8 and CR9 should be CR6 and CR7. In 3.10, R15, R16, and C7 should be R56, R57, and C23.

EQUALIZER

10.02 The compromise equalizer is composed of two second-order stages that provide slope equalization with a low-pass filter and delay equalization with an all-pass filter. A second all-pass section in the path of the FRN insertion point helps to compensate for the delay distortion caused by the FRN when reverse channel is installed. The filters are realized using a single amplifier biquadratic-type realization for the low-pass filter and a Sallen-Key type realization for the all-pass filters.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 All circuits in data set 202T type and the 39A1 and 40B1 data mountings are designed to work in an ambient temperature of 40° to 120°F and a relative humidity of 20 to 95 percent.

1.02 The power supply transformers require a source of 105 to 129 volts rms at 57 to 63 Hz.

1.03 The output level of the data set is 0 dBm.

1.04 The input level to the data set should be in the range from 0 to -32 dBm.

2. FUNCTIONAL DESIGNATIONS

2.01 The customer connector leads with the single set housing or the 40B1 data mounting are designated as follows:

Pin No.	Designation	Meaning
1	AA	Frame Ground
2	BA	Transmitted Data
3	BB	Received Data
4	CA	Request-to-Send
5	CB	Clear-to-Send
6	CC	Data Set Ready
7	AB	Signal Ground
8	CF	Received Line Signal Detector
9	+P	+14 Volts dc
10	-P	-14 Volts dc
11	SCA1	Secondary Request-to-Send
12	SCF	Secondary Received Line Signal Detector
19	SCA	Secondary Request-to-Send
25	CR	Carrier Detector Reset

2.02 The telephone connector leads with the single set housing are designated as follows:

Pin No.	Designation	Meaning
7	DT1	Data Tip 1
8	DR1	Data Ring 1
9	DT	Data Tip
10	DR	Data Ring
11	TEK6	Data Set Ready Control From DAS 828 or 829 Type
13	TEK5	Data Set Ready Control From DAS 828 or 829 Type

2.03 See SD-1D243-01 for the telephone connector lead designations for the 40B1 data mounting.

3. FUNCTIONS

3.01 Provides asynchronous transmission and reception of binary serial data at speeds up to 1800 b/s over 2- or 4-wire private line facilities.

3.02 Provides an analog loop test mode to check the transmitter and receiver operation while off-line from the customer interface.

3.03 Provides a local self-test mode to automatically check the transmitter and receiver operation with the exception of the customer interface circuitry while off-line.

3.04 Provides a remote test mode in 2-wire operation to check the transmitter and receiver operation with the exception of the customer interface circuitry from a serving test center.

3.05 Provides a remote test mode in 4-wire operation which connects the output of the demodulator to the input of the modulator to permit a loopback test from the serving test center.

4. CONNECTING CIRCUITS

4.01 The following data sets are compatible with data set 202T type:

(a) Data Set 202D Type - SD-1D049-01

(b) Data Set 202E Type - SD-1D078-01

(c) Data Set 202M Type - SD-1D169-01

(d) Data Set 202P Type - SD-1D224-01.

4.02 Data set 202T type will function with the following data auxiliary sets:

(a) Data Auxiliary Set 828A - SD-1D225-01.

(b) Data Auxiliary Set 828C - SD-1D233-01.

(c) Data Auxiliary Set 829 - SD-1D247-01.

5. MANUFACTURING TESTING REQUIREMENTS

5.01 The manufacturing test requirements are found in specification X-18012. They are supplemented by the provisions of X-18265, Reliability Screening for Data Products.

SECTION IV - REASONS FOR REISSUE

CHANGES

D.1 Data set 202T-L1A replaces data set 202T-L1.

D.2 Reverse channel JY4 must be used with data set 202T-L1A and replaces reverse channel JY2.

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